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LTC3859A

Low I_Q, Triple Output, Buck/Buck/Boost Synchronous Controller with Improved Burst Mode Operation

FEATURES

- **Dual Buck Plus Single Boost Synchronous Controllers**
- **Outputs Remain in Regulation Through Cold Crank Down to 2.5V**
- **Low Operating I_Q: 55μA (One Channel On)**
- **Wide Bias Input Voltage Range: 4.5V to 38V**
- **Buck Output Voltage Range: 0.8V ≤ V_{OUT} ≤ 24V**
- **Boost Output Voltage Up to 60V**
- **R_{SENSE} or DCR Current Sensing**
- **100% Duty Cycle for Boost Synchronous MOSFET Even in Burst Mode® Operation**
- Phase-Lockable Frequency (75kHz to 850kHz)
- Programmable Fixed Frequency (50kHz to 900kHz)
- Selectable Continuous, Pulse-Skipping or Low Ripple Burst Mode Operation at Light Loads
- Very Low Buck Dropout Operation: 99% Duty Cycle
- Adjustable Output Voltage Soft-Start or Tracking
- Low Shutdown I_Q: 14μA
- Small 38-Pin 5mm × 7mm QFN and TSSOP Packages

APPLICATIONS

- Automotive Always-On and Start-Stop Systems
- Battery Operated Digital Devices
- Distributed DC Power Systems
- Multioutput Buck-Boost Applications

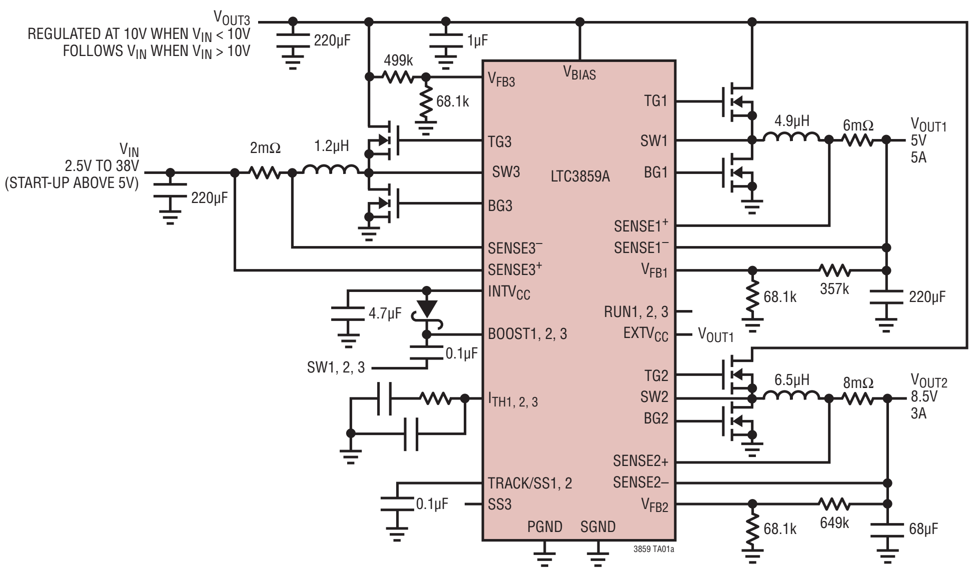
DESCRIPTION

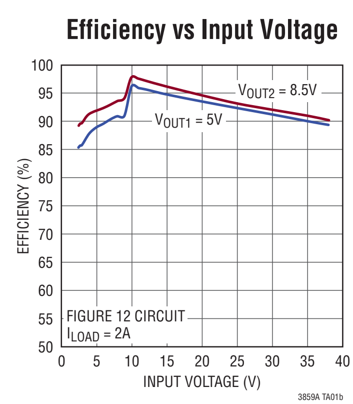
The LTC®3859A is a high performance triple output (buck/buck/boost) synchronous DC/DC switching regulator controller that drives all N-channel power MOSFET stages. Constant frequency current mode architecture allows a phase-lockable switching frequency of up to 850kHz. The LTC3859A operates from a wide 4.5V to 38V input supply range. When biased from the output of the boost converter or another auxiliary supply, the LTC3859A can operate from an input supply as low as 2.5V after start-up.

The 55μA no-load quiescent current extends operating runtime in battery powered systems. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC3859A features a precision 0.8V reference for the bucks, 1.2V reference for the boost and a power good output indicator. The PLLIN/MODE pin selects among Burst Mode operation, pulse-skipping mode, or continuous inductor current mode at light loads.

Compared to the LTC3859, the LTC3859A's boost controller has improved performance in Burst Mode operation when the input voltage is higher than the regulated output voltage.

TYPICAL APPLICATION

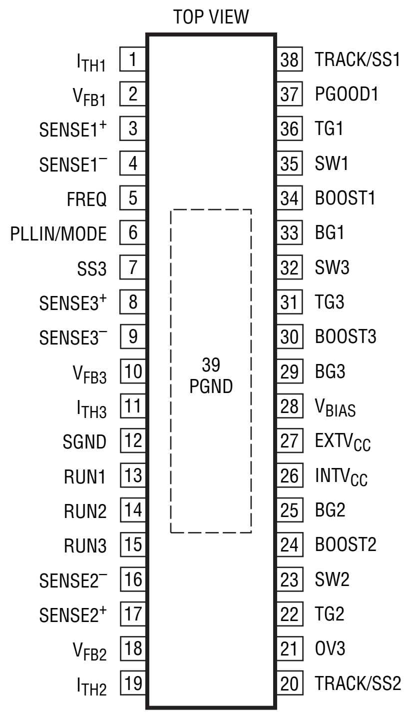




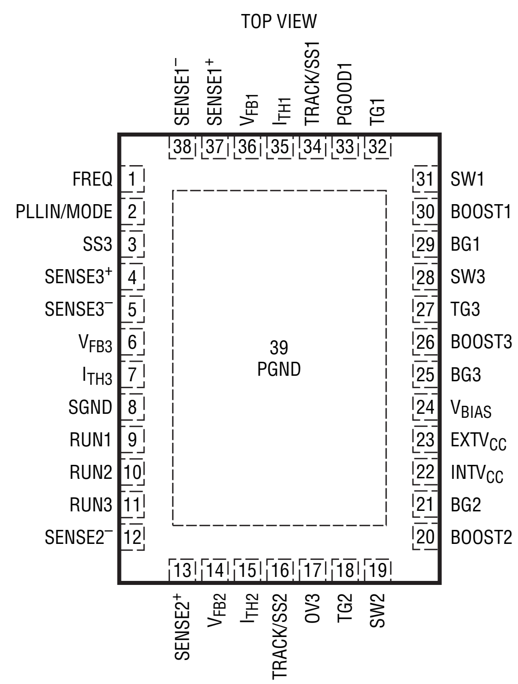
ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

Bias Input Supply Voltage (V_{BIAS}) .... –0.3V to 40V
Buck Top Side Driver Voltages
(BOOST1, BOOST2) .... –0.3V to 46V
Boost Top Side Driver Voltages
(BOOST3) .... –0.3V to 76V
Buck Switch Voltage (SW1, SW2) .... –5V to 40V
Boost Switch Voltage (SW3) .... –5V to 70V
$INTV_{CC}$, (BOOST1–SW1),
(BOOST2–SW2), (BOOST3–SW3), ... –0.3V to 6V
RUN1, RUN2, RUN3 .... –0.3V to 8V
Maximum Current Sourced Into Pin
from Source >8V 100µA
$SENSE1^+$, $SENSE2^+$, $SENSE1^-$
$SENSE2^-$ Voltages .... –0.3V to 28V
$SENSE3^+$, $SENSE3^-$ Voltages .... –0.3V to 40V
FREQ Voltages .... –0.3V to $INTV_{CC}$
$EXTV_{CC}$ .... –0.3V to 14V
I_{TH1}, I_{TH2}, I_{TH3}, V_{FB1}, V_{FB2}, V_{FB3} Voltages .... –0.3V to 6V
PLLIN/MODE, PGOOD1, OV3 Voltages .... –0.3V to 6V
TRACK/SS1, TRACK/SS2, SS3 Voltages ..... –0.3V to 6V
Operating Junction Temperature Range (Note 2)
LTC3859AE, LTC3859AI..................... –40°C to 125°C
LTC3859AH....................................... –40°C to 150°C
LTC3859AMP.................................... –55°C to 150°C
Storage Temperature Range .... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 34.7°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3859A#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3859AEFE#PBF	LTC3859AEFE#TRPBF	LTC3859AFE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3859AIFE#PBF	LTC3859AIFE#TRPBF	LTC3859AFE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3859AHFE#PBF	LTC3859AHFE#TRPBF	LTC3859AFE	38-Lead Plastic TSSOP	–40°C to 150°C
LTC3859AMPFE#PBF	LTC3859AMPFE#TRPBF	LTC3859AFE	38-Lead Plastic TSSOP	–55°C to 150°C
LTC3859AEUHF#PBF	LTC3859AEUHF#TRPBF	3859A	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3859AIUHF#PBF	LTC3859AIUHF#TRPBF	3859A	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3859AHUHF#PBF	LTC3859AHUHF#TRPBF	3859A	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 150°C
LTC3859AMPUHF#PBF	LTC3859AMPUHF#TRPBF	3859A	38-Lead (5mm × 7mm) Plastic QFN	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{BIAS} = 12V, $V_{RUN1,2,3}$ = 5V, $EXTV_{CC}$ = 0V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BIAS}	Bias Input Supply Operating Voltage Range			4.5		38	V
$V_{FB1,2}$	Buck Regulated Feedback Voltage	(Note 4); $I_{TH1,2}$ Voltage = 1.2V					
		–40°C to 85°C, All Grades		0.792	0.800	0.808	V
		LTC3859AE, LTC3859AI	●	0.788	0.800	0.812	V
		LTC3859AH, LTC3859AMP	●	0.786	0.800	0.812	V
V_{FB3}	Boost Regulated Feedback Voltage	(Note 4); I_{TH3} Voltage = 1.2V					
		–40°C to 85°C, All Grades		1.188	1.200	1.212	V
		LTC3859AE, LTC3859AI	●	1.182	1.200	1.218	V
		LTC3859AH, LTC3859AMP	●	1.179	1.200	1.218	V
$I_{FB1,2,3}$	Feedback Current	(Note 4)			–10	±50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	(Note 4); V_{IN} = 4V to 38V			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4)					
		Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V	●		0.01	0.1	%
		Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 2V	●		–0.01	–0.1	%
$g_{m1,2,3}$	Transconductance Amplifier g_m	(Note 4); $I_{TH1,2,3}$ = 1.2V; Sink/Source 5μA			2		mmho

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{BIAS} = 12V, $V_{RUN1,2,3}$ = 5V, $EXTV_{CC}$ = 0V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Input DC Supply Current	(Note 5)					
	Pulse-Skipping or Forced Continuous Mode (One Channel On)	RUN1 = 5V and RUN2,3 = 0V or RUN2 = 5V and RUN1,3 = 0V or RUN3 = 5V and RUN1,2 = 0V $V_{FB1,2}$ ON = 0.83V (No Load) V_{FB3} = 1.25V			1.5		mA
	Pulse-Skipping or Forced Continuous Mode (All Channels On)	RUN1,2,3 = 5V, $V_{FB1,2}$ = 0.83V (No Load) V_{FB3} = 1.25V			3		mA
	Sleep Mode (One Channel On, Buck)	RUN1 = 5V and RUN2,3 = 0V or RUN2 = 5V and RUN1,3 = 0V $V_{FB,ON}$ = 0.83V (No Load)			55	80	µA
	Sleep Mode (One Channel On, Boost)	RUN3 = 5V and RUN1,2 = 0V V_{FB3} = 1.25V			55	80	µA
	Sleep Mode (Buck and Boost Channel On)	RUN1 = 5V and RUN2 = 0V or RUN2 = 5V and RUN1 = 0V RUN3 = 5V $V_{FB1,2}$ = 0.83V (No Load) V_{FB3} = 1.25V			65	100	µA
	Sleep Mode (All Three Channels On)	RUN1,2,3 = 5V, $V_{FB1,2}$ = 0.83V (No Load) V_{FB3} = 1.25V			80	120	µA
	Shutdown	RUN1,2,3 = 0V			14	30	µA
UVLO	Undervoltage Lockout	$INTV_{CC}$ Ramping Up	●		4.15	4.5	V
		$INTV_{CC}$ Ramping Down	●	3.5	3.8	4.0	V
$V_{OVL1,2}$	Buck Feedback Overvoltage Protection	Measured at $V_{FB1,2}$ Relative to Regulated $V_{FB1,2}$		7	10	13	%
$I_{SENSE1,2+}$	SENSE⁺ Pin Current	Bucks (Channels 1 and 2)				±1	µA
$I_{SENSE3+}$	SENSE⁺ Pin Current	Boost (Channel 3)			170		µA
$I_{SENSE1,2-}$	SENSE⁻ Pin Current	Bucks (Channels 1 and 2) $V_{OUT1,2} < V_{INTVCC} - 0.5V$ $V_{OUT1,2} > V_{INTVCC} + 0.5V$			 700	 ±2	 µA µA
$I_{SENSE3-}$	SENSE⁻ Pin Current	Boost (Channel 3) $V_{SENSE3+}$, $V_{SENSE3-}$ = 12V				±1	µA
$DF_{MAX,TG}$	Maximum Duty Factor for TG	Bucks (Channels 1,2) in Dropout, FREQ = 0V Boost (Channel 3) in Overvoltage		98	99 100		% %
$DF_{MAX,BG}$	Maximum Duty Factor for BG	Bucks (Channels 1,2) in Overvoltage Boost (Channel 3)			100 96		% %
$I_{TRACK/SS1,2}$	Soft-Start Charge Current	$V_{TRACK/SS1,2}$ = 0V		0.7	1.0	1.4	µA
I_{SS3}	Soft-Start Charge Current	V_{SS3} = 0V		0.7	1.0	1.4	µA
V_{RUN1} ON $V_{RUN2,3}$ ON	RUN1 Pin Threshold RUN2,3 Pin Threshold	V_{RUN1} Rising $V_{RUN2,3}$ Rising	● ●	1.19 1.23	1.25 1.28	1.31 1.33	V V
$V_{RUN1,2,3}$ Hyst	RUN Pin Hysteresis				80		mV
$V_{SENSE1,2,3(MAX)}$	Maximum Current Sense Threshold	$V_{FB1,2}$ = 0.7V, $V_{SENSE1,2-}$ = 3.3V $V_{FB1,2,3}$ = 1.1V, $V_{SENSE3+}$ = 12V	●	43	50	57	mV
$V_{SENSE3(CM)}$	SENSE3 Pins Common Mode Range (BOOST Converter Input Supply Voltage)			2.5		38	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{BIAS} = 12V, $V_{RUN1,2,3}$ = 5V, $EXTV_{CC}$ = 0V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver							
TG1,2	Pull-Up On-Resistance Pull-Down On-Resistance				2.5 1.5		Ω Ω
BG1,2	Pull-Up On-Resistance Pull-Down On-Resistance				2.4 1.1		Ω Ω
TG3	Pull-Up On-Resistance Pull-Down On-Resistance				1.2 1.0		Ω Ω
BG3	Pull-Up On-Resistance Pull-Down On-Resistance				1.2 1.0		Ω Ω
 TG1,2,3 t_r TG1,2,3 t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 16		 ns ns
 BG1,2,3 t_r BG1,2,3 t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 28 13		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver Bucks (Channels 1, 2) Boost (Channel 3)			30 70		ns ns
BG/TG t_{1D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver Bucks (Channels 1, 2) Boost (Channel 3)			30 70		ns ns
$t_{ON(MIN)1,2}$	Buck Minimum On-Time	(Note 7)			95		ns
$t_{ON(MIN)3}$	Boost Minimum On-Time	(Note 7)			120		ns
$INTV_{CC}$ Linear Regulator							
$V_{INTVCCVBIAS}$	Internal V_{CC} Voltage	6V < V_{BIAS} < 38V, V_{EXTVCC} = 0V, I_{INTVCC} = 0mA		5.0	5.4	5.6	V
$V_{LDOVBIAS}$	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V			0.7	2	%
$V_{INTVCCEXT}$	Internal V_{CC} Voltage	6V < V_{EXTVCC} < 13V, I_{INTVCC} = 0mA		5.0	5.4	5.6	V
V_{LDOEXT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 8.5V			0.7	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7		V
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				200		mV
Oscillator and Phase-Locked Loop							
f_{25k}	Programmable Frequency	R_{FREQ} = 25k; PLLIN/MODE = DC Voltage			115		kHz
f_{65k}	Programmable Frequency	R_{FREQ} = 65k; PLLIN/MODE = DC Voltage		375	440	505	kHz
f_{105k}	Programmable Frequency	R_{FREQ} = 105k; PLLIN/MODE = DC Voltage			835		kHz
f_{LOW}	Low Fixed Frequency	V_{FREQ} = 0V PLLIN/MODE = DC Voltage		320	350	380	kHz
f_{HIGH}	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$; PLLIN/MODE = DC Voltage		485	535	585	kHz
f_{SYNC}	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75		850	kHz
PGOOD1 Output							
V_{PGL1}	PGOOD1 Voltage Low	I_{PGOOD1} = 2mA			0.2	0.4	V
I_{PGOOD1}	PGOOD1 Leakage Current	V_{PGOOD1} = 5V				±1	μA
V_{PG1}	PGOOD1 Trip Level	V_{FB1} with Respect to Set Regulated Voltage V_{FB1} Ramping Negative		–13	–10	–7	%
		Hysteresis			2.5		%
		V_{FB1} Ramping Positive		7	10	13	%
		Hysteresis			2.5		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{BIAS} = 12V, $V_{RUN1,2,3}$ = 5V, $EXTV_{CC}$ = 0V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
T_{PG1}	Delay For Reporting a Fault				20		μs
OV3 Boost Overvoltage Indicator Output							
V_{OV3L}	OV3 Voltage Low	I_{OV3} = 2mA			0.2	0.4	V
I_{OV3}	OV3 Leakage Current	V_{OV3} = 5V				±1	μA
V_{OV}	OV3 Trip Level	V_{FB} With Respect to Set Regulated Voltage		6	10	13	%
		Hysteresis			1.5		%
BOOST3 Charge Pump							
I_{BST3}	BOOST3 Charge Pump Available Output Current	V_{BOOST3} = 16V; V_{SW3} = 12V; Forced Continuous Mode			65		μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3859A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3859AE is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3859AI is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3859AH is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3859AMP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} = 34°C/W for the QFN package and θ_{JA} = 25°C/W for the TSSOP package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The LTC3859A is tested in a feedback loop that servos $V_{ITH1,2,3}$ to a specified voltage and measures the resultant V_{FB}. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC3859AE/LTC3859AI, 150°C for the LTC3859AH/LTC3859AMP). For the LTC3859AMP, the specification at –40°C is not tested in production and is assured by design, characterization and correlation to production testing at –55°C.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥ 40% of I_{MAX} (See the Minimum On-Time Considerations in the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency and Power Loss vs Output Current (Buck)

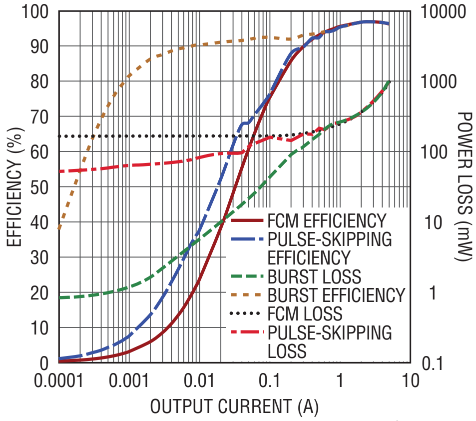
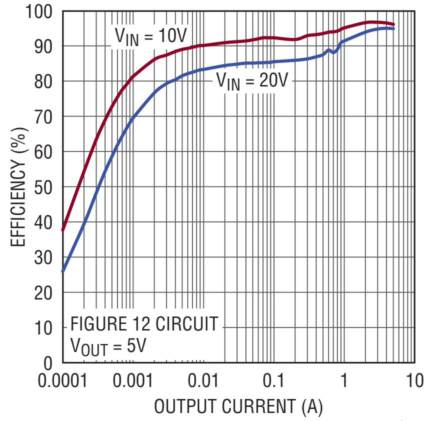
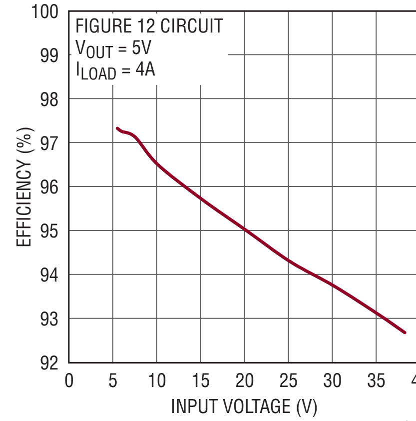


FIGURE 12 CIRCUIT
V_{IN} = 10V, V_{OUT} = 5V

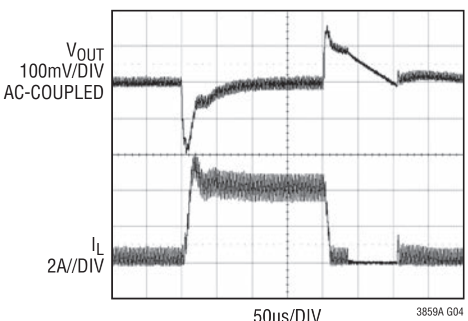
Efficiency vs Output Current (Buck)



Efficiency vs Input Voltage (Buck)

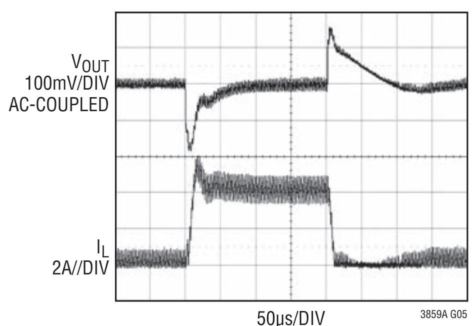


Load Step (Buck) Burst Mode Operation



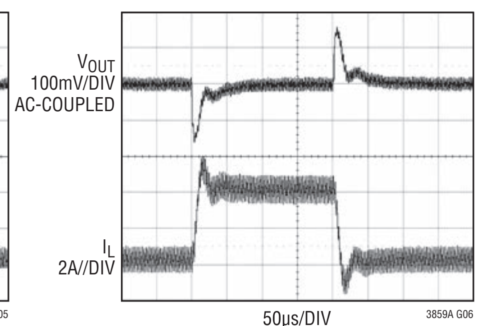
V_{IN} = 12V
V_{OUT} = 5V
FIGURE 12 CIRCUIT

Load Step (Buck) Pulse-Skipping Mode



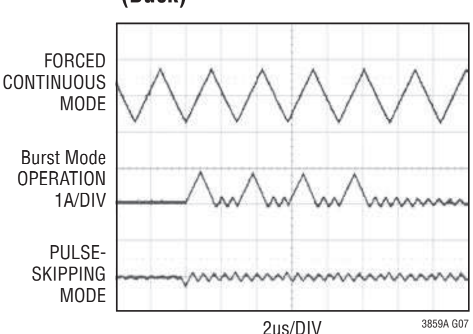
V_{IN} = 12V
V_{OUT} = 5V
FIGURE 12 CIRCUIT

Load Step (Buck) Forced Continuous Mode



V_{IN} = 12V
V_{OUT} = 5V
FIGURE 12 CIRCUIT

Inductor Current at Light Load (Buck)



V_{IN} = 10V
V_{OUT} = 5V
I_{LOAD} = 1mA
FIGURE 12 CIRCUIT

Soft Start-Up

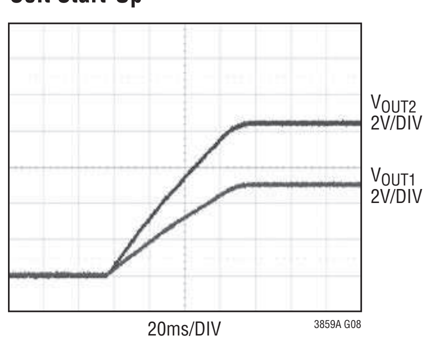
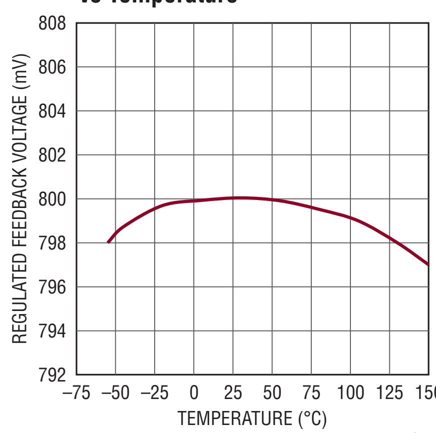


FIGURE 12 CIRCUIT

Buck Regulated Feedback Voltage vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency and Power Loss vs Output Current (Boost)

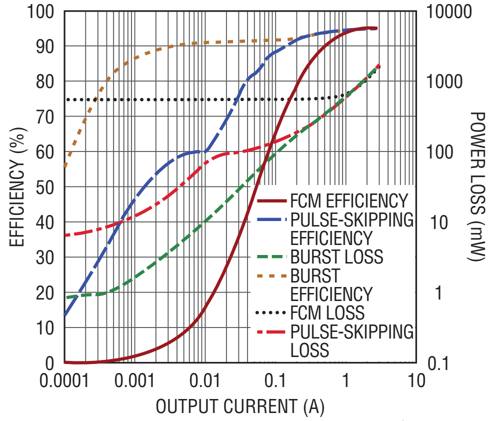
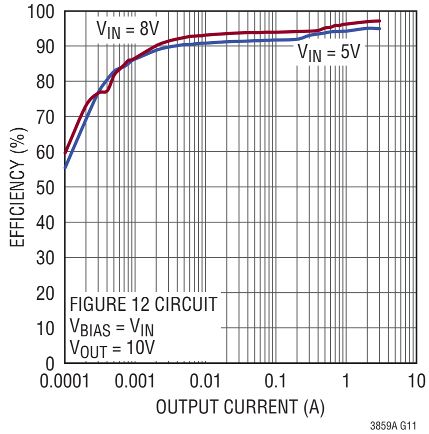
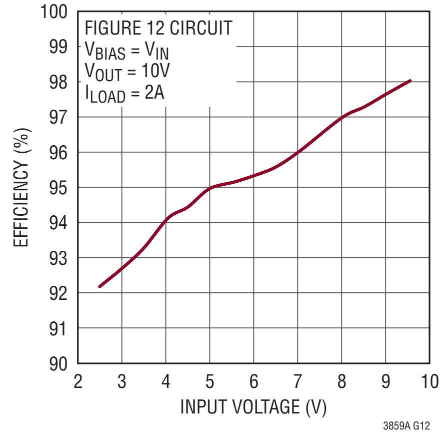


FIGURE 12 CIRCUIT
V_{IN} = 5V, V_{OUT} = 10V, V_{BIAS} = V_{IN}

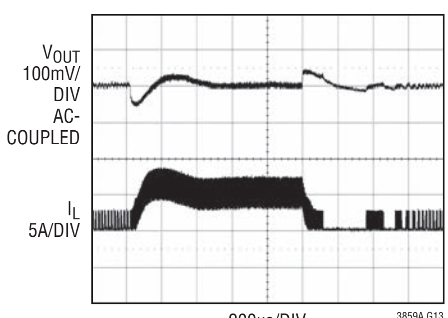
Efficiency vs Output Current (Boost)



Efficiency vs Input Voltage (Boost)

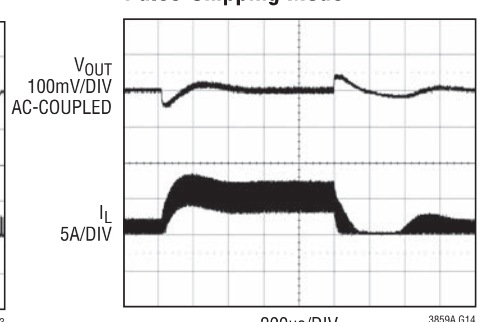


Load Step (Boost) Burst Mode Operation



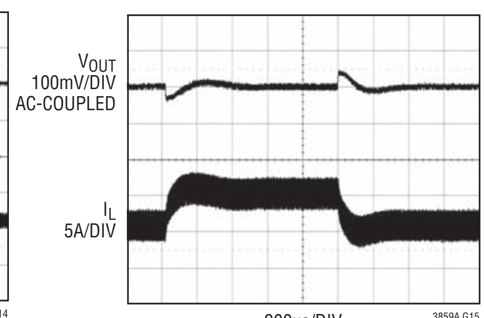
V_{OUT} = 10V
V_{IN} = 5V
FIGURE 12 CIRCUIT

Load Step (Boost) Pulse-Skipping Mode



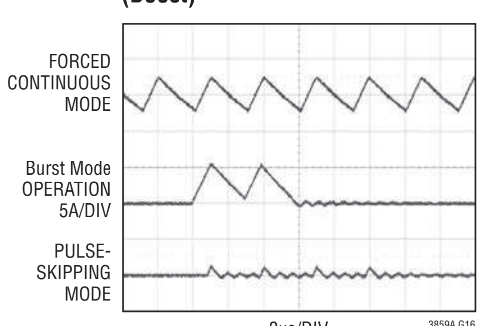
V_{OUT} = 10V
V_{IN} = 5V
FIGURE 12 CIRCUIT

Load Step (Boost) Forced Continuous Mode



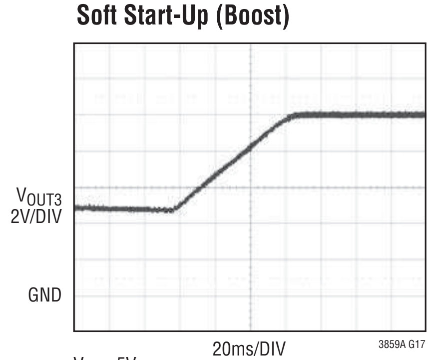
V_{OUT} = 10V
V_{IN} = 5V
FIGURE 12 CIRCUIT

Inductor Current at Light Load (Boost)



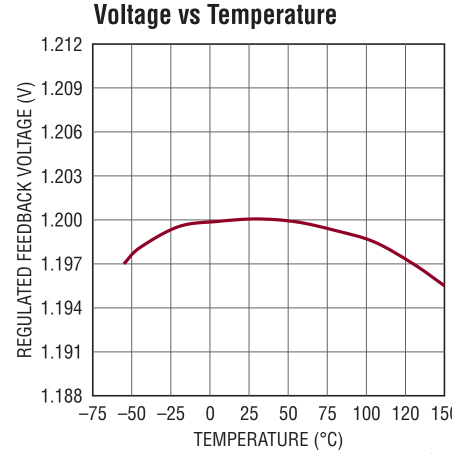
V_{OUT} = 10V
V_{IN} = 7V
I_{LOAD} = 1mA
FIGURE 12 CIRCUIT

Soft Start-Up (Boost)



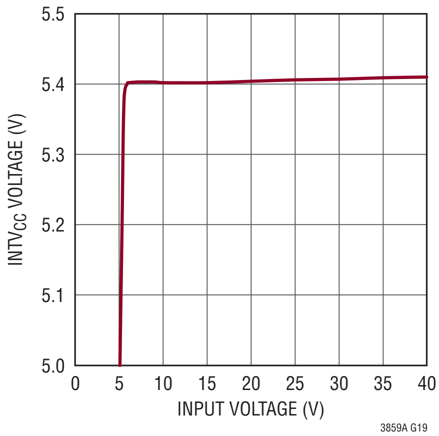
V_{IN} = 5V
FIGURE 12 CIRCUIT

Boost Regulated Feedback Voltage vs Temperature

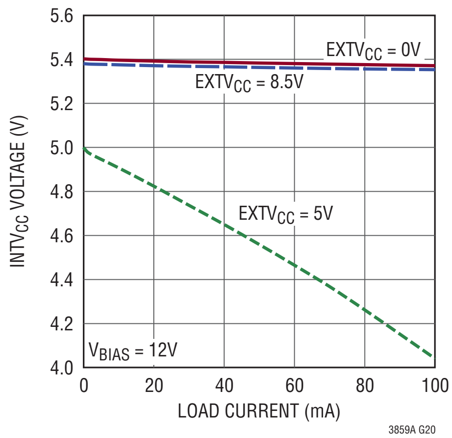


TYPICAL PERFORMANCE CHARACTERISTICS

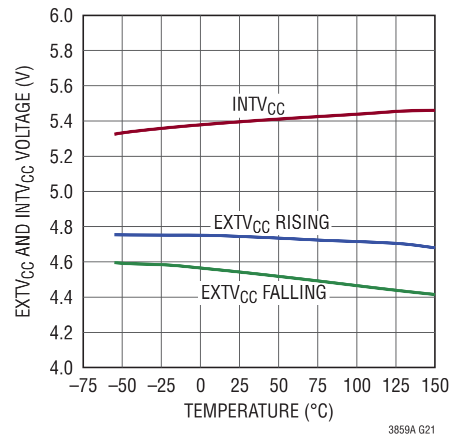
$INTV_{CC}$ Line Regulation



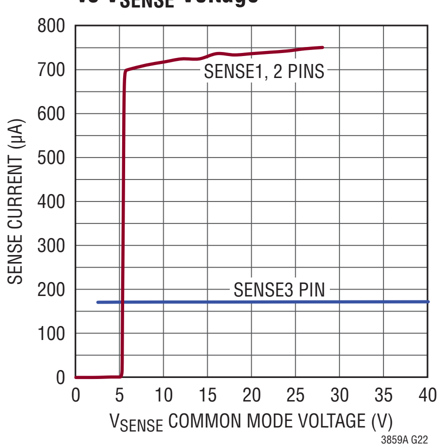
$INTV_{CC}$ and $EXTV_{CC}$ vs Load Current



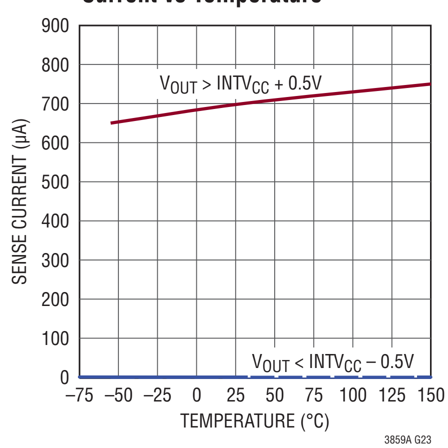
$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltages vs Temperature



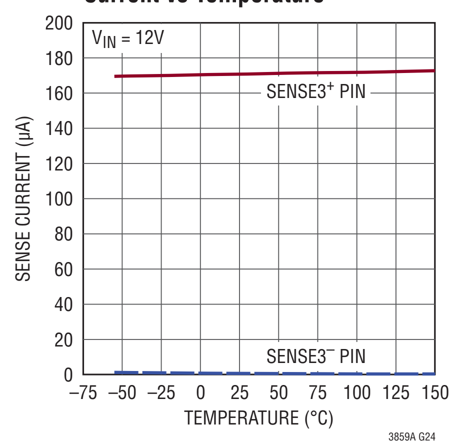
SENSE Pins Total Input Current vs V_{SENSE} Voltage



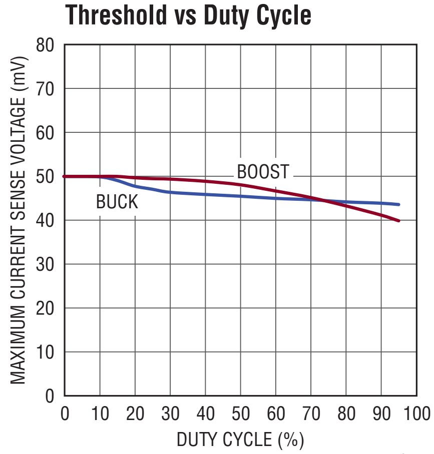
Buck $SENSE^{–}$ Pin Input Bias Current vs Temperature



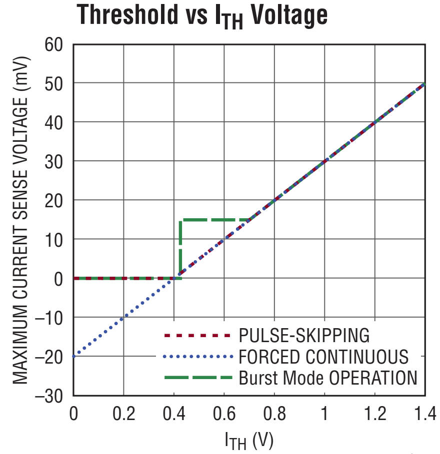
Boost SENSE Pin Total Input Current vs Temperature



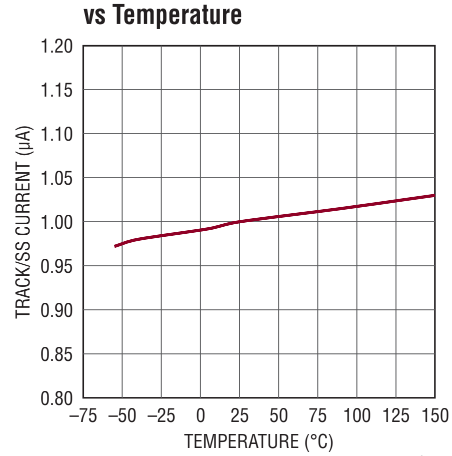
Maximum Current Sense Threshold vs Duty Cycle



Maximum Current Sense Threshold vs I_{TH} Voltage

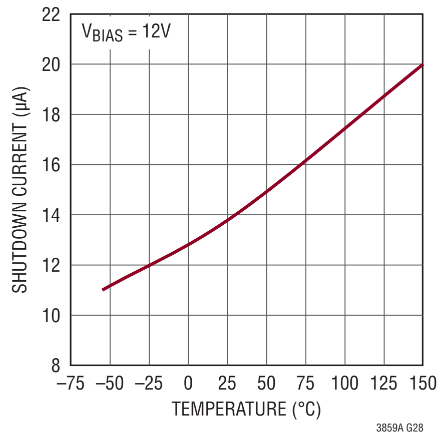


TRACK/SS Pull-Up Current vs Temperature

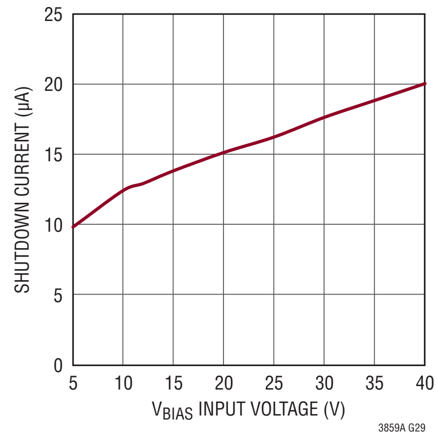


TYPICAL PERFORMANCE CHARACTERISTICS

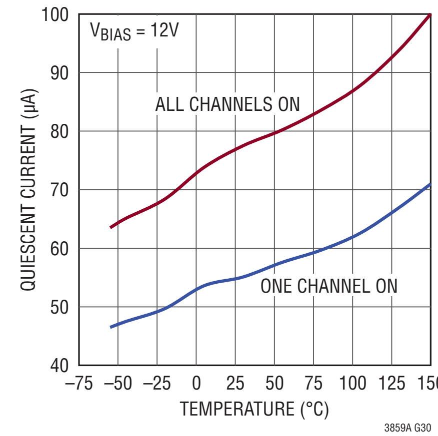
Shutdown Current vs Temperature



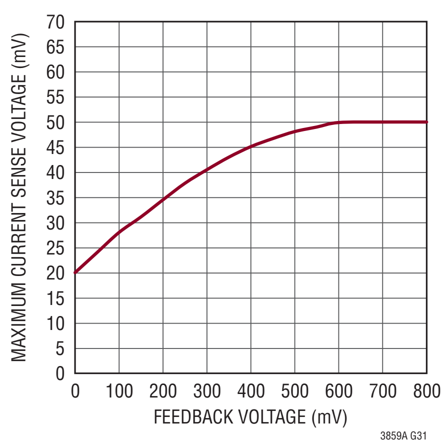
Shutdown Current vs Input Voltage



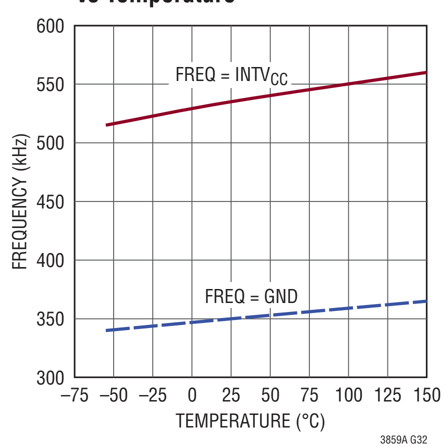
Quiescent Current vs Temperature



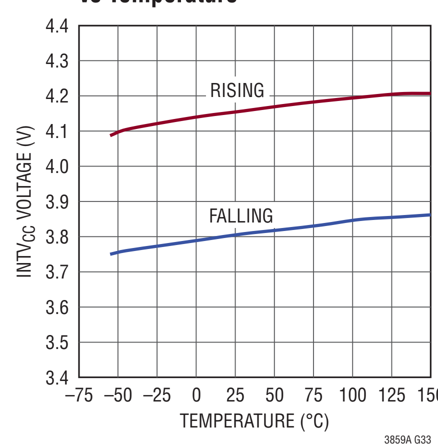
Buck Foldback Current Limit



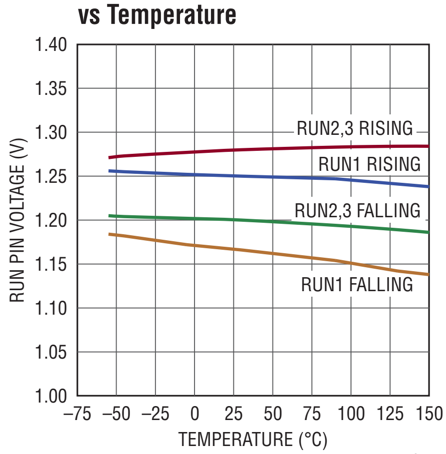
Oscillator Frequency vs Temperature



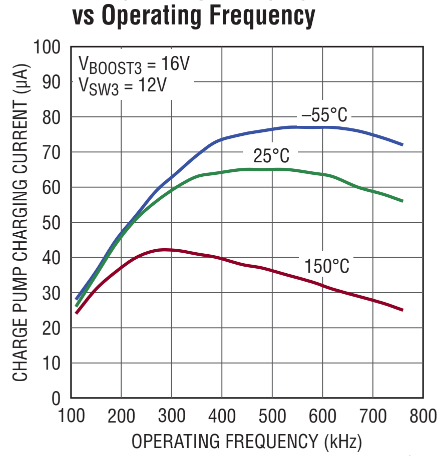
Undervoltage Lockout Threshold vs Temperature



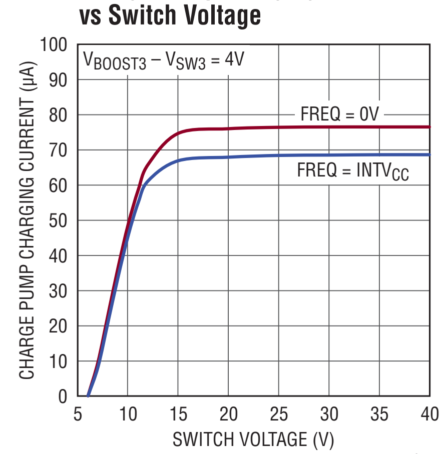
Shutdown (RUN) Threshold vs Temperature



Charge Pump Charging Current vs Operating Frequency



Charge Pump Charging Current vs Switch Voltage



PIN FUNCTIONS (QFN/TSSOP)

FREQ (Pin 1/Pin 5): The Frequency Control Pin for the Internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed using a resistor between FREQ and GND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency.

PLLIN/MODE (Pin 2/Pin 6): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, the phase-locked loop will force the rising TG1 signal to be synchronized with the rising edge of the external clock, and the regulators operate in forced continuous mode. When not synchronizing to an external clock, this input, which acts on all three controllers, determines how the LTC3859AA operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation. This can be done by connecting a 100k resistor from this pin to $INTV_{CC}$.

SGND (Pin 8/Pin 12): Small Signal Ground common to all three controllers, must be routed separately from high current grounds to the common (–) terminals of the C_{IN} capacitors.

RUN1, RUN2, RUN3 (Pins 9, 10, 11/Pins 13, 14, 15): Digital Run Control Inputs for Each Controller. Forcing RUN1 below 1.17V and RUN2/RUN3 below 1.20V shuts down that controller. Forcing all of these pins below 0.7V shuts down the entire LTC3859A, reducing quiescent current to approximately 14µA.

OV3 (Pin 17/Pin 21): Overvoltage Open-Drain Logic Output for the Boost Regulator. OV3 is pulled to ground when the voltage on the V_{FB3} pin is under 110% of its set point, and becomes high impedance when V_{FB3} goes over 110% of its set point.

$INTV_{CC}$ (Pin 22/Pin 26): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to PGND with a minimum of 4.7µF ceramic or tantalum capacitor.

$EXTV_{CC}$ (Pin 23/Pin 27): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{BIAS} whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not float or exceed 14V on this pin.

V_{BIAS} (Pin 24/Pin 28): Main Bias Input Supply Pin. A bypass capacitor should be tied between this pin and the SGND pin.

BG1, BG2, BG3 (Pins 29, 21, 25/Pins 33, 25, 29): High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

BOOST1, BOOST2, BOOST3 (Pins 30, 20, 26/Pins 34, 24, 30): Bootstrapped Supplies to the Top Side Floating Drivers. Capacitors are connected between the BOOST and SW pins and Schottky diodes are tied between the BOOST and $INTV_{CC}$ pins. Voltage swing at the BOOST pins is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

SW1, SW2, SW3 (Pins 31, 19, 28/Pins 35, 23, 32): Switch Node Connections to Inductors.

TG1, TG2, TG3 (Pins 32, 18, 27/Pins 36, 22, 31): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

PGOOD1 (Pin 33/Pin 37): Open-Drain Logic Output. PGOOD1 is pulled to ground when the voltage on the V_{FB1} pin is not within ±10% of its set point.

PIN FUNCTIONS (QFN/TSSOP)

TRACK/SS1, TRACK/SS2, SS3 (Pins 34, 16, 3/Pins 38, 20, 7): External Tracking and Soft-Start Input. For the buck channels, the LTC3859A regulates the $V_{FB1,2}$ voltage to the smaller of 0.8V, or the voltage on the TRACK/SS1, 2 pin. For the boost channel, the LTC3859A regulates the V_{FB3} voltage to the smaller of 1.2V, or the voltage on the SS3 pin. An internal 1µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to the TRACK/SS pins of the buck channels allow the LTC3859A buck outputs to track the other supply during start-up.

I_{TH1}, I_{TH2}, I_{TH3} (Pins 35, 15, 7/Pins 1, 19, 11): Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage.

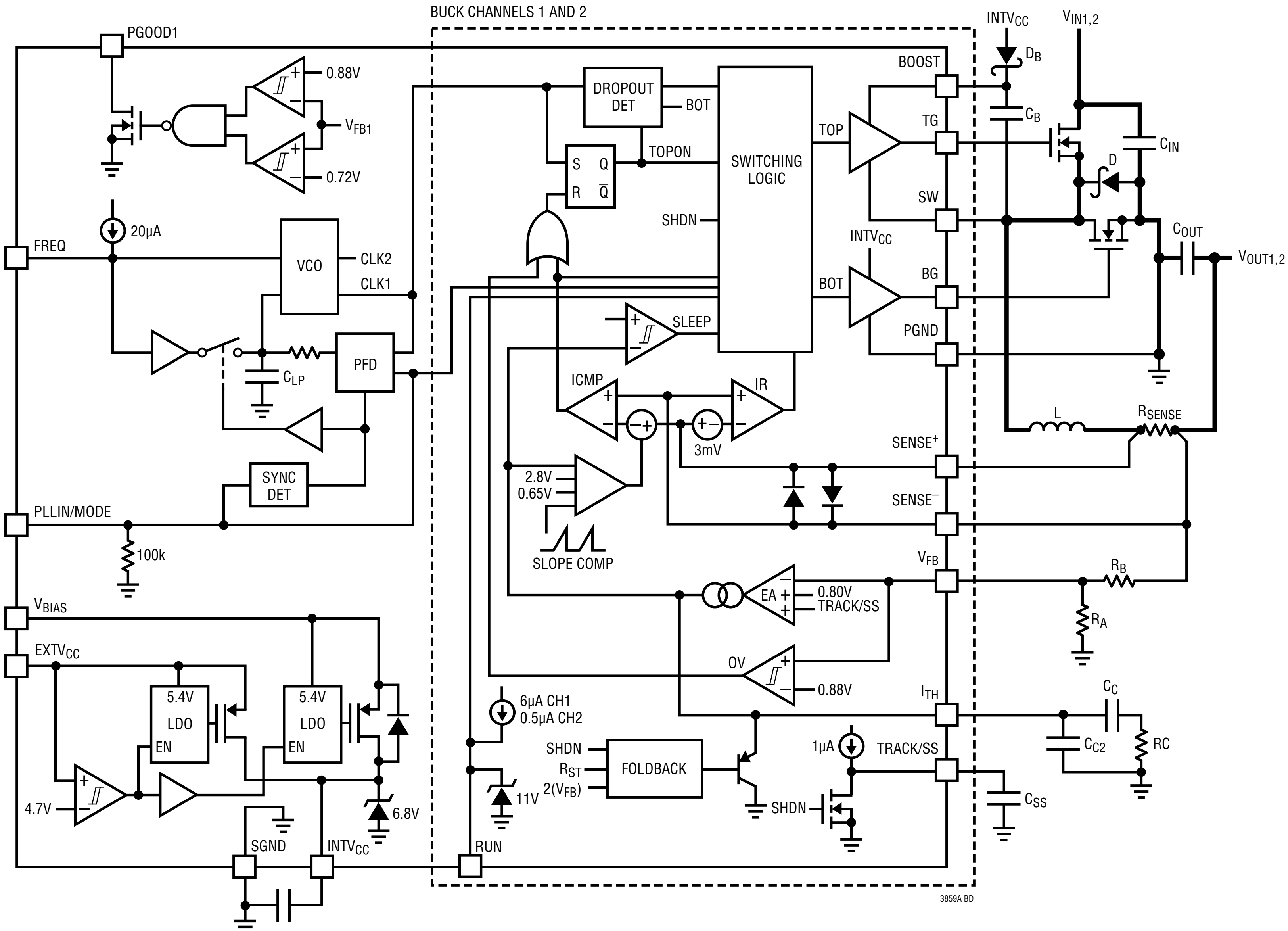
V_{FB1}, V_{FB2}, V_{FB3} (Pins 36, 14, 6/Pins 2, 18, 10): Receives the remotely sensed feedback voltage for each controller from an external resistive divider across the output.

SENSE1$^+$, SENSE2$^+$, SENSE3$^+$ (Pins 37, 13, 4/Pins 3, 17, 8): The (+) Input to the Differential Current Comparators. The I_{TH} pin voltage and controlled offsets between the SENSE$^-$ and SENSE$^+$ pins in conjunction with R_{SENSE} set the current trip threshold. For the boost channel, the SENSE3$^+$ pin supplies current to the current comparator.

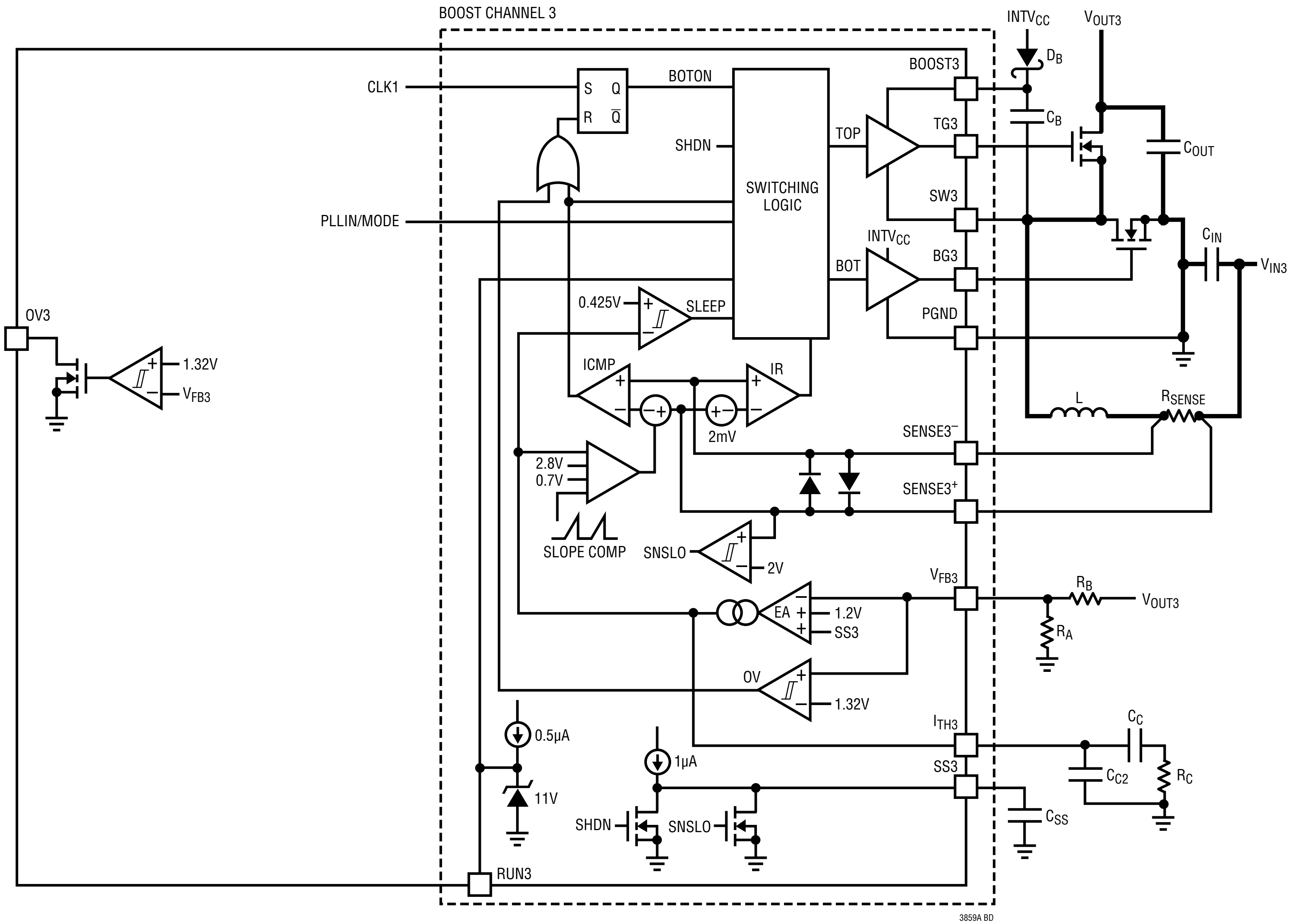
SENSE1$^-$, SENSE2$^-$, SENSE3$^-$ (Pins 38, 12, 5/Pins 4, 16, 9): The (–) Input to the Differential Current Comparators. When SENSE1,2$^-$ for the buck channels is greater than $INTV_{CC}$, then SENSE1,2$^-$ pin supplies current to the current comparator.

PGND (Exposed Pad Pin 39): Driver Power Ground. Connects to the sources of bottom N-channel MOSFETs and the (–) terminal(s) of C_{IN}. The exposed pad must be soldered to the PCB for rated electrical and thermal performance.

FUNCTIONAL DIAGRAM



FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3859A uses a constant frequency, current mode step-down architecture. The two buck controllers, channels 1 and 2, operate 180 degrees out of phase with each other. The boost controller, channel 3, operates in phase with channel 1. During normal operation, the external top MOSFET for the buck channels (the external bottom MOSFET for the boost channel) is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin, (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.800V reference voltage for the bucks (1.2V reference voltage for the boost). When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the I_{TH} voltage until the average inductor current matches the new load current.

After the top MOSFET for the bucks (the bottom MOSFET for the boost) is turned off each cycle, the bottom MOSFET is turned on (the top MOSFET for the boost) until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

$INTV_{CC}$/$EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, the V_{BIAS} LDO (low dropout linear regulator) supplies 5.4V from V_{BIAS} to $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.7V, the V_{BIAS} LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies 5.4V from $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as one of the LTC3859A switching regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each cycle through an external diode when the switch voltage goes low.

For buck channels 1 and 2, if the buck's input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one twelfth of the clock period every tenth cycle to allow C_B to recharge.

Shutdown and Start-Up (RUN1, RUN2, RUN3 and TRACK/SS1, TRACK/SS2, SS3 Pins)

The three channels of the LTC3859A can be independently shut down using the RUN1, RUN2 and RUN3 pins. Pulling RUN1 below 1.17V and RUN2/RUN3 below 1.20V shuts down the main control loop for that channel. Pulling all three pins below 0.7V disables all controllers and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC3859A draws only 14μA of quiescent current.

Releasing a RUN pin allows a small internal current to pull up the pin to enable that controller. The RUN1 pin has a 6μA pull-up current while the RUN2 and RUN3 pins have a smaller 0.5μA. The 6μA current on RUN1 is designed to be large enough so that the RUN1 pin can be safely floated (to always enable the controller) without worry of condensation or other small board leakage pulling the pin down. This is ideal for always-on applications where one or more controllers are enabled continuously and never shut down.

Each RUN pin may also be externally pulled up or driven directly by logic. When driving a RUN pin with a low impedance source, do not exceed the absolute maximum rating of 8V. Each RUN pin has an internal 11V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, V_{BIAS}), so long as the maximum current in the RUN pin does not exceed 100μA.

The start-up of each channel's output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, TRACK/SS2 for channel 2, SS3 for channel 3). When the voltage on the TRACK/SS pin is less than the 0.8V internal reference for the bucks and the 1.2V internal

OPERATION

reference for the boost, the LTC3859A regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the corresponding reference voltage. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to SGND. An internal 1µA pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V/1.2V (and beyond up to $INTV_{CC}$), the output voltage V_{OUT} rises smoothly from zero to its final value.

Alternatively the TRACK/SS pins for buck channels 1 and 2 can be used to cause the start-up of V_{OUT} to track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section).

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping, or Continuous Conduction) (PLLIN/MODE Pin)

The LTC3859A can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground. To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V.

When a controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of the maximum sense voltage (30% for the boost) even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier EA will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The I_{TH} pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3859A draws. If one channel is in sleep mode and the other two are shut down, the LTC3859A draws only 55µA of quiescent current. If two channels are in sleep mode and the other shut down, it draws only 65µA of quiescent current. If all three controllers are enabled in sleep mode, the LTC3859A draws only 80µA of quiescent. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the I_{TH} pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the bottom external MOSFET (the top external MOSFET for the boost) just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation or clocked by an external clock source to use the phase-locked loop (see the Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3859A operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

OPERATION

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3859A's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to SGND, tied to $INTV_{CC}$, or programmed through an external resistor. Tying FREQ to SGND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and SGND allows the frequency to be programmed between 50kHz and 900kHz.

A phase-locked loop (PLL) is available on the LTC3859A to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC3859A's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of controller 1's external top MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external top MOSFET is 180 degrees out of phase to the rising edge of the external clock source.

The VCO input voltage is pre-biased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of TG1. The ability to pre-bias the loop filter allows the PLL to lock in rapidly without deviating far from the desired frequency.

The typical capture range of the LTC3859A's phase-locked loop is from approximately 55kHz to 1MHz, with a guarantee over all manufacturing variations to be between 75kHz and 850kHz. In other words, the LTC3859A's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling).

Boost Controller Operation When $V_{IN} > V_{OUT}$

When the input voltage to the boost channel rises above its regulated V_{OUT} voltage, the controller can behave differently depending on the mode, inductor current and V_{IN} voltage. In forced continuous mode, the loop works to keep the top MOSFET on continuously once V_{IN} rises above V_{OUT}. An internal charge pump delivers current to the boost capacitor from the BOOST3 pin to maintain a sufficiently high TG voltage. (The amount of current the charge pump can deliver is characterized by two curves in the Typical Performance Characteristics section.)

In pulse-skipping mode, if V_{IN} is between 100% and 110% of the regulated V_{OUT} voltage, TG3 turns on if the inductor current rises above approximately 3% of the programmed I_{LIM} current. If the part is programmed in Burst Mode operation under this same V_{IN} window, then TG3 turns on at the same threshold current as long as the chip is awake (one of the buck channels is awake and switching). If both buck channels are asleep or shut down in this V_{IN} window, then TG3 will remain off regardless of the inductor current.

If V_{IN} rises above 110% of the regulated V_{OUT} voltage in any mode, the controller turns on TG3 regardless of the inductor current. In Burst Mode operation, however, the internal charge pump turns off if the entire chip is asleep (the two buck channels are asleep or shut down). With the charge pump off, there would be nothing to prevent the boost capacitor from discharging, resulting in an insufficient TG voltage needed to keep the top MOSFET completely on. The charge pump turns back on when the chip wakes up, and it remains on as long as one of the buck channels is actively switching.

Boost Controller at Low SENSE Pin Common Voltage

The current comparator of the boost controller is powered directly from the $SENSE3^+$ pin and can operate to voltages as low as 2.5V. Since this is lower than the V_{BIAS} UVLO of the chip, V_{BIAS} can be connected to the output of the boost controller, as illustrated in the typical application circuit in Figure 12. This allows the boost controller to handle input voltage transients down to 2.5V while maintaining output voltage regulation. If the $SENSE3^+$ rises back above 2.5V, the SS3 pin will be released initiating a new soft-start sequence.

OPERATION

Buck Controller Output Overvoltage Protection

The two buck channels have an overvoltage comparator that guards against transient overshoots as well as other more serious conditions that may overvoltage their outputs. When the $V_{FB1,2}$ pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Channel 1 Power Good (PGOOD1)

Channel 1 has a PGOOD1 pin that is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD1 pin low when the V_{FB1} pin voltage is not within ±10% of the 0.8V reference voltage for the buck channel. The PGOOD1 pin is also pulled low when the RUN1 pin is low (shut down). When the V_{FB1} pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V.

Boost Overvoltage Indicator (OV3)

The OV3 pin is an overvoltage indicator that signals whether the output voltage of the channel 3 boost controller goes over its programmed regulated voltage. The pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the OV3 pin low when the V_{FB3} pin voltage is less than 110% of the 1.2V reference voltage for the boost channel. The OV3 pin is also pulled low when the RUN3 pin is low (shut down). When the V_{FB3} pin voltage goes higher than 110% of the 1.2V reference, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V.

Buck Foldback Current

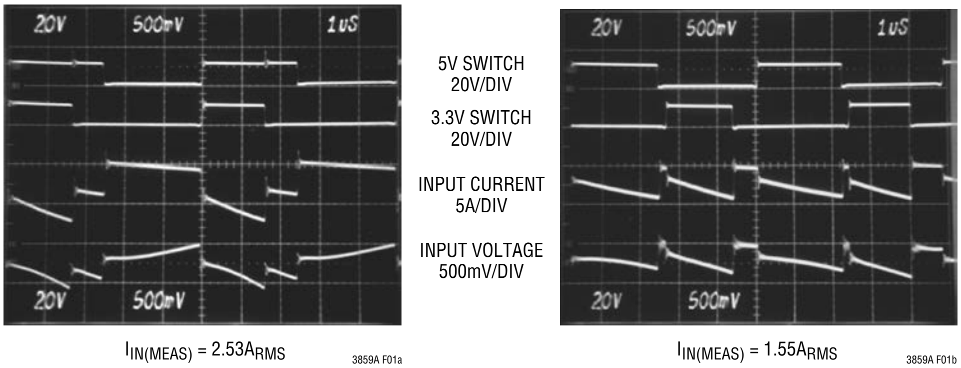
When the buck output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB} voltage is keeping up with the TRACK/SS1,2 voltage). There is no foldback current limiting for the boost channel.

THEORY AND BENEFITS OF 2-PHASE OPERATION

Why the need for 2-phase operation? Up until the 2-phase family, constant-frequency dual switching regulators operated both channels in phase (i.e., single-phase operation). This means that both switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor and battery. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor and battery.

With 2-phase operation, the two buck controllers of the LTC3859A are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by the switches, greatly reducing the overlap time where they add together. The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.

OPERATION



(a) (b)

Figure 1. Input Waveforms Comparing Single-Phase (a) and 2-Phase (b) Operation for Dual Switching Regulators Converting 12V to 5V and 3.3V at 3A Each. The Reduced Input Ripple with the 2-Phase Regulator Allows Less Expensive Input Capacitors, Reduces Shielding Requirements for EMI and Improves Efficiency

Figure 1 compares the input waveforms for a representative single-phase dual switching regulator to the 2-phase dual buck controllers of the LTC3859A. An actual measurement of the RMS input current under these conditions shows that 2-phase operation dropped the input current from 2.53A_{RMS} to 1.55A_{RMS}. While this is an impressive reduction in itself, remember that the power losses are proportional to I_{RMS2}, meaning that the actual power wasted is reduced by a factor of 2.66. The reduced input ripple voltage also means less power is lost in the input power path, which could include batteries, switches, trace/connector resistances and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles which, in turn, are dependent upon the input voltage V_{IN} (Duty Cycle = V_{OUT}/V_{IN}). Figure 2 shows how the RMS input current varies for single-phase and 2-phase operation for 3.3V and 5V regulators over a wide input voltage range.

It can readily be seen that the advantages of 2-phase operation are not just limited to a narrow operating range, for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

The schematic on the first page is a basic LTC3859A application circuit. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE} and the inductor value. Next, the power MOSFETs are selected. Finally, C_{IN} and C_{OUT} are selected.

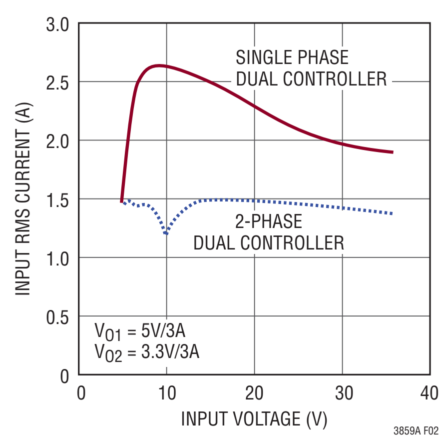


Figure 2. RMS Input Current Comparison

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The Typical Application on the first page is a basic LTC3859A application circuit. LTC3859A can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption, and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected.

$SENSE^+$ and $SENSE^–$ Pins

The $SENSE^+$ and $SENSE^–$ pins are the inputs to the current comparators.

Buck Controllers ($SENSE1^+$/$SENSE1^–$, $SENSE2^+$/$SENSE2^–$): The common mode voltage range on these pins is 0V to 28V (absolute maximum), enabling the LTC3859A to regulate buck output voltages up to a nominal 24V (allowing margin for tolerances and transients). The $SENSE^+$ pin is high impedance over the full common mode range, drawing at most ±1µA. This high impedance allows the current comparators to be used in inductor DCR sensing. The impedance of the $SENSE^–$ pin changes depending on the common mode voltage. When $SENSE^–$ is less than $INTV_{CC}$–0.5V, a small current of less than 1µA flows out of the pin. When $SENSE^–$ is above $INTV_{CC}$+0.5V, a higher current (≈700µA) flows into the pin. Between $INTV_{CC}$–0.5V and $INTV_{CC}$+0.5V, the current transitions from the smaller current to the higher current.

Boost Controller ($SENSE3^+$/$SENSE3^–$): The common mode input range for these pins is 2.5V to 38V, allowing the boost converter to operate from inputs over this full range. The $SENSE3^+$ pin also provides power to the current comparator and draws about 170µA during normal operation (when not shut down or asleep in Burst Mode operation). There is a small bias current of less than 1µA that flows out of the $SENSE3^–$ pin. This high impedance on the $SENSE3^–$ pin allows the current comparator to be used in inductor DCR sensing.

Filter components mutual to the sense lines should be placed close to the LTC3859A, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 3). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 4b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

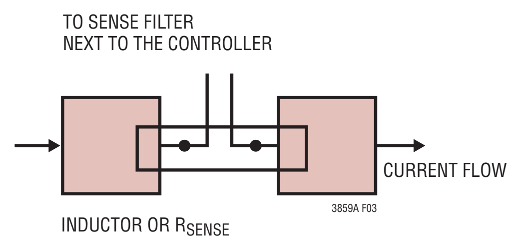

Figure 3. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 4a. R_{SENSE} is chosen based on the required output current.

The current comparators have a maximum threshold $V_{SENSE(MAX)}$ of 50mV. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

When using the buck controllers in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak output current level depending upon the operating duty factor.

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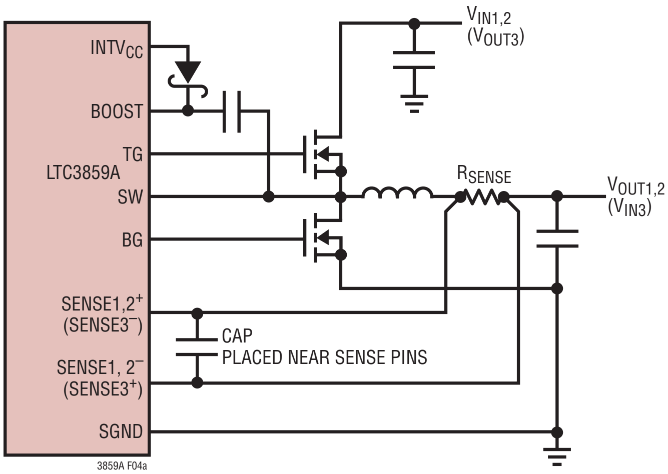
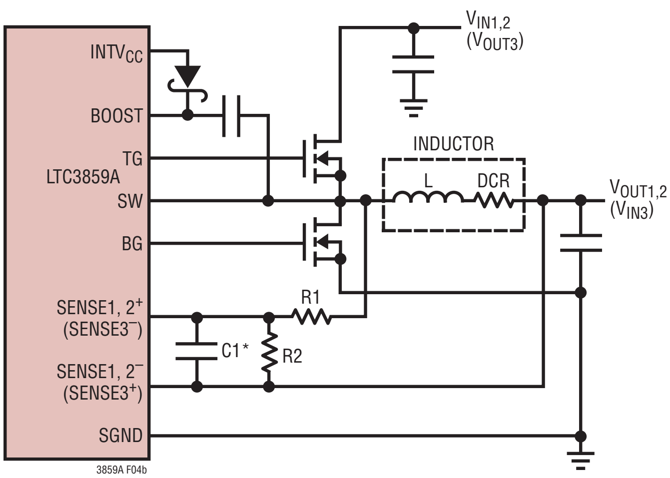


4a. Using a Resistor to Sense Current



*PLACE C1 NEAR SENSE PINS

(R1||R2) • C1 = L/DCR
$R_{SENSE(EQ)}$ = DCR(R2/(R1+R2))

4b. Using the Inductor DCR to Sense Current

Figure 4. Current Sensing Methods

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3859A is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 4b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, determine $R_{SENSE(EQUIV)}$, keeping in mind that the maximum current sense threshold ($V_{SENSE(MAX)}$) for the LTC3859A is fixed at 50mV.

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1||R2 to around 2k, reducing error that might have been caused by the SENSE$^+$ pin's ±1µA current.

The equivalent resistance R1||R2 is scaled to the room temperature inductance and maximum DCR:

$$R1 \,||\, R2 = \frac{L}{(DCR \text{ at } 20°C) \cdot C1}$$

The sense resistor values are:

$$R1 = \frac{R1 \,||\, R2}{R_D}; \quad R2 = \frac{R1 \cdot R_D}{1 - R_D}$$

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The maximum power loss in R1 is related to duty cycle. For the buck controllers, the maximum power loss will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

For the boost controller, the maximum power loss in R1 will occur in continuous mode at $V_{IN} = 1/2 \bullet V_{OUT}$:

$$P_{LOSS}\ R1 = \frac{(V_{OUT(MAX)} - V_{IN}) \bullet V_{IN}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency. For the buck controllers, ΔI_L increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For the boost controller, the inductor ripple current ΔI_L increases with higher V_{OUT}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{IN} \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage for the bucks and $V_{IN} = 1/2 \bullet V_{OUT}$ for the boost.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit (30% for the boost) determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

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Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3859A: one N-channel MOSFET for the top switch (main switch for the buck, synchronous for the boost), and one N-channel MOSFET for the bottom switch (main switch for the boost, synchronous for the buck).

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.4V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Buck Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Buck Sync Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

$$\text{Boost Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Boost Sync Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN\_BUCK} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{OUT(MAX)}}{2}\right)(R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC\_BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)}$$

$$P_{MAIN\_BOOST} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2}\left(I_{OUT(MAX)}\right)^2 \bullet (1+\delta)R_{DS(ON)} + \left(\frac{V_{OUT}^3}{V_{IN}}\right)\left(\frac{I_{OUT(MAX)}}{2}\right) \bullet (R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC\_BOOST} = \frac{V_{IN}}{V_{OUT}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)}$$

where ς is the temperature dependency of $R_{DS(ON)}$ and RDR (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the main N-channel equations for the buck and boost controllers include an additional term for transition losses, which are highest at high input voltages for the bucks and low input voltages for the boost. For V_{IN} < 20V (high V_{IN} for the boost) the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V (low V_{IN} for the boost) the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher

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efficiency. The synchronous MOSFET losses for the buck controllers are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period. The synchronous MOSFET losses for the boost controller are greatest when the input voltage approaches the output voltage or during an overvoltage event when the synchronous switch is on 100% of the period.

The term (1+ ζ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but ζ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes D4, D5, and D6 shown in Figure 13 conduct during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the synchronous MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

Boost C_{IN}, C_{OUT} Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The boost input capacitor C_{IN} voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

In a boost converter, the output has a discontinuous current, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\text{Ripple} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings such as OS-CON and POSCAP.

Buck C_{IN}, C_{OUT} Selection

The selection of C_{IN} for the two buck controllers is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation (1) to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

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In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN} - V_{OUT})\right]^{1/2} \quad (1)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3859A, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC3859A 2-phase operation can be calculated by using Equation (1) for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The drains of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN} (s). Separating the drains and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3859A, is also suggested. A small (1Ω to 10Ω) resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting Output Voltage

The LTC3859A output voltages are each set by an external feedback resistor divider carefully placed across the output, as shown in Figure 5. The regulated output voltages are determined by:

$$V_{OUT,\,BUCK} = 0.8V\left(1 + \frac{R_B}{R_A}\right)$$

$$V_{OUT,\,BOOST} = 1.2V\left(1 + \frac{R_B}{R_A}\right)$$

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

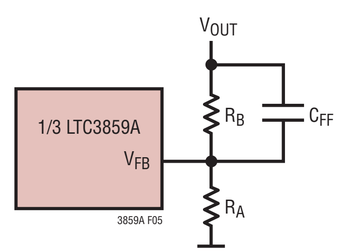

Figure 5. Setting Output Voltage