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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Multi-Phase Current Mode Step-Up DC/DC Controller

## FEATURES

- **Wide $V_{IN}$ Range: 5.5V to 36V Operation**
- **2-Phase Operation Reduces Input and Output Capacitance**
- **Fixed Frequency, Peak Current Mode Control**
- **Internal 10V LDO Regulator**
- **Lower UVLO Thresholds Allows the Use of MOSFETs Rated at 6V $V_{GS}$**
- **Adjustable Slope Compensation Gain**
- **Adjustable Max Duty Cycle (Up to 96%)**
- **Adjustable Leading Edge Blanking**
- ±1% Internal Voltage Reference
- Programmable Operating Frequency with One External Resistor (75kHz to 500kHz)
- Phase-Lockable Fixed Frequency 50kHz to 650kHz
- SYNC Input and CLKOUT for 2-, 3-, 4-, 6- or 12-Phase Operation (PHASEMODE Programmable)
- 24-Lead Narrow SSOP Package
- 5mm × 5mm QFN Package with 0.65mm Lead Pitch
- 24-Lead Thermally Enhanced TSSOP Package

## APPLICATIONS

- Automotive, Telecom and Industrial Power Supplies

## DESCRIPTION

The LTC®3862-2 is a two-phase constant frequency, current mode boost and SEPIC controller that drives N-channel power MOSFETs. Two-phase operation reduces system filtering capacitance and inductance requirements.

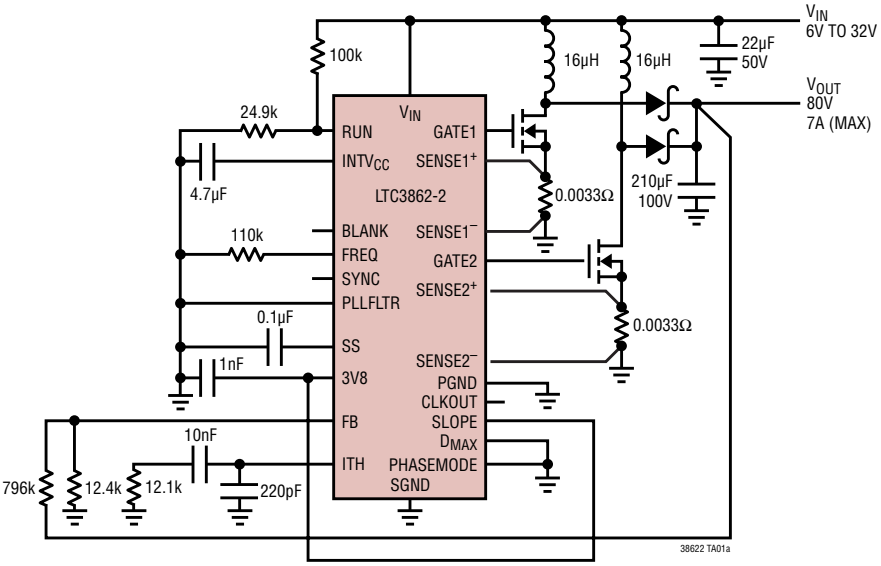
The operating frequency can be set with an external resistor over a 75kHz to 500kHz range and can be synchronized to an external clock using the internal PLL. Multiphase operation is possible using the SYNC input, the CLKOUT output and the PHASEMODE control pin allowing 2-, 3-, 4-, 6- or 12-phase operation.

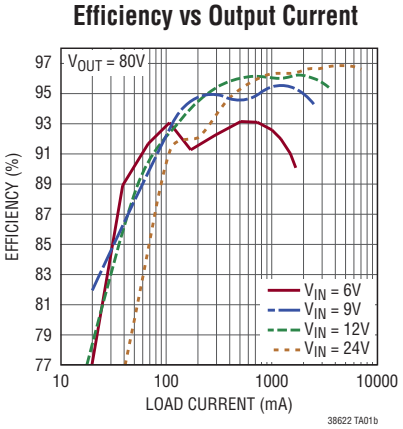
Other features include an internal 10V LDO with undervoltage lockout protection for the gate drivers, a precision RUN pin threshold with programmable hysteresis, soft-start and programmable leading edge blanking and maximum duty cycle.

| PART NUMBER | $INTV_{CC}$ | $V_{IN}$ ON | $V_{IN}$ OFF |
|---|---|---|---|
| LTC3862 | 5V | 3.3V | 2.9V |
| LTC3862-1 | 10V | 7.5V | 7.0V |
| LTC3862-2 | 10V | 4.4V | 3.9V |



## TYPICAL APPLICATION

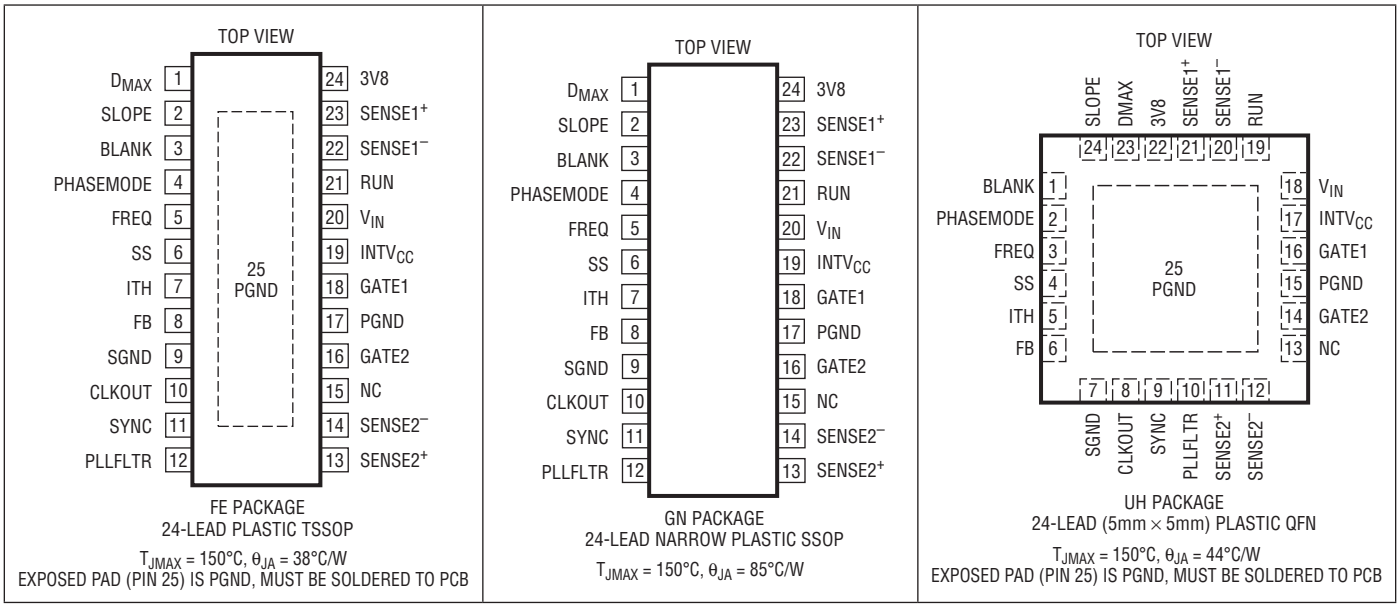


## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Input Supply Voltage ($V_{IN}$) ..... –0.3V to 40V
$INTV_{CC}$ Voltage ..... –0.3V to 11V
$INTV_{CC}$ LDO RMS Output Current ..... 50mA
RUN Voltage ..... –0.3V to 8V
SYNC Voltage ..... –0.3V to 6V
SLOPE, PHASEMODE, $D_{MAX}$, BLANK Voltage ..... –0.3V to $V_{3V8}$
$SENSE1^+$, $SENSE1^-$, $SENSE2^+$, $SENSE2^-$ Voltage ..... –0.3V to $V_{3V8}$
SS, PLLFLTR Voltage ..... –0.3V to $V_{3V8}$
ITH Voltage ..... –0.3V to 2.7V
FB Voltage ..... –0.3V to $V_{3V8}$
FREQ Voltage ..... –0.3V to 1.5V
Operating Junction Temperature Range (Notes 3, 4)
LTC3862-2E ..... –40°C to 85°C
LTC3862-2I ..... –40°C to 125°C
LTC3862-2H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Reflow Peak Body Temperature ..... 260°C

## PIN CONFIGURATION



## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3862EFE-2#PBF | LTC3862EFE-2#TRPBF | LTC3862FE-2 | 24-Lead Plastic TSSOP | –40°C to 85°C |
| LTC3862IFE-2#PBF | LTC3862IFE-2#TRPBF | LTC3862FE-2 | 24-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3862HFE-2#PBF | LTC3862HFE-2#TRPBF | LTC3862FE-2 | 24-Lead Plastic TSSOP | –40°C to 150°C |
| LTC3862EGN-2#PBF | LTC3862EGN-2#TRPBF | LTC3862GN-2 | 24-Lead Plastic SSOP | –40°C to 85°C |
| LTC3862IGN-2#PBF | LTC3862IGN-2#TRPBF | LTC3862GN-2 | 24-Lead Plastic SSOP | –40°C to 125°C |
| LTC3862HGN-2#PBF | LTC3862HGN-2#TRPBF | LTC3862GN-2 | 24-Lead Plastic SSOP | –40°C to 150°C |
| LTC3862EUH-2#PBF | LTC3862EUH-2#TRPBF | 38622 | 24-Lead (5mm × 5mm) Plastic QFN | –40°C to 85°C |
| LTC3862IUH-2#PBF | LTC3862IUH-2#TRPBF | 38622 | 24-Lead (5mm × 5mm) Plastic QFN | –40°C to 125°C |
| LTC3862HUH-2#PBF | LTC3862HUH-2#TRPBF | 38622 | 24-Lead (5mm × 5mm) Plastic QFN | –40°C to 150°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**(Notes 2, 3) The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 12V, RUN = 2V and SS = open, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Supply Input and $INTV_{CC}$ Linear Regulator** | | | | | | | |
| $V_{IN}$ | $V_{IN}$ Supply Voltage Range | | ● | 5.5 | | 36 | V |
| $I_{VIN}$ | $V_{IN}$ Supply Current<br>Normal Mode, No Switching<br>Shutdown | <br>(Note 5)<br>$V_{RUN}$ = 0V | <br>●<br>● | | <br>1.8<br>30 | <br>3.0<br>80 | <br>mA<br>µA |
| $INTV_{CC}$ | LDO Regulator Output Voltage | | | 9.5 | 10.0 | 10.5 | V |
| $dV_{INTVCC(LINE)}$ | Line Regulation | 12V < $V_{IN}$ < 36V | | | 0.002 | 0.02 | %/V |
| $dV_{INTVCC(LOAD)}$ | Load Regulation | Load = 0mA to 20mA | | –2 | | | % |
| $V_{UVLO}$ | $INTV_{CC}$ $UV^+$ Voltage | Rising $INTV_{CC}$ | | | 4.4 | | V |
| | $INTV_{CC}$ $UV^-$ Voltage | Falling $INTV_{CC}$ | | | 3.9 | | V |
| 3V8 | LDO Regulator Output Voltage | | | | 3.8 | | V |
| **Switcher Control Loop** | | | | | | | |
| $V_{FB}$ | Reference Voltage | $V_{ITH}$ = 0.8V (Note 6) E-Grade (Note 3)<br>I-Grade and H-Grade (Note 3) | ●<br>● | 1.210<br>1.199 | 1.223<br>1.223 | 1.235<br>1.248 | V<br>V |
| $dV_{FB}/dV_{IN}$ | Feedback Voltage $V_{IN}$ Line Regulation | $V_{IN}$ = 5.5V to 36V (Note 6) | | | ±0.002 | 0.01 | %/V |
| $dV_{FB}/dV_{ITH}$ | Feedback Voltage Load Regulation | $V_{ITH}$ = 0.5V to 1.2V (Note 6) | | | 0.01 | 0.1 | % |
| $g_m$ | Transconductance Amplifier Gain | $V_{ITH}$ = 0.8V (Note 6), ITH Pin Load = ±5µA | | | 660 | | µMho |
| $f_{0dB}$ | Error Amplifier Unity-Gain Crossover Frequency | (Note 7) | | | 1.8 | | MHz |

## ELECTRICAL CHARACTERISTICS

**(Notes 2, 3) The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 12V, RUN = 2V and SS = open, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{ITH}$ | Error Amplifier Maximum Output Voltage (Internally Clamped) | $V_{FB}$ = 1V, No Load | | | 2.7 | | V |
| | Error Amplifier Minimum Output Voltage | $V_{FB}$ = 1.5V, No Load | | | 50 | | mV |
| $I_{ITH}$ | Error Amplifier Output Source Current | | | | –30 | | µA |
| | Error Amplifier Output Sink Current | | | | 30 | | µA |
| $I_{FB}$ | Error Amplifier Input Bias Currents | (Note 6) | | | –50 | –200 | nA |
| $V_{ITH(PSKIP)}$ | Pulse Skip Mode Operation ITH Pin Voltage | Rising ITH Voltage (Note 6)<br>Hysteresis | | | 0.275<br>25 | | V<br>mV |
| $I_{SENSE(ON)}$ | SENSE Pin Current | | | | 0.01 | 2 | µA |
| $V_{SENSE(MAX)}$ | Maximum Current Sense Input Threshold | $V_{SLOPE}$ = Float, Low Duty Cycle<br>(Note 3) | <br>● | 68<br>65 | 75<br>75 | 82<br>85 | mV<br>mV |
| $V_{SENSE(MATCH)}$ | CH1 to CH2 Maximum Current Sense Threshold Matching | $V_{SLOPE}$ = Float, Low Duty Cycle (Note 3)<br>($V_{SENSE1}$ – $V_{SENSE2}$) | ● | –7 | | 7 | mV |
| **RUN/Soft-Start** | | | | | | | |
| $I_{RUN}$ | RUN Source Current | $V_{RUN}$ = 0V<br>$V_{RUN}$ = 1.5V | | | –0.5<br>–5 | | µA<br>µA |
| $V_{RUN}$ | High Level RUN Channel Enable Threshold | | | | 1.22 | | V |
| $V_{RUNHYS}$ | RUN Threshold Hysteresis | | | | 80 | | mV |
| $I_{SS}$ | SS Pull-Up Current | $V_{SS}$ = 0V | | | –5 | | µA |
| $R_{SS}$ | SS Pull-Down Resistance | $V_{RUN}$ = 0V | | | 10 | | kΩ |
| **Oscillator** | | | | | | | |
| $f_{OSC}$ | Oscillator Frequency | $R_{FREQ}$ = 45.6k<br>$R_{FREQ}$ = 45.6k | <br>● | 280<br>260 | 300<br>300 | 320<br>340 | kHz kHz |
| | Oscillator Frequency Range | | ● | 75 | | 500 | kHz |
| $V_{FREQ}$ | Nominal FREQ Pin Voltage | $R_{FREQ}$ = 45.6k | | | 1.223 | | V |
| $f_{SYNC}$ | SYNC Minimum Input Frequency | $V_{SYNC}$ = External Clock | ● | | | 50 | kHz |
| | SYNC Maximum Input Frequency | $V_{SYNC}$ = External Clock | ● | 650 | | | kHz |
| $V_{SYNC}$ | SYNC Input Threshold | Rising Threshold | | | 1.5 | | V |
| $I_{PLLFLTR}$ | Phase Detector Sourcing Output Current | $f_{SYNC} > f_{OSC}$ | | | –15 | | µA |
| | Phase Detector Sinking Output Current | $f_{SYNC} < f_{OSC}$ | | | 15 | | µA |
| CH1-CH2 | Channel 1 to Channel 2 Phase Relationship | $V_{PHASEMODE}$ = 0V<br>$V_{PHASEMODE}$ = Float<br>$V_{PHASEMODE}$ = 3V8 | | | 180<br>180<br>120 | | Deg<br>Deg<br>Deg |
| CH1-CLKOUT | Channel 1 to CLKOUT Phase Relationship | $V_{PHASEMODE}$ = 0V<br>$V_{PHASEMODE}$ = Float<br>$V_{PHASEMODE}$ = 3V8 | | | 90<br>60<br>240 | | Deg<br>Deg<br>Deg |
| $D_{MAX}$ | Maximum Duty Cycle | $V_{DMAX}$ = 0V (Note 9)<br>$V_{DMAX}$ = Float<br>$V_{DMAX}$ = 3V8 | | | 96<br>84<br>75 | | %<br>%<br>% |

## ELECTRICAL CHARACTERISTICS

**(Notes 2, 3) The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 12V, RUN = 2V and SS = open, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{ON(MIN)1}$ | Minimum On-Time | $V_{BLANK}$ = 0V (Note 8) | | | 210 | | ns |
| $t_{ON(MIN)2}$ | Minimum On-Time | $V_{BLANK}$ = Float (Note 8) | | | 290 | | ns |
| $t_{ON(MIN)3}$ | Minimum On-Time | $V_{BLANK}$ = 3V8 (Note 8) | | | 375 | | ns |
| **Gate Driver** | | | | | | | |
| $R_{DS(ON)}$ | Driver Pull-Up $R_{DS(ON)}$ | | | | 3 | | Ω |
| | Driver Pull-Down $R_{DS(ON)}$ | | | | 0.9 | | Ω |
| **Overvoltage** | | | | | | | |
| $V_{FB(OV)}$ | $V_{FB}$, Overvoltage Lockout Threshold | $V_{FB(OV)}$ – $V_{FB(NOM)}$ in Percent | | 8 | 10 | 12 | % |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

**Note 3:** The LTC3862E-2 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3862I-2 is guaranteed over the full –40°C to 125°C operating temperature range and the LTC3862H-2 is guaranteed over the full –40°C to 150°C operating temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 5:** Supply current in normal operation is dominated by the current needed to charge the external MOSFET gates. This current will vary with supply voltage and the external MOSFETs used.

**Note 6:** The IC is tested in a feedback loop that adjusts $V_{FB}$ to achieve a specified error amplifier output voltage.

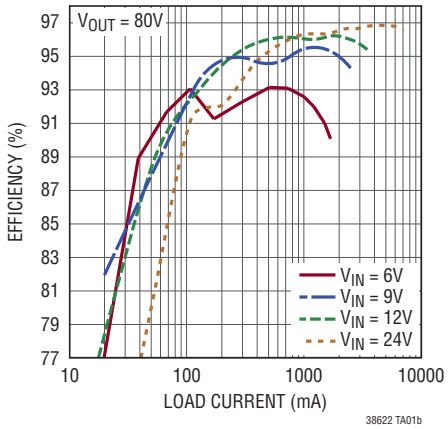
**Note 7:** Guaranteed by design, not subject to test.

**Note 8:** The minimum on-time condition is specified for an inductor peak-to-peak ripple current = 30% (see Minimum On-Time Considerations in the Applications Information section).

**Note 9:** The maximum duty cycle limit is derived from an internal clock that runs at 12× the programmed switching frequency. See the Applications Information section for additional information.

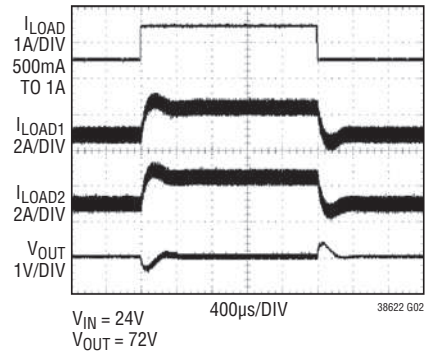
## TYPICAL PERFORMANCE CHARACTERISTICS

### Efficiency vs Output Current



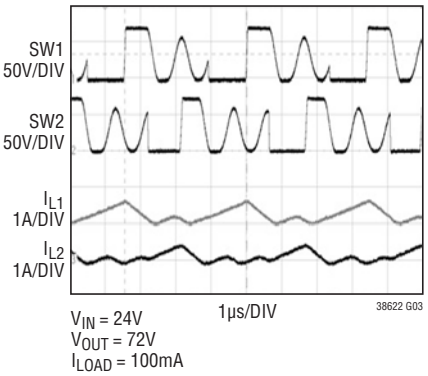

38622 TA01b

### Load Step



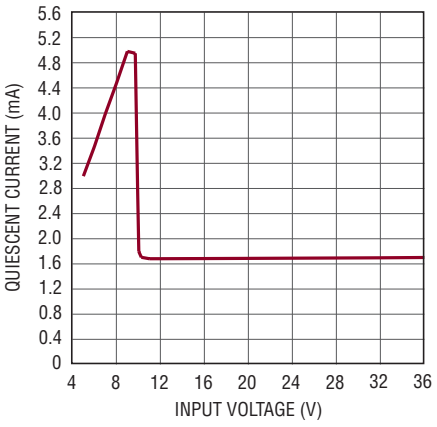

38622 G02

### Inductor Current at Light Load



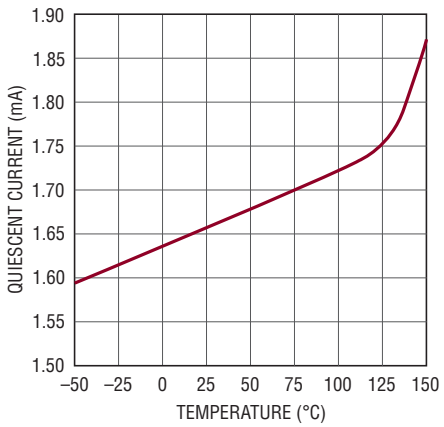

38622 G03

### Quiescent Current vs Input Voltage



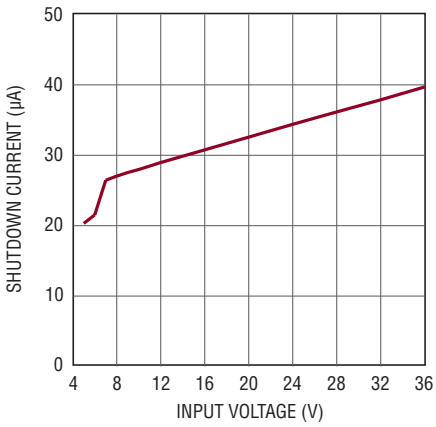

38622 G04

### Quiescent Current vs Temperature



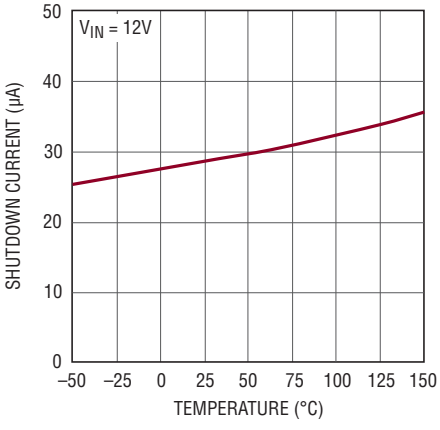

38622 G05

### Shutdown Quiescent Current vs Input Voltage



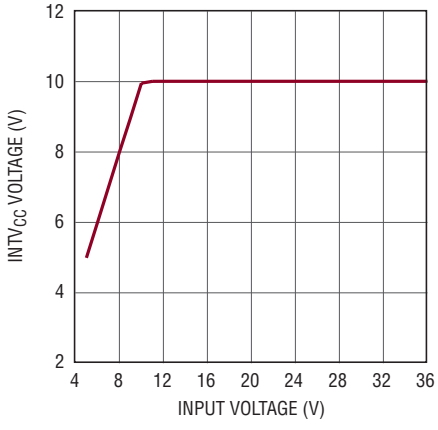

38622 G06

### Shutdown Quiescent Current vs Temperature



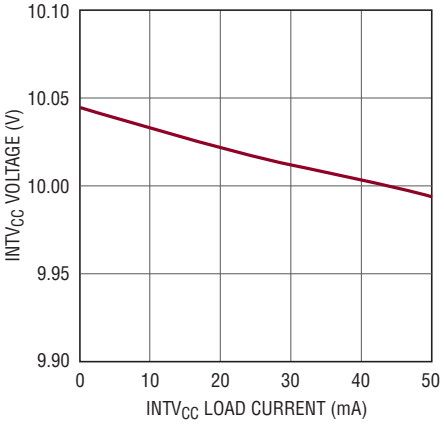

38622 G07

### $INTV_{CC}$ Line Regulation




38622 G08

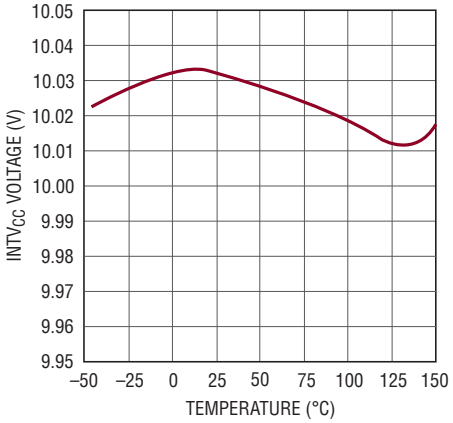
### $INTV_{CC}$ Load Regulation




38622 G09

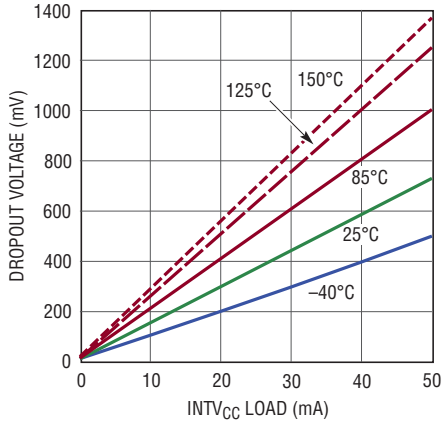
# TYPICAL PERFORMANCE CHARACTERISTICS

### $INTV_{CC}$ vs Temperature



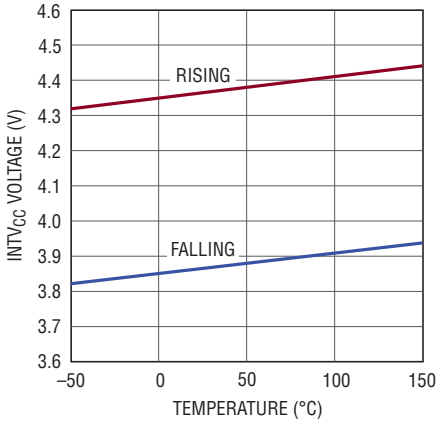

38622 G10

### $INTV_{CC}$ LDO Dropout Voltage vs Load Current, Temperature



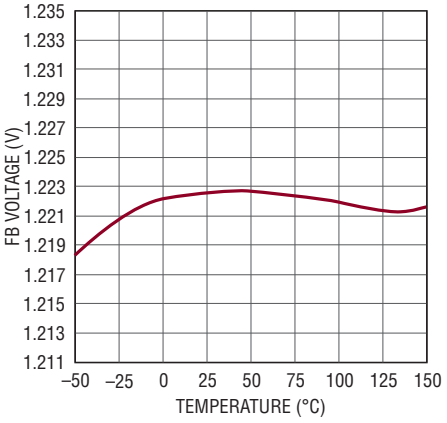

38622 G11

### $INTV_{CC}$ UVLO Threshold vs Temperature



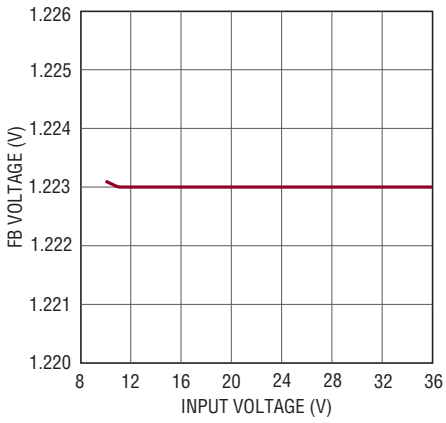

38622 G12

### Feedback Voltage vs Temperature



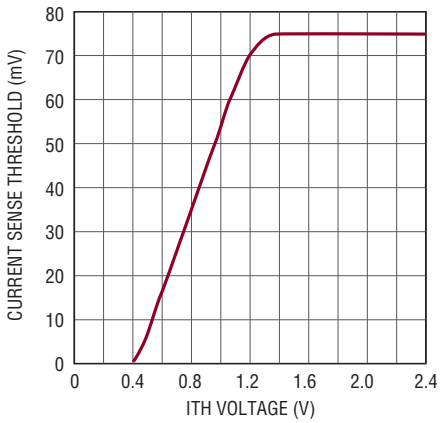

38622 G13

### Feedback Voltage Line Regulation



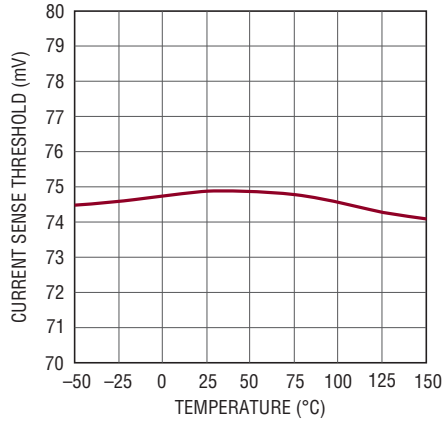

38622 G14

### Current Sense Threshold vs ITH Voltage



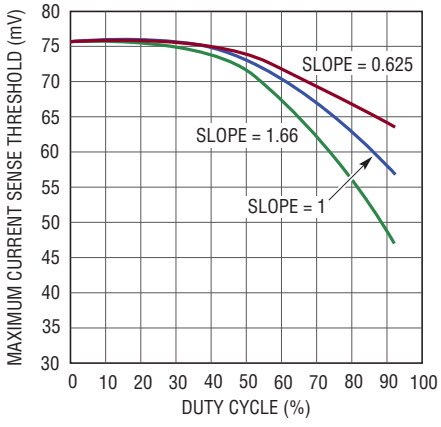

38622 G15

### Current Sense Threshold vs Temperature



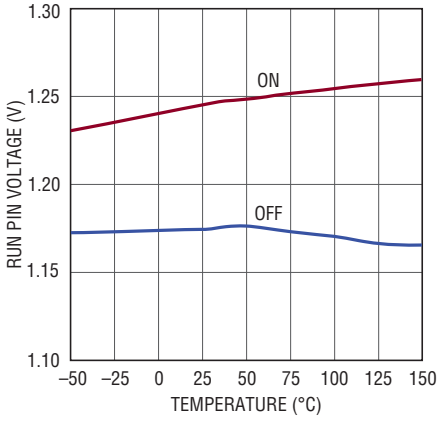

38622 G16

### Maximum Current Sense Threshold vs Duty Cycle




38622 G17

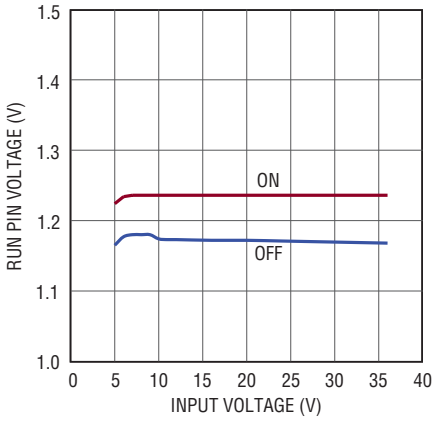
### RUN Threshold vs Temperature




38622 G18

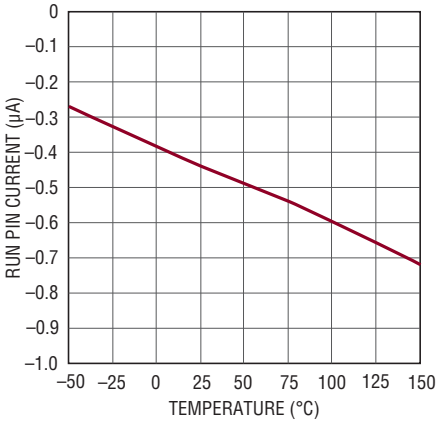
## TYPICAL PERFORMANCE CHARACTERISTICS

**RUN Threshold vs Input Voltage**



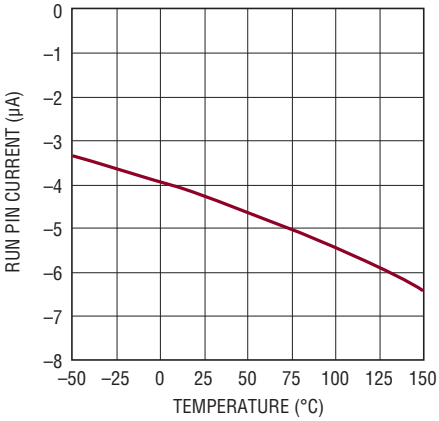

38622 G19

**RUN (Off) Source Current vs Temperature**



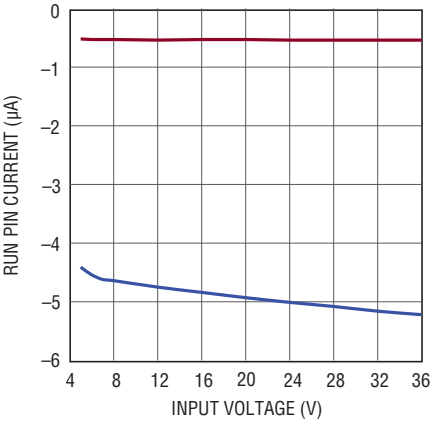

38622 G20

**RUN (On) Source Current vs Temperature**



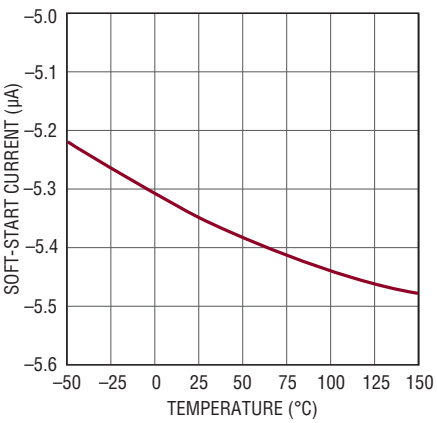

38622 G21

**RUN Source Current vs Input Voltage**



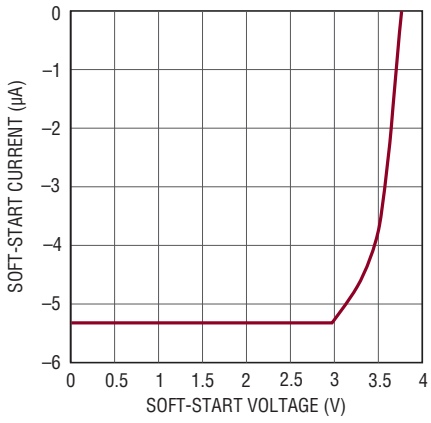

38622 G19

**Soft-Start Current vs Temperature**



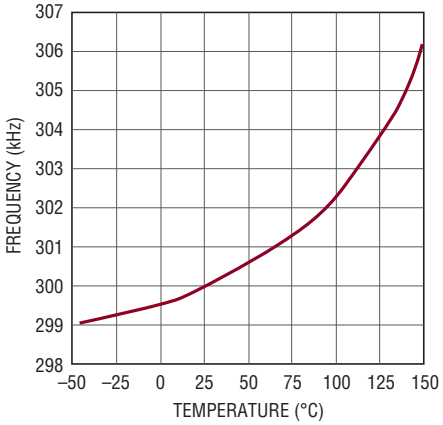

38622 G23

**Soft-Start Current vs Soft-Start Voltage**



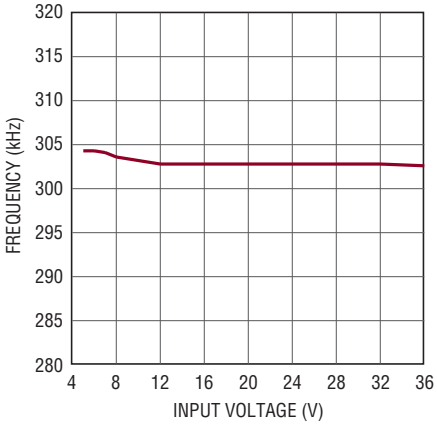

38622 G24

**Oscillator Frequency vs Temperature**



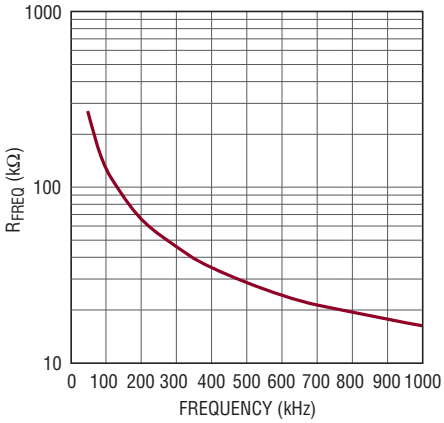

38622 G25

**Oscillator Frequency vs Input Voltage**




38622 G26

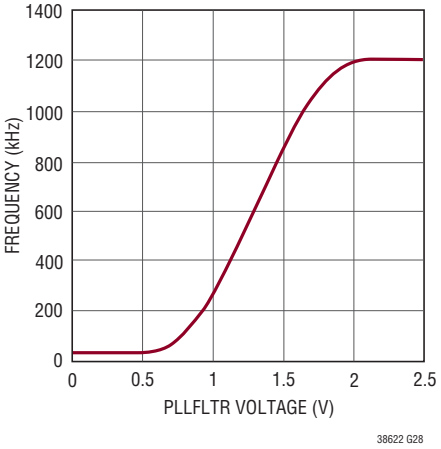
**$R_{FREQ}$ vs Frequency**



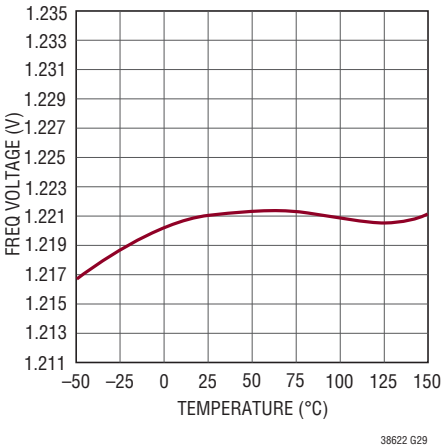

38622 G27

# TYPICAL PERFORMANCE CHARACTERISTICS

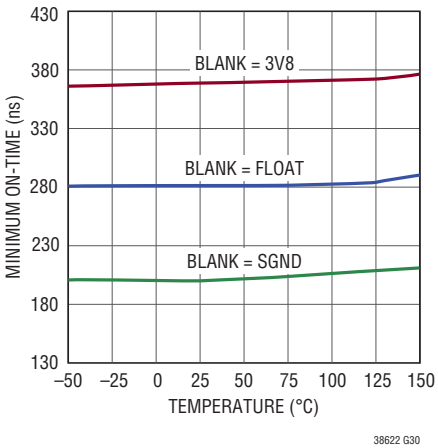
### Frequency vs PLLFLTR Voltage



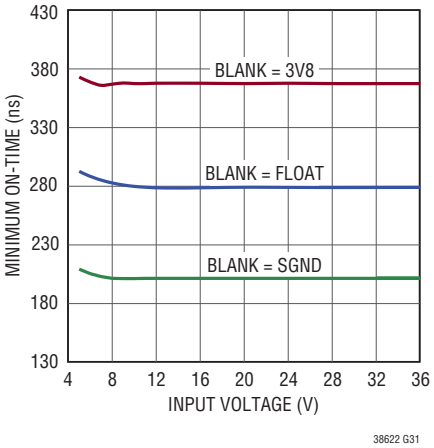

### Frequency Pin Voltage vs Temperature



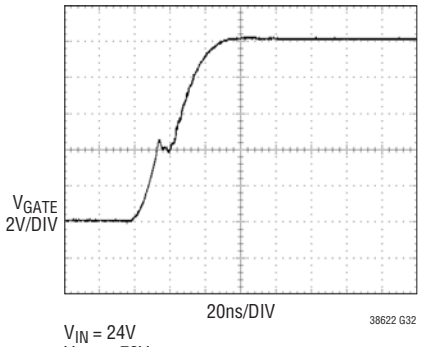

### Minimum On-Time vs Temperature




### Minimum On-Time vs Input Voltage

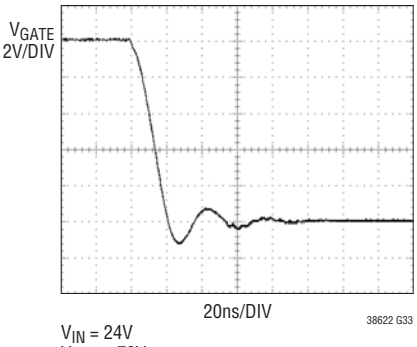



### Gate Turn-On Waveform Driving Renesas HAT2267H




$V_{IN}$ = 24V
$V_{OUT}$ = 72V
$I_{LOAD}$ = 0.25A

### Gate Turn-Off Waveform Driving Renesas HAT2267H




$V_{IN}$ = 24V
$V_{OUT}$ = 72V
$I_{LOAD}$ = 0.25A

## PIN FUNCTIONS (SSOP/QFN/TSSOP)

**3V8 (Pin 24/Pin 22/Pin 24):** Output of the Internal 3.8V LDO from $INTV_{CC}$. Supply pin for the low voltage analog and digital circuits. A low ESR 1nF ceramic bypass capacitor should be connected between 3V8 and SGND, as close as possible to the IC.

**BLANK (Pin 3/Pin 1/Pin 3):** Blanking Time. Floating this pin provides a nominal minimum on-time of 290ns. Connecting this pin to 3V8 provides a minimum on-time of 375ns, while connecting it to SGND provides a minimum on-time of 210ns.

**CLKOUT (Pin 10/Pin 8/Pin 10):** Digital Output Used for Daisy-Chaining Multiple LTC3862-2 ICs in Multi-Phase Systems. The PHASEMODE pin voltage controls the relationship between CH1 and CH2 as well as between CH1 and CLKOUT.

**$D_{MAX}$ (Pin 1/Pin 23/Pin 1):** Maximum Duty Cycle. This pin programs the maximum duty cycle. Floating this pin provides 84% duty cycle. Connecting this pin to 3V8 provides 75% duty cycle, while connecting it to SGND provides 96% duty cycle. The maximum duty cycle limit is derived from an internal clock that runs at 12× the programmed switching frequency. As a result, the maximum duty cycle limit $D_{MAX}$ is extremely precise.

**FB (Pin 8/Pin 6/Pin 8):** Error Amplifier Input. The FB pin should be connected through a resistive divider network to $V_{OUT}$ to set the output voltage.

**FREQ (Pin 5/Pin 3/Pin 5):** A resistor from FREQ to SGND sets the operating frequency.

**GATE1 (Pin 18/Pin 16/Pin 18):** Gate Drive Output. The LTC3862-2 provides a 10V gate drive referenced to PGND to drive a high voltage MOSFET. The GATE pin is rated for an absolute maximum voltage of –0.3V minimum and 11V maximum.

**GATE2 (Pin 16/Pin 14/Pin 16):** Gate Drive Output. The LTC3862-2 provides a 10V gate drive referenced to PGND to drive a high voltage MOSFET. The GATE pin is rated for an absolute maximum voltage of –0.3V minimum and 11V maximum.

**$INTV_{CC}$ (Pin 19/Pin 17/Pin 19):** Output of the Internal 10V Low Dropout Regulator (LDO). A low ESR 4.7µF (X5R or better) ceramic bypass capacitor should be connected between $INTV_{CC}$ and PGND, as close as possible to the IC.

**ITH (Pin 7/Pin 5/Pin 7):** Error Amplifier Output. The current comparator trip threshold increases with the ITH control voltage. The ITH pin is also used for compensating the control loop of the converter.

**PGND (Pin 17/Pin 15, Exposed Pad Pin 25/Pin 17, Exposed Pad Pin 25):** Power Ground. Connect this pin close to the sources of the power MOSFETs. PGND should also be connected to the negative terminals of $V_{IN}$ and $INTV_{CC}$ bypass capacitors. PGND is electrically isolated from the SGND pin. The exposed pad of the QFN and FE packages is connected to PGND and must be soldered to PCB ground for electrical contact and rated thermal performance.

**PHASEMODE (Pin 4/Pin 2/Pin 4):** The PHASEMODE pin voltage programs the phase relationship between CH1 and CH2 rising gate signals, as well as the phase relationship between CH1 gate signal and CLKOUT. Floating this pin or connecting it to either 3V8, or SGND changes the phase relationship between CH1, CH2 and CLKOUT.

**PLLFLTR (Pin 12/Pin 10/Pin 12):** PLL Lowpass Filter Input. When synchronizing to an external clock, this pin serves as the lowpass filter input for the PLL. A series resistor and capacitor connected from PLLFLTR to SGND compensate the PLL feedback loop.

**RUN (Pin 21/Pin 19/Pin 21):** Run Control Input. A voltage above 1.22V on the pin turns on the IC. Forcing the pin below 1.22V causes the IC to shut down. There is a 0.5µA pull-up current for this pin. Once the RUN pin raises above 1.22V, an additional 4.5µA pull-up current is added to the pin for programmable hysteresis.

**$SENSE1^+$ (Pin 23/Pin 21/Pin 23):** Positive Inputs to the Current Comparators. The ITH pin voltage programs the current comparator offset in order to set the peak current trip threshold. This pin is normally connected to a sense resistor in the source of the power MOSFET.

## PIN FUNCTIONS (SSOP/QFN/TSSOP)

**SENSE2$^+$ (Pin 13/Pin 11/Pin 13):** Positive Inputs to the Current Comparators. The ITH pin voltage programs the current comparator offset in order to set the peak current trip threshold. This pin is normally connected to a sense resistor in the source of the power MOSFET.

**SENSE1$^-$ (Pin 22/Pin 20/Pin 22):** Negative Inputs to the Current Comparators. This pin is normally connected to the bottom of the sense resistor.

**SENSE2$^-$ (Pin 14/Pin 12/Pin 14):** Negative Inputs to the Current Comparators. This pin is normally connected to the bottom of the sense resistor.

**SGND (Pin 9/Pin 7/Pin 9):** Signal Ground. All feedback and soft-start connections should return to SGND. For optimum load regulation, the SGND pin should be kelvin connected to the PCB location between the negative terminals of the output capacitors.

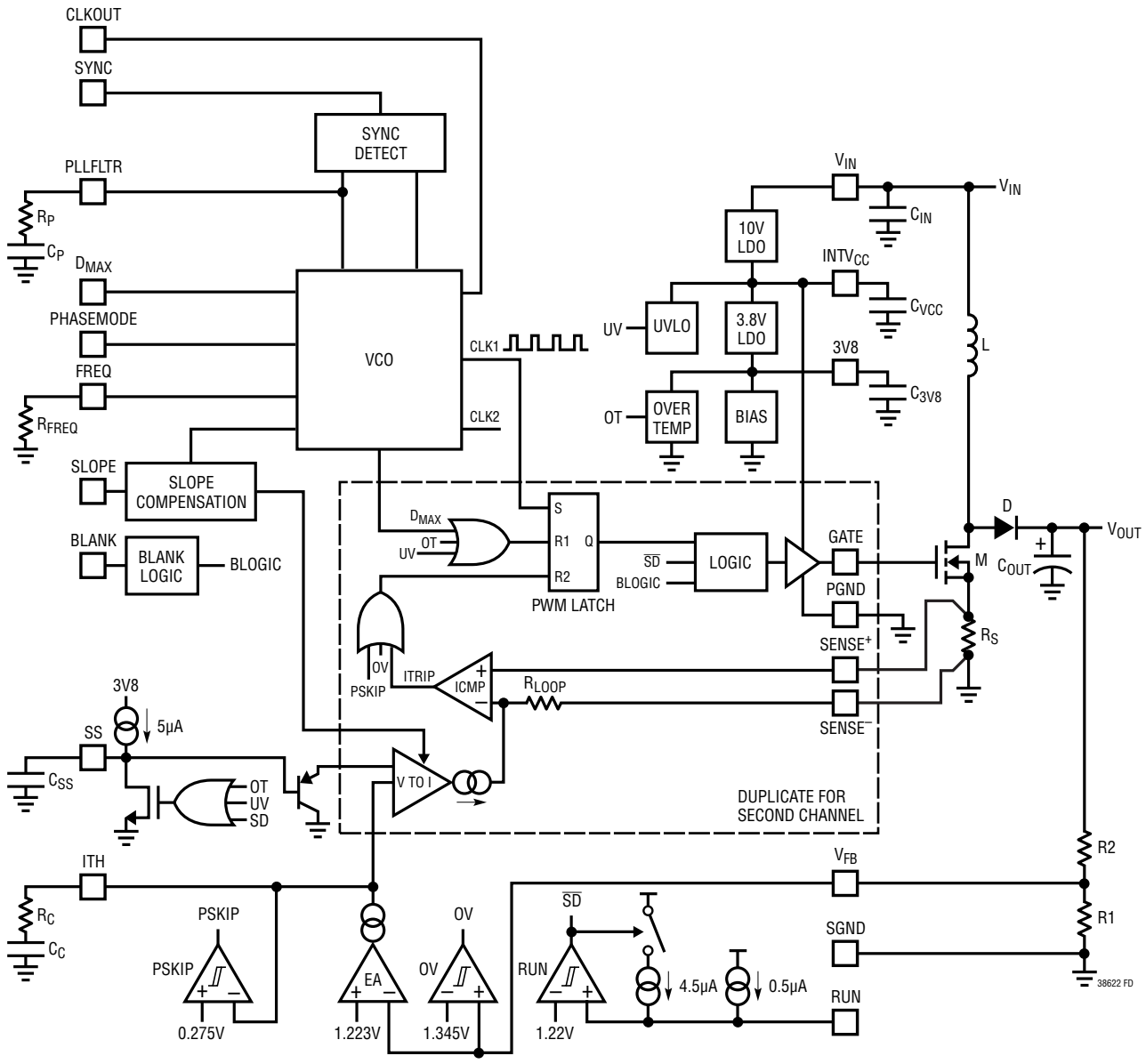
**SLOPE (Pin 2/Pin 24/Pin 2):** This pin programs the gain of the internal slope compensation. Floating this pin provides a normalized slope compensation gain of 1.00. Connecting this pin to 3V8 increases the normalized slope compensation by 66%, and connecting it to SGND decreases the normalized slope compensation by 37.5%. See the Applications Information section for more details.

**SS (Pin 6/Pin 4/Pin 6):** Soft-Start Input. For soft-start operation, connecting a capacitor from this pin to SGND will clamp the output of the error amp. An internal 5µA current source will charge the capacitor and set the rate of increase of the peak switch current of the converter.

**SYNC (Pin 11/Pin 9/Pin 11):** PLL Synchronization Input. Applying an external clock between 50kHz and 650kHz will cause the operating frequency to synchronize to the clock. SYNC is pulled down by a 50k internal resistor. The rising edge of the SYNC input waveform will align with the rising edge of GATE1 in closed-loop operation. A SYNC signal with an amplitude greater than 1.6V is considered an active high, while any signal below 0.9V is considered an active low.

**$V_{IN}$ (Pin 20/Pin 18/Pin 20):** Main Supply Input. A low ESR ceramic capacitor should be connected between this pin and SGND.

## FUNCTIONAL DIAGRAM



## OPERATION

### The Control Loop

The LTC3862-2 uses a constant frequency, peak current mode step-up architecture with its two channels operating 180 degrees out-of-phase. During normal operation, each external MOSFET is turned on when the clock for that channel sets the PWM latch, and is turned off when the main current comparator, ICMP, resets the latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output feedback signal at the $V_{FB}$ pin to the internal 1.223V reference and generates an error signal at the ITH pin. When the load current increases it causes a slight decrease in $V_{FB}$ relative to the reference voltage, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current. After the MOSFET is turned off, the inductor current flows through the boost diode into the output capacitor and load, until the beginning of the next clock cycle.

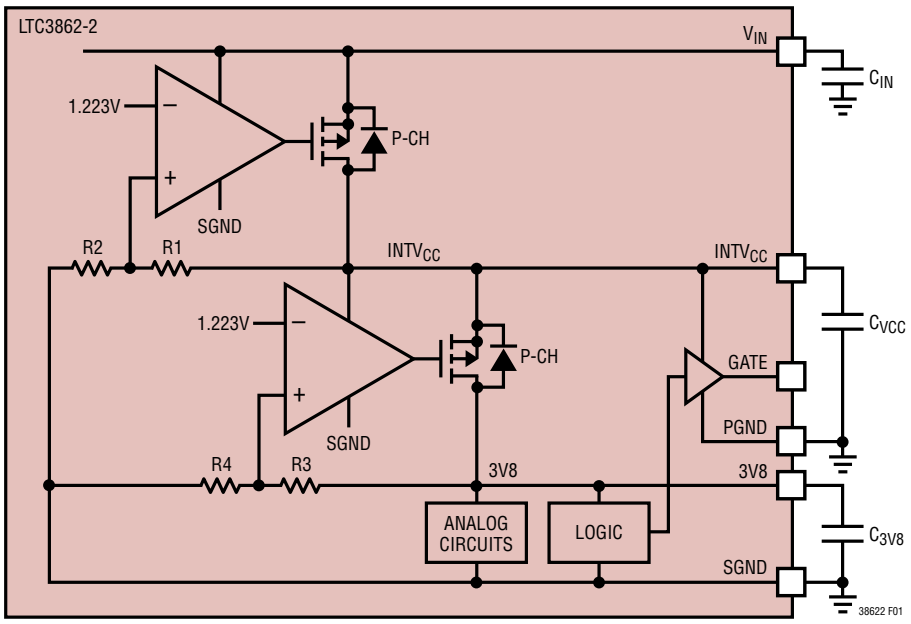
### Cascaded LDOs Supply Power to the Gate Driver and Control Circuitry

The LTC3862-2 contains two cascaded PMOS output stage low dropout voltage regulators (LDOs), one for the gate drive supply ($INTV_{CC}$) and one for the low voltage analog and digital control circuitry (3V8). A block diagram of this power supply arrangement is shown in Figure 1.

### The Gate Driver Supply LDO ($INTV_{CC}$)

The 10V output ($INTV_{CC}$) of the first LDO is powered from $V_{IN}$ and supplies power to the power MOSFET gate drivers. The $INTV_{CC}$ pin should be bypassed to PGND with a minimum of 4.7µF of ceramic capacitance (X5R or better), placed as close as possible to the IC pins. If two power MOSFETs are connected in parallel for each channel in order to increase the output power level, or if a single MOSFET with a $Q_G$ greater than 50nC is used, then it is recommended that the bypass capacitance be increased to a minimum of 10µF.

An undervoltage lockout (UVLO) circuit senses the $INTV_{CC}$ regulator output in order to protect the power MOSFETs from operating with inadequate gate drive. For the LTC3862-2 the rising UVLO threshold is typically 4.4V and the hysteresis is typically 500mV. The LTC3862-2 was optimized for high voltage power MOSFETs with $R_{DS(ON)}$ ratings at a $V_{GS}$ of 6V. For applications requiring logic-level power MOSFETs, please refer to the LTC3862 data sheet.




NOTE: PLACE $C_{VCC}$ AND $C_{3V8}$ CAPACITORS AS CLOSE AS POSSIBLE TO DEVICE PINS

**Figure 1. Cascaded LDOs Provide Gate Drive and Control Circuitry Power**

## OPERATION

In multi-phase applications, all of the FB pins are connected together and all of the error amplifier output pins (ITH) are connected together. **The $INTV_{CC}$ pins, however, should not be connected together.** The $INTV_{CC}$ regulator is capable of sourcing current but is not capable of sinking current. As a result, when two or more $INTV_{CC}$ regulator outputs are connected together, the highest voltage regulator supplies all of the gate drive and control circuit current, and the other regulators are off. This would place a thermal burden on the highest output voltage LDO and could cause the maximum die temperature to be exceeded. In multi-phase LTC3862-2 applications, each $INTV_{CC}$ regulator output should be independently bypassed to its respective PGND pin as close as possible to each IC.

### The Low Voltage Analog and Digital Supply LDO (3V8)

The second LDO within the LTC3862-2 is powered off of $INTV_{CC}$ and serves as the supply to the low voltage analog and digital control circuitry, as shown in Figure 1. The output voltage of this LDO (which also has a PMOS output device) is 3.8V. Most of the analog and digital control circuitry is powered from the internal 3V8 LDO. The 3V8 pin should be bypassed to SGND with a 1nF ceramic capacitor (X5R or better), placed as close as possible to the IC pins. This LDO is not intended to be used as a supply for external circuitry.

### Thermal Considerations and Package Options

The LTC3862-2 is offered in three package options. The 5mm × 5mm QFN package (UH24) has a thermal resistance $R_{TH(JA)}$ of 34°C/W, the 24-pin TSSOP (FE24) package has a thermal resistance of 38°C/W, and the 24-pin SSOP (GN24) package has a thermal resistance of 85°C/W. The QFN and TSSOP package options have a lead pitch of 0.65mm, and the GN24 option has a lead pitch of 0.025in.

The $INTV_{CC}$ regulator can supply up to 50mA of total current. As a result, care must be taken to ensure that the maximum junction temperature of the IC is never exceeded. The junction temperature can be estimated using the following equations:

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f$$

$$P_{DISS} = V_{IN} \bullet (I_Q + Q_{G(TOT)} \bullet f)$$

$$T_J = T_A + P_{DISS} \bullet R_{TH(JA)}$$

The total quiescent current ($I_{Q(TOT)}$) consists of the static supply current ($I_Q$) and the current required to charge the gate capacitance of the power MOSFETs. The value of $Q_{G(TOT)}$ should come from the plot of $V_{GS}$ vs $Q_G$ in the Typical Performance Characteristics section of the MOSFET data sheet. The value listed in the electrical specifications may be measured at a higher $V_{GS}$, such as 15V, whereas the value of interest is at the 10V $INTV_{CC}$ gate drive voltage.

As an example of the required thermal analysis, consider a 2-phase boost converter with a 5.5V to 24V input voltage range and an output voltage of 72V at 1.5A. The switching frequency is 150kHz and the maximum ambient temperature is 70°C. The power MOSFET used for this application is the Renesas HAT2267H, which has a typical $R_{DS(ON)}$ of 13mΩ at $V_{GS}$ = 10V. From the plot of $V_{GS}$ vs $Q_G$, the total gate charge at $V_{GS}$ = 10V is 30nC (the temperature coefficient of the gate charge is low). One power MOSFET is used for each phase. For the QFN package option:

$$I_{Q(TOT)} = 3mA + 2 \bullet 30nC \bullet 150kHz = 12mA$$

$$P_{DISS} = 24V \bullet 12mA = 288mW$$

$$T_J = 70°C + 288mW \bullet 34°C/W = 79.8°C$$

In this example, the junction temperature rise is only 9.8°C. These equations demonstrate how the gate charge current typically dominates the quiescent current of the IC, and how the choice of package option and board heat sinking can have a significant effect on the thermal performance of the solution.

## OPERATION

To prevent the maximum junction temperature from being exceeded, the input supply current to the IC should be checked when operating in continuous mode (heavy load) at maximum $V_{IN}$. A trade-off between the operating frequency and the size of the power MOSFETs may need to be made in order to maintain a reliable junction temperature. Finally, it is important to verify the calculations by performing a thermal analysis of the final PCB using an infrared camera or thermal probe. As an option, an external regulator shown in Figure 3 can be used to reduce the total power dissipation on the IC.

### Thermal Shutdown Protection

In the event of an overtemperature condition (external or internal), an internal thermal monitor will shut down the gate drivers and reset the soft-start capacitor if the die temperature exceeds 170°C. This thermal sensor has a hysteresis of 10°C to prevent erratic behavior at hot temperatures. The LTC3862-2's internal thermal sensor is intended to protect the device during momentary overtemperature conditions. Continuous operation above the specified maximum operating junction temperature, however, may result in device degradation.

### Operation at Low Supply Voltage

The LTC3862-2 has a minimum input voltage of 5.5V, making it a good choice for applications that require high voltage power MOSFETs with 6V $R_{DS(ON)}$ ratings. The gate driver for the LTC3862-2 consists of PMOS pull-up and NMOS pull-down devices, allowing the full $INTV_{CC}$ voltage to be applied to the gates during power MOSFET switching. Nonetheless, care should be taken to determine the minimum gate drive supply voltage ($INTV_{CC}$) in order to choose the optimum power MOSFETs. Important parameters that can affect the minimum gate drive voltage are the minimum input voltage ($V_{IN(MIN)}$), the LDO dropout voltage, the $Q_G$ of the power MOSFETs, and the operating frequency.

If the input voltage $V_{IN}$ is low enough for the $INTV_{CC}$ LDO to be in dropout, then the minimum gate drive supply voltage is:

$$V_{INTVCC} = V_{IN(MIN)} – V_{DROPOUT}$$

The LDO dropout voltage is a function of the total gate drive current and the quiescent current of the IC (typically 3mA). A curve of dropout voltage vs output current for the LDO is shown in Figure 2. The temperature coefficient of the LDO dropout voltage is approximately 6000ppm/°C.

The total Q-current ($I_{Q(TOT)}$) flowing in the LDO is the sum of the controller quiescent current (3mA) and the total gate charge drive current.

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f$$

After the calculations have been completed, it is important to measure the gate drive waveforms and the gate driver supply voltage ($INTV_{CC}$ to PGND) over all operating conditions (low $V_{IN}$, nominal $V_{IN}$ and high $V_{IN}$, as well as from light load to full load) to ensure adequate power MOSFET enhancement. Consult the power MOSFET data sheet to determine the actual $R_{DS(ON)}$ for the measured $V_{GS}$, and verify your thermal calculations by measuring the component temperatures using an infrared camera or thermal probe.

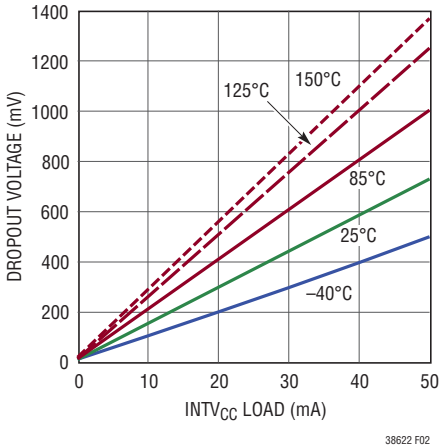



**Figure 2. $INTV_{CC}$ LDO Dropout Voltage vs Current**

## OPERATION

### Operation at High Supply Voltage

At high input voltages, the LTC3862-2's internal LDO can dissipate a significant amount of power, which could cause the maximum junction temperature to be exceeded. Conditions such as a high operating frequency, or the use of more than one power MOSFET per channel, could push the junction temperature rise to high levels. If the thermal equations above indicate too high a rise in the junction temperature, an external bias supply can always be used to reduce the power dissipation on the IC, as shown in Figure 3.

For example, a 12V system rail that is available would be more suitable than the 24V main input power rail to power the LTC3862-2. Also, the bias power can be generated with a separate switching or LDO regulator. An example of an LDO regulator is shown in Figure 3. The output voltage of the LDO regulator can be set by selecting an appropriate zener diode to be higher than 10V but low enough to divide the power dissipation between LTC3862-2 and Q1 in Figure 3. The absolute maximum voltage rating of the $INTV_{CC}$ pin is 11V.

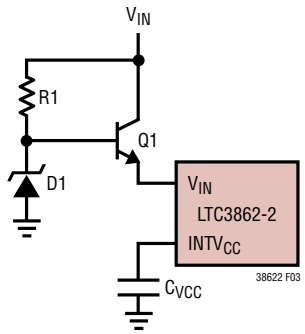



**Figure 3. Using the LTC3862-2 with an External Bias Supply**

### Power Supply Sequencing

As shown in Figure 1, there are body diodes in parallel with the PMOS output transistors in the two LDO regulators in the LTC3862-2. As a result, it is not possible to bias the $INTV_{CC}$ and $V_{IN}$ pins of the chip from separate power supplies. Independently biasing the $INTV_{CC}$ pin from a separate power supply can cause one of two possible failure modes during supply sequencing. If the $INTV_{CC}$ supply comes up before the $V_{IN}$ supply, high current will flow from the external $INTV_{CC}$ supply, through the body diode of the LDO PMOS device, to the input capacitor and $V_{IN}$ pin. This high current flow could trigger a latchup condition and cause catastrophic failure of the IC.

If, however, the $V_{IN}$ supply to the IC comes up before the $INTV_{CC}$ supply, the external $INTV_{CC}$ supply will act as a load to the internal LDO in the LTC3862-2, and the LDO will attempt to charge the $INTV_{CC}$ output with its short-circuit current. This will result in excessive power dissipation and possible thermal overload of the LTC3862-2.

### Programming the Output Voltage

The output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 1.223V\left(1+\frac{R2}{R1}\right)$$

The external resistor divider is connected to the output as shown in Figure 4. Resistor R1 is normally chosen so that the output voltage error caused by the current flowing out of the $V_{FB}$ pin during normal operation is negligible compared to the current in the divider. For an output voltage error due to the error amp input bias current of less than 0.5%, this translates to a maximum value of R1 of about 30k.

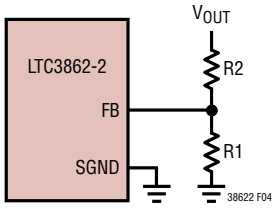



**Figure 4. Programming the Output Voltage with a Resistor Divider**

## OPERATION

### Operation of the RUN Pin

The control circuitry in the LTC3862-2 is turned on and off using the RUN pin. Pulling the RUN pin below 1.22V forces shutdown mode and releasing it allows a 0.5µA current source to pull this pin up, allowing a "normally on" converter to be designed. Alternatively, the RUN pin can be externally pulled up or driven directly by logic. Care must be taken not to exceed the absolute maximum rating of 8V for this pin.

The comparator on the RUN pin can also be used to sense the input voltage, allowing an undervoltage detection circuit to be designed. This is helpful in boost converter applications where the input current can reach very high levels at low input voltage:

$$I_{IN} = \frac{I_{OUT} \bullet V_{OUT}}{V_{IN}}$$

The 1.22V input threshold of the RUN comparator is derived from a precise bandgap reference, in order to maximize the accuracy of the undervoltage-sensing function. The RUN comparator has 80mV built-in hysteresis. When the voltage on the RUN pin exceeds 1.22V, the current sourced into the RUN pin is switched from 0.5µA to 5µA current. The user can therefore program both the rising threshold and the amount of hysteresis using the values of the resistors in the external divider, as shown in the following equations:

$$V_{IN(ON)} = 1.22V\left(1+\frac{R_A}{R_B}\right) - 0.5\mu \bullet R_A$$

$$V_{IN(OFF)} = 1.22V\left(1+\frac{R_A}{R_B}\right) - 5\mu \bullet R_A$$

Several of the possible RUN pin control techniques are illustrated in Figure 5.

### Frequency Selection and the Phase-Locked Loop

The selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires a larger inductor and output capacitor to maintain low output ripple.

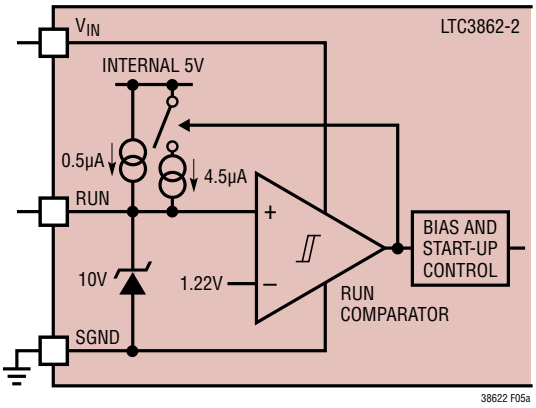



**Figure 5a. Using the RUN Pin for a "Normally On" Converter**

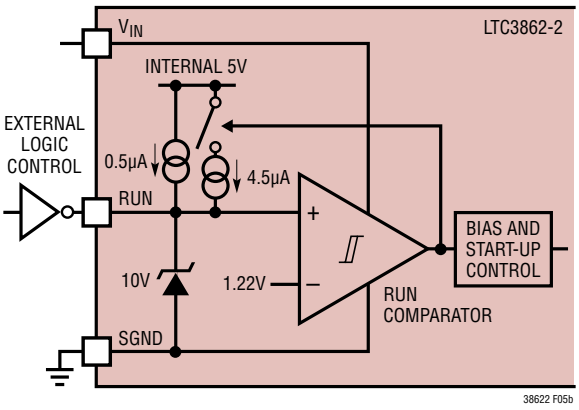



**Figure 5b. On/Off Control Using External Logic**

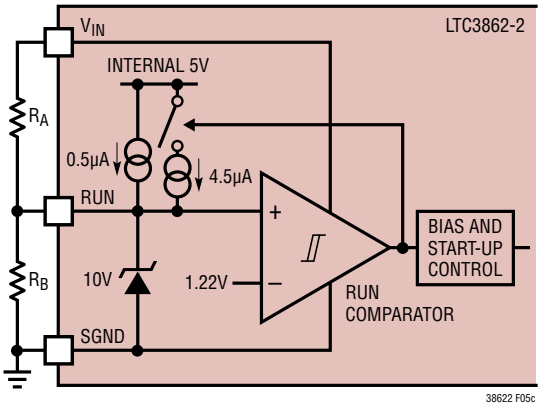



**Figure 5c. Programming the Input Voltage Turn-On and Turn-Off Thresholds Using the RUN Pin**

## OPERATION

The LTC3862-2 uses a constant frequency architecture that can be programmed over a 75kHz to 500kHz range using a single resistor from the FREQ pin to ground. Figure 6 illustrates the relationship between the FREQ pin resistance and the operating frequency.

The operating frequency of the LTC3862-2 can be approximated using the following formula:

$$R_{FREQ} = 5.5096E9(f_{OSC})^{-0.9255}$$

A phase-lock loop is available on the LTC3862-2 to synchronize the internal oscillator to an external clock source connected to the SYNC pin. Connect a series RC network from the PLLFLTR pin to SGND to compensate PLL's feedback loop. Typical compensation components are a 0.01µF capacitor in series with a 10k resistor. The PLLFLTR pin is both the output of the phase detector and the input to the voltage controlled oscillator (VCO). The LTC3862-2 phase detector adjusts the voltage on the PLLFLTR pin to align the rising edge of GATE1 to the leading edge of the external clock signal, as shown in Figure 7. The rising edge of GATE2 will depend upon the voltage on the PHASEMODE pin. The capture range of the LTC3862-2's PLL is 50kHz to 650kHz.

Because the operating frequency of the LTC3862-2 can be programmed using an external resistor, in synchronized applications, it is recommended that the free-running frequency (as defined by the external resistor) be set to the same value as the synchronized frequency. This results in a start-up of the IC at approximately the same frequency as the external clock, so that when the sync signal comes alive, no discontinuity at the output will be observed. It also ensures that the operating frequency remains essentially constant in the event the sync signal is lost. The SYNC pin has an internal 50k resistor to ground.

### Using the CLKOUT and PHASEMODE Pins in Multi-Phase Applications

The LTC3862-2 features two pins (CLKOUT and PHASEMODE) that allow multiple ICs to be daisy-chained together for higher current multi-phase applications. For a 3- or 4-phase design, the CLKOUT signal of the master controller is connected to the SYNC input of the slave controller in order to synchronize additional power stages for a single high current output. The PHASEMODE pin is used to adjust the phase relationship between channel 1 and channel 2, as well as the phase relationship between channel 1 and CLKOUT, as summarized in Table 1. The phases are calculated relative to the zero degrees, defined as the rising edge of the GATE1 output. In a 6-phase application the CLKOUT pin of the master controller connects to the SYNC input of the 2nd controller and the CLKOUT pin of the 2nd controller connects to the SYNC pin of the 3rd controller.

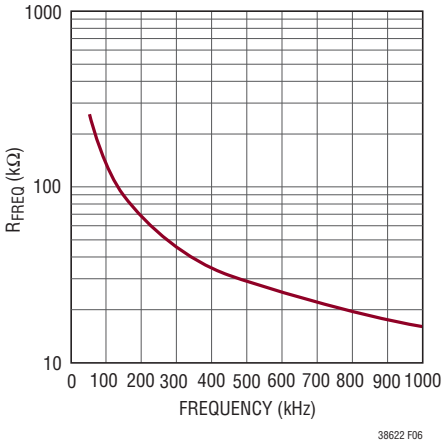



**Figure 6. FREQ Pin Resistor Value vs Frequency**

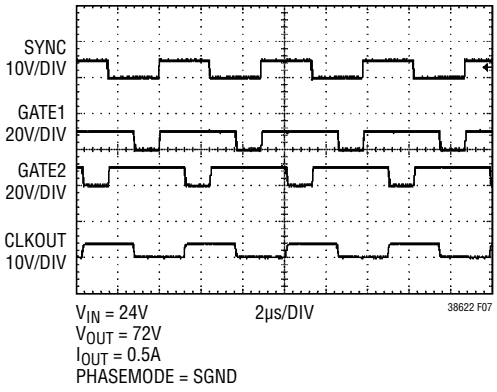



**Figure 7. Synchronization of the LTC3862-2 to an External Clock Using the PLL**

**Table 1**

| PHASEMODE | CH-1 to CH-2 PHASE | CH-1 to CLKOUT PHASE | APPLICATION |
|---|---|---|---|
| SGND | 180° | 90° | 2-Phase, 4-Phase |
| Float | 180° | 60° | 6-Phase |
| 3V8 | 120° | 240° | 3-Phase |

## OPERATION

### Using the LTC3862-2 Transconductance ($g_m$) Error Amplifier in Multi-Phase Applications

The LTC3862-2 error amplifier is a transconductance, or $g_m$ amplifier, meaning that it has high DC gain but high output impedance (the output of the error amplifier is a current proportional to the differential input voltage). This style of error amplifier greatly eases the task of implementing a multi-phase solution, because the amplifiers from two or more chips can be connected in parallel. In this case the FB pins of multiple LTC3862-2s can be connected together, as well as the ITH pins, as shown in Figure 8. The $g_m$ of the composite error amplifier is simply n times the transconductance of one amplifier, or $g_{m(TOT)} = n \bullet 660\mu S$, where n is the number of amplifiers connected in parallel. The transfer function from the ITH pin to the current comparator inputs was carefully designed to be accurate, both from channel-to-channel and chip-to-chip. This way the peak inductor current matching is kept accurate.

A buffered version of the output of the error amplifier determines the threshold at the input of the current comparator. The ITH voltage that represents zero peak current is 0.4V and the voltage that represents current limit is 1.2V (at low duty cycle). During an overload condition, the output of the error amplifier is clamped to 2.6V at low duty cycle, in order to reduce the latency when the overload condition terminates. A patented circuit in the LTC3862-2 is used to recover the slope compensation signal, so that the maximum peak inductor current is not a strong function of the duty cycle.

In multi-phase applications that use more than one LTC3862-2 controller, it is possible for ground currents on the PCB to disturb the control lines between the ICs, resulting in erratic behavior. In these applications the FB pins should be connected to each other through 100Ω resistors and each slave FB pin should be decoupled locally with a 100pF capacitor to ground, as shown in Figure 8.

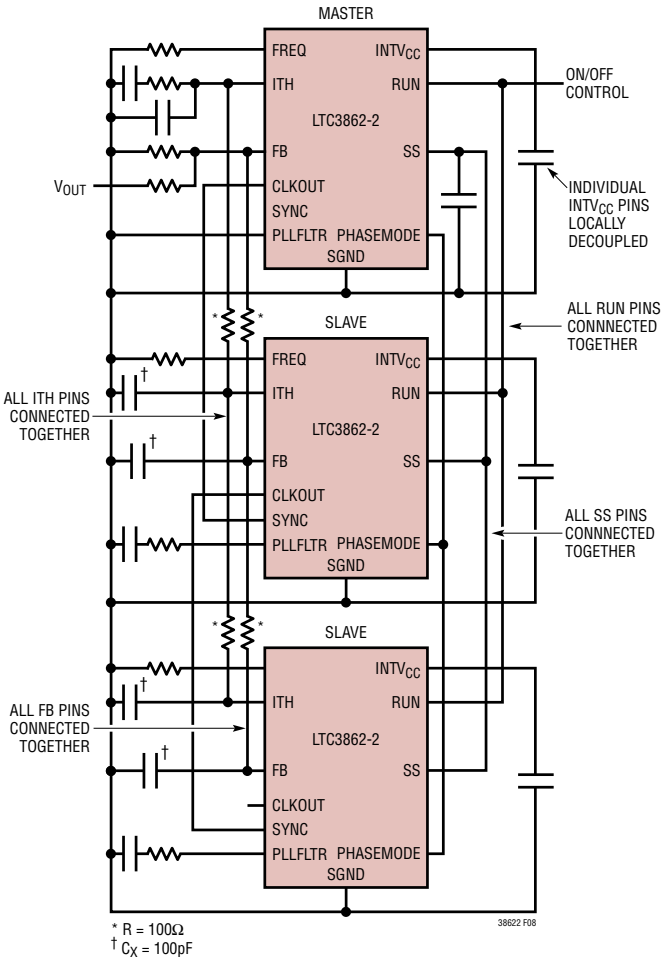



**Figure 8. LTC3862-2 Error Amplifier Configuration for Multi-Phase Operation**

### Soft-Start

The start-up of the LTC3862-2 is controlled by the voltage on the SS pin. An internal PNP transistor clamps the current comparator sense threshold during soft-start, thereby limiting the peak switch current. The base of the PNP is connected to the SS pin and the emitter to an internal, buffered ITH node (please note that the ITH pin voltage may not track the soft-start voltage during this time period). An internal 5µA current source charges the SS capacitor, and clamps the peak sense threshold until the voltage on the soft-start capacitor reaches approximately 0.6V. The required amount of soft-start capacitance can be estimated using the following equation:

$$C_{SS} = 5\mu A\left(\frac{t_{SS}}{0.6V}\right)$$

The SS pin has an internal open-drain NMOS pull-down transistor that turns on when the RUN pin is pulled low, when the voltage on the $INTV_{CC}$ pin is below its undervoltage lockout threshold, or during an overtemperature condition. In multi-phase applications that use more than

## OPERATION

one LTC3862-2 chip, connect all of the SS pins together and use one external capacitor to program the soft-start time. In this case, the current into the soft-start capacitor will be $I_{SS}$ = n • 5µA, where n is the number of SS pins connected together. Figure 9 illustrates the start-up waveforms for a 2-phase LTC3862-2 application.

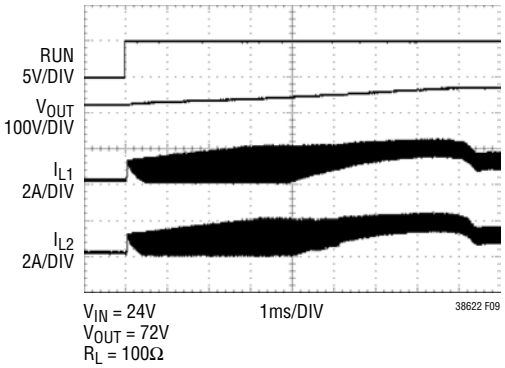



**Figure 9. Typical Start-Up Waveforms for a Boost Converter Using the LTC3862-2**

### Pulse-Skipping Operation at Light Load

As the load current is decreased, the controller enters discontinuous mode (DCM). The peak inductor current can be reduced until the minimum on-time of the controller is reached. Any further decrease in the load current will cause pulse-skipping to occur, in order to maintain output regulation, which is normal. The minimum on-time of the controller in this mode is approximately 210ns (with the blanking time set to its minimum value), the majority of which is leading edge blanking. Figure 10 illustrates the LTC3862-2 switching waveforms at the onset of pulse-skipping.

### Programmable Slope Compensation

For a current mode boost regulator operating in CCM, slope compensation must be added for duty cycles above 50%, in order to avoid subharmonic oscillation. For the LTC3862-2, this ramp compensation is internal and user adjustable. Having an internally fixed ramp compensation waveform normally places some constraints on the value of the inductor and the operating frequency. For example, with a fixed amount of internal slope compensation, using

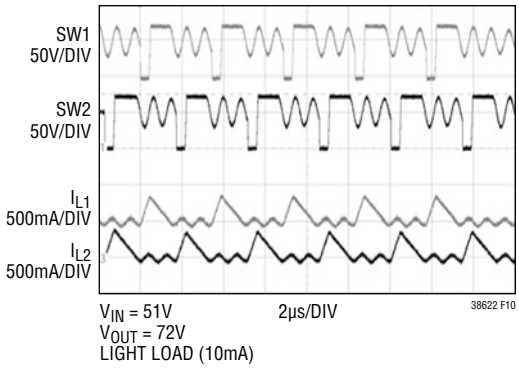



**Figure 10. Light Load Switching Waveforms for the LTC3862-2 at the Onset of Pulse-Skipping**

an excessively large inductor would result in too much effective slope compensation, and the converter could become unstable. Likewise, if too small an inductor were used, the internal ramp compensation could be inadequate to prevent subharmonic oscillation.

The LTC3862-2 contains a pin that allows the user to program the slope compensation gain in order to optimize performance for a wider range of inductance. With the SLOPE pin left floating, the normalized slope gain is 1.00. Connecting the SLOPE pin to ground reduces the normalized gain to 0.625 and connecting this pin to the 3V8 supply increases the normalized slope gain to 1.66.

With the normalized slope compensation gain set to 1.00, the design equations assume an inductor ripple current of 20% to 40%, as with previous designs. Depending upon the application circuit, however, a normalized gain of 1.00 may not be optimum for the inductor chosen. If the ripple current in the inductor is greater than 40%, the normalized slope gain can be increased to 1.66 (an increase of 66%) by connecting the SLOPE pin to the 3V8 supply. If the inductor ripple current is less than 20%, the normalized slope gain can be reduced to 0.625 (a decrease of 37.5%) by connecting the SLOPE pin to SGND.

To check the effectiveness of the slope compensation, apply a load step to the output and monitor the cycle-by-cycle behavior of the inductor current during the leading and trailing edges of the load current. Vary the input voltage over its full range and check for signs of cycle-by-cycle SW node instability or subharmonic oscillation. When the

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slope compensation is too low the converter can suffer from excessive jitter or, worst case, subharmonic oscillation. When excess slope compensation is applied to the internal current sense signal, the phase margin of the control loop suffers. Figure 11 illustrates inductor current waveforms for a properly compensated loop.

The LTC3862-2 contains a patented circuit whereby most of the applied slope compensation is recovered, in order to provide a $SENSE^+$ to $SENSE^-$ threshold which is not a strong function of the duty cycle. This sense threshold is, however, a function of the programmed slope gain, as shown in Figure 12. The data sheet typical specification of 75mV for $SENSE^+$ minus $SENSE^-$ is measured at a normalized slope gain of 1.00 at low duty cycle. For applications where the normalized slope gain is not 1.00, use Figure 12 to determine the correct value of the sense resistor.

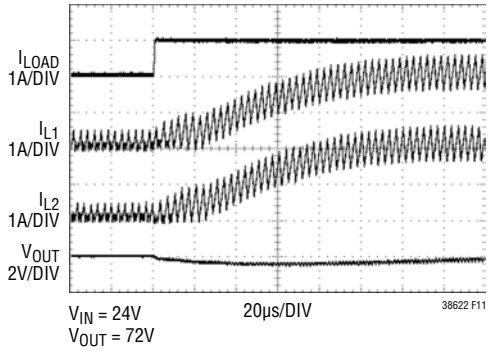


**Figure 11. Inductor Current Waveforms for a Properly Compensated Control Loop**

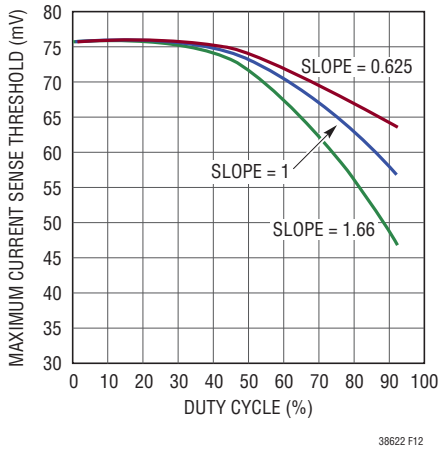


**Figure 12. Effect of Slope Gain on the Peak SENSE Threshold**

### Programmable Blanking and the Minimum On-Time

The BLANK pin on the LTC3862-2 allows the user to program the amount of leading edge blanking at the SENSE pins. Connecting the BLANK pin to SGND results in a minimum on-time of 210ns, floating the pin increases this time to 290ns, and connecting the BLANK pin to the 3V8 supply results in a minimum on-time of 375ns. The majority of the minimum on-time consists of this leading edge blanking, due to the inherently low propagation delay of the current comparator (25ns typ) and logic circuitry (10ns to 15ns).

The purpose of leading edge blanking is to filter out noise on the SENSE pins at the leading edge of the power MOSFET turn-on. During the turn-on of the power MOSFET the gate drive current, the discharge of any parasitic capacitance on the SW node, the recovery of the boost diode charge, and parasitic series inductance in the high di/dt path all contribute to overshoot and high frequency noise that could cause false-tripping of the current comparator. Due to the wide range of applications the LTC3862-2 is well-suited to, fixing one value of the internal leading edge blanking time would have required the longest delay time to have been used. Providing a means to program the blank time allows users to optimize the SENSE pin filtering for each application. Figure 13 illustrates the effect of the programmable leading edge blank time on the minimum on-time of a boost converter.

### Programmable Maximum Duty Cycle

In order to maintain constant frequency and a low output ripple voltage, a single-ended boost (or flyback or SEPIC) converter is required to turn off the switch every cycle for some minimum amount of time. This off-time allows the transfer of energy from the inductor to the output capacitor and load, and prevents excessive ripple current and voltage. For inductor-based topologies like boost and SEPIC converters, having a maximum duty cycle as close as possible to 100% may be desirable, especially in low $V_{IN}$ to high $V_{OUT}$ applications. However, for transformer-based solutions, having a maximum duty cycle near 100% is undesirable, due to the need for V • sec reset during the primary switch off-time.

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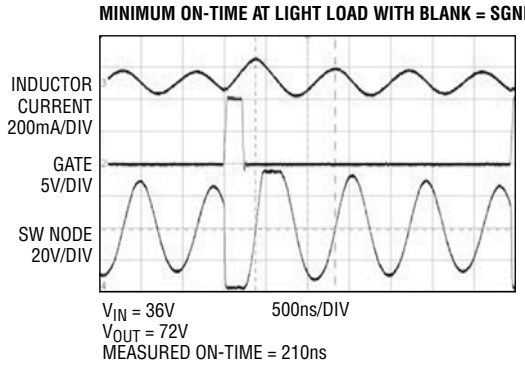


**Figure 13. Leading Edge Blanking Effects on the Minimum On-Time**

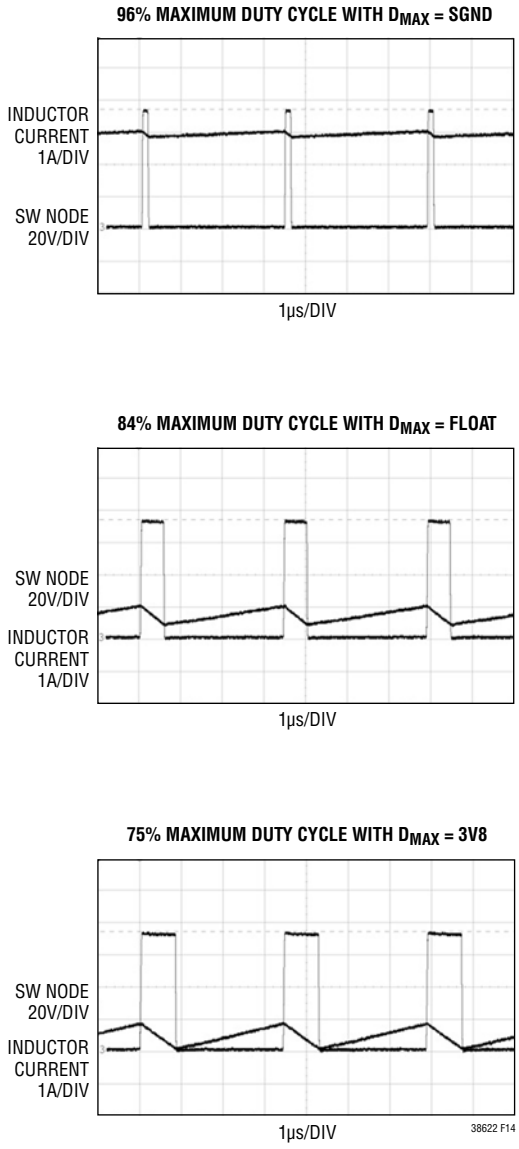


**Figure 14. SW Node Waveforms with Different Duty Cycle Limits**

In order to satisfy these different applications requirements, the LTC3862-2 has a simple way to program the maximum duty cycle. Connecting the $D_{MAX}$ pin to SGND limits the maximum duty cycle to 96%. Floating this pin limits the duty cycle to 84% and connecting the $D_{MAX}$ pin to the 3V8 supply limits it to 75%. Figure 14 illustrates the effect of limiting the maximum duty cycle on the SW node waveform of a boost converter.

The LTC3862-2 contains an oscillator that runs at 12× the programmed switching frequency, in order to provide for 2-, 3-, 4-, 6- and 12-phase operation. A digital counter is used to divide down the fundamental oscillator frequency in order to obtain the operating frequency of the gate drivers. **Since the maximum duty cycle limit is obtained from this digital counter, the percentage maximum duty cycle does not vary with process tolerances or temperature.**

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### The SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are high impedance inputs to the CMOS current comparators for each channel. Nominally, there is no DC current into or out of these pins. There are ESD protection diodes connected from these pins to SGND, although even at hot temperature the leakage current into the SENSE+ and SENSE– pins should be less than 1µA.

Since the LTC3862-2 contains leading edge blanking, an external RC filter is not required for proper operation. However, if an external filter is used, the filter components should be placed close to the SENSE+ and SENSE– pins on the IC, as shown in Figure 15. The positive and negative sense node traces should then run parallel to each other to a Kelvin connection underneath the sense resistor, as shown in Figure 16. Sensing current elsewhere on the board can add parasitic inductance and capacitance to the current sense element, degrading the information at the sense pins and making the programmed current limit unpredictable. Avoid the temptation to connect the SENSE– line to the ground plane using a PCB via; this could result in unpredictable behavior.

The sense resistor should be connected to the source of the power MOSFET and the ground node using short, wide PCB traces, as shown in Figure 16. Ideally, the bottom terminal of the sense resistors will be immediately adjacent to the negative terminal of the output capacitor, since this path is a part of the high di/dt loop formed by the switch, boost diode, output capacitor and sense resistor. Placement of the inductors is less critical, since the current in the inductors is a triangle waveform.

### Checking the Load Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, $V_{OUT}$ shifts by an amount equal to $\Delta I_{LOAD}$ (ESR), where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$, generating the feedback error signal that forces the regulator to adapt to the current change and return $V_{OUT}$ to its steady-state value. During this recovery time $V_{OUT}$ can be monitored for excessive overshoot or ringing, which would indicate a stability problem.

The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

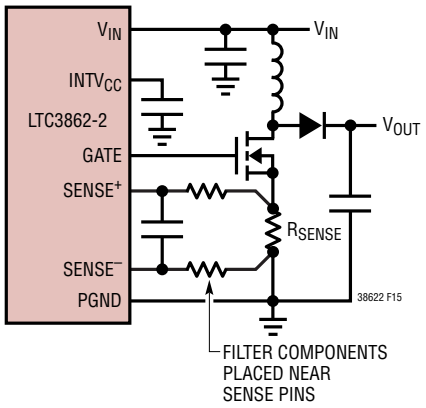


**Figure 15. Proper Current Sense Filter Component Placement**

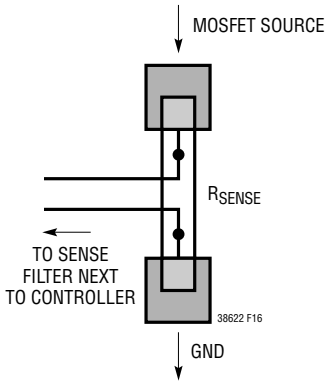


**Figure 16. Connecting the SENSE+ and SENSE– Traces to the Sense Resistor Using a Kelvin Connection**

## OPERATION

The ITH series $R_C$ • $C_C$ filter sets the dominant pole-zero loop compensation. The transfer function for boost and flyback converters contains a right half plane zero that normally requires the loop crossover frequency to be reduced significantly in order to maintain good phase margin. The $R_C$ • $C_C$ filter values can typically be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type(s) and value(s) have been determined. The output capacitor configuration needs to be selected in advance because the effective ESR and bulk capacitance have a significant effect on the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET and load resistor directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a fast load step condition. The initial output voltage step resulting from the step change in the output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing $R_C$ and the bandwidth of the loop will be increased by decreasing $C_C$. If $R_C$ is increased by the same factor that $C_C$ is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. Figure 17 illustrates the load step response of a properly compensated boost converter.

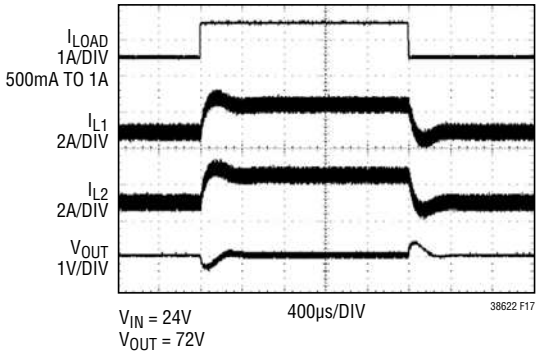


**Figure 17. Load Step Response of a Properly Compensated Boost Converter**

# APPLICATIONS INFORMATION

### Typical Boost Applications Circuit

A basic 2-phase, single output LTC3862-2 application circuit is shown in Figure 18. External component selection is driven by the characteristics of the load and the input supply.

### Duty Cycle Considerations

For a boost converter operating in a continuous conduction mode (CCM), the duty cycle of the main switch is:

$$D = \left( \frac{V_O + V_F - V_{IN}}{V_O + V_F} \right) = t_{ON} \bullet f$$

where $V_F$ is the forward voltage of the boost diode. The minimum on-time for a given application operating in CCM is:

$$t_{ON(MIN)} = \frac{1}{f}\left( \frac{V_O + V_F - V_{IN(MAX)}}{V_O + V_F} \right)$$

For a given input voltage range and output voltage, it is important to know how close the minimum on-time of the application comes to the minimum on-time of the control IC. The LTC3862-2 minimum on-time can be programmed from 210ns to 375ns using the BLANK pin.

### Minimum On-Time Limitations

In a single-ended boost converter, two steady-state conditions can result in operation at the minimum on-time of the controller. The first condition is when the input voltage is close to the output voltage. When $V_{IN}$ approaches $V_{OUT}$ the voltage across the inductor approaches zero during the switch off-time. Under this operating condition the converter can become unstable and the output can experience high ripple voltage oscillation at audible frequencies. For applications where the input voltage can approach or exceed the output voltage, consider using a SEPIC or buck-boost topology instead of a boost converter.

The second condition that can result in operation at the minimum on-time of the controller is at light load, in deep discontinuous mode. As the load current is decreased, the on-time of the switch decreases, until the minimum on-time limit of the controller is reached. Any further decrease in the output current will result in pulse-skipping, a typically benign condition where cycles are skipped in order to maintain output regulation.

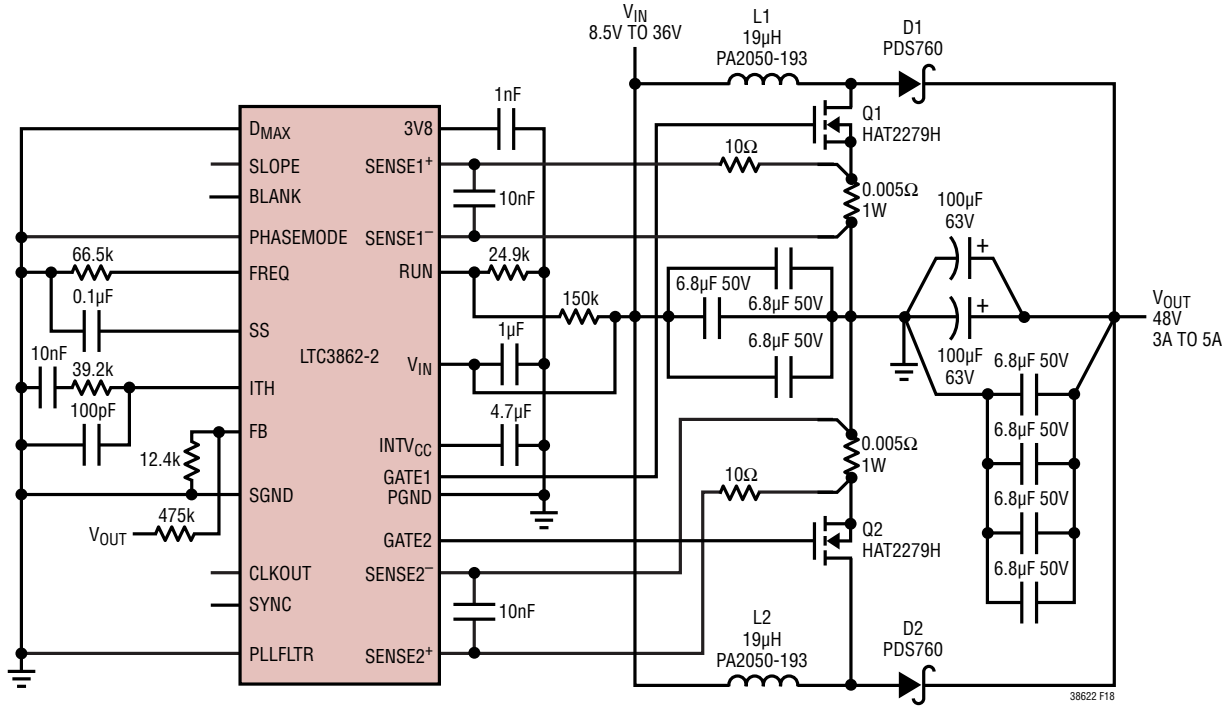


**Figure 18. A Typical 2-Phase, Single Output Boost Converter Application Circuit**