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Dual, 2-Phase Synchronous Step-Down DC/DC Controllers

FEATURES

- Dual, 180° Phased Controllers Reduce Required Input Capacitance and Power Supply Induced Noise
- Accurate Multiphase Current Matching
- R_{SENSE} or DCR Current Sensing
- $\pm 0.75\%$ 0.6V Output Voltage Accuracy
- Phase-Lockable Fixed Frequency 250kHz to 780kHz
- High Efficiency: Up to 95%
- Dual N-channel MOSFET Synchronous Drive
- Wide V_{IN} Range: 4V to 38V (40V Max) Operation
- Wide V_{OUT} Range: 0.6V to 12.5V Operation
- Adjustable Soft-Start Current Ramping or Tracking
- Foldback Output Current Limiting
- Output Overvoltage Protection
- Power Good Output Voltage Monitor
- 5V Low Dropout Regulator
- Small 28-Lead QFN and Narrow SSOP Packages

APPLICATIONS

- Server Systems
- Telecom Systems
- Industrial and Medical Instruments
- High Power Battery-Operated Devices
- DC Power Distribution Systems

DESCRIPTION

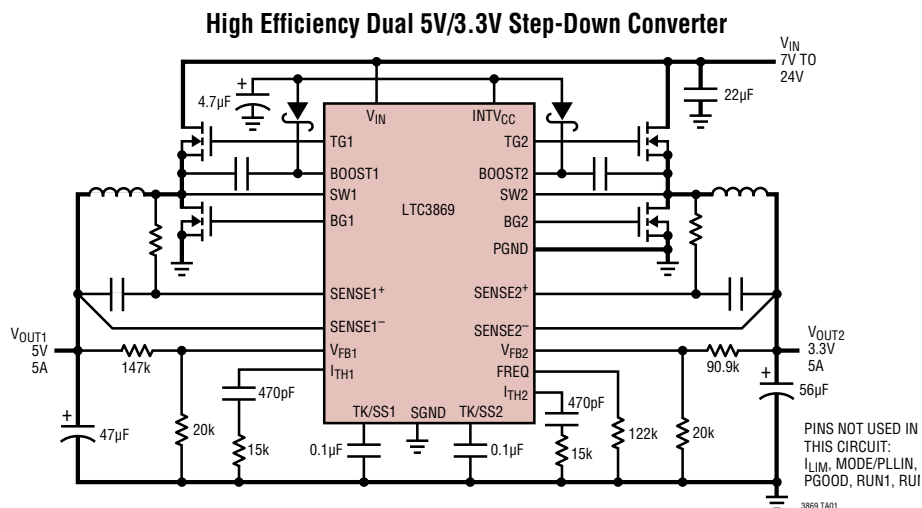
The **LTC[®]3869** is a high performance dual synchronous step-down switching regulator controller that drives all N-channel synchronous power MOSFET stages. A constant frequency current mode architecture allows a phase-lockable frequency of up to 780kHz. Power loss and noise due to the ESR of the input capacitors are minimized by operating the two controller output stages out-of-phase.

OPTI-LOOP[®] compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. A wide 4V to 38V input supply range encompasses most battery chemistries. Independent TK/SS pins for each controller ramp the output voltage during start-up. Current foldback limits MOSFET heat dissipation during short-circuit conditions. The MODE/PLLIN pin selects among Burst Mode[®] operation, pulse-skipping mode, or continuous inductor current mode and allows the IC to be synchronized to an external clock.

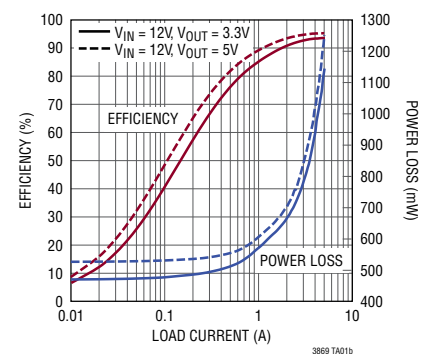
The LTC3869 is available in low profile 4mm × 4mm and 4mm × 5mm QFN packages. The LTC3869-2 is available in an SSOP-28 package. The LTC3869 is pin-compatible with the LTC3850.

LT, LT, LTC, LTM, Linear Technology, the Linear logo, μ Module, OPTI-LOOP, Burst Mode and PolyPhase are registered trademarks and No R_{SENSE} is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents including 5481178, 5705919, 5929620, 6100678, 6144194, 6177787, 6580258, 6498466, 6611131.

TYPICAL APPLICATION



Efficiency and Power Loss

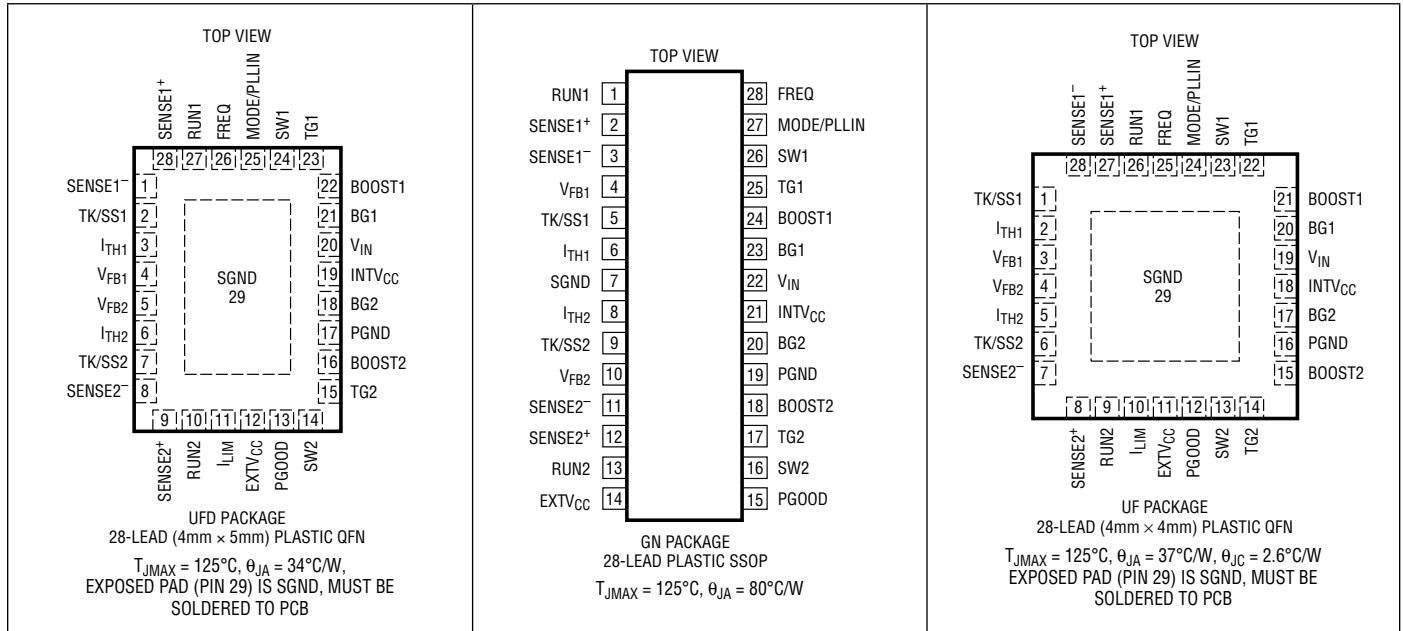


LTC3869/LTC3869-2

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage: V_{IN}	40V to $-0.3V$	I_{TH1} , I_{TH2} , V_{FB1} , V_{FB2} Voltages	$INTV_{CC}$ to $-0.3V$
Top Side Driver Voltages:		$INTV_{CC}$ Peak Output Current	100mA
BOOST1, BOOST2	46V to $-0.3V$	Operating Junction Temperature Range	
Switch Voltage: SW1, SW2	40V to $-5V$	(Note 2).....	$-40^{\circ}C$ to $125^{\circ}C$
$INTV_{CC}$, RUN1, RUN2, PGOOD, $EXTV_{CC}$,		Junction Temperature (Note 3)	$125^{\circ}C$
BOOST1-SW1, BOOST2-SW2.....	6V to $-0.3V$	Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
SENSE1 ⁺ , SENSE2 ⁺ , SENSE1 ⁻ ,		Lead Temperature (Soldering, 10 sec)	
SENSE2 ⁻ Voltages	13V to $-0.3V$	GN Package	$300^{\circ}C$
MODE/PLLIN, I_{LIM} , TK/SS1, TK/SS2,			
FREQ Voltages	$INTV_{CC}$ to $-0.3V$		

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3869EUF#PBF	LTC3869EUF#TRPBF	3869	28-Lead (4mm × 4mm) Plastic QFN	$-40^{\circ}C$ to $125^{\circ}C$
LTC3869IUF#PBF	LTC3869IUF#TRPBF	3869	28-Lead (4mm × 4mm) Plastic QFN	$-40^{\circ}C$ to $125^{\circ}C$
LTC3869EUF#PBF	LTC3869EUF#TRPBF	3869	28-Lead (4mm × 5mm) Plastic QFN	$-40^{\circ}C$ to $125^{\circ}C$
LTC3869IUF#PBF	LTC3869IUF#TRPBF	3869	28-Lead (4mm × 5mm) Plastic QFN	$-40^{\circ}C$ to $125^{\circ}C$
LTC3869IGN-2#PBF	LTC3869IGN-2#TRPBF	LTC3869GN-2	28-Lead Narrow Plastic SSOP	$-40^{\circ}C$ to $125^{\circ}C$

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 2). $V_{IN} = 15\text{V}$, $V_{RUN1,2} = 5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Main Control Loops						
V_{IN}	Input Voltage Range		4		38	V
V_{OUT}	Output Voltage Range		0.6		12.5	V
$V_{FB1,2}$	Regulated Feedback Voltage (Notes 2, 4)	$I_{TH1,2}$ Voltage = 1.2V, 0°C to 85°C $I_{TH1,2}$ Voltage = 1.2V, -40°C to 125°C	● 0.5955 ● 0.5940	0.600 0.600	0.6045 0.6060	V V
$I_{FB1,2}$	Feedback Current	(Note 4)		-15	-50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	$V_{IN} = 4.0\text{V}$ to 38V (Note 4)		0.002	0.01	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 1.6V	● ●	0.01 -0.01	0.1 -0.1	% %
$g_{m1,2}$	Transconductance Amplifier g_m	$I_{TH1,2} = 1.2\text{V}$; Sink/Source $5\mu\text{A}$; (Note 4)		2		mmho
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 5) $V_{IN} = 15\text{V}$ $V_{RUN1,2} = 0\text{V}$		3 30	50	mA μA
DF_{MAX}	Maximum Duty Factor	In Dropout	94	95		%
$UVLO$	Undervoltage Lockout	V_{INTVCC} Ramping Down	● 3.0	3.2	3.4	V
$UVLO_{HYS}$	UVLO Hysteresis			0.6		V
V_{OVL}	Feedback Overvoltage Lockout	Measured at $V_{FB1,2}$	● 0.64	0.66	0.68	V
I_{SENSE}	Sense Pins Bias Current	(Each Channel); $V_{SENSE1,2} = 3.3\text{V}$	●	± 1	± 2	μA
$I_{TK/SS1,2}$	Soft-Start Charge Current	$V_{TK/SS1,2} = 0\text{V}$	● 1.0	1.25	1.5	μA
$V_{RUN1,2}$	RUN Pin On Threshold	V_{RUN1} , V_{RUN2} Rising	● 1.1	1.22	1.35	V
$V_{RUN1,2(HYS)}$	RUN Pin On Hysteresis			80		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold, 0°C to 85°C (Note 2)	$V_{FB1,2} = 0.5\text{V}$, $V_{SENSE1,2} = 3.3\text{V}$, $I_{LIM} = 0\text{V}$	● 25	30	35	mV
		$V_{FB1,2} = 0.5\text{V}$, $V_{SENSE1,2} = 3.3\text{V}$, $I_{LIM} = \text{Float}$	● 45	50	55	mV
		$V_{FB1,2} = 0.5\text{V}$, $V_{SENSE1,2} = 3.3\text{V}$, $I_{LIM} = \text{INTVCC}$	● 68	75	82	mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold, -40°C to 125°C (Note 2)	$V_{FB1,2} = 0.5\text{V}$, $V_{SENSE1,2} = 3.3\text{V}$, $I_{LIM} = 0\text{V}$	● 23	30	37	mV
		$V_{FB1,2} = 0.5\text{V}$, $V_{SENSE1,2} = 3.3\text{V}$, $I_{LIM} = \text{Float}$	● 43	50	57	mV
		$V_{FB1,2} = 0.5\text{V}$, $V_{SENSE1,2} = 3.3\text{V}$, $I_{LIM} = \text{INTVCC}$	● 68	75	82	mV
		$V_{FB1,2} = 0.5\text{V}$, $V_{SENSE1,2} = 3.3\text{V}$, LTC3869IGN-2	● 40	50	60	mV
$V_{MISMATCH}$	Channel to Channel Current Sense Mismatch Voltage of $V_{SENSE(MAX)}$	$I_{LIM} = \text{Float}$			2	mV
TG1, 2 t_r TG1, 2 t_f	TG Transition Time: Rise Time Fall Time	(Note 8) $C_{LOAD} = 3300\text{pF}$ $C_{LOAD} = 3300\text{pF}$		25		ns ns
				25		
BG1, 2 t_r BG1, 2 t_f	BG Transition Time: Rise Time Fall Time	(Note 8) $C_{LOAD} = 3300\text{pF}$ $C_{LOAD} = 3300\text{pF}$		25		ns ns
				25		
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	$C_{LOAD} = 3300\text{pF}$ Each Driver (Note 6)		30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	$C_{LOAD} = 3300\text{pF}$ Each Driver (Note 6)		30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)		90		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 2). $V_{IN} = 15\text{V}$, $V_{RUN1,2} = 5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTV_{CC} Linear Regulator						
V_{INTVCC}	Internal V_{CC} Voltage	$6\text{V} < V_{IN} < 38\text{V}$	4.8	5	5.2	V
$V_{LDO INT}$	INTV _{CC} Load Regulation	$I_{CC} = 0\text{mA}$ to 20mA		0.5	2	%
V_{EXTVCC}	EXTV _{CC} Switchover Voltage	EXTV _{CC} Ramping Positive	● 4.5	4.7		V
V_{LDOHYS}	EXTV _{CC} Hysteresis			200		mV
$V_{LDO EXT}$	EXTV _{CC} Voltage Drop	$I_{CC} = 20\text{mA}$, $V_{EXTVCC} = 5\text{V}$		50	100	mV
PGOOD Output						
V_{PGL}	PGOOD Voltage Low	$I_{PGOOD} = 2\text{mA}$		0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	$V_{PGOOD} = 5\text{V}$			±2	μA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive		-10 10		% %
Oscillator and Phase-Locked Loop						
f_{NOM}	Nominal Frequency	$V_{FREQ} = 1.2\text{V}$	450	500	550	kHz
f_{LOW}	Lowest Frequency	$V_{FREQ} = 0\text{V}$	210	250	290	kHz
f_{HIGH}	Highest Frequency	$V_{FREQ} \geq 2.4\text{V}$	700	780	850	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance			250		kΩ
I_{FREQ}	Frequency Setting Current		9	10	11	μA
On Chip Driver						
TG R_{UP}	TG Pull-Up $R_{DS(ON)}$	TG High		2.6		Ω
TG R_{DOWN}	TG Pull-Down $R_{DS(ON)}$	TG Low		1.5		Ω
BG R_{UP}	BG Pull-Up $R_{DS(ON)}$	BG High		2.4		Ω
BG R_{DOWN}	BG Pull-Down $R_{DS(ON)}$	BG Low		1.1		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3869 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3869E is guaranteed to meet performance specifications from 0°C to 85°C . Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3869I is guaranteed to meet performance specifications over the full -40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

$$\text{LTC3869UFD: } T_J = T_A + (P_D \cdot 34^\circ\text{C/W})$$

$$\text{LTC3869GN-2: } T_J = T_A + (P_D \cdot 80^\circ\text{C/W})$$

$$\text{LTC3869UFD: } T_J = T_A + (P_D \cdot 37^\circ\text{C/W})$$

Note 4: The LTC3869 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant $V_{FB1,2}$.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

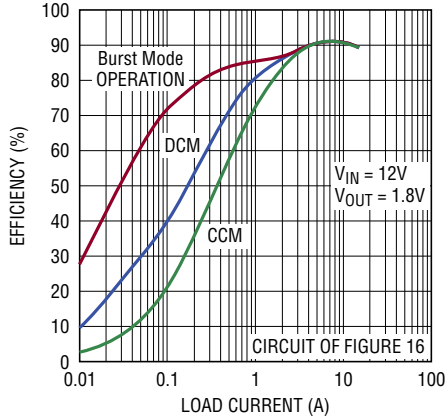
Note 6: Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current $\geq 40\%$ of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

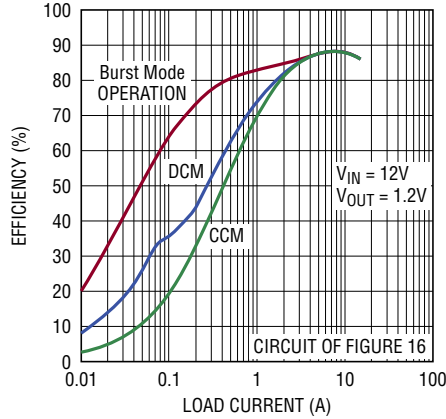
Note 8: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.

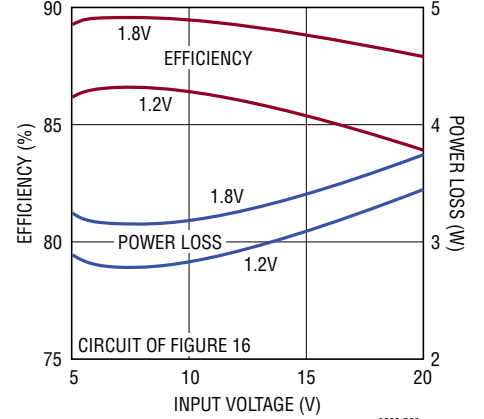
Efficiency vs Output Current and Mode



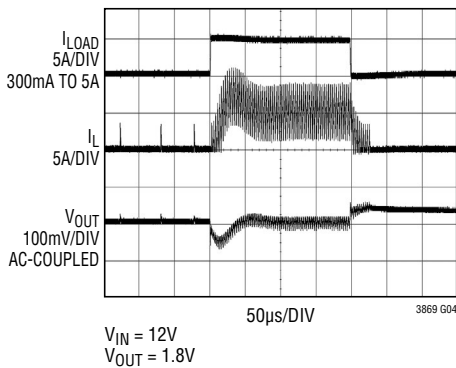
Efficiency vs Output Current and Mode



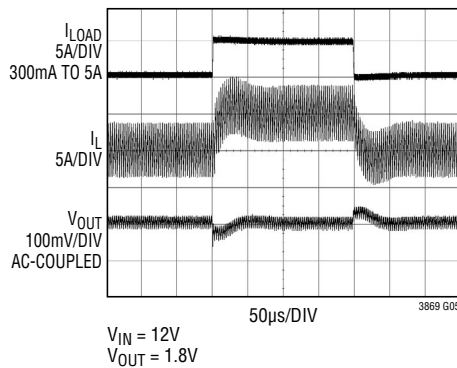
Full Load Efficiency and Power Loss vs Input Voltage



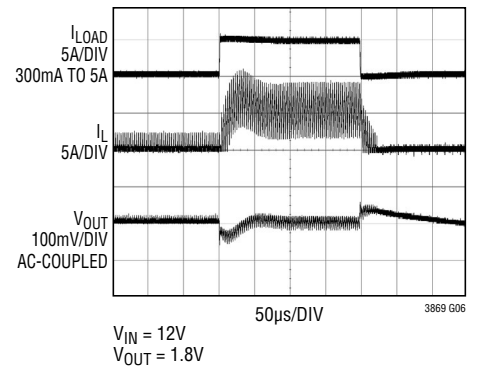
Load Step (Burst Mode Operation)



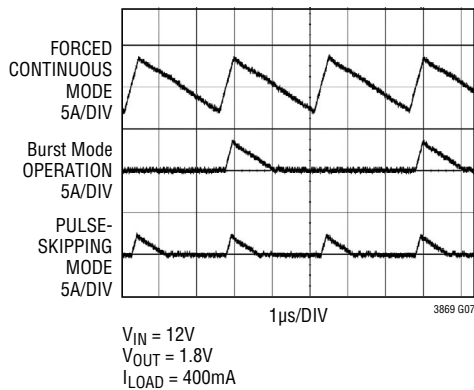
Load Step (Forced Continuous Mode)



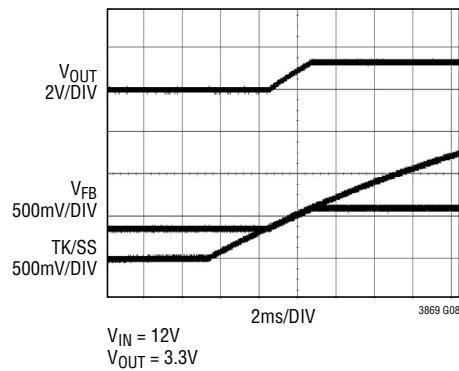
Load Step (Pulse-Skipping Mode)



Inductor Current at Light Load

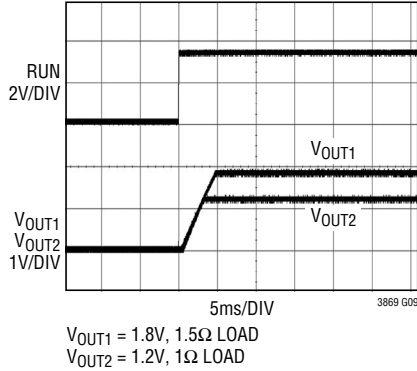


Prebiased Output at 2V

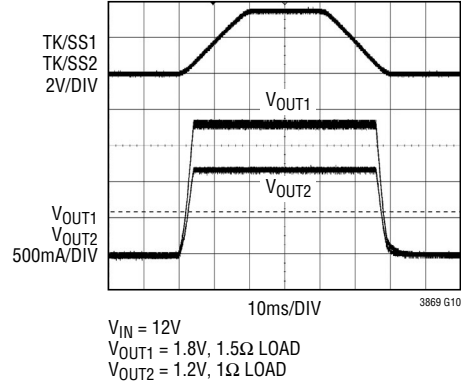


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.

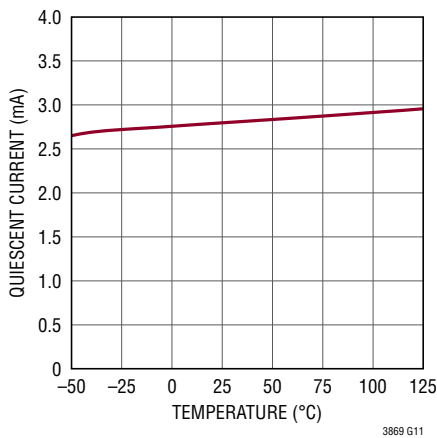
Coincident Tracking



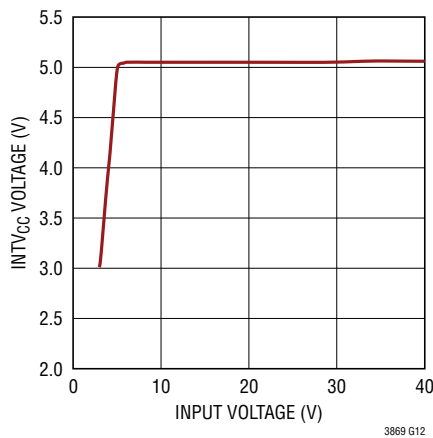
Tracking Up and Down with External Ramp



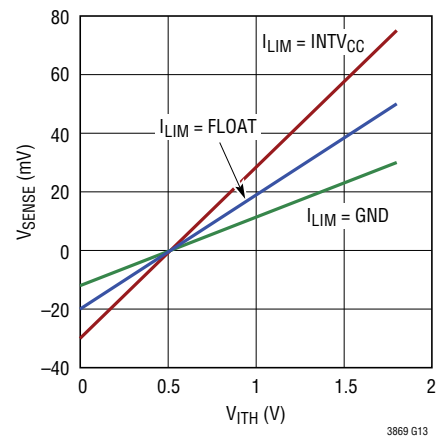
Quiescent Current without EXT V_{CC} vs Temperature



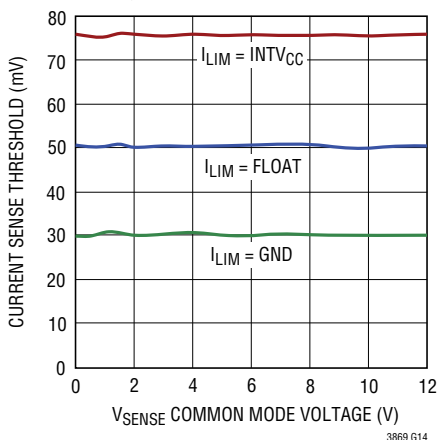
INT V_{CC} Line Regulation



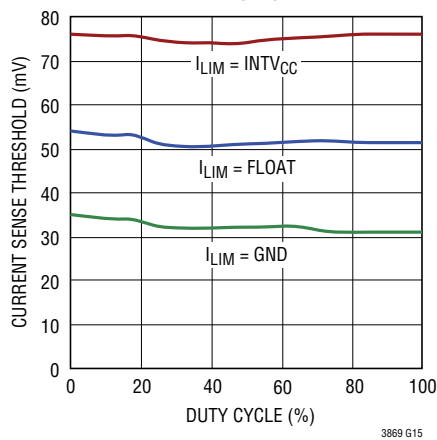
Current Sense Threshold vs I_{TH} Voltage



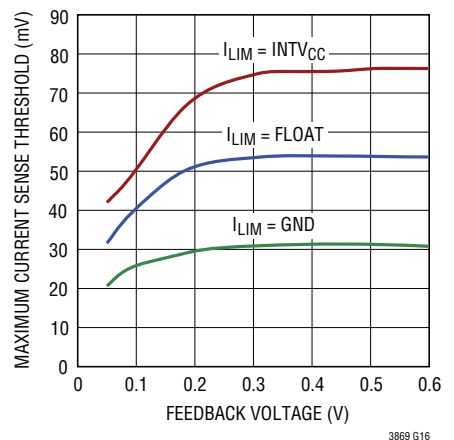
Maximum Current Sense Threshold vs Common Mode Voltage



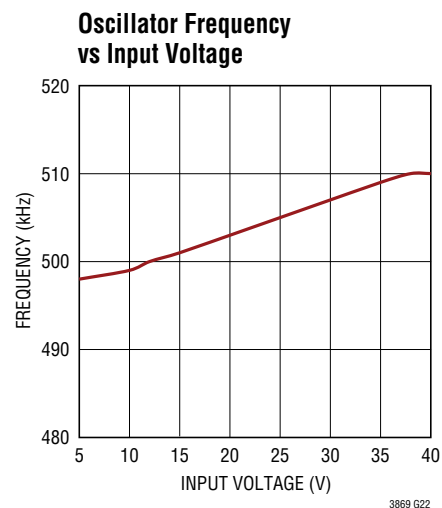
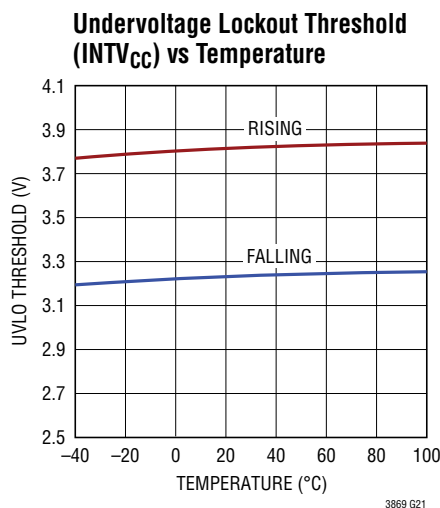
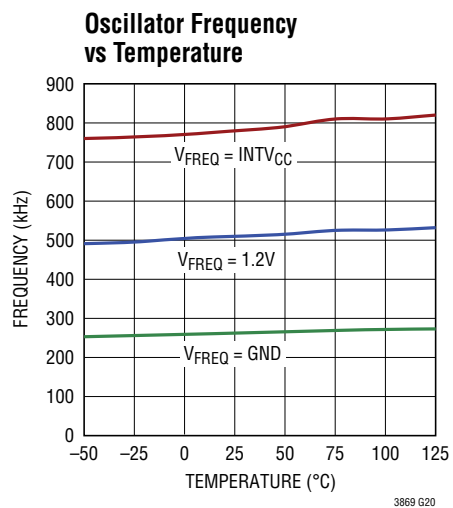
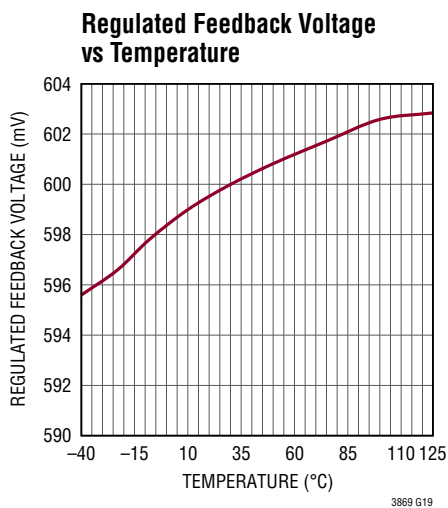
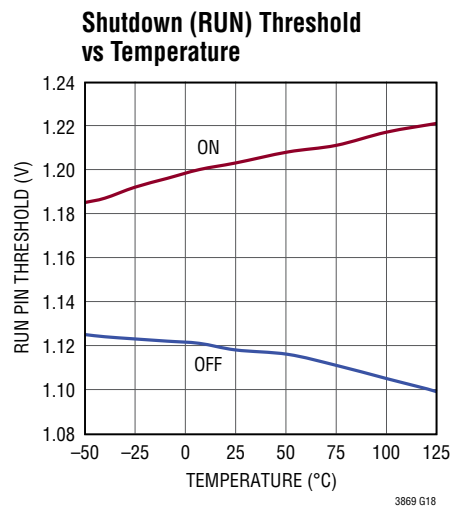
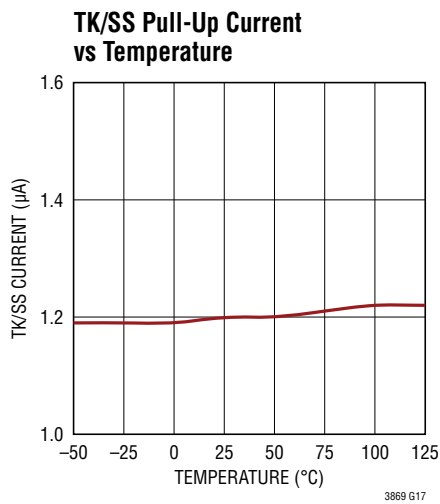
Maximum Current Sense Threshold vs Duty Cycle



Maximum Current Sense Voltage vs Feedback Voltage (Current Foldback)

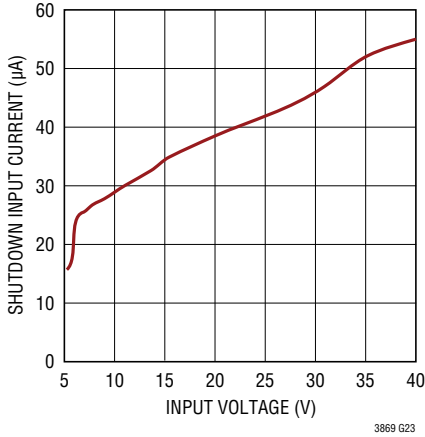


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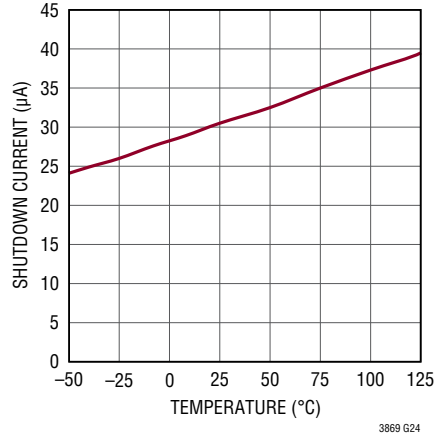


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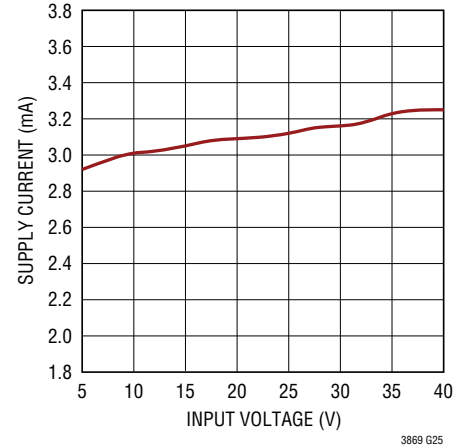
Shutdown Current vs Input Voltage



Shutdown Current vs Temperature



Quiescent Current vs Input Voltage without EXT_{VC}



PIN FUNCTIONS (UF/UFD/GN)

RUN1, RUN2 (Pin 26, Pin 9/Pin 27, Pin 10/Pin 1, Pin 13): Run Control Inputs. A voltage above 1.2V on either pin turns on the IC. However, forcing either of these pins below 1.2V causes the IC to shut down the circuitry required for that particular channel. There are 1 μ A pull-up currents for these pins. Once the RUN pin raises above 1.2V, an additional 4.5 μ A pull-up current is added to the pin.

V_{FB1}, V_{FB2} (Pin 3, Pin 4/Pin 4, Pin 5/Pin 4, Pin 10): Error Amplifier Feedback Inputs. These pins receive the remotely sensed feedback voltages for each channel from external resistive dividers across the outputs.

I_{TH1}, I_{TH2} (Pin 2, Pin 5/Pin 3, Pin 6/Pin 6, Pin 8): Current Control Thresholds and Error Amplifier Compensation Points. Each associated channels' current comparator tripping threshold increases with its I_{TH} control voltage.

SGND (Pin 29/Pin 29/Pin 7): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point. Pin 29 is the exposed pad, only available for the UF/UFD package. The exposed pad must be soldered to PCB ground for electrical connection and rated thermal performance.

TK/SS1, TK/SS2 (Pin 1, Pin 6/Pin 2, Pin 7/Pin 5, Pin 9): Output Voltage Tracking and Soft-Start Inputs. When one particular channel is configured to be the master of two channels, a capacitor to ground at this pin sets the ramp rate for the master channel's output voltage. When the channel is configured to be the slave of two channels, the V_{FB} voltage of the master channel is reproduced by a resistor divider and applied to this pin. Internal soft-start currents of 1.2 μ A are charging these pins.

MODE/PLLIN (Pin 24/Pin 25/Pin 27): Forced Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force both chan-

nels in continuous mode of operation. Connect to INTV_{CC} to enable pulse-skipping mode of operation. Leave the pin floating will enable Burst Mode operation. A clock on the pin will force the controller into continuous mode of operation and synchronize the internal oscillator with the clock on this pin. The PLL compensation components are integrated inside the IC.

FREQ (Pin 25/Pin 26/Pin 28): There is a precision 10 μ A current flowing out of this pin. Connect a resistor to ground set the controllers' operating frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

I_{LIM} (Pin 10/Pin 11/NA): Current Comparator Sense Voltage Range Inputs. This pin is to be programmed to SGND, FLOAT or INTV_{CC} to set the maximum current sense threshold to three different levels for each comparator. The current limit default value is set to be 50mV for LTC3869GN-2.

EXTV_{CC} (Pin 11/Pin 12/Pin 14): External Power Input to an Internal Switch Connected to INTV_{CC}. This switch closes and supplies the IC power, bypassing the internal low dropout regulator, whenever EXTV_{CC} is higher than 4.7V. Do not exceed 6V on this pin.

V_{IN} (Pin 19/Pin 20/Pin 22): Main Input Supply. Decouple this pin to PGND with a capacitor (0.1 μ F to 1 μ F).

BOOST1, BOOST2 (Pin 21, Pin 15/Pin 22, Pin 16/Pin 24, Pin 18): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitors connect to these pins. These pins swing from a diode voltage drop below INTV_{CC} up to V_{IN} + INTV_{CC}.

TG1, TG2 (Pin 22, Pin 14/Pin 23, Pin 15/Pin 25, Pin 17): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to INTV_{CC} superimposed on the switch nodes voltages.

PIN FUNCTIONS (UF/UFD/GN)

SW1, SW2 (Pin 23, Pin 13/Pin 24, Pin 14/Pin 26, Pin 16): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN} .

SENSE1+, SENSE2+ (Pin 27, Pin 8/Pin 28, Pin 9/Pin 2, Pin 12): Current Sense Comparator Inputs. The (+) inputs to the current comparators are normally connected to DCR sensing networks or current sensing resistors.

SENSE1-, SENSE2- (Pin 28, Pin 7/Pin 1, Pin 8/Pin 3, Pin 11): Current Sense Comparator Inputs. The (-) inputs to the current comparators are connected to the outputs.

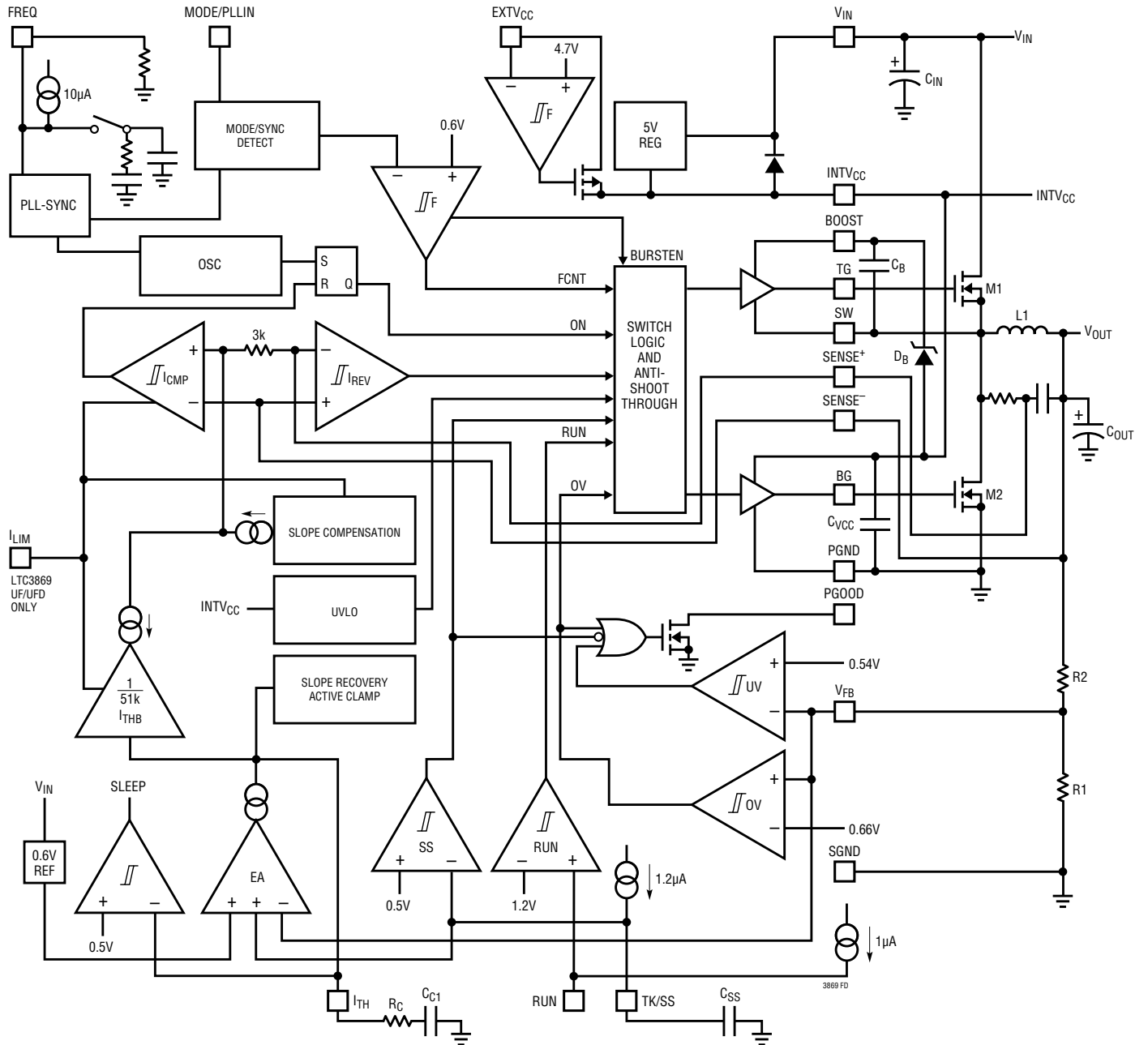
PGND (Pin 16/Pin 17/Pin 19): Power Ground Pin. Connect this pin closely to the sources of the bottom N-channel MOSFETs, the (-) terminal of CV_{CC} and the (-) terminal of C_{IN} .

BG1, BG2 (Pin 20, Pin 17/Pin 21, Pin 18/Pin 23, Pin 20): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-channel MOSFETs between PGND and $INTV_{CC}$.

INTV_{CC} (Pin 18/Pin 19/Pin 21): Internal 5V Regulator Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7 μ F low ESR tantalum or ceramic capacitor. It is not recommended to power other applications with this power source.

PGOOD (Pin 12/Pin 13/Pin 15): Power Good Indicator Output. Open drain logic out that is pulled to ground when either channel output exceeds $\pm 10\%$ regulation windows, after the internal 20 μ s power bad mask timer expires.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3869 is a constant-frequency, current mode step-down controller with two channels operating 180 degrees out-of-phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP} , resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of each error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator I_{REV} , or the beginning of the next cycle.

INTV_{CC}/EXTV_{CC} Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the INTV_{CC} pin. When the EXTV_{CC} pin is left open or tied to a voltage less than 4.7V, an internal 5V linear regulator supplies INTV_{CC} power from V_{IN} . If EXTV_{CC} is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on connecting EXTV_{CC}. Using the EXTV_{CC} pin allows the INTV_{CC} power to be derived from a high efficiency external source such as one of the LTC3869 switching regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B , which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT} , the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns

every third cycle to allow C_B to recharge. However, it is recommended that a load be present or the IC operates at low frequency during the drop-out transition to ensure C_B is recharged.

Shutdown and Start-Up (RUN1, RUN2 and TK/SS1, TK/SS2 Pins)

The two channels of the LTC3869 can be independently shut down using the RUN1 and RUN2 pins. Pulling either of these pins below 1.2V shuts down the main control loop for that controller. Pulling both pins low disables both controllers and most internal circuits, including the INTV_{CC} regulator. Releasing either RUN pin allows an internal 1 μ A current to pull up the pin and enable that controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the Absolute Maximum Rating of 6V on this pin.

The start-up of each controller's output voltage V_{OUT} is controlled by the voltage on the TK/SS1 and TK/SS2 pins. When the voltage on the TK/SS pin is less than the 0.6V internal reference, the LTC3869 regulates the V_{FB} voltage to the TK/SS pin voltage instead of the 0.6V reference. This allows the TK/SS pin to be used to program the soft-start period by connecting an external capacitor from the TK/SS pin to SGND. An internal 1.2 μ A pull-up current charges this capacitor, creating a voltage ramp on the TK/SS pin. As the TK/SS voltage rises linearly from 0V to 0.6V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively the TK/SS pin can be used to cause the start-up of V_{OUT} to "track" that of another supply. Typically, this requires connecting to the TK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the corresponding RUN pin is pulled low to disable a controller, or when INTV_{CC} drops below its undervoltage lockout threshold of 3.2V, the TK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, both controllers are disabled and the external MOSFETs are held off.

OPERATION

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping, or Continuous Conduction)

The LTC3869 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to a DC voltage below 0.6V (e.g., SGND). To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to INTV_{CC}. To select Burst Mode operation, float the MODE/PLLIN pin. When a controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier EA will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.5V, the internal sleep signal goes high (enabling sleep mode) and the top MOSFET is turned off immediately, but the bottom MOSFET is turned off when the inductor current reaches zero.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_{REV}) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE/PLLIN pin is connected to INTV_{CC}, the LTC3869 operates in PWM pulse-skipping mode at light loads. At very light loads, the current comparator I_{CMP} may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e.,

skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Single Output Multiphase Operation

The LTC3869 can be used for single output multiphase converters by making these connections

- Tie all of the I_{TH} pins together.
- Tie all of the V_{FB} pins together.
- Tie all of the TK/SS pins together.
- Tie all of the RUN pins together.

LTC3869 has excellent current matching performance between channels to ensure that there are equal thermal stress for both channels.

Frequency Selection and Phase-Locked Loop (FREQ and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3869 controller can be selected using the FREQ pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 250kHz to 780kHz.

There is a precision 10μA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the application section showing the relationship between the voltage on the FREQ pin and switching frequency.

A phase-locked loop (PLL) is integrated on the LTC3869 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The controller is operating in forced continuous mode when it is synchronized.

OPERATION

The PLL loop filter network is integrated inside the LTC3869. The phase-locked loop is capable of locking any frequency within the range of 250kHz to 780kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Power Good (PGOOD Pin)

When V_{FB} pin voltage is not within $\pm 10\%$ of the 0.6V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when the RUN pin is below 1.2V or when the LTC3869 is in the soft-start or tracking phase. The PGOOD pin will flag power good immediately

when both V_{FB} pins are within the $\pm 10\%$ of the reference window. However, there is an internal 20 μ s power bad mask when V_{FB} goes out the $\pm 10\%$ window. The PGOOD pin is allowed to be pulled up by an external resistor to a source of up to 6V.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots ($>10\%$) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3869 application circuit. LTC3869 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption, and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The I_{LIM} pin is a tri-level logic input which sets the maximum current limit of the controller. When I_{LIM} is either grounded, floated or tied to $INTV_{CC}$, the typical value for the maximum current sense threshold will be 30mV, 50mV or 75mV, respectively.

Which setting should be used? For the best current limit accuracy, use the 75mV setting. The 30mV setting will allow for the use of very low DCR inductors or sense resistors, but at the expense of current limit accuracy. The 50mV setting is a good balance between the two. For single output dual phase applications, use the 50mV or 75mV setting for optimal current sharing.

SENSE+ and SENSE- Pins

The SENSE+ and SENSE- pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 0V to 12.5V. Both SENSE pins are high impedance inputs with small base currents of less than 1 μ A. When the SENSE pins ramp up from 0V to 1.4V, the small base currents flow out of the SENSE pins. When the SENSE pins ramp down from 12.5V to 1.1V, the small base currents flow into the SENSE pins. The high impedance inputs to the current comparators allow accurate DCR sensing. However, care must be taken not to float these pins during normal operation. The LTC3869GN-2 defaults to 50mV current limit value.

Filter components mutual to the sense lines should be placed close to the LTC3869, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins.

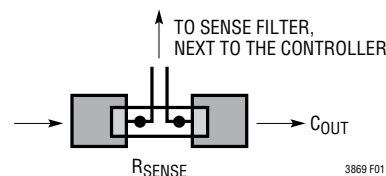


Figure 1. Sense Lines Placement with Sense Resistor

Low Value Resistors Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIM} setting. The input common mode range of the current comparator is 0V to 12.5V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L . To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Because of possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \cdot R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 10mV ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications, for duty cycles less than 40%.

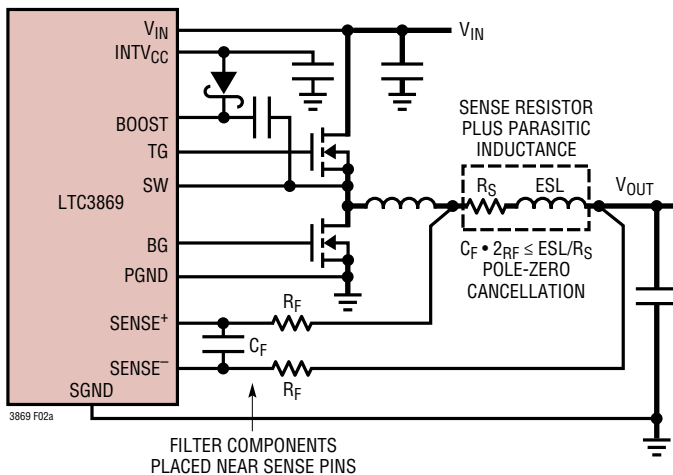
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APPLICATIONS INFORMATION

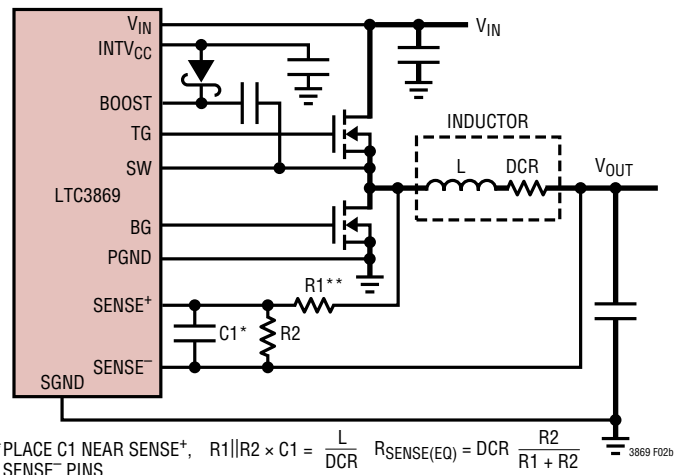
For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628/LTC3728 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. For today's highest current density solutions, however, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 20mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions the voltage drop across the sense resistor's parasitic inductance is no longer negligible. A typical sensing circuit using a discrete resistor is shown in Figure 2a. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 3 illustrates the voltage waveform across a 2mΩ sense resistor with a 2010 footprint for the 1.2V/15A converter operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)} \cdot t_{ON} \cdot t_{OFF}}{\Delta L \cdot (t_{ON} + t_{OFF})}$$



(2a) Using a Resistor to Sense Current



**PLACE R1 NEXT TO INDUCTOR

(2b) Using the Inductor DCR to Sense Current

Figure 2. Two Different Methods of Sensing Current

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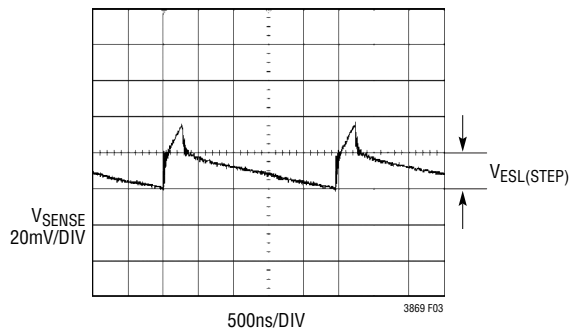


Figure 3. Voltage Waveform Measured Directly Across the Sense Resistor

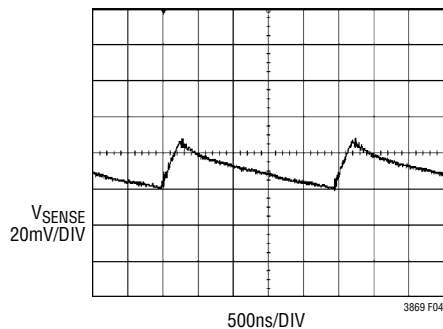


Figure 4. Voltage Waveform Measured After the Sense Resistor Filter. $C_F = 1000\text{pF}$, $R_F = 100\Omega$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resulting waveform looks resistive again, as shown in Figure 4. For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use the equation above to determine the ESL. However, do not over-filter. Keep the RC time constant less than or equal to the inductor time constant to maintain a high enough ripple voltage on V_{SENSE} .

The above generally applies to high density/high current applications where $I_{\text{MAX}} > 10\text{A}$ and low values of inductors are used. For applications where $I_{\text{MAX}} < 10\text{A}$, set R_F to 10Ω and C_F to 1000pF . This will provide a good starting point.

The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin connected to the sense resistor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3869 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than $1\text{m}\Omega$ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

If the external $R1 \parallel R2 \cdot C1$ time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by $R2/(R1 + R2)$. $R2$ scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{\text{SENSE(EQUIV)}} = \frac{V_{\text{SENSE(MAX)}}}{I_{\text{MAX}} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the Maximum Current Sense Threshold ($V_{\text{SENSE(MAX)}}$) in the Electrical Characteristics table (23mV , 43mV , or 68mV , depending on the state of the I_{LIM} pin).

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C . Increase this value to account for the temperature coefficient of resistance, which is approximately $0.4\%/^\circ\text{C}$. A conservative value for $T_{\text{L(MAX)}}$ is 100°C .

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To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{\text{SENSE(EQUIV)}}}{\text{DCR}_{(\text{MAX})} \text{ at } T_{L(\text{MAX})}}$$

C1 is usually selected to be in the range of 0.047μF to 0.47μF. This forces R1 || R2 to around 2kΩ, reducing error that might have been caused by the SENSE pins' ±1μA current. T_{L(MAX)} is the maximum inductor temperature.

The equivalent resistance R1 || R2 is scaled to the room temperature inductance and maximum DCR:

$$R1 || R2 = \frac{L}{(\text{DCR at } 20^\circ\text{C}) \cdot C1}$$

The sense resistor values are:

$$R1 = \frac{R1 || R2}{R_D}; \quad R2 = \frac{R1 \cdot R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{\text{LOSS } R1} = \frac{(V_{\text{IN(MAX)}} - V_{\text{OUT}}) \cdot V_{\text{OUT}}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

To maintain a good signal to noise ratio for the current sense signal, use a minimum ΔV_{SENSE} of 10mV for duty cycles less than 40%. For a DCR sensing application, the actual ripple voltage will be determined by the equation:

$$\Delta V_{\text{SENSE}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{R1 \cdot C1} \cdot \frac{V_{\text{OUT}}}{V_{\text{IN}} \cdot f_{\text{OSC}}}$$

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles > 40%. However, the LTC3869 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency f_{OSC} directly determine the inductor's peak-to-peak ripple current:

$$I_{\text{RIPPLE}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \left(\frac{V_{\text{IN}} - V_{\text{OUT}}}{f_{\text{OSC}} \cdot L} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of I_{OUT(MAX)} for a duty cycle less than 40%. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{\text{IN}} - V_{\text{OUT}}}{f_{\text{OSC}} \cdot I_{\text{RIPPLE}}} \cdot \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

For duty cycles greater than 40%, the 10mV current sense ripple voltage requirement is relaxed because the slope compensation signal aids the signal-to-noise ratio and because a lower limit is placed on the inductor value to avoid subharmonic oscillations. To ensure stability for

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duty cycles up to the maximum of 95%, use the following equation to find the minimum inductance.

$$L_{\text{MIN}} > \frac{V_{\text{OUT}}}{f_{\text{SW}} \cdot I_{\text{LOAD(MAX)}}} \cdot 1.4$$

where

L_{MIN} is in units of μH

f_{SW} is in units of MHz

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3869: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the INTV_{CC} voltage. This voltage is typically 5V during start-up (see EXTV_{CC} Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected ($V_{\text{IN}} < 5\text{V}$); then, sub-logic level threshold MOSFETs ($V_{\text{GS(TH)}} < 3\text{V}$) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{\text{DS(ON)}}$, Miller capacitance C_{MILLER} , input voltage and maximum output current. Miller capacitance, C_{MILLER} , can be approximated from the gate charge curve usually provided on the MOSFET manufacturers’ data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS} . This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS} . When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{V_{\text{IN}}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{\text{MAIN}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} (I_{\text{MAX}})^2 (1 + \delta) R_{\text{DS(ON)}} + (V_{\text{IN}})^2 \left(\frac{I_{\text{MAX}}}{2} \right) (R_{\text{DR}}) (C_{\text{MILLER}}) \cdot \left[\frac{1}{V_{\text{INTVCC}} - V_{\text{TH(MIN)}}} + \frac{1}{V_{\text{TH(MIN)}}} \right]^2 \cdot f_{\text{OSC}}$$

$$P_{\text{SYNC}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{V_{\text{IN}}} (I_{\text{MAX}})^2 (1 + \delta) R_{\text{DS(ON)}}$$

where δ is the temperature dependency of $R_{\text{DS(ON)}}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET’s Miller threshold voltage. $V_{\text{TH(MIN)}}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{\text{IN}} < 20\text{V}$ the high current efficiency generally improves with larger MOSFETs, while for $V_{\text{IN}} > 20\text{V}$ the transition losses rapidly increase to the point that the use of a higher $R_{\text{DS(ON)}}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input

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voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/^\circ\text{C}$ can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes conduct during the dead time between the conduction of the two power MOSFETs. These prevent the body diodes of the bottom MOSFETs from turning on, storing charge during the dead time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN} . A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance. A Schottky diode in parallel with the bottom FET may also provide a modest improvement in Burst Mode efficiency.

Soft-Start and Tracking

The LTC3869 has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When one particular channel is configured to soft-start by itself, a capacitor should be connected to its TK/SS pin. This channel is in the shutdown state if its RUN pin voltage is below 1.2V. Its TK/SS pin is actively pulled to ground in this shutdown state.

Once the RUN pin voltage is above 1.2V, the channel powers up. A soft-start current of 1.2 μA then starts to charge its soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage

according to the ramp rate on the TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.6V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{\text{SOFTSTART}} = 0.6 \cdot \frac{C_{\text{SS}}}{1.2\mu\text{A}}$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse-skipping mode up to TK/SS = 0.5V. Between TK/SS = 0.5V and 0.54V, it will operate in forced continuous mode and revert to the selected mode once TK/SS > 0.54V. The output ripple is minimized during the 40mV forced continuous mode window ensuring a clean PGOOD signal.

When the channel is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider value to be small enough to make this error negligible.

In order to track down another channel or supply after the soft-start phase expires, the LTC3869 is forced into continuous mode of operation as soon as V_{FB} is below the undervoltage threshold of 0.54V regardless of the setting on the MODE/PLLIN pin. However, the LTC3869 should always be set in force continuous mode tracking down when there is no load. After TK/SS drops below 0.1V, its channel will operate in discontinuous mode.

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Output Voltage Tracking

The LTC3869 allows the user to program how its output ramps up and down by means of the TK/SS pins. Through these pins, the output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 5. In the following discussions, V_{OUT1} refers to the LTC3869's output 1 as a master channel and V_{OUT2} refers to the LTC3869's output 2 as a slave channel. In practice, though, either phase can be used as the master. To implement the coincident tracking in Figure 5a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TK/SS pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 6a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2} .

To implement the ratiometric tracking in Figure 6b, the ratio of the V_{OUT2} divider should be exactly the same as the master channel's feedback divider shown in Figure 6b. By selecting different resistors, the LTC3869 can achieve different modes of tracking including the two in Figure 5.

So which mode should be programmed? While either mode in Figure 5 satisfies most practical applications, some trade-offs exist. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation.

When the master channel's output experiences dynamic excursion (under load transient, for example), the slave channel output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.

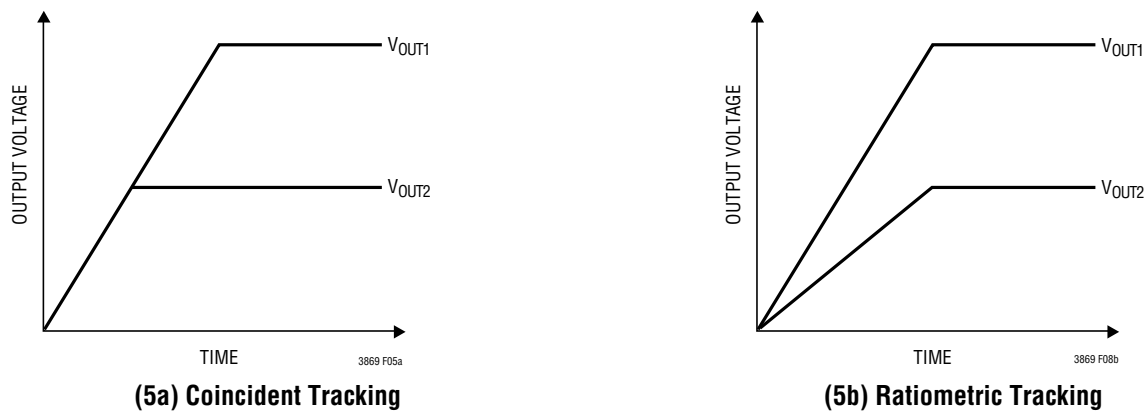


Figure 5. Two Different Modes of Output Voltage Tracking

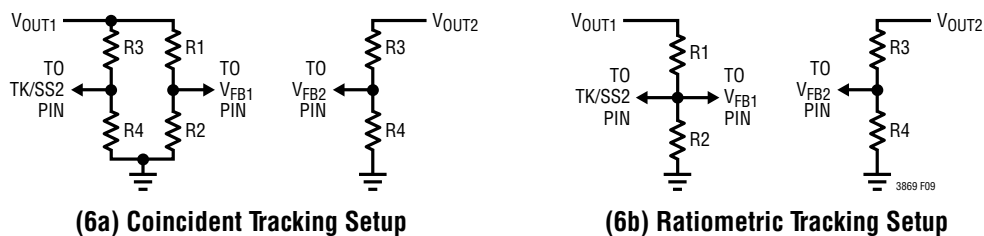


Figure 6. Setup for Coincident and Ratiometric Tracking

APPLICATIONS INFORMATION

INTV_{CC} Regulators and EXTV_{CC}

The LTC3869 features a true PMOS LDO that supplies power to INTV_{CC} from the V_{IN} supply. INTV_{CC} powers the gate drivers and much of the LTC3869's internal circuitry. The linear regulator regulates the voltage at the INTV_{CC} pin to 5V when V_{IN} is greater than 5.5V. EXTV_{CC} connects to INTV_{CC} through a P-channel MOSFET and can supply the needed power when its voltage is higher than 4.7V. Each of these can supply a peak current of 100mA and must be bypassed to ground with a minimum of 4.7μF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1μF ceramic capacitor placed directly adjacent to the INTV_{CC} and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3869 to be exceeded. The INTV_{CC} current, which is dominated by the gate charge current, may be supplied by either the 5V linear regulator or EXTV_{CC}. When the voltage on the EXTV_{CC} pin is less than 4.7V, the linear regulator is enabled. Power dissipation for the IC in this case is highest and is equal to V_{IN} • I_{INTVCC}. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3869 INTV_{CC} current is limited to less than 42mA from a 38V supply in the UFD package and not using the EXTV_{CC} supply:

$$T_J = 70^\circ\text{C} + (42\text{mA})(38\text{V})(34^\circ\text{C}/\text{W}) = 125^\circ\text{C}$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE/PLLIN = SGND) at maximum V_{IN}. When the voltage applied to EXTV_{CC} rises above 4.7V, the INTV_{CC} linear regulator is turned off and the EXTV_{CC} is connected to the INTV_{CC}. The EXTV_{CC}

remains on as long as the voltage applied to EXTV_{CC} remains above 4.5V. Using the EXTV_{CC} allows the MOSFET driver and control power to be derived from one of the LTC3869's switching regulator outputs during normal operation and from the INTV_{CC} when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the EXTV_{CC} than is specified, an external Schottky diode can be added between the EXTV_{CC} and INTV_{CC} pins. Do not apply more than 6V to the EXTV_{CC} pin and make sure that EXTV_{CC} < V_{IN} at all times.

Significant efficiency and thermal gains can be realized by powering INTV_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

Tying the EXTV_{CC} pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70^\circ\text{C} + (42\text{mA})(5\text{V})(34^\circ\text{C}/\text{W}) = 77^\circ\text{C}$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive INTV_{CC} power from the output.

The following list summarizes the four possible connections for EXTV_{CC}:

1. EXTV_{CC} left open (or grounded). This will cause INTV_{CC} to be powered from the internal 5V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. EXTV_{CC} connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. EXTV_{CC} connected to an external supply. If a 5V external supply is available, it may be used to power EXTV_{CC} providing it is compatible with the MOSFET gate drive requirements.
4. EXTV_{CC} connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting EXTV_{CC} to an output-derived voltage that has been boosted to greater than 4.7V.

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For applications where the main input power is below 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 7 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET which is typically 4.5V for logic level devices.

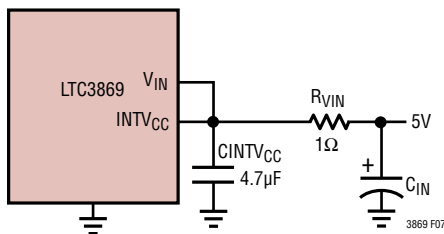


Figure 7. Setup for a 5V Input

Topside MOSFET Driver Supply (C_B , DB)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged through external diode DB from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTV_{CC}}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. Make sure the diode is a low leakage diode even at hot temperature to prevent leakage current feeding $INTV_{CC}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Undervoltage Lockout

The LTC3869 has two functions that help protect the controller in case of undervoltage conditions. A precision

UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.2V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 600mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pins have a precision turn-on reference of 1.2V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4.5μA of current flows out of the RUN pin once the RUN pin voltage passes 1.2V. One can program the hysteresis of the run comparator by adjusting the values of the resistive divider. For accurate V_{IN} undervoltage detection, V_{IN} needs to be higher than 4.5V.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX}}{V_{IN}} [(V_{OUT})(V_{IN} - V_{OUT})]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life.

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This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3869, ceramic capacitors can also be used for C_{IN} . Always consult the manufacturer if there is any question.

The benefit of the LTC3869 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The sources of the top MOSFETs should be placed within 1cm of each other and share a common $C_{IN}(s)$. Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN} .

A small (0.1 μ F to 1 μ F) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3869, is also suggested. A 2.2 Ω to 10 Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE} \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

Setting Output Voltage

The LTC3869 output voltages are each set by an external feedback resistive divider carefully placed across the output, as shown in Figure 8. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R_B}{R_A} \right)$$

To improve the frequency response, a feed-forward capacitor, C_{FF} , may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

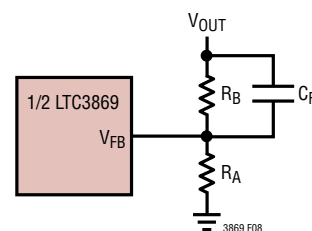


Figure 8. Setting Output Voltage

Fault Conditions: Current Limit and Current Foldback

The LTC3869 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 50% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum programmed value to one-third of the maximum value. Foldback current limiting is disabled during the soft-start or tracking up. Under short-circuit conditions with very low duty cycles, the LTC3869 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3869 (≈ 90 ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \cdot \frac{V_{IN}}{L}$$

The resulting short-circuit current is:

$$I_{SC} = \frac{1/3 V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \Delta I_{L(SC)}$$

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Phase-Locked Loop and Frequency Synchronization

The LTC3869 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (V_{CO}) and a phase detector. This allows the turn-on of the top MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. The turn-on of controller 2's top MOSFET is thus 180 degrees out-of-phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision $10\mu\text{A}$ of current flowing out of FREQ pin. This allows the user to use a single resistor to SGND to set the switching frequency when no external clock is applied to the MODE/PLLIN pin. The internal switch between FREQ pin and the integrated PLL filter network is ON, allowing the filter network to be pre-charged to the same voltage potential as the FREQ pin. The relationship between the voltage on the FREQ pin and the operating frequency is shown in Figure 9 and specified in the Electrical Characteristics table. If an external clock is detected on the MODE/PLLIN pin, the internal switch mentioned above will turn off and isolate the influence of FREQ pin. Note that the LTC3869 can only be synchronized to an external clock whose frequency is within range of the LTC3869's internal V_{CO} . This is guaranteed to be between 250kHz and 780kHz. A simplified block diagram is shown in Figure 10.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC} , then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC} , current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor holds the voltage.

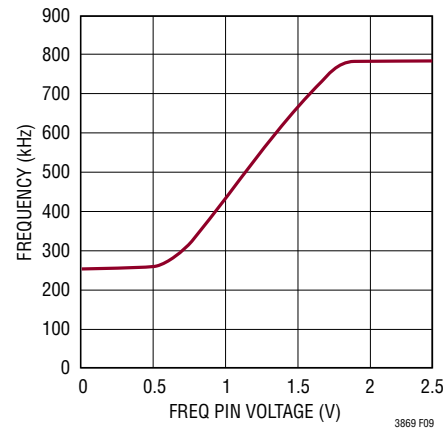


Figure 9. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

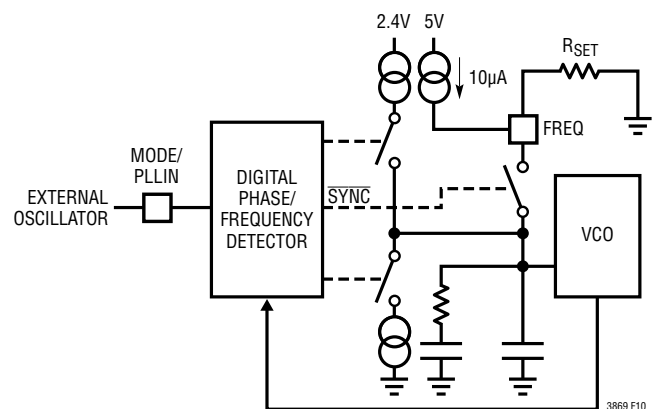


Figure 10. Phase-Locked Loop Block Diagram

Typically, the external clock (on MODE/PLLIN pin) input high threshold is 1.6V, while the input low threshold is 1V. It is not recommended to apply the external clock when IC is in shutdown.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3869 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$