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Dual Output PolyPhase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management

FEATURES

- **PMBus/I²C Compliant Serial Interface**
  - **Monitor Voltage, Current, Temperature and Faults**
  - **Program Voltage, Soft-Start/Stop, Sequencing, Margining, AVP and UV/OV/OC Limits**
- **3V ≤ VINSNS ≤ 38V, 0.5V ≤ V_{OUT} ≤ 5.25V**
- **±0.5% Output Voltage Error**
- **Programmable PWM Frequency or External Clock Synchronization from 250kHz to 1.25MHz**
- **Accurate PolyPhase® Current Sharing**
- **Internal EEPROM with Fault Logging and ECC**
- IC Supply Range: 3V to 13.2V
- Resistor or Inductor DCR Current Sensing
- Power Good Output Voltage Monitor
- Optional Resistor Programming for Key Parameters
- 40-Pin (6mm × 6mm) QFN Package

APPLICATIONS

- High Current Distributed Power Systems
- Servers, Network and Storage Equipment
- Intelligent Energy Efficient Power Regulation

DESCRIPTION

The LTC®3882-1 is a dual, PolyPhase DC/DC synchronous step-down switching regulator controller with PMBus compliant serial interface. It uses a constant frequency, leading-edge modulation, voltage mode architecture for excellent transient response and output regulation. Each PWM channel can produce output voltages from 0.5V to 5.25V using a wide range of 3.3V compatible power stages, including power blocks, DrMOS or discrete FET drivers. Up to four LTC3882-1 devices can operate in parallel for 2-, 3-, 4-, 6- or 8-phase operation.

System configuration and monitoring is supported by the LTpowerPlay™ software tool. The LTC3882-1 serial interface can read back input voltage, output voltage and current, temperature and fault status. Most operating parameters can be set via the digital interface or stored in internal EEPROM for use at power up. Switching frequency and phase, output voltage and device address can also be set using external configuration resistors.

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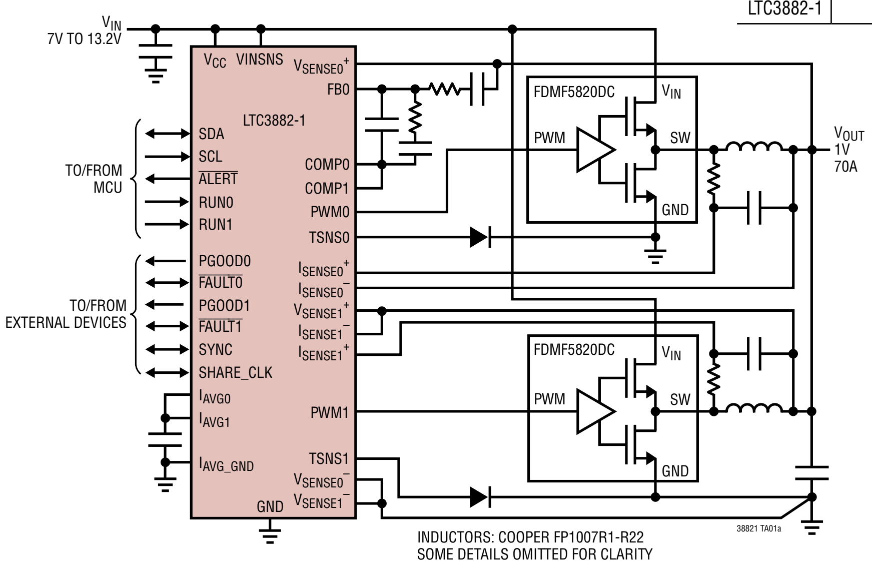
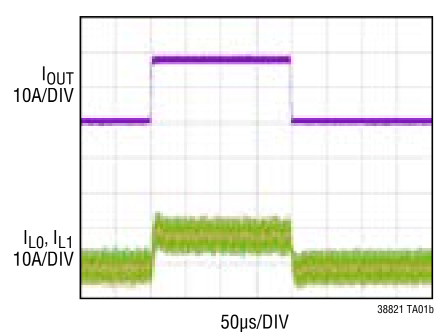
TYPICAL APPLICATION

	PWM ENABLE OUTPUT	TG/BG CONTROL	HW WRITE PROTECT	DEDICATED PGOOD OUTPUT	DIFFERENTIAL V_{OUT} SENSE
LTC3882	•	•	•		V_{OUT0} Only
LTC3882-1				•	V_{OUT0} & V_{OUT1}



Load Step Transient Current Sharing (Using FDMF5820DC DrMOS)



Rev A

TABLE OF CONTENTS

Features 1
Applications 1
Typical Application 1
Description 1
Absolute Maximum Ratings 4
Order Information 4
Pin Configuration 4
Electrical Characteristics 5
Typical Performance Characteristics 9
Pin Functions 13
Block Diagram 15
Test Circuit 16
Timing Diagram 16
Operation 16
Overview 16
Main Control Loop 17
Power-Up and Initialization 19
Soft-Start 20
Time-Based Output Sequencing 20
Output Ramping Control 20
Voltage-Based Output Sequencing 20
Minimum Output Disable Times 21
Output Short Cycle 21
Light Load Current Operation 21
Switching Frequency and Phase 21
PolyPhase Load Sharing 22
Active Voltage Positioning 22
Input Supply Monitoring 22
Output Voltage Sensing and Monitoring 22
Output Current Sensing and Monitoring 22
External and Internal Temperature Sense 23
Resistor Configuration Pins 23
Internal EEPROM with CRC and ECC 24
Fault Detection 24
Input Supply Faults 24
Hardwired PWM Response to V_{OUT} Faults 24
Power Good Indication (Master) 25
Power Good Indication (Slave) 25
Hardwired PWM Response to I_{OUT} Faults 25
Hardwired PWM Response to Temperature Faults 25
Hardwired PWM Response to Timing Faults 26
External Faults 26
Fault Handling 26
Status Registers and $\overline{\text{ALERT}}$ Masking 26
$\overline{\text{FAULT}}$ Pin I/O 28
Fault Logging 28
Factory Default Operation 31
Serial Interface 32
Serial Bus Addressing 32
Serial Bus Timeout 36
Serial Communication Errors 36
PMBus Command Summary 37
PMBus Commands 37
Data Formats 37
Applications Information 42
Efficiency Considerations 42
PWM Frequency and Inductor Selection 42
Power MOSFET Selection 43
MOSFET Driver Selection 44
Using PWM Protocols 44
C_{IN} Selection 44
C_{OUT} Selection 45
Feedback Loop Compensation 46
PCB Layout Considerations 47
Output Current Sensing 48
Output Voltage Sensing 50
Soft-Start and Stop 51
Time-Based Output Sequencing and Ramping 51
Voltage-Based Output Sequencing 52
Using Output Voltage Servo 54
Using AVP 54
PWM Frequency Synchronization 55
PolyPhase Operation and Load Sharing 56
External Temperature Sense 60
Resistor Configuration Pins 60
Internal Regulator Outputs 62
IC Junction Temperature 62
Derating EEPROM Retention at Temperature 63
Configuring Open-Drain Pins 63
PMBus Communication and Command Processing 64
Status and Fault Log Management 65
LTpowerPlay – An Interactive Digital Power GUI 65
Interfacing to the DC1613 66
Design Example 66
PMBus COMMAND DETAILS 69
Addressing and Write Protect 69
PAGE 69
PAGE_PLUS_WRITE 69
PAGE_PLUS_READ 70
WRITE_PROTECT 70
MFR_ADDRESS 71
MFR_RAIL_ADDRESS 71
General Device Configuration 71
PMBUS_REVISION 71
CAPABILITY 71
On, Off and Margin Control 72
ON_OFF_CONFIG 72
MFR_CONFIG_ALL_LTC3882-1 72
OPERATION 73
MFR_RESET 73
PWM Configuration 74
FREQUENCY_SWITCH 74

Rev A

TABLE OF CONTENTS

MFR_PWM_CONFIG_LTC3882-1 75
MFR_CHAN_CONFIG_LTC3882-1 76
MFR_PWM_MODE_LTC3882-1 77
Input Voltage and Limits 78
VIN_ON 78
VIN_OFF 78
VIN_OV_FAULT_LIMIT 78
VIN_UV_WARN_LIMIT 78
Output Voltage and Limits 79
VOUT_MODE 79
VOUT_COMMAND 79
MFR_VOUT_MAX 79
VOUT_MAX 80
MFR_VOUT_AVP 80
VOUT_MARGIN_HIGH 80
VOUT_MARGIN_LOW 80
VOUT_OV_FAULT_LIMIT 80
VOUT_OV_WARN_LIMIT 81
VOUT_UV_WARN_LIMIT 81
VOUT_UV_FAULT_LIMIT 81
Output Current and Limits 82
IOUT_CAL_GAIN 82
MFR_IOUT_CAL_GAIN_TC 82
IOUT_OC_FAULT_LIMIT 82
IOUT_OC_WARN_LIMIT 82
Output Timing, Delays, and Ramping 83
MFR_RESTART_DELAY 83
TON_DELAY 83
TON_RISE 83
TON_MAX_FAULT_LIMIT 84
VOUT_TRANSITION_RATE 84
TOFF_DELAY 84
TOFF_FALL 84
TOFF_MAX_WARN_LIMIT 84
External Temperature and Limits 85
MFR_TEMP_1_GAIN 85
MFR_TEMP_1_OFFSET 85
OT_FAULT_LIMIT 85
OT_WARN_LIMIT 85
Status Reporting 86
STATUS_BYTE 86
UT_FAULT_LIMIT 86
STATUS_WORD 87
STATUS_VOUT 87
STATUS_IOUT 87
STATUS_INPUT 88
STATUS_TEMPERATURE 88
STATUS_CML 88
STATUS_MFR_SPECIFIC 89
MFR_PADS_LTC3882-1 89
MFR_COMMON 90
MFR_INFO 90
CLEAR_FAULTS 90
Telemetry 91
READ_VIN 91
MFR_VIN_PEAK 91
READ_VOUT 91
MFR_VOUT_PEAK 91
READ_IOUT 92
MFR_IOUT_PEAK 92
READ_POUT 92
READ_TEMPERATURE_1 92
MFR_TEMPERATURE_1_PEAK 92
READ_TEMPERATURE_2 92
MFR_TEMPERATURE_2_PEAK 93
READ_DUTY_CYCLE 93
READ_FREQUENCY 93
MFR_CLEAR_PEAKS 93
Fault Response and Communication 94
VIN_OV_FAULT_RESPONSE 94
VOUT_OV_FAULT_RESPONSE 95
VOUT_UV_FAULT_RESPONSE 95
IOUT_OC_FAULT_RESPONSE 96
OT_FAULT_RESPONSE 97
UT_FAULT_RESPONSE 97
MFR_OT_FAULT_RESPONSE 97
TON_MAX_FAULT_RESPONSE 98
MFR_RETRY_DELAY 98
SMBALERT_MASK 98
MFR_FAULT_PROPAGATE_LTC3882-1 99
MFR_FAULT_RESPONSE 100
MFR_FAULT_LOG 101
Fault Log Operation 101
MFR_FAULT_LOG_CLEAR 101
EEPROM User Access 102
STORE_USER_ALL 102
RESTORE_USER_ALL 102
MFR_COMPARE_USER_ALL 102
MFR_FAULT_LOG_STORE 103
MFR_EE_xxxx 103
USER_DATA_0x 103
Unit Identification 103
MFR_ID 103
MFR_MODEL 103
MFR_SERIAL 103
MFR_SPECIAL_ID 103
Typical Applications 104
Package Description 106
Revision History 107
Typical Application 108
Related Parts 108

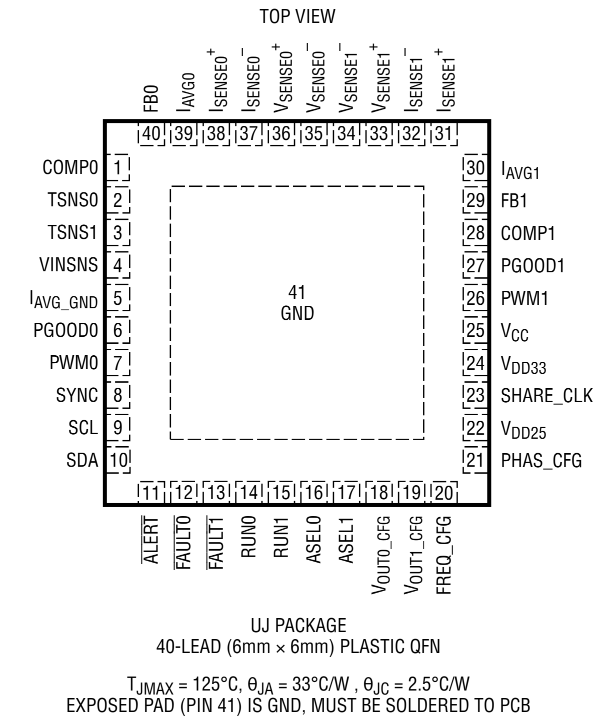
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Supply Voltage .... –0.3V to 15V
VINSNS Voltage .... –0.3V to 40V
V_{SENSEn}^- .... –0.3V to 1V
V_{SENSEn}^+, I_{SENSEn}^+, I_{SENSEn}^- .... –0.3V to 6V
FB*n*, COMP*n*, TSNS*n*, I_{AVG_GND}, I_{AVGn} ...... –0.3V to 3.6V
SYNC, $\overline{FAULTn}$, PGOOD*n*, SHARE_CLK........–0.3V to 3.6V
SCL, SDA, RUN*n*, $\overline{ALERT}$ .... –0.3V to 5.5V
ASEL*n*, VOUT*n*_CFG, FREQ_CFG,
PHAS_CFG... –0.3V to 2.75V
PWM*n*, V_{DD25} .... (Note 13)
V_{DD33} .... (Note 14)
Operating Junction Temperature
(Notes 2, 3) .... –40°C to 125°C*
Storage Temperature Range .... –65°C to 150°C*

*See Derating EEPROM Retention at Temperature in the Applications Information section for junction temperatures in excess of 125°C.

PIN CONFIGURATION



ORDER INFORMATION http://www.linear.com/product/LTC3882-1#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3882EUJ-1#PBF	LTC3882EUJ-1#TRPBF	LTC3882UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3882IUJ-1#PBF	LTC3882IUJ-1#TRPBF	LTC3882UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{CC} = 5V, V_{SENSE0}^+ = V_{SENSE1}^+ = 1.8V, V_{SENSE0}^- = V_{SENSE1}^- = I_{AVG_GND} = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IC Supply							
V_{CC}	V_{CC} Voltage Range	V_{DD33} = Internal LDO		4.5		13.8	V
V_{DD33_EXT}	V_{DD33} Voltage Range	V_{CC} = V_{DD33} (Note 6)	●	3		3.6	V
V_{UVLO}	Undervoltage Lockout Threshold	V_{DD33} Rising Hysteresis	●		 42	3	V mV
I_Q	IC Operating Current				32		mA
t_{INIT}	Controller Initialization Time	Delay from RESTORE_USER_ALL, MFR_RESET or V_{DD33} > V_{UVLO} Until TON_DELAY Can Begin			35		ms
V_{DD33} Linear Regulator							
V_{DD33}	V_{DD33} Regulator Output Voltage	V_{CC} ≥ 4.5V		3.2	3.3	3.4	V
I_{DD33}	V_{DD33} Current Limit	V_{DD33} = 2.8V V_{DD33} = 0V			85 40		mA mA
V_{DD25} Linear Regulator							
V_{DD25}	V_{DD25} Regulator Output Voltage			2.25	2.5	2.75	V
I_{DD25}	V_{DD25} Current Limit				95		mA
PWM Control Loops							
VINSNS	V_{IN} Sense Voltage Range			3		38	V
R_{VINSNS}	VINSNS Input Resistance				278		kΩ
V_{OUT_R0}	Range 0 Maximum V_{OUT} Range 0 Set Point Error (Note 7) Range 0 Set Point Resolution	 0.6V ≤ V_{OUT} ≤ 5V 0.6V ≤ V_{OUT} ≤ 5V	 ●	 –0.5	5.25 ±0.2 1.375	 0.5	V % % mV
V_{OUT_R1}	Range 1 Maximum V_{OUT} Range 1 Set Point Error (Note 7) Range 1 Set Point Resolution	 0.6V ≤ V_{OUT} ≤ 2.5V 0.6V ≤ V_{OUT} ≤ 2.5V	 ●	 –0.5	2.65 ±0.2 0.6875	 0.5	V % % mV
I_{VSENSE}	V_{SENSE} Input Current	V_{SENSE}^+ = 5.5V V_{SENSE}^- = 0V			235 –335		µA µA
$V_{LINEREG}$	V_{CC} Line Regulation, No Output Servo	4.5V ≤ V_{CC} ≤ 13.2V (See Test Circuit)		–0.02		0.02	%/V
AVP	AVP ΔV_{OUT}	AVP = 10%, VOUT_COMMAND = 1.8V, I_{SENSE} Differential Step 3mV to 12mV with IOUT_OC_WARN_LIMIT = 15mV	●	–118	–108	–96	mV
$A_{V(OL)}$	Error Amplifier Open-Loop Voltage Gain				87		dB
SR	Error Amplifier Slew Rate				9.5		V/µs
f_{0dB}	Error Amplifier Bandwidth	(Note 12)			30		MHz
I_{COMP}	Error Amplifier Output Current	Sourcing Sinking			–2.6 34		mA mA
R_{VSFB}	Resistance Between V_{SENSE}^+ and FB	Range 0 Range 1	● ●	52 37	67 49	83 61	kΩ kΩ
V_{ISENSE}	I_{SENSE} Differential Input Range				±70		mV
I_{ISENSE}	$I_{SENSE}^{\pm}$ Input Current	0V ≤ V_{PIN} ≤ 5.5V		–1	±0.1	1	µA
I_{AVG_VOS}	I_{AVG} Current Sense Offset	Referred to I_{SENSE} Inputs	 ●	 –600	±175	 650	µV µV
V_{SIOS}	Slave Current Sharing Offset	Referred to I_{SENSE} Inputs	 ●	 –800	±300	 700	µV µV
f_{SYNC}	SYNC Frequency Error	250kHz ≤ f_{SYNC} ≤ 1.25MHz	●	–10		10	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{CC} = 5V, V_{SENSE0}^+ = V_{SENSE1}^+ = 1.8V, V_{SENSE0}^- = V_{SENSE1}^- = I_{AVG_GND} = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Supervisor							
V_{ON_TOL}	Input ON/OFF Threshold Error	15V ≤ V_{IN_ON} ≤ 35V	●	–2		2	%
N_{VON}	Input ON/OFF Threshold Resolution				143		mV
Output Voltage Supervisors							
V_{UVOV_R0}	Range 0 Maximum Threshold Range 0 Error Range 0 Threshold Resolution Range 0 Threshold Hysteresis	 2V ≤ V_{OUT} ≤ 5V (Falling for UV and Rising for OV)	 ●	 –1	5.5 11	 1 54	V % mV mV
V_{UVOV_R1}	Range 1 Maximum Threshold Range 1 Error Range 1 Threshold Resolution Range 1 Threshold Hysteresis	 1V ≤ V_{OUT} ≤ 2.5V (Falling for UV and Rising for OV)	 ●	 –1	2.75 5.5	 1 27	V % mV mV
Output Current Supervisors							
V_{ILIM_TOL}	Output Current Limit Tolerance $I_{SENSE}^+ – I_{SENSE}^-$	15mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 30mV 30mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 50mV 50mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 70mV	● ● ●	–1.7 –2.5 –5.2		1.7 2.5 5.2	mV mV mV
N_{ILIM}	$I_{SENSE}^+ – I_{SENSE}^-$ Threshold Resolution	1LSB			0.4		mV
ADC Readback Telemetry (Note 8)							
N_{VIN}	VINSNS Readback Resolution	(Note 9)			10		Bits
V_{IN_TUE}	VINSNS Total Unadjusted Readback Error	4.5V ≤ VINSNS ≤ 38V	 ●			0.5 2	% %
N_{DC}	PWM Duty Cycle Resolution	(Note 9)			10		Bits
DC_{TUE}	PWM Duty Cycle Total Unadjusted Readback Error	PWM Duty Cycle = 12.5%		–2		2	%
N_{VOUT}	V_{OUT} Readback Resolution				244		µV
V_{OUT_TUE}	V_{OUT} Total Unadjusted Readback Error	0.6V ≤ V_{OUT} ≤ 5.5V, Constant Load	 ●	 –0.5	±0.2	 0.5	% %
N_{ISENSE}	I_{OUT} Readback Resolution LSB Step Size (at $I_{SENSE}^{\pm}$)	(Note 9) 0mV ≤ $\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ < 16mV 16mV ≤ $\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ < 32mV 32mV ≤ $\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ < 63.9mV 63.9mV ≤ $\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ ≤ 70mV			10 15.625 31.25 62.5 125		Bits µV µV µV µV
I_{SENSE_TUE}	I_{OUT} Total Unadjusted Readback Error	$\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ ≥ 6mV, 0V ≤ V_{OUT} ≤ 5.5V	●	–1		1	%
I_{SENSE_OS}	I_{OUT} Zero-Code Offset Voltage				±32		µV
N_{TEMP}	Temperature Resolution				0.25		°C
T_{EXT_TUE}	External Temperature Total Unadjusted Readback Error	TSNS0, TSNS1 ≤ 1.85V (Note 10) MFR_PWM_MODE_LTC3882-1[6] = 0 MFR_PWM_MODE_LTC3882-1[6] = 1	 ● ●	 –3 –7		 3 7	 °C °C
T_{INT_TUE}	Internal Temperature Total Unadjusted Readback Error	Internal Diode (Note 10)			±1		°C
$t_{CONVERT}$	Update Rate	(Note 11)			90		ms
Internal EEPROM (Notes 4, 6)							
Endurance	Number of Write Operations	0°C ≤ T_J ≤ 85°C During All Write Operations		10,000			Cycles
Retention	Stored Data Retention	T_J ≤ 125°C		10			Years
Mass Write Time	STORE_USER_ALL Execution Duration	0°C ≤ T_J ≤ 85°C During All Write Operations			0.2	2	s

Rev A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{CC} = 5V, V_{SENSE0}^+ = V_{SENSE1}^+ = 1.8V, V_{SENSE0}^- = V_{SENSE1}^- = I_{AVG_GND} = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs (SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*, SYNC, SHARE_CLOCK)							
V_{IH}	Input High Voltage	SCL, SDA, RUN0, RUN1, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$ SYNC, SHARE_CLK	● ●	1.35 1.8			V V
V_{IL}	Input Low Voltage	SCL, SDA, RUN0, RUN1, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$ SYNC, SHARE_CLK	● ●			0.8 0.6	V V
V_{HYST}	Input Hysteresis	SCL, SDA			80		mV
C_{IN}	Input Capacitance	SCL, SDA, RUN0, RUN1, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, SYNC, SHARE_CLK (Note 12)				10	pF
t_{FILT}	Input Digital Filter Delay	$\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$ RUN0, RUN1			3 10		µs µs
Digital Outputs (SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*, SYNC, SHARE_CLOCK, $\overline{\text{ALERT}}$, PWM*n*, PGOOD*n*)							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA; SDA, SCL, RUN0, RUN1, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, SYNC, SHARE_CLK, $\overline{\text{ALERT}}$, I_{SINK} = 2mA; PWM*n*, PGOOD*n*	● ●		0.2	0.4 0.3	V V
V_{OH}	PWM*n* Output High Voltage	I_{SOURCE} = 2mA	●	2.7			V
I_{LKG}	Output Leakage Current	0V ≤ PWM0, PWM1, PGOOD0, PGOOD1 ≤ V_{DD33} 0V ≤ $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, SYNC, SHARE_CLK ≤ 3.6V 0V ≤ RUN0, RUN1 ≤ 5.5V 0V ≤ SCL, SDA, $\overline{\text{ALERT}}$ ≤ 5.5V	 ●	–1 –5 –5		1 5 5	µA µA µA
t_{RO}	PWM*n* Output Rise Time	C_{LOAD} = 30pF, 10% to 90%			5		ns
t_{FO}	PWM*n* Output Fall Time	C_{LOAD} = 30pF, 90% to 10%			4		ns
Serial Bus Timing							
f_{SMB}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition. After This Period, the First Clock Is Generated		●	0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		●	0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD,DAT}$	Data Hold Time: Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 ns µs
$t_{SU,DAT}$	Input Data Setup Time		●	100			ns
$t_{TIMEOUT}$	Clock Low Timeout		●	25		35	ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3882-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3882-1E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3882-1I is guaranteed over the full –40°C to 125°C operating junction temperature range. Junction temperature T_J is calculated in °C from the ambient temperature T_A and power dissipation P_D according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} is the package thermal impedance. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. Refer to the Applications Information section.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: EEPROM endurance, retention and mass write times are guaranteed by design, characterization and correlation with statistical process controls. Minimum retention applies only for devices cycled less than the minimum endurance specification. EEPROM read commands (e.g. RESTORE_USER_ALL) are valid over the entire specified operating junction temperature range.

Note 5: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 6: Minimum EEPROM endurance, retention and mass write time specifications apply when writing data with $3.15V \le V_{DD33} \le 3.45V$. EEPROM read commands are valid over the entire specified V_{DD33} operating range.

Note 7: Specified V_{OUT} error with AVP = 0% requires servo mode to be set with MFR_PWM_MODE_LTC3882-1 command bit 6. Performance is guaranteed by testing the LTC3882-1 in a feedback loop that servos V_{OUT} to a specified value.

Note 8: ADC tested with PWMs disabled. Comparable capability demonstrated by in-circuit evaluations. Total Unadjusted Error includes all gain and linearity errors, as well as offsets.

Note 9: Internal 32-bit calculations using 16-bit ADC results are limited to 10-bit resolution by PMBus Linear 11-bit data format.

Note 10: Limits guaranteed by TSNS voltage and current measurements during test, including ADC readback.

Note 11: Data conversion is done in round robin fashion. All inputs signals are continuously scanned in sequence resulting in a typical conversion latency of 90ms.

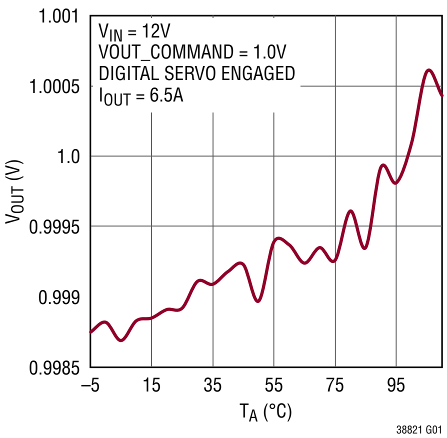
Note 12: Guaranteed by design.

Note 13: Do not apply a voltage or current source directly to these pins. They should only be connected to passive RC loads, otherwise permanent damage may occur.

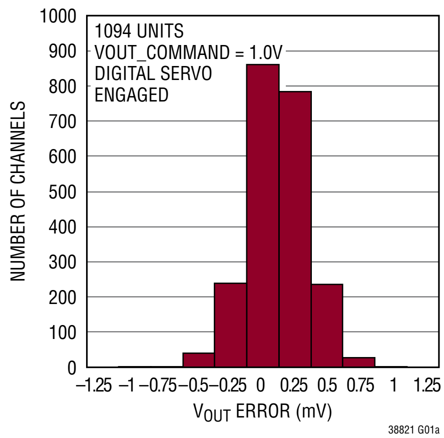
Note 14: Do not apply a voltage source to this pin unless shorted to V_{CC}. See Electrical Characteristics for applicable limits beyond which permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

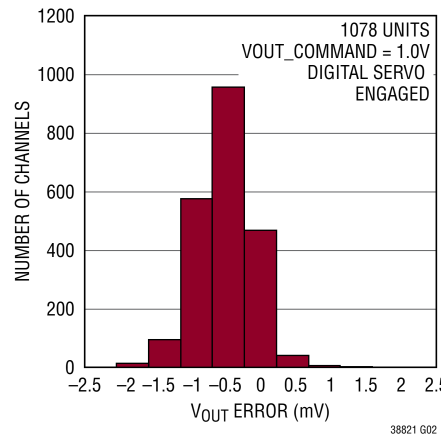
LTC3882-1 1.0V Regulated Output vs Temperature



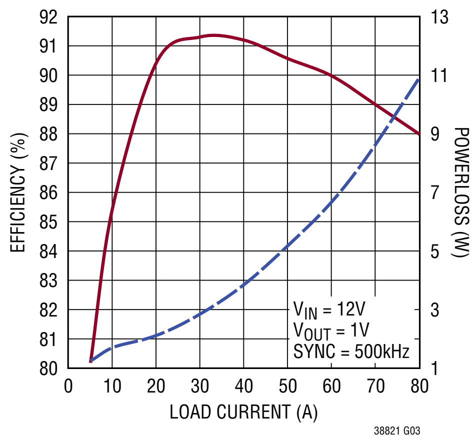
Typical LTC3882-1 Output Voltage Distribution at 0°C



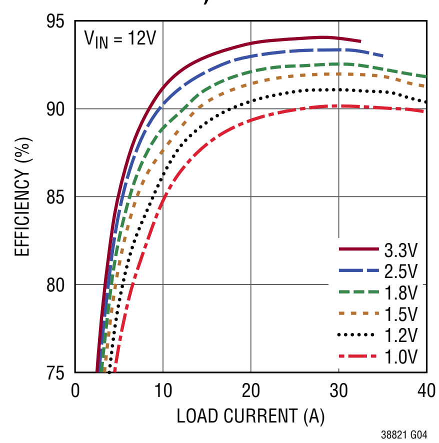
Typical LTC3882-1 Output Voltage Distribution at 105°C



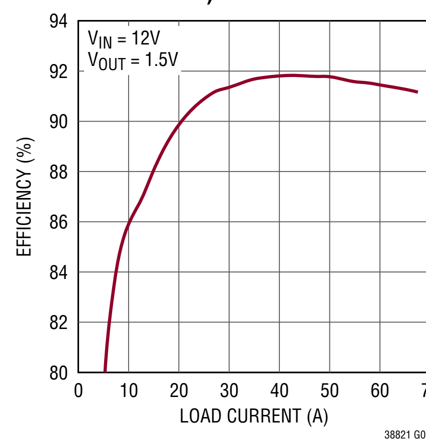
Efficiency and Loss vs Load (2-Phase Using FDMF5820DC DRMOS)



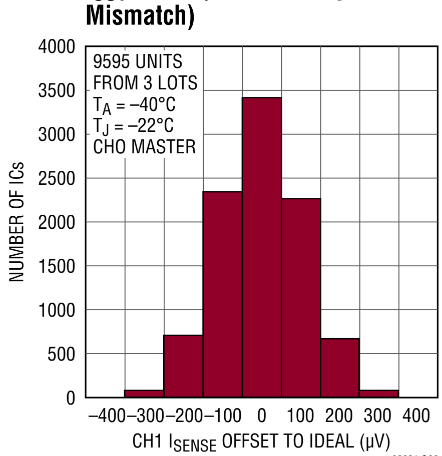
Efficiency vs Load Current (1-Phase Using D12S1R880A Power Block)



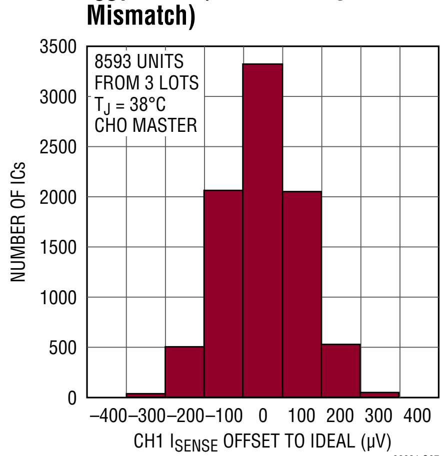
Efficiency vs Load Current (3-Phase Using D12S1R845A Power Block)



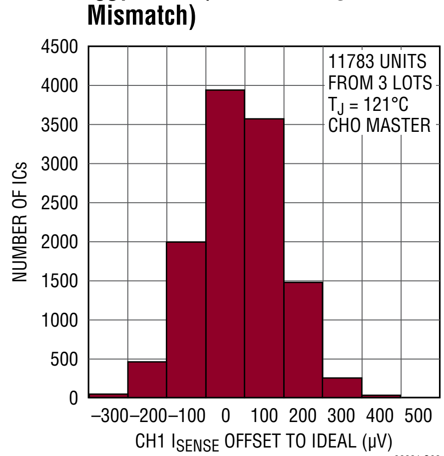
Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)



Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)

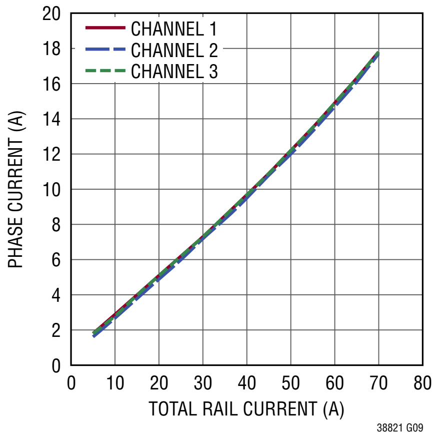


Typical Distribution of Slave I_{OUT} Offset (Not Including DCR Mismatch)

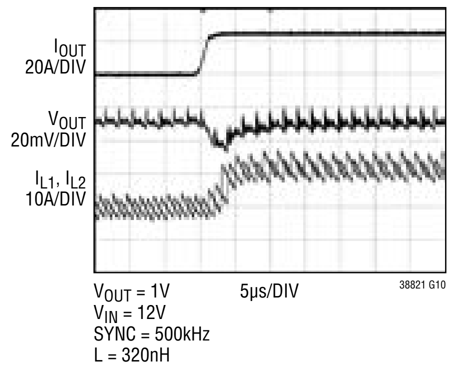


TYPICAL PERFORMANCE CHARACTERISTICS

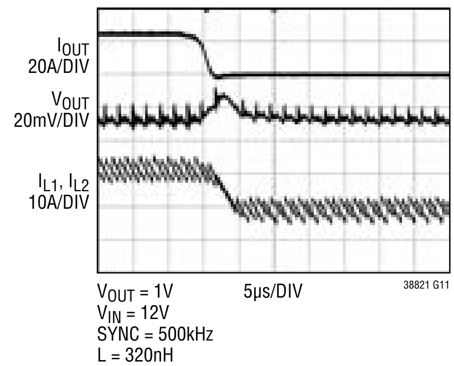
3-Phase DC Output Current Sharing (Using D12S1R845A Power Block



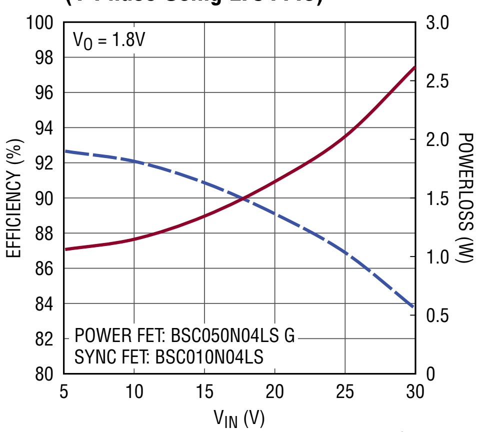
Load Step Transient Current Sharing (Using FDMF6707B DrMOS)



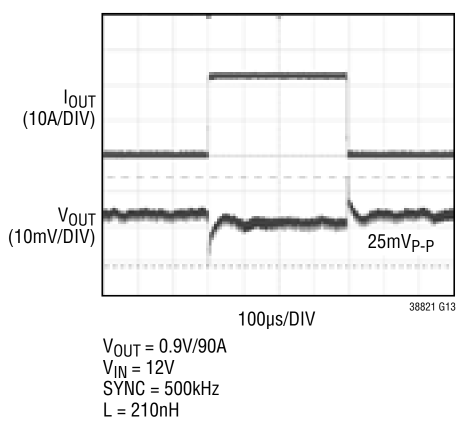
Load Dump Transient Current Sharing (Using FDMF6707B DrMOS)



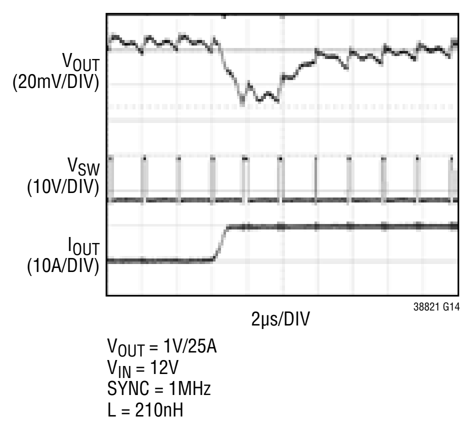
Efficiency and Power Loss vs Input Voltage (1-Phase Using LTC4449)



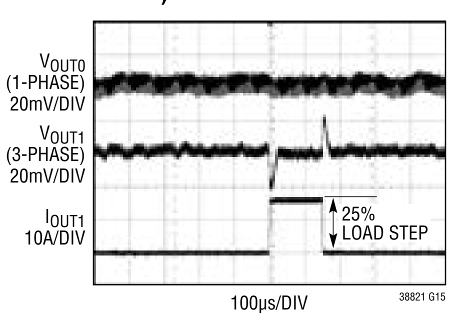
3-Phase Transient Response (Using D12S1R860A Power Block)



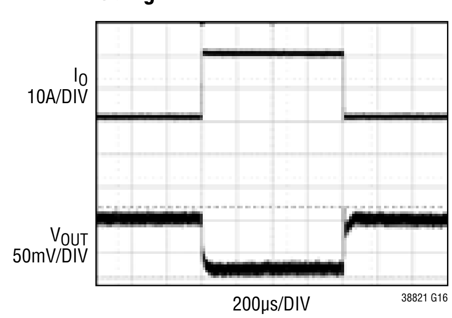
1-Phase Single Cycle Response (Using D12S1R860A Power Block with C_{OUT} = 6 × 100µF X5R 1210)



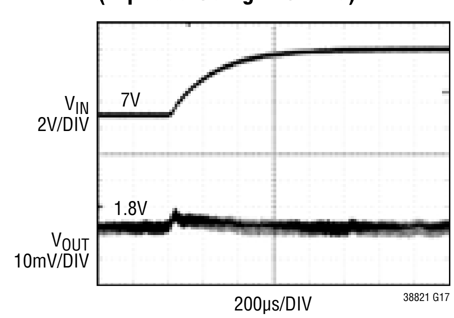
3+1 Channel Crosstalk (Using D12S1R845A Power Blocks)



Load Step Transient Response Using AVP

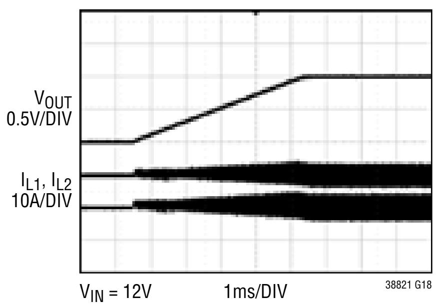


Line Step Transient Response (1-phase Using LTC4449)

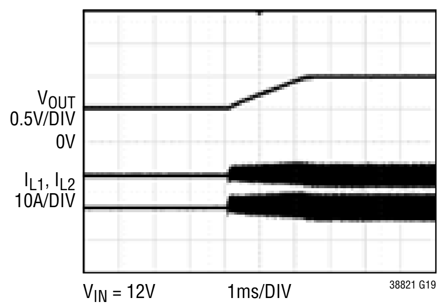


TYPICAL PERFORMANCE CHARACTERISTICS

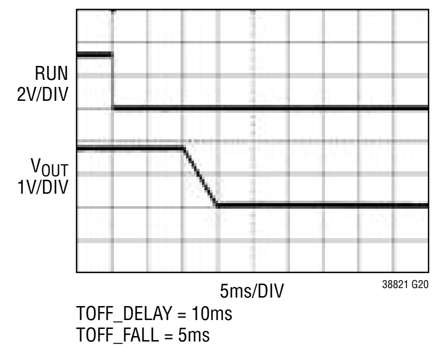
Soft-Start Ramp



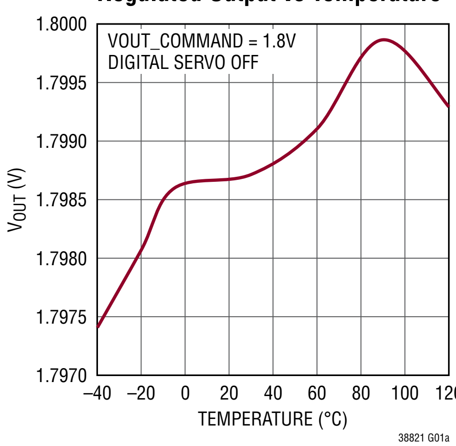
Start-Up Into a Prebiased Load



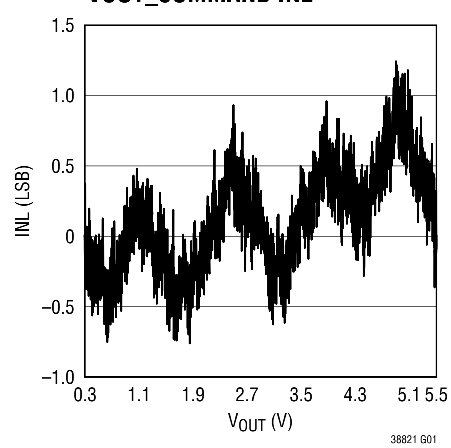
Soft-Off Ramp



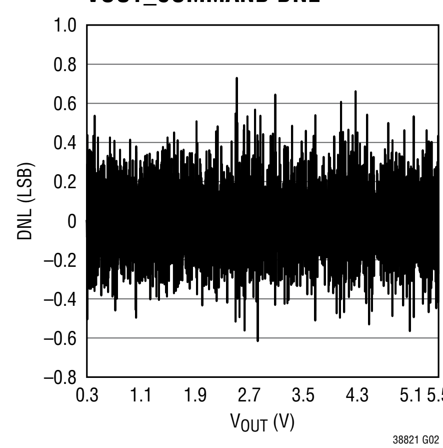
Regulated Output vs Temperature



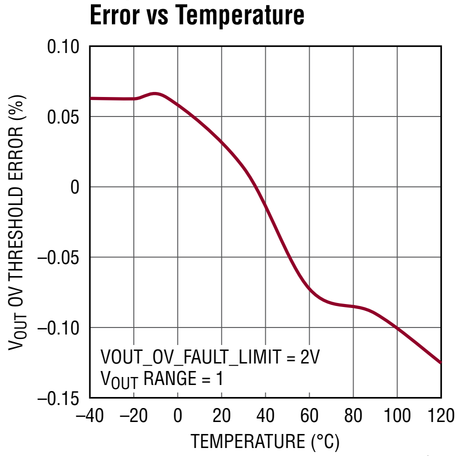
VOUT_COMMAND INL



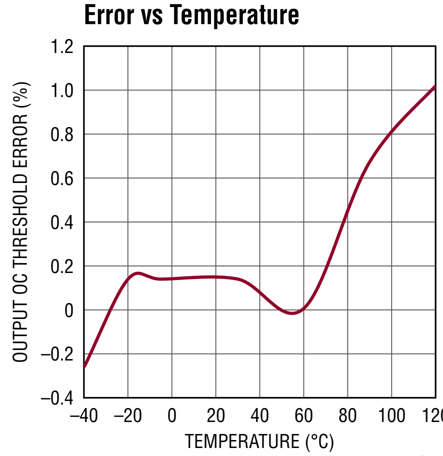
VOUT_COMMAND DNL



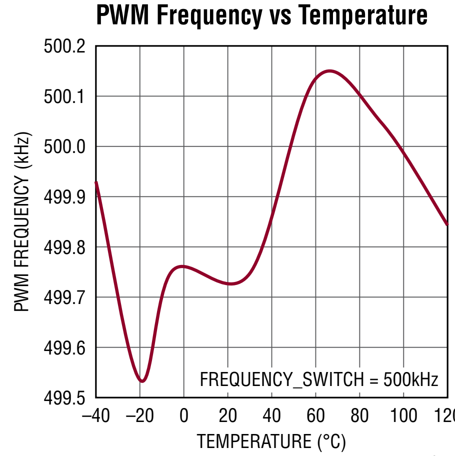
Output Overvoltage Threshold Error vs Temperature



Output Overcurrent Threshold Error vs Temperature

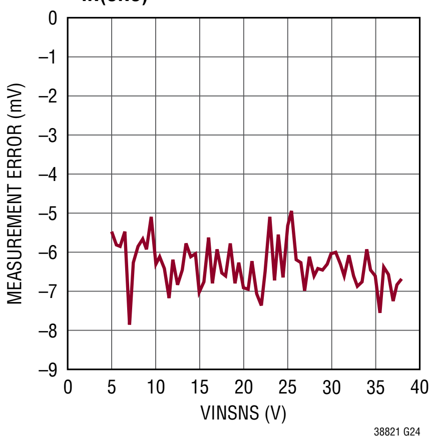


PWM Frequency vs Temperature

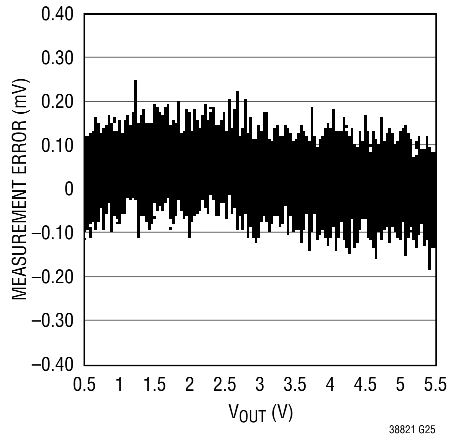


TYPICAL PERFORMANCE CHARACTERISTICS

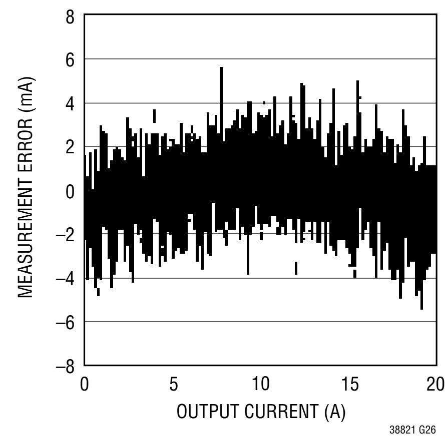
$V_{IN(SNS)}$ ADC TUE



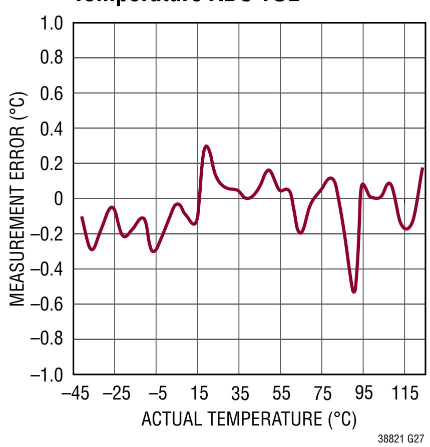
V_{OUT} ADC TUE



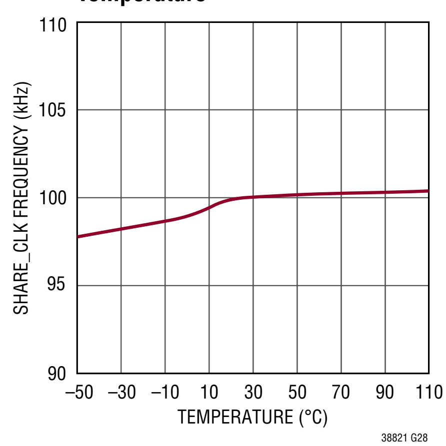
I_{OUT} ADC TUE



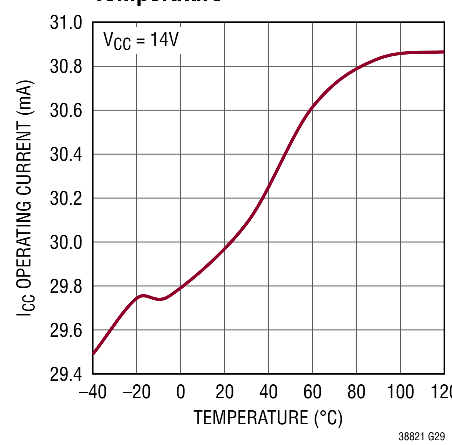
Temperature ADC TUE



SHARE_CLK Frequency vs Temperature



IC Operating Current vs Temperature



Rev A

PIN FUNCTIONS

COMP0/COMP1 (Pin 1/Pin 28): Error Amplifier Outputs. PWM duty cycle increases with this control voltage. These are true low impedance outputs and cannot be directly connected together when active. For PolyPhase operation, wiring FB to V_{DD33} will three-state the error amplifier output of that channel, making it a slave. PolyPhase control is then implemented in part by connecting all slave COMP pins together to one master error amplifier output.

TSNS0/TSNS1 (Pin 2/Pin 3): External Temperature Sense Inputs. The LTC3882-1 supports two methods of calculation of external temperature based on forward-biased P/N junctions between these pins and GND.

VINSNS (Pin 4): V_{IN} Supply Sense. Connect to the V_{IN} power supply to provide line feedforward compensation. A change in V_{IN} immediately modulates the input to the PWM comparator and inversely changes the pulse width to provide excellent transient line regulation and fixed modulator voltage gain. An external lowpass filter can be added to this pin to prevent noisy signals from affecting the loop gain.

I_{AVG_GND} (Pin 5): I_{AVG} Ground Reference. The same I_{AVG_GND} should be shared between all channels of a PolyPhase rail and connected to system ground at a single point. I_{AVG_GND} may be wired directly to GND on ICs that do not share phases with other chips.

PGOOD/PGOOD1 (Pin 6/Pin 27): Power Good Indicator Open-Drain Outputs. These outputs are driven low through a 30µs filter when the respective channel output is below its programmed UV fault limit or above its programmed OV fault limit. If used, a pull-up resistor is required in the application. Operating voltage range is GND to V_{DD33}.

PWM0/PWM1 (Pin 7/Pin 26): PWM Three-State Control Outputs. These pins provide single-wire PWM switching control for each channel to an external gate driver, DrMOS or power block. Operating voltage range is GND to V_{DD33}.

SYNC (Pin 8): External Clock Synchronization Input and Open-Drain Output. If desired, an external clock can be applied to this pin to synchronize the internal PWM channels. If the LTC3882-1 is configured as a clock master, this pin will also pull to ground at the selected PWM switching frequency with a 125ns pulse width. A pull-up resistor to 3.3V is required in the application if SYNC is driven by any LTC3882-1. Minimize the capacitance on this line to ensure its time constant is fast enough for the application.

SCL (Pin 9): Serial Bus Clock Input. A pull-up resistor to 3.3V is required in the application.

SDA (Pin 10): Serial Bus Data Input and Output. A pull-up resistor to 3.3V is required in the application.

$\overline{ALERT}$ (Pin 11): Open-Drain Status Output. This pin may be connected to the system $\overline{SMBALERT}$ wire-AND interrupt signal and should be left open if not used. If used, a pull-up resistor is required in the application. Operating voltage range is GND to V_{DD33}.

$\overline{FAULT0}$/$\overline{FAULT1}$ (Pin 12/Pin 13): Programmable Digital Inputs and Open-Drain Outputs for Fault Sharing. Used for channel-to-channel fault communication and propagation. These pins should be left open if not used. If used, a pull-up resistor to 3.3V is required in the application.

RUN0/RUN1 (Pin 14/Pin 15): Run Control Inputs and Open-Drain Outputs. A voltage above 2V is required on these pins to enable the respective PWM channel. The LTC3882-1 will drive these pins low under certain reset/restart conditions regardless of any PMBus command settings. A pull-up resistor to 3.3V is required in the application.

ASEL0/ASEL1 (Pin 16/Pin 17): Serial Bus Address Select Pins. Connect optional 1% resistor dividers between V_{DD25} and GND to these pins to select the serial bus interface address. Refer to the Applications Information section for more detail.

V_{OUT0_CFG}/V_{OUT1_CFG} (Pin 18/Pin 19): Output Voltage Configuration Pins. Connect optional 1% resistor dividers between V_{DD25} and GND to these pins to select the output voltage for each channel. Refer to the Applications Information section for more detail.

FREQ_CFG (Pin 20): Frequency Configuration Pin. Connect an optional 1% resistor divider between V_{DD25} and GND to this pin to configure PWM switching frequency. Refer to the Applications Information section for more detail.

PIN FUNCTIONS

PHAS_CFG (Pin 21): Phase Configuration Pin. Connect an optional 1% resistor divider between V_{DD25} and GND to this pin to configure the phase of each PWM channel relative to SYNC. Refer to the Applications Information section for more detail.

V_{DD25} (Pin 22): Internal 2.5V Regulator Output. Bypass this pin to GND with a low ESR 1µF capacitor. Do not load this pin with external current beyond that required for local LTC3882-1 configuration pins, if any.

SHARE_CLK (Pin 23): Share Clock Open-Drain Output (bussed). Share Clock, nominally 100kHz, is used to sequence multiple rails in a power system utilizing more than one LTC PSM controller. A pull-up resistor is required in the application. Minimize the capacitance on this line to ensure the time constant is fast enough for the application. Operating voltage range is GND to V_{DD33}.

V_{DD33} (Pin 24): Internal 3.3V Regulator Output. Bypass this pin to GND with a low ESR 2.2µF capacitor. The LTC3882-1 may also be powered from an external 3.3V rail attached to this pin, if also shorted to V_{CC}. Do not overload this pin with external system current. Local pull-up resistors for the LTC3882-1 itself may be powered from V_{DD33}. Refer to the Applications Information section for more detail.

V_{CC} (Pin 25): 3.3V Regulator Input. Bypass this pin to GND with a capacitor (0.1µF to 1µF ceramic) in close proximity to the IC.

V_{SENSE0}^-/V_{SENSE1}^- (Pin 35/Pin 34): Negative Output Voltage Sense Inputs. These pins must still be properly connected on slave channels for accurate output current telemetry.

V_{SENSE0}^+/V_{SENSE1}^+ (Pin 36/Pin 33): Positive Output Voltage Sense Inputs. These pins must still be properly connected on slave channels for accurate output current telemetry.

I_{SENSE0}^-/I_{SENSE1}^- (Pin 37/Pin 32): Current Sense Amplifier Inputs. The (–) inputs to the amplifiers are normally connected to the low side of a DCR sensing network or output current sense resistor for each phase.

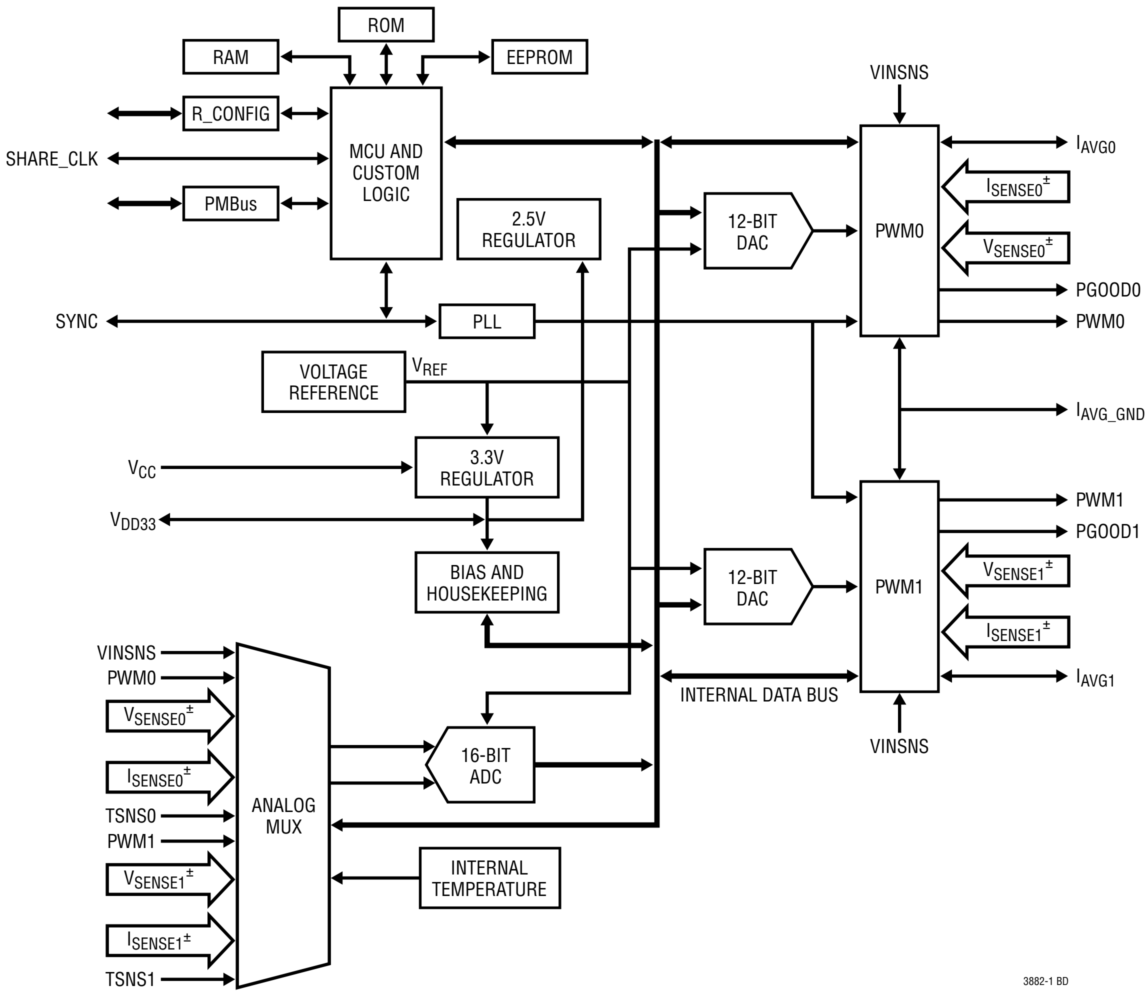
I_{SENSE0}^+/I_{SENSE1}^+ (Pin 38/Pin 31): Current Sense Amplifier Inputs. The (+) inputs are normally connected to the high side of an output current sense resistor or the R-C midpoint of a parallel DCR sense circuit.

I_{AVG0}/I_{AVG1} (Pin 39/Pin 30): Average Current Control Pins. A capacitor connected between these pins and I_{AVG_GND} stores a voltage proportional to the average output current of the master channel. PolyPhase control is then implemented in part by connecting all slave I_{AVG} pins together to the master I_{AVG} output. This pin should be left open on channels that control single-phase outputs. Operating voltage range is GND to 2.1V.

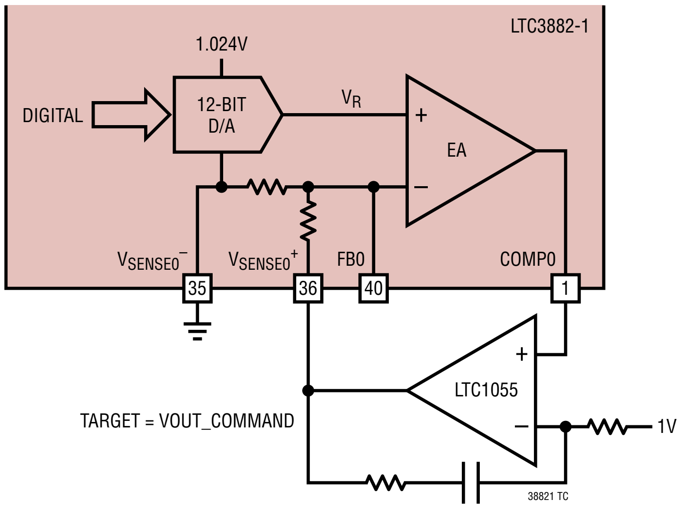
FB0/FB1 (Pin 40/Pin 29): Error Amplifier Inverting Inputs. These pins provide an internally scaled version of the output voltage for use in loop compensation. Refer to the Applications Information section for additional details on compensating the output voltage control loop with external components.

GND (Exposed Pad Pin 41): Ground. All small-signal and compensation components should connect to this pad. *The exposed pad must be soldered to a suitable PCB copper ground plane for proper electrical operation and to obtain the specified package thermal resistance.*

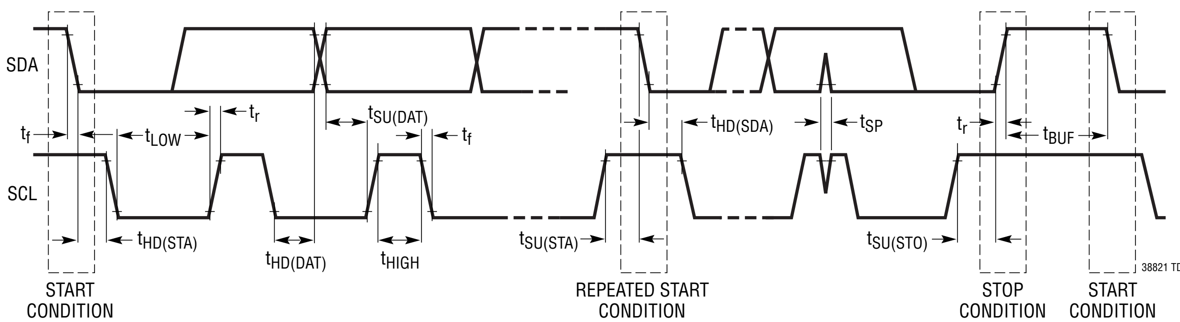
BLOCK DIAGRAM



TEST CIRCUIT (Channel 0 Example)



TIMING DIAGRAM



OPERATION

Overview

The LTC3882-1 is a dual channel/dual phase, constant frequency analog voltage mode controller for DC/DC step-down applications. It features a PMBus compliant digital interface for monitoring and control of important power system parameters. The chip operates from an IC power supply between 3V and 13.2V and is intended for conversion from V_{IN} between 3V and 38V to output voltages between 0.5V and 5.25V. It is designed to be used in a switching architecture with external FET drivers, including higher level integrations such as non-isolated power blocks.

Major features include:

- Digitally Programmable Output Voltage
- Digitally Programmable Output Current Limit
- Digitally Programmable Input Voltage Supervisor
- Digitally Programmable Output Voltage Supervisors
- Digitally Programmable Switching Frequency
- Digitally Programmable On and Off Delay Times
- Digitally Programmable Soft-Start/Stop

OPERATION

- Operating Condition Telemetry
- Phase Locked Loop for Synchronous PolyPhase Operation (2, 3, 4, 6, or 8 phases)
- Fully Differential Load Sense
- Non-Volatile Configuration Memory with ECC
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time-Base Interconnect for Synchronization Between Multiple Controllers
- Fault Event Data Logging
- Capable of Standalone Operation with Default Factory Configuration
- PMBus Revision 1.2 Compliant Interface up to 400kHz

The PMBus interface provides access to important power management data during system operation including:

- Average Input Voltage
- Average Output Voltages
- Average Output Currents
- Average PWM Duty Cycles
- Internal LTC3882-1 Temperature
- External Sensed Temperatures
- Warning and Fault Status, Including Input and Output Undervoltage and Overvoltage

The LTC3882-1 supports four serial bus addressing schemes to access the individual PWM channels separately or jointly.

Fault communication, reporting and system response behavior are fully configurable. Two fault I/Os are provided ($\overline{FAULT0}$, $\overline{FAULT1}$) that can be controlled independently. A separate $\overline{ALERT}$ pin also provides for a maskable SMBALERT#. Fault responses for each channel may be individually programmed, depending on the fault type. PMBus status commands allow fault reporting over the serial bus to identify a specific fault event.

Main Control Loop

The LTC3882-1 utilizes constant frequency voltage mode control with leading-edge modulation. This provides improved response to a load step increase, especially at larger V_{IN}/V_{OUT} ratios found in the low voltage, high current solutions demanded by modern digital subsystems. The LTC3882-1 leading-edge modulation architecture does not have a minimum on-time requirement. Minimum duty cycle will be determined by performance limits of the external power stage. The IC is also capable of active voltage positioning (AVP) to afford the smallest output capacitors possible for a given output voltage accuracy over the anticipated full load range. The LTC3882-1 error amplifiers have high bandwidth, low offset and low output impedance, allowing the control loop compensation network to be optimized for very high crossover frequencies and excellent transient response. The controller also achieves outstanding line transient response by using input feedforward compensation to instantaneously adjust PWM duty cycle and significantly reduce output under/overshoot during supply voltage changes. This also has the added advantage of making the DC loop gain independent of input voltage.

The main PWM control loop used for each channel is illustrated in Figure 1. During normal operation the top MOSFET (power switch) driving choke L1 is commanded off when the clock for that channel resets the RS latch. The power switch is commanded back on when the main PWM comparator VC, sets the RS latch. The error amplifier EA output (COMP) controls the PWM duty cycle to match the FB voltage to the EA positive terminal voltage in steady state. A patented circuit adjusts this output for VINSNS line feedforward.

The positive terminal of the EA is connected to the output of a 12-bit DAC with values ranging from 0V to 1.024V. The DAC value is determined by the resistor configuration pins detailed in application Table 8, by values retrieved from internal EEPROM, or by a combination of PMBus commands to synthesize the desired output voltage. Refer to the following PMBus Command Details section of this document for more information. The LTC3882-1 supports two output ranges. EA can regulate the output voltage to 5.5x the DAC output (Range 0) or 2.75x the DAC output (Range 1).

OPERATION

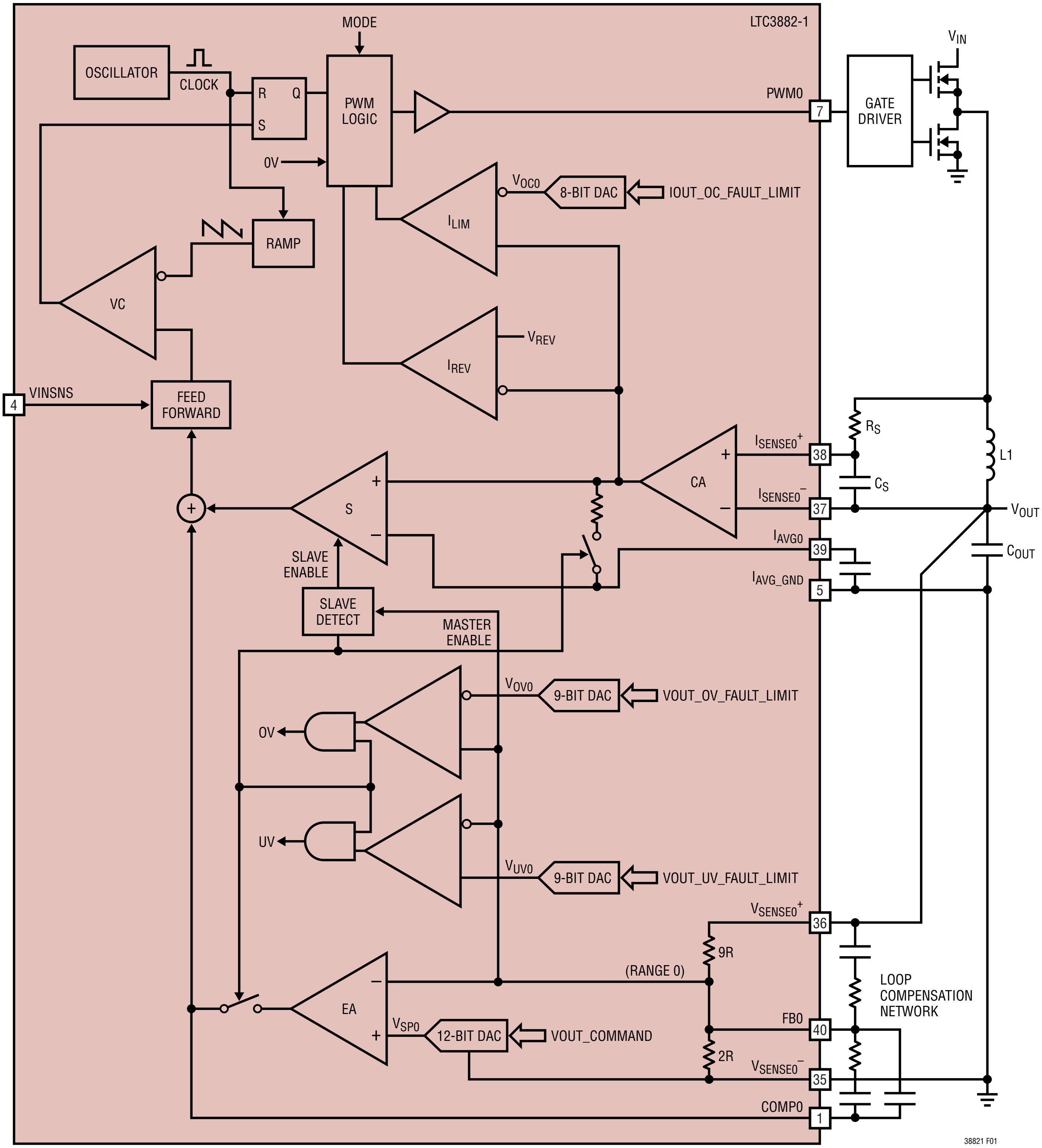


Figure 1. LTC3882-1 PWM Control Loop Diagram

Rev A

OPERATION

VC discriminates its positive input against an internally generated PWM voltage ramp. The positive input is a composite control based on COMP voltage with line feedforward compensation, and current sharing if the channel controls a slave phase. When the ramp falls below this voltage the comparator trips and sets the PWM latch.

If load current increases, V_{SENSE}^+ and FB will droop slightly with respect to the 12-bit DAC output. This causes the COMP voltage to increase until the average inductor current matches the new load current and the desired output voltage is restored. Programmable comparators I_{LIM} and I_{REV} monitor peak instantaneous forward and reverse inductor current for pulse-by-pulse protection. The top power MOSFET is immediately commanded off if the programmed positive limit is reached, and the bottom MOSFET is immediately commanded off if the negative limit is reached. Repeated peak overcurrent events cause an overcurrent fault to be set.

When the top MOSFET is commanded off, the bottom MOSFET is normally commanded on. In continuous conduction mode (CCM) the bottom MOSFET stays on until comparator VC turns the top MOSFET back on. Otherwise in discontinuous conduction mode (DCM, also known as diode emulation) the bottom MOSFET is commanded off if the I_{REV} comparator detects that the inductor current has decayed to approximately 0A. In any case the next PWM cycle starts when the clock for that channel again clears the RS latch.

Power-Up and Initialization

The LTC3882-1 is designed to provide stand-alone supply sequencing with controlled turn-on and turn-off functions. It operates from a single IC input supply of 3V to 13.2V while two on-chip linear regulators generate internal 2.5V and 3.3V. If V_{CC} is below 4.5V, the V_{CC} and V_{DD33} pins must be shorted together and limited to a maximum operating voltage of 3.6V. Controller configuration is reset by the internal UVLO threshold, where V_{DD33} must be at or above 3V and the internal 2.5V supply must be within about 20% of its regulated value. At that point the internal microcontroller begins initialization. A PMBus RESTORE_USER_ALL or MFR_RESET command forces this same initialization.

The LTC3882-1 features an internal RAM built-in self-test (BIST) that runs during initialization. Should RAM BIST fail, the following steps are taken.

- Device responds only at device address 0x7C and global addresses 0x5A and 0x5B
- A persistent Memory Fault Detected is indicated by STATUS_CML
- Internal EEPROM is not accessed
- RUN*n* and SHARE_CLK are driven low continuously

Normal operation can be restored if the RAM BIST subsequently passes, for instance as the result of another MFR_RESET command issued to address 0x7C.

During initialization all PWM outputs are disabled. The RUN*n* pins and SHARE_CLK are held low and $\overline{\text{FAULT}n}$ pins are high impedance. External configuration resistors are identified and the contents of the onboard EEPROM are read into the controller command memory space. The LTC3882-1 can determine key operating parameters from external configuration resistors according to application Table 8 through Table 11. See the following Resistor Configuration Pins section for more detail. The resistor configuration pins only determine some of the preset values of the controller. The remaining values, retrieved from internal EEPROM, are programmed at the factory or with PMBus commands.

If the configuration resistor pins are all open, the LTC3882-1 will use only EEPROM contents to determine all operating parameters. If Ignore Resistor Configuration Pins is set (bit 6 of MFR_CONFIG_ALL_LTC3882-1), the LTC3882-1 will use only its EEPROM contents to determine all operating parameters except device address. Unless both ASEL pins are completely open, the LTC3882-1 will always determine some portion of its device address from the resistors on these pins. See Serial Bus Addressing later in this section.

The internal microcontroller typically requires 35ms to complete initialization from VDD33 ≥ 3V. At that point, an internal comparator monitors VINSNS, which must exceed the VIN_ON threshold before output power sequencing can begin (SHARE_CLK released, ready for TON_DELAY). Accurate readback telemetry can then require an additional 90ms for initial round-robin A/D conversions.

OPERATION

Soft-Start

The RUN pins are released for external control after the part initializes and VINSNS is greater than the VIN_ON threshold. If multiple LTC3882-1 ICs are used in an application, shared RUN pins are held low until all units initialize and VINSNS exceeds the VIN_ON threshold for all devices. A common SHARE_CLK signal can also ensure all connected devices use the same time reference for initial start-up even if RUN pins cannot be shared due to other design requirements. SHARE_CLK is not released by each IC until the conditions for power sequencing have been fully satisfied.

After a channel RUN pin rises above 2V and any specified turn on delay (TON_DELAY) has expired, the LTC3882-1 performs an initial monotonic soft-start ramp on that channel. This is carried out with a digitally controlled ramp of the regulated output voltage from 0V to the commanded voltage set point over the programmed TON_RISE period, allowing inrush current control. During the soft-start ramp, the LTC3882-1 does not initiate PWM operation until the commanded output exceeds the actual rail voltage. This allows the regulator to start up into a pre-biased load even when using gate drivers or power blocks that do not support discontinuous operation. The soft-start feature is disabled by setting the value of TON_RISE to any time less than 0.25ms.

Time-Based Output Sequencing

The LTC3882-1 supports time-based on and off output sequencing using a shared time reference (SHARE_CLK). Following a valid qualified command to turn on, each output is enabled after waiting its programmed TON_DELAY. This can be used to sequence outputs in a prescribed order that can be preprogrammed as needed without hardware modification. Channel off-sequencing is accomplished in a similar way with the TOFF_DELAY command.

Output Ramping Control

The LTC3882-1 supports synchronized output on and off ramping control using a shared time reference (SHARE_CLK). Power rail on and off relationships similar to those of conventional analog tracking functions can be achieved by using programmed delays and TON_RISE and TOFF_FALL times. However, with LTC3882-1 digital control, on and off ramping methods need not be the same, and ramping configurations can be reprogrammed as needed without hardware modification.

Programmable fault responses and fault sharing can ensure that any desired time-based output sequencing and ramping control is properly accomplished each time the system powers up or down. Refer to the Applications Information section for various LTC3882-1 hardware and PMBus command configurations needed to fully support synchronization for time-based sequencing and output ramping when using multiple ICs.

Voltage-Based Output Sequencing

It is also possible to sequence outputs using cascaded voltage events. To do this, the PGOOD status output from one PWM channel can be used to control the RUN pin of a downstream channel. This keeps the downstream channel off unless acceptable output conditions exist on the controlling channel.

Output Disable

Both PWM channels are disabled any time VINSNS is below the VIN_OFF threshold. The power stages are immediately shut off to stop the transfer of energy to the load(s) as quickly as possible.

A PWM channel may also be disabled in response to certain internal fault conditions, an external fault propagated into a $\overline{\text{FAULT}}$ pin, or loss of SHARE_CLK. In these cases the power stage is immediately shut off to stop the transfer of energy to the load as quickly as possible. Refer to the following Fault Detection and Handling section for additional details related to fault recovery.

Each PWM channel can be disabled with a PMBus OPERATION command at any time if enabled by ON_OFF_CONFIG. This will force a controlled turn-off response with defined delay (TOFF_DELAY) and ramp down rate (TOFF_FALL). The controller will maintain the programmed mode of operation for TOFF_FALL. In DCM, the controller will not draw current from the load and fall time will be set by output capacitance and load current.

OPERATION

Finally, each PWM channel can be commanded off by pulling the associated RUN pin low. Pulling the RUN pin low can force the channel to perform a controlled turn off or immediately disable the power stage, depending on the programming of the ON_OFF_CONFIG command.

Minimum Output Disable Times

When a PMBus OPERATION command is used to turn off an LTC3882-1 channel, a minimum output disable time of 120ms is imposed regardless of how quickly the channel is commanded back on. If bit 4 of MFR_CHAN_CONFIG is clear, a PMBus command to turn the channel off also pulses the RUN pin low. Once the RUN pin is pulled low internally or externally, a minimum output disable time (RUN forced low) of TOFF_DELAY + TOFF_FALL + 136ms is enforced. If MFR_RESTART_DELAY is greater than this mandatory minimum, the larger value of MFR_RESTART_DELAY is used. In either case the LTC3882-1 holds its own RUN pin low during the entire disable period. These minimum off times allow a consistent channel restart with coherent monitor ADC values and make the LTC3882-1 highly compatible with other LTC PMBus digital power system management products.

Output Short Cycle

An output short cycle condition is created when a master channel is commanded back on while waiting for TOFF_DELAY or TOFF_FALL to expire. Any time this occurs, the LTC3882-1 asserts the Short Cycle bit in STATUS_MFR_SPECIFIC. Device response at that point is governed by bits in MFR_CHAN_CONFIG_LTC3882-1 and SMBALERT_MASK. Refer to the detailed descriptions of those commands for additional details. Generally, the LTC3882-1 should be controlled so that short cycle conditions are not created during normal operation.

Light Load Current Operation

The LTC3882-1 has two modes of PWM operation: discontinuous conduction mode (DCM) and forced continuous conduction mode (CCM). Mode selection is made with the MFR_PWM_MODE command.

In DCM, the inductor current is not allowed to reverse. The reverse current comparator I_{REV} disables the external bottom MOSFET (synchronous rectifier) when the inductor current reaches approximately 0A, preventing it from going substantially negative. The external gate driver or power block must have short delays to a high impedance output, relative to the PWM cycle, to support DCM.

Efficiency at light loads in CCM is lower than in DCM. Continuous conduction mode exhibits less interference with audio circuitry but may result in reverse inductor current, for instance at light loads or under large transient conditions.

Switching Frequency and Phase

There is a high degree of flexibility for setting the PWM operating frequency of the LTC3882-1. The switching frequency of the PWM can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes PWM control to this timing reference with proper phase relation, whether the clock is provided internally or externally. The device can also be configured to provide the master clock to other ICs through PMBus command, EEPROM setting, or external configuration resistors as outlined in application Table 10. For PMbus or EEPROM configuration, the LTC3882-1 is designated as a clock master by clearing bit 4 of MFR_CONFIG_ALL_LTC3882-1. As clock master, the LTC3882-1 will drive its open-drain SYNC pin at the selected rate with a pulse width of 125ns. An external pull-up resistor between SYNC and V_{DD33} is required in this case. Only one device connected to SYNC should be designated to drive the pin. If more than one LTC3882-1 sharing SYNC is programmed as clock master, just one of the devices is automatically elected to provide the clock. The others disable their SYNC outputs and indicate this with bit 10 of MFR_PADS_LTC3882-1.

The LTC3882-1 will automatically accept an external SYNC input, disabling is own SYNC drive if necessary, as long as the external clock frequency is greater than 1/2 of the programmed internal oscillator. Whether configured to drive SYNC or not, the LTC3882-1 can continue PWM operation at the selected frequency (FREQUENCY_SWITCH) using its own internal oscillator, if an external clock signal is subsequently lost.

The MFR_PWM_CONFIG_LTC3882-1 command can be used to configure the phase of each channel. Desired phase

OPERATION

can also be set from EEPROM or external configuration resistors as outlined in Table 10. Phase designates the relationship between the falling edge of SYNC and the internal clock edge that resets the PWM latch. That reset turns off the top power switch, producing a PWM falling edge. Additional small propagation delays to the PWM control pins will apply.

The phase relationships and frequency are independent of each other, providing numerous application options. Multiple LTC3882-1 ICs can be synchronized to realize a PolyPhase array. In this case the phases should be separated by 360/n degrees, where n is the number of phases driving the output voltage rail.

PolyPhase Load Sharing

Multiple LTC3882-1 ICs can be combined to provide a balanced load-share solution by configuring the necessary pins. The SHARE_CLK and SYNC pins of all load-sharing channels should be bussed together. Connecting the SYNC pins synchronizes the PWM controllers with each other. Bussing the SHARE_CLK pins together allows the phases to start synchronously. Refer to the discussion in the previous Power-Up and Initialization section. The last device to see all start-up conditions satisfied controls the initiation of power sequencing for all phases.

Due to the low output impedance of the LTC3882-1 error amplifiers, PolyPhase applications should use the error amplifier of only one phase as the master. The FB pins of each slave channel must be wired to V_{DD33}, and the COMP pins of each slave phase must be connected to the master error amplifier COMP output. This disables the slave error amplifiers and provides a single point of voltage control and loop stabilization for the PolyPhase output rail.

For PolyPhase load sharing the LTC3882-1 also incorporates an auxiliary current sharing loop. Referring back to Figure 1, the instantaneous current of each slave phase is sensed by current amplifier CA and compared to the I_{AVG} pin. The I_{AVG} and I_{AVG_GND} pins of each phase are wired together, and a small capacitor (50pF to 200pF) between I_{AVG} and I_{AVG_GND} stores a voltage corresponding to the average master phase output current. The difference in this average and the instantaneous phase current is integrated. The output of integrator S of each slave phase is then proportionally summed with the master error amplifier COMP output to adjust the duty cycle and balance the current contribution of that phase. Additional hardware configuration and digital programming requirements apply in PolyPhase systems. Refer to the Applications Information section for complete details on building PolyPhase rails with the LTC3882-1.

Active Voltage Positioning

Load slope is programmable in the LTC3882-1 via the MFR_VOUT_AVP PMBus command. The inductor current measured at the I_{SENSE} pins is converted to a voltage which is then subtracted from the voltage reference at the positive input of the error amplifier. The final load slope is defined by the inductor current sense element and the bits set in the MFR_VOUT_AVP PMBus command. Setting MFR_VOUT_AVP to a value greater than 0.0% automatically disables output servo mode for that channel.

Input Supply Monitoring

The input supply voltage is sensed by the LTC3882-1 at the VINSNS pin. Undervoltage, overvoltage, valid on and off levels can be programmed for V_{IN}. Refer to the following PMBus Command Details section for more information on programming the input supply thresholds. In addition, the telemetry ADC monitors the VINSNS voltage relative to GND. Conversion results are returned by the READ_VIN PMBus command.

Output Voltage Sensing and Monitoring

Both PWM channels allow remote, differential sensing of the load voltage with V_{SENSE} pins. The channel 1 output sense pin V_{SENSE1}^{-} is internally shorted to GND (the exposed pad). The telemetry ADC is fully differential and makes its measurements of the output voltages of channels 0 and 1 at $V_{SENSE0}^{\pm}$ and $V_{SENSE1}^{\pm}$, respectively. Conversion results are returned by the READ_VOUT PMBus command.

Output Current Sensing and Monitoring

Both channels allow differential sensing of the inductor current using either the inductor DCR or a resistor in series with the inductor across the I_{SENSE} pins. When the I_{SENSE} pins for a channel are multiplexed to the differential inputs

OPERATION

of the LTC3882-1 monitor ADC, they have an input range of approximately ±128mV and a noise floor of 7µV_{RMS}. Peak-peak noise is approximately 46.5µV. The internal ADC anti-aliasing filter and conversion rate produce an average reading of the I_{SENSE} differential voltage. The resulting value is returned by the READ_IOUT PMBus command. Refer to the Applications Information section for details on sensing output current using inductor DCR or discrete resistors.

External and Internal Temperature Sense

External temperature can best be measured using a remote, diode-connected PNP transistor such as the MMBT3906. The emitter should be connected to a TSNS pin while the base and collector terminals of the PNP transistor must be shorted together and returned directly to the LTC3882-1 GND pin. Two different currents are applied to the diode (nominally 2µA and 32µA) and the temperature is calculated from a ΔV_{BE} measurement made with the internal 16-bit monitor ADC.

The LTC3882-1 also supports direct V_{BE} based external temperature measurements. In this case the diode or diode network is trimmed to a specific voltage at a specific current and temperature. In general this method does not yield as accurate a result as the ΔV_{BE} measurement. Refer to MFR_PWM_MODE_LTC3882-1 in the PMBus Command Details section for additional information on programming the LTC3882-1 for these two external temperature sense configurations.

The calculated temperature is returned by the PMBus READ_TEMPERATURE_1 command. Refer to the Applications Information section for details on proper layout of external temperature sense elements and PMBus commands that can be used to improve the accuracy of calculated temperatures.

The READ_TEMPERATURE_2 command returns the internal junction temperature of the LTC3882-1 using an on-chip diode with a ΔV_{BE} measurement and calculation.

Resistor Configuration Pins

Six input pins can be used to configure key operating parameters with selected 1% resistors arranged between V_{DD25} and GND as a divider to the pin(s). The pins are ASEL0, ASEL1, V_{OUT0_CFG}, V_{OUT1_CFG}, FREQ_CFG, and PHAS_CFG. If any of these pins are left open the value stored in the corresponding EEPROM command is used. The resistor configuration pins are only measured during power-up and execution of RESTORE_USER_ALL or MFR_RESET commands. If bit 6 of the MFR_CONFIG_ALL_LTC3882-1 command is set in EEPROM, all resistor inputs **except** ASEL*n* are ignored. Per the PMBus specification, all pin-programmed parameters can be overridden at any time by commands from the digital interface.

The ASEL*n* pin settings are described in application Table 11. These pins can be used to select the entire LTC3882-1 device address. ASEL0 always programs the bottom four bits of the device address for the LTC3882-1 unless left open. ASEL1 can be used to program the three most-significant bits. Either portion of the address can also be retrieved from the MFR_ADDRESS value in EEPROM. If both pins are left open, the full 7-bit MFR_ADDRESS value stored in EEPROM is used to determine the device address. The LTC3882-1 always responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS should not be set to either of these values.

The V_{OUTn_CFG} pin settings are described in application Table 8. These pins select the output voltages for the related channel.

The following parameters are also set as a percentage of the programmed V_{OUT} if resistor configuration pins are used to determined output voltage:

- VOUT_OV_FAULT_LIMIT: +10%
- VOUT_OV_WARN_LIMIT: +7.5%
- VOUT_MAX: +7.5%
- VOUT_MARGIN_HIGH: +5%
- VOUT_MARGIN_LOW: –5%
- VOUT_UV_WARN_LIMIT: –6.5%
- VOUT_UV_FAULT_LIMIT: –7%

The FREQ_CFG pin settings are described in application Table 9. This pin selects the switching frequency of the internal oscillator and enables the SYNC output if not left open, shorted to GND or ignored by EEPROM setting.

OPERATION

The PHAS_CFG pin settings are described in Table 10. This pin selects the phase relationships between the two channels and the selected clock source.

Internal EEPROM with CRC and ECC

The LTC3882-1 contains internal EEPROM with Error Correcting Coding (ECC) to store user configuration settings and fault log information. EEPROM endurance and retention for user space and fault log pages are specified in the Absolute Maximum Ratings and Electrical Characteristics table.

The integrity of the entire onboard EEPROM is checked with a CRC calculation each time its data is to be read, such as after a power-on reset or execution of a RESTORE_USER_ALL command. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the EEPROM CRC Error bit in the STATUS_MFR_SPECIFIC command is set, and the $\overline{\text{ALERT}}$ and RUN pins pulled low (PWM channels off). At that point the device will only respond at special address 0x7C, which is activated only after an invalid CRC has been detected. The chip will also respond at the global addresses 0x5A and 0x5B, but use of these addresses when attempting to recover from a CRC issue is not recommended. All power supply rails associated with either PWM channel of a device reporting an invalid CRC should remain disabled until the issue is resolved.

LTC recommends that the EEPROM not be written when die temperature is greater than 85°C. If internal die temperature exceeds 130°C, all EEPROM operations except RESTORE_USER_ALL and MFR_RESET are disabled. Full EEPROM operation is not re-enabled until die temperature falls below 125°C. Refer to the Applications Information section for equations to predict retention degradation due to elevated operating temperatures.

See the Applications Information section or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming, which the LTC3882-1 also supports.

Fault Detection

A variety of fault and warning detection, reporting and handling mechanisms are provided by the LTC3882-1. Fault or warning detection capabilities include:

- Input Under/Overvoltage
- Output Under/Overvoltage
- Output Overcurrent (Peak and Average)
- Internal and External Overtemperature and External Undertemperature
- CML Fault (Communication, Memory, or Logic)
- External Fault Detection via Bidirectional $\overline{\text{FAULT}}$ Pins

Reporting is covered in following sections on status commands (registers) and $\overline{\text{ALERT}}$ pin function. Fault handling mechanisms include hardwired, low-level PWM safety responses that always occur, and higher-level programmable event management. Both types are covered in the following sections.

Input Supply Faults

Input undervoltage and overvoltage limits are determined from multiplexed monitor ADC conversions. Therefore the input UV/OV response is naturally deglitched by the 90ms typical conversion cycle of the ADC. There is no hardwired low-level PWM response for any input supply fault.

Hardwired PWM Response to V_{OUT} Faults

V_{OUT} undervoltage (UV) and overvoltage (OV) faults are detected by supervisor comparators. The OV and UV fault limits can be set in three ways:

- As a Percentage of V_{OUT} if Using the Resistor Configuration Pins
- From Stored EEPROM Values
- By PMBus Command

The output overvoltage comparator guards against transient overshoots as well as long term overvoltages at the output. When an output OV fault is detected the top MOSFET for that channel is commanded off and the bottom MOSFET is commanded on until the overvoltage condition is cleared

OPERATION

or for PWM control protocol 0, reverse overcurrent is detected. See I_{OUT} faults below.

UV faults and warnings are masked if the channel has been commanded off or until all of the following criteria are achieved.

- TON_DELAY Has Expired
- TON_RISE Ramp Has Completed
- TON_MAX_FAULT_LIMIT Has Been Reached
- IOUT_OC_FAULT_LIMIT Has Not Been Reached
- TOFF_FALL Is Not in Progress

Output UV warnings are determined from multiplexed monitor ADC conversions. The LTC3882-1 has no hardwired PWM response for output UV faults or warnings.

Power Good Indication (Master)

An LTC3882-1 master phase indicates Power Good on its PGOOD pin and in PMBus commands STATUS_WORD (paged) and MFR_PADS_LTC3882-1 based on programmed UV and OV fault limits. Power Good is indicated on a master phase as long as it is enabled to run and V_{OUT} is between the UV and OV fault limits. If a master channel is off for any reason, its PGOOD pin is driven low and Power Not Good is indicated in the status commands.

Power Good Indication (Slave)

As long as they are enabled, slave phases indicate Power Good on PGOOD and in PMBus status commands, unless a master error amplifier (EA) fault is detected. An EA fault indicates the bussed COMP voltage appears to be too high.

When a slave detects an EA fault, its output is immediately disabled and OV is indicated (see Figure 2). Any valid higher-level OV fault response and propagation may be set for a slave channel to handle a detected EA fault. If the OV fault response is set to ignore, the slave output is re-enabled when the EA/COMP condition clears.

A slave indicates Power Not Good with PMBus status commands during an EA fault, but its PGOOD pin remains high impedance. If a slave phase is off for any other reason, its PGOOD pin is also driven low.

Hardwired PWM Response to I_{OUT} Faults

The LTC3882-1 measures average I_{OUT} from the voltage across the I_{SENSE} pins, taking into account the sense resistor or DCR value and its associated temperature coefficient. Both are provided by PMBus command or EEPROM values.

An output overcurrent (OC) fault condition is detected by a supervisor comparator for each PWM output when the sensed instantaneous current for that channel reaches its maximum allowed value. Refer to the IOUT_OC_FAULT_LIMIT PMBus command for details. When an OC fault is detected the controller immediately disables the top FET, and the bottom FET is normally commanded on for the remainder of that PWM cycle.

If programmed to operate in CCM, the LTC3882-1 also uses the negative of IOUT_OC_FAULT_LIMIT to detect a reverse overcurrent (ROC) fault. When an ROC fault occurs the controller immediately disables both top and bottom FETs, unless PWM output protocol 1 is selected with MFR_PWM_MODE_LTC3882-1.

OC and ROC faults are both handled according to the IOUT_OC_FAULT_RESPONSE for that channel. Either hardware response can result in current-limited operation using pulse truncation or skipping. Because the LTC3882-1 uses leading edge modulation, this will cause a shift in average phase toward 0° on the faulted channel and an increase in input ripple current

Output OC warnings are determined from multiplexed monitor ADC conversions. The LTC3882-1 has no hardwired PWM response if an output OC warning occurs.

Hardwired PWM Response to Temperature Faults

An internal temperature sensor measured by the monitor ADC protects against EEPROM and other IC damage. When die temperature rises above 130°C, the LTC3882-1 will NACK any EEPROM-related command except RESTORE_USER_ALL and MFR_RESET and issue a CML fault for Invalid/Unsupported Command. Normal EEPROM access is re-enabled when die temperature drops below 125°C. Above 160°C, the part shuts down all PWM outputs until die temperature is below 150°C. Internal temperature fault limits cannot be adjusted. Writing to the EEPROM above a die temperature of 85°C is strongly discouraged.