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Dual Output PolyPhase Step-Down DC/DC Controller with Digital Power System Management

FEATURES

- **PMBus/I²C Compliant Serial Interface**
  - **Telemetry Read Back includes V_{IN}, I_{IN}, V_{OUT}, I_{OUT}, Temperature, Duty Cycle and Faults**
  - **Programmable Voltage, Current Limit, Digital Soft-Start/Stop, Sequencing, Margining, OV/UV and Frequency Synchronization (250kHz to 1MHz)**
- **±0.5% Output Voltage Accuracy Over Temperature**
- **Integrated 16-Bit ADC**
- **V_{OUT} Range: 0.5V to 5.5V (V_{OUT0}, V_{OUT1})**
- **Internal EEPROM and Fault Logging**
- **Integrated N-Channel MOSFET Gate Drivers (LTC3887)**
- Wide V_{IN} Range: 4.5V to 24V
- Analog Current Mode Control Loop
- Remote Differential Sense for PolyPhase® Applications
- Accurate PolyPhase Current Sharing for Up to Six Phases
- Available in a 40-Pin (6mm × 6mm) QFN Package

APPLICATIONS

- High Current Distributed Power Systems
- Telecom, Datacom and Storage Systems
- Intelligent Energy Efficient Power Regulation

DESCRIPTION

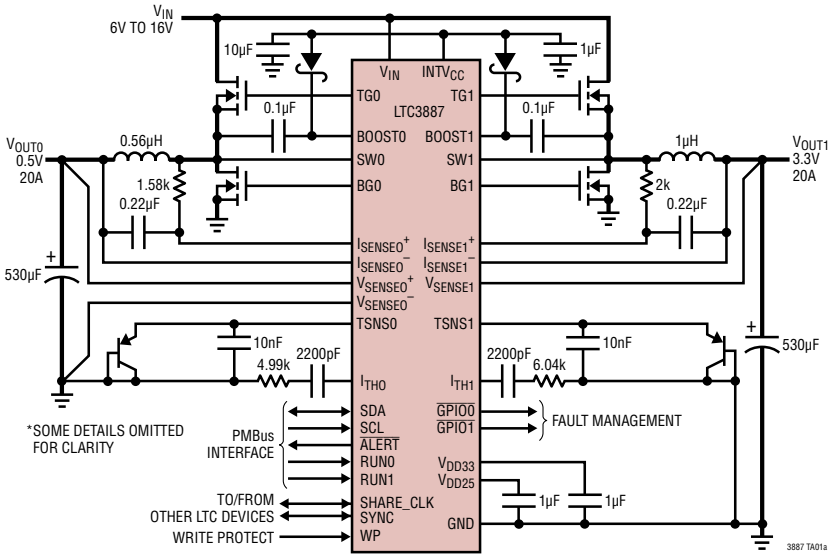
The LTC®3887/LTC3887-1 are dual, PolyPhase DC/DC synchronous step-down switching regulator controllers with an I²C-based PMBus compliant serial interface. The controllers use a constant frequency, current mode architecture that is supported by LTpowerPlay™ a software development tool with graphical user interface (GUI).

Switching frequency, channel phasing, output voltage, and device address can be programmed using external configuration resistors. Additionally, parameters can be set via the digital interface or stored in EEPROM. Voltage, current, internal/external temperature and fault status can be read back through the bus interface.

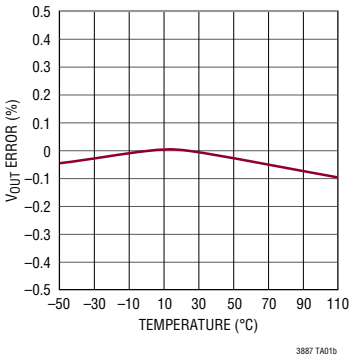
The LTC3887 has integrated gate drivers. The LTC3887-1 has three-state PWM pins to drive power blocks or DrMOS power stages. The LTC3887 is an enhanced version of the LTC3880 with greater output voltage range and more digital features. Refer to page 15 for more detail.

TYPICAL APPLICATION

Dual 350kHz 3.3V/0.5V Step-Down Converter



Regulated Output Voltage vs Temperature, V_{OUT} = 0.5V



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ABSOLUTE MAXIMUM RATINGS

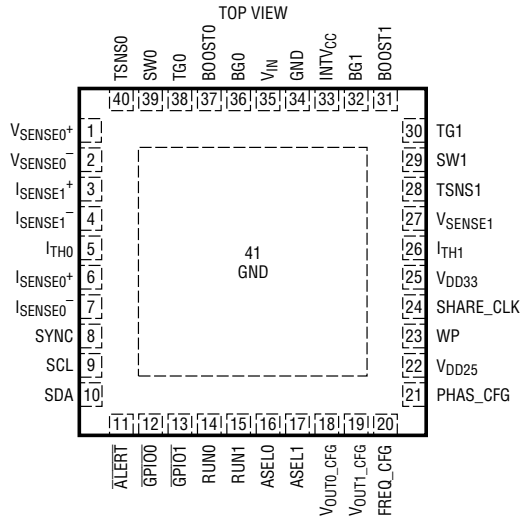
(Note 1)

V_{IN} Voltage ..... –0.3V to 28V
Top Gate Transient Voltage TG0,
TG1 LTC3887 ..... –5V to 34V
Top Gate Transient Voltage PWM0,
PWM1 LTC3887-1 ..... –0.3V to 6V
BOOST1, BOOST0 LTC3887 ..... –0.3V to 34V
V_{CC1}, V_{CC0} LTC3887-1 ..... –0.3V to 6V
Switch Transient Voltage SW1,
SW0 LTC3887 ..... –5V to 28V
$INTV_{CC}$, (BOOST1 – SW1), (BOOST0 – SW0),
BG0, BG1, LTC3887 ..... –0.3V to 6V

V_{SENSE0}^+, V_{SENSE1}, $I_{SENSE0n}$, $I_{SENSE1n}$ ..... –0.3V to 6V
RUN0, RUN1, SDA, SCL, $\overline{ALERT}$ ..... –0.3V to 5.5V
FREQ_CFG, V_{OUTn_CFG}, ASEL0/1, V_{DD25} .... –0.3V to 2.75V
V_{DD33}, $\overline{GPIO0}$, $\overline{GPIO1}$, TSNS0, TSNS1, V_{SENSE0}^-,
SHARE_CLK, WP, SYNC, ITH*n* ..... –0.3V to 3.6V
$INTV_{CC}$ Peak Output Current 100mA
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –40°C to 150°C*
*See Derating EEPROM Retention at Temperature in the Applications Information section for junction temperatures in excess of 125°C.

PIN CONFIGURATION

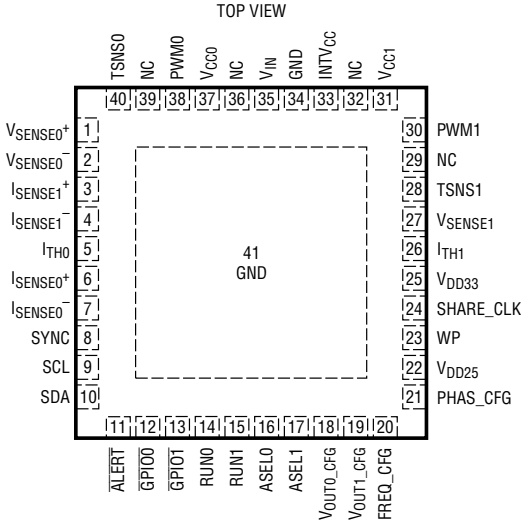
LTC3887



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 33°C/W, θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

LTC3887-1



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 33°C/W, θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3887#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC3887EUJ#PBF	LTC3887EUJ#TRPBF	LTC3887UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3887IUJ#PBF	LTC3887IUJ#TRPBF	LTC3887UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3887EUJ-1#PBF	LTC3887EUJ-1#TRPBF	LTC3887UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3887IUJ-1#PBF	LTC3887IUJ-1#TRPBF	LTC3887UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage							
V_{IN}	Input Voltage Range	(Note 12)	●	4.5		24	V
I_Q	Input Voltage Supply Current Normal Operation	 $V_{RUN0,1}$ = 3.3V, No Caps on TG and BG $V_{RUN0,1}$ = 0V			 25 20		 mA mA
V_{UVLO}	Undervoltage Lockout Threshold when V_{IN} > 4.3V	V_{INTVCC} Falling V_{INTVCC} Rising			3.7 3.95		V V
T_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts.			70		ms
Control Loop							
V_{OUTR0}	Full-Scale Voltage High Range Set Point Accuracy (0.6V to 5V) Resolution LSB Step Size	VOUT_COMMAND = 5.500V (Note 9)	● ●	5.45 –0.5	 12 1.375	5.55 0.5	V % Bits mV
V_{OUTR1}	Full-Scale Voltage Low Range Set Point Accuracy (0.6V to 2.5V) Resolution LSB Step Size	VOUT_COMMAND = 2.75V (Note 9)	● ●	2.7 –0.5	 12 0.6875	2.8 0.5	V % Bits mV
$V_{LINEREG}$	Line Regulation	6V < V_{IN} < 24V	●			±0.02	%/V
$V_{LOADREG}$	Load Regulation	ΔV_{ITH} = 1.35V – 0.7V ΔV_{ITH} = 1.35V – 2.0V	● ●		0.01 –0.01	0.1 –0.1	% %
$g_{m0,1}$	Error Amplifier g_m	$I_{TH0,1}$ =1.22V			3		mmho
$I_{ISENSE0,1}$	Input Current	V_{ISENSE} = 5.5V	●		±1	±3	µA
$V_{SENSERIN0}$	V_{SENSE} Input Resistance to Ground	0V ≤ V_{PIN} ≤ 5.5V			41		kΩ
$V_{SENSERIN1}$	V_{SENSE} Input Resistance to Ground	0V ≤ V_{PIN} ≤ 5.5V			37		kΩ
$V_{IILIMIT}$	Resolution				3		bits
	$V_{ILIMMAX}$	Hi Range Lo Range	● ●	68 44	75 50	82 56	mV mV
	V_{ILMMIN}	Hi Range Lo Range			37.5 25		mV mV
Gate Drivers LTC3887							
TG0,1 t_r t_f	TG Transition Time (LTC3887/LTC3887-1) Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
BG0,1 t_r t_f	BG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time (LTC3887/LTC3887-1)				90		ns
OV Output Voltage Supervisor							
N	Resolution				8		Bits
V_{RANGE0}	Voltage Monitoring Range	Range Value = 0		1		5.6	V
V_{RANGE1}	Voltage Monitoring Range	Range Value = 1		0.5		2.7	V
V_{OUSTP0}	Threshold Programming Step	Range Value = 0			22.5		mV
V_{OUSTP1}	Threshold Programming Step	Range Value = 1			11.25		mV
V_{THACC0}	Threshold Accuracy 2V < V_{OUT} < 5V	Range Value = 0	●			±2	%
V_{THACC1}	Threshold Accuracy 1V < V_{OUT} < 2.5V	Range Value = 1	●			±2	%
t_{PROPOV}	OV Comparator to $\overline{GPIO}$ Low Time	V_{OD} = 10% of Threshold				35	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
UV Output Voltage Supervisor							
N	Resolution				8		bits
V_{RANGE0}	Voltage Range	High Range		1		5.5	V
V_{RANGE1}	Voltage Range	Low Range		0.5		2.7	V
V_{OUSTP0}	Step Size	Range Value = 0, High Range			22		mV
V_{OUSTP1}	Step Size	Range Value = 1, Low Range			11		mV
V_{THACC0}	Threshold Accuracy 2V < V_{OUT} < 5V	Range Value = 0, High Range	●			±2	%
V_{THACC1}	Threshold Accuracy 1V < V_{OUT} < 2.5V	Range Value = 1, Low Range	●			±2	%
t_{PROPUV}	UV Comparator to $\overline{GPIO}$ Low Time	V_{OD} = 10% of Threshold				100	µs
V_{IN} Voltage Supervisor							
N	Resolution				8		bits
$V_{INRANGE}$	Full-Scale Voltage			4.5		20	V
V_{INSTP}	Step Size				82		mV
$V_{INTHACC}$	Threshold Accuracy 9.0V < V_{IN} < 20V		●			±2.5	%
$V_{INTHACC\backslash M}$	Threshold Accuracy 4.5V < V_{IN} ≤ 9V		●			±5	%
$t_{PROPVIN}$	Comparator Response Time (VIN_ON and VIN_OFF)	V_{OD} = 10% of Threshold				100	µs
Output Voltage Readback							
N	Resolution LSB Step Size				16 244		Bits µV
V_{OFS}	Full-Scale Voltage	(Note 10) V_{RUNn} = 0V (Note 8)			8		V
V_{OUT_TUE}	Total Unadjusted Error	(Note 8) V_{OUTn} > 0.6V	●			0.5	%
V_{OS}	Zero-Code Offset Voltage					±500	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			100		ms
V_{IN} Voltage Readback							
N	Resolution	(Note 5)			10		Bits
V_{IFS}	Full-Scale Voltage	(Note 11)			38.91		V
V_{IN_TUE}	Total Unadjusted Error	V_{VIN} > 4.5V (Note 8) 	 ●			0.5 2	% %
$t_{CONVERT}$	Conversion Time	(Note 6)			100		ms
Output Current Readback							
N	Resolution LSB Step Size	(Note 5) 0V ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 16mV 16mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 32mV 32mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 63.9mV 63.9mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 127.9mV			10 15.625 31.25 62.5 125		Bits µV µV µV µV
I_{FS}	Full-Scale Current	(Note 7) R_{ISENSE} = 1mΩ			±128		A
I_{OUT_TUE}	Total Unadjusted Error	(Note 8) V_{ISENSE} > 6mV	●			±1	%
V_{OS}	Zero-Code Offset Voltage					±28	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			100		ms
Input Current and Duty Cycle Readback							
D_RES	Resolution				10		Bits
D_TUE	Total Unadjusted Error	16.3% Duty Cycle		–3		3	%
$t_{CONVERT}$	Update Rate	(Note 6)			100		ms
Temperature Readback (T0, T1, T2)							
T_{RES_T}	Resolution				0.25		°C
T0,1_TUE	External TSNS TUE	ΔV_{TSNS} = 72mV (Note 8)	●			±3	°C
T2_TUE	Internal TSNS TUE	$V_{RUN0,1}$ = 0.0V, f_{SYNC} = 0kHz (Note 8)			±1		°C
$t_{CONVERT\_T}$	Update Rate	(Note 6)			100		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Regulator							
V_{INTVCC}	Internal V_{CC} Voltage No Load	6V < V_{IN} < 24V		4.8	5	5.2	V
V_{LDO_INT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	±2	%
V_{DD33} Regulator							
V_{DD33}	Internal V_{DD33} Voltage	4.5V < V_{INTVCC}		3.2	3.3	3.4	V
$I_{LIM(VDD33)}$	V_{DD33} Current Limit	V_{DD33} = GND			70		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold				3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold				3.1		V
V_{DD25} Regulator							
V_{DD25}	Internal V_{DD25} Voltage				2.5		V
$I_{LIM(VDD25)}$	V_{DD25} Current Limit	V_{DD25} = GND			50		mA
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency Accuracy	250kHz < f_{SYNC} < 1MHz Measured Falling Edge-to-Falling Edge of SYNC with SWITCH_FREQUENCY = 250.0 and 1000.0	●			±7.5	%
$V_{TH,SYNC}$	SYNC Input Threshold	V_{CLKIN} Falling V_{CLKIN} Rising			1 1.5		V V
$V_{OL,SYNC}$	SYNC Low Output Voltage	I_{LOAD} = 3mA			0.2	0.4	V
$I_{LEAKSYNC}$	SYNC Leakage Current in Slave Mode	0V ≤ V_{PIN} ≤ 3.6V				±5	µA
θSYNC-θ0	SYNC to Ch0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	MFR_PWM_CONFIG_LTC3887[2:0] = 0, 2, 3 MFR_PWM_CONFIG_LTC3887[2:0] = 5 MFR_PWM_CONFIG_LTC3887[2:0] = 1 MFR_PWM_CONFIG_LTC3887[2:0] = 4, 6			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1	SYNC to Ch1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	MFR_PWM_CONFIG_LTC3887[2:0] = 3 MFR_PWM_CONFIG_LTC3887[2:0] = 0 MFR_PWM_CONFIG_LTC3887[2:0] = 2, 4, 5 MFR_PWM_CONFIG_LTC3887[2:0] = 1 MFR_PWM_CONFIG_LTC3887[2:0] = 6			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 13)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 13)	T_J < T_{JMAX}	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < TJ < 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, RUN0, RUN1, $\overline{GPIO0}$, $\overline{GPIO1}$							
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN0, RUN1, $\overline{GPIO0}$, $\overline{GPIO1}$	●			2.0	V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN0, RUN1, $\overline{GPIO0}$, $\overline{GPIO1}$	●	1.4			V
V_{HYST}	Input Hysteresis	SCL, SDA			0.08		V
C_{PIN}	Input Capacitance					10	pF
Digital Input WP							
I_{PUWP}	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL, SDA, $\overline{GPIO0}$, $\overline{GPIO1}$, $\overline{ALERT}$, RUN0, RUN1, SHARE_CLK							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
Digital Inputs SHARE_CLK, WP							
V_{IH}	Input High Threshold Voltage				1.5	1.8	V
V_{IL}	Input Low Threshold Voltage			0.6	1		V
Leakage Current SDA, SCL, $\overline{ALERT}$, RUN0, RUN1							
I_{OL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V	●			±5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Leakage Current $\overline{GPIO0}$, $\overline{GPIO1}$							
I_{GL}	Input Leakage Current	0V ≤ V_{PIN} < 3.6V	●			±5	µA
Digital Filtering of $\overline{GPIO0}$, $\overline{GPIO1}$							
I_{FLTG}	Input Digital Filtering $\overline{GPIO}$				3		µs
Digital Filtering of RUN0, RUN1							
I_{FLTR}	Input Digital Filtering RUN				10		µs
PMBus Interface Timing Characteristics							
f_{SMB}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD,STA}$	Hold time After Repeated Start Condition. After this Period, the First Clock is Generated		●	0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		●	0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD,DAT}$	Data Hold Time Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 µs µs
$t_{SU,DAT}$	Data Setup Time Receiving Data		 ●	 0.1			 µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer Non-Block Reads Stuck PMBus Timer Block Reads	Measured from the Last PMBus Start Event			32 150		ms ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3887/LTC3887-1 are tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3887E/LTC3887E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3887I/LTC3887I-1 are guaranteed over the full –40°C to 125°C operating junction temperature range. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 5: The data format in PMBus is 5 bits exponent (signed) and 11 bits mantissa (signed). This limits the output resolution to 10 bits though the internal ADC is 16 bits and the calculations use 32-bit words.

Note 6: The data conversion is done in round robin fashion. All inputs signals are continuously converted for a typical latency of 100ms. Unless the MFR_ADC_CONTROL command is utilized.

Note 7: The IOUT_CAL_GAIN = 1.0mΩ and MFR_IOUT_CAL_GAIN_TC = 0.0. Value as read from READ_IOUT in amperes.

Note 8: Part tested with PWM disabled. Evaluation in application demonstrates capability. TUE (%) = ADC Gain Error (%) + 100 • [Zero Code Offset + ADC Linearity Error]/Actual Value.

Note 9: All V_{OUT} commands assume the ADC is used to auto-zero the output to achieve the stated accuracy. LTC3887 is tested in a feedback loop that servos V_{OUT} to a specified value.

Note 10: The maximum V_{OUT} voltage is 5.5V.

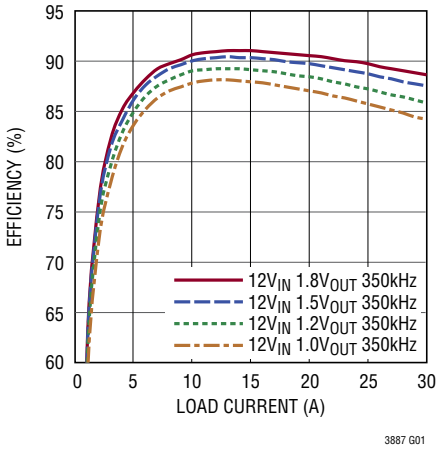
Note 11: The maximum V_{IN} voltage is 28V.

Note 12: When V_{IN} < 6V, $INTV_{CC}$ must be tied to V_{IN}.

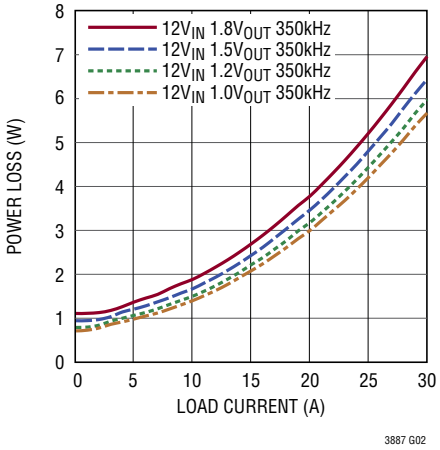
Note 13: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification. The RESTORE_USER_ALL command (EEPROM read) is valid over the entire operating junction temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

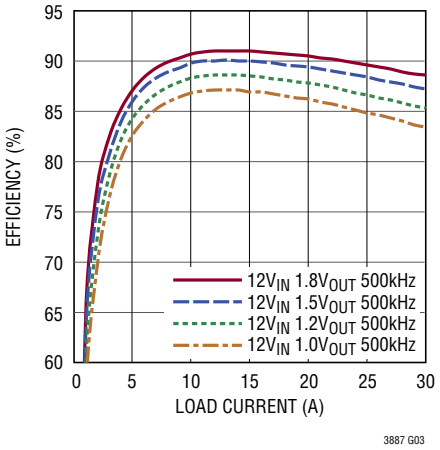
Efficiency vs Load Current
F_{SW} = 350kHz (LTC3887)



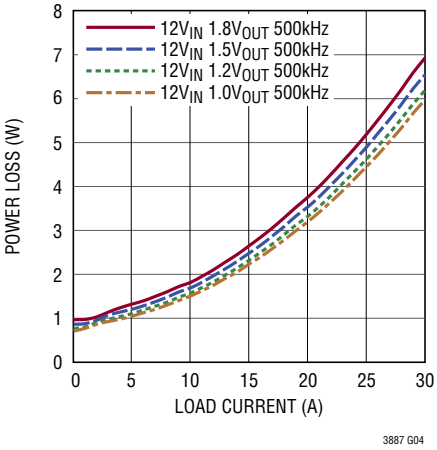
Power Loss vs Load Current
F_{SW} = 350kHz (LTC3887)



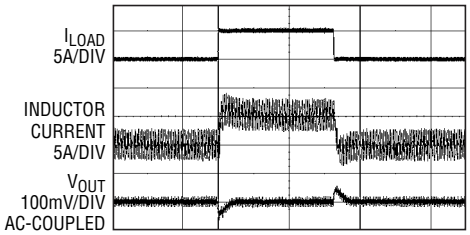
Efficiency vs Load Current
F_{SW} = 500kHz (LTC3887)



Power Loss vs Load Current
F_{SW} = 500kHz (LTC3887)

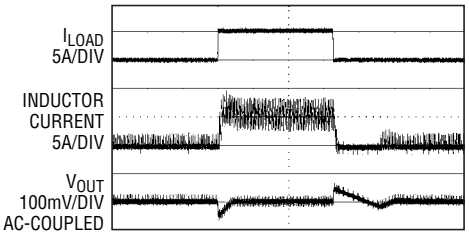


Load Step
(Forced Continuous Mode)



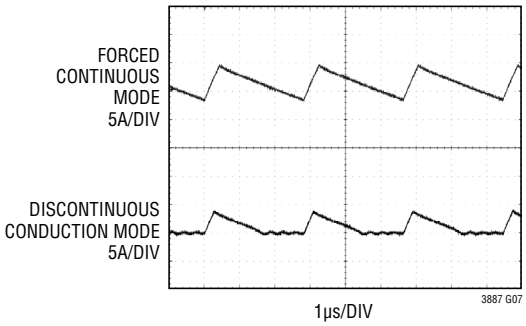
V_{IN} = 12V
50µs/DIV
V_{OUT} = 1.8V
0.3A TO 5A STEP

Load Step
(Pulse-Skipping Mode)



V_{IN} = 12V
50µs/DIV
V_{OUT} = 1.8V
0.3A TO 5A STEP

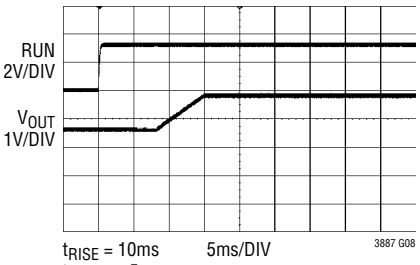
Inductor Current at Light Load



1µs/DIV

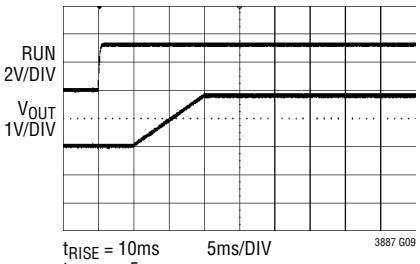
V_{IN} = 12V
V_{OUT} = 1.8V
I_{LOAD} = 1A

Start-Up into a Prebiased Load



t_{RISE} = 10ms
5ms/DIV
t_{DELAY} = 5ms

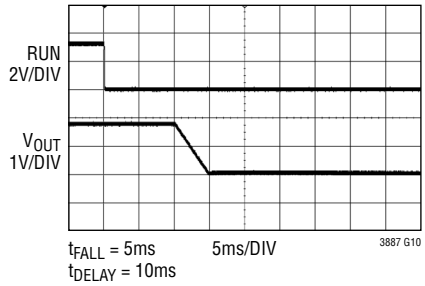
Soft-Start Ramp



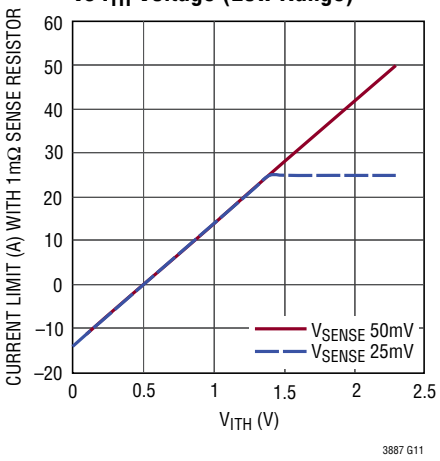
t_{RISE} = 10ms
5ms/DIV
t_{DELAY} = 5ms

TYPICAL PERFORMANCE CHARACTERISTICS

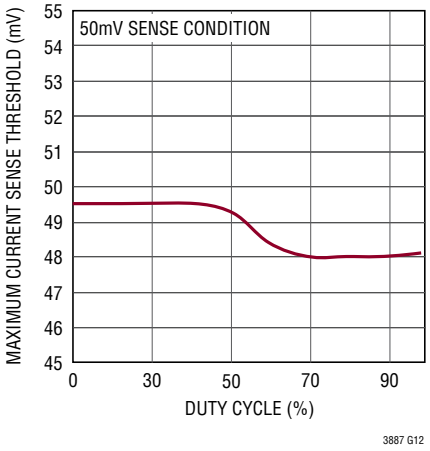
Soft-Off Ramp



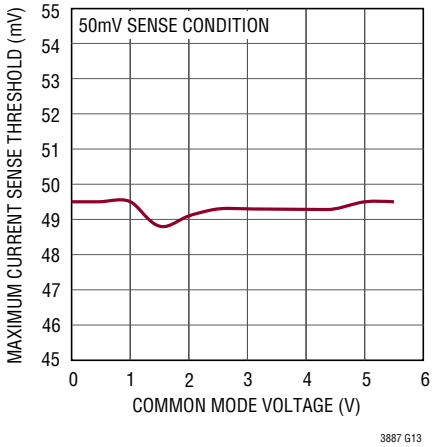
Current Sense Threshold vs I_{TH} Voltage (Low Range)



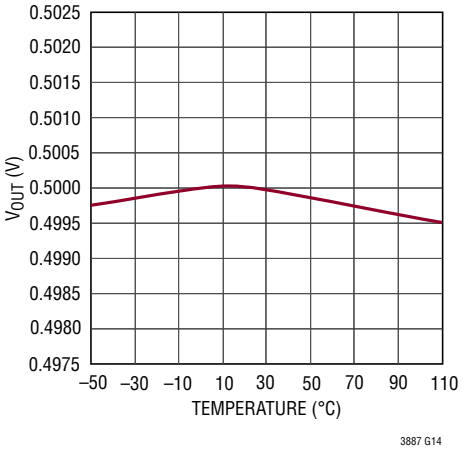
Maximum Current Sense Threshold vs Duty Cycle, V_{OUT} = 0V



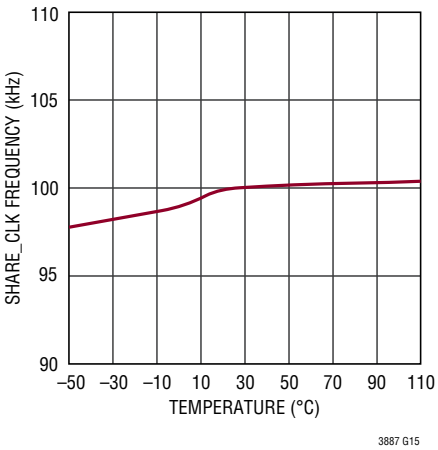
Maximum Current Sense Threshold vs Common Mode Voltage



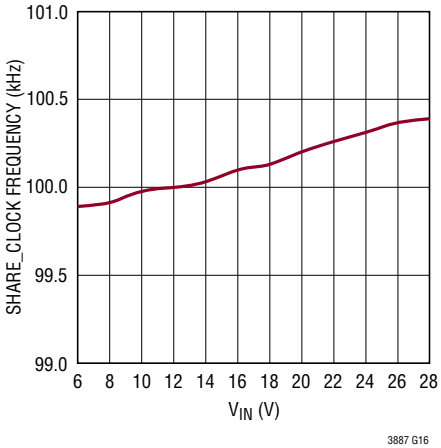
Regulated Output vs Temperature



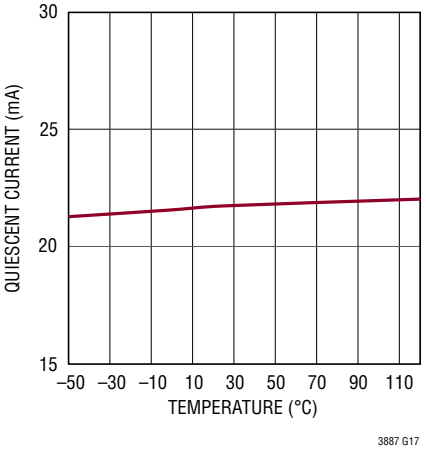
SHARE_CLK Frequency vs Temperature



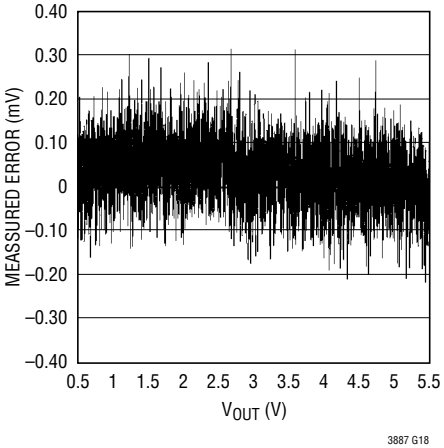
SHARE-CLK Frequency vs V_{IN}



Quiescent Current vs Temperature

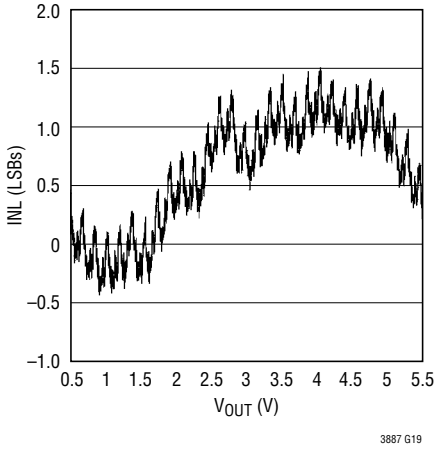


V_{OUT} Measurement vs V_{OUT}



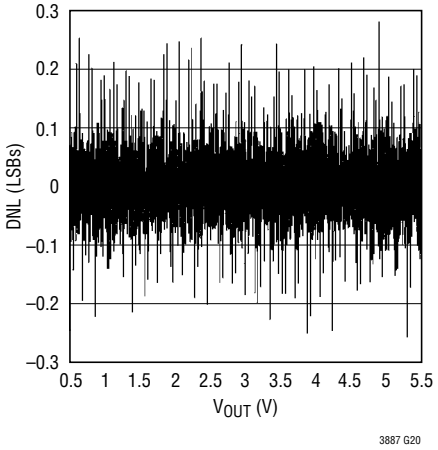
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUT} Command INL



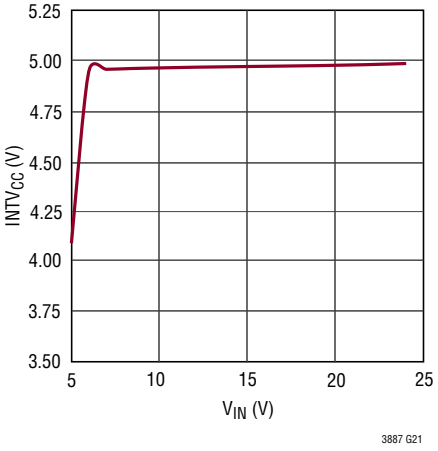
3887 G19

V_{OUT} Command DNL



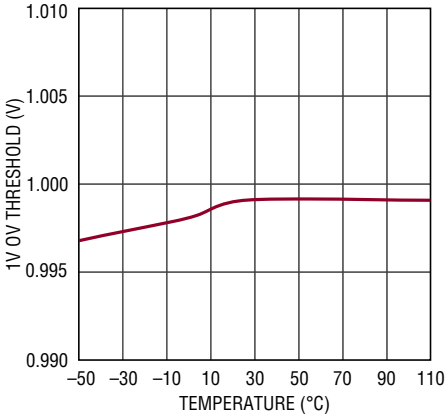
3887 G20

$INTV_{CC}$ Line Regulation



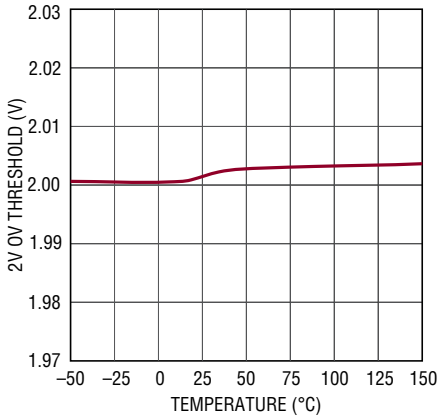
3887 G21

V_{OUT} OV Threshold vs Temperature (1V Target)



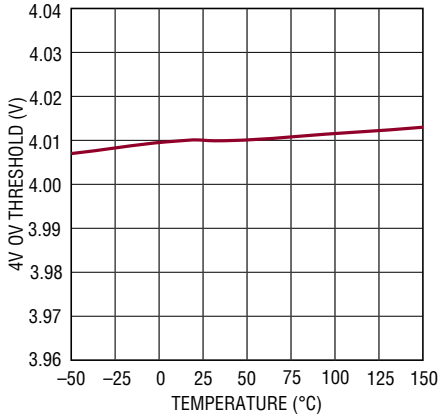
3887 G22

V_{OUT} OV Threshold vs Temperature (2V Target)



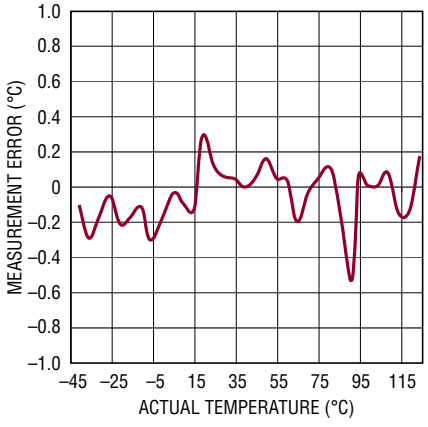
3887 G23

V_{OUT} OV Threshold vs Temperature (4V Target)



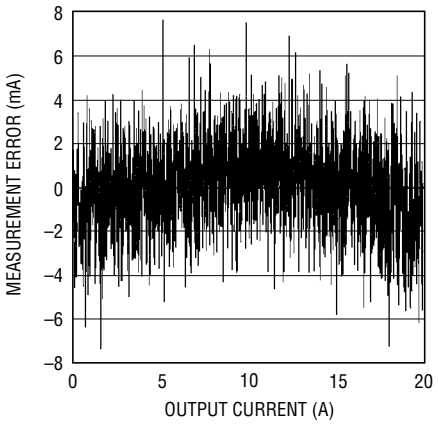
3887 G24

Temperature Error vs Temperature



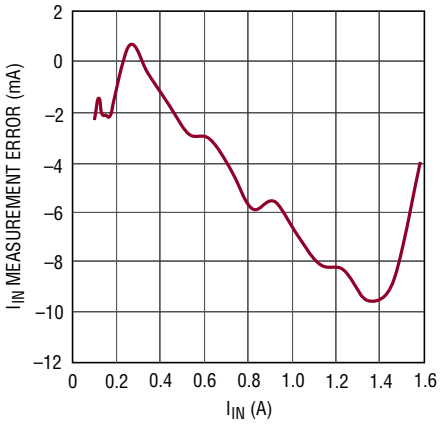
3887 G25

I_{OUT} Error vs I_{OUT} Room Temperature



3887 G26

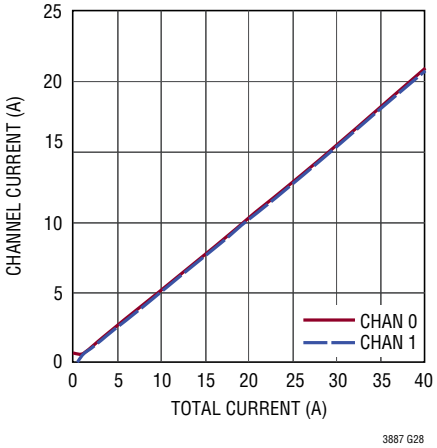
I_{IN} Measurement Error vs I_{IN}



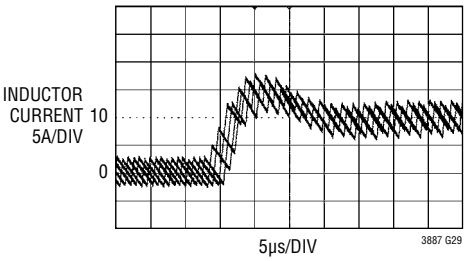
3887 G27

TYPICAL PERFORMANCE CHARACTERISTICS

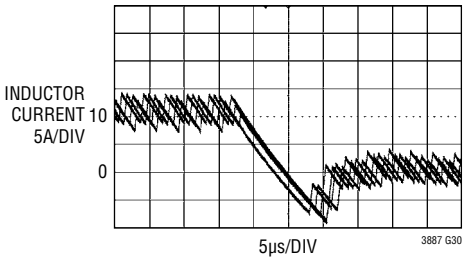
DC Output Current Matching in a 2-Phase System (LTC3887)



Dynamic Current Sharing During a Load Transient in a 4-Phase System



Dynamic Current Sharing During a Load Transient in a 4-Phase System



PIN FUNCTIONS

V_{SENSE0}^+ (Pin 1): Channel 0 Positive Voltage Sense Input.

V_{SENSE0}^- (Pin 2): Channel 0 Negative Voltage Sense Input.

I_{TH0}/I_{TH1} (Pin 5/Pin 26): Current Control Threshold and Error Amplifier Compensation Nodes. Each associated channel's current comparator tripping threshold increases with its I_{TH} voltage.

I_{SENSE0}^+/I_{SENSE1}^+ (Pins 6/Pin 3): Current Sense Comparator Inputs. The (+) inputs to the current comparators are normally connected to DCR sensing networks or current sensing resistors.

I_{SENSE0}^-/I_{SENSE1}^- (Pin 7/Pin 4): Current Sense Comparator Inputs. The (–) inputs are connected to the low side of the current sense element.

SYNC (Pin 8): External Clock Synchronization Input and Open-Drain Output Pin. If an external clock is present at this pin, the switching frequency will be synchronized to the external clock. If the SYNC output is enabled, this pin will pull low at the switching frequency with a 500ns pulse to ground. A resistor pull up to 3.3V is required in the application if the LTC3887 SYNC output is enabled.

SCL (Pin 9): Serial Bus Clock Input. Open-drain output, can hold the output low if clock stretching is enabled. A pull-up resistor to 3.3V is required in the application.

SDA (Pin 10): Serial Bus Data Input and Output. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{ALERT}}$ (Pin 11): Open-Drain Digital Output. Connect the $\overline{\text{SMBALERT}}$ signal to this pin. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{GPIO0}}$/$\overline{\text{GPIO1}}$ (Pin 12/Pin 13): Digital Programmable General Purpose Inputs and Outputs. Open-drain output. A pull-up resistor to 3.3V is required in the application.

RUN0/RUN1 (Pin 14/Pin 15): Enable Run Input and Output. Logic high on these pins enables the controller. Open-drain output holds the pin low until the LTC3887 is out of reset. A pull-up resistor to 3.3V is required in the application.

ASEL0 (Pin 16): Serial Bus Address Configuration Input. Connect a ±1% resistor divider between the chip V_{DD25} ASEL0 and SGND in order to select the 4LSBs of the serial bus interface address. A resistor divider on ASEL0 is recommended if there are more than one LTC3887s on the same board to assure the user can independently program each IC. If the pin is left open, the IC will use the value programmed in the EEPROM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

ASEL1 (Pin 17): Serial Bus Address Configuration Input. Connect a ±1% resistor divider between the chip V_{DD25} ASEL1 and SGND in order to select the 3MSBs of the serial bus interface address. A resistor divider on ASEL1 is recommended if there are more than 16 LTC3887s on the same board to assure the user can independently program each IC. If the pin is left open, the IC will use the value programmed in the EEPROM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

PIN FUNCTIONS

FREQ_CFG (Pin 20): Frequency Select Pin. Connect a ±1% resistor divider between the chip V_{DD25} FREQ_CFG and GND in order to select switching frequency. If the pin is left open, the IC will use the value programmed in the EEPROM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

PHAS_CFG (Pin 21): Phase Select Pin. Connect a ±1% resistor divider between the chip V_{DD25} PHAS_CFG and GND in order to select channel phasing. If the pin is left open, the IC will use the value programmed in the EEPROM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

V_{OUT0_CFG}/V_{OUT1_CFG} (Pin 18/Pin 19): Voltage Select Pin. Connect a ±1% resistor divider between the chip V_{DD25} $V_{OUT}n$_CFG and GND in order to adjust the output voltage set point. If the pin is left open, the IC will use EEPROM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

V_{DD25} (Pin 22): Internally Generated 2.5V power Supply Output Pin. Bypass this pin to GND with a low ESR 1µF capacitor. Do not load this pin with external current except for the ±1% resistor dividers required for the configuration pins.

WP (Pin 23): Write Protect Pin Active High. An internal 10µA current source pulls the pin to V_{DD33}. If WP is high, the PMBus writes are restricted.

SHARE_CLK (Pin 24): Share Clock, Bidirectional Open-Drain Clock Sharing Pin. Nominally 100kHz. Used to synchronize the timing between multiple LTC388Xs. Tie all SHARE_CLK pins together. All LTC388Xs will synchronize to the fastest clock. A pull-up resistor to 3.3V is required.

V_{DD33} (Pin 25): Internally Generated 3.3V Power Supply Output Pin. Bypass this pin to GND with a low ESR 1µF capacitor. Do not load this pin with external current except for the pull-up resistors required for $\overline{GPIO}n$, SCLK, SYNC and possibly RUN*n*, $\overline{ALERT}$, SDA and SCL.

V_{SENSE1} (Pin 27): Channel 1 Voltage Sense Input. This input voltage is referenced to the GND pin.

$INTV_{CC}$ (Pin 33): Internal Regulator 5V Output. The control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

GNDSNS (Pin 34): Ground Sense Pin. This pin is connected to the back paddle ground and can be used to detect if there is a good ground connection between the back paddle and the board.

V_{IN} (Pin 35): Main Input Supply. Decouple this pin to PGND with a capacitor (0.1µF to 1µF). For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together.

BG0/BG1 (Pin 36/Pin 32): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-Channel MOSFETs between PGND and $INTV_{CC}$. BG0/BG1 are not connected on the LTC3887-1. They may be floated or tied to ground.

BOOST0/BOOST1 (LTC3887) (Pin 37/Pin 31): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

V_{CC0}/V_{CC1} (LTC3887-1) (Pins 37/31): These pins should be connected to $INTV_{CC}$ or V_{DD33}.

TG0/TG1 (LTC3887) (Pin 38/Pin 30): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltages.

PWM0/PWM1 (LTC3887-1) (Pin 38/Pin 30): PWM Outputs. These are the three-state control outputs with a voltage swing of GND to V_{CC} used to control gate drivers. The LTC3887-1 PWM pin is three-state which is required to produce discontinuous operation in some gate driver or DrMOS circuits.

SW0/SW1 (LTC3887) (Pin 39/Pin 29): Switch Node Connections to Inductors. Voltage swings at the pins are from a Schottky diode (external) voltage drop below ground to V_{IN}. In the LTC3887-1 these pins are not connected to internal circuitry. They may be floated or tied to ground.

TSNS0/TSNS1 (Pin 40/Pin 28): Channel 0,1 External Diode Temperature Sense. Connect to the anode of a diode connected PNP transistor and directly connect the cathode to SGND in order to sense remote temperature. If external temperature sense elements are not installed, short pin to ground and set the UT_FAULT_LIMIT to –275°C, IOUT_CAL_GAIN_TC set to zero and the UT_FAULT_RESPONSE to ignore.

GND (Exposed Pad Pin 41): Ground. Both the small-signal and compensation components should connect to this ground, which in turn connects to power ground at one point.

BLOCK DIAGRAM One of two channels (CH0) shown. (LTC3887 application only)

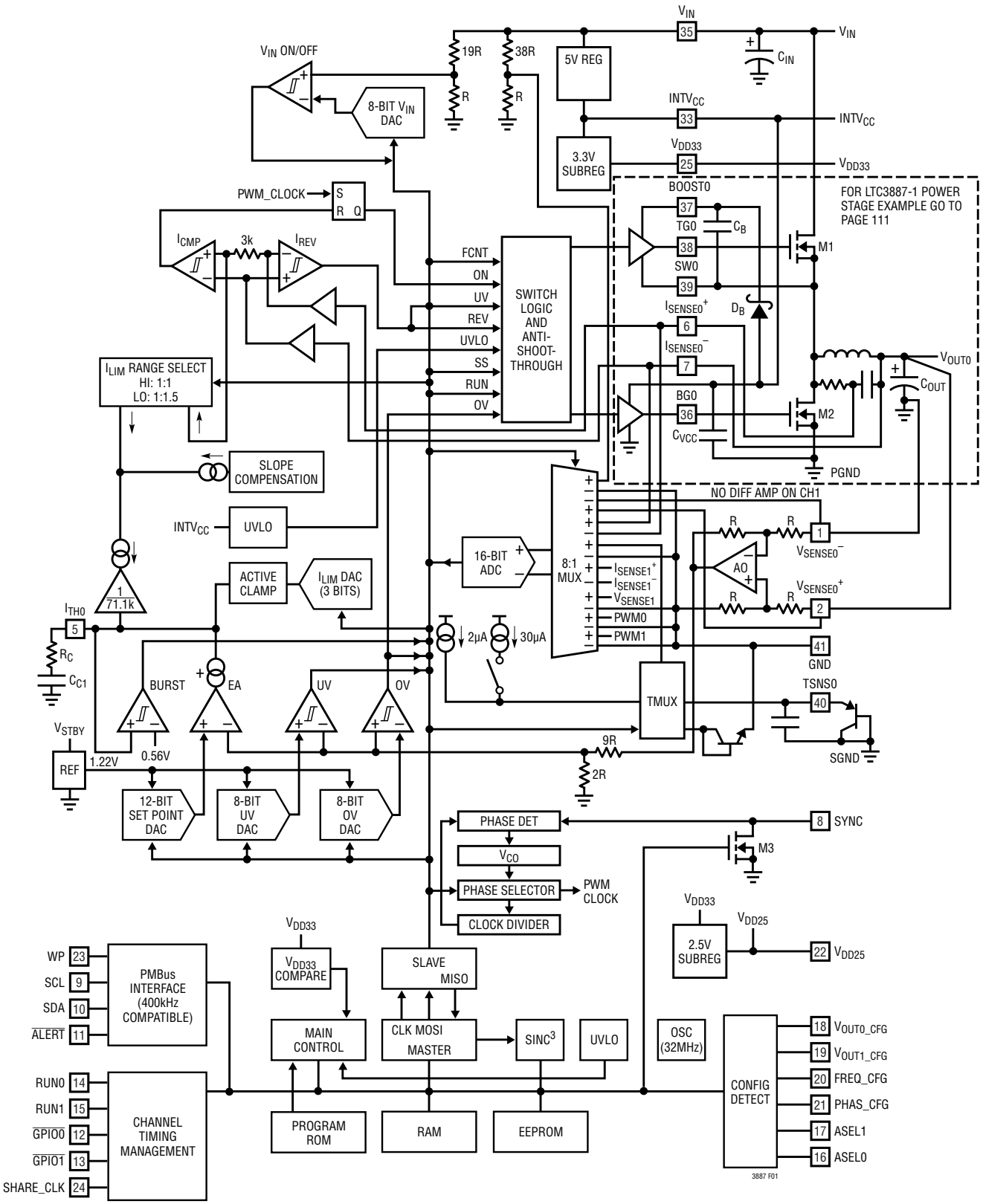


Figure 1. Block Diagram

OPERATION

OVERVIEW

The LTC3887/LTC3887-1 are a dual channel/dual phase, constant frequency, analog current mode controller for DC/DC step-down applications with a digital interface. The LTC3887 is used in applications where the gate driver is required. The LTC3887-1 is used in applications where the gate driver is external, for example a DrMOS power stage. The LTC3887-1 allows the TG pin to three-state which is required to produce discontinuous operation in some gate driver DrMOS circuits. Discontinuous operation assures the inductor current remains positive and is required to start up into a prebiased load.

The LTC3887 is very similar in features to the LTC3880. The major improvements are as follows:

- T_{INIT} start-up time 70ms
- VOUT0/VOUT1 are both programmable up to 5.5 Volts
- PWM synchronization circuit, review Frequency and Phasing section for details
- MFR_ADC_CONTROL for fast ADC sampling of one parameter. See PMBus Command Details.
- PMBus compliant to version 1.2 which adds PAGE _PLUS and SMBALERT mask. See PMBus Command Details.
- Improved fault logging. See PMBus Command Details.
- Share EA for channel 0/1 for 2-phase operation
- Resistor configuration pins modified. There are two Address select pins, VOUTn_CONFIG, PHAS_CONFIG and FREQ_CONFIG. The VOUTn_TRIM pins were removed.

The LTC3887 digital interface is compatible with PMBus which supports bus speeds of up to 400kHz. A typical application circuit is shown on the first page of this data sheet.

Major features include:

- Programmable Output Voltage
- Programmable Input Voltage Comparator
- Programmable Current Limit
- Programmable Switching Frequency
- Programmable OV and UV Comparators
- Programmable On and Off Delay Times
- Programmable Output Rise/Fall Times
- Phase-Locked Loop for Synchronous, Polyphase Operation (2, 3, 4 or 6 Phases)
- Input and Output Voltage/Current, Temperature and Duty Cycle Telemetry
- Fully Differential Load Sense
- Integrated Gate Drivers (LTC3887)
- Non-Volatile Configuration Memory
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time-Base Interconnect for Synchronization Between Multiple Controllers
- Fault Logging
- WP Pin to Protect Internal Configuration
- Standalone Operation After User Factory Configuration
- PMBus, 400kHz Compliant Interface

The PMBus interface provides access to important power management data during system operation including:

- Internal Die Temperature
- External System Temperature via Optional Diode Sense Elements
- Average Output Current
- Average PWM Duty Cycle
- Average Output Voltage
- Average Input Voltage
- Average Input Current
- Configurable, Latched and Unlatched Individual Fault and Warning Status

Individual channels are accessed through the PMBus using the PAGE command, i.e., PAGE 0 or 1.

OPERATION

Fault reporting and shutdown behavior are fully configurable. Two individual $\overline{GPIO}$ outputs are provided ($\overline{GPIO0}$, $\overline{GPIO1}$), both of which can be masked independently. A dedicated pin for $\overline{ALERT}$ is provided. The shutdown operation also allows all faults to be individually masked and can be operated in either unlatched (hiccup) or latched modes.

Individual status commands enable fault reporting over the serial bus to identify the specific fault event. Fault or warning detection includes the following:

- Output Undervoltage/Overvoltage
- Input Undervoltage/Overvoltage
- Input and Output Overcurrent
- Internal Overtemperature
- External Overtemperature
- Communication, Memory or Logic (CML) Fault

MAIN CONTROL LOOP

The LTC3887 is a constant frequency, current mode step-down controller containing two channels operating with various user-defined relative phasing. During normal operation each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin which is the output of each error amplifier, EA. The EA negative terminal is equal to the V_{SENSE} voltage divided by 5.5 (2.75 if range = 1). The positive terminal of the EA is connected to the output of a 12-bit DAC with values ranging from 0V to 1.024V. The output voltage, through feedback of the EA, will be regulated to 5.5 times the DAC output (2.75 times if range = 1). The DAC value is calculated by the part to synthesize the users desired output voltage. The output voltage is programmed by the user either with the resistor configuration pins detailed in Table 12 or by the V_{OUT} command (either from EEPROM or by PMBus command). Refer to the PMBus command section of the data sheet or the PMBus specification for more details. The output voltage can be modified by the user at any time with a PMBus VOUT_COMMAND. This command will typically have a latency less than 10ms. The user is encouraged to reference the PMBus Power System Management Protocol Specification to understand how to program the LTC3887. This specification can be found at http://www.pmbus.org/specs.html.

Continuing the basic operation description, the current mode controller will turn off the top gate when the peak current is reached. If the load current increases, V_{SENSE} will slightly droop with respect to the DAC reference. This causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on. In continuous conduction mode, the bottom MOSFET stays on until the end of the switching cycle.

EEPROM (NVM)

The LTC3887 contains internal EEPROM or NVM (non-volatile memory) to store configuration settings and fault log information. EEPROM endurance retention and mass write operation time are specified in the Electrical Characteristics and Absolute Maximum Ratings sections. Write operations above T_J = 85°C are possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded. Read operations performed at temperatures between –40°C and 125°C will not degrade the EEPROM. Writing to the EEPROM above 85°C will result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 85°C, the slight degradation in the data retention characteristics of the fault log will not take away from the usefulness of the function.

It is recommended that the EEPROM not be written when the die temperature is greater than 85°C. If the die temperature exceeds 130°C, the LTC3887 will disable all EEPROM write operations. All EEPROM write operations will be re-enabled when the die temperature drops below 125°C. (The controller will also disable when the die temperature exceeds the internal overtemperature fault limit 160°C with a 10°C hysteresis)

OPERATION

The degradation in EEPROM retention for temperatures >125°C can be approximated by calculating the dimensionless acceleration factor using the following equation:

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

K = $8.617 \bullet 10^{-5}$ eV/°K

T_{USE} = 125°C specified junction temperature

T_{STRESS} = actual junction temperature in °C

Example: Calculate the effect on retention when operating at a junction temperature of 135°C for 10 hours.

T_{STRESS} = 130°C

T_{USE} = 125°C

$AF = e^{[(1.4/8.617 \bullet 10^{-5}) \bullet (1/398 - 1/403)]} = 1.66$

The equivalent operating time at 125°C = 16.6 hours.

Thus the overall retention of the EEPROM was degraded by 6.6 hours as a result of operating at a junction temperature of 130°C for 10 hours. The effect of the overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a maximum junction temperature of 125°C.

The integrity of the EEPROM is checked with a CRC calculation each time its data is read, such as after a power-on reset or execution of a RESTORE_USER_ALL command. If CRC error occurs, the MFR bit is set in the STATUS_BYTE and STATUS_WORD commands. The NVM CRC error bit in the STATUS_MFR_SPECIFIC command is set and the $\overline{\text{ALERT}}$ and RUN pins are pulled low disabling the output as a safety measure. The device will only respond at special address 0x7C or global addresses 0x5A and 0x5B.

POWER UP AND INITIALIZATION

The LTC3887 is designed to provide standalone supply sequencing and controlled turn-on and turn-off operation. It operates from a single input supply (4.5V to 24V) while three on-chip linear regulators generate internal 2.5V, 3.3V and 5V. If V_{IN} does not exceed 6V, the $INTV_{CC}$ and V_{IN} pins must be tied together. The controller configuration is initialized by an internal threshold based UVLO where V_{IN} must be approximately 4V and the 5V, 3.3V and 2.5V linear regulators must be within approximately 20% of the regulated values.

During initialization, the external configuration resistors are identified and/or contents of the EEPROM are read into the controller's commands. The $\overline{\text{GPIO}}n$ pins are in high impedance (Hi-Z) mode. The TG*n*, BG*n* and RUN*n* pins are held low. (The LTC3887-1 PWM pins are three-state.) The LTC3887 will use the contents of Tables 12 to 15 to determine the resistor defined parameters. See the Resistor Configuration section for more detail. The resistor configuration pins only control some of the preset values of the controller. The remaining values are programmed in EEPROM either at the factory or by the user.

If the configuration resistors are not inserted or if the ignore RCONFIG bit is asserted (bit 6 of the MFR_CONFIG_ALL_LTC3887 configuration command), the LTC3887 will use only the contents of EEPROM to determine the DC/DC characteristics. The ASEL0 and 1 values read at power-up or reset or after a RESTORE_USER _ALL command are always respected unless the pins are open. See the Applications Information section for more detail.

After the part has initialized, an additional comparator monitors V_{IN}. The VIN_ON threshold must be exceeded before the output power sequencing can begin. After V_{IN} is initially applied, the part will typically require 70ms to initialize and begin the TON_DELAY timer. The readback of voltages and currents require an additional 200ms to 300ms.

SOFT-START

The part must enter the run state prior to soft-start. The run pins are released by the LTC3887 after the part initializes and V_{IN} is greater than the VIN_ON threshold. If multiple LTC3887s are used in an application, they all hold their respective run pins low until all devices initialize and V_{IN} exceeds the VIN_ON threshold for every device. The SHARE_CLK pin assures all the devices connected to the signal use the same time base. The SHARE_CLK pin is

OPERATION

held low until the part has initialized after V_{IN} is applied and V_{IN} exceeds the VIN_ON threshold. The LTC3887 can be set to turn off (or remain off) if SHARE_CLK is low (set bit 2 of MFR_CHAN_CONFIG_LTC3887 to a 1). This allows the user to assure synchronization across numerous LTC ICs even if the RUN pins can not be connected together due to board constraints. In general, if the user cares about synchronization between chips it is best to connect all the respective RUN pins together and to connect all the respective SHARE_CLK pins together. This assures all chips begin sequencing at the same time and use the same time base.

After the RUN pin releases and prior to entering a constant output voltage regulation state, the LTC3887 performs a monotonic initial ramp or "soft-start". Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set-point. Once the LTC3887 is commanded to turn on, (after power up and initialization) the controller waits for the user specified turn-on delay (TON_DELAY) prior to initiating this output voltage ramp. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting the value of TON_RISE to any value less than 0.25ms. The LTC3887 PWM always uses discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom gate is turned off as soon as reverse current is detected in the inductor. In the LTC3887-1 this causes the TG pin to three-state. This will allow the regulator to start up into a prebiased load. When the TON_MAX_FAULT_LIMIT is reached, the part transitions to continuous mode, if so programmed. If TON_MAX_FAULT_LIMIT is set to zero, there is no time limit and the part transitions to the desired conduction mode after TON_RISE completes and V_{OUT} has exceeded the VOUT_UV_FAULT_LIMIT and IOUT_OC is not present. Setting TON_MAX_FAULT_LIMIT to a value of 0 is not recommended. This described method of start-up sequencing is time based.

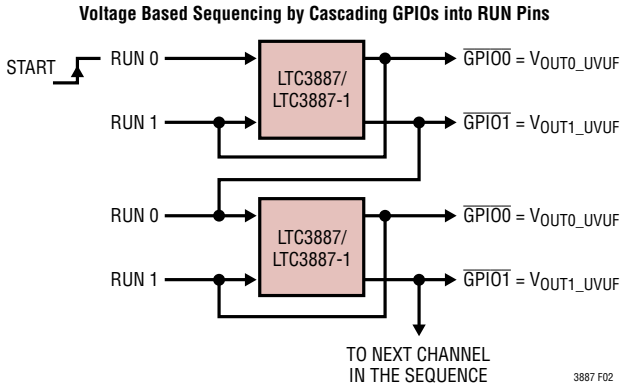


Figure 2. Event (Voltage) Based Sequencing

SEQUENCING

The default mode for sequencing the outputs on and off is time based. Each output is enabled after waiting TON_DELAY amount of time following either a RUN pin going high, a PMBus command to turn on or the V_{IN} rising above a preprogrammed voltage. Off sequencing is handled in a similar way. To assure proper sequencing, make sure all ICs connect the SHARE_CLK pin together and RUN pins together. If the RUN pins can not be connected together for some reason, set bit 2 of MFR_CHAN_CONFIG_LTC3887 to a 1. This bit requires the SHARE_CLK pin to be clocking before the power supply output can start. When the RUN pin is pulled low, the LTC3887 will hold the pin low for the MFR_RESTART_DELAY. The minimum MFR_RESTART_DELAY is TOFF_DELAY + TOFF_FALL + 136ms. This delay assures proper sequencing of all rails. The LTC3887 calculates this delay internally and will not process a shorter delay. However, a longer commanded MFR_RESTART_DELAY will be used by the part. The maximum allowed value is 65.52 seconds.

EVENT-BASED SEQUENCING

The $\overline{GPIO}n$ pins can be asserted when the UV threshold is exceeded for each output. It is possible to feed the $\overline{GPIO}$ pin from one output into the RUN pin of the next output in the sequence. To use the $\overline{GPIO}n$ pin for voltage based sequencing, set bit 12 of the MFR_GPIO*n*_PROPAGATE command = 1. Bit 12 is the VOUT_UVUF which is the unfiltered VOUT_UV comparator. Using the unfiltered VOUT_UV fault limit is recommended because there is little appreciable time delay between the comparator crossing the UV threshold and the $\overline{GPIO}$ pin releasing This can be implemented across multiple LTC3887s. The VOUT_UVUF has a 250µs filter. If the V_{OUT} voltage bounces around the

OPERATION

UV threshold for a long period of time it is possible for the $\overline{GPIO}$ output to toggle more than once. To minimize this problem, set the TON_RISE time under 100ms. If a fault in the string of rails is detected, only the faulted rail and downstream rails will fault off. The rails in the string of devices in front of the faulted rail will remain on unless commanded off.

SHUTDOWN

The LTC3887 supports two shutdown modes. The first mode is closed-loop shutdown response, with user-defined turn-off delay (TOFF_DELAY) and ramp down rate (TOFF_FALL). The controller will maintain the mode of operation for TOFF_FALL. In discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current.

The other shutdown mode occurs in response to a fault condition or loss of SHARE_CLK (if bit 2 of MFR_CHAN_CONFIG_LTC3887 is set to a 1) or V_{IN} falling below the VIN_OFF threshold or $\overline{GPIO}$ pulled low externally (if the MFR_GPIO_RESPONSE is set to inhibit). Under these conditions the power stage is disabled in order to stop the transfer of energy to the load as quickly as possible. The shutdown state can be entered from the soft-start or active regulation states either through user intervention (deasserting RUN*n* or the PMBus OPERATION command) or in response to a detected fault or an external fault via the bidirectional $\overline{GPIO}$*n* pins, or loss of SHARE_CLK (if bit 2 of MFR_CHAN_CONFIG_LTC3887 is set to a 1) or V_{IN} falling below the VIN_OFF threshold.

In hiccup mode, the controller responds to a fault by shutting down and entering the inactive state for a programmable delay time (MFR_RETRY_DELAY). This delay minimizes the duty cycle associated with autonomous retries if the fault that caused the shutdown disappears once the output is disabled. The retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If multiple outputs are controlled by the same $\overline{GPIO}$ pin, the decay time of the faulted output determines the retry delay. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG_LTC3887. Alternatively, the controller can be configured so that it remains latched-off following a fault and clearing requires user intervention such as toggling RUN*n* or commanding the part OFF then ON.

LIGHT LOAD CURRENT OPERATION

The LTC3887 has two modes of operation including discontinuous conduction mode and forced continuous conduction mode. Mode selection is done using the MFR_PWM_MODE_LTC3887 command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

If a controller is enabled for discontinuous operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom gate external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. The LTC3887-1 three-states the TG pin to accomplish the same result. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in discontinuous mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry. Forced continuous conduction mode may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this and turn off the offending channel. However, this fault is based on an ADC read and can take up to 120ms to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction operation.

If the part is set to discontinuous mode operation, as the inductor average current increases, the controller will automatically modify the operation from discontinuous mode to continuous mode.

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SWITCHING FREQUENCY AND PHASE

The switching frequency of the LTC3887's controller can be established with internal clock references or with an external time-base. The LTC3887 can be configured for an external clock input through the programmed value in EEPROM, a PMBus command or setting the SYNC output to disable with the PHAS_CFG pin. The MFR_PWM_CONFIG_LTC3887 command determines the relative phasing. The rails should be selected to be out of phase with each other. Both RUN pins must be low or both channels commanded off before the FREQUENCY and MFR_PWM_CONFIG_LTC3887 commands can be written to the LTC3887. The relative phasing of all devices in a PolyPhase rail should be optimally phased. The relative phasing of each rail is 360/n where n is the number of phases in the rail.

The LTC3887 will automatically accept an external SYNC input, disabling its own SYNC output if necessary, as long as the external clock frequency is greater than 1/2 of the internal PWM clock. Whether configured to drive SYNC output or not, the LTC3887 can continue PWM operation using its own internal oscillator if an external clock signal is subsequently lost.

If the LTC3887 is configured as the oscillator output on SYNC, SYNC ENABLED, the switching frequency source can be selected with either external configuration resistors or through serial bus programming. The FREQ_CFG configuration resistor pin can be used to select the FREQUENCY_SWITCH. The PHAS_CFG pin can be used to set the MFR_PWM_CONFIG_LTC3887 and enable the SYNC output to produce the output frequency as outlined in Tables 13 and 14. Otherwise, the FREQUENCY_SWITCH and MFR_PWM_CONFIG_LTC3887 PMBus commands can be used to select PWM switching frequency and the PWM channel phase relationship. The phase and frequency relationships are completely independent of each other providing the numerous application options for the user.

If the LTC3887 is configured to drive the SYNC output by setting bit 4 of MFR_CONFIG_ALL_LTC3887 to a 0 the SYNC pin will pull low at the desired clock rate, set with the FREQUENCY_SWITCH command, with 500ns low pulse. Care must be taken in the application to assure the capacitance on SYNC is minimized to assure the pull-up resistor versus the capacitor load has a low enough time constant for the application. In addition, a phase-locked loop (PLL) is available to synchronize the internal oscillator to an external clock source that is connected to the SYNC pin. All phase relationships are between the falling edge of SYNC and the rising edge of the LTC3887 TG outputs. Multiple LTC3887s can be synchronized in order to realize PolyPhase arrays.

OUTPUT VOLTAGE SENSING

The channel 0 differential amplifier allows remote, differential sensing of the load voltage with $V_{SENSE0n}$ pins. The channel 1 sense pin (V_{SENSE1}) is referenced to GND. The telemetry ADC is fully differential and makes measurements of channels 0 and 1 output voltages at the $V_{SENSE0n}$ and V_{SENSE1}/GND pins, respectively. The maximum allowed sense voltage is 5.5V.

CURRENT SENSING

For DCR current sense applications, a resistor in series with a capacitor is placed across the inductor. In this configuration, the resistor is tied to the FET side of the inductor while the capacitor is tied to the load side of the inductor as shown in Figure 3. If the RC values are chosen such that the RC time constant matches the inductor time constant (L/DCR, where DCR is the inductor series resistance), the resultant voltage appearing across the capacitor will equal the voltage across the inductor series resistance (V_{DCR}) and thus represent the current flowing through the inductor. The RC calculations are based on the room temperature DCR of the inductor.

The RC time constant should remain constant, as a function of temperature. This assures the transient response of the circuit is the same regardless of the temperature. The DCR of the inductor has a large temperature coefficient, approximately 3900ppm/°C. The temperature coefficient of the inductor must be written to the MFR_IOUT_CAL_GAIN_TC register. The external temperature is sensed near the inductor and used to modify the internal current limit circuit to maintain an essentially constant current limit with temperature. In this application, the I_{SENSEn}^+ pin is connected to the power stage side of the capacitor while

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the I_{SENSEn}^- pin is placed on the load side of the capacitor. The current sensed from the input is then given by the expression V_{DCR}/DCR. V_{DCR} is digitized by the LTC3887's telemetry ADC with an input range of ±128mV, a noise floor of $7\mu V_{RMS}$, and a peak-peak noise of approximately 46.5µV. The LTC3887 computes the inductor current using the DCR value stored in the IOUT_CAL_GAIN command and the temperature coefficient stored in command MFR_IOUT_CAL_GAIN_TC. The resulting current value is returned by the READ_IOUT command.

POLYPHASE LOAD SHARING

Multiple LTC3887's can be arrayed in order to provide a balanced load-share solution by bussing the necessary pins. Figure 3 illustrates the shared connections required for load sharing.

If an external oscillator is not provided, the SYNC output should only be enabled on one of the LTC3887s. The other(s) should be programmed to disable the SYNC output using bit 4 of MFR_CONFIG_ALL_LTC3887. Set the oscillator to the desired PWM frequency in both chips. If an external oscillator is present, the chip with the SYNC output enabled will detect the presence of the external clock and stop driving the SYNC output.

The error amp of two PWM controls on the same chip can be shared by asserting bit 7 of MFR_PWM_CONFIG_LTC3887. Both error amps remain in the circuit so the loop gain does not change. Do not assert this bit unless both V_{OUT} pins are connected together and both ITH pins are tied together in the application. This allows remote differential voltage sensing for PolyPhase rails.

EXTERNAL/INTERNAL TEMPERATURE SENSE

External temperature can be best measured using a remote diode-connected PNP transistor such as the MMBT3906. The emitter should be connected to the TSNS*n* pin while

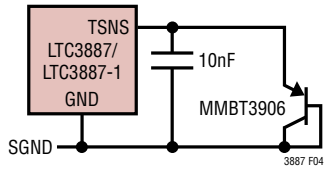

Figure 4. Temperature Sense Circuit

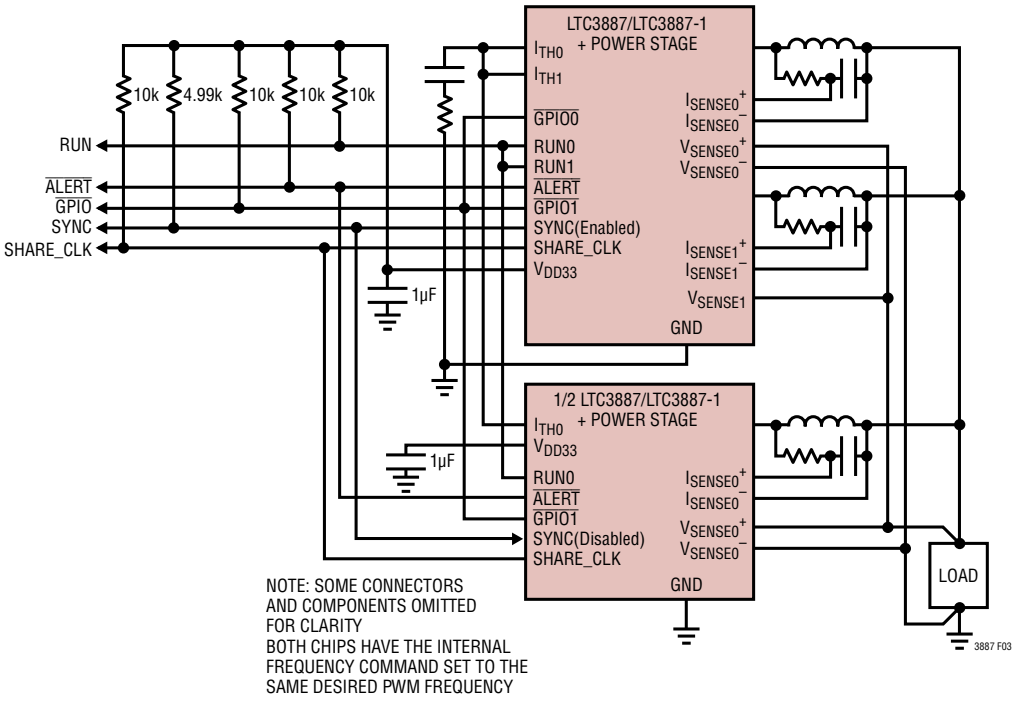

Figure 3. Load Sharing Connections for 3-Phase Operation

OPERATION

the base and collector terminals of the PNP transistor must be connected and returned directly to the LTC3887's GND pin. Place the PNP in close proximity to the inductor to accurately measure the inductor temperature. For best noise immunity, the connections should be routed differentially and a 10nF capacitor should be placed in parallel with the diode connected PNP. Two different currents are applied to the diode (nominally 2µA and 32µA) and the temperature is calculated from the ΔV_{BE} measurement. The external transistor temperature is digitized by the telemetry ADC, and the value is returned by the PMBus READ_TEMPERATURE_1 (Ch*n*) command.

The READ_TEMPERATURE_2 command returns the junction temperature of the LTC3887 using an on-chip diode. The slope of the external temperature sensor can be modified with the temperature slope coefficient stored in MFR_TEMP_1_GAIN. Typical PNPs require temperature slope adjustments slightly less than 1. The MMBT3906 has a recommended value in this command of approximately MFR_TEMP_1_GAIN = 0.991 based on the ideality factor of 1.01. Simply invert the ideality factor to calculate the MFR_TEMP_1_GAIN. Different manufacturers and different lots may have different ideality factors. Consult with the manufacturer to set this value.

The offset of the external temperature sense can be adjusted by MFR_TEMP_1_OFFSET. A value of 0 in this register sets the temperature offset to –273.15°C.

If the PNP cannot be placed in direct contact with the inductor, the slope or offset can be increased to account for temperature mismatches. If the user is adjusting the slope, the intercept point is at absolute zero, –273.15°C, so small adjustments in slope can change the apparent measured temperature significantly. Another way to artificially increase the slope of the temperature term is to increase the MFR_IOUT_CAL_GAIN_TC term. This will modify the temperature slope with respect to room temperature.

RCONFIG (RESISTOR CONFIGURATION) PINS

There are six input pins utilizing 1% resistor dividers between V_{DD25} and GND to select key operating parameters. The pins are ASEL0, ASEL1, FREQ_CFG, V_{OUT0_CFG}, V_{OUT1_CFG}, PHAS_CFG. If pins are floated, the value stored in the corresponding EEPROM command is used. If bit 6 of the MFR_CONFIG_ALL_LTC3887 configuration command is asserted in EEPROM, the resistor inputs are ignored upon power-up except for ASEL0 and ASEL1 which are always respected. The resistor configuration pins are only measured during a power-up reset, after an MFR_RESET or after a RESTORE_USER_ALL command is executed.

The V_{OUTn_CFG} pin settings are described in Table 12. These pins select the output voltages for the LTC3887's analog PWM controllers. If the pin is open, the VOUT_COMMAND command is loaded from EEPROM to determine the output voltage. The default factory EEPROM setting is to have the switcher off unless the voltage configuration pins are installed. The user may reprogram the EEPROM to the desired setting for the application. When the EEPROM configuration is loaded, it is recommended the user assert bit 6 of MFR_CONFIG_ALL_LTC3887 to disable the resistor configuration pins for all subsequent reset operations.

The following parameters are set as a percentage of the output voltage if the RCONFIG pins are used to determined output voltage:

- VOUT_OV_FAULT_LIMIT..... +10%
- VOUT_OV_WARN..... +7.5%
- VOUT_MAX..... +7.5%
- VOUT_MARGIN_HIGH .....+5%%
- VOUT_MARGIN_LOW.....–5%
- VOUT_UV_WARN.....–6.5%
- VOUT_UV_FAULT_LIMIT.....–7%

The FREQ_CFG pin settings are described in Table 14. This pin selects the switching frequency. The phase relationships between the two channels and SYNC pin is determined by the PHAS_CFG pin described in Table 13. To synchronize to an external clock, the part should be put into external clock mode (SYNC output disabled but frequency set to the nominal value). If no external clock is supplied, the part will clock at the programmed frequency. If the application is multi-phase and the SYNC signal between chips is lost, the parts will not be at the same frequency increasing the ripple voltage on the output, possibly producing undesirable operation. If the SYNC signal is being generated internally and SYNC output enabled is not selected, bit 10 of MFR_PADS_LTC3887 will be asserted. If no frequency is selected and the external SYNC frequency is not present, a PLL_FAULT will occur. If the user does not wish to

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see the $\overline{\text{ALERT}}$ from a PLL_FAULT even if there is not a valid synchronization signal at power-up, the $\overline{\text{ALERT}}$ mask for PLL_FAULT must be written. See the description on SMBALERT_MASK for more details. If the SYNC pin is connected between multiple ICs only one of the ICs should should have the SYNC output enabled, all other ICs should be configured to SYNC output disabled.

The ASEL0 and 1 pin settings are described in Table 15. ASLE1 selects the top three bits of the slave address for the LTC3887. If ASEL1 is floating, the three most significant bits are retrieved from the EEPROM MFR_ADDRESS command. ASEL0 selects the bottom four bits of the slave address for the LTC3887. If ASEL0 is floating, the four LSB bits stored in EEPROM MFR_ADDRESS command are used to determine the four LSB bits of the slave address. For more detail, refer to Table 15.

Note: Per the PMBus specification, pin programmed parameters can be overridden by commands from the digital interface with the exception of ASEL0 and ASEL1 which are always honored. Do not set any part address to 0x0C, 0x5A, 0x5B or 0x7C because these are global addresses and all LTC PMBus parts may respond to them.

FAULT DETECTION AND HANDLING

A variety of fault and warning reporting and handling mechanisms are available. Fault and warning detection capabilities include:

- Input OV/FAULT Protection and UV Warning
- Average Input OC Warn
- Output OV/UV Fault and Warn Protection
- Output OC Fault and Warn Protection
- Internal and External Overtemperature Fault and Warn Protection
- External Undertemperature Fault Protection
- CML Fault (Communication, Memory or Logic)
- External Fault Detection via the Bidirectional $\overline{\text{GPIO}}n$ Pins.

In addition, the LTC3887 can map any combination of fault indicators to their respective $\overline{\text{GPIO}}n$ pin using the propagate $\overline{\text{GPIO}}n$ response commands, MFR_GPIO_PROPAGATE_LTC3887. Typical usage of a $\overline{\text{GPIO}}$ pin is as a driver for an external crowbar device, overtemperature alert, overvoltage alert or as an interrupt to cause a microcontroller to poll the fault commands. Alternatively, the $\overline{\text{GPIO}}n$ pins can be used as inputs to detect external faults downstream of the controller that require an immediate response. The $\overline{\text{GPIO0}}$ and/or $\overline{\text{GPIO1}}$ pins can also be configured as power good outputs. Power good indicates the controller output is within the OV/UV fault thresholds. At power-up the pin will initially be three-state. If it is necessary to have the desired polarity on the pin at power-up in this configuration, attach a Schottky diode between the RUN pin of the propagated power good signal and the $\overline{\text{GPIO}}$ pin. The Cathode must be attached to RUN and the Anode to the $\overline{\text{GPIO}}$ pin. If the $\overline{\text{GPIO}}$ pin is set to a power good status, the MFR_GPIO_RESPONSE must be ignore otherwise a latched off condition exists.

As described in the Soft-Start section, it is possible to control start-up through concatenated events. If $\overline{\text{GPIO}}n$ is used to drive the RUN pin of another controller, the unfiltered VOUT_UV fault limit should be mapped to the $\overline{\text{GPIO}}$ pin.

Any fault or warning event will cause the $\overline{\text{ALERT}}$ pin to assert low unless the $\overline{\text{ALERT}}$ is masked by the SMBALERT_MASK command. The pin will remain asserted low until the CLEAR_FAULTS command is issued, the fault bit is written to a 1, the PMBus master successfully reads the device ARA register, bias power is cycled a MFR_RESET or RESTORE_USER_ALL command is issued. Channel specific faults are cleared if the RUN pins are toggled OFF/ON or the part is commanded OFF/ON via PMBus. If bit 0 of MFR_CONFIG_ALL_LTC3887 is set to a 1, toggling the RUN pins OFF/ON or commanding the part OFF/ON via PMBus clears all faults. The MFR_GPIO_PROPAGATE_LTC3887 command determines if the $\overline{\text{GPIO}}$ pins are pulled low when a fault is detected; however, the $\overline{\text{ALERT}}$ pin is always pulled low if a fault or warning is detected and the status bits are updated unless the $\overline{\text{ALERT}}$ pin is masked using the SMBALERT_MASK command.

Output and input fault event handling is controlled by the corresponding fault response byte as specified in Tables 5 to 9. Shutdown recovery from these types of faults can either be autonomous or latched. For autonomous re-

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covery, the faults are not latched, so if the fault condition is not present after the retry interval has elapsed, a new soft-start is attempted. If the fault persists, the controller will continue to retry. The retry interval is specified by the MFR_RETRY_DELAY command and prevents damage to the regulator components by repetitive power cycling. The MFR_RETRY_DELAY must be greater than 120ms. It can not exceed 83.88 seconds.

Channel-to-channel fault dependencies can be created by connecting $\overline{\text{GPIO}}n$ pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed $\overline{\text{GPIO}}n$ pins low. The other channels are then configured to shut down when the $\overline{\text{GPIO}}n$ pins are pulled low. For autonomous group retry, the faulted channel is configured to release the $\overline{\text{GPIO}}n$ pin(s) after a retry interval, assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence. If the fault response is LATCH_OFF, the $\overline{\text{GPIO}}$ pin remains asserted low until either the RUN pin is toggled OFF/ON or the part is commanded OFF/ON. The toggling of the RUN either by the pin or OFF/ON command will clear faults associated with the channel. If it is desired to have all faults cleared when either RUN pin is toggled, set bit 0 of MFR_CONFIG_ALL_LTC3887 to a 1.

The status of all faults and warnings is summarized in the STATUS_WORD and STATUS_BYTE commands.

Additional fault detection and handling capabilities are:

CRC Protection

The integrity of the EEPROM memory is checked after a power-on reset. A CRC error will prevent the controller from leaving the OFF state. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$ pin will be pulled low. EEPROM repair can be attempted by writing the desired configuration to the controller and executing a STORE_USER_ALL command followed by a CLEAR_FAULTS command.

The LTC3887 manufacturing section of the EEPROM is mirrored. The LTC3887 has the ability to operate if either one of the two sections of the manufacturing section of the EEPROM configuration becomes corrupted. If a discrepancy is detected, the “NVM CRC Fault” in the STATUS_MFR_SPECIFIC command is set. If this bit remains set after being cleared by issuing a CLEAR_FAULTS or writing a 1 to this bit, an irrecoverable internal fault has occurred. There are no provisions for field repairing unrecoverable EEPROM faults in the manufacturing section.

SERIAL INTERFACE

The LTC3887 serial interface is a PMBus compliant slave device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using either the EEPROM or an external resistor divider. In addition the LTC3887 always responds to the global broadcast address of 0x5A (7 bit) or 0x5B (7 bit). Address 0x5A is not paged and is performed on both channels. 0x5B respects the page command. Because address 0x5A does not support page, it can not be used for any paged reading commands.

The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte, 6) read word and 7) read block 8) PAGE_PLUS_READ, 9) PAGE_PLUS_WRITE 10) SMBALERT_MASK read, 11) SMBALERT_MASK write. All read operations will return a valid PEC if the PMBus master requests it. If the PEC_REQUIRED bit is set in the MFR_CONFIG_ALL_LTC3887 command, the PMBus write operations will not be acted upon until a valid PEC has been received by the LTC3887.

Communication Protection

PEC write errors (if PEC_REQUIRED is active), attempts to access unsupported commands, or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_CML command, and the $\overline{\text{ALERT}}$ pin is pulled low.

DEVICE ADDRESSING

The LTC3887 offers four different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

OPERATION

Global addressing provides a means of the PMBus master to address all LTC3887 devices on the bus. The LTC3887 global address is fixed 0x5A (7 bit) or 0xB4 (8 bit) and cannot be disabled. Commands sent to the global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global command 0x5B (7 bit) or 0xB6 (8 bit) is paged and allows channel specific command of all LTC3887 devices on the bus. Other LTC device types may respond at one or both of these global addresses; therefore do not read from global addresses.

Rail addressing provides a means for the bus master to simultaneously communicate with all channels connected together to produce a single output voltage (PolyPhase). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Do not read from rail addresses because multiple LTC devices may respond.

Device addressing provides the standard means of the PMBus master communicating with a single instance of an LTC3887. The value of the device address is set by a combination of the ASEL0 and ASEL1 configuration pins and the MFR_ADDRESS command. When this addressing means is used, the PAGE command determines the channel being acted upon. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts. Communication to LTC3887 devices at global and rail addresses should be limited to command write operations.

RESPONSES TO V_{OUT} AND I_{OUT} FAULTS

V_{OUT} OV and UV conditions are monitored by comparators. The OV and UV limits are set in three ways.

- As a Percentage of the V_{OUT} if Using the Resistor Configuration Pins
- In EEPROM if Either Programmed at the Factory or Through the GUI
- By PMBus Command

The I_{IN} and I_{OUT} overcurrent monitors are performed by ADC readings and calculations. Thus these values are based on average currents and can have a time latency of up to 120ms. The I_{OUT} calculation accounts for the sense resistor and the temperature coefficient of the resistor. The input current is equal to the sum of output current times the respective channel duty cycle plus the input offset current for each channel. If this calculated input current exceeds the IN_OC_WARN_LIMIT the $\overline{\text{ALERT}}$ pin is pulled low and the IIN_OC_WARN bit is asserted in the STATUS_INPUT register.

The LTC3887 provides the ability to ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). The retry interval is set in MFR_RETRY_DELAY and can be from 120ms to 83.88 seconds in 1ms increments. The shutdown for OV/UV and OC can be done immediately or after a user selectable deglitch time.

Output Overvoltage Fault Response

A programmable overvoltage comparator (OV) guards against transient overshoots as well as long-term overvoltages at the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared *regardless of the PMBus VOUT_OV_FAULT_RESPONSE command byte value.* This hardware level fault response delay is typically 2µs from the overvoltage condition to BG asserted high. Using the VOUT_OV_FAULT_RESPONSE command, the user can select any of the following behaviors:

- OV Pull-Down Only (OV cannot be ignored)
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely using the Time Interval Specified in MFR_RETRY_DELAY

Either the Latch Off or Retry fault responses can be deglitched in increments of (0 to 7) • 10µs. See Table 5.

Output Undervoltage Response

The response to an undervoltage comparator output can be either:

- Ignore