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Multichemistry Buck Battery Charger Controller with Digital Telemetry System

FEATURES

- **Multichemistry Li-Ion/Polymer, LiFePO$_4$, or Lead-Acid Battery Charger with Termination**
- **High Efficiency Synchronous Buck Battery Charger**
- **Digital Telemetry System Monitors V_{BAT}, I_{BAT}, R_{BAT},NTC Ratio (Battery Temperature), V_{IN}, I_{IN}, V_{SYSTEM}, Die Temperature**
- **Coulomb Counter and Integrated 14-Bit ADC**
- **Wide Charging Input Voltage Range: 4.5V to 35V**
- **Wide Battery Voltage Range: Up to 35V**
- **Input Undervoltage Charge Current Limit Loop**
- **Maximum Power Point Tracking**
- Optional I^{2}C Serial Port Control
- Input Current Limit Prioritizes System Load Output
- Input and Output Ideal Diodes Provide Low Loss PowerPath™ Operation
- Instant-On Operation with Discharged Battery

APPLICATIONS

- Portable Medical Instruments/Military Equipment
- Industrial Handhelds/Lighting
- Ruggedized Notebook/Tablet Computers

DESCRIPTION

The LTC®4015 is a complete synchronous buck controller/charger with pin-selectable, chemistry specific charging and termination algorithms.

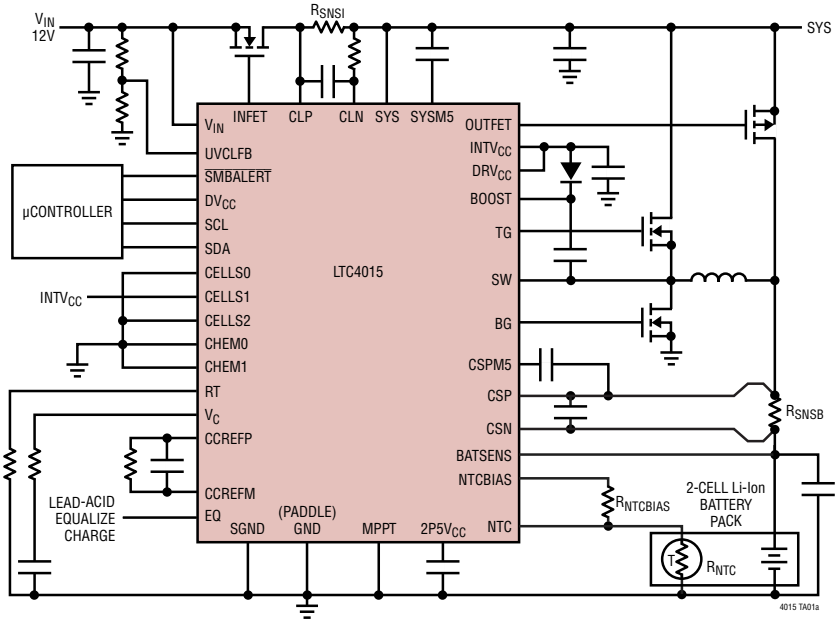
The LTC4015 can charge Li-Ion/Polymer, LiFePO$_4$, or lead-acid batteries. Battery charge voltage is pin selectable and I^{2}C adjustable. Input current limit and charge current can be accurately programmed with sense resistors and can be individually adjusted via the I^{2}C serial port. A digital telemetry system monitors all system power parameters.

Safety timer and current termination algorithms are supported for lithium chemistry batteries. The LTC4015 also includes automatic recharge, precharge (Li-Ion) and NTC thermistor protection. The LTC4015's I^{2}C port allows user customization of charger algorithms, reading of charger status information, configuration of the maskable and programmable alerts, plus use and configuration of the Coulomb counter.

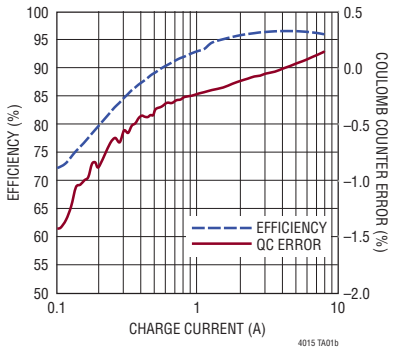
Available in a 38-Lead 5mm × 7mm QFN package.

TYPICAL APPLICATION

12V$_{IN}$ 2-Cell Li-Ion 8A Step-Down Battery Charger Controller



Step-Down Charger Efficiency and Coulomb Counter Error vs Battery Charge Current



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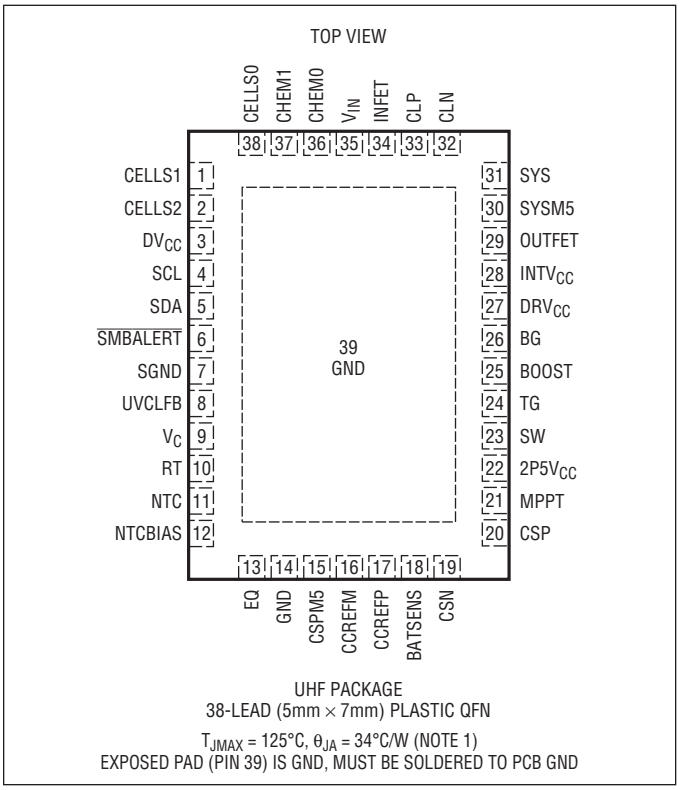
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 5)

V_{IN}, CSN..... –0.3V to 40V
BOOST to SW..... –0.3 to 5.5V
BATSENS to CSN, CSP to CSN, CLP to CLN, CLP, CLN to SYS.....±0.3V
DV_{CC}, DRV_{CC}..... –0.3V to 5.5V
CELLSO, CELLS1, CELLS2, CHEM0, CHEM1, MPPT, EQ.....–0.3V to $INTV_{CC}$
SDA, SCL, $\overline{SMBALERT}$..... –0.3V to DV_{CC}
I_{UVCLFB} (Note 4) .....±200µA
$INTV_{CC}$ Peak Output Current.....100mA
Operating Junction Temperature Range (Notes 2,3).....–40 to 125°C
Storage Temperature Range .....–65 to 150°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W (NOTE 1)
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB GND

ORDER INFORMATION

http://www.linear.com/product/LTC4015#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4015EUHF#PBF	LTC4015EUHF#TRPBF	4015	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC4015IUHF#PBF	LTC4015IUHF#TRPBF	4015	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

DATA SHEET CONVENTIONS

- $V_{PINNAME}$ and $I_{PINNAME}$ represents the voltage on a pin or the pin current; V_{EQ} = EQ Pin Voltage.
- Hexadecimal numbers are prefixed with 0x; 0x10 is a hexadecimal 10
- Register symbol names will be capitalized. Symbols within a register will be lower case;

  en_meas_sys_valid_alert is bit 15 in register EN_LIMIT_ALERTS (0x0D)

- $LiFePO_4$ is lithium iron phosphate, Li-Ion is used for both lithium-ion and lithium-ion polymer
- Lithium chemistries refers to $LiFePO_4$, lithium-ion, and lithium-ion polymer as a group.
- When a register name is used in square brackets, this means the 16 bit value associated with that register; For example [VBAT] is the 16 bit ADC measurement value of the per cell battery voltage.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2), DV_{CC} = 3.3V, UVCLFB = 1.5; CELLS1 = $INTV_{CC}$; EQ, MPPT, CELLS0, CELLS2, CHEM0, CHEM1 = 0; RT = 95.3k; R_{CCREF} = 301k, $R_{NTCBIAS}$ = R_{NTC} = 10k; BATSENS = CSN = CSP; DRV_{CC} = $INTV_{CC}$; SYS = CLP = CLN. Conditions: Charging; V_{IN} = 12V, SYS = 12V, BATSENS = 7.4V .....Battery Only; V_{IN} = 0V, SYS = 8.4V, BATSENS = 8.4V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Voltage Range	Note 8	●	3.1		35	V
V_{BAT}	Battery Voltage Range	Note 8	●			35	V
$V_{CHARGE(TOL)}$	Charge Voltage, Regulated Battery per Cell Tolerance, All Chemistries	Li-Ion ,4.2V per Cell; $LiFePO_4$ 3.6V per Cell; Lead-Acid 2.2V per Cell	●	–1.25		1.25	%
	Regulated Battery Charge Current Tolerance	Full-Scale $V_{CSP–CSN}/R_{SNSB}$	●	–2.0		2.0	%
V_{SYS}	SYS Pin Voltage	Note 8	●	3.05		35	V
Quiescent Current $I_Q = I_{VIN} + I_{CLP} + I_{CLN} + I_{SYS} + I_{SW} + I_{CSP} + I_{CSN} + I_{BATSENS}$							
	Battery Discharge Current (No Input Supply, Coulomb Counter Disabled)	Battery Only, Telemetry Inactive	●		112	325	µA
		Battery Only, Telemetry Active 1% Duty Cycle	●		140	364	µA
		Battery Only, Telemetry Active Continuously			2.84		mA
	I_Q, Charging	Charging, Switcher Suspended			3.00		mA
		Charging, $V_{BAT} > V_{CHARGE}$ (Note 7)			4.10		mA
	I_Q, Ship Mode	Ship Mode (V_{IN} = 0)	●		5	40	µA
I_{Vin}	V_{IN} Pin Current	Battery Only (No Input Supply)		–200		200	nA
		Charging			<140		µA
I_{SYS}	SYS Pin Current	Battery Only, Telemetry Off			100		µA
		Battery Only, Telemetry On			2.75		mA
		Charging, $V_{BAT} > V_{CHARGE}$ (Note 7)			3.65		mA
V_{IN_DUVLO}	V_{IN} to $V_{BATSENS}$ Differential Undervoltage (Must Be Satisfied for Charging)	Rising Threshold Hysteresis	●	140	200 100	250	mV mV
V_{IN_OVLO}	Input Overvoltage Lockout (Inhibits Charger)	Rising Threshold Hysteresis	●	37.7	38.6 1.4	39.5	V V
Input Undervoltage Current Limit							
V_{UVCLFB}	UVCLFB Pin Regulation Range (8-Bit DAC)	V_{UVCLFB} Maximum Code 0xFF V_{UVCLFB} Minimum Code 0x00	●	1188	1200 4.6875	1212	mV mV
	UVCLFB Pin Regulation DAC LSB				4.6875		mV
	UVCLFB Pin Leakage Current	V_{UVCLFB} = 1.2V	●	–100		100	nA
Input Current Limit							
	Regulated Input Current Limit Tolerance	Full-Scale $V_{CLP–CLN}/R_{SNSI}$	●	–2.0		2.0	%
I_{CL}	Input Current Limit Range	$I_{CL} = (V_{CLP – CLN})/R_{SNSI}$			0.5 – 32		mV/R_{SNSI}
	Input Current Limit LSB Step Size				0.5		mV/R_{SNSI}
	CLP Input Current	V_{CLP} = 12V, $V_{CLP–CLN}$ = 32mV			45		µA
	CLN Input Current	V_{CLP} = 12V, $V_{CLP–CLN}$ = 32mV		–100		100	nA
	CLP, CLN Common Mode Range	Note 8		4		35	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2), DV_{CC} = 3.3V, UVCLFB = 1.5; CELLS1 = $INTV_{CC}$; EQ, MPPT, CELLS0, CELLS2, CHEM0, CHEM1 = 0; RT = 95.3k; R_{CCREF} = 301k, $R_{NTCBIAS}$ = R_{NTC} = 10k; BATSENS = CSN = CSP; DRV_{CC} = $INTV_{CC}$; SYS = CLP = CLN. Conditions: Charging; V_{IN} = 12V, SYS = 12V, BATSENS = 7.4V .....Battery Only; V_{IN} = 0V, SYS = 8.4V, BATSENS = 8.4V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Regulator (SYS is Supply Pin for This Regulator)							
V_{INTVCC}	Internal Regulator Output Voltage	No Load			5		V
	Load Regulation	I_{INTVCC} = 50 mA			1.5	2.5	%
V_{INTVCC_CUVLO}	$INTV_{CC}$ Undervoltage Charger Lockout	Rising Threshold Hysteresis	●	4.2	4.3 0.3	4.4	V V
V_{INTVCC_TUVLO}	$INTV_{CC}$ Undervoltage Telemetry System Lockout	Rising Threshold Hysteresis	●	2.75	2.85 0.12	2.95	V V
DRV_{CC} INPUT (External Supply or Supplied by $INTV_{CC}$)							
V_{DRVCC}	DRV_{CC} Supply Voltage			4.3		5.5	V
	DRV_{CC} Undervoltage Lockout	Rising Threshold Hysteresis	●	4.1	4.2 0.3	4.3	V V
Battery Charger (All Chemistries)							
I_{CHARGE}	Battery Charge Current Range, Battery Charge Current Resolution	V_{CSP} > 2.6V (Note 10)			1 – 32 1		mV/R_{SNSB} mV/R_{SNSB}
	Peak Low V_{CSP} Charge Current	V_{CSP} < 2.4V			7.0		mV/R_{SNSB}
	$I_{BATSENS}$ + I_{CSP} + I_{CSN}	Charger Suspended (Telemetry Active) V_{IN}, V_{SYS} = 12V, $V_{BATSENS}$ = 7.4V V_{IN}, V_{SYS} = 35V, $V_{BATSENS}$ = 34V (9 Cells)			 110 200		 µA µA
Lithium-Ion/Lithium Polymer Battery Charger							
Lithium-Ion/Lithium Polymer Programmable, CHEM1, CHEM0 = [LL] (Note 9)							
	Li-Ion Charge Voltage Max DAC Setting	Code 11111 (Note 11)			4.2		V/Cell
	Li-Ion Charge Voltage Min DAC Setting	Code 00000 (Note 11)			3.8125		V/Cell
	Li-Ion Charge Voltage DAC LSB				12.5		mV
	Li-Ion Recharge Voltage	Percent of Charge Voltage			97.5		%
	Charge C/x Termination Setting	$V_{CSP–CSN}$ (I^2C Termination Option)			3.2		mV
Lithium-Ion/Lithium Polymer Fixed 4.2, 4.1, 4.0 Charge Voltage, CHEM1, CHEM0 = [HH,LZ,ZL] (Note 9)							
	4.2V Fixed Li-Ion Charge Voltage	CHEM1,0 = [H,H] (Note 11)			4.200		V/Cell
	4.2V Fixed Li-Ion Recharge Voltage	CHEM1,0 = [H,H]			4.095		V/Cell
	4.1V Fixed Li-Ion Charge Voltage	CHEM1,0 = [L,Z] (Note 11)			4.100		V/Cell
	4.1V Fixed Li-Ion Recharge Voltage	CHEM1,0 = [L,Z]			4.000		V/Cell
	4.0V Fixed Li-Ion Charge Voltage	CHEM1,0 = [Z,L] (Note 11)			4.000		V/Cell
	4.0V Fixed Li-Ion Recharge Voltage	CHEM1,0 = [Z,L]			3.900		V/Cell
Lithium-Ion/Lithium Polymer, CHEM1, CHEM0 = [LL, HH, LZ, ZL] (Note 9)							
	Low Battery Precharge Threshold	Charge Voltage = 4.2V			2.85		V/Cell
	Low Battery Precharge Hysteresis	Charge Voltage = 4.2V			50		mV/Cell
	Low Battery Precharge Current	I_{CHARGE} Set to 32 mV/R_{SNSB}			3		mV/R_{SNSB}
	Max Charge Time				18.2		hrs
	Charge Termination Timer	(Default Termination)			4		hrs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2), DV_{CC} = 3.3V, UVCLFB = 1.5; CELLS1 = $INTV_{CC}$; EQ, MPPT, CELLS0, CELLS2, CHEM0, CHEM1 = 0; RT = 95.3k; R_{CCREF} = 301k, $R_{NTCBIAS}$ = R_{NTC} = 10k; BATSENS = CSN = CSP; DRV_{CC} = $INTV_{CC}$; SYS = CLP = CLN. Conditions: Charging; V_{IN} = 12V, SYS = 12V, BATSENS = 7.4V .....Battery Only; V_{IN} = 0V, SYS = 8.4V, BATSENS = 8.4V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$LiFePO_4$ Battery Charger							
$LiFePO_4$, Programmable, CHEM1,CHEM0 = [LH] (Note 9)							
	$LiFePO_4$ Charge Voltage Max DAC setting	Code 11111 (Note 11)			3.8		V/Cell
	$LiFePO_4$ Charge Voltage Min DAC setting	Code 00000 (Note 11)			3.4125		V/Cell
	$LiFePO_4$ Charge Voltage DAC LSB				12.5		mV
	$LiFePO_4$ Recharge Voltage	POR Value I^2C Programmable			3.35		V/Cell
$V_{LiFePO4-C/x}$	Charge Termination C/x Threshold	$V_{CSP-CSN}$ (I^2C Programmable)			3.2		mV
$LiFePO_4$ Fixed Standard Charge, Fixed Fast Charge, CHEM1, CHEM0 = [ZH,HZ] (Note 9)							
	$LiFePO_4$ Fixed Fast Charge Absorb Voltage	CHEM1, CHEM0 = [HZ] Only (Note 11)			3.8		V/Cell
	$LiFePO_4$ Charge Voltage	CHEM1, CHEM0 = [ZH,HZ] (Note 11)			3.6		V/Cell
	$LiFePO_4$ Recharge Voltage	CHEM1, CHEM0 = [ZH,HZ] (Note 11)			3.35		V/Cell
$LiFePO_4$, CHEM1, CHEM0 = [LH,HZ,ZH] (Note 9)							
	Max Charge Time				18.2		hrs
$V_{LiFePO4-T(CV)}$	Charge Termination Time				1		hrs
Lead-Acid Battery Charger							
Lead-Acid Fixed, CHEM1, CHEM0 = [ZZ] (Note 9)							
$V_{Lead\_Acid\_Vcharge}$	Lead-Acid V_{CHARGE}, Equalization Lead-Acid V_{CHARGE}, Absorption Lead-Acid V_{CHARGE}, CV Lead-Acid Temperature Compensation	(Note 11) (Note 11) (Note 11)			2.6 2.4 2.2 –3.65		V/Cell V/Cell V/Cell mV/Cell/°C
Lead-Acid Programmable, CHEM1, CHEM0 = [HL] (Note 9)							
$V_{Lead\_Acid\_Vcharge}$	Lead-Acid V_{CHARGE} DAC Maximum Lead-Acid V_{CHARGE} DAC Minimum Lead-Acid V_{CHARGE} DAC Resolution Lead-Acid Temperature Comp	Code 111111 (Note 11) Code 000000 (Note 11) Temperature Comp Enabled			2.6 2.0 9.5 –3.65		V/Cell V/Cell mV mV/Cell/°C
Thermistor (NTC) BIAS							
$V_{NTCBIAS}$	Applied NTC Bias Voltage	Internally Switched to 1.2V			1.2		V
I_{NTC}	NTC Leakage Current			–50		50	nA
SYSM5, CSPM5 Regulators							
$–5V_{VINM5}$	$V_{SYS} – V_{SYSM5}$, $V_{CSP} – V_{CSPM5}$	No Load			4.8		V
Power Path/Ideal Diode Controllers							
V_{FTO}	Forward Turn-On Voltage				50		mV
V_{FR}	Forward Regulation				15		mV
V_{RTO}	Reverse Turn-Off				–30		mV
$t_{IF(ON)}$	INFET Turn-On Time	INFET – V_{IN} > 3V, C_{INFET} = 3.3nF			550		µs
$t_{IF(OFF)}$	INFET Turn-Off Time	INFET – V_{IN} < 1V, C_{INFET} = 3.3nF			2		µs
$t_{OF(ON)}$	OUTFET Turn-On Time	VBAT – OUTFET > 3V, C_{OUTFET} = 3.3nF			2.3		µs
$t_{OF(OFF)}$	OUTFET Turn-Off Time	VBAT – OUTFET < 1V, C_{OUTFET} = 3.3nF			1.9		µs
Inductor Current Regulation							
I_{LIM}	Cycle by Cycle Max Charge Current	Note 5	●	47	52	57	mV/R_{SNSB}
I_{REV}	Reverse Inductor Current		●	3.8	7.0	10	mV/R_{SNSB}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2), DV_{CC} = 3.3V, UVCLFB = 1.5; CELLS1 = $INTV_{CC}$; EQ, MPPT, CELLS0, CELLS2, CHEM0, CHEM1 = 0; RT = 95.3k; R_{CCREF} = 301k, $R_{NTCBIAS}$ = R_{NTC} = 10k; BATSENS = CSN = CSP; DRV_{CC} = $INTV_{CC}$; SYS = CLP = CLN. Conditions: Charging; V_{IN} = 12V, SYS = 12V, BATSENS = 7.4V .....Battery Only; V_{IN} = 0V, SYS = 8.4V, BATSENS = 8.4V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator							
f_{OSC}	Switching Frequency	R_T = 95.3k	●	475	500	525	kHz
f_{MAX}	Maximum Programmable Frequency	R_T = 47.5k			1		MHz
f_{MIN}	Minimum Programmable Frequency	R_T = 237k			200		kHz
Gate Drivers							
R_{UP-TG}	TG Pull-Up On-Resistance				2.0		Ω
$R_{DOWN-TG}$	TG Pull-Down On-Resistance				0.5		Ω
R_{UP-BG}	BG Pull-Up On-Resistance				2.0		Ω
$R_{DOWN-BG}$	TG Pull-Down On-Resistance				0.5		Ω
t_{R-TG}	TG 10% to 90% Rise Time	C_{LOAD} = 3.3nF			20		ns
t_{F-TG}	TG 90% to 10% Fall Time	C_{LOAD} = 3.3nF			10		ns
t_{R-BG}	BG 10% to 90% Rise Time	C_{LOAD} = 3.3nF			20		ns
t_{F-BG}	BG 90% to 10% Fall Time	C_{LOAD} = 3.3nF			10		ns
t_{NO}	Non-Overlap Time				60		ns
$t_{ON(MIN)}$	Minimum On-Time				140		ns
DC_{MAX}	Maximum Duty Cycle				98.4		%
VC Error Amplifier							
g_m	Transconductance to V_C pin g_m ($V_{CSP-CSM}$) (Constant-Current) g_m ($V_{BATSENS}$) (Constant-Voltage Lithium) g_m ($V_{BATSENS}$) (Constant-Voltage LA) g_m (V_{UVCLFB}) (Input Voltage Regulation) g_m ($V_{CLP-CLM}$) (Input Current Limiting)	 2 Cell; (gm = 1.06^{-3} • 2/(7 • Cell Count) 6 Cell; (gm = 1.06^{-3} • 3/(7 • Cell Count)			 4.10 0.15 0.08 1.06 4.10		 mmho mmho mmho mmho mmho
Telemetry A/D Measurement Subsystem, Battery Only Mode							
V_{ERR}	Measurement Error (Note 6)	V_{IN} = 1V V_{IN} = 35V				±100 ±1.5	mV %
		V_{SYS} = 2.5V V_{SYS} = 35V				±100 ±1.5	mV %
		V_{BAT} = 1.75V, 1 Cell Li-Ion V_{BAT} = 35V, 9 Cell Li-Ion				±50 ±1.5	mV %
		$V_{CLP-CLN}$ = 0mV $V_{CLP-CLN}$ = 32mV				±200 ±2.5	µV %
		$V_{CSP-CSN}$ = 0mV $V_{CSP-CSN}$ = 32mV				±200 ±2.5	µV %
		NTC/NTCBIAS = 50%, 75% NTC/NTCBIAS = 5%				±2 ±3.5	% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2), DV_{CC} = 3.3V, UVCLFB = 1.5; CELLS1 = $INTV_{CC}$; EQ, MPPT, CELLS0, CELLS2, CHEM0, CHEM1 = 0; RT = 95.3k; R_{CCREF} = 301k, $R_{NTCBIAS}$ = R_{NTC} = 10k; BATSENS = CSN = CSP; DRV_{CC} = $INTV_{CC}$; SYS = CLP = CLN. Conditions: Charging; V_{IN} = 12V, SYS = 12V, BATSENS = 7.4V .....Battery Only; V_{IN} = 0V, SYS = 8.4V, BATSENS = 8.4V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Coulomb Counter							
V_{SENSE}	Sense Voltage Differential Input Range	$V_{CSP–CSN}$				±50	mV
q_{LSB}	Charge Measurement Resolution	Prescaler M = 512 (Default)			0.017		mVhr
TCE	Total Charge Error	10mV ≤ $\|V_{SENSE}\|$ ≤ 50mV				±1.5	%
		10mV ≤ $\|V_{SENSE}\|$ ≤ 50mV	●			±2.5	%
		V_{SENSE} = 1mV			<1.0		%
I_{QC_CSP}	I_Q^- Coulomb Counter	V_{SENSE} = 30mV, Battery Only			78		µA
CELLS0, CELLS1, CELLS2, CHEM0, CHEM1 Programming Input Pins (Note 9)							
V_{IHPP}	Input High Threshold	$INT_{VCC} – V_{PIN}$	●			0.3	V
V_{ILPP}	Input Low Threshold	V_{PIN}	●			0.3	V
R_{IZPP}	Input High-Z Test Resistance	Internal 50k/50k Resistor Divider Applied to Inputs During Chemistry/Cell Read			25		kΩ
MPPT, EQ Input Pins							
	MPPT, EQ Input High Threshold		●	1.1			V
	MPPT, EQ Input Low Threshold		●			0.2	V
	MPPT, EQ Pin Leakage Current	V_{EQ}, V_{MPPT} = 5V			0	1	µA
$\overline{SMBALERT}$ Pin Characteristics							
$I_{\overline{SMBALERT}}$	$\overline{SMBALERT}$ Pin Leakage Current	$V_{\overline{SMBALERT}}$ = 5V			0	1	µA
$V_{\overline{SMBALERT}}$	$\overline{SMBALERT}$ Pin Output Low Voltage	$I_{\overline{SMBALERT}}$ = 1mA			65	100	mV
I^2C Port, SDA, SCL							
DV_{CC}	I^2C Logic Reference Level			1.6		5.5	V
I_{DVCCQ}	DV_{CC} Current	SCL/SDA = 0kHz			0		µA
ADDRESS	I^2C Address				1101_000[R/$\overline{W}$]b		
V_{IHI2C}	Input High Threshold					70	% DV_{CC}
V_{ILI2C}	Input Low Threshold			30			% DV_{CC}
I_{IHI2C}	Input Leakage High			–1		1	µA
I_{ILI2C}	Input Leakage Low			–1		1	µA
V_{OLI2C}	Digital Output Low (SDA)	I_{SDA} = 3mA				0.4	V
F_{SCL}	SCL Clock Frequency					400	kHz
t_{LOW}	LOW Period of SCL Clock			1.3			µS
t_{HIGH}	HIGH Period of SCL Clock			0.6			µS
t_{BUF}	Bus Free Time Between Start and Stop Conditions			1.3			µs
$t_{HD(STA)}$	Hold Time, After (Repeated) Start Condition			0.6			µs
$t_{SU(STA)}$	Setup Time After a Repeated Start Condition			0.6			µs
$t_{SU(STO)}$	Stop Condition Set-Up Time			0.6			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2), DV_{CC} = 3.3V, UVCLFB = 1.5; CELLS1 = $INTV_{CC}$; EQ, MPPT, CELLS0, CELLS2, CHEM0, CHEM1 = 0; RT = 95.3k; R_{CCREF} = 301k, $R_{NTCBIAS}$ = R_{NTC} = 10k; BATSENS = CSN = CSP; DRV_{CC} = $INTV_{CC}$; SYS = CLP = CLN. Conditions: Charging; V_{IN} = 12V, SYS = 12V, BATSENS = 7.4V .....Battery Only; V_{IN} = 0V, SYS = 8.4V, BATSENS = 8.4V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{HD(DAT(OUT))}$	Output Data Hold Time		0		900	ns
$t_{HD)DAT(IN))}$	Input Data Hold Time		0			ns
$t_{SU(DAT)}$	Data Set-Up Time		100			ns
t_{SP}	Input Spike Suppression Pulse Width				50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4015 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4015E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4015I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (PD, in Watts) according to the formula:

$$T_J = T_A + (PD \bullet \theta_{JA})$$

where θ_{JA} = 34°C/W for the UHF package.

Note 3: The LTC4015 includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: UVCLFB is internally clamped above the maximum UVCLFB regulation point (2.5V at 200µA nominally). Maximum input current must be limited to 200µA when this clamp is reached.

Note 5: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current may result in device degradation or failure.

Note 6: Measurement error is the magnitude of the difference between the actual measured value and the ideal value. Error for $V_{CLP-CLN}$ and $V_{CSP-CSN}$ is expressed in µV, a conversion to an equivalent current may be made by dividing by the sense resistors, R_{SNSI} and R_{SNSB}, respectively.

Note 7: V_{CHARGE} is the battery charge voltage (or CV, constant-voltage) target. V_{BAT} is the battery voltage. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

Note 8: V_{IN}, or V_{BAT} for battery only operation, may be connected to any suitable DC power source from 2.8V to 35V such that the voltage at V_{SYS} is high enough to allow $INTV_{CC}$ to support the desired mode of operation. In order for the telemetry system to operate, $INTV_{CC}$ must exceed the telemetry undervoltage lockout (V_{INTVCC_TUVLO}). In order for the battery charger to operate, $INTV_{CC}$ must exceed the charger undervoltage lockout (V_{INTVCC_CUVLO}). Allowing for 0.3V of drop from V_{IN} to $INTV_{CC}$, these modes require a minimum input voltage of 3.1V and 4.35V, respectively. Additionally the V_{IN} to $V_{BATSENS}$ (V_{IN_DULVO}) differential must also be satisfied for charging.

Note 9: Chemistry selection is made using the CHEM1 and CHEM0 pins. These are three-state pins used by the LTC4015 to select of one of nine chemistry specific charging algorithms. These pins should be hard wired to GND(L), $INTV_{CC}$(H), or left open (Z > 1000kΩ).

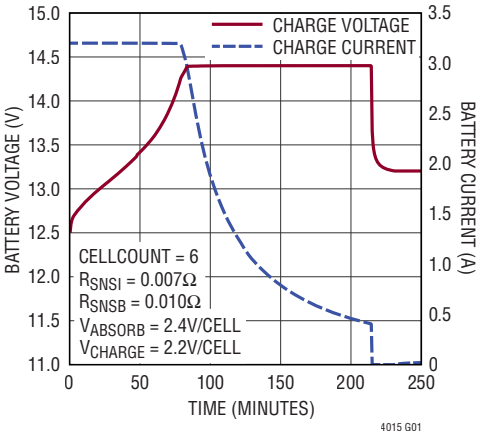
Note 10: I_{CHARGE} is the battery charge current (or CC, constant-current) target. I_{CHG} is the charge current when charging.

Note 11: Charge voltage tolerance is $V_{CHARGE(TOL)}$ which is specified at the beginning of the electrical table. The LTC4015 is not a substitute for pack protection! The 4015 does not monitor or balance individual cells – the full stack voltage is divided by number of cells for simplicity only.

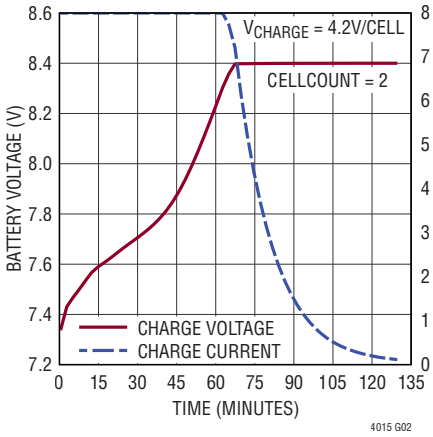
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, application circuit 1 unless otherwise noted.

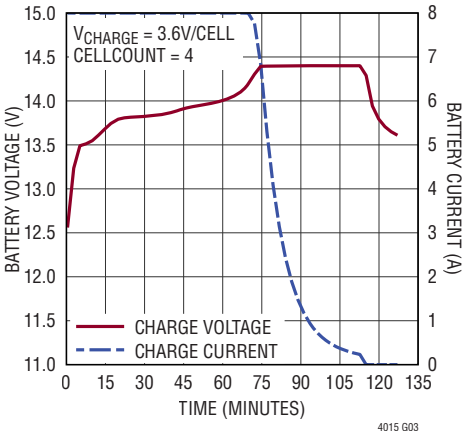
Lead-Acid Charging Profile Voltage, Current vs Time



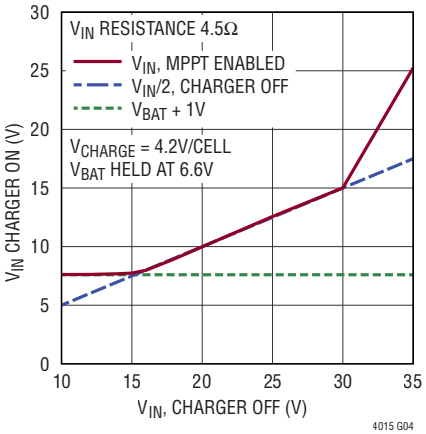
Li-Ion Charging Profile Voltage, Current vs Time



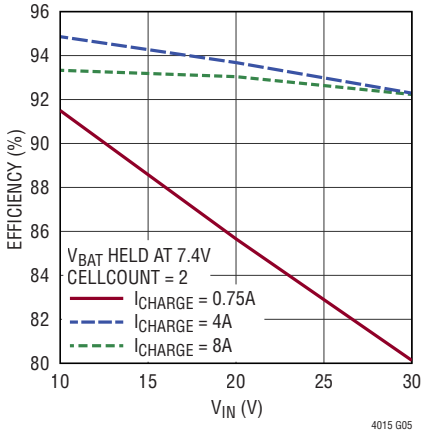
LiFePO4 Charging Profile Voltage, Current vs Time



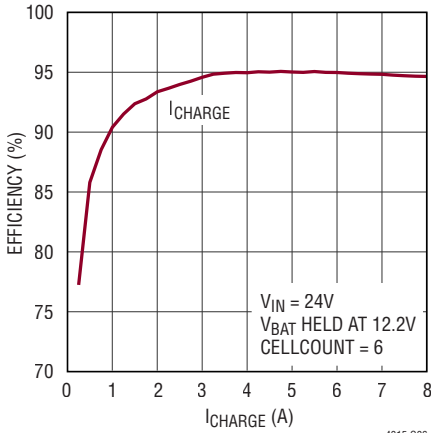
VIN (Resistive), MPPT Enabled Charger On/Off



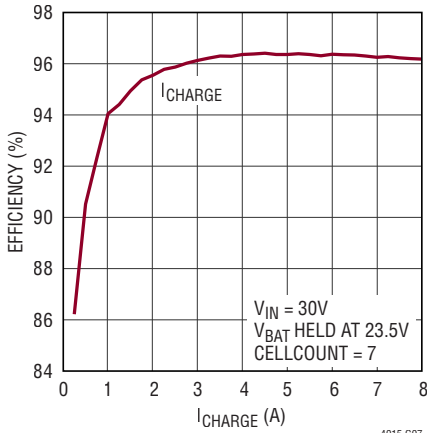
Li-Ion Charging Efficiency vs VIN



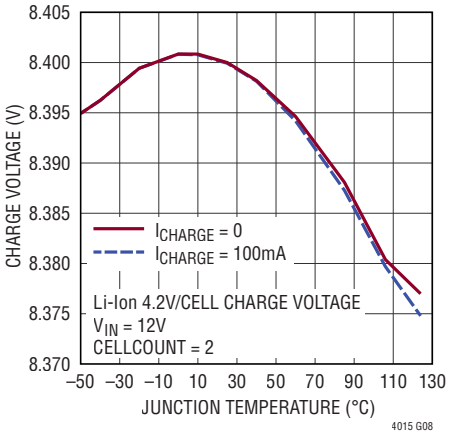
Lead-Acid Charging Efficiency vs ICHARGE



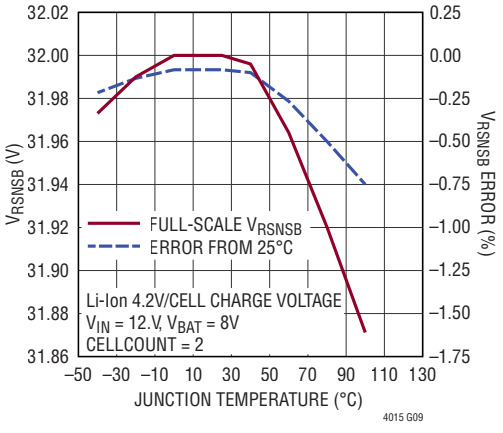
LiFePO4 Charging Efficiency vs ICHARGE



Charge Voltage (CV Mode) vs Junction Temperature



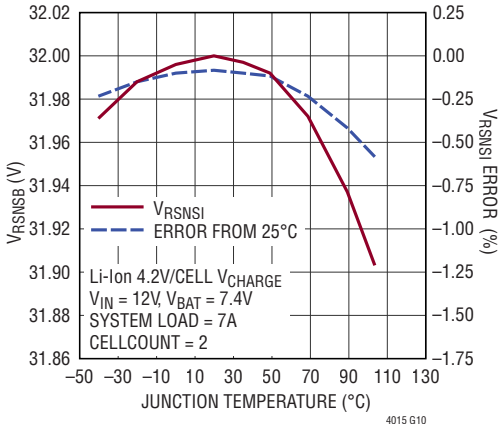
VRSNSB Current (CC Mode) vs Junction Temperature



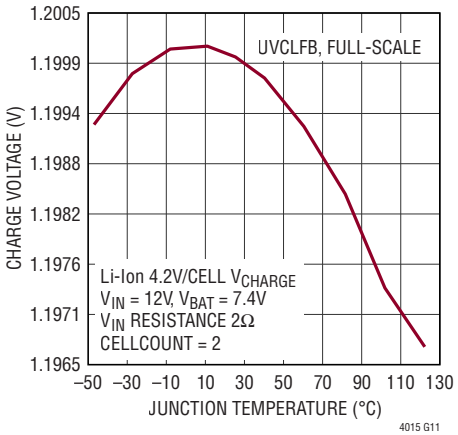
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, application circuit 1 unless otherwise noted.

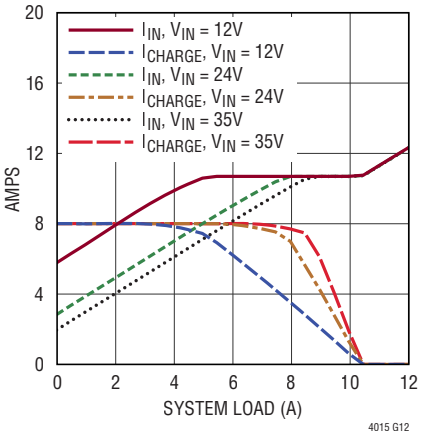
V_{RSNSI} Charging (ICL Mode) vs Junction Temperature



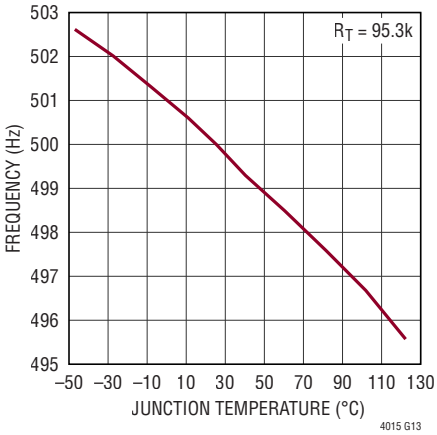
UVCLFB Voltage (UVCL Mode) vs Junction Temperature



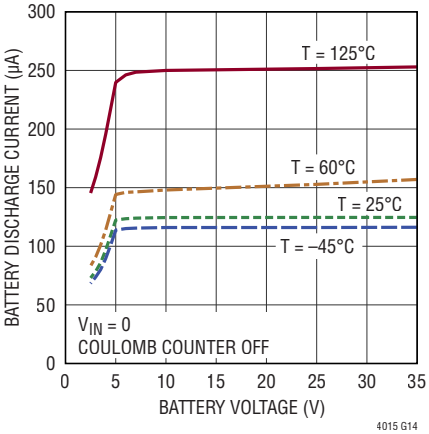
Input Current Limiting I_{IN} and I_{CHARGE} vs System Load



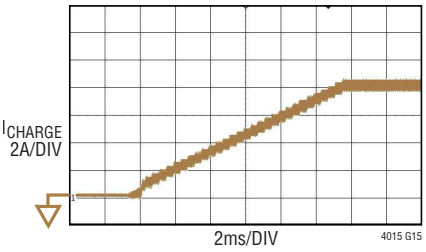
RT Oscillator Frequency vs Junction Temperature



Battery Discharge Current vs Battery Voltage

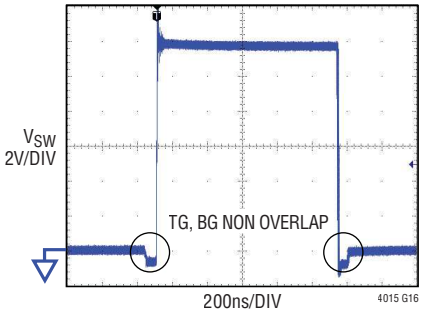


Battery Charger Soft-Start (I_{CHARGE} vs Time)



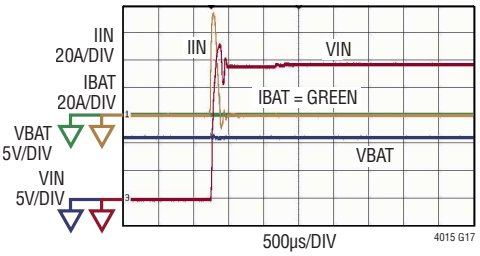
I_{CHARGE} MAX = 8A
R_{SNSB} = 0.004Ω

Gate Drive Non-Overlap (Transient)

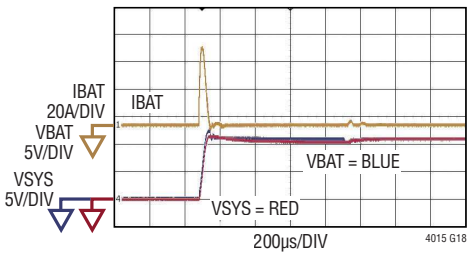


V_{IN} = 12V
V_{BAT} = 7.4V

V_{IN} Hot Plug, 0 to 24V, 4-Cell $LiFePO_4$

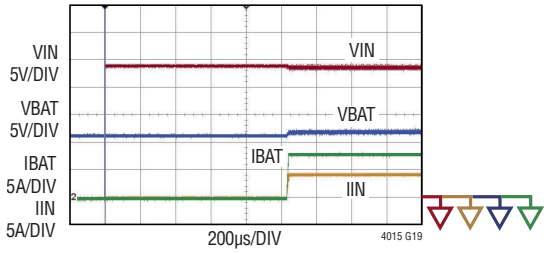


Battery Hot Plug, 0 to 11V, 4-Cell $LiFePO_4$

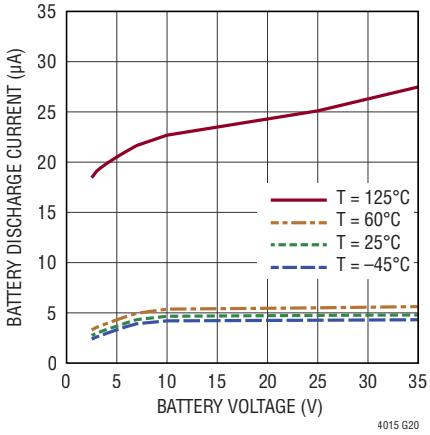


TYPICAL PERFORMANCE CHARACTERISTICS

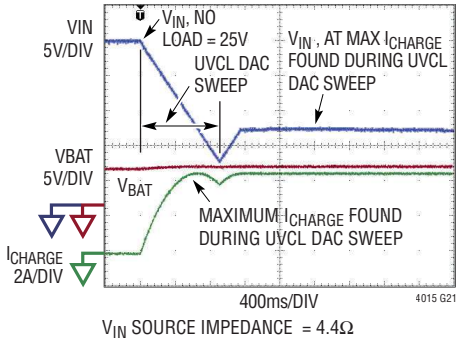
Start-Up from 24V V_{IN} Hot Plug, I_{CHARGE} = 8A (R_{SNSB} = 0.004Ω)



Ship Mode Battery Discharge Current vs Battery Voltage

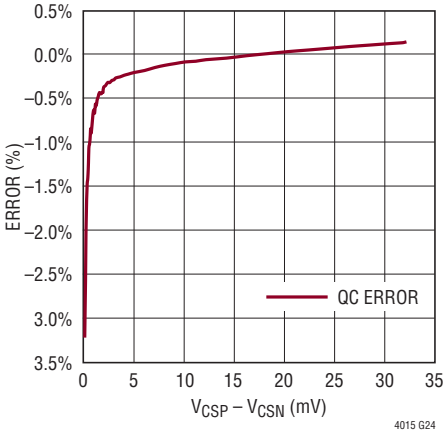


MPPT Algorithm Using UVCL DAC Sweep to Find MPP



V_{IN} SOURCE IMPEDANCE = 4.4Ω

Coulomb Counter Accuracy vs $V_{CSP–CSN}$



PIN FUNCTIONS

CELLS1 (Pin 1): Number of Cells Select Pin. Three-state pin used in combination with CELLS0 and CELLS2 to set the total number of battery cells.

CELLS2 (Pin 2): Number of Cells Select Pin. Three-state pin used in combination with CELLS0 and CELLS1 to set the total number of battery cells.

DV_{CC} (Pin 3): Logic Supply for the I^2C Serial Port. DV_{CC} sets the reference level of the SDA and SCL pins for I^2C compliance. It must be connected to the same power supply used to power the I^2C pull up resistors. If the I^2C port is unused connect this pin to $INTV_{CC}$, do not float.

SCL (Pin 4): Clock Input for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC} for I^2C compliance. If the I^2C port is unused connect this pin to $INTV_{CC}$, do not float.

SDA (Pin 5): Data Input/Output for the I^2C serial port. The I^2C input levels are scaled with respect to DV_{CC} for I^2C compliance. If the I^2C port is unused connect this pin to $INTV_{CC}$, do not float.

$\overline{\text{SMBALERT}}$ (Pin 6): Open-Drain Interrupt Request. Pulls low when something important needs to be reported back to the system.

SGND (Pin 7): Signal Ground. All small signal components and compensation should connect to this ground, which should be connected to PGND at a single point.

UVCLFB (Pin 8): Undervoltage Current Limit Feedback Pin. UVCLFB can be used to reduce charge current when the V_{IN} pin reaches a level programmed by the user supplied resistor divider. This feature can be used for power sources with higher source impedance such as a solar panel. Maximum charge current is tapered off when this pin is below 1.2V, at 1.15V the charge current is zero. UVCLFB is internally clamped to about 2.5V with 200µA in this pin. Limit the current into this pin to 200µA at maximum V_{IN} using the thevenin resistance of the input divider. If the input undervoltage current limit feature is not desired, connect UVCLFB to $2P5V_{CC}$ through a 10k resistor or to V_{IN} through an appropriately sized resistor.

VC (Pin 9): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage normally ranges from 900mV to 2.4V.

RT (Pin 10): Connect a resistor from RT to GND to set frequency of the switching power supply.

NTC (Pin 11): Thermistor Input. The NTC pin connects to a negative temperature coefficient thermistor (Type_2) to monitor the temperature of the battery. The voltage on this pin is digitized by the analog to digital converter and is available via the I^2C port. The thermistor value is also used to qualify battery charging. Connect a low drift bias resistor from NTCBIAS to NTC and a thermistor from NTC to ground. If NTC functions are unwanted, use a resistor equal in value to $R_{NTCBIAS}$ instead of a thermistor.

NTCBIAS (Pin 12): NTC Thermistor Bias Output. Connect a bias resistor between NTCBIAS and NTC, and a thermistor between NTC and GND. The bias resistor should be equal in value to the nominal value of the thermistor. The LTC4015 applies 1.2V to this pin during NTC measurement.

EQ (Pin 13): Equalize. Apply a logic signal between 1.5V and $INTV_{CC}$ (5V) to this pin to allow the 4015 to trigger lead-acid equalize mode. GND this pin if unused, do not float.

GND (Pin 14, Exposed Pad Pin 39): Ground. The exposed pad should be connected by multiple vias directly under the LTC4015 to a continuous ground plane on the second layer of the printed circuit board.

CSPM5 (Pin 15): Internal Supply Pin. The V_{CSPM5} pin regulates at the higher of ground or approximately $V_{CSP} – 5V$. A low impedance multilayer ceramic capacitor should be connected from V_{CSP} to V_{CSPM5}.

CCREFM (Pin 16): Coulomb Counter Reference Resistor Pin. Leakage on this pin will affect Coulomb counter accuracy. Connect a 301k, 0.1%, 25ppm resistor from CCREFM to CCREP.

CCREFP (Pin 17): Coulomb Counter Reference Resistor Pin. CCREFP in conjunction with CCREFM provide a reference for the Coulomb counter to make an accurate measure of charge into and out of the battery. CCREFP is connected internally to CSP with 50Ω. Connect a 301k, 0.1%, 25ppm resistor from CCREFP to CCREM.

PIN FUNCTIONS

BATSENS (Pin 18): Battery Voltage Sense Input. For proper operation, this pin must be connected physically close to the positive input terminal of the battery.

CSN (Pin 19): Connection Point for the Negative Terminal of the Charge Current Sense Resistor.

CSP (Pin 20): Connection Point for the Positive Terminal of the Charge Current Sense Resistor.

MPPT (Pin 21): MPPT Enable Pin. Apply a logic signal between 1.5V and $INTV_{CC}$ (5V) to this pin to allow the 4015 to enter MPPT mode. MPPT mode can also be entered via the I^2C port. GND this pin if unused, do not float.

$2P5V_{CC}$ (Pin 22): Bypass Pin for the Internal 2.5V Regulator. This regulator provides power to the internal logic circuitry. Bypass $2P5V_{CC}$ with a 2.2µF multilayer ceramic capacitor to GND.

SW (Pin 23): Switch Node. SW pin swings from a diode drop below ground up to V_{SYS}.

TG (Pin 24): Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to DRV_{CC} superimposed on the switch node voltage V_{SW}.

BOOST (Pin 25): Boosted Floating Top Gate Drive Supply. The BOOST pin swings from a diode voltage below DRV_{CC} up to V_{SYS} + DRV_{CC}.

BG (Pin 26): Bottom Gate Drive. Drives the bottom N-channel MOSFET between DRV_{CC} and ground.

DRV_{CC} (Pin 27): External Supply for Gate Driver. Do not exceed 5.5V on this pin. If DRV_{CC} is not connected to $INTV_{CC}$, $INTV_{CC}$ must be greater than 3V before DRV_{CC} is applied. If not connected to $INTV_{CC}$ bypass this pin to ground with a low ESR ceramic capacitor.

$INTV_{CC}$ (Pin 28): Internal 5V Regulator Output. The control circuits and optionally the gate drivers are powered from this pin. Bypass this pin to ground with a minimum 4.7µF low ESR tantalum or ceramic capacitor.

OUTFET (Pin 29): Output Ideal Diode Gate Control Pin for External P-channel MOSFET.

SYSM5 (Pin 30): Internal Supply Pin. The V_{SYSM5} pin regulates at the higher of ground or approximately V_{SYS} – 5V. A low impedance multilayer ceramic capacitor should be connected from V_{SYS} to V_{SYSM5}.

SYS (Pin 31): System Input Voltage. Primary power input to the 4015. This pin powers the internal $INTV_{CC}$ LDO. SYS is the max of V_{BAT} or V_{IN}. V_{SYS} should be bypassed with a low impedance multilayer ceramic capacitor, along with large bulk capacitors.

CLN (Pin 32): Connection Point for the Negative Terminal of the Input Current Sense Resistor.

CLP (Pin 33): Connection Point for the Positive Terminal of the Input Current Sense Resistor.

INFET (Pin 34): Input Ideal Diode Gate Control Pin for External N-channel MOSFET.

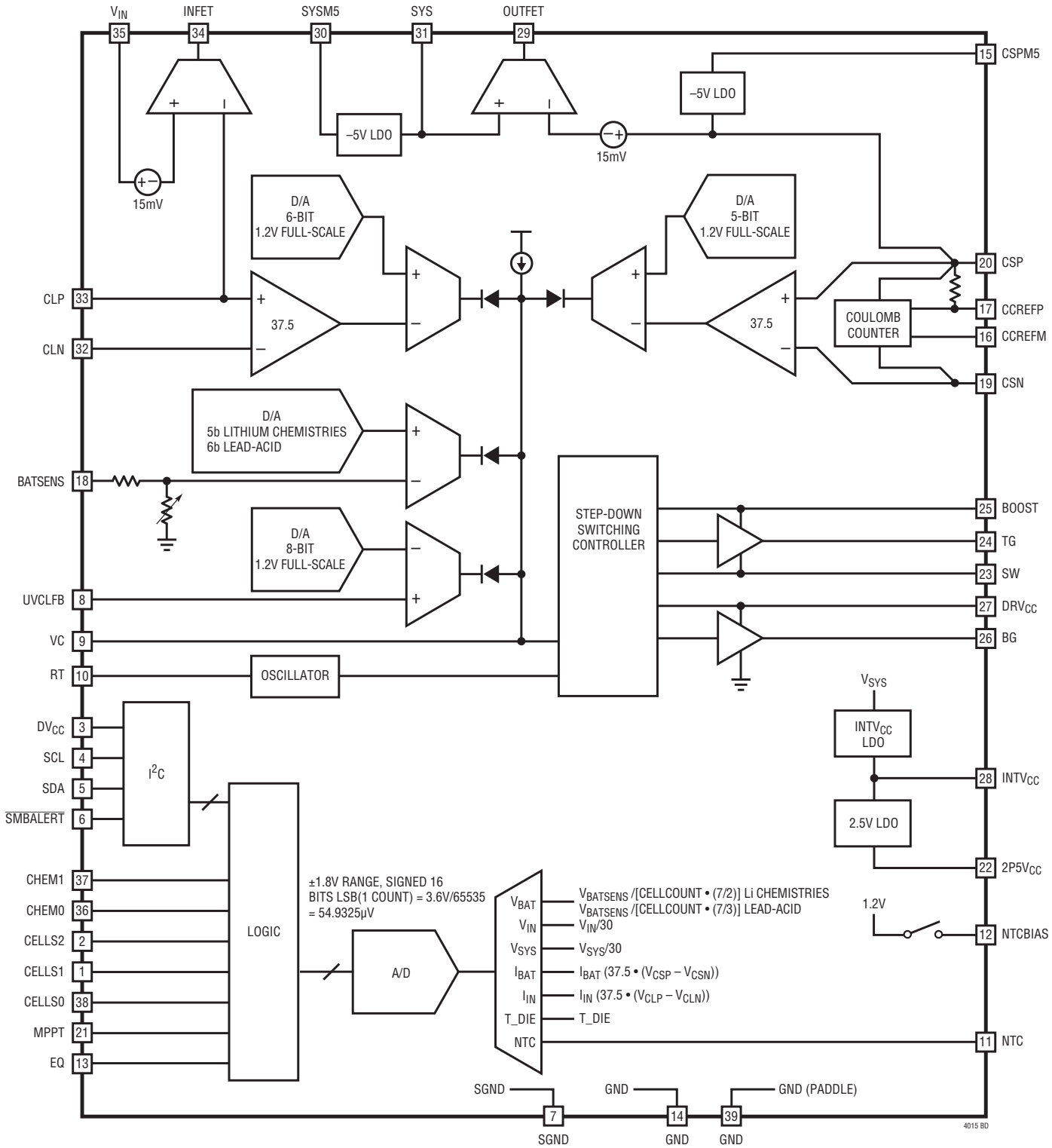
V_{IN} (Pin 35): Supply Voltage for the PowerPath Step-down Switching Charger. V_{IN} may be connected to any suitable DC power source from 2.8V to 35V such that the voltage at V_{SYS} is high enough to allow $INTV_{CC}$ to support the desired mode of operation. In order for the telemetry system to operate $INTV_{CC}$ must exceed the telemetry undervoltage lockout. V_{IN} should be bypassed with a low impedance multilayer ceramic capacitor.

CHEM0 (Pin 36): Chemistry Select Pin. Three-state pin used in combination with CHEM1 to set the battery chemistry and charge algorithm.

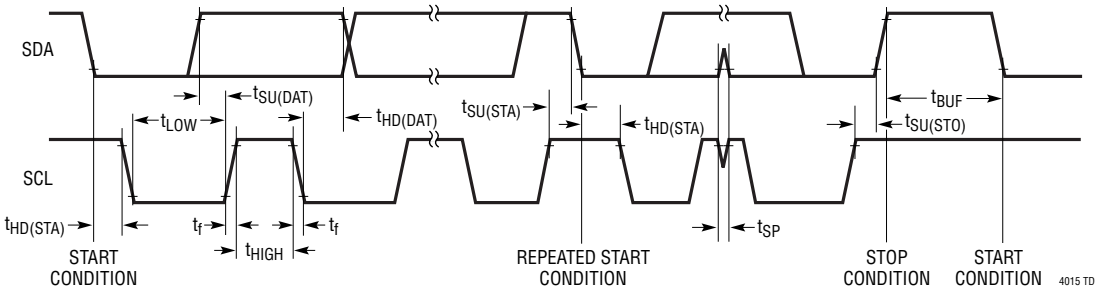
CHEM1 (Pin 37): Chemistry Select Pin. Three-state pin used in combination with CHEM0 to set the battery chemistry and charge algorithm.

CELLS0 (Pin 38): Number of Cells Select Pin. Three-state pin used in combination with CELLS1 and CELLS2 to set the total number of battery cells.

BLOCK DIAGRAM



I²C TIMING DIAGRAM



I²C SMBus Legend

S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
A	ACKNOWLEDGE
N	NACK
P	STOP CONDITION
PEC*	PACKET ERROR CODE
	MASTER TO SLAVE
	SLAVE TO MASTER

SMBus WRITE WORD PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

SMBus WRITE WORD WITH PEC PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC*	A	P

SMBus READ WORD PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	N	P

SMBus READ WORD WITH PEC PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC*	N	P

SMBus ALERT RESPONSE ADDRESS PROTOCOL

S	ALERT RESPONSE ADDRESS	Rd	A	DEVICE ADDRESS	Rd	N	P

SMBus ALERT RESPONSE ADDRESS PROTOCOL WITH PEC

S	ALERT RESPONSE ADDRESS	Rd	A	DEVICE ADDRESS	Rd	A	PEC*	N	P

*USE OF PACKET ERROR CHECKING IS OPTIONAL

OPERATION

Introduction

The LTC4015 is a Li-Ion/LiFePO$_4$/lead-acid battery charger utilizing a step-down switching controller. It is designed to efficiently transfer power from a variety of possible sources, such as wall adapters and solar panels, to a battery and system load while minimizing power dissipation and easing thermal budgeting constraints. Since a switching regulator conserves power, the LTC4015 allows the charge current to exceed the source's output current, making maximum use of the allowable power for battery charging without exceeding the source's delivery specifications. By incorporating input voltage and current measurement and control systems, the switching charger interfaces seamlessly to these sources without requiring application software to monitor and adjust system loads.

By decoupling the system load from the battery and prioritizing power to the system, the instant-on PowerPath architecture ensures that the system is powered immediately after V_{IN} is applied, even with a completely dead battery.

Two ideal diode controllers drive external MOSFETs to provide low loss power paths from V_{IN} and V_{BAT} to the system. Two ideal diodes work with the charger to provide power from V_{BAT} to the system without back driving V_{IN}. The ideal diode from V_{BAT} to the system load guarantees that power is available to the system even if there is insufficient or absent power from V_{IN}. The ideal diode from V_{IN} to the system load guarantees neither V_{BAT} or the system will back drive V_{IN}.

A wide range of input current settings as well as battery charge current settings are available by software control and the values of sense resistors R_{SNSI} and R_{SNSB}. A measurement subsystem periodically monitors and reports system parameters via the I^{2}C serial port. Included in this subsystem is a Coulomb counter to allow battery gas gauging.

An interrupt subsystem can be enabled to alert the host microprocessor of various status change events so that system parameters can be varied as needed by the system. Many status change events are maskable for maximum flexibility.

To eliminate battery drain between manufacture and sale, a ship-and-store feature reduces the already low battery drain and optionally disconnects power from downstream circuitry.

The input undervoltage current loop (UVCL) can be engaged to help keep the input voltage from decreasing beyond a minimum voltage when a resistive cable or power limited supply such as a solar panel is providing input power to the LTC4015. A maximum power point algorithm using this control loop has been preprogrammed into the LTC4015 to maximize power extraction from solar panels and other resistive sources.

Finally, the LTC4015 has a digital subsystem that provides substantial adjustability so that power levels and status information can be controlled and monitored via the simple 2-wire I^{2}C serial port.

LTC4015 Digital System Overview

The LTC4015 contains an advanced digital system which can be optionally accessed using the I^{2}C serial port. The LTC4015 digital system can be used extensively in the application or not at all, as dictated by the application requirements. This data sheet provides extensive details of the digital functions of the LTC4015, though much of this detail is not required for simpler applications.

Use of the serial port is completely optional. Even without use of the serial port, the LTC4015 is a fully functioning high performance battery charger which is highly configurable using external components and pin connections. Chemistry/algorithm, cell count, charge current, input current regulation (ICL), V_{IN} undervoltage regulation (UVCL), maximum power point tracking (MPPT), and switching charger frequency and compensation are all externally configurable without using the serial port.

For applications requiring the LTC4015's advanced digital features, the serial port provides a means to use the Coulomb counter, read status and ADC telemetry data from the measurement system, monitor charger operation, configure charger settings (e.g. charge voltage, charge current, temperature response, etc), enable/disable/read/clear alerts, activate low power ship mode, and enable/disable the battery charger.

Detailed information about the digital system and the serial port registers, as well as digital system usage examples, can be found in the section LTC4015 Digital System.

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Power Path Ideal Diode Controllers

The LTC4015 features input and output ideal diode controllers. These controllers make up a power path that allows power to be delivered to the system (V_{SYS}) by either V_{IN} or V_{BAT}, whichever is greater. The input ideal diode provides a one way path from V_{IN} to V_{SYS}. The output ideal diode provides a one way path from V_{BAT} to V_{SYS}.

The ideal diode controllers consist of a precision amplifier that drives the gate of a MOS transistor whenever the voltage at V_{SYS} is approximately 15mV (V_{FWD}) below the voltage at V_{IN} or V_{BAT}. Within the amplifier's linear range, the small signal resistance of the ideal diode will be quite low, keeping the forward drop near 15mV. At higher current levels, the MOS transistors will be in full conduction.

The input ideal diode controller assumes control of an external NMOS transistor by modulating the gate voltage of the NMOS transistor to allow current to flow from V_{IN} to V_{SYS} while blocking current in the opposite direction to prevent back driving V_{IN}. Additionally a fastoff comparator shuts off the NMOS if V_{IN} falls 25mV below V_{SYS}.

The output ideal diode provides a path for V_{BAT} to power V_{SYS} when V_{IN} is unavailable, while blocking current in the opposite direction to prevent overcharging of the battery. The output ideal diode controller controls an external PMOS transistor by modulating the gate voltage of the PMOS transistor. In addition to a fast-off comparator the output ideal diode also has a fast-on comparator that turns on the external MOSFET when V_{SYS} drops 45mV below V_{BAT}.

When limited power is available to the switching charger because either the programmed input current limit or input undervoltage limit is active, charge current will automatically be reduced to prioritize power delivery to the system load. Note that the LTC4015 only limits charge current, but does not limit current from the input to the system load—if the system load alone requires more power than is available from the input after charge current has been reduced to zero, V_{SYS} must fall to the battery voltage in order for the battery to provide supplemental power. Note that a system load fault can dissipate very large amounts of power, as the system load current will not be limited by the ideal diode controllers.

Input Current Regulation (ICL)

The LTC4015 contains a control loop, ICL (input current limit), that automatically reduces charge current when the overall average input current reaches a maximum level.

The input current regulation function can only reduce charge current to zero, it cannot limit the overall input current which is a function of the load on V_{SYS}.

This level is set by the combination of the current sense resistor R_{SNSI} from CLP to CLN and either the default 32mV servo voltage or a value programmed into IIN_LIMIT_SETTING via the serial port. The maximum servo voltage that can be programmed is 32mV. The voltage across the sense resistor divided by its value determines the target maximum possible input current. A 2mΩ resistor, for example, would have an upper limit of input current of 16A using a 32mV servo voltage.

Input Undervoltage Regulation (UVCL) and Solar Panel Maximum Power Point Tracking (MPPT)

The LTC4015 contains a control loop, UVCL (under voltage current limit) that allows it to tolerate a resistive connection to the input power source by automatically reducing charge current as V_{IN} (as observed at the UVCLFB pin using a V_{IN} voltage divider) drops to a programmable level (VIN_UVCL_SETTING). This circuit helps prevent UVLO oscillations by regulating the input voltage above the LTC4015's undervoltage lockout level. The UVCL function can only reduce charge current to zero, it cannot limit the overall input current which is also a function of the load on V_{SYS}.

Optionally, the LTC4015 includes a maximum power point tracking (MPPT) algorithm to find and track the VIN_UVCL_SETTING that delivers the maximum charge current to the battery. If enabled by the MPPT pin or by the mppt_en_i2c bit via the serial port, the MPPT algorithm performs a sweep of VIN_UVCL_SETTING values, measuring battery charge current at each setting. When the sweep is completed, the LTC4015 applies the VIN_UVCL_SETTING value corresponding to the maximum battery charge current (i.e. the maximum power point). The LTC4015 then tracks small changes in the maximum power point by slowly dithering the VIN_UVCL_SETTING. The LTC4015 periodically performs a new sweep of

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VIN_UVCL_SETTING values, applies the new maximum power point, and resumes dithering at that point. With the automatic MPPT algorithm enabled, a solar panel can be used as a suitable power source for charging a battery and powering a load. The MPPT feature can be enabled either via the serial port or by connecting the MPPT pin to the $2P5V_{CC}$ pin or a suitable GPIO from a microcontroller.

The MPPT algorithm may not work for all solar panel applications and does not have to be used, alternatively a solar panel can be used without the MPPT algorithm by setting the UVCL V_{IN} minimum value to match the optimum loaded solar panel voltage by selecting the appropriate VIN_UVCL_SETTING and UVCLFB pin resistor divider.

Serial Port, SMBus and I²C Protocol Compatibility

The LTC4015 uses an SMBus/I²C style 2-wire serial port for programming and monitoring functions. Using the serial port, the user may program alerts, set control parameters and read status data. The timing diagram shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors or active loads, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC4015 is both a slave receiver and slave transmitter. It is never a master. The control signals, SDA and SCL, are scaled internally to the DV_{CC} supply in compliance with the I²C specification. DV_{CC} must be connected to the same power supply as the bus pull-up resistors.

Aside from electrical levels and bus speed, the SMBus specification is generally compatible with the I²C bus specification, but extends beyond I²C to define and standardize specific protocol formats for various types of transactions. The LTC4015 serial port is compatible with the 400kHz speed and ratiometric input thresholds of the I²C specification and supports the read word and write word protocols of the SMBus specification. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches.

Programmable Alerts and Interrupt Controller

The serial port supports the SMBus $\overline{\text{SMBALERT}}$ protocol. An alert can optionally be generated if a monitored parameter exceeds a programmed limit or if selected battery charger states or status events occur. This offloads much of the continuous monitoring from the system's microcontroller and onto the LTC4015; reducing bus traffic and microprocessor load.

The $\overline{\text{SMBALERT}}$ pin is asserted (pulled low) whenever an enabled alert occurs (see the following tables and register descriptions). The LTC4015 will de-assert (release) the $\overline{\text{SMBALERT}}$ pin only after successfully responding to an SMB alert response address (ARA). The alert response is an SMB protocol used to respond to an $\overline{\text{SMBALERT}}$. The host reads from the alert response address 0001_1001b (0x19) and each part asserting $\overline{\text{SMBALERT}}$ begins to respond with its address. The responding parts arbitrate in such a way that only the part with the lowest address responds. Only when a part has responded with its address does it release the $\overline{\text{SMBALERT}}$ signal. If multiple parts are asserting the $\overline{\text{SMBALERT}}$ signal then multiple reads from the ARA are needed. Therefore, only a response of 1101_0001b (0xD1) will clear the LTC4015/SMBALERT signal. Any other response indicates a device with a lower I²C address also requests attention from the host. For more information refer to the SMBus specification.

Table 1. Shows a Summary of LTC4015 Limit Alerts. Each Alert Has an Associated Enable (Mask), Limit, and Bit That Is Set to 1 to Indicate the Enabled Alert Has Occurred.

LIMIT ALERTS	ALERT ENABLE BITS (0x0D)	ALERT LIMIT SET POINT REGISTER	ALERT REPORTING BITS (0x36)
Measurement System Valid Alert (ADC Ready)	15	N/A	15
Reserved	14	N/A	N/A
Coulomb Counter Accumulator Low and High Alert	13, 12	0x10, 0x11	13, 12
Battery Voltage Low and High Alert	11, 10	0x01, 0x02	11, 10
Input Voltage Low and High Alert	9, 8	0x03, 0x04	9, 8
System Voltage Low and High Alert	7, 6	0x05, 0x06	7, 6
Input Current High Alert	5	0x07	5
Battery Current Low Alert	4	0x08	4
Die Temperature High Alert	3	0x09	3
Battery Series Resistance High Alert	2	0x0A	2
NTC Ratio High and Low Alert	1, 0	0x0B, 0x0C	1, 0

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Table 2. Shows a Summary of LTC4015 Charger State Alerts. Each Alert Has an Associated Enable (or Mask), and Bit That Is Set to 1 to Indicate the Alert Has Occurred.

CHARGER STATE ALERTS	ALERT ENABLE BITS (0x0E)	ALERT REPORTING BITS (0x37)
Equalize	10	10
Absorb	9	9
Charger Suspended	8	8
Precharge	7	7
CC_CV	6	6
NTC Pause	5	5
Timer Termination	4	4
C/x Termination	3	3
Max Charge Time Fault	2	2
Battery Missing Fault	1	1
Battery Short Fault	0	0

Table 3. Shows a Summary of LTC4015 Charger Status Alerts. These Alerts Indicate Which Control Loop Is in Control During Charging. Each Alert Has an Associated Enable (or Mask), and Bit That Is Set to 1 to Indicate the Alert Has Occurred.

CHARGER STATUS ALERTS	ALERT ENABLE BITS (0x0F)	ALERT REPORTING BITS (0x38)
UVCL (V_{IN} Undervoltage Charge Current Limiting)	3	3
ICL (I_{IN} Charge Current Limiting)	2	2
CC (Constant-Current Mode)	1	1
CV (Constant-Voltage Mode)	0	0

Measurement Subsystem

The LTC4015 includes a 14-bit analog-to-digital converter (ADC) and signal channel multiplexer to monitor several analog parameters. It can measure the voltages at V_{IN}, SYS and BATSENS, the current into the SYS node (voltage across R_{SNSI}), the battery charge current (voltage across R_{SNSB}), the voltage across the battery pack thermistor, and its own internal die temperature. After a charge cycle begins the LTC4015 uses the appropriate analog parameters to calculate the series resistance of the battery. To save battery power the measurement system will not run if the battery is the only source of power, unless the force_meas_sys_on bit is set.

The converter is automatically multiplexed between all of the measured channels and its results are stored in registers accessible via the I^2C port.

The seven channels measured by the ADC each take approximately 1.6ms to measure. The result of the analog-to-digital conversion is stored in a 16-bit register as a signed, two's complement number. The lower two bits of this number are sub-bits. These bits are ADC outputs which are too noisy to be reliably used on any single conversion, however, they may be included if multiple samples are averaged. The maximum range of the ADC is ±1.8V, which gives a LSB size of 3.6V/65535 ($2^{16} – 1$).

Table 4 summarizes the LSB scaling and resultant LSB size for these ADC measurements.

Table 4. Measurement Subsystem Scaling and LSB Size

ADC LSB (3.6V/65535) =				54.932479	µV
MEASUREMENT	REGISTER SYMBOL	REGISTER NUMBER	LSB SCALING	LSB SIZE	UNITS
$V_{BATSENS}$/Cellcount (Lithium Chemistries)	VBAT	0x3A	*7/2	192.264	µV
$V_{BATSENS}$/Cellcount (Lead-Acid)	VBAT	0x3A	*7/3	128.176	µV
V_{IN}	VIN	0x3B	*30	1.648	mV
V_{SYS}	VSYS	0x3C	*30	1.648	mV
V_{RSNSB} ($V_{CSP} – V_{CSN}$)	IBAT	0x3D	/37.5	1.465	µV
V_{RSNSI} ($V_{CLP} – V_{CLN}$)	IIN	0x3E	/37.5	1.465	µV
Die Temperature (Note 1)	DIE_TEMP	0x3F	1	54.932	µV

Note 1: DIE_TEMP is the ADC conversion of a internal PTAT (proportional to absolute temperature) voltage. DIE temperature = (DIE_TEMP – 12010)/45.6 in °C.

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When input power is absent, the measurement system can be sampled periodically at reduced battery load using the following procedure as an example:

a. Write en_meas_sys_valid_alert = 1

b. Write force_meas_sys_on = 1

c. Wait for $\overline{\text{SMBALERT}}$ to go low (typically 20ms from force_meas_sys_on = 1)

d. Upon $\overline{\text{SMBALERT}}$ going low, perform ARA command. If there are multiple slave devices, verify that the LTC4015 is asserting the alert.

e. Verify meas_sys_valid_alert = 1

f. Write en_meas_sys_valid_alert = 0

g. Write force_meas_sys_on = 0

h. Read updated measurement system data from the LTC4015

This procedure can be repeated at desired intervals (for example, once per second) in order to periodically monitor the system.

Thermistor/NTC Measurement

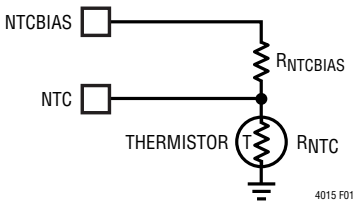

Figure 1. NTC Bias Configuration

Battery temperature is sensed by using an external NTC (negative temperature coefficient) thermistor, R_{NTC}. R_{NTC} is normally located in the battery pack. Connect R_{NTC} between the NTC pin and ground. A bias resistor, $R_{NTCBIAS}$, is connected between NTCBIAS and NTC. $R_{NTCBIAS}$ should be a 1% resistor with a value equal to the value of the chosen thermistor at 25°C (r25). NTC_RATIO (0x40) is available via the serial port, except when the ship mode feature has been activated.

The LTC4015 measurement system is configured to directly calculate NTC_RATIO, where:

$$NTC\_RATIO = 21845 \bullet \frac{R_{NTC}}{R_{NTCBIAS} + R_{NTC}}$$

$$R_{NTC} = R_{NTCBIAS} \bullet \frac{NTC\_RATIO}{21845 - NTC\_RATIO}$$

NTC_RATIO has a bit weight of 1/21845 = 4.5777^{-5}/LSB. For a NTC_RATIO of 0.5, where R_{NTC} = $R_{NTCBIAS}$, the value of NTC_RATIO reported by the serial port would be approximately 10922.

The data in the first two columns in the following table are from a Vishay NTC thermistor with a R_{25} of 10k and β value of 3490k, such as provided by a Vishay NTCS0402E3103FLT or NTHS0402N02N1002JE. The NTC_RATIO value is $21845 \bullet [R_{NTC}/(R_{NTC} + R_{NTCBIAS})]$, where $R_{NTCBIAS} = R_{25}$ = 10k.

TEMPERATURE	R_{NTC}	NTC_RATIO
10.0	18290	14122
15.0	14867	13059
20.0	12157	11985
25.0	10000	10922
30.0	8272	9889
35.0	6879	8902
40.0	5751	7975

Steps to find NTC resistor temperature given a NTC_RATIO value;

1. Retrieve value for the NTC_RATIO from the LTC4015 via the I^2C port
2. Calculate R_{NTC}; $R_{NTC} = R_{NTCBIAS} \frac{NTC\_RATIO}{21845 - NTC\_RATIO}$
3. Using the calculated R_{NTC}, use NTC resistor manufacturers data to determine temperature.

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ICL, UVCL, ICHARGE and VCHARGE DACS

The LTC4015 has four DAC's for setting target values of:

1. Maximum battery charge voltage (VCHARGE_SETTING)
2. Maximum battery charge current (ICHARGE_TARGET)
3. Minimum input voltage, UVCL (VIN_UVCL_SETTING)
4. Maximum input current (IIN_LIMIT_SETTING)

The user can program the target values only with the I^2C port. The LTC4015 uses the target values as a starting point, the charging algorithms calculate the actual values to be applied to the DACs to support functions such as Li-Ion precharge, absorb and equalize charge voltage adders, MPPT, lead-acid charge voltage temperature compensation, and charger soft starting.

The target value register is read/write, the actual value register is read only. In the case of the UVCL register, minimum input voltage is scaled by external resistors. For further information see the Register Description and Battery Charging sections.

JEITA temperature controlled charging does not use VCHARGE_SETTING or ICHARGE_TARGET for setting target values, see JEITA Temperature Controlled Charging section for further information.

Charging Timers

There are a total of four timers in the LTC4015 used in the charging algorithms. Timers are 16-bit, and measure time in seconds. $2^{16} = 65535$ seconds or 18.2 hours maximum. Each timer has current value (read only) and a timeout value (read/write):

TIMED PARAMETER	CURRENT VALUE	TIMEOUT VALUE	APPLICABLE CHEMISTRIES
Constant-Voltage State Time	CV_TIMER (0x31)	MAX_CV_TIME (0x1D)	Lithium Chemistries
Maximum Total Charge Time	MAX_CHARGE_TIMER (0x30)	MAX_CHARGE_TIME (0x1E)	Lithium Chemistries
Maximum Absorb Charge Time	ABSORB_TIMER (0x32)	MAX_ABSORB_TIME (0x2B)	LiFeP04, Lead-Acid
Maximum Equalize Charge Time	EQUALIZE_TIMER (0x33)	EQUALIZE_TIME (0x2D)	Lead-Acid

Low Power Ship Mode

The LTC4015 can reduce its already low standby current to approximately 5µA in a special mode designed for shipment and storage. Ship mode is armed by setting the ARM_SHIP_MODE register to 0x534D (ASCII for SM) via the serial port. Note that once armed, ship mode cannot be disarmed (the ARM_SHIP_MODE register cannot be cleared once set to 0x534D). Once armed, ship mode takes

The Target and Actual Registers as Well as the DAC Size are Shown Below:

FUNCTION	TARGET VALUE REGISTER			ACTUAL VALUE REGISTER		
	NAME	HEX ADDRESS (SIZE)	DEFAULT	NAME	HEX ADDRESS (SIZE)	DEFAULT
Input Current Limit	IIN_LIMIT_SETTING	0x15(5:0)	0x3F	IIN_LIMIT_DAC	0x46(5:0)	0x3F
Battery Charge Voltage	VCHARGE_SETTING	0x1B(5:0)[1]	0x3F	VCHARGE_DAC	0x45(5:0)	0x3F
Minimum Input Voltage (UVCL)	VIN_UVCL_SETTING	0x16(8:0)	0xFF	Scaled by External Resistors		
Battery Charge Current	ICHARGE_TARGET	0x1A(4:0)	0x1F	ICHARGE_DAC	0x44(4:0)	0x1F

[1] Lithium chemistries = 5b (4:0), lead-acid chemistry = 6b (5:0)

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effect when the input voltage drops below approximately 1V. Upon return of the input voltage above approximately 1V the LTC4015 wakes from ship mode and all registers reset to their initial default values. The decision to remain out of ship mode is latched once the voltage reference is re-biased and $INTV_{CC}$ is detected as having reached about 4.3V. Upon exiting ship mode, all internal registers are reset to their default values.

If the application requires that power be cut off from downstream system circuitry in SHIP MODE, a second external PMOS can optionally be added as shown in Figure 2. Unlike normal battery only mode, in ship mode the SYSM5 pin is driven to the SYS voltage to disable conduction through the second PMOS. This action cuts off power to the downstream system, thus minimizing battery drain between product manufacture and sale. If the application does not require the battery to be isolated from downstream devices, significant power savings in the LTC4015 may still be realized by activating ship mode without the second PMOS.

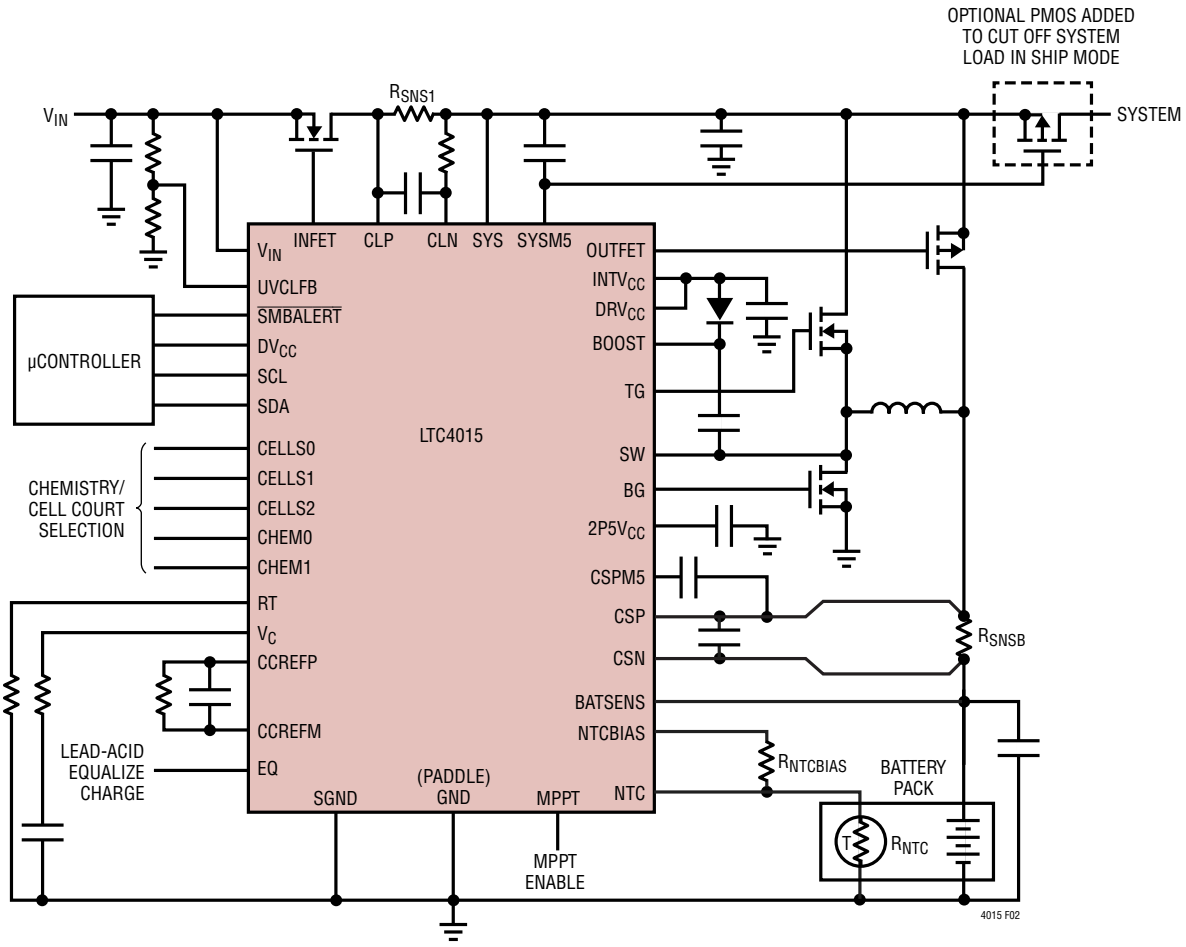

Figure 2. Typical Application with Optional PMOS Added for SHIP MODE Cutoff

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Cells Selection

Number of series cells selection is made using the CELLS2, CELLS1, and CELLS0 pins. For lithium chemistries the LTC4015 allows charging of up to nine series cells. For lead-acid there are only three valid selections 3, 6 or 12 cells corresponding to 6, 12, and 24V batteries respectively. Note that number of cells multiplied by their expected maximum cell voltage during charging cannot exceed V_{IN} – 200mV. With V_{IN}/V_{SYS} limited to 35V as an upper bound for V_{BAT}, at nine cells the maximum V/cell would be 3.89V. In practice the 3.89V/cell will be lower, due to several factors including; input ideal diode drop (V_{IN} – V_{SYS}) and switcher max duty cycle. These pins should be hard wired to GND(L), $INTV_{CC}$(H), or left open (Z). The LTC4015 does not monitor or balance individual cells – the full battery stack voltage is divided by number of cells (V/cell) for simplicity only. The 4015 is not a substitute for pack protection!

NUMBER OF CELLS	CELLS2	CELLS1	CELLS0
Invalid	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	L	L	Z
5	L	Z	L
6	L	H	Z
7	L	Z	H
8	L	Z	Z
9	H	L	L
Invalid	H	L	H
Invalid	H	H	L
12*	H	H	H

* Lead-acid only

Chemistry Selection

Chemistry selection is made using the CHEM1 and CHEM0 pins. These are three-state pins used by the LTC4015 to select of one of nine chemistry specific charging algorithms. These pins should be hard wired to GND(L), $INTV_{CC}$(H), or left open (Z).

CHEMISTRY	CHEM1	CHEM0
Li-Ion Programmable	L	L
Li-Ion 4.2V/Cell Fixed	H	H
Li-Ion 4.1V/Cell Fixed	L	Z
Li-Ion 4V/Cell Fixed	Z	L
$LiFePO_4$ Programmable	L	H
$LiFePO_4$ Fixed Fast Charge	H	Z
$LiFePO_4$ Fixed Standard Charge	Z	H
Lead-Acid Fixed	Z	Z
Lead-Acid Programmable	H	L

Li-Ion/$LiFePO_4$ Battery Charging

It is the responsibility of the user of the LTC4015 to consult with the battery manufacturer to determine the recommended charging parameters for a particular battery. Battery allowable temperature range while charging and any required charging parameter temperature coefficients also need to be considered.

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Li-Ion/Charging Parameters

Table 5 shows Li-Ion charging parameters. For Li-Ion programmable, defaults values are shown.

Bold parameters are I²C programmable in Li-Ion programmable mode only. ICHARGE_TARGET and VCHARGE_SETTING values are at 25°C if JEITA is enabled[1]. Shown in Figure 3 is an example of a Li-Ion battery charging profile. Shown in Table 6 are the Li-Ion programmable I²C configurable charging parameters.

Table 5. Li-Ion Charging Parameters

CHARGING ALGORITHM	ICHARGE_ TARGET	V_{CHARGE} (PER CELL)	CV TIMER TERM ENABLE	MAX CV TIME	C/x TERM ENABLE	C/x THRESH	JEITA	MAX CHARGE TIME	LOW BAT PRECHARGE CURRENT	LOW BAT THRESHOLD (PER CELL)
Li-Ion Programmable	**32mV/ R_{SNSB}[1]**	**4.20[1]**	**Yes**	**4 Hours**	**No**	**10%**	**Y**	**18 Hrs**	~10%[2]	2.9V
Li-Ion 4.2V/cell Fixed	32mV/ R_{SNSB}[1]	4.20[1]	Yes	4 Hours	No	–	Y	18 Hrs	~10%[2]	2.9V
Li-Ion 4.1V/cell Fixed	32mV/ R_{SNSB}[1]	4.10[1]	Yes	4 Hours	No	–	Y	18 Hrs	~10%[2]	2.9V
Li-Ion 4V/cell Fixed	32mV/ R_{SNSB}[1]	4.00[1]	Yes	4 Hours	No	–	Y	18 Hrs	~10%[2]	2.9V

Table 6. Li-Ion Programmable I²C Configurable Parameters

PROGRAMMABLE MODE PARAMETER	RANGE	BITS	RESOLUTION
ICHARGE_TARGET[1]	1mV to 32mV/ R_{SNSB}	5	1mV/R_{SNSB}
VCHARGE_SETTING[1]	3.8125V to 4.2V/Cell	5	12.5mV
MAX_CV_TIME	0 to 65535	16	1 Second
en_jeita	0, 1	1	1 = Enable
en_c_over_x_term	0, 1	1	1 = Enable
C_OVER_X_THRESHOLD	0mV to 32mV/ R_{SNSB}	16	1.465µV/R_{SNSB}
MAX_CHARGE_TIME	0 to 65535	16	1 Second

Notes

1) When JEITA is enabled (en_jeita=1), ICHARGE_TARGET and VCHARGE_SETTING are controlled by the JEITA temperature controlled charging algorithm, as described in the descriptions for ICHARGE_ JEITA_n and VCHARGE_JEITA_n.

2) Precharge current is 10% of ICHARGE_TARGET, rounded down to the next LSB.

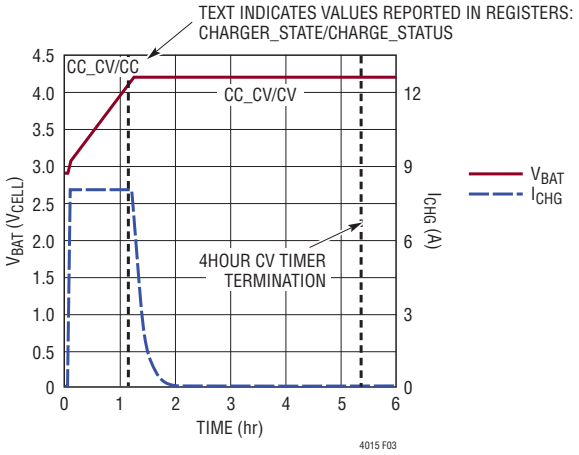

Figure 3. Li-Ion 4.2V/Cell Fixed Charging Profile