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40V 400mA Synchronous Step-Down Battery Charger

FEATURES

- **Wide Input Voltage Range: 4.4V to 40V**
- **Temperature Compensated Input Voltage Regulation for Maximum Power Point Tracking (MPPT)**
- **Adjustable Float Voltage 3.5V to 18V (LTC4121)**
- **Fixed 4.2V Float Voltage Option (LTC4121-4.2)**
- High Efficiency: Up to 95%
- 50mA to 400mA Programmable Charge Current
- ±1% Feedback Voltage Accuracy
- Programmable 5% Accurate Charge Current
- Thermally Enhanced, Low Profile (0.75mm) 16-Lead (3mm × 3mm) QFN Package

APPLICATIONS

- Handheld Instruments
- Solar Powered Devices
- Industrial/Military Sensors and Devices

DESCRIPTION

The LTC®4121 is a 400mA constant-current/constant-voltage (CC/CV) synchronous step-down battery charger. In addition to CC/CV operation, the LTC4121 regulates its input voltage to a programmable percentage of the input open-circuit voltage. This technique maintains maximum power transfer with high impedance input sources such as solar panels.

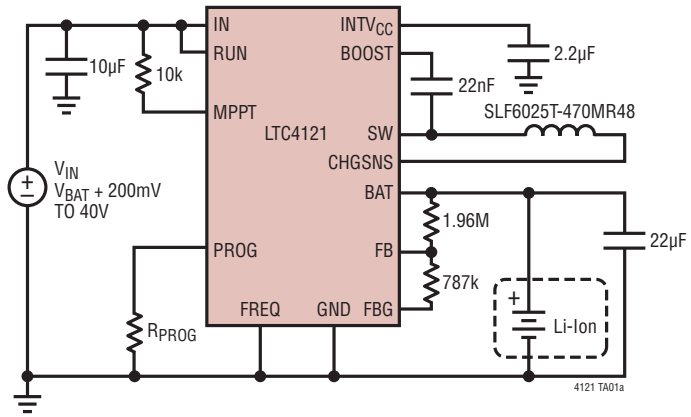
An external resistor programs the charge current up to 400mA. The LTC4121-4.2 is suitable for charging Li-Ion/Polymer batteries, while the programmable float voltage of the LTC4121 is suitable for several battery chemistries.

The LTC4121 and LTC4121-4.2 include an accurate RUN pin threshold, low voltage battery preconditioning and bad battery fault detection, timer termination, auto-recharge, and NTC temperature qualified charging. The $\overline{\text{FAULT}}$ pin provides an indication of bad battery or temperature faults.

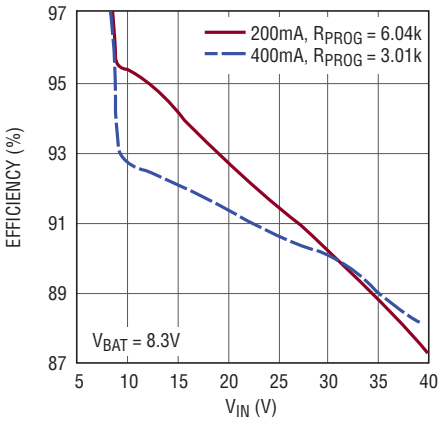
Once charging is terminated, the LTC4121 signals end-of-charge via the $\overline{\text{CHRG}}$ pin, and enters a low current SLEEP mode. An auto-restart feature starts a new charging cycle if the battery voltage drops by 2.2%.

TYPICAL APPLICATION

High Efficiency, Wide Input Voltage Range Charging with LTC4121



LTC4121 Efficiency vs V_{IN} at V_{FLOAT} = 8.4V



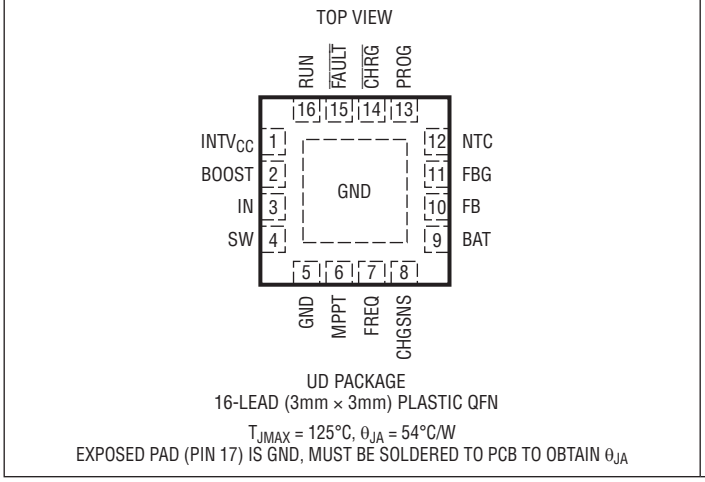
ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN, RUN, $\overline{CHRG}$, $\overline{FAULT}$, MPPT ..... –0.3V to 43V
BOOST ..... V_{SW} – 0.3V to (V_{SW} + 6V)
SW (DC) ..... –0.3V to (V_{IN} + 0.3V)
SW (Pulsed <100ns) ..... –1.5V to (V_{IN} + 1.5V)
CHGSNS, BAT, FB/BATSNS, FBG ..... –0.3V to 18V
FREQ, NTC, PROG, $INTV_{CC}$ ..... –0.3V to 6V
I_{CHGSNS}, I_{BAT} ..... ±600mA
$I_{\overline{CHRG}}$, $I_{\overline{FAULT}}$, ... ±5mA
I_{FB}, I_{FBG} (LTC4121) ..... ±5mA
I_{BATSNS} (LTC4121-4.2) ..... ±5mA
I_{INTVCC} ..... –5mA
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°

PIN CONFIGURATION

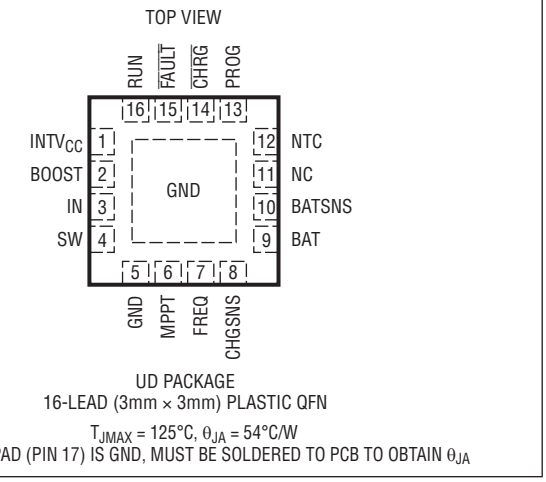
LTC4121



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 54°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB TO OBTAIN θ_{JA}

LTC4121-4.2



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 54°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB TO OBTAIN θ_{JA}

ORDER INFORMATION

(http://www.linear.com/product/LTC4121#orderinfo)

LTC4121 Options

PART NUMBER	FLOAT VOLTAGE
LTC4121	Programmable
LTC4121-4.2	4.2V Fixed

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4121EUD#PBF	LTC4121EUD#TRPBF	LGHC	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC4121IUD#PBF	LTC4121IUD#TRPBF	LGHC	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC4121EUD-4.2#PBF	LTC4121EUD-4.2#TRPBF	LGMV	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC4121IUD-4.2#PBF	LTC4121IUD-4.2#TRPBF	LGMV	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{RUN} = 15V, V_{CHGSNS} = V_{BAT} = 4V, R_{PROG} = 3.01k, V_{FB} = 2.29V (LTC4121), V_{BATSNS} = 4V (LTC4121-4.2). Current into a pin is positive out of a pin is negative. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Operating Input Supply Range		●	4.4		40	V
	Battery Voltage Range	LTC4121 (Note 3)		0		18	V
		LTC4121-4.2		0		4.2	V
I_{IN}	DC Supply Current	Switching: FREQ = GND			3.5		mA
		Standby Mode: (Note 4)	●		142	260	µA
		Sleep Mode: (Note 4) LTC4121-4.2: V_{BATSNS} = 4.4V LTC4121: V_{FB} = 2.51V (Note 6)	●		60	110	µA
		Disabled Mode: $V_{SD} < V_{RUN} < V_{EN}$ (Note 4)	●		37	80	µA
		Shutdown Mode: (Note 4)	●		20	40	µA
ΔV_{DUVLO}	Differential Undervoltage Lockout	$V_{IN} – V_{BAT}$ Falling, V_{IN} = 5V (LTC4121) $V_{IN} – V_{BATSNS}$ Falling, V_{IN} = 5V (LTC4121-4.2)	●	20	80	160	mV
	Hysteresis	$V_{IN} – V_{BAT}$ Rising, V_{IN} = 5V (LTC4121) $V_{IN} – V_{BATSNS}$ Rising, V_{IN} = 5V (LTC4121-4.2)			115		mV
UV_{INTVCC}	$INTV_{CC}$ Undervoltage Lockout (Note 5)	$INTV_{CC}$ Rising, V_{IN} = $INTV_{CC}$ + 100mV	●	4.00	4.15	4.26	V
	Hysteresis	$INTV_{CC}$ Falling			220		mV
Battery Charger							
I_{BAT}	BAT Standby Current	Standby Mode (LTC4121) (Notes 4, 8, 9) Standby Mode (LTC4121-4.2) (Notes 4, 8, 9)	● ●		2.5 50	4.5 1000	µA nA
	BAT Shutdown Current	Shutdown Mode (LTC4121) (Notes 4, 8, 9) Shutdown Mode (LTC4121-4.2) (Notes 4, 8, 9)	● ●		1100 10	2000 1000	nA nA
I_{BATSNS}	BATSNS Standby Current (LTC4121-4.2)	Standby Mode (Notes 4, 8, 9)	●		5.4	10	µA
	BATSNS Shutdown Current (LTC4121-4.2)	Shutdown Mode (Notes 4, 8, 9)	●		1100	2000	nA
I_{FB}	Feedback Pin Bias Current (LTC4121)	V_{FB} = 2.5V (Note 6)	●		25	60	nA
I_{FBG_LEAK}	Feedback Ground Leakage Current (LTC4121)	Shutdown Mode (Note 4)	●			1	µA
R_{FBG}	Feedback Ground Return Resistance (LTC4121)		●		1000	2000	Ω
$V_{FB(REG)}$	Feedback Pin Regulation Voltage (LTC4121)	(Note 6)		2.393	2.400	2.407	V
			●	2.370		2.418	V
V_{FLOAT}	Regulated Float Voltage (LTC4121-4.2)			4.188	4.200	4.212	V
			●	4.148		4.231	V
I_{CHG}	Battery Charge Current	R_{PROG} = 3.01k	●	383	402	421	mA
		R_{PROG} = 24.3k	●	45	50	55	mA
V_{RCHG}	Battery Recharge Threshold	V_{FB} Falling Relative to $V_{FB(REG)}$ (LTC4121)	●	–38	–49	–62	mV
$V_{RCHG\_4.2}$		V_{BATSNS} Falling Relative to V_{FLOAT} (LTC4121-4.2)	●	–70	–93	–114	mV
h_{PROG}	Ratio of BAT Current to PROG Current	$V_{TRKL} < V_{FB} < V_{FB(REG)}$ (LTC4121), $V_{TRKL\_42} < V_{BATSNS} < V_{FLOAT}$ (LTC4121-4.2)			988		mA/mA
V_{PROG}	PROG Pin Servo Voltage		●	1.206	1.227	1.248	V
R_{SNS}	CHGSNS-BAT Sense Resistor	I_{BAT} = –100mA			300		mΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{RUN} = 15V, V_{CHGSNS} = V_{BAT} = 4V, R_{PROG} = 3.01k, V_{FB} = 2.29V (LTC4121), V_{BATSNS} = 4V (LTC4121-4.2). Current into a pin is positive out of a pin is negative. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LOWBAT}	Low Battery Linear Charge Current	$V_{FB} < V_{TRKL}$, V_{BAT} = 2.6V (LTC4121) (Note 6)		6	9	16	mA
		$V_{BATSNS} < V_{TRKL\_4.2}$, V_{BAT} = 2.6V (LTC4121-4.2)					
V_{LOWBAT}	Low Battery Threshold Voltage	V_{BAT} Rising (LTC4121) V_{BATSNS} Rising (LTC4121-4.2)	●	2.15	2.21	2. 28	V
		Hysteresis			147		mV
I_{TRKL}	Switch Mode Trickle Charge Current	$V_{LOWBAT} < V_{BAT}$, $V_{FB} < V_{TRKL}$ (LTC4121) (Note 6)			I_{CHG}/10		mA
		$V_{LOWBAT} < V_{BATSNS} < V_{TRKL\_42}$ (LTC4121-4.2)					
	PROG Pin Servo Voltage in Trickle Charge	$V_{LOWBAT} < V_{BAT}$, $V_{FB} > V_{TRKL}$ (LTC4121) (Note 6)			122		mV
		$V_{LOWBAT} < V_{BATSNS} < V_{TRKL\_42}$ (LTC4121-4.2)					
V_{TRKL}	Trickle Charge Threshold (LTC4121)	V_{FB} Rising (Note 6)	●	1.65	1.68	1.71	V
	Hysteresis (LTC4121)	V_{FB} Falling (Note 6)			50		mV
$V_{TRKL\_4.2}$	Trickle Charge Threshold (LTC4121-4.2)	V_{BATSNS} Rising	●	2.86	2.91	2.98	V
	Hysteresis (LTC4121-4.2)	V_{BATSNS} Falling			88		mV
$h_{C/10}$	End of Charge Indication Current Ratio	(Note 7)			0.1		mA/mA
	Safety Timer Termination Period			1.3	2.0	2.8	hrs
	Bad Battery Termination Timeout			19	30	42	min
Switcher							
f_{OSC}	Switching Frequency	FREQ = $INTV_{CC}$	●	1.0	1.5	2.0	MHz
		FREQ = GND	●	0.5	0.75	1.0	MHz
t_{MIN_ON}	Minimum Controllable On-Time				120		ns
	Duty Cycle Maximum			94			%
	Top Switch R_{DSON}	I_{SW} = –100mA			0.8		Ω
	Bottom Switch R_{DSON}	I_{SW} = 100mA			0.5		Ω
I_{PEAK}	Peak Inductor Current Limit	Measured Across R_{SNS} with a 15µH Inductor in Series with R_{SNS} (Note 10)		585	1050	1250	mA
I_{SW}	Switch Pin Current (Note 9)	IN Open-Circuit, V_{BAT} = V_{SW} = 4.2V (LTC4121-4.2)	●		7	15	µA
		IN Open-Circuit, V_{BAT} = V_{SW} = 8.4V (LTC4121)	●		15	30	µA
Status Pins $\overline{FAULT}$, $\overline{CHRG}$							
	Pin Output Voltage Low	I = 2mA				550	mV
	Pin Leakage Current	V = 43V, Pin High-Impedance			0	1	µA
NTC							
	Cold Temperature V_{NTC}/V_{INTVCC} Fault	Rising V_{NTC} Threshold	●	73	74	75	%$INTV_{CC}$
		Falling V_{NTC} Threshold			72		%$INTV_{CC}$
	Hot Temperature V_{NTC}/V_{INTVCC} Fault	Falling V_{NTC} Threshold	●	35.5	36.5	37.5	%$INTV_{CC}$
		Rising V_{NTC} Threshold			37.5		%$INTV_{CC}$
	NTC Disable Voltage	Falling V_{NTC} Threshold	●	1	2	3	%$INTV_{CC}$
		Rising V_{NTC} Threshold			3		%$INTV_{CC}$
	NTC Input Leakage Current	V_{NTC} = V_{INTVCC}		–50		50	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{RUN} = 15V, V_{CHGSNS} = V_{BAT} = 4V, R_{PROG} = 3.01k, V_{FB} = 2.29V (LTC4121), V_{BATSNS} = 4V (LTC4121-4.2). Current into a pin is positive out of a pin is negative. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RUN							
V_{EN}	Enable Threshold	V_{RUN} Rising	●	2.35	2.45	2.55	V
	Hysteresis	V_{RUN} Falling			200		mV
	Run Pin Input Current	V_{RUN} = 40V			0.01	0.1	µA
V_{SD}	Shutdown Threshold	V_{RUN} Falling	●	0.4		1.2	V
	Hysteresis				220		mV
FREQ							
	FREQ Pin Input Low		●	0.4			V
	FREQ Pin Input High		●			3.6	V
	FREQ Pin Input Current	$0 < V_{FREQ} < V_{INTVCC}$				±1	µA
MPPT							
I_{MPPT}	MPPT Pin Leakage Current	V_{MPPT} = 4.2V	●		15	1000	nA
T_{MP}	MPPT Sample Period	Period Between Charger Disabled Events			28		s
PW_{MP}	MPPT Sample Pulse Width	Charger Disabled Pulse Width			36		ms
K_F	Internal Divider Gain	Internal DAC Voltage as a Ratio to V_{IN}		0.098	0.1	0.102	V/V
$V_{MP(OS)}$	MPPT Error Amp Gain Offset	$V_{MPPT} - V_{DAC}$, I_{BAT} = 50%• I_{CHG}		10	–45	–100	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4121 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4121E is guaranteed to meet performance specifications for junction temperatures from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4121I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

Note 3: If a battery voltage greater than 11V can be hot plugged to the LTC4121 a reverse blocking diode is required in series with the BAT pin to prevent large inrush current into the low impedance BAT pin.

Note 4: Standby mode occurs when the LTC4121/LTC4121-4.2 stops switching due to an NTC fault, MPPT pause, or when the charge current has dropped low enough to enter Burst Mode operation. Disabled mode occurs when V_{RUN} is between V_{SD} and V_{EN}. Shutdown mode occurs when V_{RUN} is below V_{SD} or when the differential undervoltage lockout is engaged. Sleep mode occurs after a timeout while the battery voltage remains above the V_{RCHG} or V_{RCHG_42} threshold.

Note 5: The internal supply $INTV_{CC}$ should only be used for the NTC divider, it should not be used for any other loads

Note 6: For the LTC4121, the FB pin is measured with a resistance of 588k in series with the pin.

Note 7: $h_{C/10}$ is expressed as a fraction of measured full charge current as measured at the PROG pin voltage when the $\overline{CHRG}$ pin de-asserts.

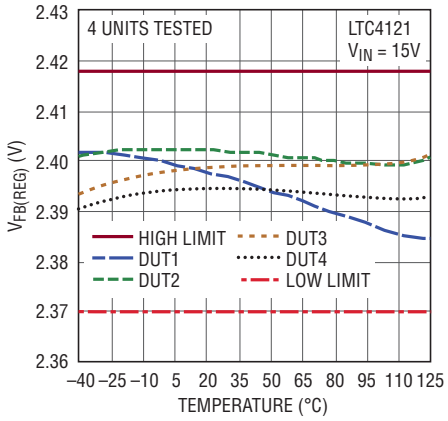
Note 8: In an application circuit with an inductor connected from SW to CHGSNS, the total battery leakage current when disabled is the sum of I_{BATSNS} and I_{SW} (LTC4121-4.2) or I_{BAT} and I_{FBG_LEAK} and I_{SW} (LTC4121).

Note 9: When no supply is present at IN, the SW powers IN through the body diode of the top side switch. This may cause additional SW pin current depending on the load present at IN.

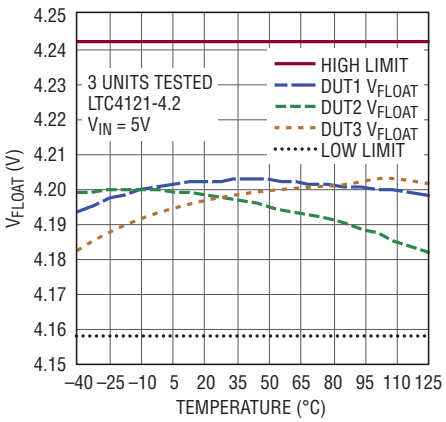
Note 10: Guaranteed by design and/or correlation to static test.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

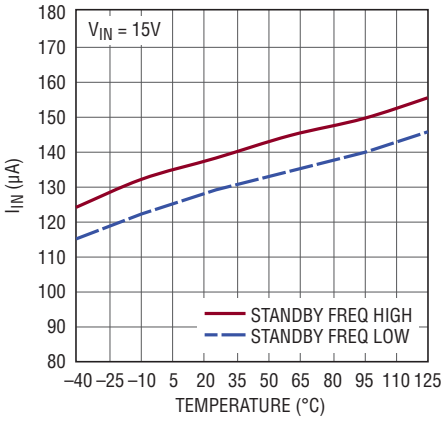
Typical $V_{FB(REG)}$ vs Temperature



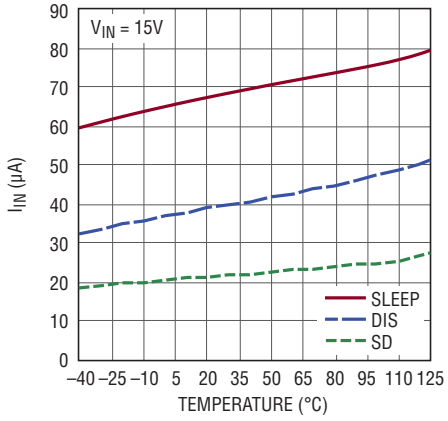
Typical V_{FLOAT} vs Temperature



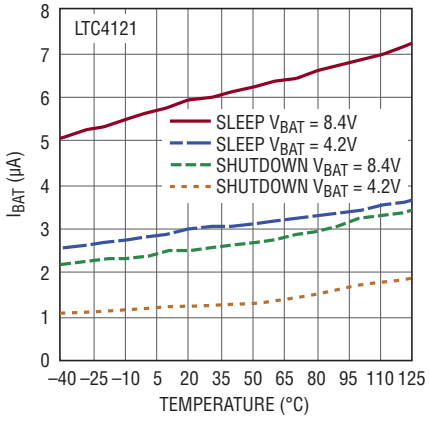
IN Pin Standby Current vs Temperature



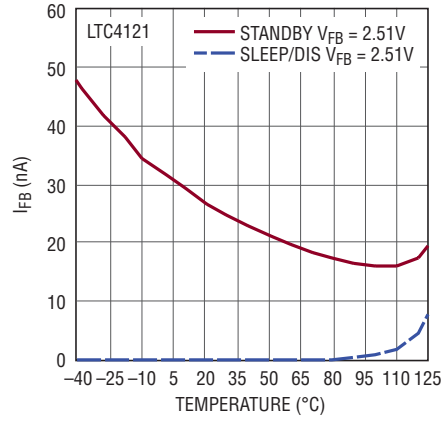
IN Pin Sleep/Disabled/Shutdown Current vs Temperature



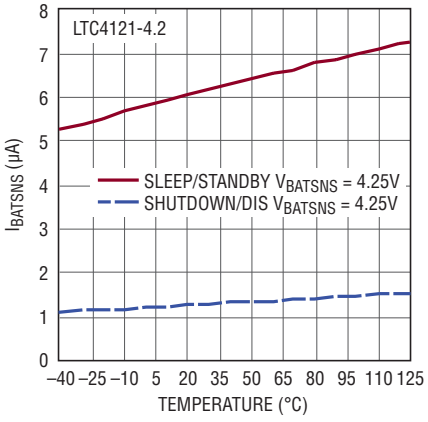
BAT Pin Sleep/Shutdown Current vs Temperature



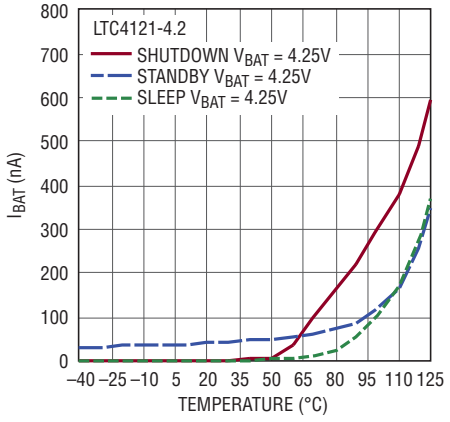
Feedback Pin Standby or Sleep/ Disabled Current vs Temperature



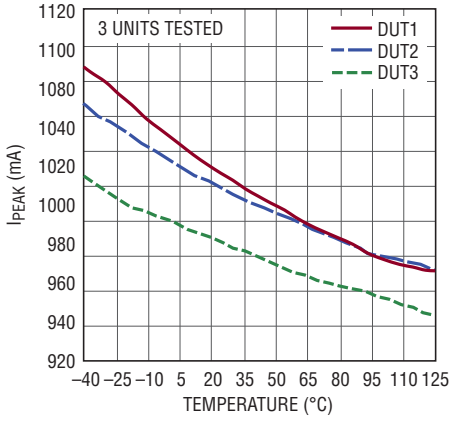
BATSNS Pin Sleep/Standby or Shutdown/Disabled Current vs Temperature



BAT Pin Standby/Sleep/Shutdown Current vs Temperature

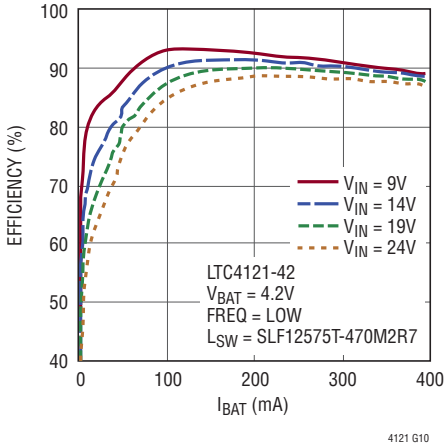


Typical R_{SNS} Current Limit I_{PEAK} vs Temperature

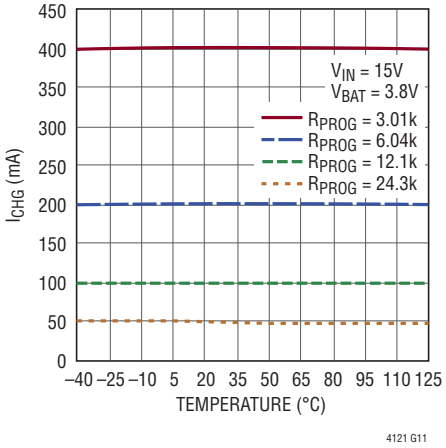


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

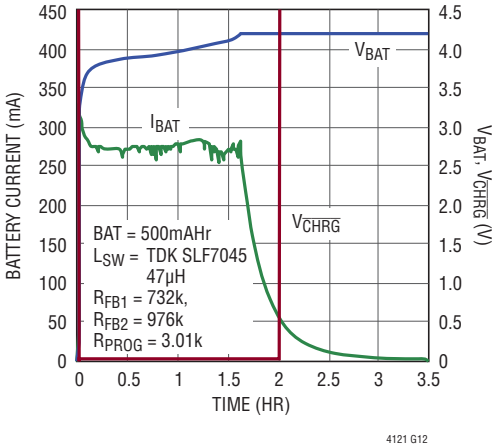
Efficiency vs I_{BAT}



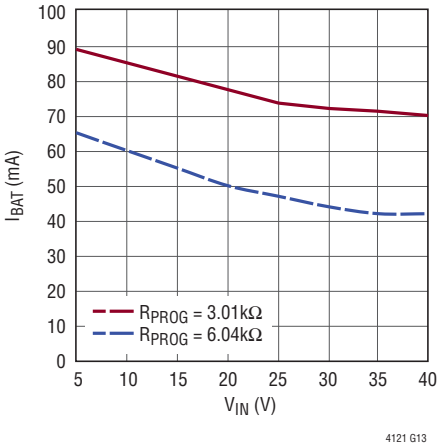
Typical Battery Charge Current vs Temperature



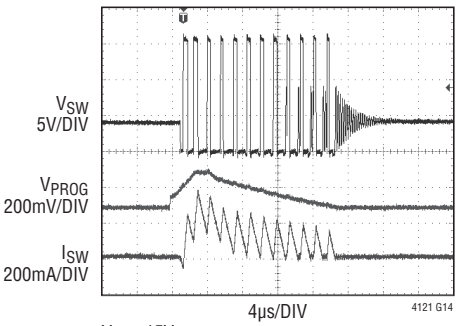
Typical Solar Charging Cycle



Burst Mode Trigger Current

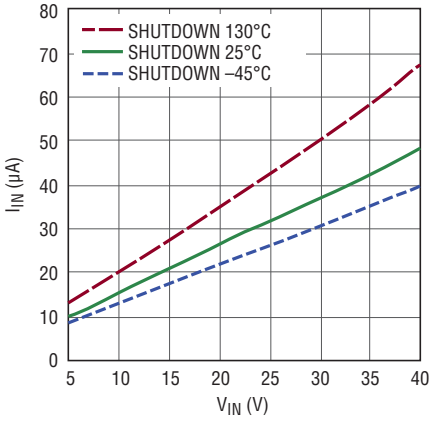


Typical Burst Mode Waveforms

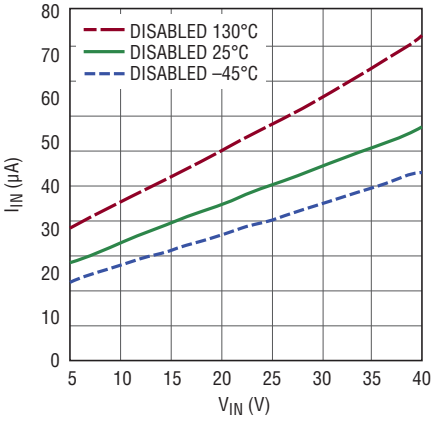


VIN = 15V
VBAT = 4.2V
IBAT = 38mA
FREQ = GND

IN Pin Shutdown Current vs Input Voltage

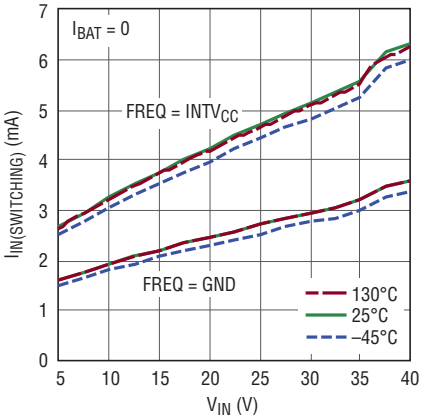


IN Pin Disabled Current vs Input Voltage

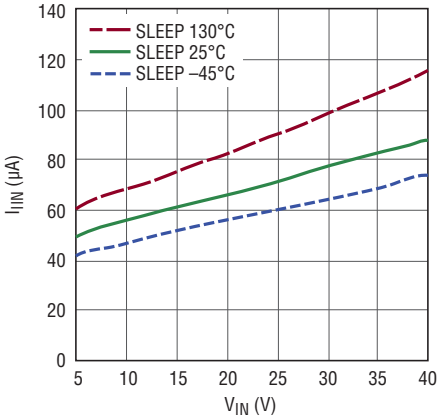


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

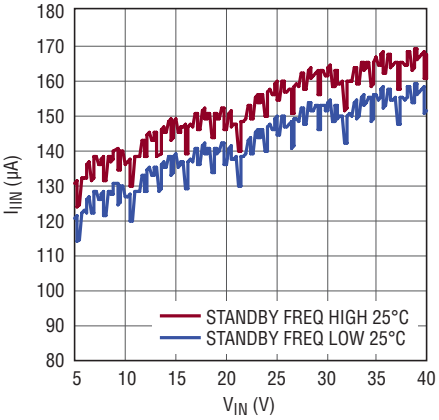
IN Pin Switching Current vs Input Voltage



IN Pin Sleep Current vs Input Voltage



IN Pin Standby Current vs Input Voltage



PIN FUNCTIONS

$INTV_{CC}$ (Pin 1): Internal Low Drop Out (LDO) Regulator Output Pin. This pin is the output of an internal linear regulator that generates the internal $INTV_{CC}$ supply from IN. It also supplies power to the switch gate drivers and the low battery linear charge current I_{LOWBAT}. Connect a 2.2µF low ESR capacitor from $INTV_{CC}$ to GND. Do not place any external load on $INTV_{CC}$ other than the NTC bias network. Overloading this pin can disrupt internal operation. When the RUN pin is above V_{EN}, and $INTV_{CC}$ rises above the UVLO threshold and IN rises above BAT by ΔV_{DUVLO} and its hysteresis, the charger is enabled.

BOOST (Pin 2): Boosted Supply Pin. Connect a 22nF boost capacitor from this pin to the SW pin.

IN (Pin 3): Positive Input Power Supply. Decouple to GND with a 10µF or larger low ESR capacitor. The input supply impedance and the input decoupling capacitor form an RC network that must settle during the MPPT sample pulse width of about 36ms. This allows the LTC4121 to sample the open-circuit voltage.

SW (Pin 4): Switch Pin. The SW pin delivers power from IN to BAT via the step-down switching regulator. An inductor should be connected from SW to CHGSNS. See the Applications Information section for a discussion of inductor selection.

GND (Pin 5, Exposed Pad Pin 17): Ground Pin. Connect to Exposed Pad. The Exposed Pad must be soldered to PCB GND to provide a low electrical and thermal impedance connection to ground.

MPPT (Pin 6): Maximum Power Point Tracking Pin. This pin is used to program an input voltage regulation loop. Connect an external resistive divider from V_{IN} to MPPT to GND. This divider programs the maximum power point voltage as percentage of the input open-circuit voltage. For more information on programming the MPPT resistive divider refer to the Application Information section. If the input voltage regulation feature is not used, connect MPPT to either $INTV_{CC}$ or IN with a minimum 10k resistor. Keep parasitic capacitance at the MPPT pin to a minimum as capacitance at this pin forms a pole that may interfere with switching regulator stability.

FREQ (Pin 7): Step-Down Regulator Switching Frequency Select Input Pin. Connect to $INTV_{CC}$ to select a 1.5MHz switching frequency or GND to select a 750kHz switching frequency. Do not float.

CHGSNS (Pin 8): Battery Charge Current Sense Pin. An internal current sense resistor between CHGSNS and BAT pins monitors battery charge current. An inductor should be connected from SW to CHGSNS.

PIN FUNCTIONS

BAT (Pin 9): Battery Output Pin. Battery charge current is delivered from this pin through the internal charge current sense resistor. In low battery conditions a small linear charge current, I_{LOWBAT}, is sourced from this pin to precondition the battery. Decouple the BAT pin with a low ESR 22µF ceramic capacitor to GND.

BATSNS (Pin 10, LTC4121-4.2 Only): Battery Voltage Sense Pin. For proper operation, this pin must always be connected physically close to the positive battery terminal.

FB (Pin 10, LTC4121 Only): Battery Voltage Feedback Reference Pin. The charge function operates to achieve a final float voltage of 2.4V at this pin. Battery float voltage is programmed using a resistive divider from BAT to FB to FBG, and can be programmed from 3.5V up to 18V. The feedback pin input bias current, I_{FB}, is 25nA. Using a resistive divider with a Thevenin equivalent resistance of 588k compensates for input bias current error.

FBG (Pin 11, LTC4121 Only): Feedback Ground Pin. This pin disconnects the external FB divider load from the battery when it is not needed. When sensing the battery voltage this pin presents a low resistance, R_{FBG}, to GND. When in disabled or shutdown modes this pin is high impedance.

NTC (Pin 12): Input to the Negative Temperature Coefficient Thermistor Monitoring Circuit. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, the LTC4121 enters STANDBY mode and charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from $INTV_{CC}$ to NTC and a thermistor is required from NTC to GND. Tie the NTC pin to GND, and omit the NTC resistive divider to disable NTC qualified charging if NTC functionality is not required.

PROG (Pin 13): Charge Current Program and Charge Current Monitor Pin. Connect a 1% resistor between 3.01k (400mA) and 24.3k (50mA) from PROG to ground to program the charge current. While in constant-current mode, this pin regulates to 1.227V. The voltage at this pin represents the average charge current using the following formula:

$$I_{CHG} = h_{PROG} \bullet \frac{V_{PROG}}{R_{PROG}}$$

where h_{PROG} is typically 988. Keep parasitic capacitance on the PROG pin to a minimum. If monitoring charge current via the voltage at the PROG pin add a series resistor of at least 2k to isolate stray capacitance from this node.

$\overline{\text{CHRG}}$ (Pin 14): Open-drain Charge Status Output Pin. Typically pulled up through a resistor to a reference voltage, the $\overline{\text{CHRG}}$ pin indicates the status of the battery charger. The pin can be pulled up to voltages as high as IN when disabled, and can sink currents up to 5mA when enabled. When the battery is being charged, the $\overline{\text{CHRG}}$ pin is pulled low. When the termination timer expires or the charge current drops below 10% of the programmed value, the $\overline{\text{CHRG}}$ pin is forced to a high impedance state.

$\overline{\text{FAULT}}$ (Pin 15): Open-drain Fault Status Output Pin. Typically pulled up through a resistor to a reference voltage, this status pin indicates fault conditions during a charge cycle. The pin can be pulled up to voltages as high as IN when disabled, and can sink currents up to 5mA when enabled. An NTC temperature fault causes this pin to be pulled low. A bad battery fault also causes this pin to be pulled low. If no fault conditions exist, the $\overline{\text{FAULT}}$ pin remains high impedance.

RUN (Pin 16): Run Pin. When RUN is pulled below V_{EN} and its hysteresis, the device is disabled. In disabled mode, battery charge current is zero and the $\overline{\text{CHRG}}$ and $\overline{\text{FAULT}}$ pins assume high impedance states. If the voltage at RUN is pulled below V_{SD}, the device is in SHUTDOWN mode. When the voltage at the RUN pin rises above V_{EN}, the $INTV_{CC}$ LDO turns on. When the $INTV_{CC}$ LDO rises above its UVLO threshold the charger is enabled. The RUN pin should be tied to a resistive divider from V_{IN} to program the input voltage at which charging is enabled. Do not float the RUN pin.

BLOCK DIAGRAM

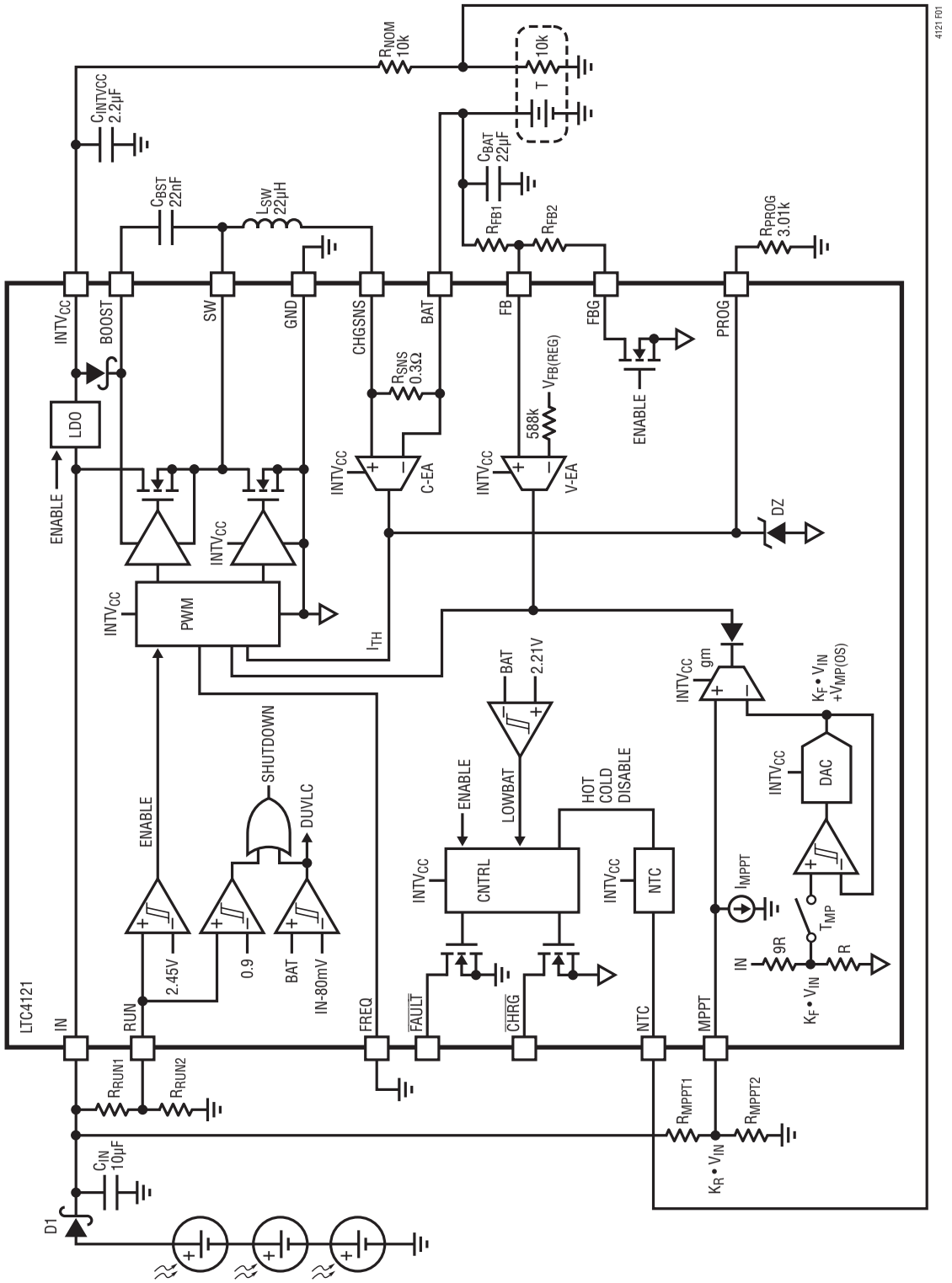


Figure 1. Block Diagram

BLOCK DIAGRAM

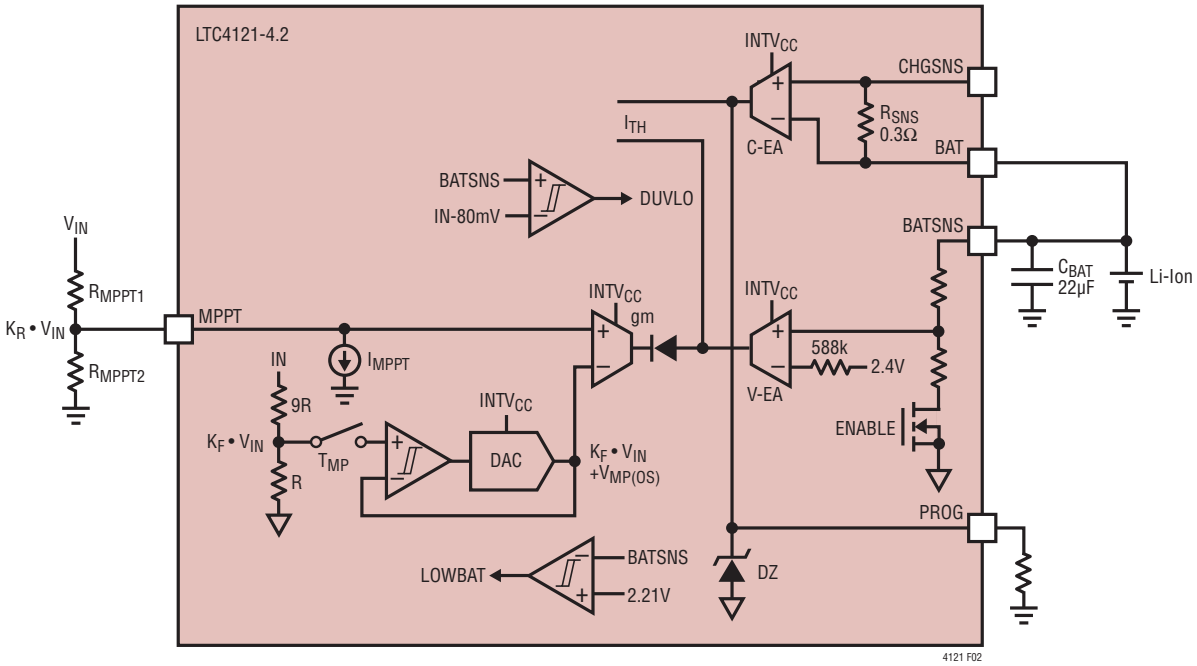


Figure 2. LTC4121-4.2 BATSNS Connections

OPERATION

Overview

The LTC4121 is a synchronous step-down (buck) monolithic battery charger with maximum power-point tracking (MPPT) control of the source voltage. The LTC4121/LTC4121-4.2 serves as a constant-current/constant-voltage battery charger with the following built-in charger functions: programmable charge current, battery precondition with ½ hour timeout, precision shutdown/run control, NTC thermal protection, a 2-hour safety termination timer, and automatic recharge. The LTC4121/LTC4121-4.2 also provides output pins to indicate state of charge and fault status.

Maximum Power Point Tracking

The LTC4121 employs an MPPT algorithm that compares a stored open-circuit input voltage measurement against the instantaneous input voltage while charging. The LTC4121 automatically reduces the charge current if the input voltage falls below the user defined percentage of the open-circuit voltage. This algorithm lets the LTC4121 optimize power transfer for a variety of different input sources including first order temperature compensation of a solar panel.

The LTC4121 periodically pauses charging to measure the open-circuit voltage allowing the LTC4121 to track fluctuations in the available power. About once every 30 seconds the LTC4121 pauses charging and waits about 36ms (PW_{MP}) for the input voltage to recover to its open-circuit potential. At the end of this recovery time, the LTC4121 samples the input voltage divided by 10 ($1/K_F$), and stores this value on a digital to analog converter (DAC). When charging resumes, the DAC voltage is compared against the MPPT pin voltage that is programmed with a resistive divider. If the MPPT voltage falls below the DAC voltage, the charge current is reduced to regulate the input voltage at that level. This regulation loop serves to maintain the input voltage at or above a user defined level that corresponds to the peak power available from the applied source.

A timing diagram illustrating the sampling of the open-circuit voltage is shown below. The charge current drops to zero and the LTC4121 waits PW_{MP} and then samples the open-circuit voltage. When charging resumes the input voltage collapses if the source cannot support the demanded charge current. When the input voltage drops to V_{MP}, the charge current is reduced so as to maintain V_{IN} at V_{MP}.

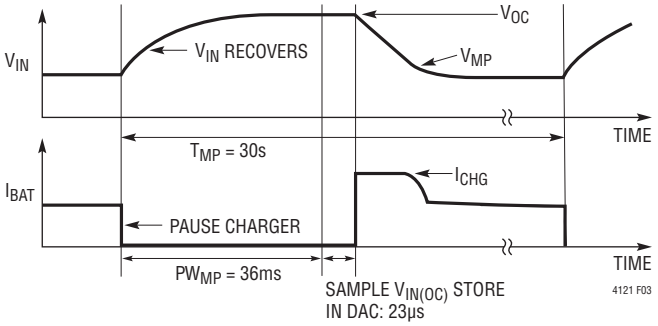


Figure 3. MPPT Timing Diagram

Connect the MPPT pin to a resistive input voltage divider, as shown in Figure 4, to program the fraction (K_R) of the input voltage where the input voltage regulation loop reduces available charge current. The LTC4121 reduces charge current if the MPPT pin voltage falls below the fixed fraction (K_F) of the open-circuit voltage (V_{OC}). The ratio of (K_F/K_R) defines the maximum power voltage (V_{MP}) of the applied power source as a ratio to the open-circuit voltage (V_{OC}) following the relation:

$$\frac{V_{MP}}{V_{OC}} = \frac{K_F}{K_R} = \frac{0.1}{K_R} = \frac{0.1 \bullet (R_{MPPT1} + R_{MPPT2})}{R_{MPPT2}}$$

where the MPPT pin resistive divider gain is $K_R = R_{MPPT2}/(R_{MPPT1} + R_{MPPT2})$. These equations can be rearranged to solve for R_{MPPT2} in terms of K_F (0.1) and the maximum power voltage divided by the open circuit voltage, (V_{MP}/V_{OC}) as:

$$R_{MPPT2} = \frac{0.1}{\left(\frac{V_{MP}}{V_{OC}}\right) - 0.1} \bullet R_{MPPT1}$$

This function serves to maintain the input voltage at or above the peak power voltage while the LTC4121 charges a battery.

Because MPPT operation involves large changes of input voltage, it is important to ensure that the programmed maximum power voltage does not violate minimum input operating conditions: 4.4V or 160mV above the battery voltage, whichever is higher.

OPERATION

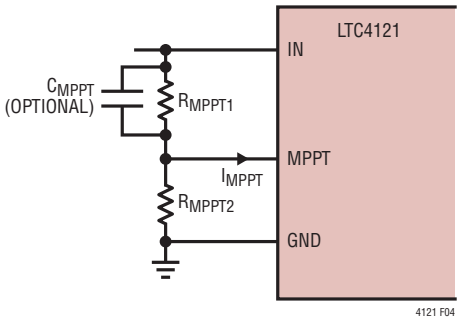


Figure 4. MPPT Resistive Divider

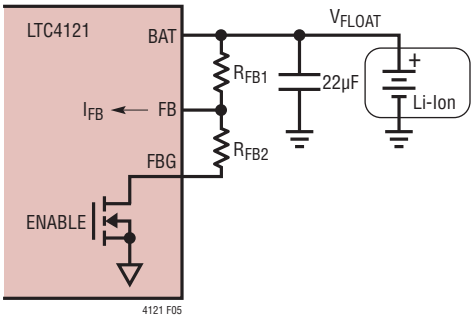


Figure 5. Programming the Float Voltage with LTC4121

When no power source is applied to V_{IN}, for example when using a solar panel source and the panel is in the dark, the MPPT pin divider drains power from the battery through the body diode of the top side switch of the switching regulator. To eliminate this leakage path, the MPPT divider may be connected to the anode of the Schottky diode that is in series with the panel, for examples see Figures 1, 9, or 10.

For example, consider charging a battery from a source with an open-circuit voltage of 30V and a source impedance of 120Ω. This resistive supply has a short circuit current of 250mA, and the peak available power of 1.875W occurs with a load of 125mA at 50% of V_{OC}. To program the LTC4120 to optimize the available power for this source simply program V_{MP}/V_{OC} to 50% by selecting the MPPT resistive divider gain $K_R = 0.2$. This is obtained with a resistive divider as shown in Figure 4 with $R_{MPPT2} = R_{MPPT1}/4$. With standard 1% resistors this is approximated with R_{MPPT1} = 402k, and R_{MPPT2} = 100k.

If the MPPT pin sees excess capacitance to GND, this may affect switching regulator stability. In such cases, one may optionally add a 50pF to 150pF lead capacitor (C_{MPPT}) as shown in Figure 4.

The sampling of V_{OC} is done at an extremely low duty cycle so as to have minimum impact on the average charge current. The time between sample events, T_{MP}, is typically about 30 seconds, with an idle time, PW_{MP}, of about 36ms to allow the source to recover to its open-circuit voltage through the time constant associated with the input decoupling capacitor C_{IN}. The time constant for the source to recover to its open-circuit voltage must be kept below the idle period. Limit the input capacitor to 10µF to avoid increasing the source recovery time.

Programming the Battery Float Voltage

For the LTC4121, the battery float voltage is programmed by placing a resistive divider from the battery to FB and FBG as shown in Figure 5. The battery float voltage is programmable anywhere from 3.5V up to 18V. The programmable battery float voltage, V_{FLOAT}, is then governed by the following equation:

$$V_{FLOAT} = V_{FB(REG)} \bullet \frac{(R_{FB1} + R_{FB2})}{R_{FB2}}$$

where $V_{FB(REG)}$ is typically 2.4V.

Due to the input bias current (I_{FB}) of the voltage error amp (V-EA), care must also be taken to select the Thevenin equivalent resistance of $R_{FB1}//R_{FB2}$ close to 588kΩ. Start by calculating R_{FB1} to satisfy the following relations:

$$R_{FB1} = \frac{V_{FLOAT} \bullet 588k}{V_{FB(REG)}}$$

Find the closest 0.1% or 1% resistor to the calculated value. With R_{FB1} calculate:

$$R_{FB2} = \frac{V_{FB(REG)} \bullet R_{FB1}}{V_{FLOAT} - V_{FB(REG)}} - 1000\Omega$$

Where 1000Ω represent the typical value of R_{FBG}. This is the resistance of the FBG pin which serves as the ground return for the battery float voltage divider.

Once R_{FB1} and R_{FB2} are selected re-calculate the value of V_{FLOAT} obtained with the resistors available. If the error

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is too large substitute another standard resistor value for R_{FB1} and recalculate R_{FB2}. Repeat until the float voltage error is acceptable.

Table 1 and Table 2 below list recommended standard 0.1% and 1% resistor values for common battery float voltages.

Table 1. Recommended 0.1% Resistors for Common V_{FLOAT}

V_{FLOAT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	TYPICAL ERROR (%)
3.6	887	1780	–0.13
4.1	1010	1420	0.15
4.2	1010	1350	–0.13
7.2	1800	898	0.08
8.2	2000	825	0.14
8.4	2050	816	0.27

Table 2 Recommended 1% Resistors for Common V_{FLOAT}

V_{FLOAT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	TYPICAL ERROR (%)
3.6	887	1780	–0.13
4.1	1000	1430	0.26
4.2	1020	1370	–0.34
7.2	1780	887	0.16
8.2	2000	825	0.14
8.4	2100	845	–0.50

Programming the Charge Current

The current-error amp (C-EA) measures the current through an internal 0.3Ω current sense resistor between the CHGSNS and BAT pins. The C-EA outputs a fraction of the charge current, $1/h_{PROG}$, to the PROG pin. The voltage-error amp (V-EA) and PWM control circuitry can limit the PROG pin voltage to control charge current. An internal clamp (DZ) limits the PROG pin voltage to V_{PROG}, which in turn limits the charge current to:

$$I_{CHG} = \frac{h_{PROG} \bullet V_{PROG}}{R_{PROG}} = \frac{1212V}{R_{PROG}}$$

$$I_{CHG\_TRKL} = \frac{120V}{R_{PROG}}$$

where h_{PROG} is typically 988, V_{PROG} is either 1.227V or 122mV during trickle charge, and R_{PROG} is the resistance of the grounded resistor applied to the PROG pin. The PROG resistor sets the maximum charge current, or the current delivered while the charger is operating in constant-current (CC) mode.

Analog Charge Current Monitor

The PROG pin provides a voltage signal proportional to the actual charge current. Care must be exercised in measuring this voltage as any capacitance at the PROG pin forms a pole that may cause loop instability. If observing the PROG pin voltage, add a series resistor of at least 2k and limit stray capacitance at this node to less than 50pF.

In the event that the input voltage cannot support the demanded charge current, the PROG pin voltage may not represent the actual charge current. In cases such as this, the PWM switch frequency drops as the charger enters dropout operation where the top switch remains on for more than one clock cycle as the inductor current attempts to ramp up to the desired current. If the top switch remains on in dropout for 8 clock cycles a dropout detector forces the bottom switch on for the remainder of the 8th cycle. In such a case, the PROG pin voltage remains at 1.227V, but the charge current may not reach the desired level.

NTC Thermal Battery Protection

The LTC4121 monitors battery temperature using a thermistor during the charging cycle. If the battery temperature moves outside a safe charging range, the IC suspends charging and signals a fault condition until the tempera-

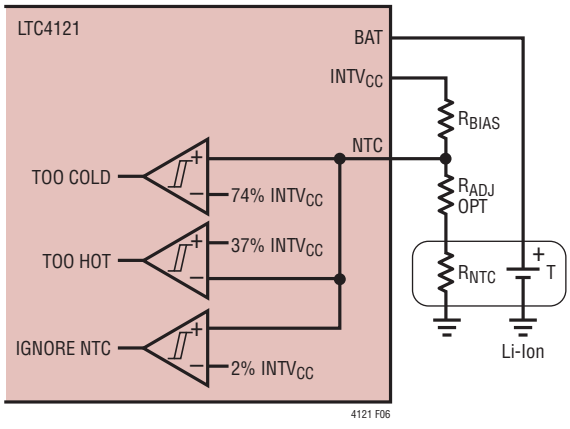

Figure 6. NTC Connection

OPERATION

ture returns to the safe charging range. The safe charging range is determined by two comparators that monitor the voltage at the NTC pin. NTC qualified charging is disabled if the NTC pin is pulled below about 85mV (V_{DIS}).

Thermistor manufacturers usually include either a temperature lookup table identified with a characteristic curve number, or a formula relating temperature to the resistor value. Each thermistor is also typically designated by a thermistor gain value B25/85.

The NTC pin should be connected to a voltage divider from $INTV_{CC}$ to GND as shown in Figure 6. In the simple application (R_{ADJ} = 0) a 1% resistor, R_{BIAS}, with a value equal to the resistance of the thermistor at 25°C is connected from $INTV_{CC}$ to NTC, and a thermistor is connected from NTC to GND. With this setup, the LTC4121 pauses charging when the resistance of the thermistor increases to 285% the R_{BIAS} resistor as the temperature drops. For a Vishay Curve 2 thermistor with B25/85 = 3490 and 25°C resistance of 10kΩ, this corresponds to a temperature of about 0°C. The LTC4121 also pauses charging if the thermistor resistance decreases to 58.8% of the R_{BIAS} resistor. For the same Vishay Curve 2 thermistor, this corresponds to approximately 40°C. With a Vishay Curve 2 thermistor, the hot and cold comparators both have about 2°C of hysteresis to prevent oscillations about the trip points. The NTC comparator trip points are ratio metric to the $INTV_{CC}$ voltage, so NTC trip points are defined as a percentage of $INTV_{CC}$. The HOT threshold is calculated as 285%/385% = 74% of $INTV_{CC}$ and the COLD threshold is calculated as 58.8%/158% = 37% of $INTV_{CC}$.

The hot and cold trip points may be adjusted using a different type of thermistor, or a different R_{BIAS} resistor, or by adding a desensitizing resistor, R_{ADJ}, or by a combination of these measures as shown in Figure 6. For example, by increasing R_{BIAS} to 12.4kΩ, with the same thermistor as before, the cold trip point moves down to –5°C, and the hot trip point moves down to 34°C. If a Vishay Curve 1 thermistor with B25/85 = 3964 and resistance of 100kΩ at 25°C is used, a 1% R_{BIAS} resistor of 118kΩ and a 1% R_{ADJ} resistor of 12.1kΩ results in a cold trip point of 0°C, and a hot trip point of 39°C.

End-of-Charge Indication and Safety Timeout

The LTC4121 uses a safety timer to terminate charging. Whenever the LTC4121 is in constant current mode the timer is paused, and when FB rises or falls through the V_{RCHG} threshold the timer is reset. When the battery voltage reaches the float voltage, the safety timer begins counting down a 2-hour timeout. If charge current falls below one tenth of the programmed maximum charge current ($h_{C/10}$), the $\overline{CHRG}$ status pin rises, but top-off charge current continues to flow until the timer finishes. After the timeout, the LTC4121 enters a low-power sleep mode.

Automatic Recharge

In sleep mode, the IC continues to monitor battery voltage. If the battery falls 2.2% (V_{RCHG} or V_{RCHG_42}) from the full-charge float voltage, the LTC4121 engages an automatic recharge cycle as the safety timer is reset. Automatic recharge has a built in delay of about 0.5ms to prevent triggering a new charge cycle if a load transient causes the battery voltage to drop temporarily.

State of Charge and Fault Status Pins

The LTC4121 contains two open-drain outputs which provide charge status and signal fault indications. The $\overline{CHRG}$ pin pulls low to indicate charging at a rate higher than C/10. The $\overline{FAULT}$ pin pulls low to indicate a bad battery timeout, or to indicate an NTC thermal fault condition. During NTC faults the $\overline{CHRG}$ pin remains low, but when a bad-battery timeout occurs the $\overline{CHRG}$ pin de-asserts. When the open drain outputs are pulled up with a resistor, Table 3 summarizes the charger state that is indicated by the pin voltages.

Table 3 LTC4121 Open-Drain Indicators with Resistor Pull-Ups

$\overline{FAULT}$	$\overline{CHRG}$	CHARGER STATE
High	High	Off or Topping-Off Charge at a Rate Less Than C/10.
High	Low	Charging at Rate Higher Than C/10
Low	High	Bad Battery Fault
Low	Low	NTC Thermal Fault, Charging Paused

Low Battery Voltage Operation

The LTC4121 automatically preconditions heavily discharged batteries. If the battery voltage is below V_{LOWBAT} minus its hysteresis (typically 2.05V - e.g. battery pack

OPERATION

protection has been engaged) a DC current, I_{LOWBAT}, is applied to the BAT pin from the $INTV_{CC}$ supply. When the battery voltage rises above V_{LOWBAT}, the switching regulator is enabled and charges the battery at a trickle charge level of 10% of the full scale charge current (in addition to the DC I_{LOWBAT} current). Trickle charging of the battery continues until the sensed battery voltage rises above the trickle charge threshold, V_{TRKL}, or V_{TRKL_42}. When the battery rises above the trickle charge threshold the full scale charge current is applied and the DC trickle charge current is turned off. If the battery remains below the trickle charge threshold for more than 30 minutes, charging terminates and the fault status pin is asserted to indicate a bad battery. After a bad battery fault, the LTC4121 automatically restarts a new charge cycle once the failed battery is removed and replaced with another battery. The LTC4121-4.2 monitors the BATSNS pin voltage to sense LOWBAT and TRKL conditions.

Precision Run/Shutdown Control

The LTC4121 remains in a low power disabled mode until the RUN pin is driven above V_{EN} (typically 2.45V). While the LTC4121 is in disabled mode, current drain from the battery is reduced to extend battery lifetime, the status pins are both de-asserted, and the FBG pin is high impedance. Charging can be stopped at any time by pulling the RUN pin below 2.25V. The LTC4121 also offers an extremely low operating current shutdown mode when the RUN pin is pulled below V_{SD} (typically about 0.7V). In this condition less than 20µA is pulled from the supply at IN. Tie the RUN pin to a resistive divider from the IN supply to program the voltage where the LTC4121 turns on. Examples are shown in Figures 9 and 10.

Differential Under Voltage Lockout

The LTC4121 monitors the difference between the battery voltage, V_{BAT}, and the input supply voltage, V_{IN}. If the difference ($V_{IN} – V_{BAT}$) falls to ΔV_{DUVLO}, all functions are disabled and the part is forced into shutdown mode until ($V_{IN} – V_{BAT}$) rises above the ΔV_{DUVLO} rising threshold. The LTC4121-4.2 monitors the V_{BATSNS} and V_{IN} pin voltages to sense DUVLO condition.

User Selectable Switching Regulator Operating Frequency

The LTC4121 uses a constant-frequency synchronous step-down switching regulator architecture to produce high operating efficiency. The nominal operating frequency, f_{OSC}, is programmed by pulling the FREQ pin to either $INTV_{CC}$ or to GND to obtain a switching frequency of 1.5MHz or 750kHz, respectively. The high operating frequency allows the use of smaller external components.

Selection of the operating frequency is a trade-off between efficiency, component size, and margin from the minimum on-time of the switcher. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses, but requires larger inductance values to maintain low output ripple. Operation at higher frequency allows the use of smaller components, but may require sufficient margin from the minimum on-time at the lowest duty cycle if fixed-frequency switching is required.

PWM Dropout Detector

If the input voltage approaches the battery voltage, the LTC4121 may require duty cycles approaching 100%. This mode of operation is known as dropout. In dropout, the operating frequency may fall well below the programmed f_{OSC} value. If the top switch remains on for eight clock cycles, the dropout detector activates and forces the bottom switch on for the remainder of that clock cycle or until the inductor current decays to zero. This avoids a potential source of audible noise when using ceramic input or output capacitors and prevents the boost supply capacitor for the top gate drive from discharging. In dropout operation, the actual charge current may not be able to reach the full-scale programmed value. In such a scenario the analog charge current monitor function does not represent actual charge current being delivered.

Burst Mode® Operation

At low charge currents, for example during constant-voltage mode, the LTC4121 automatically enters Burst Mode operation. In Burst Mode operation the switcher is periodically forced into standby mode in order to improve

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efficiency. The LTC4121 automatically enters Burst Mode operation after it exits constant-current (CC) mode and as the charge current drops below about 80mA. Burst Mode operation is triggered at lower currents for larger PROG resistors, and depends on the input supply voltage, the battery voltage, and the selected inductor. Refer to the Burst Mode Trigger Current and Typical Burst Mode Waveforms graphs in the Typical Performance Characteristics section for more information on Burst Mode operation. Burst Mode operation has some hysteresis and remains engaged for battery current up to about 150mA, depending on L_{SW}, V_{IN} and V_{BAT}. When operating in Burst Mode, the PROG pin voltage to average charge current relationship is not well defined. This may cause the $\overline{CHRG}$ pin to de-assert early depending on the amplitude of the burst ripple.

Boost Supply Refresh

The BOOST supply for the top gate drive in the LTC4121 switching regulator is generated by bootstrapping the BOOST flying capacitor to $INTV_{CC}$ whenever the bottom switch is turned on. This technique provides a voltage of $INTV_{CC}$ from the BOOST pin to the SW pin. In the event that the bottom switch remains off for a prolonged period of time, e.g. during Burst Mode operation, the BOOST supply may require a refresh. Similar to the PWM dropout timer, the LTC4121 counts the number of clock cycles since the last BOOST refresh. When this count reaches 32 the next PWM cycle begins by turning on the bottom side switch first. This pulse refreshes the BOOST flying capacitor to $INTV_{CC}$ and ensures that the top-side gate driver has sufficient voltage to turn on the top side switch at the beginning of the next cycle.

Operation without an Input Supply or Shaded Panel

When a battery is the only available power source, care should be taken to eliminate loading of the IN pin. Load current on IN drains the battery voltage through the body diode of the top side power switch as V_{IN} falls below V_{SW}. A diode inserted in series with the solar panel, as shown on the front page schematic, eliminates this discharge path. Alternatively, a diode may be placed in series with the BAT pin (as shown in Figure 8).

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MPPT Programming

The maximum power-point tracking loop is programmed by selecting a resistive divider from IN to MPPT to GND as shown in Figure 4. This user programmable voltage divider (K_R) serves to define a fraction of the input voltage that appears at the MPPT pin:

$$K_R = \frac{R_{MPPT2}}{R_{MPPT1} + R_{MPPT2}} = \frac{V_{MPPT}}{V_{IN}}$$

This fraction of V_{IN} is continuously compared against a fixed fraction of the open-circuit input voltage that is stored within the LTC4121. A fixed internal resistive divider ($0.1 \bullet V_{IN}$) is periodically sampled to compare the open-circuit input voltage against the user defined fraction of the loaded input voltage ($K_R \bullet V_{IN}$). On an interval of T_{MP}, the LTC4121 turns off all charger functions reverting to STANDBY mode. The LTC4121 then waits for a delay, of about 36ms, PW_{MP}, after turning off the charge current to allow the input supply to recover to its open-circuit voltage. Finally, the LTC4121 samples the open-circuit input voltage V_{OC} through a fixed internal divider; K_F = 1/10. After sampling the open-circuit voltage, the LTC4121 turns on all functions and reverts to normal operation. During normal operation, the stored $0.1 \bullet V_{OC}$ voltage is compared against the instantaneous MPPT pin voltage: $K_R \bullet V_{IN}$. If the MPPT voltage falls below the stored level, the charge current is reduced to maintain the input voltage. The ratio of $0.1/K_R$ defines the percentage below the open-circuit voltage where charge current is reduced to maintain the maximum input power.

Because MPPT operation involves large changes of input voltage, it is important to ensure that the programmed maximum power voltage does not violate minimum input operating conditions: 4.4V or 160mV above the battery voltage, whichever is higher.

For example, to select an MPPT set point, V_{MP}, at 75% of the open-circuit voltage, V_{OC}, select ratio K_R using the following relation:

$$K_R = \frac{K_F}{75\%} = \frac{0.1}{0.75} = 0.1333$$

Using the schematic of Figure 4, this ratio is obtained by selecting:

$$R_{MPPT1} = \frac{1 - \left(\frac{K_F}{75\%}\right)}{\left(\frac{K_F}{75\%}\right)} \bullet R_{MPPT2}$$

$$R_{MPPT1} = 6.5 \bullet R_{MPPT2}$$

Using standard 1% resistors, this is obtained with:

R_{MPPT1} = 787k and R_{MPPT2} = 121k.

MPPT Error Terms

Uncertainty in programming the MPPT set point is bound by three error terms: MPPT pin leakage, DAC quantization error, and the finite offset error in the MPPT error amp. All error terms are lumped into $V_{MP(OS)}$, with a typical value of –45mV. This offset at the input to the MPPT error amp is multiplied by $1/K_R$ when observed at the IN regulation point, V_{MP}.

For example, with the same K_R = 0.1333 (R_{MPPT1} = 787k and R_{MPPT2} = 121k) the –45mV $V_{MP(OS)}$ error gets amplified to –45mV/0.1333 = –338mV at V_{IN} from the V_{MP} set point of 75% of V_{OC}. If V_{OC} is 30V, the minimum V_{MP} regulation point is about 22.16V, or 73.9% of the open-circuit voltage.

For solar panel sources, the available power drops off quickly on the high side, and relatively slowly on the low side, this is illustrated in the curve in Figure 7. For these types of sources, it is usually better to err on the low side when programming the V_{MP} voltage. This is what the LTC4121 does normally, so most users can simply design for a V_{MP} voltage at (or just below) the level specified by the solar panel manufacturer. For more information on solar panels, refer to the panel's data sheet.

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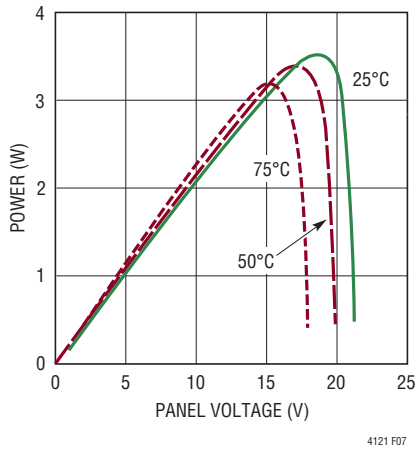

Figure 7. Typical 3W Panel Power vs Voltage

Input Voltage and Minimum On-Time

The LTC4121 maintains constant frequency operation under most operating conditions. Under certain situations with high input voltage and high switching frequency selected and a low battery voltage, the LTC4121 may not be able to maintain constant frequency operation. These factors, combined with the minimum on-time of the LTC4121, impose a minimum limit on the duty cycle to maintain fixed-frequency operation. The on-time of the top switch is related to the duty cycle (V_{BAT}/V_{IN}) and the switching frequency, f_{OSC} in Hz:

$$t_{ON} = \frac{V_{BAT}}{f_{OSC} \bullet V_{IN}}$$

When operating from a high input voltage with a low battery voltage, the PWM control algorithm may attempt to enforce a duty cycle which requires an on-time lower than the LTC4121 minimum, $t_{MIN(ON)}$. This minimum duty cycle is approximately 18% for 1.5MHz operation or 9% for 750kHz operation. If this occurs, the charge current and battery voltage remains in regulation, but the switching duty cycle may not remain fixed, or the switching frequency may decreases to an integer fraction of its programmed value.

The maximum input voltage allowed to maintain constant frequency operation is:

$$V_{IN(MAX)} = \frac{V_{LOWBAT}}{f_{OSC} \bullet t_{MIN(ON)}}$$

where V_{LOWBAT}, is the lowest battery voltage where the switcher is enabled.

Exceeding the minimum on-time constraint does not affect charge current or battery float voltage, so it may not be of critical importance in most cases and high switching frequencies may be used in the design without any fear of severe consequences. As the sections on Inductor Selection and Capacitor Selection show, high switching frequencies allow the use of smaller board components, thus reducing the footprint of the applications circuit.

Fixed-frequency operation may also be influenced by dropout and burst mode operation as discussed previously.

Switching Inductor Selection

The primary criterion for switching inductor value selection in an LTC4121 charger is the ripple current created in that inductor. Once the inductance value is determined, the saturation current rating for that inductor must be equal to or exceed the maximum peak current in the inductor, $I_{L(PEAK)}$. The peak value of the inductor current is the sum of the programmed charge current, I_{CHG}, plus one half of the ripple current, ΔI_L. The peak inductor current must also remain below the current limit of the LTC4121, I_{PEAK}.

$$I_{L(PEAK)} = I_{CHG} + \frac{\Delta I_L}{2} < I_{PEAK}$$

The current limit of the LTC4121, I_{PEAK}, is at least 585mA (and at most 1250mA). The typical value of I_{PEAK} is illustrated in a graph in the Typical Performance Characteristics, R_{SNS} Current Limit vs Temperature.

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For a given input and battery voltage, the inductor value and switching frequency determines the peak-to-peak ripple current amplitude according to the following formula:

$$\Delta I_L = \frac{(V_{IN} - V_{BAT}) \bullet V_{BAT}}{f_{OSC} \bullet V_{IN} \bullet L_{SW}}$$

Ripple current is typically set to be within a range of 20% to 40% of the programmed charge current, I_{CHG}. To obtain a ripple current in this range, select an inductor value using the nearest standard inductance value available that obeys the following formula:

$$L_{SW} \geq \frac{\left(V_{IN(MAX)} - V_{FLOAT}\right) \bullet V_{FLOAT}}{f_{OSC} \bullet V_{IN(MAX)} \bullet \left(30\% \bullet I_{CHG}\right)}$$

Then select an inductor with a saturation current rating greater than $I_{L(PEAK)}$.

Input Capacitor

The LTC4121 charger is biased directly from the input supply at the V_{IN} pin. This supply provides large switched currents, so a high-quality, low ESR decoupling capacitor is recommended to minimize voltage glitches at V_{IN}. Bulk capacitance is a function of the desired input ripple voltage (ΔV_{IN}), and follows the relation:

$$C_{IN(BULK)} = \frac{I_{CHG} \bullet \frac{V_{BAT}}{V_{IN}}}{\Delta V_{IN}} (\mu F)$$

Input ripple voltages (ΔV_{IN}) above 0.01V are not recommended. 10µF is typically adequate for most charger applications, with a voltage rating of 40V.

The input capacitor also forms a pole with the source impedance that supplies power to V_{IN}. This R-C network must settle within the 36ms PW_{MP} period for the LTC4121 to accurately sample the open-circuit voltage at V_{IN}. Adequate settling is usually achieved in 3 to 5 R-C time constants. To allow the LTC4121 to correctly sample the open-circuit voltage, limit C_{IN} to:

$$C_{IN} < PW_{MP} / (5 \bullet R_{SOURCE}),$$

where R_{SOURCE} is the impedance of the power source. For a solar panel this is the impedance of the panel at the open-circuit voltage. Looking at a panel's I-V curve, the source impedance is approximated by $(V_{OC} - V_{MP})/I_{MP}$. Typically V_{MP} is about 80% of V_{OC}, so the solar panels source impedance can be approximated as:

$$R_{SOURCE} \approx V_{OC} / (5 \bullet I_{MP}).$$

Reverse Blocking

When a fully charged battery is suddenly applied to the BAT pin, a large in-rush current charges the C_{IN} capacitor through the body diode of the LTC4121 topside power switch. While the amplitude of this current can exceed several Amps, the LTC4121 will survive provided the battery voltage is below about 11V. To completely eliminate this in-rush current, a blocking P-channel MOSFET should be placed in series with the BAT pin. When the battery is the only source of power, this PMOS also serves to decrease battery drain current due to any load placed at V_{IN}, conducted through the body diode of the topside power switch on the LTC4121. The PMOS body diode shown in Figure 8 serves as the blocking component since $\overline{CHRG}$ is high impedance when the battery voltage is greater than the input voltage. When $\overline{CHRG}$ pulls low, i.e. during most of a normal charge cycle, the PMOS is on to reduce power dissipation. The PMOS requires a forward current rating equal to the programmed charge current and a reverse breakdown voltage equal to the programmed float voltage.

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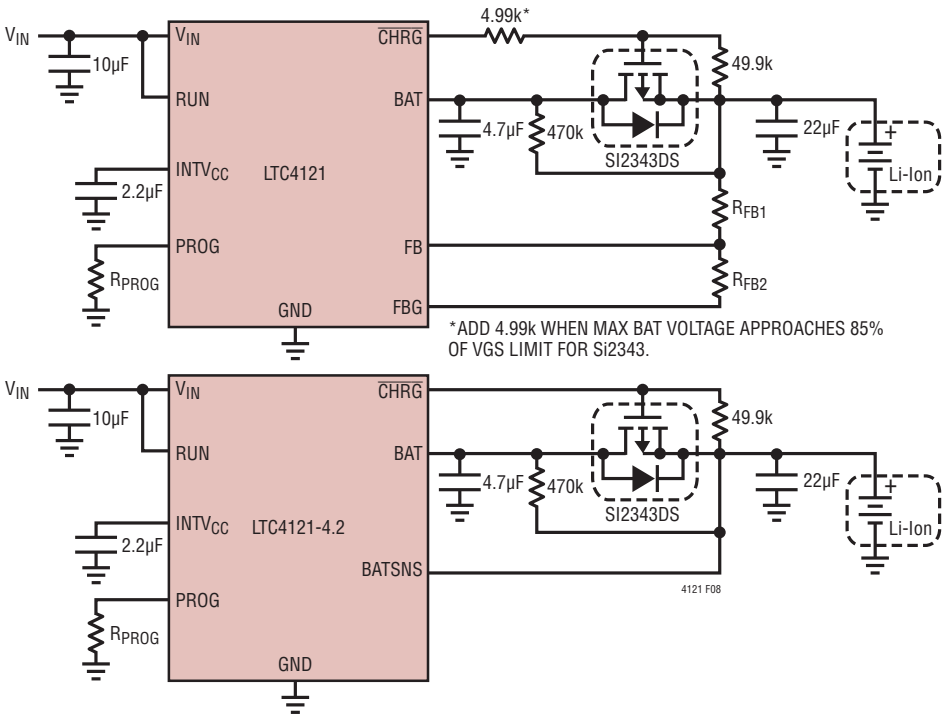

Figure 8. Reverse Blocking with a P-Channel MOSFET in Series with the BAT Pin

BAT Capacitor and Output Ripple: C_{BAT}

The LTC4121 charger output requires bypass capacitance connected from BAT to GND (C_{BAT}). A 22µF ceramic capacitor is required for all applications. In systems where the battery can be disconnected from the charger output, additional bypass capacitance may be desired. In this type of application, excessive ripple and/or low amplitude oscillations can occur without additional output bulk capacitance. For optimum stability, the additional bulk capacitance should also have a small amount of ESR. For these applications, place a 100µF low ESR non-ceramic capacitor (chip tantalum or organic semiconductor capacitors such as Sanyo OS-CONs or POSCAPs) from BAT to GND, in parallel with the 22µF ceramic bypass capacitor, or use large ceramic capacitors with an additional small series ESR resistor of less than 1Ω. This additional bypass capacitance may also be required in systems where the battery is connected to the charger with long wires. The voltage rating of all capacitors applied to C_{BAT} must meet or exceed the battery float voltage.

Boost Supply Capacitor

The BOOST pin provides a bootstrapped supply rail that provides power to the top gate drivers. The operating voltage of the BOOST pin is internally generated from $INTV_{CC}$ whenever the SW pin pulls low. This provides a floating voltage of $INTV_{CC}$ above SW that is held by a capacitor tied from BOOST to SW. A low ESR ceramic capacitor of 10nF to 33nF is sufficient, with a voltage rating of 6V.

$INTV_{CC}$ Supply and Capacitor

Power for the top and bottom gate drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. A low ESR ceramic capacitor of 2.2µF is required on the $INTV_{CC}$ pin. The $INTV_{CC}$ supply has a relatively low current limit (about 20mA) that is dialed back when $INTV_{CC}$ is low to reduce power dissipation. Do not use the $INTV_{CC}$ voltage to supply power for any external circuitry except for the NTCBIAS network. When the RUN pin is above V_{EN}, the $INTV_{CC}$ supply is enabled, and when $INTV_{CC}$ rises above UV_{INTVCC}, the charger is enabled.

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Calculating IC Power Dissipation

The user should ensure that the maximum rated junction temperature is not exceeded under all operating conditions. The thermal resistance of the LTC4121 package (θ_{JA}) is 54°C/W; provided that the Exposed Pad is in good thermal contact with the PCB. The actual thermal resistance in the application will depend on the forced air cooling and other heat sinking means, especially the amount of copper on the PCB to which the LTC4121 is attached. The actual power dissipation while charging is approximated by the following formula:

$$P_D = \left(V_{IN} - V_{BAT}\right) \bullet I_{TRKL} + V_{IN} \bullet I_{IN(SWITCHING)} + R_{SNS} \bullet I^2_{CHG} + R_{DSON(TOP)} \bullet \left(\frac{V_{BAT}}{V_{IN}}\right) \bullet I^2_{CHG} + R_{DSON(BOT)} \bullet \left(1 - \frac{V_{BAT}}{V_{IN}}\right) \bullet I^2_{CHG}$$

During trickle charge ($V_{BAT} < V_{TRKL}$) the power dissipation may be significant as I_{TRKL} is typically 10mA, however during normal charging the I_{TRKL} term is zero. I_{TRKL} is also zero if V_{BAT} approaches $INTV_{CC}$, since I_{TRKL} is sourced from the $INTV_{CC}$ LDO.

The junction temperature can be estimated using the following formula:

$$T_J = T_A + P_D \bullet \Theta_{JA}.$$

where T_A is the ambient operating temperature.

PCB Layout

To prevent magnetic and electrical field radiation and high frequency resonant problems, proper layout of the components connected to the LTC4121 is essential. For maximum efficiency, the switch node rise and fall times should be minimized. The following PCB design priority list will help insure proper topology. Layout the PCB using the guidelines listed below in this specific order:

1. V_{IN} input capacitor should be placed as close as possible to the IN pin with the shortest copper traces possible. The ground return of the input capacitor should be connected to a solid ground plane.
2. Place the inductor as close as possible to the SW pin. Minimize the surface area of the SW pin node. Make the trace width the minimum needed to support the programmed charge current, and ensure that the spacing to other copper traces be maximized to reduce capacitance from the SW node to any other node.
3. Place the BAT capacitor adjacent to the BAT pin and ensure that the ground return feeds to the solid ground plane.
4. Route analog ground (RUN pin divider grounded resistor, the MPPT pin divider, and $INTV_{CC}$ capacitor ground) to the solid ground plane.
5. It is important to minimize parasitic capacitance on the PROG pin. The trace connecting to this pin should be as short as possible with extra wide spacing from adjacent copper traces.
6. Keep the GND capacitance of the MPPT pin to a minimum, and reduce coupling from the MPPT pin to any of the switching pins (SW, BOOST, and CHGSNS) by routing the MPPT trace away from these signals.

Maximize the copper area connected to the exposed pad. Place via connections directly under the exposed pad to connect a large copper ground plane to the LTC4121 to improve heat transfer.

Example PCB layout files of the LTC4121 are available at the following link:

http://www.linear.com/product/LTC4121#demoboards.

APPLICATIONS EXAMPLES

Design Example 1

Consider the design example, shown in Figure 14 on the last page, for the LTC4121-4.2. Input power is from a solar panel that has an open-circuit voltage V_{OC} = 21.6V, and maximum power voltage V_{MP} = 17V, or 79% of the open-circuit voltage. The battery float voltage is 4.2V, and the desired charge current is 400mA. The application has a minimum battery voltage of 2.5V.

There is no requirement given for the input voltage where the LTC4121-4.2 should turn on. Given that the MPPT set point, V_{MP}, is at 79% of the open-circuit voltage of 21.6V, one may elect to turn-on the LTC4121-4.2 at an input voltage anywhere below this set point. A level of 60% of the open-circuit voltage is selected, or 13V. This selection results in a RUN pin divider of R_{RUN1} = 464kΩ, and R_{RUN2} = 107kΩ. With this RUN pin divider, the LTC4121-4.2 enters DISABLED mode if the input supply drops below 12V.

Now select the MPPT resistive divider to obtain a maximum power point of 17V. The maximum power point of 17V is at 79% of the open-circuit voltage. This is used to calculate the ratio

$$\frac{V_{MP}}{V_{OC}} = \frac{0.1}{K_R}$$

Select

$$K_R = 0.1/0.79 = 0.1266$$

This ratio is obtained by selecting R_{MPPT1} and R_{MPPT2} following:

$$R_{MPPT1} = \frac{(1-0.1266)}{0.1266} R_{MPPT2} = 6.9 \bullet R_{MPPT2}$$

Using standard 1% resistors, select R_{MPPT1} = 698kΩ and R_{MPPT2} = 100kΩ to obtain a K_R of 0.1253, and an MPPT set point of 17.24V.

As described in the MPPT Error Terms section, the actual regulation voltage will vary from the programmed voltage down to 45mV/K_R = 359mV below the programmed voltage. In this example, the expected regulation voltage is 16.88V to 17.24V, or 78.2% to 80.1% of the open-circuit voltage.

The switching frequency of 750kHz is selected to achieve an on-time of 154ns which is greater than $t_{MIN(ON)}$ at the maximum input supply, and minimum battery voltage of 2.5V.

$$t_{ON} = \frac{2.5V}{750kHz \bullet 21.6V} = 154.3 > t_{MIN(ON)}$$

Next, the minimum standard inductance value is found that maintains an inductor ripple current 30% of I_{CHG}, at the peak power input voltage of 17V using the following formula:

$$L_{SW} > \frac{(17V - 4.2V) \bullet 4.2V}{750kHz \bullet 17V \bullet (30\% \bullet 400mA)} = 35\mu H$$

The next largest standard inductance value is 47µH. This inductor selection results in a ripple current of 90mA and peak inductor current $I_{L(PEAK)}$ of:

$$I_{L(PEAK)} = 400mA + \frac{(17V - 4.2V) \bullet 4.2V}{2 \bullet 750kHz \bullet 17V \bullet 47\mu H}$$

$$I_{L(PEAK)} = 444mA$$

The saturation current of the switch inductor needs to be greater than $I_{L(PEAK)}$.

Now select R_{PROG} for the desired average charge current during constant-current operation. The nearest standard 1% resistor to satisfy the following relation:

$$R_{PROG} = \frac{h_{PROG} \bullet 1.227V}{400mA} = 3.01k\Omega$$

Select C_{IN} = 10µF for the input decoupling capacitor, achieving an input voltage ripple of 10mV.

$$\Delta V_{IN} = \frac{400mA \bullet \frac{4.2V}{17V}}{10\mu F} = 10mV$$

The minimum standard voltage rating for C_{IN} is 50V.

Select C_{INTVCC} = 2.2µF, and C_{BST} = 22nF, and finally the battery capacitor should be 22µF. The lowest standard voltage rating for these capacitors is 6V.

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In this design example, maximum power dissipation is calculated during trickle charge as:

$$P_D = (17V - 2.5V) \bullet 10mA + 17V \bullet 2.5mA + 0.3\Omega \bullet 0.04A^2 + 0.8\Omega \bullet \frac{4.2V}{17V} 0.04A^2 + 0.5\Omega \bullet \left(1 - \frac{2.5V}{17V}\right) \bullet 0.04A^2 = 0.19W$$

This dissipated power results in a junction temperature rise of:

$P_D \bullet \Theta_{JA} = 0.19W \bullet 54C°/W = 10.2°C$

Estimating $I_{IN(SWITCHING)}$ at 2.5mA from the $I_{IN(SWITCHING)}$ Current vs Input Voltage graph at V_{IN} = 17V, during regular charging with $V_{BAT} > V_{TRKL}$, the power dissipation reduces to:

$$P_D = 17V \bullet 2.5mA + 0.3\Omega \bullet 0.4A^2 + 0.8\Omega \bullet \frac{4.2V}{17V} 0.4A^2 + 0.5\Omega \bullet \left(1 - \frac{4.2V}{17V}\right) \bullet 0.4A^2 = 0.18W$$

This dissipated power results in a junction temperature rise of 9.8°C over ambient.

Design Example 2

Consider the design with a 3.5W or greater solar panel with a maximum input voltage of V_{OC} = 22.4V and a maximum power voltage of V_{MP} = 18V or 80.3% of the open-circuit voltage. The minimum battery voltage is 5V, and the float voltage is 8.2V, with a charge current of 400mA.

The MPPT set point is at 80.3% of the open-circuit voltage. So select

$K_R = 0.1/0.803 = 0.1245$

This ratio is obtained by selecting R_{MPPT1} and R_{MPPT2} following:

$$R_{MPPT1} = \frac{(1 - 0.1245)}{0.1245} R_{MPPT2} = 7.03 \bullet R_{MPPT2}$$

Using standard 1% resistors, select R_{MPPT1} = 715kΩ and R_{MPPT2} = 102kΩ to obtain a K_R of 0.1248 and nominal MPPT set point of 17.94V. Including the effect of MPPT error terms, the expected MPPT regulation voltage will vary between 17.58V to 17.94V or 78.5% to 80.1% of the open-circuit voltage.

Next, the external feedback divider, R_{FB1}/R_{FB2}, is found using standard 1% values listed in Table 2.

R_{FB1} = 2.05MΩ

R_{FB2} = 845kΩ

With these resistors, and including the resistance of the FBG pin, the battery float voltage is 8.22V.

Select the RUN pin divider to turn on the charger when the solar-cell output reaches 14.7V. This is obtained by selecting R_{RUN1} = 536kΩ, and R_{RUN2} = 107kΩ. This selection turns off the charger if the input falls below 13.52V.

The switching frequency is selected at 1.5MHz which meets the minimum on-time requirement for battery voltages as low as 5V.

$$t_{ON} = \frac{5V}{1.5MHz \bullet 17.94V} = 186ns > t_{MIN(ON)}$$

The minimum standard inductance value for a 30% ripple current is

$$L_{SW} > \frac{(17.94V - 8.2V) \bullet 8.2V}{1.5MHz \bullet 17.94V \bullet (30\% \bullet 400mA)} = 24.8\mu H$$

The nearest standard inductor value greater than this is 33µH. With an inductor of 33µH, the peak inductor current is 445mA and the ripple current amplitude, ΔI_L, is 90mA. Select an inductor with a saturation current greater than the peak inductor current.

Select R_{PROG} = 3.01k, as the nearest standard 1% value to provide a charge current of 403mA during constant-current operation.

APPLICATIONS EXAMPLES

Select a 50V rated capacitor for C_{IN} = 10µF to achieve an input voltage ripple of 10mV. And select 6V rated capacitors for C_{INTVCC} = 2.2µF, C_{BOOST} = 22nF, and a 10V rated C_{BAT} = 22µF.

Due to the large float voltage diode D7 is placed in series with the BAT pin to prevent exceeding the ABS MAX current rating on the R_{SNS} resistor in the event that a fully charged battery may be connected.

In this design example, maximum power dissipation is calculated during trickle charge with the following assumptions: V_{BAT} = 5.7V, V_{IN} is 19V, and $I_{IN(SWITCHING)}$ is estimated from the $I_{IN(SWITCHING)}$ Current vs Input Voltage graph in the Typical Performance Characteristics section at V_{IN} = 19V and FREQ = $INTV_{CC}$ as 4mA.

$$P_D = 19V \bullet 4mA + 0.3\Omega \bullet 0.04A^2 + 0.8\Omega \bullet \frac{5.7V}{19V} 0.04A^2 + 0.5\Omega \bullet \left(1 - \frac{5.7V}{19V}\right) \bullet 0.04A^2 = 77mW$$

This dissipated power results in a junction temperature rise of:

$$P_D \bullet \Theta_{JA} = 0.077W \bullet 54°C/W = 4.2°C$$

During regular charging with V_{BAT} = 8.2V, and assuming V_{IN} is at the MPPT voltage of 17.94V, the power dissipation increases to:

$$P_D = 18V \bullet 4mA + 0.3\Omega \bullet 0.4A^2 + 0.8\Omega \bullet \frac{8.2V}{19V} 0.4A^2 + 0.5\Omega \bullet \left(1 - \frac{8.2V}{19V}\right) \bullet 0.4A^2 = 0.22W$$

This dissipated power results in a junction temperature rise of 12°C over ambient.

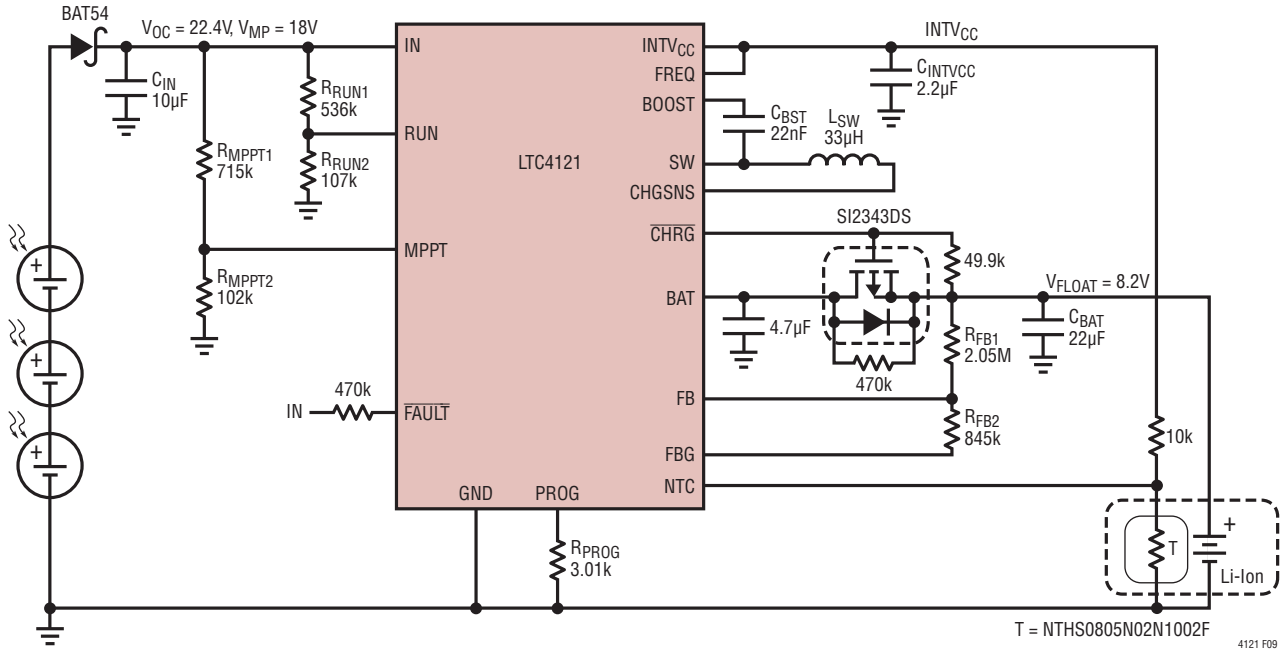

Figure 9. Design Example 2 with LTC4121