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Dual-Input Power Manager/ 3.5A LiFePO$_4$ Battery Charger with I^{2}C Control and USB OTG

FEATURES

- **High Efficiency Charger Capable of 3.5A Charge Current**
- **Charge Control Algorithm Specifically Designed for LiFePO$_4$ Batteries (Lithium Iron Phosphate)**
- **Monolithic Switching Regulator Makes Optimal Use of Limited Power and Thermal Budget**
- **Dual Input Overvoltage Protection Controller**
- **Priority Multiplexing for Multiple Inputs**
- **I^{2}C/SMBus Control and Status Feedback**
- **NTC Thermistor ADC for Temperature Dependent Charge Algorithms (JEITA)**
- **Instant-On Operation with Low Battery**
- **Battery Ideal Diode Controller for Power Management**
- **USB On-The-Go Power Delivery to the USB Port**
- Four Float Voltage Settings (3.45V, 3.55V, 3.6V, 3.8V)
- 28-Lead 4mm × 5mm QFN Package

APPLICATIONS

- Portable Medical Devices
- Portable Industrial Devices
- Backup Devices

DESCRIPTION

The LTC®4156 is a 15 watt I^{2}C controlled power manager with PowerPath™ instant-on operation, high efficiency switching battery charging and USB compatibility. The LTC4156 seamlessly manages power distribution from two 5V sources, such as a USB port and a wall adapter, to a single-cell rechargeable lithium iron phosphate battery and a system load.

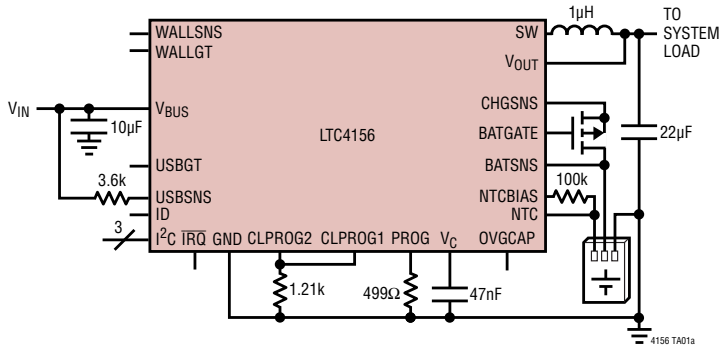
The LTC4156's switching battery charger automatically limits its input current for USB compatibility, or may draw up to 3A from a high power wall adapter. The high efficiency step-down switching charger is designed to provide maximum power to the application and reduced heat in high power density applications.

I^{2}C adjustability of input current, charge current, battery float voltage, charge termination, and many other parameters allows maximum flexibility. I^{2}C status reporting of key system and charge parameters facilitates intelligent control decisions. USB On-The-Go support provides 5V power back to the USB port without any additional components. A dual-input, priority multiplexing, overvoltage protection circuit guards the LTC4156 from high voltage damage on the V_{BUS} pin.

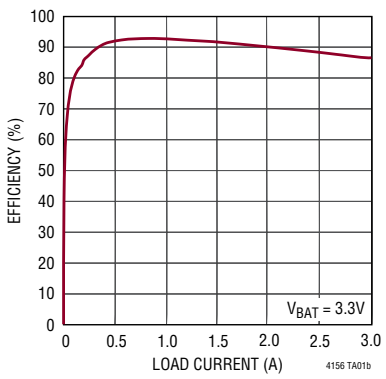
The LTC4156 is available in the low profile (0.75mm) 28-lead 4mm × 5mm QFN surface mount package.

TYPICAL APPLICATION

I^{2}C Controlled High Power Battery Charger/USB Power Manager



Switching Regulator Efficiency



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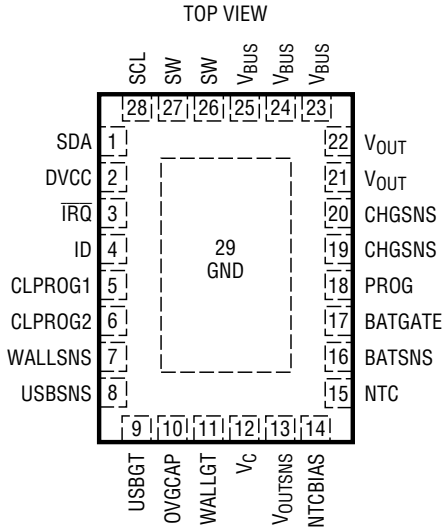
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{BUS} (Transient) t < 1ms, Duty Cycle < 1% ... –0.3V to 7V
V_{BUS} (Steady State), BATSNS, $\overline{IRQ}$, NTC..... –0.3V to 6V
DVCC, SDA, SCL (Note 3) .....–0.3V to V_{MAX}
$I_{WALLSNS}$, I_{USBSNS}..... ±20mA
$I_{NTCBIAS}$, $I_{\overline{IRQ}}$.....10mA
I_{SW}, I_{VOUT}, I_{CHGSNS} (Both Pins in Each Case).....4A
Operating Junction Temperature Range... –40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4156EUFD#PBF	LTC4156EUFD#TRPBF	4156	28-Lead (4mm × 5mm × 0.75mm) Plastic QFN	–40°C to 125°C
LTC4156IUFD#PBF	LTC4156IUFD#TRPBF	4156	28-Lead (4mm × 5mm × 0.75mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C (Note 2). V_{BUS} = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1} = R_{CLPROG2}$ = 1.21k, R_{PROG} = 499Ω, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Battery Charger							
V_{BUS}	Input Supply Voltage		●	4.35		5.5	V
V_{BUSREG}	Undervoltage Current Reduction	Input Undervoltage Current Limit Enabled			4.30		V
I_{VBUSQ}	Input Quiescent Current	USB Suspend Mode			0.060		mA
		100mA I_{VBUS} Mode, I_{VOUT} = 0µA, Charger Off			0.560		mA
		500mA – 3A I_{VBUS} Modes, I_{VOUT} = 0µA, Charger Off			17		mA
		CLPROG1 Mode, I_{VOUT} = 0µA, Charger Off			17		mA
I_{BATQ}	Battery Drain Current	$V_{BUS} > V_{UVLO}$, Battery Charger Off, I_{VOUT} = 0µA			7.0		µA
		V_{BUS} = 0V, I_{VOUT} = 0µA			2.0	3.0	µA
		Storage and Shipment Mode, DVCC = 0V			0.6	1.25	µA
$I_{VBUSLIM}$	Total Input Current When Load Exceeds Power Limit	100mA I_{VBUS} Mode (USB Lo Power) (Default)	●	65	80	100	mA
		500mA I_{VBUS} Mode (USB Hi Power)	●	460	480	500	mA
		600mA I_{VBUS} Mode		550	570	600	mA
		700mA I_{VBUS} Mode		650	670	700	mA
		800mA I_{VBUS} Mode		745	770	800	mA
		900mA I_{VBUS} Mode (USB 3.0)	●	800	850	900	mA
		1.00A I_{VBUS} Mode		950	1000	1025	mA
		1.25A I_{VBUS} Mode		1150	1230	1300	mA
		1.50A I_{VBUS} Mode		1425	1500	1575	mA
		1.75A I_{VBUS} Mode		1650	1750	1875	mA
		2.00A I_{VBUS} Mode		1900	2000	2125	mA
		2.25A I_{VBUS} Mode		2050	2175	2300	mA
		2.50A I_{VBUS} Mode		2350	2475	2600	mA
		2.75A I_{VBUS} Mode		2550	2725	2900	mA
		3.00A I_{VBUS} Mode (Default)		2800	2950	3100	mA
		2.5mA I_{VBUS} Mode (USB Suspend)			1.8	2.5	mA
V_{FLOAT}	BATSNS Regulated Output Voltage Selected by I^2C Control. Switching Modes	3.45V Setting (Default)	●	3.42	3.45	3.48	V
		3.55V Setting	●	3.52	3.55	3.58	V
		3.60V Setting	●	3.57	3.60	3.63	V
		3.80V Setting	●	3.77	3.80	3.83	V
I_{CHARGE}	Regulated Battery Charge Current Selected by I^2C Control	12.50% Charge Current Mode		290	315	340	mA
		18.75% Charge Current Mode		430	465	500	mA
		25.00% Charge Current Mode		577	620	663	mA
		31.25% Charge Current Mode		720	770	820	mA
		37.50% Charge Current Mode		870	925	981	mA
		43.75% Charge Current Mode		1013	1075	1137	mA
		50.00% Charge Current Mode		1162	1230	1298	mA
		56.25% Charge Current Mode		1316	1385	1454	mA
		62.50% Charge Current Mode		1458	1535	1612	mA
		68.75% Charge Current Mode		1601	1685	1769	mA
		75.00% Charge Current Mode		1743	1835	1927	mA
		81.25% Charge Current Mode		1881	1980	2079	mA
		87.50% Charge Current Mode		2024	2130	2237	mA
		93.75% Charge Current Mode		2166	2280	2394	mA
		100.0% Charge Current Mode (Default)		2309	2430	2552	mA
$I_{CHARGE(MAX)}$	Regulated Battery Charge Current	100.0% Charge Current Mode, R_{PROG} = 340Ω		3.44	3.57	3.70	A
V_{OUT}	PowerPath Regulated Output Voltage (V_{BUS} Power Available)	Suspend Mode, I_{VOUT} = 1mA			4.35	4.5	V
		Battery Charger Enabled, Charging, BATSNS ≥ 3.19V			BATSNS		V
		Battery Charger Terminated or Battery Charger Disabled			4.35	4.5	V
$V_{OUT(MIN)}$	Low Battery Instant-On Output Voltage (V_{BUS} Power Available)	Battery Charger Enabled, Charging, BATSNS ≤ 3.0V		3.10	3.19		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C (Note 2). V_{BUS} = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1} = R_{CLPROG2}$ = 1.21k, R_{PROG} = 499Ω, unless noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VOUT}	V_{OUT} Current Available Before Loading Battery	2.5mA I_{VBUS} Mode (USB Suspend)		1	1.3		mA
		100mA I_{VBUS} Mode, BAT = 3.3V			76		mA
		500mA I_{VBUS} Mode, BAT = 3.3V			673		mA
		600mA I_{VBUS} Mode, BAT = 3.3V			810		mA
		700mA I_{VBUS} Mode, BAT = 3.3V			944		mA
		800mA I_{VBUS} Mode, BAT = 3.3V			1093		mA
		900mA I_{VBUS} Mode, BAT = 3.3V			1200		mA
		1.00A I_{VBUS} Mode, BAT = 3.3V			1397		mA
		1.25A I_{VBUS} Mode, BAT = 3.3V			1728		mA
		1.50A I_{VBUS} Mode, BAT = 3.3V			2072		mA
		1.75A I_{VBUS} Mode, BAT = 3.3V			2411		mA
		2.00A I_{VBUS} Mode, BAT = 3.3V			2700		mA
		2.25A I_{VBUS} Mode, BAT = 3.3V			2846		mA
		2.50A I_{VBUS} Mode, BAT = 3.3V			3154		mA
		2.75A I_{VBUS} Mode, BAT = 3.3V			3408		mA
		3.00A I_{VBUS} Mode, BAT = 3.3V			3657		mA
V_{PROG}	PROG Pin Servo Voltage	12.50% Charge Current Mode			150		mV
		18.75% Charge Current Mode			225		mV
		25.00% Charge Current Mode			300		mV
		31.25% Charge Current Mode			375		mV
		37.50% Charge Current Mode			450		mV
		43.75% Charge Current Mode			525		mV
		50.00% Charge Current Mode			600		mV
		56.25% Charge Current Mode			675		mV
		62.50% Charge Current Mode			750		mV
		68.75% Charge Current Mode			825		mV
		75.00% Charge Current Mode			900		mV
		81.25% Charge Current Mode			975		mV
		87.50% Charge Current Mode			1050		mV
		93.75% Charge Current Mode			1125		mV
		100.0% Charge Current Mode (Default)			1200		mV
V_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		96.6	97.6	98.4	%
$t_{TERMINATE}$	Safety Timer Termination Period Selected by I^2C Control. Timer Starts When BATSNS ≥ V_{FLOAT}	0.25-Hour Mode		0.23	0.27	0.30	Hours
		0.5-Hour Mode		0.47	0.53	0.59	Hours
		1-Hour Mode (Default)		0.95	1.06	1.17	Hours
		4-Hour Mode		3.81	4.24	4.66	Hours
V_{LOWBAT}	Threshold Voltage	Rising Threshold		2.65	2.8	2.95	V
		Hysteresis			130		mV
t_{BADBAT}	Bad Battery Termination Time	BATSNS < ($V_{LOWBAT} - \Delta V_{LOWBAT}$)		0.47	0.53	0.59	Hours
$V_{C/x}$	Full Capacity Charge Indication PROG Voltage Selected by I^2C Control	C/10 Mode (I_{CHARGE} = 10%FS) (Default)		110	120	130	mV
		C/5 Mode (I_{CHARGE} = 20%FS)		230	240	250	mV
		C/20 Mode (I_{CHARGE} = 5%FS)		15	24	33	mV
		C/50 Mode (I_{CHARGE} = 2%FS)		50	60	70	mV
h_{PROG}	Ratio of I_{CHGSNS} to PROG Pin Current				1000		mA/mA
$h_{CLPROG1}$ (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG1 Sense Current	CLPROG1 I_{VBUS} Mode			990		mA/mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C (Note 2). V_{BUS} = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1} = R_{CLPROG2}$ = 1.21k, R_{PROG} = 499Ω, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$h_{CLPROG2}$ (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG2 Sense Current	2.5mA I_{VBUS} Mode (USB Suspend) 100mA I_{VBUS} Mode 500mA I_{VBUS} Mode 600mA I_{VBUS} Mode 700mA I_{VBUS} Mode 800mA I_{VBUS} Mode 900mA I_{VBUS} Mode 1.00A I_{VBUS} Mode 1.25A I_{VBUS} Mode 1.50A I_{VBUS} Mode 1.75A I_{VBUS} Mode 2.00A I_{VBUS} Mode 2.25A I_{VBUS} Mode 2.50A I_{VBUS} Mode 2.75A I_{VBUS} Mode 3.00A I_{VBUS} Mode			19 79 466 557 657 758 839 990 1222 1494 1746 1999 2175 2477 2730 2956		mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA
$V_{CLPROG1}$	CLPROG1 Servo Voltage in Current Limit	CLPROG1 I_{VBUS} Mode			1.2		V
$V_{CLPROG2}$	CLPROG2 Servo Voltage in Current Limit	2.5mA I_{VBUS} Mode (USB Suspend) 100mA – 3A I_{VBUS} Modes			103 1.2		mV V
f_{OSC}	Switching Frequency			2.05	2.25	2.50	MHz
R_{PMOS}	High Side Switch On Resistance				0.090		Ω
R_{NMOS}	Low Side Switch On Resistance				0.080		Ω
R_{CHG}	Battery Charger Current Sense Resistance				0.040		Ω
I_{PEAK}	Peak Inductor Current Clamp	500mA – 3A I_{VBUS} Modes			6.7		A
Step-Up Mode PowerPath Switching Regulator (USB On-The-Go)							
V_{BUS}	Output Voltage	0mA ≤ I_{VBUS} ≤ 500mA		4.75		5.25	V
V_{OUT}	Input Voltage			2.9			V
$I_{VBUSOTG}$	Output Current Limit				1.4		A
$I_{VOUTOTGQ}$	V_{OUT} Quiescent Current	I_{VBUS} = 0mA			1.96		mA
$V_{CLPROG2}$	Output Current Limit Servo Voltage				1.2		V
$V_{BATSNSUVLO}$	V_{BATSNS} Undervoltage Lockout	V_{BATSNS} Falling Hysteresis		2.65	2.8 130	2.95	V mV
$t_{SCFAULT}$	Short-Circuit Fault Delay	V_{BUS} < 4V			7.2		ms
Overvoltage Protection, Priority Multiplexer and Undervoltage Lockout; USB Input Connected to USBSNS Through 3.6k Resistor; WALL Input Connected to WALLSNS Through 3.6k Resistor							
V_{UVLO}	USB Input, Wall Input Undervoltage Lockout	Rising Threshold Falling Threshold Hysteresis		4.05 3.90	 100	4.45 4.25	V V mV
V_{DUVLO}	USB Input, Wall Input to BATSNS Differential Undervoltage Lockout	Rising Threshold Falling Threshold Hysteresis		100 50	 70	425 375	mV mV mV
V_{OVLO}	USB Input, Wall Input Overvoltage Protection Threshold	Rising Threshold		5.75	6.0	6.3	V
$V_{USBGTACTV}$	USBGT Output Voltage Active	USBSNS < $V_{USBOVLO}$			2 • V_{USBSNS}		V
$V_{WALLGTACTV}$	WALLGT Output Voltage Active	WALLSNS < $V_{WALLOVLO}$			2 • $V_{WALLSNS}$		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C (Note 2). V_{BUS} = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1} = R_{CLPROG2}$ = 1.21k, R_{PROG} = 499Ω, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{USBGTPROT}$	USBGT Output Voltage Protected	USBSNS > $V_{USBOVLO}$			0		V
$V_{WALLGTPROT}$	WALLGT Output Voltage Protected	WALLSNS > $V_{WALLOVLO}$			0		V
$V_{USBGTLOAD}$, $V_{WALLGTLOAD}$	USBGT, WALLGT Voltage Under Load	5V Through 3.6k into WALLSNS, USBSNS, I_{USBGT}, I_{WALLGT} = 1µA		8.4	8.9		V
$I_{USBSNSQ}$	USBSNS Quiescent Current	V_{USBSNS} = 5V, V_{USBSNS} > $V_{WALLSNS}$ V_{USBSNS} = 5V, $V_{WALLSNS}$ > V_{USBSNS}			27 54		µA µA
$I_{WALLSNSQ}$	WALLSNS Quiescent Current	$V_{WALLSNS}$ = 5V, $V_{WALLSNS}$ > V_{USBSNS} $V_{WALLSNS}$ = 5V, V_{USBSNS} > $V_{WALLSNS}$			27 54		µA µA
t_{RISE}	OVGCAP Time to Reach Regulation	C_{OVGCAP} = 1nF			1.2		ms
$\overline{IRQ}$ Pin Characteristics							
$I_{\overline{IRQ}}$	$\overline{IRQ}$ Pin Leakage Current	$V_{\overline{IRQ}}$ = 5V				1	µA
$V_{\overline{IRQ}}$	$\overline{IRQ}$ Pin Output Low Voltage	$I_{\overline{IRQ}}$ = 5mA			75	100	mV
ID Pin Characteristics							
I_{ID}	ID Pin Pull-Up Current	V_{ID} = 0V		35	55	85	µA
V_{ID_OTG}	ID Pin Threshold Voltage	ID Pin Falling Hysteresis		0.5	0.86 0.2	0.95	V V
Thermistor Measurement System							
κ_{OFFSET}	V_{NTC} / $V_{NTCBIAS}$ A/D Lower Range End	V_{NTC} / $V_{NTCBIAS}$ Ratio Below Which Only 0x00 Is Returned			0.113		V/V
κ_{HIGH}	V_{NTC} / $V_{NTCBIAS}$ A/D Upper Range End	V_{NTC} / $V_{NTCBIAS}$ Ratio Above Which Only 0x7F Is Returned			0.895		V/V
κ_{SPAN}	A/D Span Coefficient (Decimal Format)			6.091	6.162	6.191	mV/V/ LSB
d_{TOO_COLD}	NTCVAL at NTC_TOO_COLD (Decimal Format)	Warning Threshold Reset Threshold		102 98	102 98	102 98	Count Count
d_{HOT_FAULT}	NTCVAL at HOT_FAULT (Decimal Format)	Fault Threshold Reset Threshold		19 23	19 23	19 23	Count Count
I_{NTC}	NTC Leakage Current			–100		100	nA
Ideal Diode							
V_{FWD}	Forward Voltage Detection	Input Power Available, Battery Charger Off			15		mV
I^2C Port							
DVCC	I^2C Logic Reference Level	(Note 3)		1.7		V_{MAX}	V
I_{DVCCQ}	DVCC Current	SCL/SDA = 0kHz			0.25		µA
V_{DVCC_UVLO}	DVCC UVLO				1.0		V
ADDRESS	I^2C Address				0001_001[R/$\overline{W}$]b		
$V_{IH,SDA,SCL}$	Input High Threshold			70			% DVCC
$V_{IL,SDA,SCL}$	Input Low Threshold					30	% DVCC
$I_{IH,SDA,SCL}$	Input Leakage High	SDA, SCL = DVCC		–1		1	µA
$I_{IL,SDA,SCL}$	Input Leakage Low	SDA, SCL = 0V		–1		1	µA
V_{OL}	Digital Output Low (SDA)	I_{SDA} = 3mA				0.4	V
f_{SCL}	Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition			1.3			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C (Note 2). V_{BUS} = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1} = R_{CLPROG2}$ = 1.21k, R_{PROG} = 499Ω, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{HD_SDA}	Hold Time After (Repeated) START Condition			0.6			µs
t_{SU_SDA}	Repeated START Condition Set-Up Time			0.6			µs
t_{SU_STO}	STOP Condition Time			0.6			µs
$t_{HD\_DAT(OUT)}$	Data Hold Time			0		900	ns
$t_{HD\_DAT(IN)}$	Input Data Hold Time			0			ns
t_{SU_DAT}	Data Set-Up Time			100			ns
t_{LOW}	Clock LOW Period			1.3			µs
t_{HIGH}	Clock HIGH Period			0.6			µs
t_f	Clock Data Fall Time			20		300	ns
t_r	Clock Data Rise Time			20		300	ns
t_{SP}	Spike Suppression Time					50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4156E is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4156E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4156I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where the package thermal impedance θ_{JA} = 43°C/W)

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

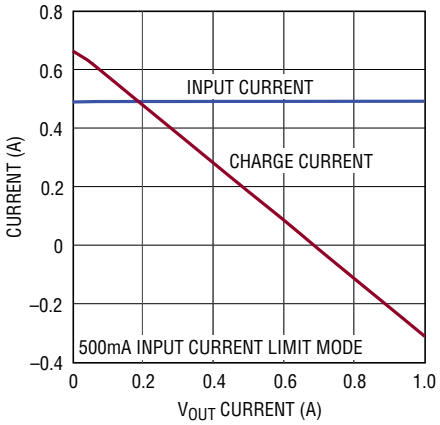
Note 3. V_{MAX} is the maximum of V_{BUS} or BATSNS

Note 4. Total input current is $I_{VBUSQ} + V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$.

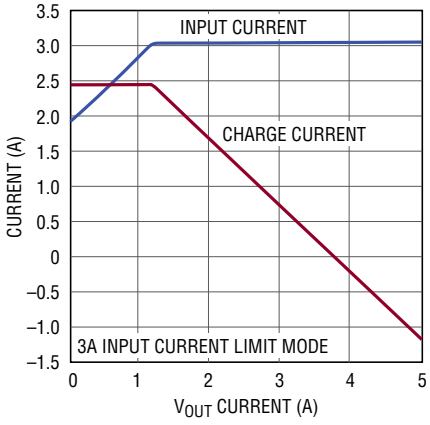
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C (Note 2). V_{BUS} = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1}$ = $R_{CLPROG2}$ = 1.21k, R_{PROG} = 499Ω, unless otherwise noted.

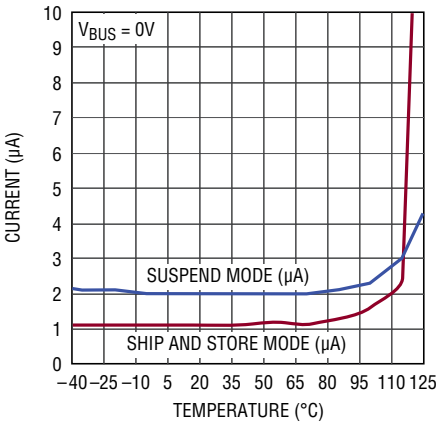
Battery and V_{BUS} Currents vs V_{OUT} Current



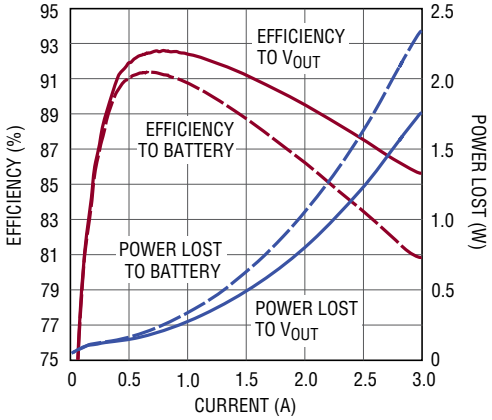
Battery and V_{BUS} Currents vs V_{OUT} Current



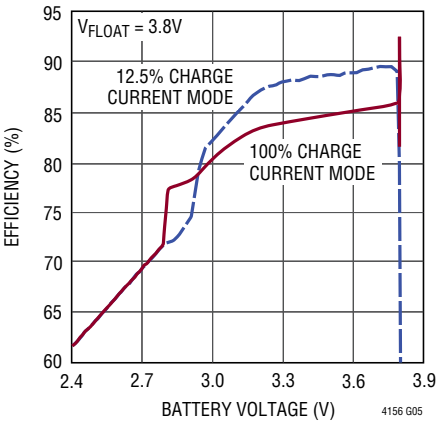
Battery Drain Current vs Temperature



Switching Regulator Efficiency

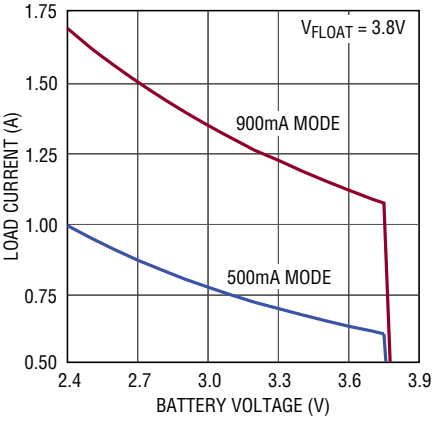


Battery Charger Total Efficiency vs Battery Voltage

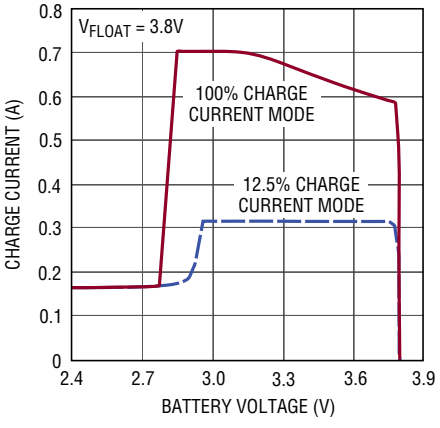


INCLUDES LOSSES FROM 2× Si7938DP OVP FETS
XFL4020-102ME INDUCTOR AND Si5481DU CHARGER FET

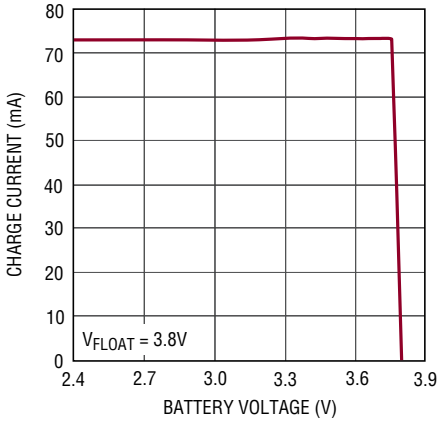
USB Compliant Load Current Available Before Discharging Battery



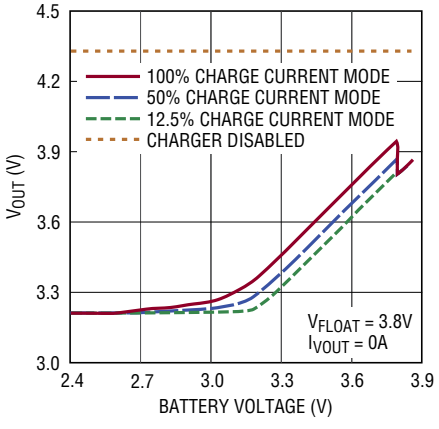
500mA USB Limited Battery Charge Current vs Battery Voltage



100mA USB Limited Battery Charge Current vs Battery Voltage



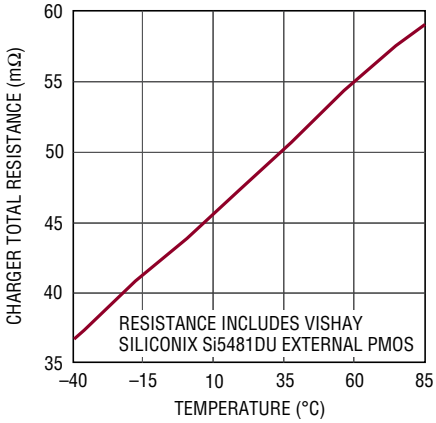
V_{OUT} Voltage vs Battery Voltage



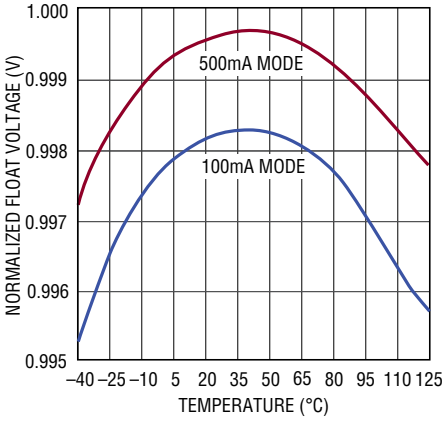
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C (Note 2). V_{BUS} = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1}$ = $R_{CLPROG2}$ = 1.21k, R_{PROG} = 499Ω, unless otherwise noted.

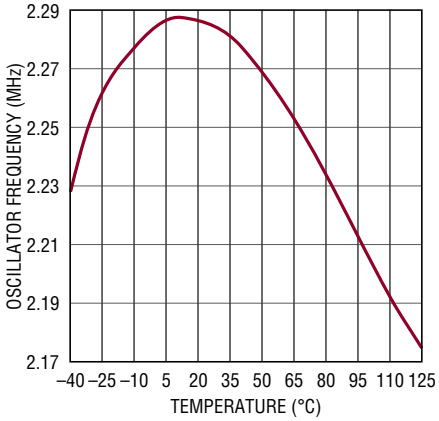
Battery Charger Resistance vs Temperature



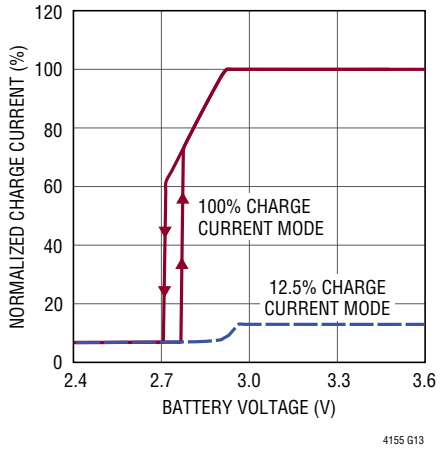
Normalized Float Voltage vs Temperature



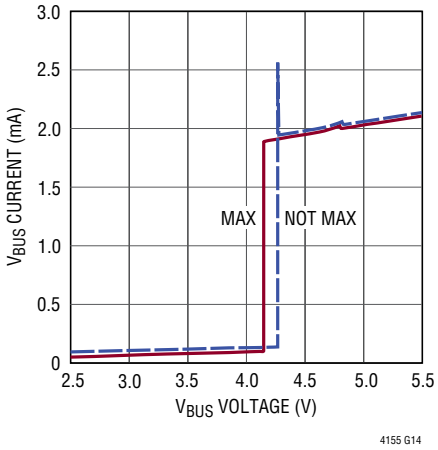
Oscillator Frequency vs Temperature



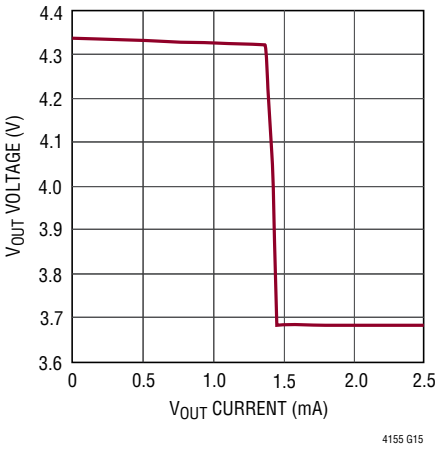
Automatic Charge Current Reduction vs Battery Voltage



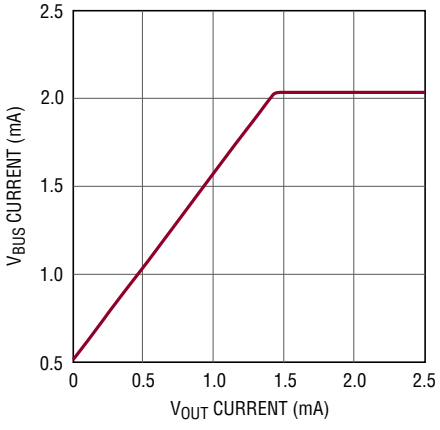
V_{BUS} Current vs V_{BUS} Voltage in USB Suspend Mode



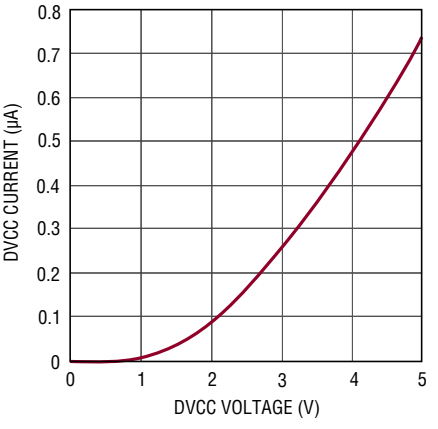
V_{OUT} Voltage vs V_{OUT} Current in USB Suspend Mode



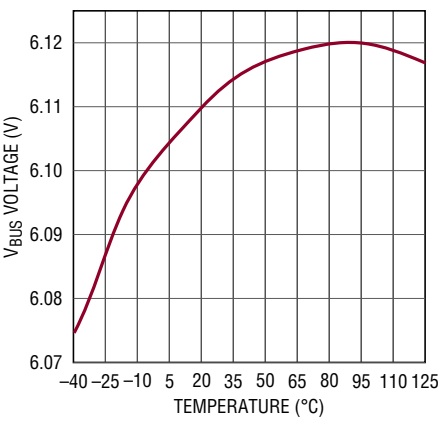
V_{BUS} Current vs V_{OUT} Current in USB Suspend Mode



Static DVCC Current vs DVCC Voltage



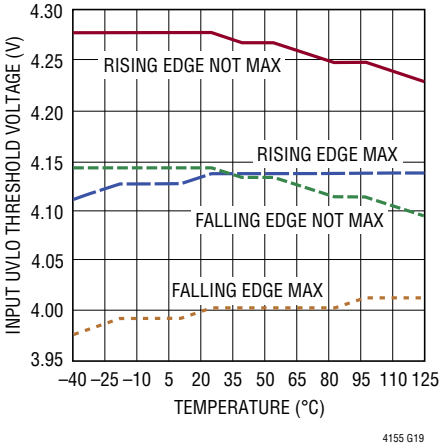
Rising Overvoltage Lockout Threshold vs Temperature



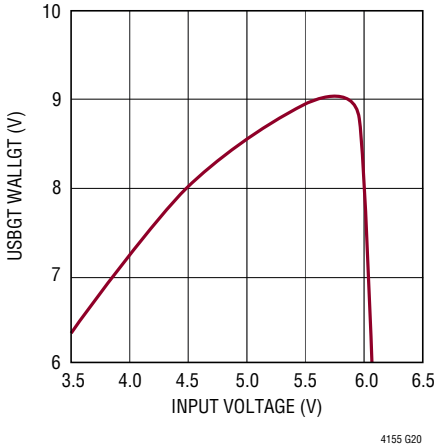
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C (Note 2). V_{BUS} = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1}$ = $R_{CLPROG2}$ = 1.21k, R_{PROG} = 499Ω, unless otherwise noted.

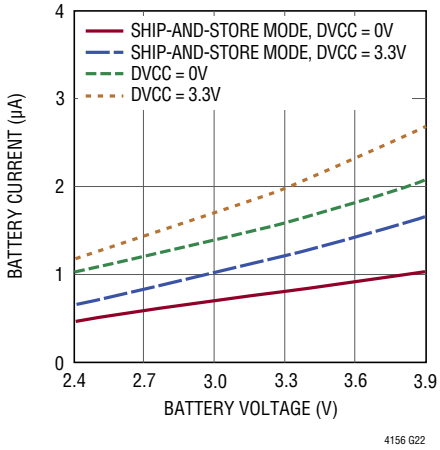
Undervoltage Lockout Thresholds vs Temperature



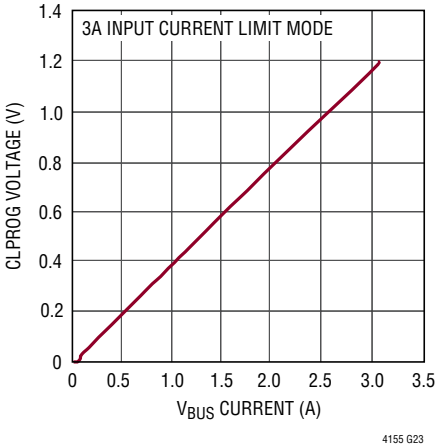
OVP Charge Pump Output vs Input Voltage



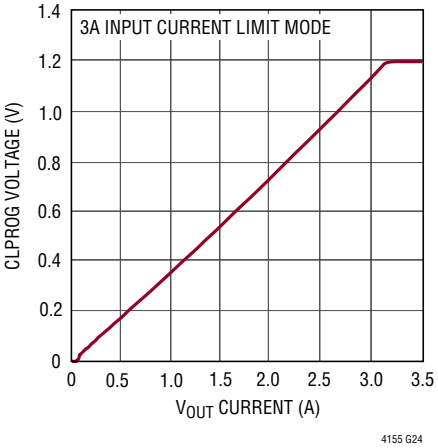
Battery Drain Current vs Battery Voltage



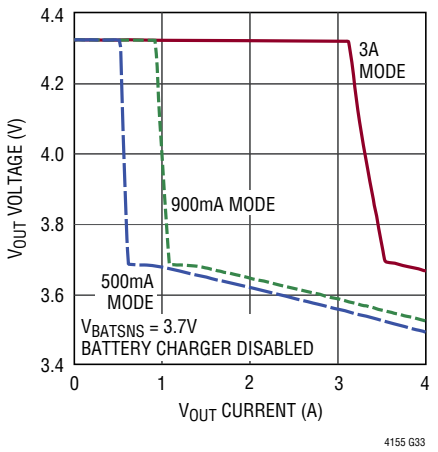
CLPROG Voltage vs V_{BUS} Current



CLPROG Voltage vs V_{OUT} Current



V_{OUT} Voltage vs V_{OUT} Current



PIN FUNCTIONS

SDA (Pin 1): Data Input/Output for the I^2C Serial Port. The I^2C input levels are scaled with respect to DVCC for I^2C compliance.

DVCC (Pin 2): Logic Supply for the I^2C Serial Port. DVCC sets the reference level of the SDA and SCL pins for I^2C compliance. It should be connected to the same power supply used to power the I^2C pull-up resistors.

$\overline{IRQ}$ (Pin 3): Open-Drain Interrupt Output. The $\overline{IRQ}$ pin can be used to generate an interrupt due to a variety of maskable status change events within the LTC4156.

ID (Pin 4): USB A-Device Detection Pin. When wired to a mini- or micro-USB connector, the ID pin detects when the "A" side of a mini or micro-USB cable is connected to the product. If the ID pin is pulled down, and the LOCKOUT_ID_PIN bit is not set in the I^2C port, the switching PowerPath operates in reverse providing USB power to the V_{BUS} pin from the battery. USB On-The-Go power can only be delivered from the USB multiplexer path.

CLPROG1 (Pin 5): Primary V_{BUS} Current Limit Programming Pin. A resistor from CLPROG1 to ground determines the upper limit of the current drawn from the V_{BUS} pin when CLPROG1 is selected. A precise measure of V_{BUS} current, $h_{CLPROG1}^{-1}$, is sent to the CLPROG1 pin. The switching regulator increases power delivery until CLPROG1 reaches 1.2V. Therefore, the current drawn from V_{BUS} will be limited to an amount given by the 1.2V reference voltage, $h_{CLPROG1}$ and $R_{CLPROG1}$.

Typically CLPROG1 is used to override the USB compliant input current control pin, CLPROG2, in applications where USB compliance is not a requirement. This would be useful for applications that use a dedicated wall adapter and would rather not be limited to the 500mW start-up value required by USB specifications. If USB compliance is a requirement at start-up, CLPROG1 should be connected to CLPROG2 and a single resistor should be used. See the CLPROG2 pin description.

In USB noncompliant designs, the user is encouraged to use an $R_{CLPROG1}$ value that best suits their application for start-up current limit. See the Operation section for more details.

CLPROG2 (Pin 6): Secondary V_{BUS} Current Limit Program Pin. CLPROG2 controls the V_{BUS} current limit when either selected via I^2C command or when CLPROG1 and CLPROG2 are shorted together. When selected, a resistor from CLPROG2 to ground determines the upper limit of the current drawn from the V_{BUS} pin. Like CLPROG1, a precise fraction of V_{BUS} current, $h_{CLPROG2}^{-1}$, is sent to the CLPROG2 pin. The switching regulator increases power delivery until CLPROG2 reaches 1.2V. Therefore, the current drawn from V_{BUS} will be limited to an amount given by the 1.2V reference voltage, $h_{CLPROG2}$ and $R_{CLPROG2}$.

There are a multitude of ratios for $h_{CLPROG2}$ available by I^2C control, three of which correspond to the 100mA, 500mA and 900mA USB specifications. CLPROG2 is also used to regulate maximum input current in the USB suspend mode and maximum output current in USB On-The-Go mode.

If CLPROG1 and CLPROG2 are shorted together at the onset of available input power, the LTC4156 selects CLPROG2 in the 100mA USB mode to limit input current. This ensures USB compliance if so desired. For USB compliance in all modes, the user is encouraged to make $R_{CLPROG2}$ equal to the value declared in the Electrical Characteristics.

WALLSNS (Pin 7): Highest Priority Multiplexer Input and Overvoltage Protection Sense Input. WALLSNS should be connected through a 3.6k resistor to a high priority input power connector and one drain of two source-connected N-channel MOSFET pass transistors. When voltage is detected on WALLSNS, it draws a small amount of current to power a charge pump which then provides gate drive to WALLGT to energize the external transistors. If the input voltage exceeds V_{OVLO}, WALLGT will be pulled to GND to disable the pass transistors and protect the LTC4156 from high voltage.

USBSNS (Pin 8): Lowest Priority Multiplexer Input and Overvoltage Protection Sense Input. USBSNS should be connected through a 3.6k resistor to a low priority input power connector and one drain of two source-connected N-channel MOSFET pass transistors. When voltage is detected on USBSNS, and no voltage is detected on WALLSNS, USBSNS draws a small amount of current to power a charge pump which then provides gate drive to

PIN FUNCTIONS

USBGT to energize the external transistors. If the input voltage exceeds V_{OVLO}, USBGT will be pulled to GND to disable the pass transistors and protect the LTC4156 from high voltage.

Power detected on WALLSNS is prioritized over USBSNS. If power is detected on both WALLSNS and USBSNS, by default, only WALLGT will receive drive for its pass transistors. See the Operations section for further information about programmable priority.

USBGT (Pin 9): Overvoltage Protection and Priority Multiplexer Gate Output. Connect USBGT to the gate pins of two source-connected external N-channel MOSFET pass transistors. One drain of the transistors should be connected to V_{BUS} and the other drain should be connected to a low priority DC input connector. In the absence of an overvoltage condition, this pin is driven from an internal charge pump capable of creating sufficient overdrive to fully enhance the pass transistors. If an overvoltage condition is detected, USBGT is brought rapidly to GND to prevent damage to the LTC4156. USBGT works in conjunction with USBSNS to provide this protection. USBGT also works in conjunction with WALLSNS to determine power source prioritization. See the Operation section.

OVGCAP (Pin 10): Overvoltage Protection Capacitor Output. A 0.1µF capacitor should be connected from OVGCAP to GND. OVGCAP is used to store charge so that it can be rapidly moved to WALLGT or USBGT. This feature provides faster power switchover when multiple inputs are supported by the end product.

WALLGT (Pin 11): Overvoltage Protection and Priority Multiplexer Gate Output. Connect WALLGT to the gate pins of two source-connected external N-channel MOSFET pass transistors. One drain of the transistors should be connected to V_{BUS} and the other drain should be connected to a high priority input connector. In the absence of an overvoltage condition, this pin is driven from an internal charge pump capable of creating sufficient gate drive to fully enhance the pass transistors. If an overvoltage condition is detected, WALLGT is brought rapidly to GND to prevent damage to the LTC4156. WALLGT works in conjunction with WALLSNS to provide this protection. WALLGT also works in conjunction with USBSNS to determine power source prioritization. See the Operation section.

V_C (Pin 12): Compensation Pin. A 0.047µF ceramic capacitor on this pin compensates the switching regulator control loops.

V_{OUTSNS} (Pin 13): Output Voltage Sense Input. Connecting V_{OUTSNS} directly to the V_{OUT} bypass capacitor ensures that V_{OUT} regulates at the correct level.

NTCBIAS (Pin 14): NTC Thermistor Bias Output. Connect a bias resistor between NTCBIAS and NTC, and a thermistor between NTC and GND. The value of the bias resistor should usually be equal to the nominal value of the thermistor.

NTC (Pin 15): Input to the Negative Temperature Coefficient Thermistor Monitoring Circuit. The NTC pin connects to a negative temperature coefficient thermistor, which is typically copackaged with the battery, to determine if the battery is too cold to charge or if the battery is dangerously hot. If the battery's temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground. The thermistor's temperature reading is continually digitized by an analog-to-digital converter and may be read back at any time via the I^2C port.

BATSNS (Pin 16): Battery Voltage Sense Input. For proper operation, this pin must always be connected to the battery. For fastest charging, connect BATSNS physically close to the lithium iron phosphate cell's positive terminal. Depending upon available power and load, a $LiFePO_4$ battery connected to the BATSNS pin will either be charged from V_{OUT} or will deliver system power to V_{OUT} via the required external P-channel MOSFET transistor.

BATGATE (Pin 17): Battery Charger and Ideal Diode Amplifier Control Output. This pin controls the gate of an external P-channel MOSFET transistor used to charge the $LiFePO_4$ cell and to provide power to V_{OUT} when the system load exceeds available input power. The source of the P-channel MOSFET should be connected to CHGSNS and the drain should be connected to BATSNS and the battery.

PIN FUNCTIONS

PROG (Pin 18): Charge Current Program and Monitor Pin. A resistor from PROG to GND programs the maximum battery charge rate. The LTC4156 features I²C programmability enabling software selection of fifteen charge currents that are inversely proportional to a single user-supplied programming resistor.

CHGSNS (Pins 19, 20): Battery Charger Current Sense Pin. An internal current sense resistor between V_{OUT} and CHGSNS monitors battery charge current. CHGSNS should be connected to the source of an external P-channel MOSFET transistor.

V_{OUT} (Pins 21, 22): Output Voltage of the Switching PowerPath Controller and Input Voltage of the Battery Charging System. The majority of the portable product should be powered from V_{OUT}. The LTC4156 will partition the available power between the external load on V_{OUT} and the battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode control function from BATSNS to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted power from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance multilayer ceramic capacitor of at least 22µF.

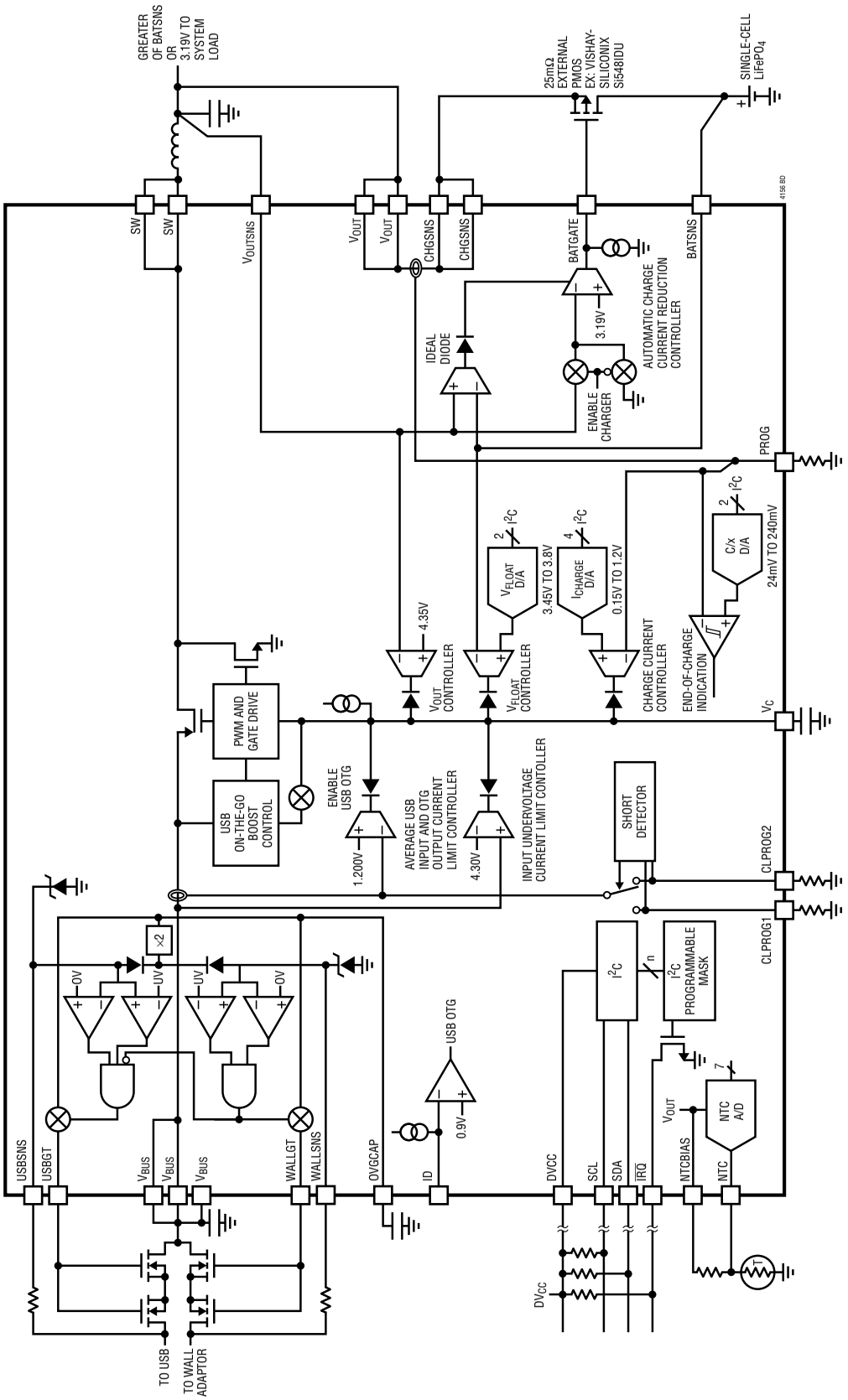
V_{BUS} (Pins 23, 24, 25): Input Voltage for the PowerPath Step-Down Switching Regulator and Output Voltage for the USB On-The-Go Step-Up Switching Regulator. V_{BUS} may be connected to the USB port of a computer or a DC output wall adapter or to one or both optional overvoltage protection/multiplexer compound transistors. V_{BUS} should be bypassed with a low impedance multilayer ceramic capacitor.

SW (Pins 26, 27): Switching Regulator Power Transmission Pin. The SW pin delivers power from V_{BUS} to V_{OUT} via the step-down switching regulator and from V_{OUT} to V_{BUS} via the step-up switching regulator. A 1µH inductor should be connected from SW to V_{OUT}. See the Applications Information section for a discussion of current rating.

SCL (Pin 28): Clock Input for the I²C Serial Port. The I²C input levels are scaled with respect to DVCC for I²C compliance.

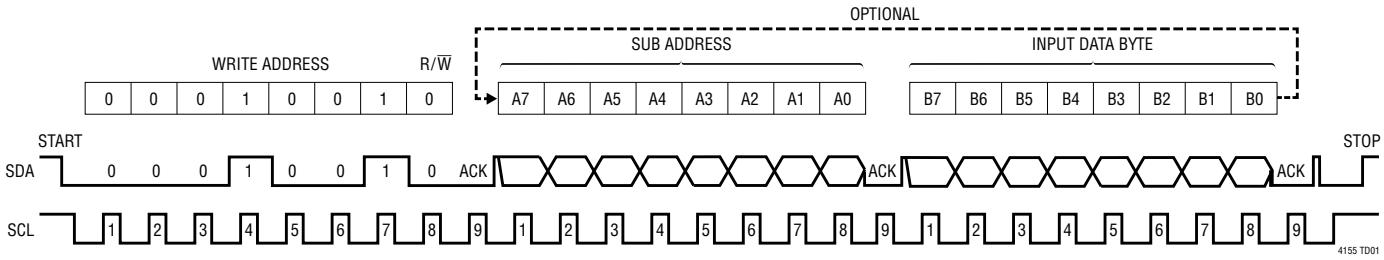
GND (Exposed Pad Pin 29): The exposed pad must be soldered to the PCB to provide a low electrical and thermal impedance connection to the printed circuit board's ground. A continuous ground plane on the second layer of a multilayer printed circuit board is strongly recommended.

BLOCK DIAGRAM

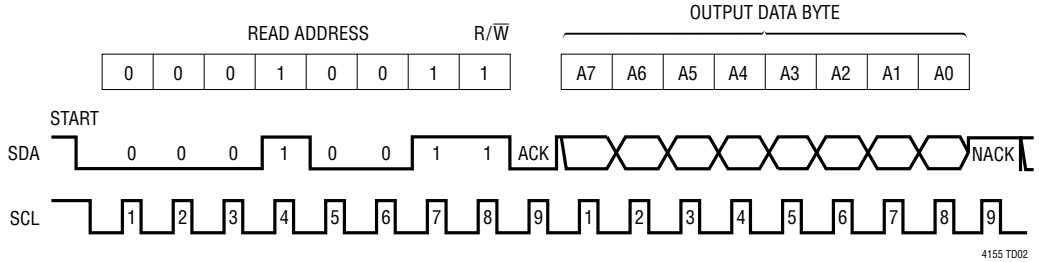


TIMING DIAGRAMS

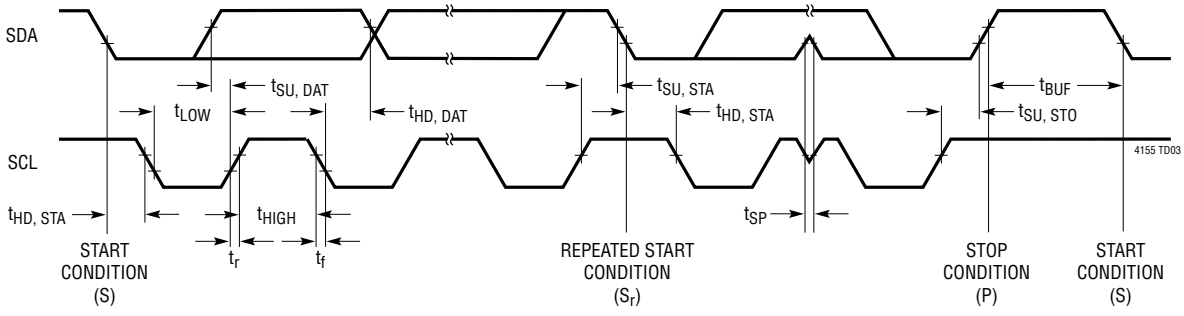
I²C Write Protocol



I²C Read Protocol



Timing Diagram



OPERATION

I²C

Table 2. I²C Map

REGISTER	ACCESS	SUB ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
REG0	WRITE/ READBACK	0x00	DISABLE INPUT UVCL	0 RESERVED	LOCKOUT USB OTG ID PIN	USB CURRENT LIMIT				
REG1	WRITE/ READBACK	0x01	INPUT PRIORITY	SAFETY TIMER		WALL CURRENT LIMIT				
REG2	WRITE/ READBACK	0x02	CHARGE CURRENT				FLOAT VOLTAGE		C/x DETECTION	
REG3	READ	0x03	CHARGER STATUS			ID PIN DETECTION STATUS	BOOST ENABLE STATUS	THERMISTOR STATUS		LOW BATTERY STATUS
REG4	READ	0x04	EXTERNAL POWER GOOD	USBSNS GOOD	WALLSNS GOOD	INPUT CURRENT LIMIT ACTIVE	INPUT UVCL ACTIVE	OVP ACTIVE	OTG FAULT	BAD CELL FAULT
REG5	READ	0x05	THERMISTOR VALUE							THERMIS-TOR WARNING
REG6	WRITE/ READBACK CLEAR INTERRUPT* DISARM SHIP-AND-STORE MODE*	0x06	ENABLE CHARGER INTERRUPTS	ENABLE FAULT INTERRUPTS	ENABLE EXTERNAL POWER INTERRUPTS	ENABLE USB OTG INTERRUPTS	ENABLE INPUT CURRENT LIMIT INTERRUPTS	ENABLE INPUT UVCL INTERRUPTS	ENABLE USB On-The-Go	0 RESERVED
REG7	WRITE ARM SHIP-AND-STORE MODE**	0x07	0 REQUIRED	0 REQUIRED	0 REQUIRED	0 REQUIRED	0 REQUIRED	0 REQUIRED	0 REQUIRED	0 REQUIRED

*Interrupts are cleared and ship-and-store mode is disarmed during the acknowledge clock cycle following a full data byte written to sub address 0x06. Reading data from sub address 0x06 has no effect.

**Ship-and-store mode is armed during the acknowledge clock cycle following a full data byte written to sub address 0x07. The data written to sub address 0x07 is ignored. Reading from sub address 0x07 has no effect and the returned data is undefined, independent of the arming state of ship-and-store mode.

OPERATION

Introduction

The LTC4156 is an advanced I²C controlled power manager and $LiFePO_4$ battery charger designed to efficiently transfer up to 15W from a variety of sources while minimizing power dissipation and easing thermal budgeting constraints. By decoupling V_{OUT} and the battery, the innovative instant-on PowerPath architecture ensures that the application is powered immediately after external voltage is applied, even with a completely dead battery, by prioritizing power to the application.

Since V_{OUT} and the battery are decoupled, the LTC4156 includes an ideal diode controller. The ideal diode from the battery to V_{OUT} guarantees that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS}.

The LTC4156 includes a monolithic step-down switching battery charger for USB support, wall adapters and other 5V sources. By incorporating a unique input current measurement and control system, the switching charger interfaces seamlessly to wall adapters and USB ports without requiring application software to monitor and adjust system loads. Because power is conserved, the LTC4156 allows the load current on V_{OUT} to exceed the current drawn by the USB port or wall adapter, making maximum use of the allowable power for battery charging without exceeding the USB or wall adapter power delivery specifications. A wide range of input current settings as well as battery charge current settings are available for selection by I²C.

Using only one inductor, the switching PowerPath can operate in reverse, boosting the battery voltage to provide 5V power at its input pin for USB On-The-Go applications. In the USB-OTG mode, the switching regulator supports USB high power loads up to 500mA. Protection circuits ensure that the current is limited and ultimately the channel is shut down if a fault is detected on the USB connector.

To support USB low power mode, the LTC4156 can deliver power to the external load and charge the battery through a linear regulator while limiting input current to less than 100mA.

The LTC4156 also features a combination overvoltage protection circuit/priority multiplexer which prevents damage to its input caused by accidental application of high voltage and selects one of two high power input connectors based on priority.

A thermistor measurement subsystem periodically monitors and reports the battery's thermistor value via the onboard I²C port. The same circuit then reports when dangerous battery temperatures are reached and can autonomously pause charging.

To minimize battery drain when a device is connected to a suspended USB port, an LDO from V_{BUS} to V_{OUT} provides the allowable USB suspend current to the application.

An interrupt subsystem can be enabled to alert the host microprocessor of various status change events so that system parameters can be varied as needed by system software. Several status change event categories are maskable for maximum flexibility.

To eliminate battery drain between manufacture and sale, a ship-and-store feature reduces the already low battery standby current to nearly zero and optionally disconnects power from downstream circuitry.

An input undervoltage amplifier optionally prevents the input voltage from decreasing below 4.3V when a resistive cable or current limited supply is providing input power to the LTC4156.

Finally, the LTC4156 has considerable adjustability built in so that power levels and status information can be controlled and monitored via the simple 2-wire I²C port.

Input Current-Limited Step-Down Switching Charger

Power delivery from V_{BUS} to V_{OUT} is controlled by a 2.25MHz constant-frequency step-down switching regulator. The switching regulator reduces output power in response to one of six regulation loops, including battery voltage, battery charge current, output voltage, input current, input undervoltage, and external PMOS charger FET power dissipation. For USB low power (100mA) and USB suspend (2.5mA) modes, the switching regulator is disabled and power is transmitted through a linear regulator.

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Battery Float Voltage Regulation

When the battery charger is enabled, the switching regulator will reduce its output power to prevent V_{BATSNS} from exceeding the programmed battery float voltage, V_{FLOAT}. The float voltage may be selected from among four possible choices via the I²C interface using bits VFLOAT[1:0]. Refer to Table 11.

Battery Charge Current Regulation and Low Cell Trickle Charge

The switching regulator will also reduce its output power to limit battery charge current, I_{CHARGE}, to a programmed maximum value. The battery charge current is programmed using both a resistor, R_{PROG}, between PROG and ground to set default maximum charge current plus I²C adjustability to optionally reduce programmed charge current. The battery charge current loop mirrors a precise fraction of the battery charge current, I_{BAT}, to the PROG pin, then reduces switching regulator output power to limit the resultant voltage, V_{PROG}, to one of fifteen possible servo reference voltages.

The following expression may be used to determine the battery charge current at any time by sampling the PROG pin voltage.

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

This expression may also be used to calculate the required value of R_{PROG} for any desired charge current. The resistor value required to program default maximum charge current may be found by substituting V_{PROG} = 1.200 and solving for R_{PROG}. The other fourteen settings are I²C selectable using ICHARGE[3:0] and reduce the charge current in 6.25% steps. The resulting limits may be found by substituting R_{PROG} and the relevant V_{PROG} servo voltage from Table 10.

The maximum charge current should be set based on the cell size and maximum charge rate without regard to input current setting or input power source.

The LTC4156 monitors the voltage across the external PMOS transistor and automatically reduces the current regulation servo voltage at V_{PROG} to limit power dissipation in the transistor. During normal operation, the PMOS channel is fully enhanced and power dissipation is typically under 100mW. Starting when the battery voltage is below approximately 2.94V, the charge current servo voltage will be gradually reduced from its I²C programmed value to a minimum value between 75mV and 100mV when the battery is below V_{LOWBAT}, typically 2.8V. This charge current reduction has the combined effect of protecting the external PMOS transistor from damage due to excessive heat, while also trickle charging the excessively depleted cell to maximize battery health and lifetime. Peak power dissipation in the external PMOS transistor is limited to approximately 700mW. Figure 1 shows the relationship between battery voltage, charge current and power dissipation.

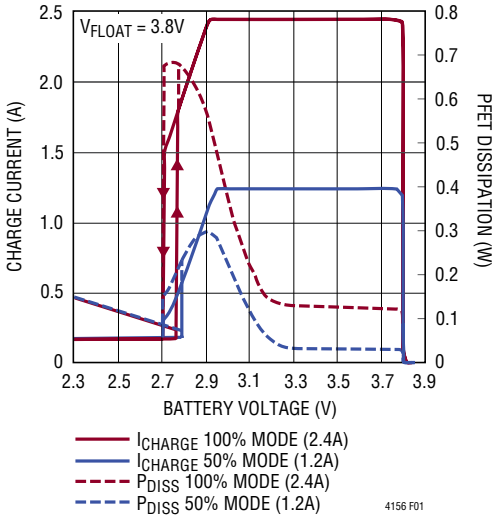

Figure 1. V_{OUT} Minimum Voltage Regulation

V_{OUT} Voltage Regulation

A third control loop reduces power delivery by the switching regulator in response to the voltage at V_{OUT}, which has a nonprogrammable servo voltage of 4.35V. When the battery charger is enabled, V_{OUT} is connected to BATSNS through the internal charge current sense resistor and the external PMOS battery FET. The two node voltages will differ only by the I • R drop through the two devices, effectively keeping V_{OUT} below its servo point for the duration of the charge cycle.

The LTC4156 will attempt to prevent V_{OUT} from falling below approximately 3.19V when the battery is deeply

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discharged. This feature allows instant-on operation when the low state of charge would otherwise prevent operation of the system. If the system load plus battery charger load exceeds the available input power, battery charge current will be sacrificed to prioritize the system load and maintain the switching regulator output voltage while continuing to observe the input current limit. If the system load alone exceeds the power available from the input, the output voltage must fall to deliver the additional current, with supplemental current eventually being supplied by the battery.

Input Current Regulation

To meet the maximum load specification of the available supply (USB/wall adapter), the switching regulator contains a measurement and control system which ensures that the average input current is below the level programmed at the CLPROG1 or CLPROG2 pin and the I²C port. Connecting a single 1% tolerance resistor of the recommended value to both the CLPROG1 and CLPROG2 pins guarantees compliance with the 2.5mA, 100mA, 500mA, and 900mA USB 2.0/3.0 current specifications, while also permitting other I²C selectable current limits up to 3A. The input current limit is independently selectable for each of the two inputs, with the USBILIM[4:0] and WALLILIM[4:0] bits in the I²C port. The USB input current limit setting resets to 100mA when power is removed from its respective input. The WALL input current limit setting resets to 100mA when power is removed from both the USB and WALL inputs. Refer to Alternate Default Input Current Limit in the Operation section to program a non USB compliant default input current limit for use with wall adapters or other power sources. Refer to Table 7 for a complete listing of I²C programmable input current limit settings.

If the combined external load plus battery charge current is large enough to cause the switching power supply to reach the programmed input current limit, the battery charger will reduce its charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the battery charge current is programmed to exceed the allowable input power, the specification for average input current will not be violated; the battery charger will reduce its current as needed. Furthermore, if the load at V_{OUT} exceeds the programmed power level from V_{BUS}, the extra load current will be drawn from the battery via the ideal diode independent of whether the battery charger is enabled or disabled.

Input Undervoltage Current Limit

The LTC4156 can tolerate a resistive connection to the input power source by automatically reducing power transmission as the V_{BUS} pin drops to 4.3V preventing a possible UVLO oscillation. The undervoltage current limit feature can be disabled by I²C using the DISABLE_INPUT_UVCL bit. Refer to Table 5.

USB On-The-Go 5V Boost Converter

The LTC4156 switching regulator can be operated in reverse to deliver power from the battery to V_{BUS} while boosting the V_{BUS} voltage to 5V. This mode can be used to implement features such as USB On-The-Go without any additional magnetics or other external components.

The step-up switching regulator may be enabled in one of two ways. The LTC4156 can optionally monitor the ID pin of a USB cable and autonomously start the step-up regulator when a host-side A/B connector is detected with a grounded ID pin. The switching regulator may also be enabled directly with the REQUEST_OTG I²C command. Note that the step-up regulator will not operate if input power is present on either the USB or WALL input, or if the battery voltage is below V_{LOWBAT}, typically 2.8V. The I²C status bits OTG_ENABLED, LOWBAT and OTG_FAULT can be used to determine if the step-up converter is running. Refer to ID Pin Detection in the Operation section for more information about the autonomous step-up regulator start-up.

The step-up regulator only provides power to the USB input. It is not possible to provide power to the WALL input. The I²C PRIORITY setting has no effect on step-up regulator operation. Refer to Dual Input Overvoltage Protection and Undervoltage Lockout in the Operation section for more information about multiple input operation.

The switching regulator is guaranteed to deliver 500mA to V_{BUS} and will limit its output current to approximately 1.4A while allowing V_{BUS} to fall when overloaded. If a short-circuit fault is detected, the channel will be shut down after approximately 8ms and the problem will be reported with the I²C status bit OTG_FAULT.

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ID Pin Detection

For USB On-The-Go compatibility, the step-up switching regulator can optionally start autonomously when the grounded ID pin in the A side of an On-The-Go cable is detected.

The ID pin is monitored at all times. Its status is reported in the I²C bit ID_DETECT, reporting true when the ID pin is grounded. Optionally, any change in ID_PIN_DETECT may trigger an interrupt request to notify the system processor. Unless the I²C LOCKOUT_ID_PIN bit has been set, ID pin detection will also automatically start the step-up regulator. Note that LOCKOUT_ID_PIN locks out automatic start-up, but not monitoring of the ID pin. Also, the REQUEST_OTG command may be used to enable the step-up regulator, independent of the state of ID_PIN_DETECT and LOCKOUT_ID_PIN. Note that the regulator will not start if input power is already present on either input. The I²C status bits OTG_ENABLED and OTG_FAULT can be used to determine if the regulator is running.

The ID pin detection circuit will report a short on the ID pin for ID pin impedances lower than approximately 24k. The USB Battery Charging Specification Rev 1.1 added additional signaling to the ID pin, specifying other possible ID pin resistances of RID_A, RID_B and RID_C. These impedances are all larger than the 24k threshold and will typically not cause an ID pin short detection.

Dual Input Overvoltage Protection and Undervoltage Lockout

The LTC4156 can provide overvoltage protection to its two power inputs with minimal external components, as shown in Figure 2.

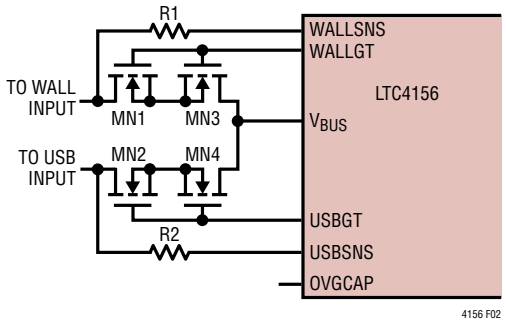

Figure 2. Dual-Input Overvoltage Protection Multiplexer

The LTC4156 acts as a shunt regulator when the input is overvoltage, clamping USBSNS or WALLSNS to 6V. Resistors R1 and R2 should be 3.6k and be rated appropriately for the worst-case power dissipation during an overvoltage event. The power dissipated in the resistor is given by the following expression:

$$P_{RESISTOR} = \frac{(V_{OVERVOLTAGE} - 6V)^2}{3.6k}$$

For example, a typical 0201 size resistor would be appropriate for possible overvoltage events up to 19V. An 0402 size resistor would be appropriate up to 20V, an 0603 up to 24V, an 0805 up to 27V, and a 1206 up to 35V. Additional power derating may be necessary at elevated ambient temperature. The maximum allowed shunt current into the USBSNS and WALLSNS pins constrains the upper limit of protection to 77V.

The drain-source voltage rating, V_{DS}, of N-channel FETs MN1-MN2 must be appropriate for the level of overvoltage protection desired, as the full magnitude of the input voltage is applied across one of these devices.

The drain-source voltage rating of N-channel FETs MN3-MN4 need only be as high as the protection threshold, typically 6.0V. MN3-MN4 are not required for overvoltage protection, but are required to block current from circulating from one input to the other through the unused channel's FET body diode. For single-input applications, only a single power FET is required. Refer to Alternate Input Power Configurations in the Applications Information section for implementation details.

Negative voltage protection can be added by reconfiguring the circuit without adding any additional power transistors. Refer to Alternate Input Power Configurations in the Applications Information section for implementation details.

For an input (USB or WALL) to be considered a valid power source, it must satisfy three conditions. First, it must be above a minimum voltage, V_{UVLO}. Second, it must be greater than the battery voltage by a minimum of V_{DUVLO}. Lastly, it must be below the overvoltage protection threshold voltage, V_{OVLO}. The USBSNS and WALLSNS pins each draw a small current which causes a voltage offset between the USB and WALL inputs and the USBSNS and

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WALLSNS pins. The voltage threshold values previously listed and specified in the Electrical Characteristics table are valid when each input is connected to its respective sense pin through a 3.6k resistor.

The status of the USB and WALL inputs is monitored continuously and reported by I²C, with the option of generating several interrupts. When all three conditions previously listed are true, the LTC4156 will report the input valid by asserting USBSNSGD or WALLSNSGD in the I²C port. Optionally, if external power interrupts are enabled, an interrupt request will be generated.

When power is applied simultaneously to both inputs, the LTC4156 will draw power from the WALL input by default. If the I²C PRIORITY bit is asserted, the LTC4156 will instead draw power from the USB input when both inputs are present. The USB On-The-Go step-up regulator delivers power only to the USB input, and the PRIORITY bit is ignored in this mode. The input current limits USBILIM[4:0] and WALLILIM[4:0] also reset to 100mA default mode under different criteria. In all other respects, the two inputs are identical.

An optional capacitor may be placed between the OVGCAP pin and GND to minimize input current disruption when switching from one input to the other while operating at high power levels. The capacitor must be rated to withstand at least 13V and should be approximately ten times larger than the total gate capacitance of the series NMOS power transistors. Capacitance on this pin can also be used to slow the gate charging if the application requires controlled inrush current to any additional input capacitance on the V_{BUS} pin. If fast switching between input or inrush control is not necessary, OVGCAP may be left unconnected.

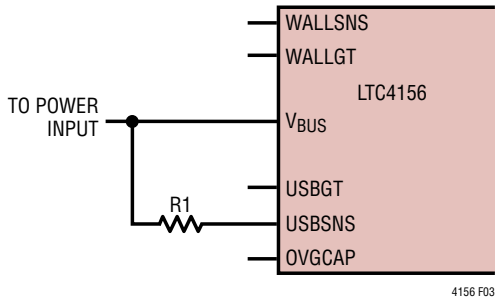

Figure 3. No Overvoltage Protection

If overvoltage protection is not necessary in the application, connect USBSNS to V_{BUS} with a 3.6k resistor, as shown in Figure 3. If the USB On-The-Go step-up regulator is not used in the application, it is also possible to connect WALLSNS to V_{BUS} through 3.6k and leave USBSNS open.

100mA Linear Battery Charger Mode

The LTC4156 features a mode to support USB low power operation. Total input current to the LTC4156 is guaranteed to remain below 100mA in this mode when the recommended resistor is used on the CLPROG2 pin. The step-down switching regulator does not operate in this mode. Instead, a linear regulator provides power from V_{BUS} to V_{OUT} and the battery. The linear battery charger follows the same constant-current/constant-voltage algorithm as the switching regulator, but regulates input current rather than battery charge current. The voltage on the CLPROG2 pin represents the input current in this mode, using the expression:

$$I_{VBUS} = \frac{V_{CLPROG2}}{R_{CLPROG2}} \bullet (80)$$

Battery charge current is represented by the voltage on the PROG pin, but it is not regulated in this mode.

$$I_{CHARGE} = \frac{V_{PROG}}{R_{PROG}} \bullet (1000)$$

V_{OUT} will generally be very close to the battery voltage when the battery charger is enabled, except when the battery voltage is very low, the LTC4156 will increase the impedance between V_{OUT} and BATSNS to facilitate instant-on operation. If the system load plus battery charge current exceeds the available input current, battery charge current will be sacrificed to give priority to the load. If the system load alone exceeds the available input current, V_{OUT} must fall to the battery voltage so that the battery may provide the supplemental current.

The battery will charge to the float voltage specified by the I²C setting VFLOAT[1:0]. See Table 11.

When the battery charger is disabled or terminated, V_{OUT} will be regulated to 4.35V.

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2.5mA Linear Suspend Mode

The LTC4156 can supply a small amount of current from V_{BUS} to V_{OUT} to power the system and reduce battery discharge when the product has access to a suspended USB port. When the system load current is less than the current available from the suspended USB port, the voltage at V_{OUT} will be regulated to 4.35V. If the system load current exceeds USB input current limit, the voltage at V_{OUT} will fall to the battery voltage and any supplemental current above that available from the USB port will be supplied by the battery. CLPROG2 will servo to 103mV in current limit. Battery charging is disabled in suspend mode. Either the USB or WALL input may utilize this current limited suspend mode by programming the appropriate setting in the respective USBILIM or WALLILIM register.

Ideal Diode and Minimum V_{OUT} Controller

The LTC4156 features an ideal diode controller to ensure that the system is provided with sufficient power even when input power is absent or insufficient. This requires an external PMOS transistor with its source connected to CHGSNS, gate to BATGATE, and drain to BATSNS. The controller modulates the gate voltage of the PMOS transistor to allow current to flow from the battery to V_{OUT} to power the system while blocking current in the opposite direction to prevent overcharging of the battery.

The ideal diode controller has several modes of operation. When input power is available and the battery is charging, the PMOS gate will generally be grounded to maximize conduction between the switching regulator and the battery for maximum efficiency. If the battery is deeply discharged, the LTC4156 will automatically increase the impedance between the switching regulator and the battery enough to prevent V_{OUT} from falling below approximately 3.19V. Power to the system load is always prioritized over battery charge current. Increasing the impedance between V_{OUT} and the battery does not necessarily affect the battery charge current, but it may do so for one of the following two reasons:

1. The charge current will be limited to prevent excessive power dissipation in the external PMOS as it becomes more resistive. Charge current reduction begins when the voltage across the PMOS reaches approximately 250mV, and can reduce the charge current as low as 8% full scale. Maximum power dissipation in the PMOS is limited to approximately 700mW with R_{PROG} = 499Ω.
2. When limited power is available to the switching regulator because either the programmed input current limit or input undervoltage current limit is active, charge current will automatically be reduced to prioritize power delivery to the system at V_{OUT}. V_{OUT} will be maintained at 3.19V as long as possible without exceeding the input power limitation. If the system load alone requires more power than is available from the input after charge current has been reduced to zero, V_{OUT} must fall to the battery voltage as the battery begins providing supplemental power.

When input power is available, but the battery charger is disabled or charging has terminated, V_{OUT} and the battery are normally disconnected to prevent overcharging the battery. If the power required by the system should exceed the power available from the input, either because of input current limit or input undervoltage current limit, V_{OUT} will fall to the battery voltage and any additional current required by the load will be supplied by the battery through the ideal diode.

When input power is unavailable, the ideal diode switches to a low power mode which maximizes conduction and power transmission efficiency between V_{OUT} and the battery by grounding the PMOS gate.

Finally, when ship-and-store mode is activated, the ideal diode is shut down and BATGATE is driven to the battery voltage to prevent conduction through the PMOS. Note that with a single FET, conduction to V_{OUT} is still possible through the body connection diode. Refer to Low Power Ship-and-Store Mode in the Operation section for more information about this mode.

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Low Power Ship-and-Store Mode

The LTC4156 can reduce its already low standby current to approximately 1µA in a special mode designed for shipment and storage. Unlike normal standby mode, in this mode the external PMOS gate is driven to the battery voltage to disable FET conduction through the external PMOS. This mode may be used to cut off all power to any downstream load on V_{OUT} to maximize battery life between product manufacture and sale. Note that the bulk connection inside the external PMOS will provide a conductive path from the battery to V_{OUT}, independent of the voltage on its gate. To block conduction to V_{OUT}, typically two PMOS transistors must be connected in series with either the sources or drains of each device connected in the center, as shown in Figure 4. If the application does not require the battery to be isolated from downstream devices, significant power savings in the LTC4156 may still be realized by activating this mode.

Ship-and-store mode is armed following the acknowledge of any data byte written to sub address 0x07 by the I^2C bus master. The contents of the data byte are ignored, but the full byte and acknowledge clock cycle must be sent. Ship-and-store mode is activated as V_{BUS} falls below approximately 1V, or immediately if no input power is present when the I^2C command is issued. V_{BUS} quiescent current falls to nearly zero when power is removed from the USB and WALL inputs, resulting in a delay of up to several hours for V_{BUS} to self-discharge to the 1V activation threshold. Faster activation may be achieved by connecting a 1M resistor between V_{BUS} and GND. Reading from sub address 0x07 has no effect on arming or activation and the returned data is undefined, independent of the arming or activation state.

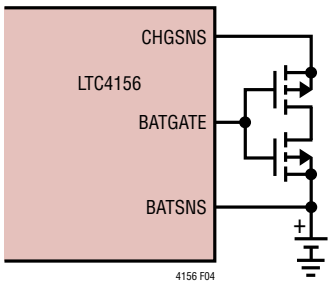

Figure 4. Ship-and-Store Mode Required Components to Enforce Downstream (V_{OUT}) Shutdown

Once engaged, ship-and-store mode can be disengaged by applying power to the USB or WALL input or by writing any full data byte and acknowledge clock cycle to sub address 0x06 if the I^2C bus master is still powered.

I^2C Interface

The LTC4156 may communicate with a bus master using the standard I^2C 2-wire interface. The Timing Diagram shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC4156 is both a slave receiver and slave transmitter. The I^2C control signals, SDA and SCL, are scaled internally to the DVCC supply. DVCC should be connected to the same power supply as the bus pull-up resistors.

The I^2C port has an undervoltage lockout on the DVCC pin. When DVCC is below approximately 1V, the I^2C serial port is cleared, the LTC4156 is set to its default configuration, pending interrupts will be cleared, and future interrupts will be disabled.

Bus Speed

The I^2C port is designed to operate at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I^2C compliant master device. It also contains input filters designed to suppress glitches.

START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC4156, the master may transmit a STOP condition which commands the LTC4156 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH.

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Byte Format

Each frame sent to or received from the LTC4156 must be eight bits long, followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC4156 most significant bit (MSB) first.

Master and Slave Transmitters and Receivers

Devices connected to an I²C bus may be classified as either master or slave. A typical bus is composed of one or more master devices and a number of slave devices. Some devices are capable of acting as either a master or a slave, but they may not change roles while a transaction is in progress.

The transmitter/receiver relationship is distinct from that of master and slave. The transmitter is responsible for control of the SDA line during the eight bit data portion of each frame. The receiver is responsible for control of SDA during the ninth and final acknowledge clock cycle of each frame.

All transactions are initiated by the master with a START or repeat START condition. The master controls the active (falling) edge of each clock pulse on SCL, regardless of its status as transmitter or receiver. The slave device never brings SCL LOW, but may extend the SCL LOW time to implement clock stretching if necessary. The LTC4156 does not clock stretch and will never hold SCL LOW under any circumstance.

The master device begins each I²C transaction as the transmitter and the slave device begins each transaction as the receiver. For bus write operations, the master acts as the transmitter and the slave acts as receiver for the duration of the transaction. For bus read operations, the master and slave exchange transmit/receive roles following the address frame for the remainder of the transaction.

Acknowledge

The acknowledge signal (ACK) is used for handshaking between the transmitter and receiver. When the LTC4156 is written to, it acknowledges its write address as well as the subsequent data bytes as a slave receiver. When it is read from, the LTC4156 acknowledges its read address as a slave receiver. The LTC4156 then changes to a slave transmitter and the master receiver may optionally acknowledge receipt of the following data byte from the LTC4156.

The acknowledge related clock pulse is always generated by the bus master. The transmitter (master or slave) releases the SDA line (HIGH) during the acknowledge clock cycle. The receiver (slave or master) pulls down the SDA line during the acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

When the LTC4156 is read from, it releases the SDA line after the eighth data bit so that the master may acknowledge receipt of the data. The I²C specification calls for a not acknowledge (NACK) by the master receiver following the last data byte during a read transaction. Upon receipt of the NACK, the slave transmitter is instructed to release control of the bus. Because the LTC4156 only transmits one byte of data under any circumstance, a master acknowledging or not acknowledging the data sent by the LTC4156 has no consequence. The LTC4156 will release the bus in either case.

Slave Address

The LTC4156 responds to a 7-bit address which has been factory programmed to 0b0001_001[R/$\overline{W}$]. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTC4156, and 1 when reading data from it. Considering the address an 8-bit word, then the write address is 0x12, and the read address is 0x13. The LTC4156 will acknowledge both its read and write addresses.

Sub Addressed Access

The LTC4156 has four command registers for control input and three status registers for status reporting. They are accessed by the I²C port via a sub addressed pointer system where each sub address value points to one of the seven control or status registers within the LTC4156. The sub address pointer is always the first byte written immediately following the LTC4156 write address during bus write operations. The sub address pointer value persists after the bus write operation and will determine which data byte is returned by the LTC4156 during any