Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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35V/3.2A Multi-Cell $LiFePO_4$ Step-Down Battery Charger with PowerPath and I^2C Telemetry

FEATURES

- **$LiFePO_4$ Battery Charger with Termination**
- **Wide Charging Input Voltage Range: 4.5V to 35V**
- **High Efficiency Synchronous Operation**
- **16-Bit Digital Telemetry System Monitors V_{BAT}, I_{BAT}, R_{BAT}, T_{BAT}, T_{DIE}, V_{IN}, I_{IN}, V_{OUT}**
- **Charges 1-9 Lithium Iron Phosphate Cells**
- Input Undervoltage Charge Current Limit Loop
- Input MPPT for Solar Panel Inputs
- Input Current Limit Prioritizes System Load Output
- Low Loss PowerPath™
- Instant-On Operation with Discharged or Missing Battery
- JEITA Temperature Controlled Charging
- Pin Compatible with Li-Ion and SLA Versions

APPLICATIONS

- Medical Instruments
- USB-C Power Delivery
- Industrial Handhelds
- Ruggedized Notebooks
- Tablet Computers

DESCRIPTION

The LTC®4162-F is an advanced monolithic synchronous step-down switching battery charger and PowerPath™ manager that seamlessly manages power distribution between input sources such as wall adapters, backplanes, solar panels, etc., and a rechargeable lithium iron phosphate battery.

A high resolution measurement system provides extensive telemetry information for circuit voltages, currents, battery resistance and temperature which can all be read back over the I^2C port. The I^2C port can also be used to configure many charging parameters including charging voltages and currents, termination algorithms and numerous system status alerts.

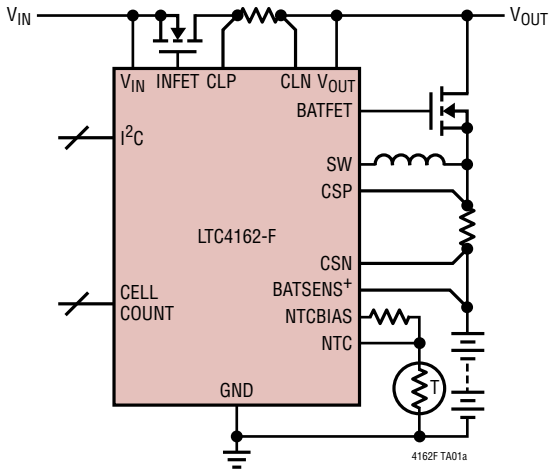
The LTC4162-F can charge $LiFePO_4$ cell stacks from 1 cell to 9 cells with as much as 3.2A of charge current.

The power path topology decouples the output voltage from the battery allowing a portable product to start up instantly under very low battery voltage conditions.

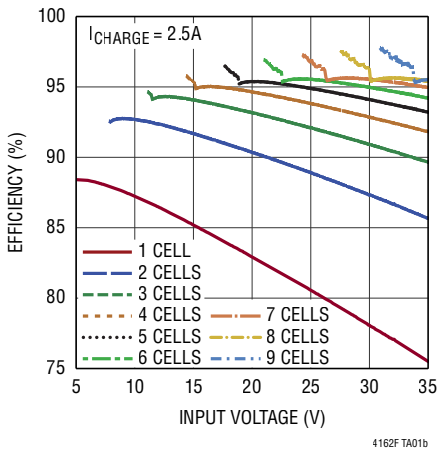
The LTC4162-F is available in a thermally enhanced 28-pin 4mm × 5mm × 0.75mm QFN surface mount package.

TYPICAL APPLICATION

1-9 Cell, 3.2A Step-Down Switching Battery Charger with PowerPath



Charging Efficiency vs Input Voltage by Cell Count



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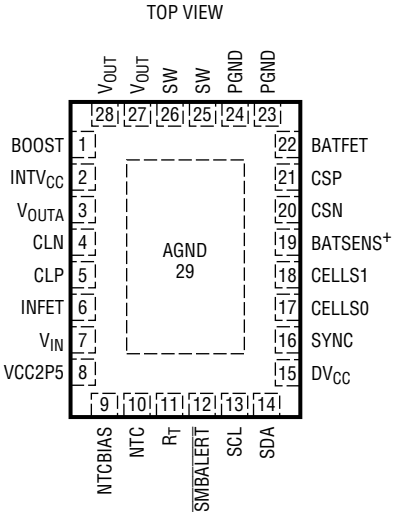
ABSOLUTE MAXIMUM RATINGS

(Note 1)

BATSENS+, V_{IN}, CSP, CSN, CLP, CLN, V_{OUT}, V_{OUTA}..... –0.3V to 36V
CSP to CSN, CLP to CLN.....±0.3V
CELLSO, CELLS1, SYNC ..... –0.3V to INTVCC
DV_{CC} ..... –0.3V to 5.5V
SDA, SCL, $\overline{SMBALERT}$..... –0.3V to DV_{CC}
I_{SW} ..... ±3.5A
Operating Junction Temperature Range (Notes 2, 4).....–40 to 125°C
Storage Temperature Range .....–65 to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

ORDER INFORMATION

PART NUMBER	PART MARKING*	TAPE AND REEL	TEMP GRADE	DESCRIPTION	TEMPERATURE RANGE
LTC4162EUFD-FAD#PBF	4162E		E	I^2C Adjustable Voltage	–40°C to 125°C
LTC4162EUFD-FST#PBF	4162G		E	3.6V Fixed Voltage	–40°C to 125°C
LTC4162EUFD-FFS#PBF	4162F		E	3.8V Rapid Charge	–40°C to 125°C
LTC4162EUFD-FADM#PBF	4162P		E	I^2C Adjustable Voltage MPPT ON	–40°C to 125°C
LTC4162EUFD-FSTM#PBF	4162S		E	3.6V Fixed Voltage MPPT ON	–40°C to 125°C
LTC4162EUFD-FFSM#PBF	4162R		E	3.8V Rapid Charge MPPT ON	–40°C to 125°C
LTC4162EUFD-FAD#TRPBF	4162E	✓	E	I^2C Adjustable Voltage	–40°C to 125°C
LTC4162EUFD-FST#TRPBF	4162G	✓	E	3.6V Fixed Voltage	–40°C to 125°C
LTC4162EUFD-FFS#TRPBF	4162F	✓	E	3.8V Rapid Charge	–40°C to 125°C
LTC4162EUFD-FADM#TRPBF	4162P	✓	E	I^2C Adjustable Voltage MPPT ON	–40°C to 125°C
LTC4162EUFD-FSTM#TRPBF	4162S	✓	E	3.6V Fixed Voltage MPPT ON	–40°C to 125°C
LTC4162EUFD-FFSM#TRPBF	4162R	✓	E	3.8V Rapid Charge MPPT ON	–40°C to 125°C
LTC4162IUFD-FAD#PBF	4162E		I	I^2C Adjustable Voltage	–40°C to 125°C
LTC4162IUFD-FST#PBF	4162G		I	3.6V Fixed Voltage	–40°C to 125°C
LTC4162IUFD-FFS#PBF	4162F		I	3.8V Rapid Charge	–40°C to 125°C
LTC4162IUFD-FADM#PBF	4162P		I	I^2C Adjustable Voltage MPPT ON	–40°C to 125°C

ORDER INFORMATION

PART NUMBER	PART MARKING*	TAPE AND REEL	TEMP GRADE	DESCRIPTION	TEMPERATURE RANGE
LTC4162IUFD-FSTM#PBF	4162S		I	3.6V Fixed Voltage MPPT ON	–40°C to 125°C
LTC4162IUFD-FFSM#PBF	4162R		I	3.8V Rapid Charge MPPT ON	–40°C to 125°C
LTC4162IUFD-FAD#TRPBF	4162E	✓	I	I^2C Adjustable Voltage	–40°C to 125°C
LTC4162IUFD-FST#TRPBF	4162G	✓	I	3.6V Fixed Voltage	–40°C to 125°C
LTC4162IUFD-FFS#TRPBF	4162F	✓	I	3.8V Rapid Charge	–40°C to 125°C
LTC4162IUFD-FADM#TRPBF	4162P	✓	I	I^2C Adjustable Voltage MPPT ON	–40°C to 125°C
LTC4162IUFD-FSTM#TRPBF	4162S	✓	I	3.6V Fixed Voltage MPPT ON	–40°C to 125°C
LTC4162IUFD-FFSM#TRPBF	4162R	✓	I	3.8V Rapid Charge MPPT ON	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 4). V_{IN} = 18V, DV_{CC} = 3.3V, R_{SNSI} = 10mΩ, R_{SNSB} = 10mΩ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
System Voltages and Currents							
V_{IN}	Input Supply Voltage		●	4.5		35	V
V_{BAT}	Battery Voltage		●	2.7		35	V
$I_{BATSENS+}$	Battery Drain Current	$V_{IN} - V_{BATSENS+} > V_{IN\_DUVLO}$, Terminated $V_{IN} - V_{BATSENS+} < V_{IN\_DUVLO}$ V_{IN} = 0, SHIPMODE Activated			0.5 54 2.8	1 100 5	µA µA µA
I_{VIN}	V_{IN} Drain Current	$V_{IN} - V_{BATSENS+} > V_{IN\_DUVLO}$, Terminated			115	200	µA
Switching Battery Charger							
V_{CHARGE}	Range Resolution (5 Bits) Accuracy	Per cell_count	 ●		3.4125–3.8 12.5 –0.5 –1.5	 0.5 1.5	V mV % %
I_{CHARGE} Servo Voltage ($V_{CSP} - V_{CSN}$)	Range Resolution (5 Bits) Accuracy	$I_{CHARGE} = (V_{CSP} - V_{CSN})/R_{SNSB}$ Note 5	 ●		1–32 1 –0.25 –0.75	 0.25 0.75	mV mV mV mV
I_{INLIM} Servo Voltage ($V_{CLP} - V_{CLN}$)	Range Resolution (6 Bits) Accuracy	$I_{IN} = (V_{CLP} - V_{CLN})/R_{SNSI}$ Note 6			0.5–32 0.5 –0.2	 0.2	mV mV mV
V_{INLIM}	Range Resolution (8 Bits) Full Scale Accuracy				0.14–36 140.625 –1	 1	V mV %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 4). V_{IN} = 18V, DV_{CC} = 3.3V, R_{SNSI} = 10mΩ, RSNSB = 10mΩ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{OSC}	Switching Frequency	R_T = 63.4k	●	1.4	1.5	1.6	MHz
D_{MAX}	Maximum Duty Cycle				99.5		%
R_{SWITCH}	Primary Switch On-Resistance				90		mΩ
R_{RECT}	Rectifier Switch On-Resistance				90		mΩ
I_{PEAK}	Peak Inductor Current Limit	Note 3			45mV/R_{SNSB}		A
System Controls							
V_{IN_UVLO}	V_{IN} Charger Enable Input Undervoltage Lockout	Rising Threshold Hysteresis		4.2	4.4 0.2	4.6	V V
V_{IN_DUVLO}	V_{IN} to BATSENS+ Charger Enable Differential Undervoltage Lockout	Rising Threshold Hysteresis		100	150 170	200	mV mV
V_{IN_OVLO}	V_{IN} Charger Disable Overvoltage Lockout	Rising Threshold Hysteresis		37.6	38.6 1.4	40	V V
V_{INTVCC_UVLO}	$INTV_{CC}$ Telemetry Enable Undervoltage Lockout	Rising Threshold Hysteresis		2.75	2.85 0.12	2.95	V V
Telemetry A/D Measurement Subsystem							
I_{BAT} ($V_{CSP} - V_{CSN}$)	Resolution Offset Error Span Error	$I_{BAT} = (V_{CSP} - V_{CSN})/R_{SNSB}$ 0.32mV < $V_{CSP} - V_{CSN}$ < 32mV		 –0.15 –1	1.466	 0.15 1	µV /LSB mV %rdng
I_{IN} ($V_{CLP} - V_{CLN}$)	Resolution Offset Error Span Error	$I_{IN} = (V_{CLP} - V_{CLN})/R_{SNSI}$ 0.32mV < $V_{CLP} - V_{CLN}$ < 32mV		 –0.15 –1	1.466	 0.15 1	µV/LSB mV %rdng
V_{IN}	Resolution Offset Error Span Error	3V < V_{IN} < 35V		 –25 –1	1.649	 25 1	mV/LSB mV %rdng
$V_{BATSENS+}$ (Per cell_count)	Resolution Offset Error Span Error	2V < $V_{BATSENS+}$ < 3.8V		 –10 –1	192.4	 10 1	µV/LSB mV %rdng
V_{OUT}	Resolution Offset Error Span Error	3V < V_{OUT} < 35V		 –25 –1	1.653	 25 1	mV/LSB mV %rdng
$V_{NTC}/V_{NTCBIAS}$	Resolution Offset Error Span Error	0 < $V_{NTC}/V_{NTCBIAS}$ < 1		 –1 –1	45.833	 1 1	µV/V/LSB mV/V %rdng
T_die	Resolution Offset				0.0215 –264.4		°C/LSB °C
Serial Port, SDA, SCL, $\overline{\text{SMBALERT}}$							
DV_{CC}	Logic Reference Level		●	1.8		5.5	V
I_{DVCCQ}	DV_{CC} Current	SCL/SDA = DV_{CC}, 0kHz			0		µA
ADDRESS	I^2C Address				0b1101000[R/W]		
V_{IHI2C}	Input High Threshold			70			% DV_{CC}
V_{ILI2C}	Input Low Threshold					30	% DV_{CC}
V_{OLI2C}	Digital Output Low (SDA/SCL/$\overline{\text{SMBALERT}}$)	$I_{SDA/SCL/\overline{SMBALERT}}$ = 3mA				400	mV
F_{SCL}	SCL Clock Frequency					400	kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 4). V_{IN} = 18V, DV_{CC} = 3.3V, R_{SNSI} = 10mΩ, RSNSB = 10mΩ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{LOW}	LOW Period of SCL Clock			1.3			µs
t_{HIGH}	HIGH Period of SCL Clock			0.6			µs
t_{BUF}	Bus Free Time Between Start and Stop Conditions			1.3			µs
$t_{HD,STA}$	Hold Time, After (Repeated) Start Condition			0.6			µs
$t_{SU,STA}$	Setup Time after a Repeated Start Condition			0.6			µs
$t_{SU,STO}$	Stop Condition Set-Up Time			0.6			µs
$t_{HD,DAT(OUT)}$	Output Data Hold Time			0		900	ns
$t_{HD,DAT(IN)}$	Input Data Hold Time			0			ns
$t_{SU,DAT}$	Data Set-Up Time			100			ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
SYNC Pin							
VIHSYNC	Input High Threshold		●	1.5			V
VILSYNC	Input Low Threshold		●			0.2	V
Pin Leakages (NTC, CELLS0, CELLS1, SDA, SCL, SYNC, $\overline{\text{SMBALERT}}$)							
	Pin Current			–50		50	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4162 includes over-temperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 3: The safety current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current may result in device degradation or failure.

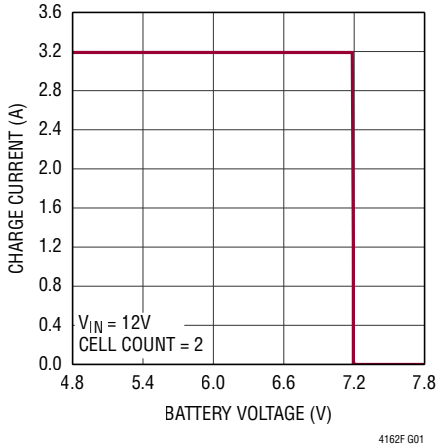
Note 4: The E-grade is tested under pulsed load conditions such that $T_J \approx T_A$. The E-grade is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The I-grade is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula $T_J = T_A + (P_D \bullet \theta J_A)$. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 5: Charge Current is given by the charger servo voltage, $V_{CSP-CSN}$, divided by the charge current setting resistor R_{SNSB}. Errors in the value of the external resistor contribute directly to the total charge current error.

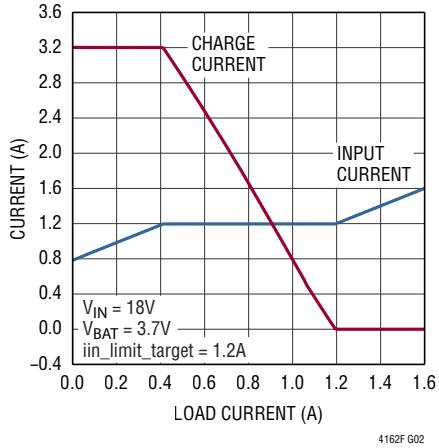
Note 6: Input Current is given by the $V_{CLP-CLN}$ servo voltage divided by the input current setting resistor R_{SNSI}. Errors in the value of the external resistor contribute directly to the total input current error.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

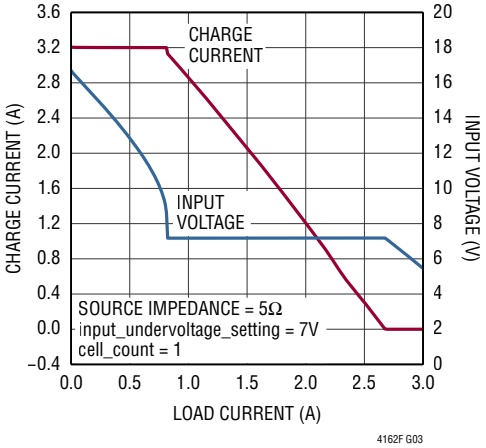
Charge Current vs Battery Voltage



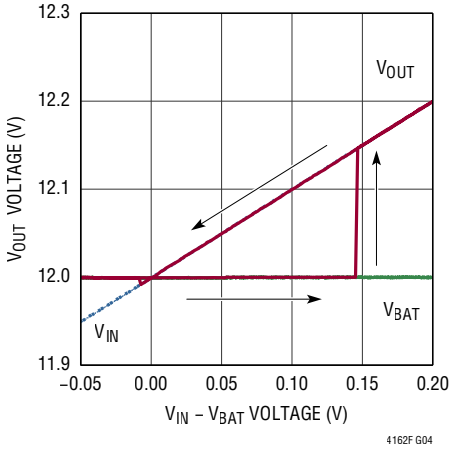
Input Current and Charge Current vs Load Current



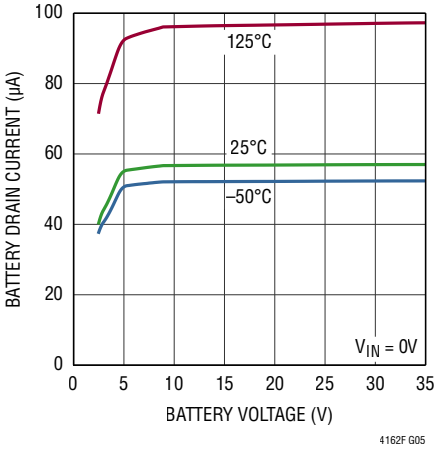
Resistive Source Input Voltage and Charge Current vs Load Current



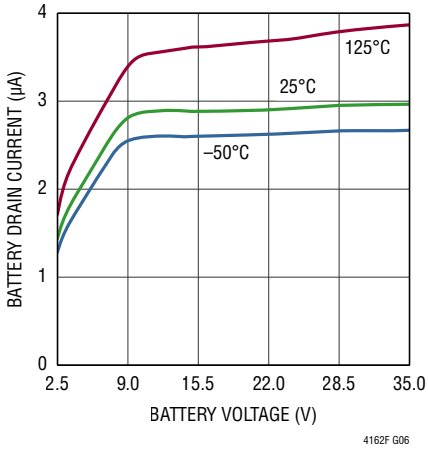
V_{OUT} vs V_{IN} Power Path Controller



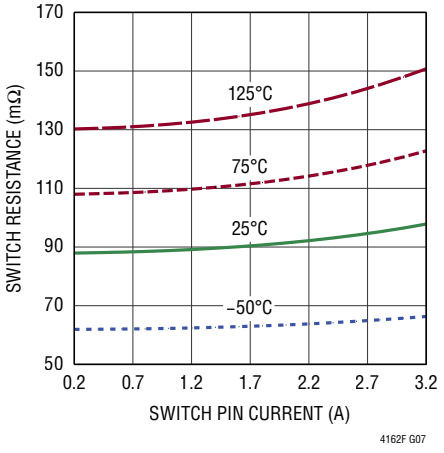
No Input Battery Drain Current vs Battery Voltage



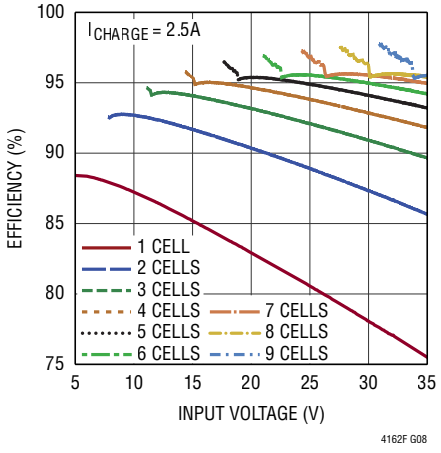
Ship Mode Battery Drain Current vs Battery Voltage



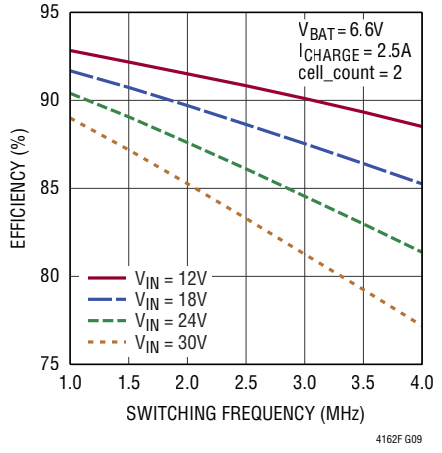
Top and Bottom Switch $R_{DS(ON)}$



Efficiency vs Input Voltage

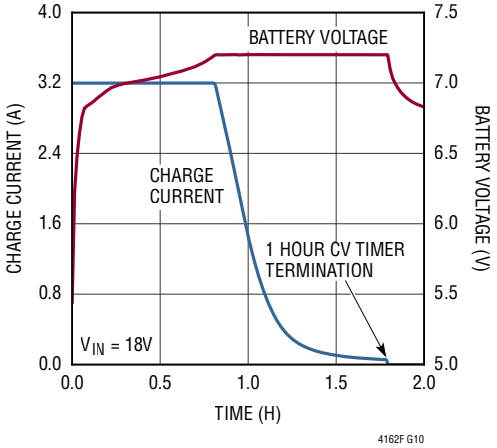


Efficiency vs Switching Frequency

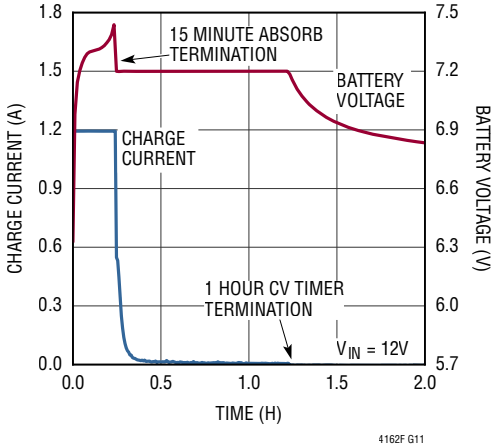


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

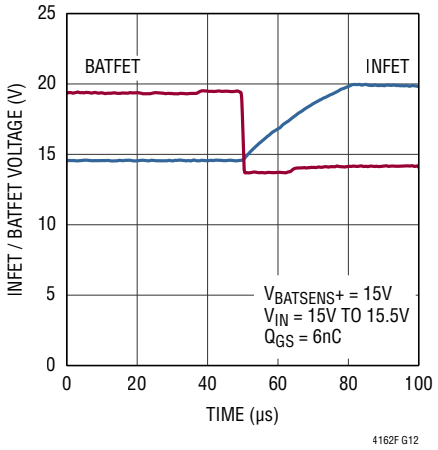
3.3Ah 2-Cell Battery Charge Current and Voltage vs Time



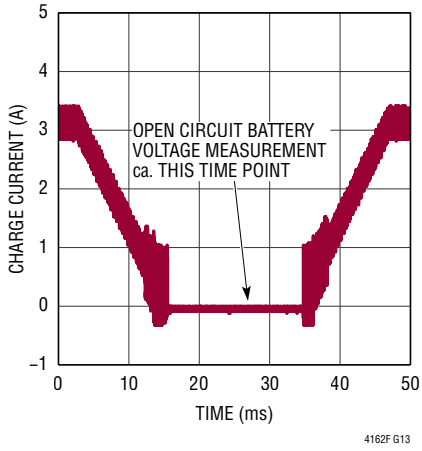
400mAh 2-Cell Battery Rapid Charge Current and Voltage vs Time



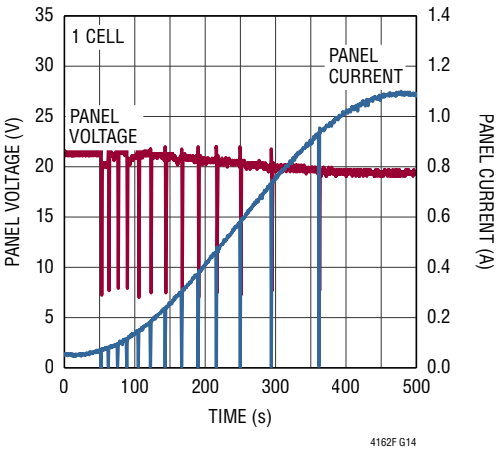
Example Power Path Handover



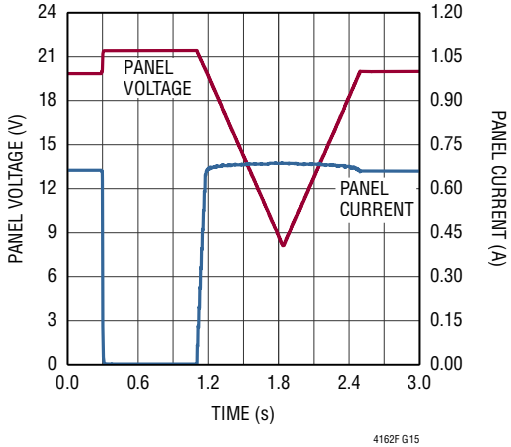
Charge Current During BSR Measurement Cycle



Light to Dark Solar Panel Tracking

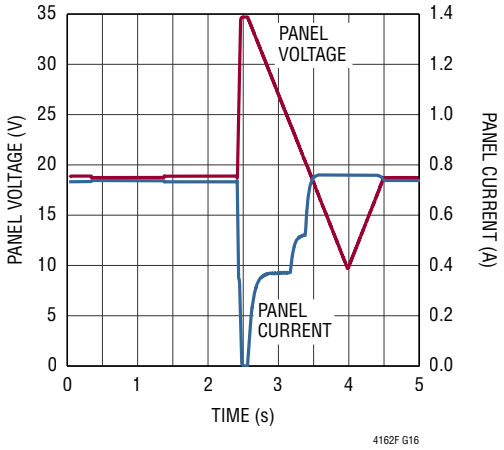


Solar Panel Global Sweep

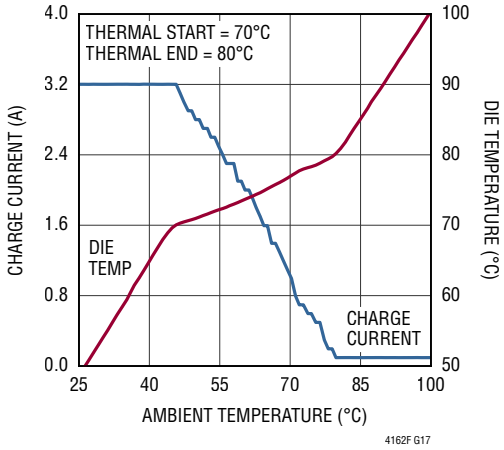


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

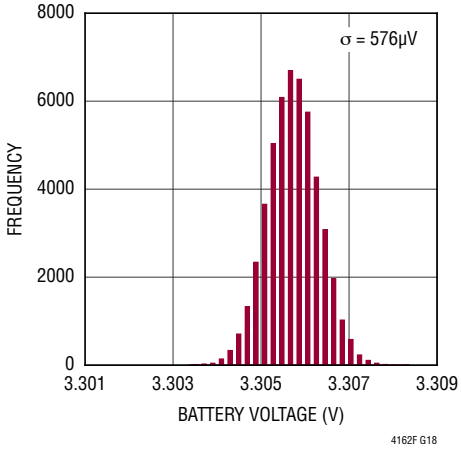
Multi-Peak Solar Panel Acquisition



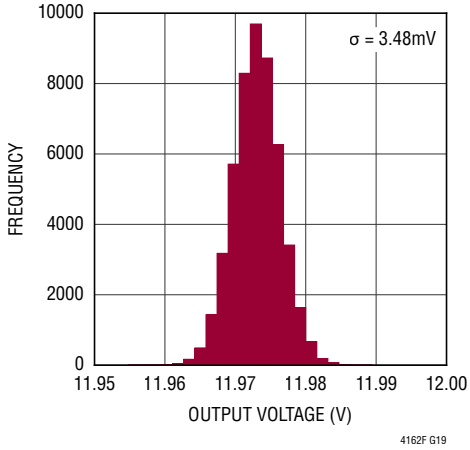
Charge Current and Die Temperature Using Thermal Regulation



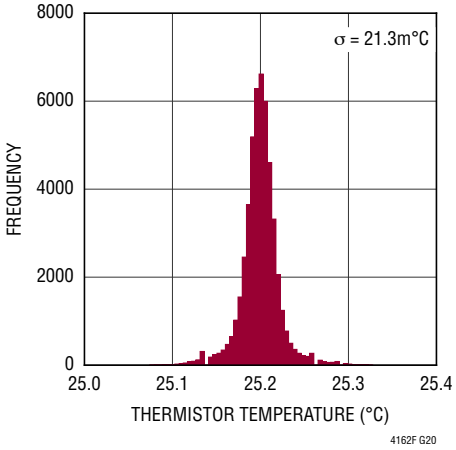
Histogram of vbat Readings



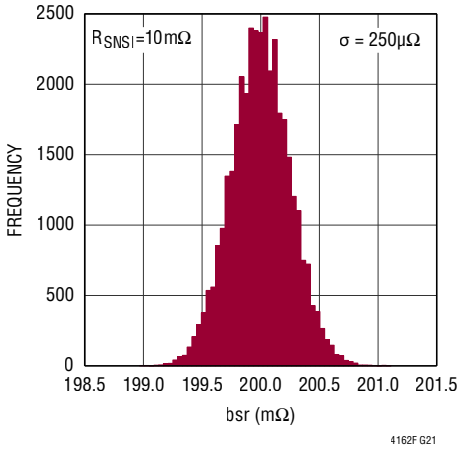
Histogram of vout Readings



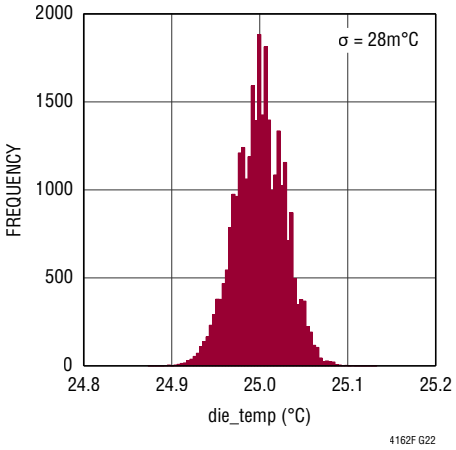
Histogram of thermistor_voltage Readings



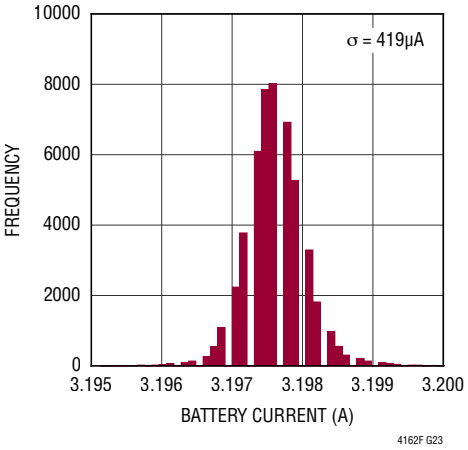
Histogram of bsr Readings



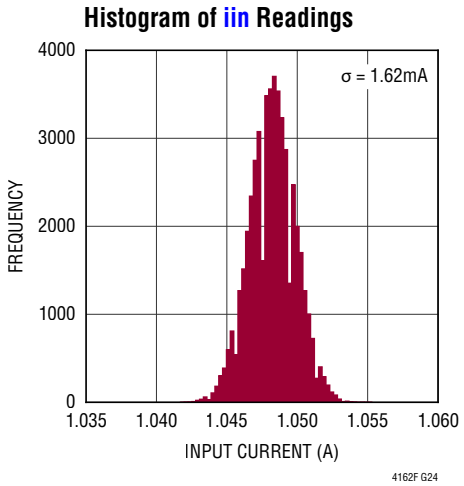
Histogram of die_temp Readings

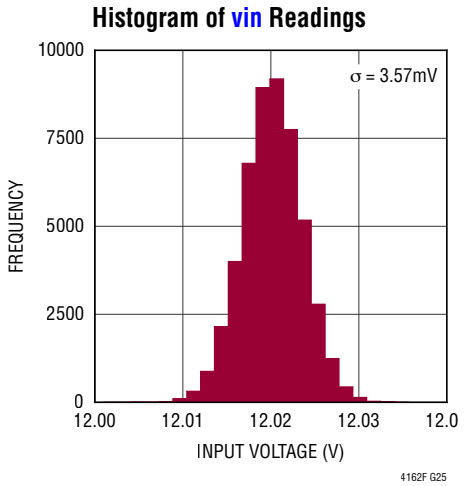


Histogram of ibat Readings



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.





PIN FUNCTIONS

BOOST (Pin 1): Gate-Drive bias for the high side switch in the switching regulator. This pin provides a pumped bias voltage relative to SW. The voltage on this pin is charged up through an internal diode from $INTV_{CC}$. A 22nF multilayer ceramic capacitor is required from SW to BOOST.

$INTV_{CC}$ (Pin 2): Bypass pin for the internal 5V regulator. This regulator provides power to the internal analog circuitry. A 4.7µF multilayer ceramic capacitor is required from $INTV_{CC}$ to GND.

V_{OUTA} (Pin 3): Analog system power pin. V_{OUTA} powers the majority of circuits on the LTC4162. A 0.1µF multilayer ceramic capacitor is required from V_{OUTA} to GND.

CLN (Pin 4): Connection point for the negative terminal of the sense resistor that measures and regulates input current by limiting charge current.

CLP (Pin 5): Connection point for the positive terminal of the sense resistor that measures and regulates input current by limiting charge current.

INFET (Pin 6): Gate control output pin for an input reverse blocking external N-channel MOSFET between V_{IN} and V_{OUT}.

V_{IN} (Pin 7): Supply voltage detection and INFET charge pump supply for the INFET/BATFET PowerPath. When voltage at V_{IN} is detected as being high enough to charge a battery, the INFET charge-pump is activated and the BATFET charge-pump is deactivated thereby powering V_{OUTA} from the input supply through an external NMOS transistor and also starting a charge cycle. A 0.1µF multilayer ceramic capacitor is required from V_{IN} to GND.

VCC2P5 (Pin 8): Bypass pin for the internal 2.5V regulator. This regulator provides power to the internal logic circuitry. A 1µF multilayer ceramic capacitor is required from VCC2P5 to GND.

NTCBIAS (Pin 9): NTC thermistor bias output. Connect a low temperature coefficient bias resistor between NTCBIAS and NTC, and a thermistor between NTC and GND. The bias resistor should be equal in value to the nominal value of the thermistor. The LTC4162 applies 1.2V to this pin during NTC measurement and expects a thermistor β value of 3490K. Higher β value thermistors can be used with simple circuit modifications.

PIN FUNCTIONS

NTC (Pin 10): Thermistor input. The NTC pin connects to a negative temperature coefficient thermistor to monitor the temperature of the battery. The voltage on this pin is digitized by the analog to digital converter to qualify battery charging and is available for readout via the I^2C port. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground.

R_T (Pin 11): Switching regulator frequency control pin. The R_T pin controls the switching regulator's internal oscillator frequency by placing a resistor from R_T to GND.

$\overline{\text{SMBALERT}}$ (Pin 12): Interrupt output. This open drain output pulls low when one or more of the programmable alerts is triggered.

SCL (Pin 13): Open drain clock input for the I^2C port. The I^2C port input levels are scaled with respect to DV_{CC} for I^2C compliance.

SDA (Pin 14): Open drain data input/output for the I^2C port. The I^2C port input levels are scaled with respect to DV_{CC} for I^2C compliance.

DV_{CC} (Pin 15): Logic supply for the I^2C port. DV_{CC} sets the reference level of the SDA and SCL pins for I^2C compliance. It should be connected to the same power supply as the SDA and SCL pull up resistors.

SYNC (Pin 16): Optional external clock input for the switching battery charger. The switching battery charger will lock to a square wave or pulse on this pin that is close to the frequency programmed by the R_T pin. Ground SYNC if this feature is not needed.

CELLS0 (Pin 17): Cell count selection pin. Used in combination with CELLS1, this pin sets the total number of series cells to be charged. The pin should be strapped to either $INTV_{CC}$, VCC2P5 or GND to represent one of three possible states. See Table 5.

CELLS1 (Pin 18): Cell count selection pin. Used in combination with CELLS0, this pin sets the total number of series cells to be charged. The pin should be strapped to either $INTV_{CC}$, VCC2P5 or GND to represent one of three possible states. See Table 5.

BATSENS+ (Pin 19): Positive terminal battery sense pin. BATSENS+ should Kelvin sense the positive terminal of the battery for optimized charging. A 10µF multilayer ceramic capacitor is required from BATSENS+ to ground.

CSN (Pin 20): Connection point for the negative terminal of the current sense resistor used to measure and limit charge current.

CSP (Pin 21): Connection point for the positive terminal of the current sense resistor used to measure and limit charge current.

BATFET (Pin 22): Gate control pin for a reverse blocking external N-channel MOSFET between the battery and V_{OUT}.

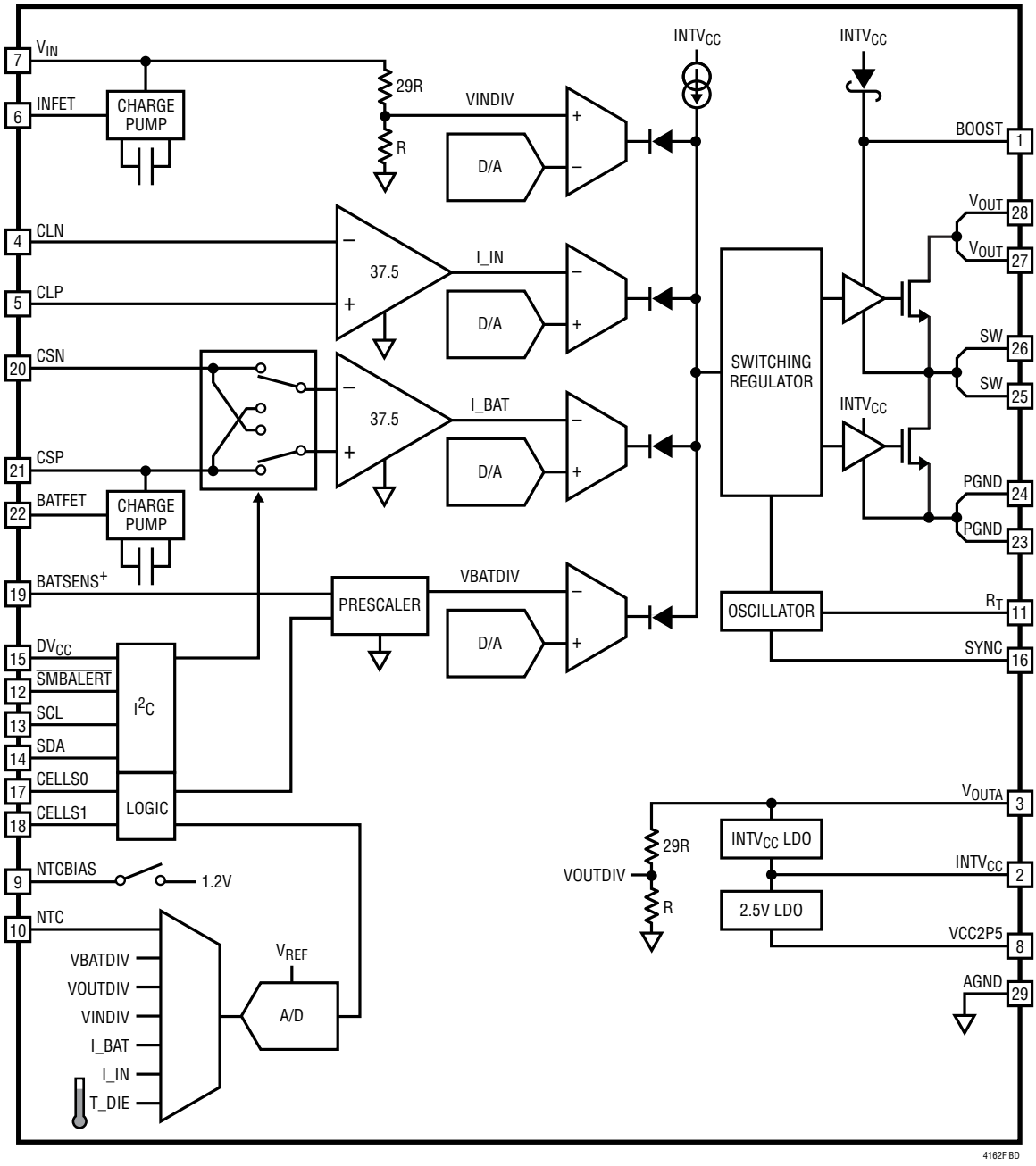
PGND (Pins 23,24): Power ground pins. These pins should be connected to a copper pour that forms the return for the V_{OUT} bypass capacitor on the top layer of the printed circuit board.

SW (Pin 25, 26): Switching regulator power transmission pins. The SW pins deliver power from the V_{OUT} pins to the battery via the step-down switching regulator. An inductor should be connected from SW to a sense resistor at CSP. See the Applications Information section for a discussion of inductor value and current rating.

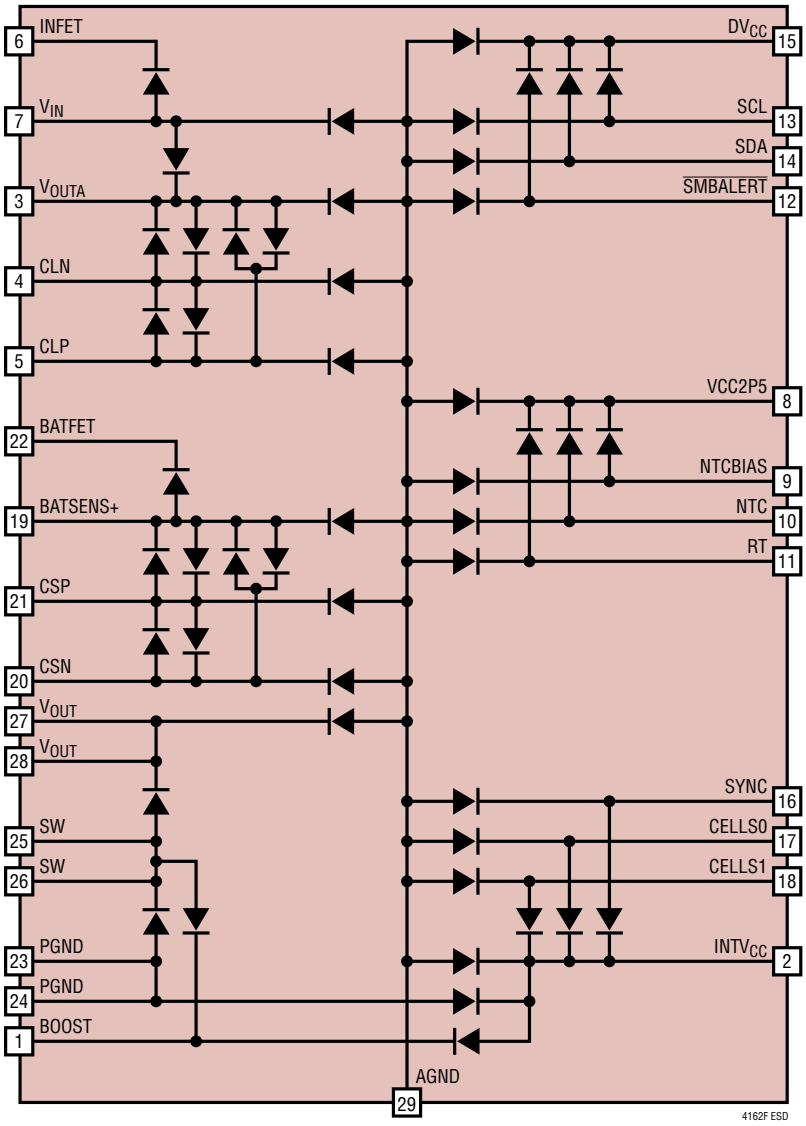
V_{OUT} (Pin 27, 28): Switching regulator input pins. The V_{OUT} pins deliver power to the switching charger. Having extremely high frequency current pulses, bypassing of the V_{OUT} pins should take precedence over all other PCB layout considerations. A bypass capacitor of 10µF is a good starting point.

AGND (Exposed PAD, Pin 29): Analog ground pin. This is the ground pin used to return all of the analog circuitry inside the LTC4162 and should be connected to an analog ground pour that is common with PGND (pins 23 and 24). It should also be connected to a ground plane on layer 2 of the PCB to which all of the analog components return such as the R_T resistor and the $INTV_{CC}$ and VCC2P5 bypass capacitors.

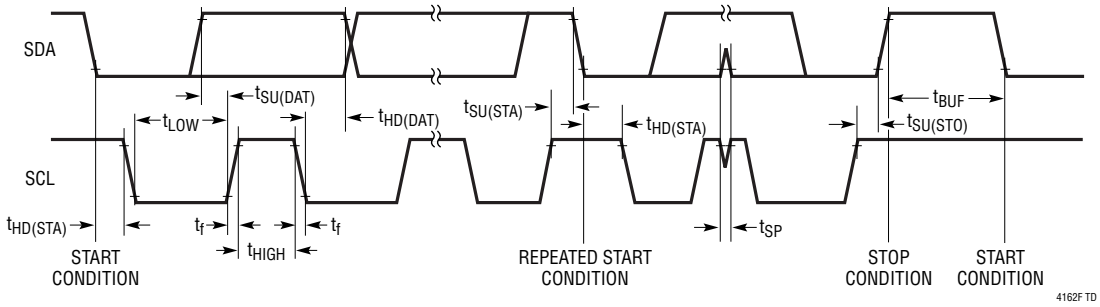
BLOCK DIAGRAM



ESD DIAGRAM


6 INFET
7 VIN
3 VOUTA
4 CLN
5 CLP
22 BATFET
19 BATSENS+
21 CSP
20 CSN
27 VOUT
28 VOUT
25 SW
26 SW
23 PGND
24 PGND
1 BOOST
29 AGND
15 DVCC
13 SCL
14 SDA
12 SMBALERT
8 VCC2P5
9 NTCBIAS
10 NTC
11 RT
16 SYNC
17 CELLS0
18 CELLS1
2 INTVCC
4162F ESD

TIMING DIAGRAM



I²C SMBus Legend

S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
A	ACKNOWLEDGE
N	NACK
P	STOP CONDITION
PEC*	PACKET ERROR CODE
	MASTER TO SLAVE
	SLAVE TO MASTER

SMBus WRITE WORD PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

SMBus WRITE WORD WITH PEC PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC*	A	P

SMBus READ WORD PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	N	P

SMBus READ WORD WITH PEC PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC*	N	P

SMBus ALERT RESPONSE ADDRESS PROTOCOL

S	ALERT RESPONSE ADDRESS	Rd	A	DEVICE ADDRESS	Rd	N	P

SMBus ALERT RESPONSE ADDRESS PROTOCOL WITH PEC

S	ALERT RESPONSE ADDRESS	Rd	A	DEVICE ADDRESS	Rd	A	PEC*	N	P

*USE OF PACKET ERROR CHECKING IS OPTIONAL

OPERATION

Introduction

The LTC4162 is an advanced power manager and switching battery charger utilizing a high efficiency synchronous step-down switching regulator.

Using multiple feedback control signals, power is delivered from the input to the battery by a 1.5MHz constant-frequency step-down switching regulator. The switching regulator reduces output power in response to one of its four regulation loops including battery voltage, battery charge current, input current and input voltage.

The switching regulator is designed to efficiently transfer power from a variety of possible sources, such as USB ports, wall adapters and solar panels, to a battery while minimizing power dissipation and easing thermal budgeting constraints. Since a switching regulator conserves power, the LTC4162 allows the charge current to exceed the source's output current, making maximum use of the allowable power for battery charging without exceeding the source's delivery specifications. By incorporating input voltage and system current measurement and control systems, the switching charger ports seamlessly to these sources without requiring application software to monitor and adjust system loads. By decoupling the system load from the battery and prioritizing power to the system, the instant-on PowerPath architecture ensures that the system is powered upon input power arrival, even with a completely dead battery.

Two low power charge pumps drive external MOSFETs to provide low loss power paths from the input supply and battery to the system load while preventing the system node from back-driving the input supply or overcharging the battery. The power path from the battery to the system load guarantees that power is available to the system even if there is insufficient or absent power from V_{IN}. A wide range of input current settings as well as battery charge current settings are available by software control and by choosing the values of input and charge current sense resistors R_{SNSI} and R_{SNSB}.

A measurement subsystem periodically monitors and reports on a large collection of system parameters via the I^2C port. An interrupt subsystem can be enabled to alert the host microprocessor of various status change events so that system parameters can be varied as needed. All of the status change events are maskable for maximum flexibility. For example, features such as battery presence detection and battery impedance measurement are easily enabled.

To eliminate battery drain between manufacture and sale, a ship-and-store feature reduces the already low battery drain current even further.

The input undervoltage control loop can be engaged to keep the input voltage from decreasing beyond a minimum level when a resistive cable or power limited supply such as a solar panel is providing input power. A maximum power point tracking algorithm using this control loop can be deployed to maximize power extraction from solar panels and other resistive sources.

Finally, the LTC4162 has a digital subsystem that provides substantial adjustability so that power levels and status information can be controlled and monitored via the conventional I^2C port.

LTC4162 Digital System Overview

The LTC4162 contains an advanced digital system which can be accessed using the I^2C port. Use of the I^2C port is optional, it can be used extensively in the application or not at all, as dictated by the application requirements. Cell count, charge current, input current regulation and switching charger frequency are all externally configurable without using the I^2C port. For applications requiring the LTC4162's advanced digital features, the I^2C port provides a means to use status and A/D telemetry data from the measurement system, monitor charger operation, configure charger settings (e.g. charge voltage, charge current, temperature response, termination algorithm, etc), enable, disable, read and clear alerts, activate the low power ship mode, and enable/disable the battery charger.

Power Path Controller

The LTC4162 features input and output N-channel MOSFET charge pump gate drivers. These drivers make up a dual unidirectional power path system that allows power to be delivered to the system load by either the input supply or the battery, whichever is greater. Only one of

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the external MOSFETs will be enabled at a time. If V_{IN} is more than 150mV above BATSENS+, the MOSFET from the input to the system load will be enabled and the one from the system load to BATSENS+ will block conduction preventing overcharging of the battery. If V_{IN} falls more than 20mV below BATSENS+ the MOSFET from the input supply to the system load will be disabled preventing reverse conduction and the MOSFET from BATSENS+ to the system load will be enabled powering downstream circuitry from the battery. It is important not to back drive V_{OUT} as one or the other of the power path MOSFETs will always be enabled.

Step Down Switching Battery Charger

The LTC4162's battery charger is based on a very efficient synchronous step down switching regulator. As with any modern battery charger, the LTC4162 incorporates both constant-current and constant-voltage feedback control loops to prevent overcharging. The switching charger can charge either a single cell or a battery of up to nine series lithium iron phosphate cells.

Normal charging begins with a constant current until the battery reaches its target voltage. The charge current is determined by the combination of the sense resistor, R_{SNSB}, placed in series with the inductor and the servo control voltage set by either icharge_jeita_2 through icharge_jeita_6 with en_jeita set or just charge_current_setting if en_jeita is cleared. An internal soft-start algorithm ramps up the charge current setting from zero to its present setting. Once the battery voltage reaches the programmed voltage limit the constant-current control loop hands off to the constant-voltage control loop. The final battery voltage is set with the combination of either vcharge_jeita_2 through vcharge_jeita_6 with en_jeita set or with just vcharge_setting if en_jeita is cleared. The cell_count, controlled by the CELLS0 and CELLS1 pins, is a charge voltage multiplier so that multiple series cells can be charged.

If en_jeita is set, the charge current is given by the expression:

$$I_{CHARGE} = (icharge\_jeita\_x + 1)\frac{1mV}{R_{SNSB}}$$

where icharge_jeita_2 through icharge_jeita_6 each range from 0 to 31.

If en_jeita is not set:

$$I_{CHARGE} = (charge\_current\_setting + 1)\frac{1mV}{R_{SNSB}}$$

where charge_current_setting ranges from 0 to 31.

If en_jeita is set, the charge voltage is given by the expression:

V_{CHARGE} = (3.4125V + 12.5mV • vcharge_jeita_x) • cell_count

where vcharge_jeita_2 through vcharge_jeita_6 each range from 0 to 31.

If en_jeita is not set:

V_{CHARGE} = (3.4125V + 12.5mV • vcharge_setting) • cell_count

where vcharge_setting ranges from 0 to 31.

Beyond the conventional constant-current and constant-voltage control loops, the LTC4162 also has the ability to monitor and control both input current and input voltage, regulating battery charge power based on any one of these four control loops. Power limit is prioritized based on the lowest set-point of the group. For example, if the combined system load plus battery charge current is large enough to cause the switching charger to reach the programmed input current limit, the input current limit will reduce charge current to limit the voltage across the input sense resistor, R_{SNSI}, to the iin_limit_target. Even if the charge current is programmed to exceed the allowable input current, the input current due to charge current will not be violated; the charger will reduce its current as needed. Similarly, the input voltage limit loop, controlled by input_undervoltage_setting, can be used to prevent resistive power sources such as a solar panel from dragging the input voltage down below its under-voltage lockout level.

Only target values can be programmed with the I^2C port. The LTC4162 uses the target values as a starting point from which the charging algorithms calculate the actual values to be applied to the DACs to support functions such as

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temperature compensated charge voltages and currents, maximum power point tracking, charger soft starting, etc. The target value registers are read/write whereas the actual DAC value registers, icharge_dac, vcharge_dac, iin_limit_dac and input_undervoltage_dac are read only.

Due to its all NMOS switch design, a small charge pump capacitor is required from SW to BOOST to provide high side boosted drive for the top switch.

Input Current Regulation

Input current control limits loading on the input source during periods of high system demand by sacrificing charge current. Note that the LTC4162 only has the authority to reduce charge current to zero and cannot further reduce input current below the system load current. The input current limit is controlled by a combination of the sense resistor, R_{SNSI}, from CLP to CLN and either the default 32mV servo voltage or a lower value set by iin_limit_target. The servo voltage across the sense resistor divided by the resistor's value determines the input current regulation set point. A 10mΩ resistor, for example, would have an upper input current limit of 3.2A using the default 32mV servo voltage. iin_limit_target has 6 bit resolution giving adjustable values from 500µV to 32mV in 500µV steps and can be calculated in Amperes, by the following expression:

$$I_{INLIM} = (iin\_limit\_target + 1)\frac{500\mu V}{R_{SNSI}}$$

where iin_limit_target ranges from integer values of 0 to 63.

Input Undervoltage Regulation and Solar Panel Maximum Power Point Tracking (MPPT)

The LTC4162 also contains an undervoltage control loop that allows it to tolerate a resistive connection to the input power source by automatically reducing charge current as the V_{IN} pin drops to input_undervoltage_setting. This circuit helps prevent UVLO oscillations by linearly regulating the input voltage above the LTC4162's undervoltage lockout level.

Optionally, the LTC4162 includes a maximum power point tracking (MPPT) algorithm to find and track the input_undervoltage_dac value that delivers the maximum charge current to the battery. If mppt_en is set, the MPPT algorithm performs a global sweep of input_undervoltage_dac values, measuring battery charge current at each setting. Once the sweep is complete, the LTC4162 applies the input_undervoltage_dac value corresponding to the maximum battery charge current ibat (i.e. the maximum power point). The LTC4162 then tracks small changes in the maximum power point by slowly dithering the input_undervoltage_dac. The LTC4162 performs a new global sweep of input_undervoltage_dac values every 15 minutes, applies the new maximum power point, and resumes dithering at that point. Alternatively, the global sweep will run immediately, bypassing the 15 minute wait, if ibat changes by more that 25%. With mppt_en, a solar panel can be used as a suitable power source for charging a battery and powering a load. The MPPT algorithm may not work for all solar panel applications and does not have to be used. Alternatively a solar panel can be used without the MPPT algorithm by setting the input_undervoltage_setting value to match the optimum loaded solar panel voltage, but significant shadows or drops in light will likely result in suboptimum power delivery.

Note that, due to the Power Path topology, current can flow from the input to the system load without being controlled by the LTC4162's switching charger. Therefore, the MPPT algorithm does not have full authority to track and find the maximum power point under all conditions. To obtain complete Maximum Power Point operation, it may be necessary to forgo the Power Path feature of the LTC4162 and connect the system load directly to the battery pack. In this configuration, the LTC4162 has full authority to track the maximum power point of the solar panel.

The input under voltage value, in Volts, will be given by the following expression:

$$V_{INLIM} = (input\_undervoltage\_setting + 1) \bullet 140.625mV$$

where input_undervoltage_setting ranges from integer values of 0 to 255.

OPERATION

System Controls

The switching battery charger can be disabled by setting suspend_charger. This might be necessary, for instance, to pass USB Suspend compliance testing. suspend_charger should be used with caution as a low battery situation could prevent the system processor from being able to clear it and may require a factory service call to remove and replace the battery.

Input Overvoltage Protection

The LTC4162 has over-voltage detection on its input. If V_{IN} exceeds approximately 38.6V as indicated by vin_ovlo, the switching charger will stop delivering power. The charger will resume switching if V_{IN} falls below roughly 37.2V. The overvoltage detection cutoff circuit provides only modest over voltage protection and is not intended to prevent damage in all circumstances.

Measurement Subsystem

The LTC4162 includes a 16-bit ΔΣ A/D converter and signal multiplexer to monitor numerous analog parameters. It can measure the voltages at vin, vbat and vout, the input current (voltage between CLP and CLN), iin, the battery charge current (voltage between CSP and CSN), ibat, the battery pack thermistor_voltage, its own internal die_temp and, once a charge cycle begins, the series resistance of the battery, bsr. To save battery current, the measurement system is disabled if the battery is the only source of power (vin_gt_vbat = 0). This can be overridden with force_telemetry_on. The A/D converter is automatically multiplexed between all of the measured channels and its 16-bit signed two's complement results are stored in registers accessible via the I^2C port. The seven channels measured by the ADC each take approximately 1.6ms to convert. The maximum range of the 16 bit ΔΣ A/D converter is ±1.8V and it has an internal span term of 18191 counts per Volt. It measures each of the above parameters through different paths giving different sensitivity terms for each measurement as summarized in Table 1.

Battery Voltage Measurement

Battery voltage is measured through a resistive voltage divider whose attenuation ratio is based on the cell_count. The result is reported in vbat. The divider ratio is BATSENS+/(3.5 • cell_count) making the A/D span term 3.5 • cell_count/18191 or 192.4µV • cell_count per LSB where cell_count varies from 1 to 9. An alert may be set on battery voltage by setting the vbat based value vbat_lo_alert_limit or vbat_hi_alert_limit and setting en_vbat_lo_alert or en_vbat_hi_alert. These alerts are indicated by vbat_lo_alert or vbat_hi_alert and are cleared by writing them to 0.

Input Voltage Measurement

Input voltage is measured through a 30:1 resistive voltage divider making the A/D span term for input voltage measurements 30/18191 or 1.649mV/LSB and is digitized to vin. An alert may be set on input voltage by setting the value vin_lo_alert_limit or vin_hi_alert_limit and setting en_vin_lo_alert or en_vin_hi_alert. These alerts are indicated by vin_lo_alert and vin_hi_alert and are cleared by writing them to 0.

Table 1. Measurement Subsystem LSB Sizes

MEASUREMENT	UNITS	REGISTER SYMBOL	LSB SIZE	OFFSET
BATTERY VOLTAGE	V	vbat	192.4µV • cell_count	
INPUT VOLTAGE	V	vin	1.649mV	
OUTPUT VOLTAGE	V	vout	1.653mV	
INPUT CURRENT	A	iin	1.466µV/RSNSI	
BATTERY CURRENT	A	ibat	1.466µV/RSNSB	
DIE TEMPERATURE	°C	die_temp	0.0215°C	264.4°C
BATTERY IMPEDANCE	Ω	bsr	RSNSB • cell_count/500	
THERMISTOR VOLTAGE	V	thermistor_voltage	45.833µV/V	

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V_{OUT} Voltage Measurement

Output voltage is measured through a 30.07:1 resistive voltage divider making the A/D span term for system voltage measurements 30.07/18191 or 1.653mV/LSB and is digitized to vout. An alert may be set on output voltage by setting the value vout_lo_alert_limit or vout_hi_alert_limit and setting en_vout_lo_alert or en_vout_hi_alert. These alerts are indicated by vout_lo_alert and vout_hi_alert and are cleared by writing them to 0.

Battery Current Measurement

Battery current is measured with a current sense resistor between the CSP and CSN pins. An amplifier with a gain of 37.5 amplifies this signal and refers it to ground internally so that the A/D converter can measure it. The sensed battery current is therefore given by $I_{BAT} \bullet R_{SNSB} \bullet 37.5$. For a 10mΩ R_{SNSB} current sense resistor, the A/D sensitivity is 1/(18191 • 10mΩ • 37.5) or 146.6µA/LSB. The battery current measurement system has a built in commutator. While charging a battery, two's complement number ibat will be positive representing current into the battery. When the battery charger is disabled or terminated, as detected by charger_suspended, the commutator is activated and ibat will be negative, representing current out of the battery. An alert may be set on the ibat measurement by setting the desired value in ibat_lo_alert_limit and setting en_ibat_lo_alert. While charging, ibat_lo_alert_limit can be used to detect when the charge current has dropped below a given threshold. When charger_suspended, if set to a negative number, ibat_lo_alert_limit can be used to detect if the battery load has exceeded a given threshold. This alert is indicated by ibat_lo_alert and is cleared by writing it to 0.

Input Current Measurement

Input current is measured with a current sense resistor between the CLP and CLN pins. An amplifier with a gain of 37.5 amplifies this signal and refers it to ground internally so that the A/D converter can measure it. The sensed input current is therefore given by $I_{IN} \bullet R_{SNSI} \bullet 37.5$. For a 10mΩ R_{SNSI} current sense resistor, the A/D sensitivity is 1/(18191 • 10mΩ • 37.5) or 146.6µA/LSB. The input current is digitized to iin. An upper limit alert may be set on input current by setting the value iin_hi_alert_limit and setting the en_iin_hi_alert. This alert is indicated by iin_hi_alert and is cleared by writing it to 0.

Battery Series Resistance (BSR) Measurement

The LTC4162 can optionally measure the series resistance of the battery stack or cell. If run_bsr is set, the LTC4162 momentarily suspends the battery charger and calculates the battery series resistance by dividing the voltage change (charging vs not charging) by the measured charge current (bsr_charge_current).

The per-cell resistance value is reported in bsr and the charge current observed during the measurement is reported in bsr_charge_current. The LTC4162 automatically resets run_bsr after the bsr measurement is complete. The total battery series resistance value is proportional to the charge current sense resistor, R_{SNSB}, as well as the cell_count, and can be computed in Ω from the expression:

$$R_{BAT}(\Omega) = \frac{bsr \bullet cell\_count \bullet R_{SNSB}}{500}$$

Higher bsr_charge_current during a bsr measurement results in a more accurate bsr measurement. Very low values of bsr_charge_current may adversely impact the accuracy of the bsr measurement. If charge current is less than C/10 (bsr_charge_current < icharge_over_10), bsr_questionable will be set indicating that bsr_charge_current during the bsr test was less than optimum for an accurate reading. Recall that full charge current typically flows at the beginning of a charge cycle (presuming the battery is more deeply depleted) and will diminish when the charger enters the constant voltage phase of charging.

If run_bsr is set to 1 and the battery charger is not currently running, then the LTC4162 will be queued to perform the bsr measurement only after the start of the next charge cycle. An alert can be set with en_bsr_done_alert to generate a bsr_done_alert interrupt indicating that a bsr measurement is complete and that the result is available. A bsr_hi_alert may also be set on battery series impedance by writing a bsr_hi_alert_limit and setting en_bsr_hi_alert. Again, the bsr reading is the per-cell battery resistance and should be scaled by cell_count or, consequently, the

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target total resistance threshold for bsr_hi_alert_limit should be divided by cell_count before being written to bsr_hi_alert_limit.

bsr_done_alert and bsr_hi_alert are cleared by writing them to 0.

Die Temperature Measurement

The LTC4162 has an integrated die temperature sensor that is monitored by the A/D converter and is digitized to die_temp. The die temperature is derived from an internal circuit and follows the equation:

$$T_{DIE}(°C) = die\_temp \bullet 0.0215°C/LSB - 264.4°C$$

An alert may be set on die temperature by setting the value die_temp_hi_alert_limit and setting en_die_temp_hi_alert. This alert is indicated by die_temp_hi_alert and is cleared by writing it to 0.

To set the die_temp_hi_alert_limit, compute the threshold value from:

$$die\_temp\_hi\_alert\_limit = \frac{T_{DIE}(°C) + 264.4°C}{0.0215°C/LSB}$$

Battery Temperature (NTC Thermistor) Measurement

To measure the battery temperature using a thermistor, connect the thermistor, R_{NTC}, normally being located in the battery pack, between the NTC pin and ground, and a low drift bias resistor, $R_{NTCBIAS}$, between NTCBIAS and NTC. $R_{NTCBIAS}$ should be a 1% or better resistor with a value equal to the value of the chosen thermistor at 25°C (R25). The LTC4162 applies an excitation voltage of 1.2V to $R_{NTCBIAS}$ to measure the thermistor value. The thermistor measurement result is available at thermistor_voltage. To minimize battery stress due to charging at temperature extremes, the LTC4162 has both a simple and a more advanced JEITA (Japan Electronics and Information Technology Industries Association) temperature qualified charging algorithm. If the application does not require temperature controlled charging, then the thermistor should be replaced with a resistor of equal value to the bias resistor $R_{NTCBIAS}$ to continuously simulate 25°C. If the thermistor is found to be open (thermistor_voltage > open_thermistor) either during the battery detection test or during charging, charger_state will switch to bat_missing_fault and charging will halt. Either a thermistor_voltage_lo_alert or thermistor_voltage_hi_alert may be set with en_thermistor_voltage_lo_alert or en_thermistor_voltage_hi_alert, both of which are cleared by writing them to 0.

The temperature vs resistance curve of a thermistor can be obtained from thermistor manufacturers in either table form or estimated by applying the modified Steinhart-Hart equation:

$$R_{NTC} = R_{25} \bullet e^{\left(A + \frac{B}{T_C + 273.15} + \frac{C}{(T_C + 273.15)^2} + \frac{D}{(T_C + 273.15)^3}\right)}$$

Where R_{25} is the thermistor's resistance at 25°C and A, B, C and D are provided by the thermistor manufacturer and T_C is the temperature in °C.

The temperature of the thermistor is computed from its resistance value by the complementary Steinhart-Hart expression where A1, B1, C1 and D1 are also provided by the thermistor manufacturer.

$$T_C = \frac{1}{A_1 + B_1 \ln\left(\frac{R_{NTC}}{R_{25}}\right) + C_1 \ln^2\left(\frac{R_{NTC}}{R_{25}}\right) + D_1 \ln^3\left(\frac{R_{NTC}}{R_{25}}\right)} - 273.15^oC \quad (1)$$

Alternatively, the more common but less accurate condensed version of Steinhart-Hart using the ubiquitous β parameter may be employed:

$$R_{NTC} = R_{25} \bullet e^{-\beta_{25/85}\left(\frac{1}{298.15^oC} - \frac{1}{T_C + 273.15^oC}\right)}$$

Where again, R_{25} is the thermistor's resistance at 25°C and several β values are provided by the thermistor manufacturer, one for each of a number of temperature ranges.

The inverse β form is:

$$T_C = \frac{\beta_{25/85}}{\ln\left(\frac{R_{NTC}}{R_{25}}\right) + \frac{\beta_{25/85}}{298.15^oC}} - 273.15^oC \quad (2)$$

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The LTC4162 thermistor measurement system is designed specifically for a thermistor with a $\beta_{25/85}$ value of 3490K and returns thermistor_voltage where:

$$thermistor\_voltage = 18191 \bullet 1.2 \bullet \frac{R_{NTC}}{R_{NTC}+R_{NTCBIAS}}$$

where typically $R_{NTCBIAS}$ is set equal to R_{25}, the 25°C value of the thermistor. To arrive at the thermistor's temperature in °C from thermistor_voltage substitute R_{NTC} from:

$$R_{NTC} = R_{NTCBIAS} \bullet \frac{thermistor\_voltage}{18191 \bullet 1.2 - thermistor\_voltage}$$

into Equation 1 or Equation 2.

For thermistors with a $\beta_{25/85}$ value higher than 3490K see Alternate Thermistors and Biasing in the Applications section.

Output Current Measurement

There is no sense resistor dedicated to measuring output current but its value can be obtained nonetheless. Output current is delivered from the input supply if vin_gt_vbat is true and from the battery if it is false.

If vin_gt_vbat is true and the battery charger is enabled (en_chg is true) then the input current measurement will be the sum of current to the switching charger and the output load. In this instance the switching charger will need to be disabled with suspend_charger to obtain an output current reading. It's also possible that the charger may already be terminated. If en_chg is false then set telemetry_speed to tel_high_speed, wait 20ms or more, and record iin as output current. If en_chg is true then set both suspend_charger and force_telemetry_on to 1 and telemetry_speed to tel_high_speed, wait 20ms or more for at least one telemetry cycle, and again record iin as output current. suspend_charger should then be cleared. Note that suspending the charger resets the tchargetimer and tcvtimer termination timers to 0.

On the other hand if vin_gt_vbat is false then the output current will be delivered from the battery and its value can be obtained from –ibat. Since vin_gt_vbat is low, the telemetry system will be disabled and the ibat reading will be stale.

To enable the telemetry system, set force_telemetry_on to 1 and telemetry_speed to tel_high_speed. telemetry_valid indicates when fresh telemetry readings are available. To avoid polling for telemetry_valid a telemetry_valid_alert can be set with en_telemetry_valid_alert. Once the reading is obtained, force_telemetry_on can be cleared or telemetry_speed set to tel_low_speed for power savings.

Low Power Telemetry

If input power is available (vin_gt_vbat = 1), and the battery is being charged, the telemetry system will be in its high speed mode returning results at a rate of roughly once per 11ms. If, on the other hand, charging has terminated normally or paused due to battery temperature out of range, the telemetry system will drop back to a rate of about once every 5 seconds to save power. When input power is not available (vin_gt_vbat = 0) it is still possible to collect telemetry data by setting force_telemetry_on. To save power in this mode the telemetry system will default to the lower speed 5 second mode. To force the higher telemetry rate, and suffer the higher quiescent current of roughly 2.5mA, the telemetry_speed can be set to the higher ~11ms rate by setting it to tel_high_speed.

Configurable Limit Alert Subsystem

The I^2C port also supports the SMBus $\overline{SMBALERT}$ protocol, including the Alert Response Address. An alert can optionally be generated if a monitored parameter exceeds a programmed limit or if a selected battery charger_state or any of a wide number of other charge_status change or fault events occur. This off-loads much of the continuous monitoring from the system's microcontroller and onto the LTC4162; reducing bus traffic and microprocessor load.

The $\overline{SMBALERT}$ pin is asserted (pulled low) whenever an enabled alert occurs. After asserting an interrupt, the LTC4162 responds to the host's Alert Response Address (ARA = 0b0001100[1]) with its own read address. If another part with a pending alert and a lower address also responds, that part wins the arbitration and the LTC4162 will stop responding to this ARA, keeping its $\overline{SMBALERT}$ pin asserted. Only a response of the LTC4162's complete read address will clear the LTC4162's $\overline{SMBALERT}$ signal.

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Table 2. Summary of Limit Alerts Registers

ALERT VALUE SETTING (0x01 – 0x0C)	EN_LIMIT_ALERTS_REG	LIMIT_ALERTS_REG
vin_hi_alert_limit	en_vin_hi_alert	vin_hi_alert
vin_lo_alert_limit	en_vin_lo_alert	vin_lo_alert
thermistor_voltage_hi_alert_limit	en_thermistor_voltage_hi_alert	thermistor_voltage_hi_alert
thermistor_voltage_lo_alert_limit	en_thermistor_voltage_lo_alert	thermistor_voltage_lo_alert
bsr_hi_alert_limit	en_bsr_hi_alert	bsr_hi_alert
die_temp_hi_alert_limit	en_die_temp_hi_alert	die_temp_hi_alert
ibat_lo_alert_limit	en_ibat_lo_alert	ibat_lo_alert
iin_hi_alert_limit	en_iin_hi_alert	iin_hi_alert
vout_hi_alert_limit	en_vout_hi_alert	vout_hi_alert
vout_lo_alert_limit	en_vout_lo_alert	vout_lo_alert
vbat_hi_alert_limit	en_vbat_hi_alert	vbat_hi_alert
vbat_lo_alert_limit	en_vbat_lo_alert	vbat_lo_alert
NA	en_bsr_done_alert	bsr_done_alert
NA	en_telemetry_valid_alert	telemetry_valid_alert

Table 3. Summary of Charger State Alerts

CHARGER_STATE_REG	EN_CHARGER_STATE_ALERTS_REG	CHARGER_STATE_ALERTS_REG
bat_detect_failed_fault	en_bat_detect_failed_fault_alert	bat_detect_failed_fault_alert
battery_detection	en_battery_detection_alert	battery_detection_alert
charger_suspended	en_charger_suspended_alert	charger_suspended_alert
cc_cv_charge	en_cc_cv_charge_alert	cc_cv_charge_alert
ntc_pause	en_ntc_pause_alert	ntc_pause_alert
timer_term	en_timer_term_alert	timer_term_alert
c_over_x_term	en_c_over_x_term_alert	c_over_x_term_alert
max_charge_time_fault	en_max_charge_time_alert	max_charge_time_fault_alert
bat_missing_fault	en_bat_missing_fault_alert	bat_missing_fault_alert
bat_short_fault	en_bat_short_fault_alert	bat_short_fault_alert

Table 4. Summary of Charger Status Alerts

CHARGE_STATUS_REG	EN_CHARGE_STATUS_ALERTS_REG	CHARGE_STATUS_ALERTS_REG
constant_voltage	en_constant_voltage_alert	constant_voltage_alert
constant_current	en_constant_current_alert	constant_current_alert
iin_limit_active	en_iin_limit_active_alert	iin_limit_active_alert
vin_uvcl_active	en_vin_uvcl_active_alert	vin_uvcl_active_alert
thermal_reg_active	en_thermal_reg_active_alert	thermal_reg_active_alert
ilim_reg_active	en_ilim_reg_active_alert	ilim_reg_active_alert

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This allows the system to have many parts share a common interrupt line. If multiple parts are asserting the $\overline{\text{SMBALERT}}$ signal then multiple reads from the ARA are needed. For more information refer to the SMBus specification.

After the ARA process is complete, alert bits can be cleared by individually writing them to 0 and writing the remaining bits in the register to 1. This preserves any other pending alert bits as writing 1s to the alert registers are ignored.

Series Cell Count Selection

Cell count selection of up to eight series cells is made via the CELLS1 and CELLS0 pins. CELLS1 and CELLS0 should be pin strapped to either GND, VCC2P5, or $INTV_{CC}$ to make the cell_count selection (see Table 5). For added safety, cell_count can be read back from the I^2C port. The GND/GND combination will result in a cell_count_err and will inhibit charging. Note that the number of cells multiplied by their expected maximum cell voltage during charging cannot exceed $V_{IN} – V_{IN\_DUVLO}$.

Table 5. CELLS0 and CELLS1 Pin Mapping to Series Cell Count

CELLS1	CELLS0	cell_count
$INTV_{CC}$	$INTV_{CC}$	1
$INTV_{CC}$	VCC2P5	2
$INTV_{CC}$	GND	3
VCC2P5	$INTV_{CC}$	4
VCC2P5	VCC2P5	5
VCC2P5	GND	6
GND	$INTV_{CC}$	7
GND	VCC2P5	8
GND	GND	9

When charging stacks of two or more cells in series it is important to consult with the battery manufacturer to ascertain requirements pertaining to cell balancing. Repeatedly charging series stacks of cells without balancing is usually degenerative and typically leads to increased mismatch accompanied with shorter battery life. For high reliability applications an auxiliary battery balancer is recommended.

Battery Detection

The LTC4162 begins a charging cycle by performing a 2-4 second battery detection test, during which a 1mA load is drawn from the battery followed by a small charge current being sent to the battery. If the battery voltage remains stable during the battery detection test, the LTC4162 proceeds with battery charger soft-start. If the battery voltage does not remain stable, the LTC4162 proceeds with a battery open/short test. The battery is charged at minimum charge current for one to two seconds. Abnormal results from the battery detection test result in charger_state becoming bat_missing_fault, bat_short_fault or bat_detect_failed_fault and will prevent further charging. A charger_state of bat_missing_fault will also occur if the thermistor is open or has a very high value (thermistor_voltage > open_thermistor). Programmable interrupts en_bat_short_fault_alert, en_bat_missing_fault_alert and en_bat_detect_failed_fault_alert can be set to generate an $\overline{\text{SMBALERT}}$ if one of these cases occurs. In the event of a battery detection fault, the battery detection test will retry every 30 seconds.

Battery Charger Soft-Start

The LTC4162 soft starts charge current by ramping icharge_dac from 0 to its target charge current setting at a nominal rate of 400µS per icharge_dac LSB. This results in a maximum charge current soft start time of 31 • 400µs or 12.4ms. Any time the battery charger needs to change its charge current setting up or down, the ramp routine is invoked. The charge current target is derived from either charge_current_setting or the JEITA temperature qualified charging system, icharge_jeita_2 through icharge_jeita_6 (See Advanced JEITA Temperature Controlled Charging).

Low Battery

If the BATSENS+ pin voltage is lower than about 2.5V, the battery charger delivers roughly 10mA directly from $INTV_{CC}$. This operating mode is mainly used to pull a pack protected battery out of protection mode. When the BATSENS+ pin voltage reaches 2.5V, charging hands over to the switching battery charger and proceeds to the full constant-current/constant-voltage charging phase reporting cc_cv_charge.

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Constant-Current Charging

The charger will attempt to deliver either (icharge_jeita_x + 1) • 1mV/R_{SNSB} with en_jeita or (charge_current_setting + 1) • 1mV/R_{SNSB} without en_jeita in constant-current mode where icharge_jeita_x or charge_current_setting ranges from 0 to 31. For example, A 10mΩ resistor between CPS and CSN would give an upper limit charge current of 3.2A. Depending on available input power and external load conditions, the battery charger may not be able to charge at the full programmed rate. An alternate control loop such as the input current limit loop or input voltage limit loop may be in force and only partial power will be available to charge the battery. If input current limit is reached, for instance, the system load will be prioritized over the battery charge current. When system loads are light, battery charge current will be maximized and could be as high as the value programmed by icharge_jeita_x or charge_current_setting.

The charge current programming resistor, R_{SNSB}, should always be set to match the capacity of the battery without regard to source or load limitations from any other control loop. The multiple control-loop architecture of the LTC4162 will correct for any discrepancies, always optimizing transfer of power to the battery and the load.

Thermal Regulation

When the switching battery charger is enabled at an elevated ambient temperature, LTC4162 self heating may push its junction temperature to an unacceptable level. To prevent overheating the LTC4162 monitors its own die_temp and automatically reduces the icharge_dac to limit power dissipation. The differential servo voltage at CSP to CSN can drop to as low as 1mV giving about 3% (1/32) of the maximum charge current. The thermal regulation algorithm achieves this by enforcing a maximum icharge_dac setting which drops linearly from 31 to 0 as die_temp increases from thermal_reg_start_temp (default 120°C) to thermal_reg_end_temp (default 125°C). When the thermal regulation algorithm is active, charge_status becomes thermal_reg_active. A thermal_reg_active_alert can be set with en_thermal_reg_active_alert and cleared by writing either back to 0. Thermal regulation can be programmed to any temperature within the LTC4162's operating range.

Constant-Voltage Charging

Once the BATSENS+ voltage reaches the programmed charging voltage the switching regulator will reduce its output power and hold the battery voltage steady at either (3.4125V + 12.5mV • vcharge_jeita_x) • cell_count with en_jeita or (3.4125V + 12.5mV • vcharge_setting) • cell_count without en_jeita where vcharge_jeita_x and vcharge_setting each range from 0 to 31. In constant voltage mode the charge current will decrease naturally toward zero providing inherently safe operation by preventing the battery from being over charged. Multiple charge voltage settings are available for final top-off voltage selection via vcharge_jeita_x with en_jeita or vcharge_setting without en_jeita. While charge voltage trade-offs can be made to preserve battery life or maximize capacity, it is not possible for the LTC4162 to be set to a charge voltage that is dangerously high or inconsistent with a Lithium-Ion/Polymer Battery.

Note that charge_current_setting and vcharge_setting do not directly control the icharge_dac and vcharge_dac. They are only target values. For example, if the JEITA Temperature Controlled Charging system is enabled (en_jeita = 1), the DACs will be controlled by this user programmable system (i.e. icharge_jeita_2 through icharge_jeita_6, vcharge_jeita_2 through vcharge_jeita_6).

Basic Temperature Controlled Charging

The LTC4162 provides temperature controlled charging if a grounded thermistor and a bias resistor are connected to the NTCBIAS and NTC pins and en_jeita is set to 0. Charging is paused if thermistor_voltage rises above jeita_t1 (0°C) or falls below jeita_t6 (60°C). Recall that thermistors have a negative temperature coefficient so higher temperatures will read lower thermistor_voltage and vice versa. If charging is not suspended, the charging voltage and current will follow vcharge_setting and charge_current_setting respectively.

The default upper and lower limits are based on a thermistor with a $\beta_{25/85}$ value of 3490K, such as provided by a Vishay NTCS0402E3103FLT. This thermistor was chosen specifically because of its weak temperature characteristic relative to other thermistors. Stronger thermistors can

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be diluted to match it by placing a low drift resistor in series with the thermistor and increasing the bias resistor accordingly. (see Alternate Thermistors and Biasing in Applications Information for details). If the application does not require temperature controlled charging then the thermistor should be replaced with a resistor of equal value to bias resistor $R_{NTCBIAS}$, for example, 100kΩ.

Advanced JEITA Temperature Controlled Charging

A control system is included to provide compliance with the Japan Electronics and Information Technology Industries Association guidelines on battery charging by leaving en_jeita set to its default value of 1. Specifically, a very flexible multi-point temperature-voltage-current profile can be programmed into the LTC4162 to ensure that charging parameters as a function of temperature are used. Figure 1 and Table 6 illustrate default values of the JEITA system available in the LTC4162. There are seven distinct temperature regions programmed by the six thermistor_voltage based temperature set points jeita_t1 through jeita_t6. For each of the temperature regions, the charge current and charge voltage can be programmed within the limits set by $(V_{CSP} – V_{CSN})/R_{SNSB}$ (charge_current_setting) and battery charge voltage (vcharge_setting). When en_jeita is true, The JEITA system writes its registers, icharge_jeita_2 through icharge_jeita_6 and vcharge_jeita_2 through vcharge_jeita_6 to charge_current_setting and vcharge_setting which are then passed on to the icharge_dac and vcharge_dac.

Writing values to charge_current_setting and vcharge_setting with en_jeita set is futile as the JEITA system will overwrite these values every 11ms.

The values for the JEITA registers are shown below. The bold values in the tables are programmable. The jeita_t1 through jeita_t6 registers determine the thermistor_voltage values for the breakpoints between regions. Table 6 lists the default values of the JEITA charging parameters along with example values of a 10kΩ thermistor with a β value of 3490K. All of the temperature, voltage and current settings can be modified for maximum flexibility.

Table 6. Tabular Representation of the JEITA system, Default JEITA Values and β = 3490K Equivalent Temperatures

jeita_region	vcharge_jeita	Charge Voltage	icharge_jeita	Charge Current	JEITA Temperature	thermistor_voltage	RNTC	Temp
R1	Charger Off							
					jeita_t1	**16117**	28215Ω	0°C
R2	**15**	3.60V	**15**	16mV/R_{SNSB}				
					jeita_t2	**14113**	18290Ω	10°C
R3	**15**	3.60V	**31**	32mV/R_{SNSB}				
					jeita_t3	**7970**	5751Ω	40°C
R4	**7**	3.50V	**31**	32mV/R_{SNSB}				
					jeita_t4	**7112**	4832Ω	45°C
R5	**7**	3.50V	**15**	16mV/R_{SNSB}				
					jeita_t5	**6325**	4080Ω	50°C
R6	**3**	3.45V	**15**	16mV/R_{SNSB}				
					jeita_t6	**4970**	2948Ω	60°C
R7	Charger Off							