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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Triple Hot Swap Controller with Multifunction Current Control

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Three Supply Voltages from 1.7V to 16.5V with $V_{CC1} \geq V_{CC2} \geq V_{CC3}$**
- **Programmable Soft-Start with Inrush Current Limiting, No External Gate Capacitor Required**
- **Faster Turn-Off Time with No Gate Capacitor**
- **Dual Level Overcurrent Fault Protection**
- **Programmable Overcurrent Response Time**
- **Programmable Overvoltage Protection**
- **Automatic Retry or Latched Mode Operation**
- Independent N-Channel FET High Side Drivers
- User-Programmable Supply Voltage Power-Up Rate
- FB*n* Pin Monitors V_{OUTn} and Signals $\overline{RESET}n$
- Glitch Filter Eliminates Spurious $\overline{RESET}n$ Signals

APPLICATIONS

- Electronic Circuit Breaker
- Hot Board Insertion and Removal (Either On Backplane or On Removable Card)
- Industrial High Side Switch/Circuit Breaker

DESCRIPTION

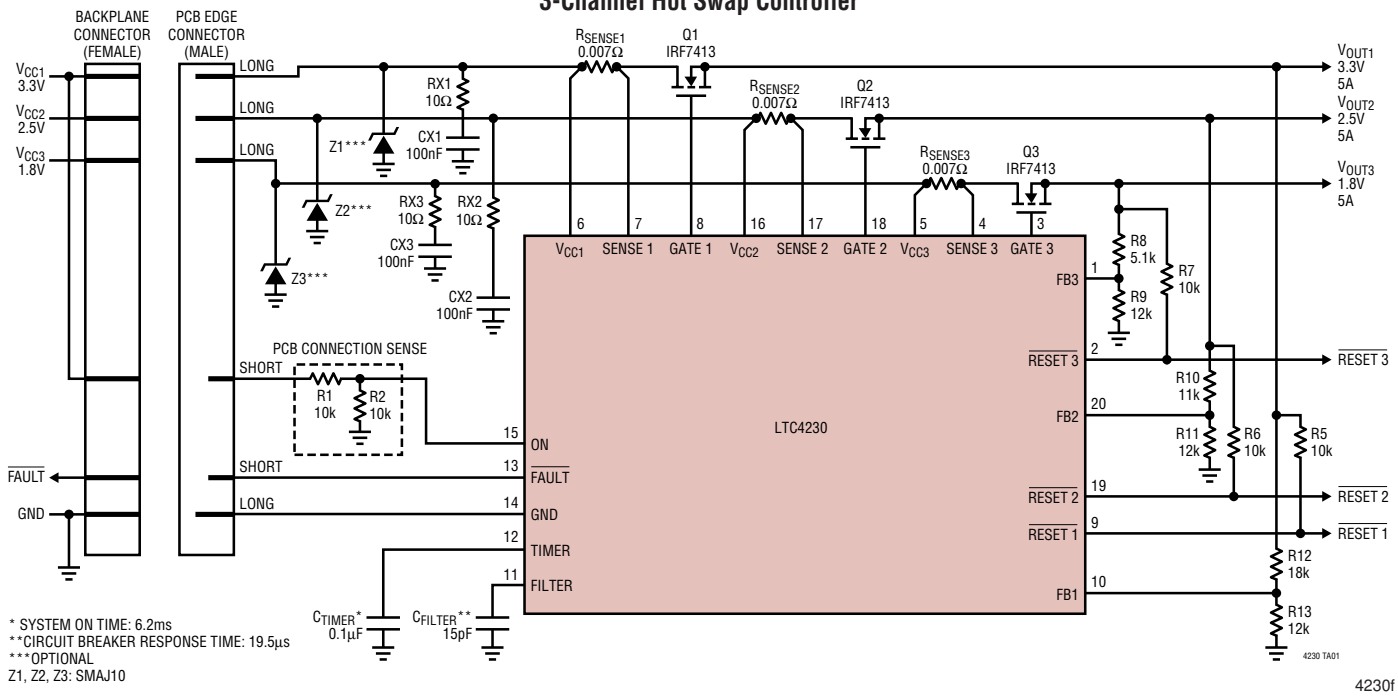
The LTC®4230 is a 3-channel Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. Internal high side switch drivers control the gates of external N-channel MOSFETs for supply voltages ranging from 1.7V to 16.5V. The LTC4230 provides soft-start and inrush current limiting during the programmable start-up period.

On-chip current limit comparators provide dual level circuit breaker protection. The slow comparators trip at V_{CCn} – 50mV and activate in 10µs or are programmed by an external filter capacitor. The fast comparators trip at V_{CCn} – 150mV and typically respond in 500ns.

Each FB*n* pin monitors its own output supply voltage and signals its $\overline{RESET}$ pin. The ON pin turns the chip on and off and can be used for a reset function. The LTC4230 also provides additional functions including fault indication, autoretry or latchoff modes, programmable current limit response time based on the $\overline{FAULT}$ and FILTER pins' functionality.

TYPICAL APPLICATION

3-Channel Hot Swap Controller

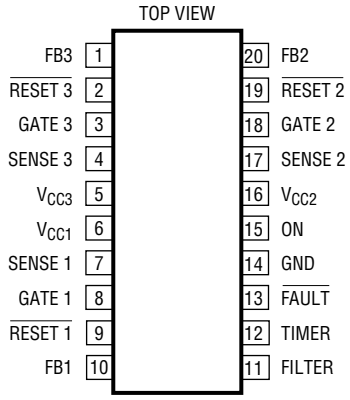


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CCn}) 17V
SENSE*n* Pins ..... –0.3V to (V_{CC} + 0.3V)
FB*n*, ON Pins ..... –0.3V to (V_{CC} + 0.3V)
TIMER Pin .....–0.3V to 2V
GATE*n* Pins ..... Internally Limited (Note 3)
$\overline{RESET}n$, $\overline{FAULT}$, FILTER Pins .....–0.3V to 17V
Operating Temperature Range
LTC4230C ..... 0°C to 70°C
LTC4230I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
20-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC4230CGN LTC4230IGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC1} = 3.3V, V_{CC2} = 2.5V, V_{CC3} = 1.8V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (V_{CC1}) Supply Voltage (V_{CC2}) Supply Voltage (V_{CC3})	 $V_{CC2} \le V_{CC1}$ $V_{CC3} \le (V_{CC1} - 1V)$	● ● ●	2.700 2.375 1.700		16.5 16.5 15.5	V V V
I_{CC}	Supply Current (I_{CC1}) Supply Current (I_{CC2}) Supply Current (I_{CC3})	ON = V_{CC1}, FB1 = High ON = V_{CC1}, FB2 = High ON = V_{CC1}, FB3 = High	● ● ●		1.8 75 65	3 150 150	mA µA µA
V_{LKO1}	Undervoltage Lockout , Channel 1	V_{CC1} Low to High Transition	●	2.15	2.35	2.52	V
V_{LKO2}	Undervoltage Lockout , Channel 2	V_{CC2} Low to High Transition	●	1.98	2.15	2.32	V
V_{LKO3}	Undervoltage Lockout , Channel 3	V_{CC3} Low to High Transition	●	1.09	1.19	1.29	V
$V_{LKOHST1}$	Undervoltage Lockout Hysteresis, Channel 1				100		mV
$V_{LKOHST2}$	Undervoltage Lockout Hysteresis, Channel 2				45		mV
$V_{LKOHST3}$	Undervoltage Lockout Hysteresis, Channel 3				35		mV
$I_{IN, FBn}$	FB*n* Pin Input Current	$0V \le V_{FBn} \le V_{CCn}$	●		±0.1	±10	µA
$I_{IN, ON}$	ON Pin Input Current	$0V \le V_{ON} \le V_{CC1}$	●		±0.1	±10	µA
$I_{IN, SENSEn}$	Input Current for SENSE*n*	$0V \le V_{SENSEn} \le V_{CCn}$	●		±0.1	±15	µA
$V_{CB(FAST)}$ $V_{CB(SLOW)}$	Circuit Breaker*n* Trip Voltage	Fast Comparator Slow Comparator	● ●	135 40	150 50	165 60	mV mV
$I_{GATEn, UP}$	GATE*n* Pull-Up Current	Charge Pump On, $0 \le V_{GATEn} < 0.2V$	●	–12.5	–10	–6.5	µA
$I_{GATEn, DN}$	Normal GATE*n* Pull-Down Current Fast GATE*n* Pull-Down Curent	ON Low, V_{GATEn} = 5V $\overline{FAULT}$ Latched and Circuit Breaker Tripped or in UVLO, V_{GATEn} = 5V			200 16		µA mA
I_{LEAK}	$\overline{RESET}n$ Leakage Current	$V_{\overline{RESET}n}$ = 15V, Pull-Down Device Off	●		±0.1	±2.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC1} = 3.3V, V_{CC2} = 2.5V, V_{CC3} = 1.8V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{GATEn}	External N-Channel Gate Drive	$V_{GATE1,2} - V_{CC1,2}$ (for $V_{CC1,2}$ = 2.7V, $V_{CC3} = V_{CC1} - 1V$)	●	4.5		8	V
		$V_{GATE3} - V_{CC3}$ (for $V_{CC1,2}$ = 2.7V, $V_{CC3} = V_{CC1} - 1V$)	●	5.5		9	V
		$V_{GATE1,2} - V_{CC1,2}$ (for $V_{CC1,2}$ = 3.3V, $V_{CC3} = V_{CC1} - 1V$)	●	5		10	V
		$V_{GATE3} - V_{CC3}$ (for $V_{CC1,2}$ = 3.3V, $V_{CC3} = V_{CC1} - 1V$)	●	6		11	V
		$V_{GATEn} - V_{CCn}$ (for $V_{CC1,2}$ = 5V, $V_{CC3} = V_{CC1} - 1V$)	●	9		16	V
		$V_{GATEn} - V_{CCn}$ (for $V_{CC1,2}$ = 12V or 15V, $V_{CC3} = V_{CC1} - 1V$)	●	7		18	V
$V_{GATEn,0V}$	GATE*n* Overvoltage Lockout Threshold				0.25		V
V_{FBn}	FB*n* Low Threshold Voltage	FB*n* High to Low Transition	●	1.209	1.234	1.259	V
ΔV_{FBn}	FB*n* Line Regulation	2.7V ≤ V_{CC1} ≤ 16.5V			0.5		mV
$V_{FBn,HST}$	FB*n* Hysteresis				3		mV
V_{ONHI}	ON High Threshold Voltage	ON Low to High Transition	●	1.250	1.314	1.380	V
V_{ONLO}	ON Low Threshold Voltage	ON High to Low Transition	●	1.172	1.234	1.270	V
V_{ONHST}	ON Hysteresis				80		mV
I_{FILTER}	FILTER Pull-Up Current	During Slow Fault Condition	●	–2.5	–2	–1.3	µA
	FILTER Pull-Down Current	During Normal and Reset Conditions	●	7	10	13	µA
V_{FILTER}	FILTER Threshold	Latched Off Threshold, FILTER Low to High	●	1.10	1.26	1.42	V
$V_{FILTERHST}$	FILTER Threshold Hysteresis				–70		mV
I_{TMR}	TIMER Pull-Up Current	TIMER On	●	–23	–20	–17	µA
	TIMER Pull-Down Current	TIMER Off, $V_{\overline{FAULT}}$ = Low	●	0.9	1.6	2.3	µA
		V_{TIMER} = 1.5V			2.5		mA
V_{TMR}	TIMER Threshold	TIMER Low to High	●	1.172	1.234	1.27	V
		TIMER High to Low	●		0.3	0.5	V
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Low Threshold Voltage	$\overline{FAULT}$ High to Low	●	1.172	1.234	1.27	V
$V_{\overline{FAULT},HST}$	$\overline{FAULT}$ Hysteresis	$\overline{FAULT}$ Low to High			50		mV
$I_{\overline{FAULT},UP}$	$\overline{FAULT}$ Pull-Up Current		●	–2.5	–2	–1.5	µA
$V_{OL\overline{FAULT}}$	Output Low Voltage	$I_{\overline{FAULT}}$ = 1.6mA, V_{CC1} = 5V	●		0.19	0.4	V
$V_{OL\overline{RESETn}}$	Output Low Voltage	$I_{\overline{RESETn}}$ = 1.6mA, V_{CC1} = 5V	●		0.19	0.4	V
t_{GATEFC}	Fast COMP*n* Trip to GATE*n* Discharging	V_{CB} = 0mV to 200mV Step	●		0.5	1	µs
$t_{\overline{FAULT}SC}$	Slow Comparator Trip to	V_{CB} = 0mV to 100mV Step, FILTER Floating			10		µs
	FILTER High and $\overline{FAULT}$ Latched	10nF at FILTER Pin to GND	●		7	12	ms
t_{OVPFTR}	FILTER Comparator Trip to GATE*n* Discharging	V_{FILTER} = 0V to 5V	●		8	12	µs
$t_{EXT\overline{FAULT}}$	$\overline{FAULT}$ Low to GATE Discharging	$V_{\overline{FAULT}}$ = 5V to 0V	●	1.5	3	4.5	µs
$t_{\overline{RESET}}$	Circuit Breaker Reset Time	ON Held Low to Guarantee $\overline{FAULT}$ High	●		15	30	µs
t_{OFF}	Turn-Off Time	ON Goes Low to GATE*n* Off			8		µs

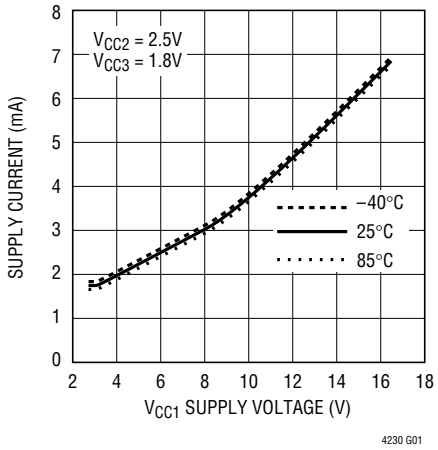
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All current into device pins is positive; all current out of device pins is negative; all voltages are referenced to ground unless otherwise specified.

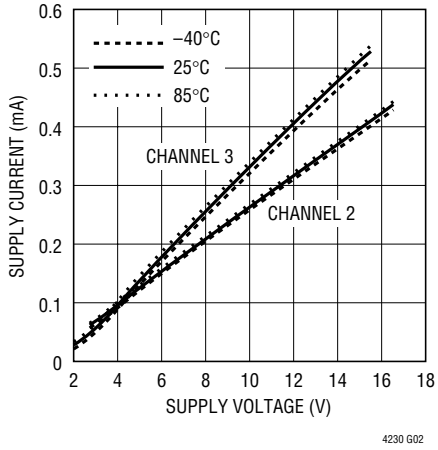
Note 3: An internal zener at the GATE*n* pin clamps the charge pump voltage to a typical maximum operating voltage of 26V. External overdrive of the GATE*n* pin beyond the internal zener voltage may damage the part. The GATE*n* capacitance must be <0.15µF at maximum V_{CC}. If a lower GATE*n* pin voltage is desired, use an external zener diode.

TYPICAL PERFORMANCE CHARACTERISTICS

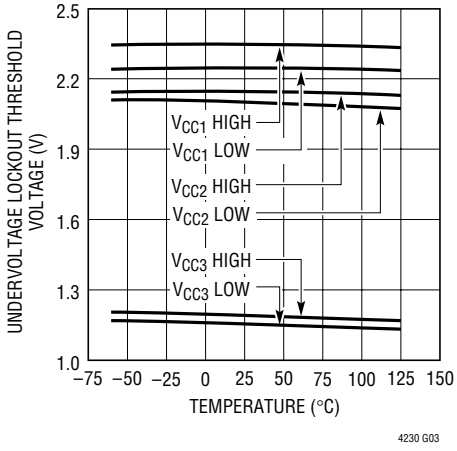
Channel 1 Supply Current vs V_{CC1} Supply Voltage



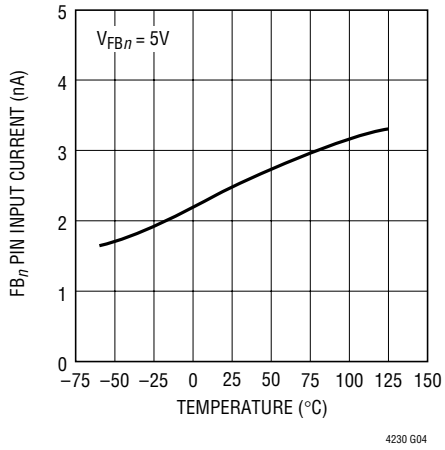
Channels 2 and 3 Supply Current vs Supply Voltage



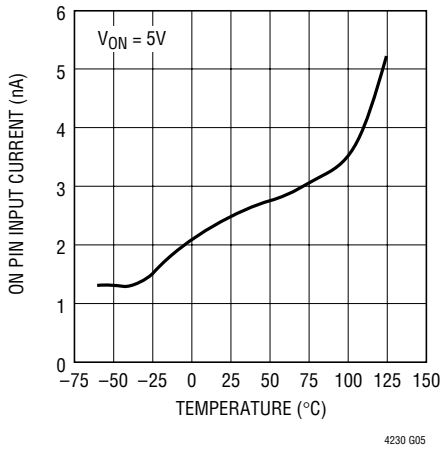
UVLO Threshold Voltage vs Temperature



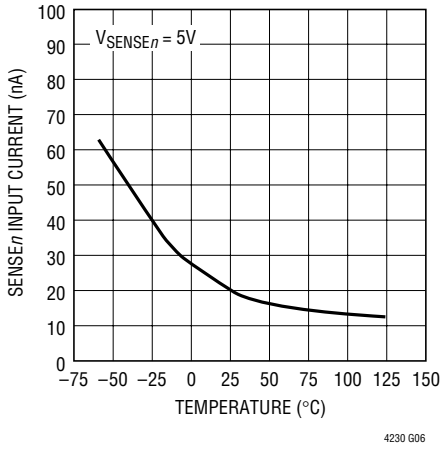
FB*n* Pin Input Current vs Temperature



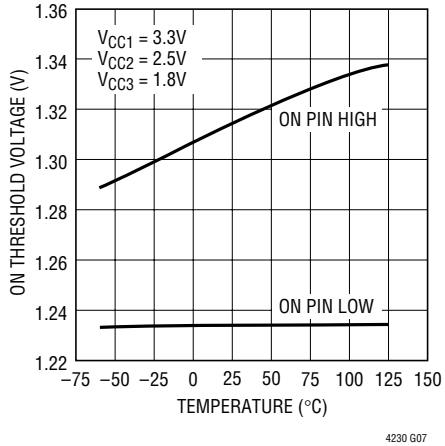
ON Pin Input Current vs Temperature



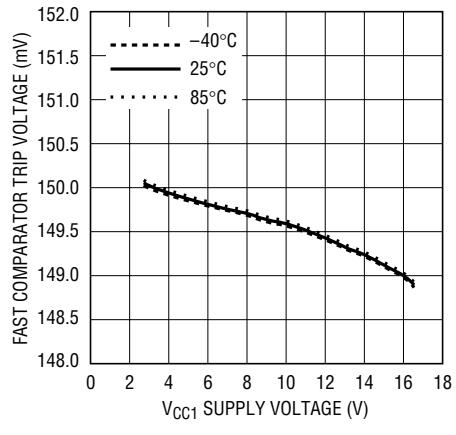
SENSE*n* Input Current vs Temperature



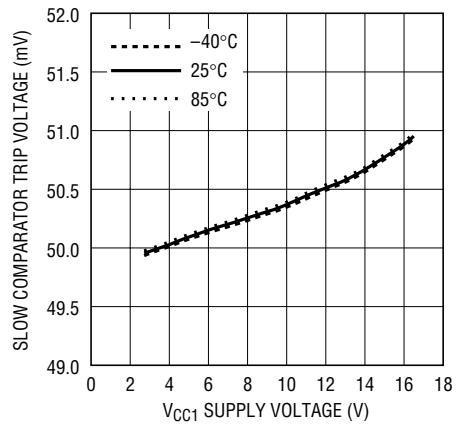
ON Threshold vs Temperature



Fast Comparator Threshold vs V_{CC1} Supply Voltage

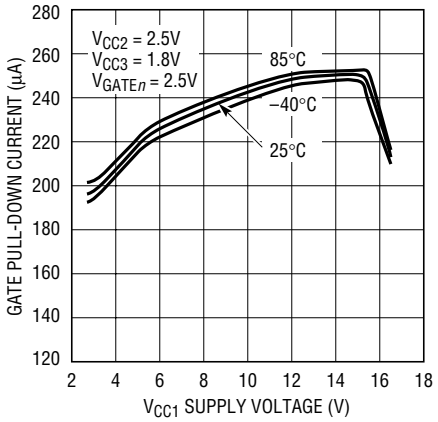


Slow Comparator Threshold vs V_{CC1} Supply Voltage

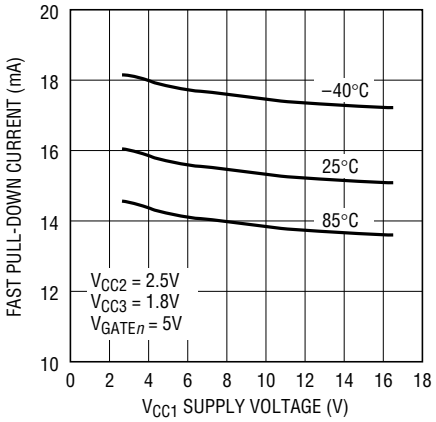


TYPICAL PERFORMANCE CHARACTERISTICS

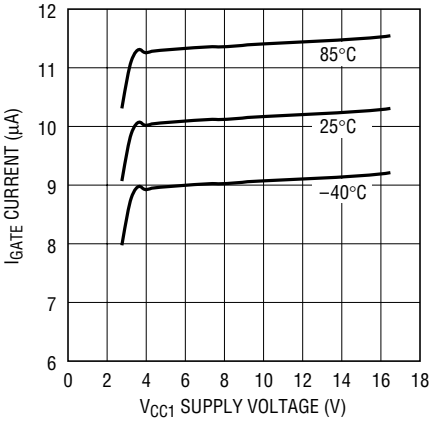
Normal GATE*n* Pull-Down Current vs V_{CC1} Supply Voltage



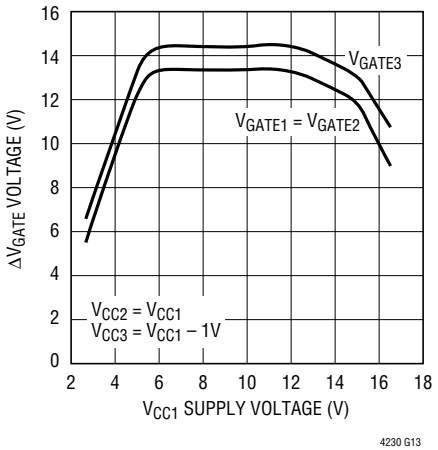
Fast GATE*n* Pull-Down Current vs V_{CC1} Supply Voltage



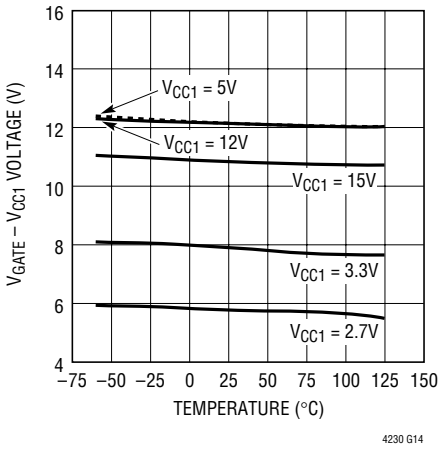
GATE*n* Output Source Current (Pull-Up) vs V_{CC1} Supply Voltage



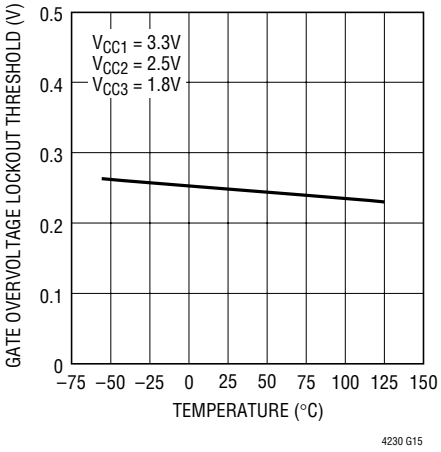
$V_{GATEn} – V_{CCn}$ vs V_{CC1} Supply Voltage



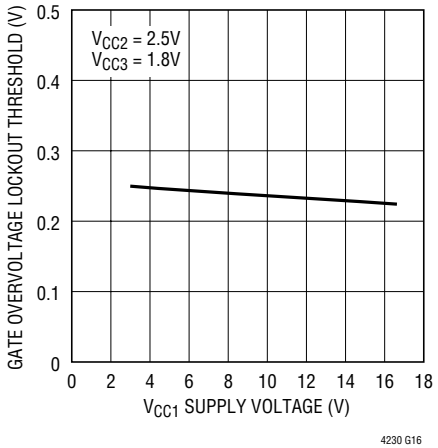
$V_{GATE1} – V_{CC1}$ vs Temperature



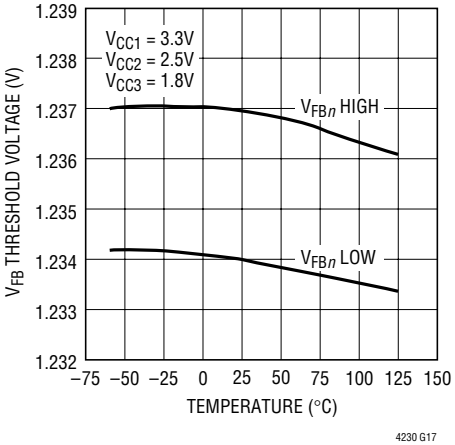
GATE*n* Overvoltage Lockout Threshold vs Temperature



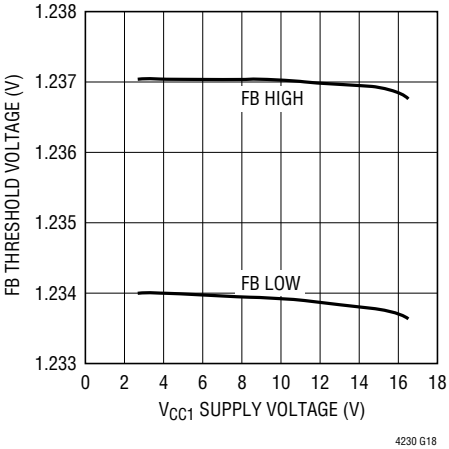
GATE*n* Overvoltage Lockout Threshold vs V_{CC1} Supply Voltage



V_{FBn} Threshold Voltage vs Temperature

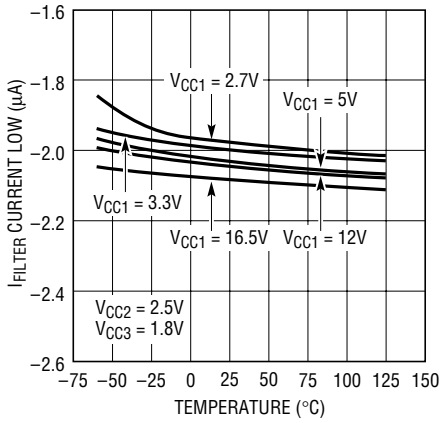


V_{FBn} Threshold Voltage vs V_{CC1} Supply Voltage

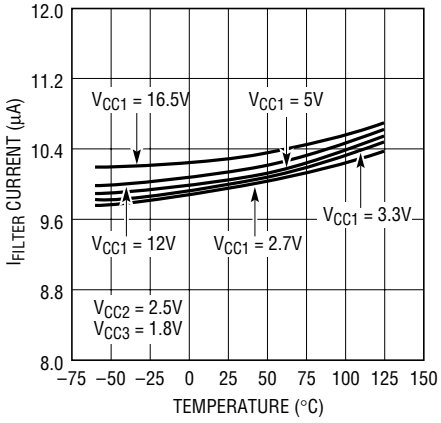


TYPICAL PERFORMANCE CHARACTERISTICS

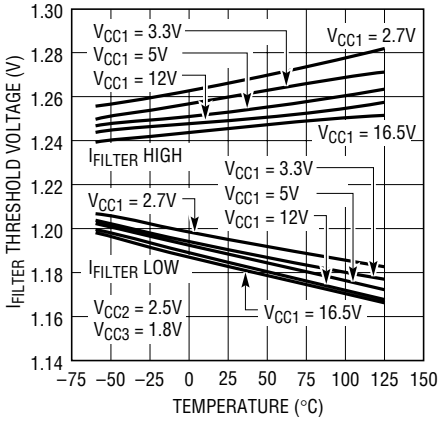
FILTER Pull-Up Current vs Temperature



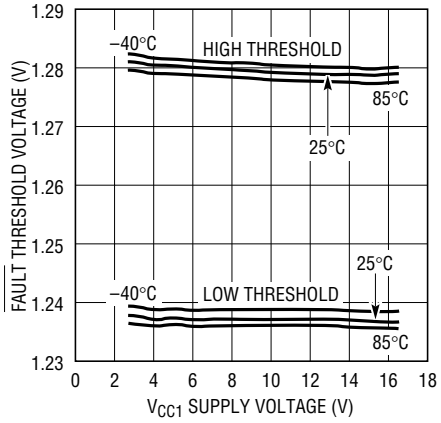
FILTER Pull-Down Current vs Temperature



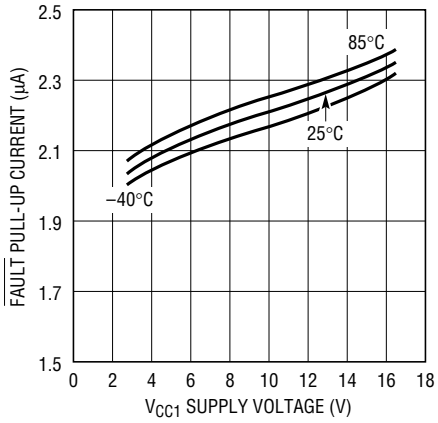
FILTER Threshold Voltage vs Temperature



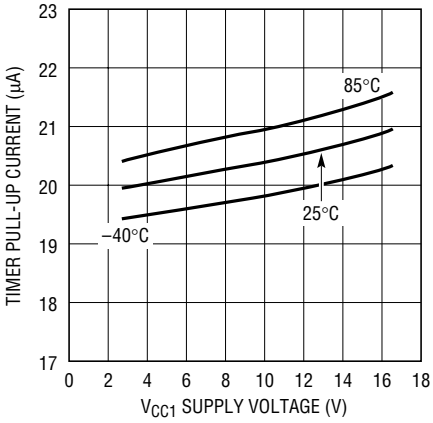
$\overline{FAULT}$ Threshold Voltage vs V_{CC1} Supply Voltage



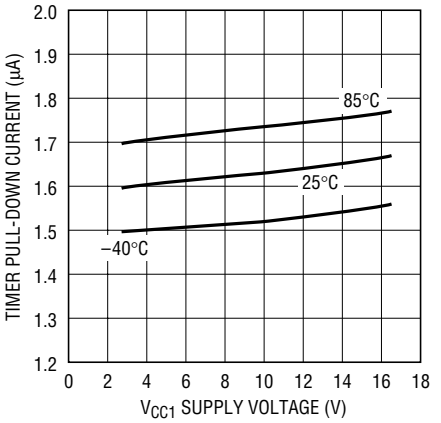
$\overline{FAULT}$ Pull-Up Current vs V_{CC1} Supply Voltage



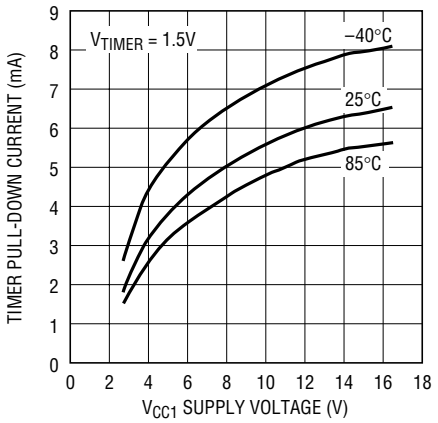
TIMER Pull-Up Current (During First Cycle) vs V_{CC1} Supply Voltage



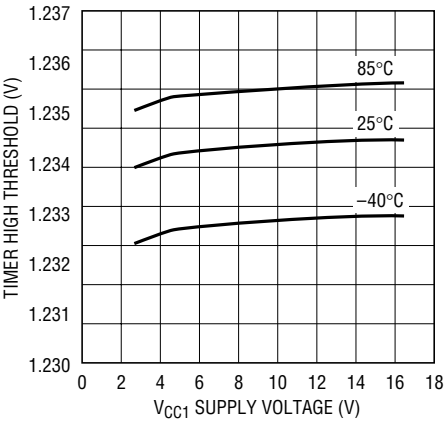
TIMER Pull-Down Current (After Second Cycle) vs V_{CC1} Supply Voltage



TIMER Fast Pull-Down (End of the First Cycle) Current vs V_{CC1} Supply Voltage

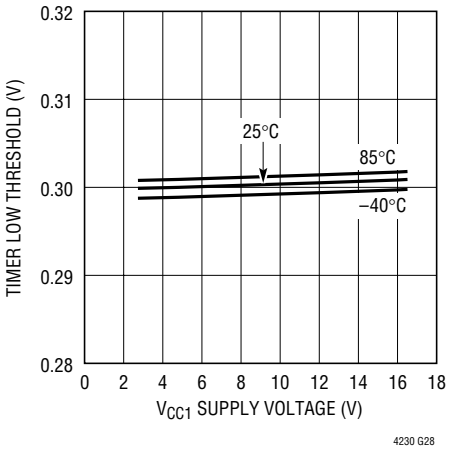


TIMER High Threshold vs V_{CC1} Supply Voltage

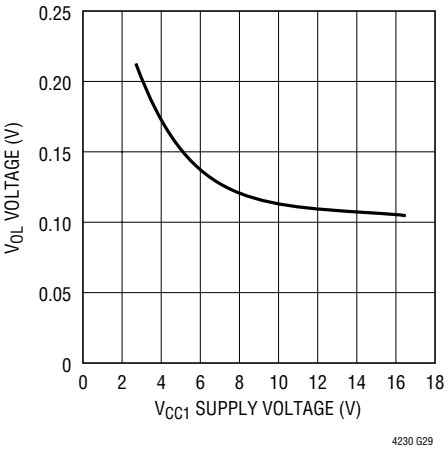


TYPICAL PERFORMANCE CHARACTERISTICS

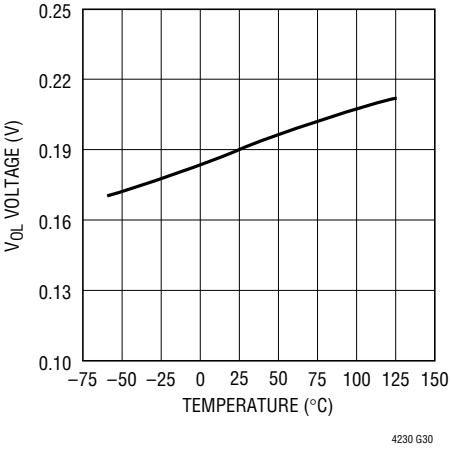
TIMER Low Threshold vs V_{CC1} Supply Voltage



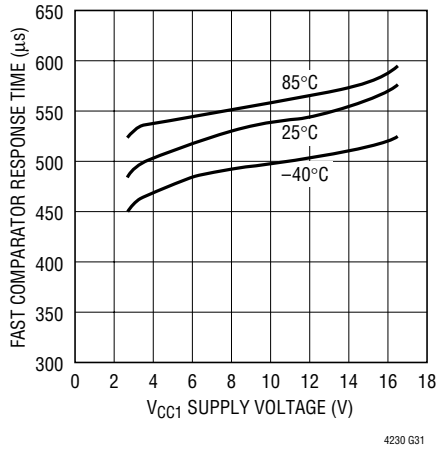
V_{OL} ($\overline{RESET}n$, $\overline{FAULT}$) vs V_{CC1} Supply Voltage



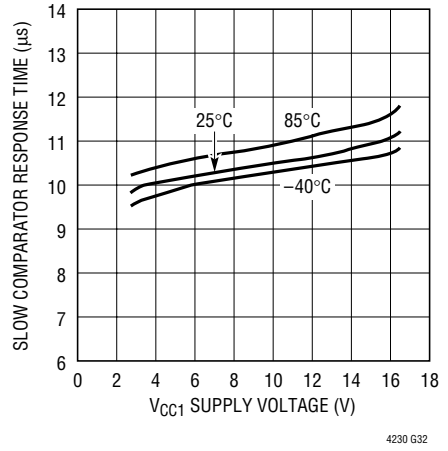
V_{OL} ($\overline{RESET}n$, $\overline{FAULT}$) vs Temperture



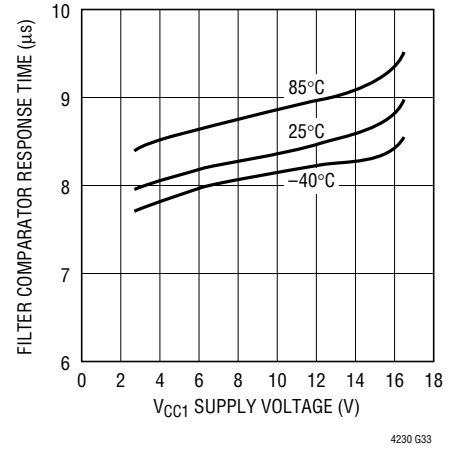
Fast Comparator Response Time vs V_{CC1} Supply Voltage



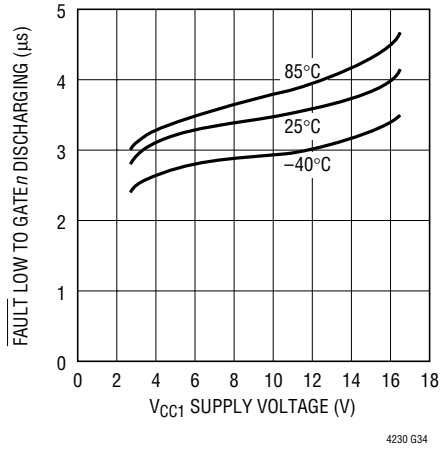
Slow Comparator Response Time (FILTER Floating) vs V_{CC1} Supply Voltage



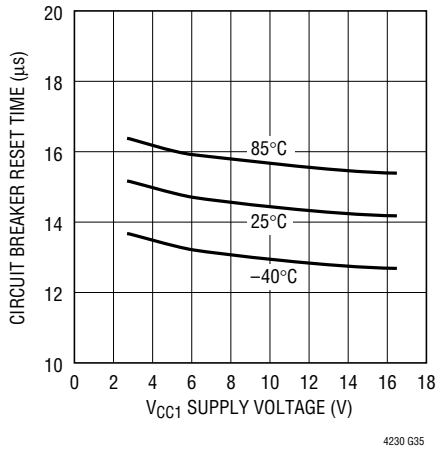
FILTER Comparator Response Time vs V_{CC1} Supply Voltage



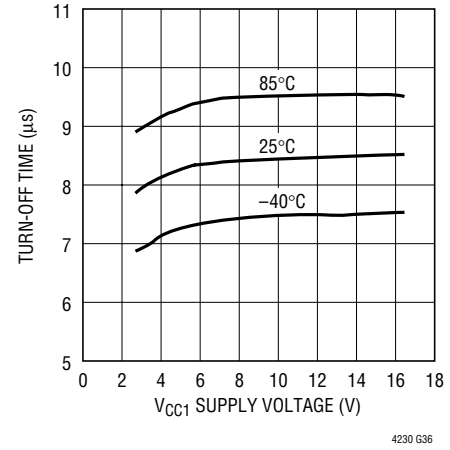
$\overline{FAULT}$ Low to GATEn Discharging vs V_{CC1} Supply Voltage



Circuit Breaker Reset Time vs V_{CC1} Supply Voltage



Turn-Off Time vs V_{CC1} Supply Voltage



PIN FUNCTIONS

FB3 (Pin 1): The FB3 (Feedback) pin is an input to the FBCOMP3 comparator which monitors the V_{CC3} output supply voltage through an external resistor divider. If V_{FB3} < 1.234V, $\overline{RESET\ 3}$ pin pulls low. An internal glitch filter at FBCOMP3's output prevents triggering a reset condition due to negative voltage transients. If V_{FB3} > 1.237V, $\overline{RESET\ 3}$ pin goes high after exiting undervoltage lockout.

$\overline{RESET\ 3}$ (Pin 2): An open-drain N-channel device whose source connects to GND (Pin 14). This pin pulls low if the voltage at FB3 (Pin 1) falls below the FB3 threshold (1.234V). This pin requires an external pull-up resistor to V_{OUT3}. If an undervoltage lockout condition occurs, $\overline{RESET\ 3}$ pulls low independently of FB3 to prevent false glitches.

GATE 3 (Pin 3): The output signal at this pin is the high side gate drive for Channel 3's external N-channel MOSFET pass transistor. An internal charge pump produces a 4.5V (minimum) to 18V (maximum) gate drive voltage for V_{CC1} supply voltages from 2.7V to 16.5V, respectively.

As shown in the Block Diagram for each channel, an internal charge pump supplies a 10µA gate current and sufficient gate voltage drive to the external MOSFET. The internal charge pump produces a minimum 4.5V gate drive for V_{CC1} < 4.75V. For V_{CC1} > 4.75V, the minimum gate voltage drive is 9V. For $V_{CC1} \geq 12V$, the minimum gate voltage drive is 7V which is set by an internal zener diode clamp connected between the GATE 3 pin and GND.

SENSE 3 (Pin 4): Circuit Breaker Sense Pin for Channel 3. With a sense resistor placed in the power path between V_{CC3} and SENSE 3, Channel 3's electronic circuit breaker trips if the voltage across the sense resistor (V_{CC3} – V_{SENSE3}) exceeds the thresholds set internally for SLOW COMP3 and FAST COMP3, as shown in the Block Diagram. The threshold for SLOW COMP3 is $V_{CB(SLOW)}$ = 50mV, and the electronic circuit breaker trips if the voltage across R_{SENSE3} exceeds 50mV for 10µs, or for the time delay programmed by C_{FILTER}. To adjust SLOW COMP3's delay, please refer to the section on Adjusting SLOW COMP*n*'s Response Time.

Under transient conditions where large step current changes can and do occur over shorter periods of time, a second (fast) comparator instead trips the electronic circuit breaker. The threshold for FAST COMP3 is set at $V_{CB(FAST)}$ = 150mV, and the circuit breaker trips if the voltage across the R_{SENSE3} exceeds 150mV for more than 500ns. FAST COMP3's delay is fixed in the LTC4230 and cannot be adjusted. To disable Channel 3's electronic circuit breaker, connect the V_{CC3} and SENSE 3 pins together.

V_{CC3} (Pin 5): Positive Supply Input for Channel 3. V_{CC3} operates from 1.7V to 15.5V ($V_{CC3} \leq V_{CC1}$ – 1V) and its supply current, I_{CC3}, is typically 65µA. The master UVLO circuit disables all three GATE*n* outputs of the LTC4230 until the voltage at V_{CC3} exceeds 1.19V.

V_{CC1} (Pin 6): This is the positive supply input to the LTC4230, the power supply input for Channel 1, and the power supply input for all three internal charge pumps. The LTC4230 operates from 2.7V to 16.5V, and the I_{CC1} supply current is typically 1.8mA. The master UVLO circuit disables all three GATE*n* outputs of the LTC4230 if V_{CC1} is less than 2.35V. The internal charge pump outputs are enabled when V_{CC1} > 2.35V, V_{CC2} > 2.15V, and V_{CC3} > 1.19V.

SENSE 1 (Pin 7): Circuit Breaker Sense Pin for Channel 1. With a sense resistor placed in the power path between V_{CC1} and SENSE 1, Channel 1's electronic circuit breaker trips if the voltage across the sense resistor (V_{CC1} – V_{SENSE1}) exceeds the thresholds set internally for SLOW COMP1 and FAST COMP1, as shown in the Block Diagram. The threshold for SLOW COMP1 is $V_{CB(SLOW)}$ = 50mV, and the electronic circuit breaker trips if the voltage across R_{SENSE1} exceeds 50mV for 10µs, or for the time delay programmed by C_{FILTER}. To adjust SLOW COMP1's delay, please refer to the section on Adjusting SLOW COMP*n*'s Response Time.

Under transient conditions where large step current changes can and do occur over shorter periods of time, a second (fast) comparator instead trips the electronic circuit breaker. The threshold for FAST COMP1 is set at $V_{CB(FAST)}$ = 150mV, and the circuit breaker trips if the voltage across the R_{SENSE1} exceeds 150mV for more than 500ns. FAST COMP1's delay is fixed in the LTC4230 and cannot be adjusted. To disable Channel 1's electronic circuit breaker, connect the V_{CC1} and SENSE 1 pins together.

PIN FUNCTIONS

GATE 1 (Pin 8): The output signal at this pin is the high side gate drive for Channel 1's external N-channel FET pass transistor. An internal charge pump produces a 4.5V (minimum) to 18V (maximum) gate drive voltage for supplies in the range of $2.7V \leq V_{CC1} \leq 16.5V$, respectively.

As shown in the Block Diagram, each channel's internal charge pump is powered by V_{CC1} and supplies a 10µA gate current and sufficient gate voltage drive to the external FET. The internal charge pump produces a minimum 4.5V gate voltage drive for $V_{CC1} < 4.75V$. For $V_{CC1} > 4.75V$, the minimum gate voltage drive is 9V. For $V_{CC1} \geq 12V$, the minimum gate voltage drive is 7V which is set by an internal zener diode clamp connected between the GATE 1 pin and GND.

$\overline{\text{RESET 1}}$ (Pin 9): An open-drain N-channel device whose source connects to GND (Pin 14). This pin pulls low if the voltage at FB1 (Pin 10) falls below the FB1 threshold (1.234V). During the start-up cycle, $\overline{\text{RESET 1}}$ goes high impedance at the end of the second timing cycle after FB1 goes above the FB1 threshold. This pin requires an external pull-up resistor to V_{OUT1}. If an undervoltage lockout condition occurs, $\overline{\text{RESET 1}}$ pulls low independently of FB1 to prevent false glitches.

FB1 (Pin 10): The FB1 (Feedback) pin is an input to the FBCOMP1 comparator which monitors the V_{CC1} output supply voltage through an external resistor divider. If $V_{FB1} < 1.234V$, $\overline{\text{RESET 1}}$ pin pulls low. An internal glitch filter at FBCOMP3's output prevents triggering a reset condition due to negative voltage transients. If $V_{FB1} > 1.237V$ after the second timing cycle, $\overline{\text{RESET 1}}$ goes high.

FILTER (Pin 11): Overcurrent Fault Timing Pin and Overvoltage Fault Set Pin. With a capacitor connected from this pin to ground, the response time of all three SLOW COMP comparators can be adjusted. Note that the response time of the SLOW COMP comparators cannot be adjusted individually.

TIMER (Pin 12): A capacitor connected from this pin to GND sets the LTC4230's system timing. The LTC4230's initial and second start-up timing cycles and its discharge mode delay time are controlled by this capacitor.

$\overline{\text{FAULT}}$ (Pin 13): $\overline{\text{FAULT}}$ is a dual function (an input and an output) internal to the LTC4230. Connected to this pin are an analog comparator (COMP6) and an open-drain N-channel FET. During normal operation, if COMP6 is driven below 1.234V, all electronic circuit breakers trip and each GATE pin pulls low. Referring to the Block Diagram, $\overline{\text{FAULT}}$ incorporates an internal 2µA current source pull up. This allows the LTC4230 to begin a second timing cycle ($V_{\overline{\text{FAULT}}} > 1.284V$) and start up properly. This also allows the use of the $\overline{\text{FAULT}}$ pin as a status output. Under normal operating conditions, the $\overline{\text{FAULT}}$ output is a logic high. Two conditions cause an active low on $\overline{\text{FAULT}}$: 1) the LTC4230's electronic circuit breakers trip because of an output short circuit ($V_{OUTn} = 0V$) or because of a fast output overcurrent transient (FAST COMP*n* trips its circuit breaker); or 2) $V_{FILTER} > 1.26V$. The $\overline{\text{FAULT}}$ output is driven to logic low and is latched logic low until the ON pin is driven to logic low for 30µs (the t_{RESET} duration).

GND (Pin 14): Device Ground Connection. Connect this pin to the system's analog ground plane.

ON (Pin 15): An active high signal used to enable or disable LTC4230 operation. As shown in the LTC4230 Block Diagram, COMP1's threshold is set at 1.234V and its hysteresis is set at 80mV. If a logic high signal is applied to the ON pin ($V_{ON} > 1.314V$), the first timing cycle begins if an overvoltage condition does not exist on any of the GATE*n* pins (Pins 3, 8, and 18). If a logic low signal is applied to the ON pin ($V_{ON} < 1.234V$), each GATE*n* pin is pulled low by an internal, dedicated 200µA current sink. The ON pin can also be used to reset all three electronic circuit breakers. If the ON pin is cycled low for more than 1 $t_{\overline{\text{RESET}}n(MAX)}$ period and then high following a circuit breaker trip, all internal circuit breakers are reset and the LTC4230 begins a new start-up cycle.

V_{CC2} (Pin 16): Positive Supply Input for Channel 2. V_{CC2} operates from 2.375V to 16.5V and its supply current, I_{CC2}, is typically 75µA. The master UVLO circuit disables all three GATE*n* outputs of the LTC4230 until the voltage at V_{CC2} exceeds 2.15V.

PIN FUNCTIONS

SENSE 2 (Pin 17): Circuit Breaker Sense Pin for Channel 2. With a sense resistor placed in the power path between V_{CC2} and SENSE 2, Channel 2's electronic circuit breaker trips if the voltage across the sense resistor ($V_{CC2} – V_{SENSE2}$) exceeds the thresholds set internally for SLOW COMP2 and FAST COMP2, as shown in the Block Diagram. The threshold for SLOW COMP2 is $V_{CB(SLOW)}$ = 50mV and the electronic circuit breaker trips if the voltage across R_{SENSE2} exceeds 50mV for 10µs, or for the time delay programmed by C_{FILTER}. To adjust SLOW COMP2's delay, please refer to the section on Adjusting SLOW COMP*n*'s Response Time.

Under transient conditions where large step current changes can and do occur over shorter periods of time, a second (fast) comparator instead trips the electronic circuit breaker. The threshold for FAST COMP2 is set at $V_{CB(FAST)}$ = 150mV, and the circuit breaker trips if the voltage across the R_{SENSE2} exceeds 150mV for more than 500ns. FAST COMP2's delay is fixed in the LTC4230 and cannot be adjusted. To disable Channel 2's electronic circuit breaker, connect the V_{CC2} and SENSE 2 pins together.

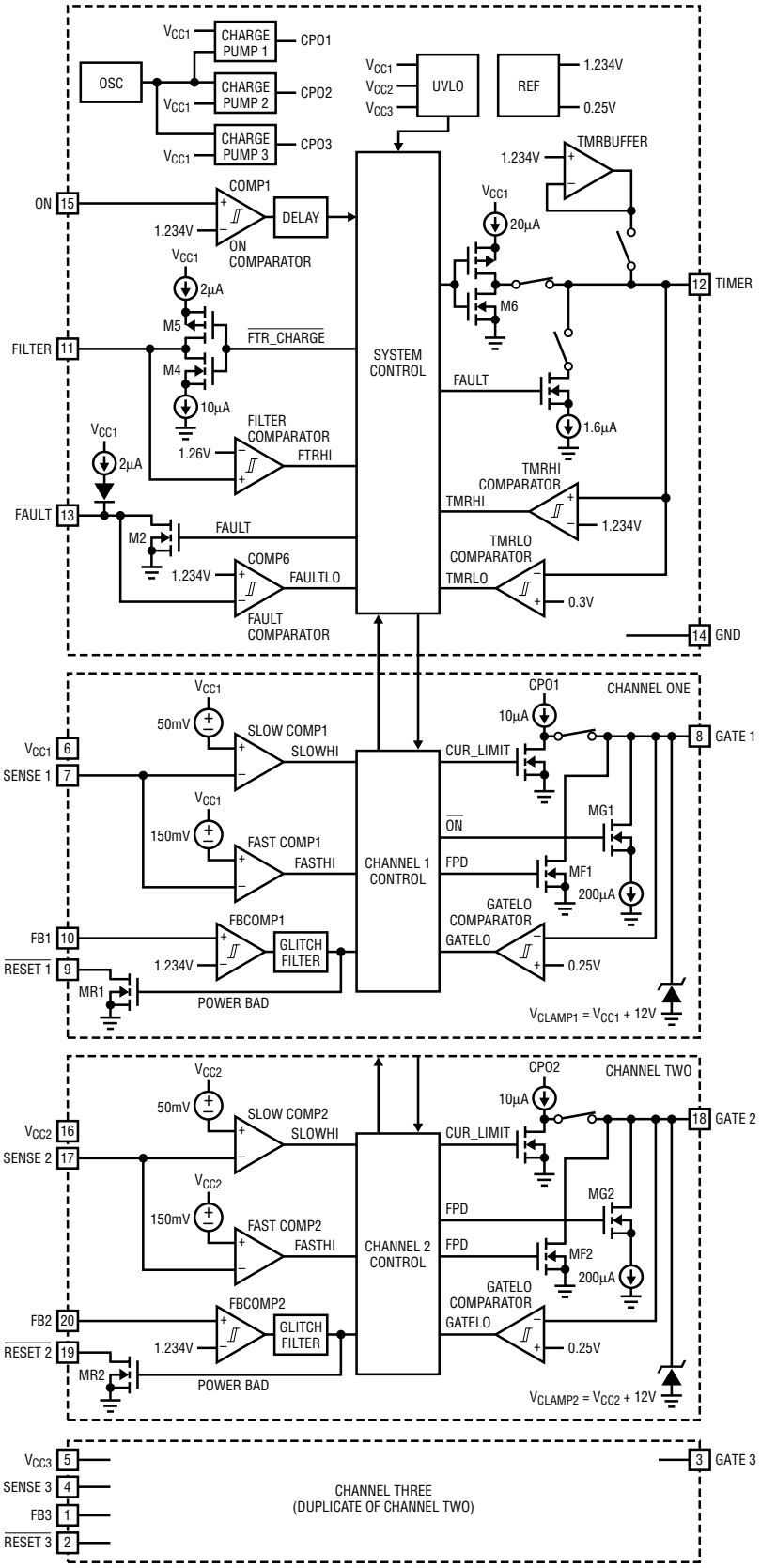
GATE 2 (Pin 18): The output signal at this pin is the high side gate drive for Channel 2's external N-channel FET pass transistor. An internal charge pump produces a 4.5V (minimum) to 18V (maximum) gate drive voltage for V_{CC1} supply voltages from 2.7V to 16.5V, respectively.

As shown in the Block Diagram for each channel, an internal charge pump supplies a 10µA gate current and sufficient gate voltage drive to the external FET. The internal charge pump produces a minimum 4.5V gate drive for V_{CC1} < 4.75V. For V_{CC1} > 4.75V, the minimum gate voltage drive is 9V. For $V_{CC1} \geq 12V$, the minimum gate voltage drive is 7V which is set by an internal zener diode clamp connected between the GATE 2 pin and GND.

$\overline{\text{RESET 2}}$ (Pin 19): An open-drain N-channel device whose source connects to GND (Pin 14). This pin pulls low if the voltage at FB2 (Pin 20) falls below the FB2 threshold (1.234V). This pin requires an external pull-up resistor to V_{OUT2}. If an undervoltage lockout condition occurs, the $\overline{\text{RESET 2}}$ pin pulls low independently of FB2 to prevent false glitches.

FB2 (Pin 20): The FB2 (Feedback) pin is an input to the FBCOMP2 comparator which monitors the V_{CC2} output supply voltage through an external resistor divider. If V_{FB2} < 1.234V, $\overline{\text{RESET 2}}$ pulls low. An internal glitch filter at FBCOMP3's output prevents triggering a reset condition due to negative voltage transients. If V_{FB2} > 1.237V, $\overline{\text{RESET 2}}$ pin goes high after exiting undervoltage lockout.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

HOT CIRCUIT INSERTION

When circuit boards are inserted into or removed from live backplanes, the supply bypass capacitors can draw huge transient currents from the backplane power bus as they charge. The transient currents can cause permanent damage to the connector pins as well as cause glitches on the system supply, causing other boards in the system to reset.

The LTC4230 is designed to turn a printed circuit board's supply voltages on and off in a controlled manner, allowing the circuit board to be safely inserted or removed from a live backplane. The device provides a system reset signal to indicate when board supply voltage drops below a predetermined level, as well as a dual function fault monitor.

OUTPUT VOLTAGE MONITOR

The LTC4230 uses a 1.234V bandgap reference, precision voltage comparators and external resistor dividers to monitor the output supply voltages as shown in Figure 1.

The operation of the supply monitor in normal mode is illustrated in Figure 2. $\overline{\text{RESET 1}}$ pulls low during an undervoltage lockout condition. It remains low until the end of the soft-start cycle (second timing cycle). FB1 then assumes control of $\overline{\text{RESET 1}}$ status. $\overline{\text{RESET 2}}$ and $\overline{\text{RESET 3}}$ also pull low during undervoltage lockout. However, FB2 controls $\overline{\text{RESET 2}}$ and FB3 controls $\overline{\text{RESET 3}}$ status immediately after clearing UVLO (Figure 2, Time Points 5 and 6).

If the voltage at FB*n* drops below its reset threshold (1.234V), the FBCOMP comparator output pulls high. After passing through a glitch filter, $\overline{\text{RESET}n}$ changes state. If the voltage at FB*n* increases above its reset threshold, the FBCOMP comparator output changes state and $\overline{\text{RESET}n}$ pulls high.

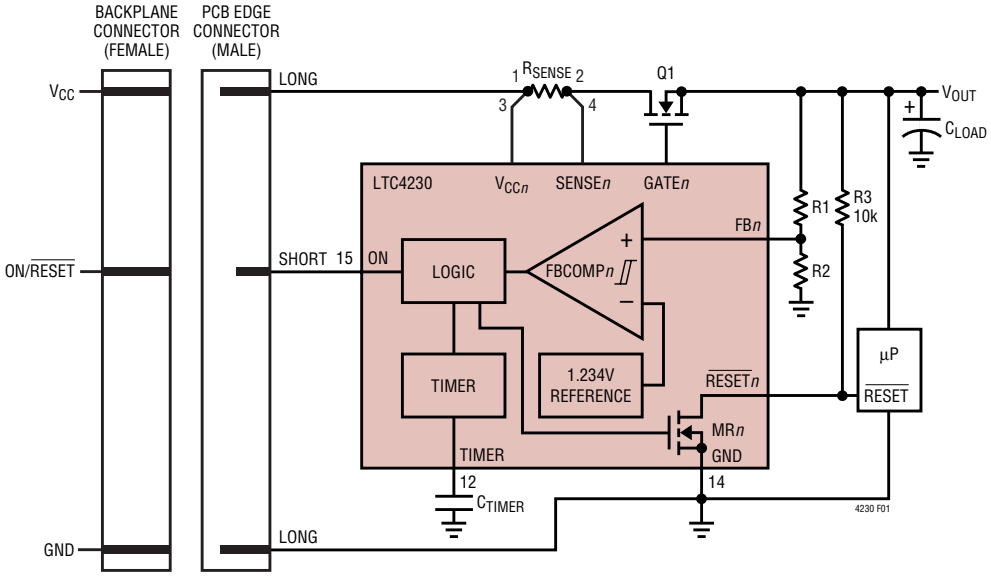


Figure 1. Supply Voltage Monitor Block Diagram

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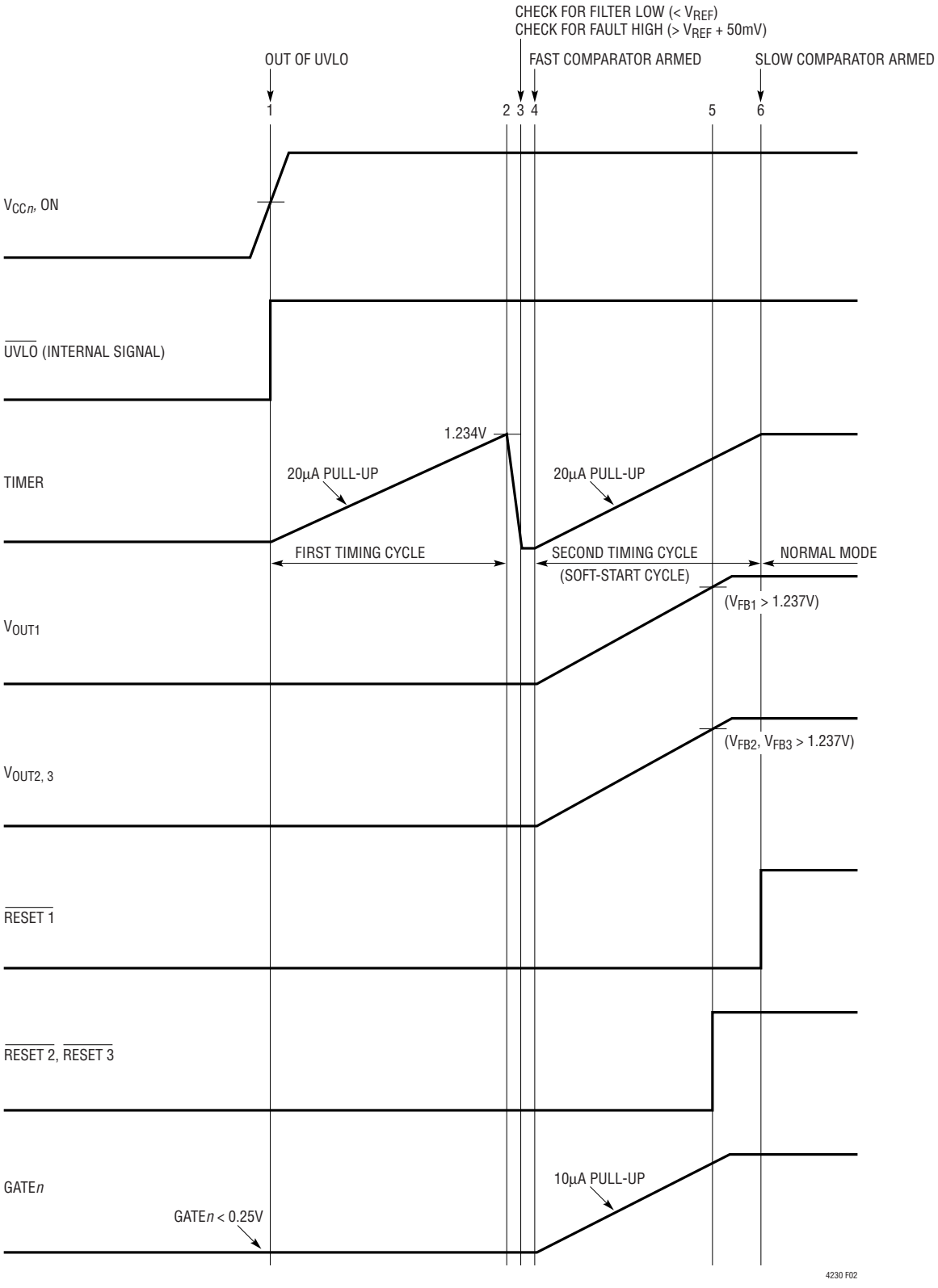

Figure 2. Supply Monitor Waveforms in Normal Mode

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INTERNAL UNDERVOLTAGE LOCKOUT (UVLO)

The LTC4230's power-on reset circuit initializes the start-up condition and ensures the chip is in the proper state if the input supply voltages are too low. If any one of the input supply voltages falls below its corresponding UVLO lower threshold (e.g., $V_{CC1} < 2.25V$, $V_{CC2} < 2.105V$ or $V_{CC3} < 1.155V$), the LTC4230 enters UVLO mode and all three GATE*n* pins are each pulled low by internal 200µA current sinks. Since the LTC4230's UVLO circuits have hysteresis, the device restarts when all three supply voltages rise above their corresponding UVLO high threshold (e.g., $V_{CC1} > 2.35V$, $V_{CC2} > 2.15V$ and $V_{CC3} > 1.19V$) and the ON pin goes high.

In addition, users can utilize the ON comparator (COMP1) or the $\overline{FAULT}$ comparator (COMP6) to effectively program a higher undervoltage lockout level. If the $\overline{FAULT}$ comparator is used for this purpose, the system will wait for the input voltage to increase above the level set by the user before starting the second timing cycle. Also, if the input voltage drops below the set level in normal operating mode, the user must cycle the ON pin or V_{CC1} to restart the system.

GLITCH FILTER FOR $\overline{RESET}$*n*

Each LTC4230 feedback comparator has a glitch filter to prevent $\overline{RESET}$*n* from generating a system reset if there are transients on the FB*n* pin. The relationship between glitch filter time and the feedback transient voltage is shown in Figure 3.

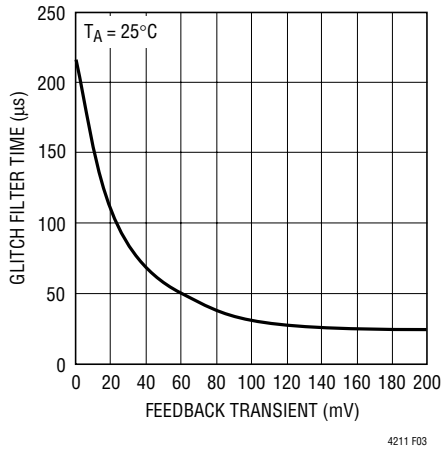

Figure 3. FB Comparator Glitch Filter Time vs Feedback Transient Voltage

SYSTEM TIMING

System timing for the LTC4230 is generated in the equivalent circuit shown in Figure 4. If the LTC4230's internal timing circuit is off, an internal N-channel FET connects the TIMER pin to GND. If the timing circuit is enabled, an internal 20µA current source is then connected to the TIMER pin to charge C_{TIMER} at a rate given by Equation 1:

$$C_{TIMER}\ Charge\text{-}Up\ Rate = \frac{20\mu A}{C_{TIMER}} \quad (1)$$

When the TIMER pin voltage reaches TMRHI's threshold of 1.234V, the TIMER pin is reset to GND. Equation 2 gives an expression for the timer period:

$$t_{TIMER} = 1.234V \bullet \frac{C_{TIMER}}{20\mu A} \quad (2)$$

As a design aid, the LTC4230's timer period as a function of the C_{TIMER} using standard values from 0.1µF to 10µF is shown in Table 1.

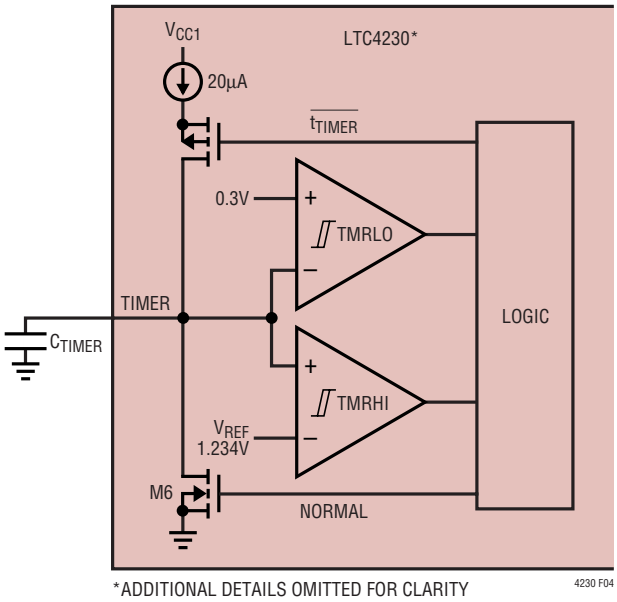

Figure 4. LTC4230 System Timing Block Diagram

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Table 1. t_{TIMER} vs C_{TIMER}

C_{TIMER}	t_{TIMER}
0.1µF	6.2ms
0.22µF	13.6ms
0.33µF	20.4ms
0.47µF	29ms
0.68µF	42ms
0.82µF	50.6ms
1µF	61.7ms
2.2µF	136ms
3.3µF	204ms
4.7µF	290ms
6.8µF	420ms
8.2µF	506ms
10µF	617ms

Ensuring a proper start-up sequence is also dependent on selecting the most appropriate value for C_{TIMER} for the application. Long timing periods affect overall system start-up times. A timing period set too short and the system may never start up. A good starting point is to set C_{TIMER} = 1µF and then adjust its value accordingly for the application.

OPERATING SEQUENCE

Power-Up, Start-Up Check and Plug-In Timing Cycle

The sequence of operations for the LTC4230 is illustrated in the timing diagram of Figure 5. When a PC board is first inserted into a live backplane, the LTC4230 first performs

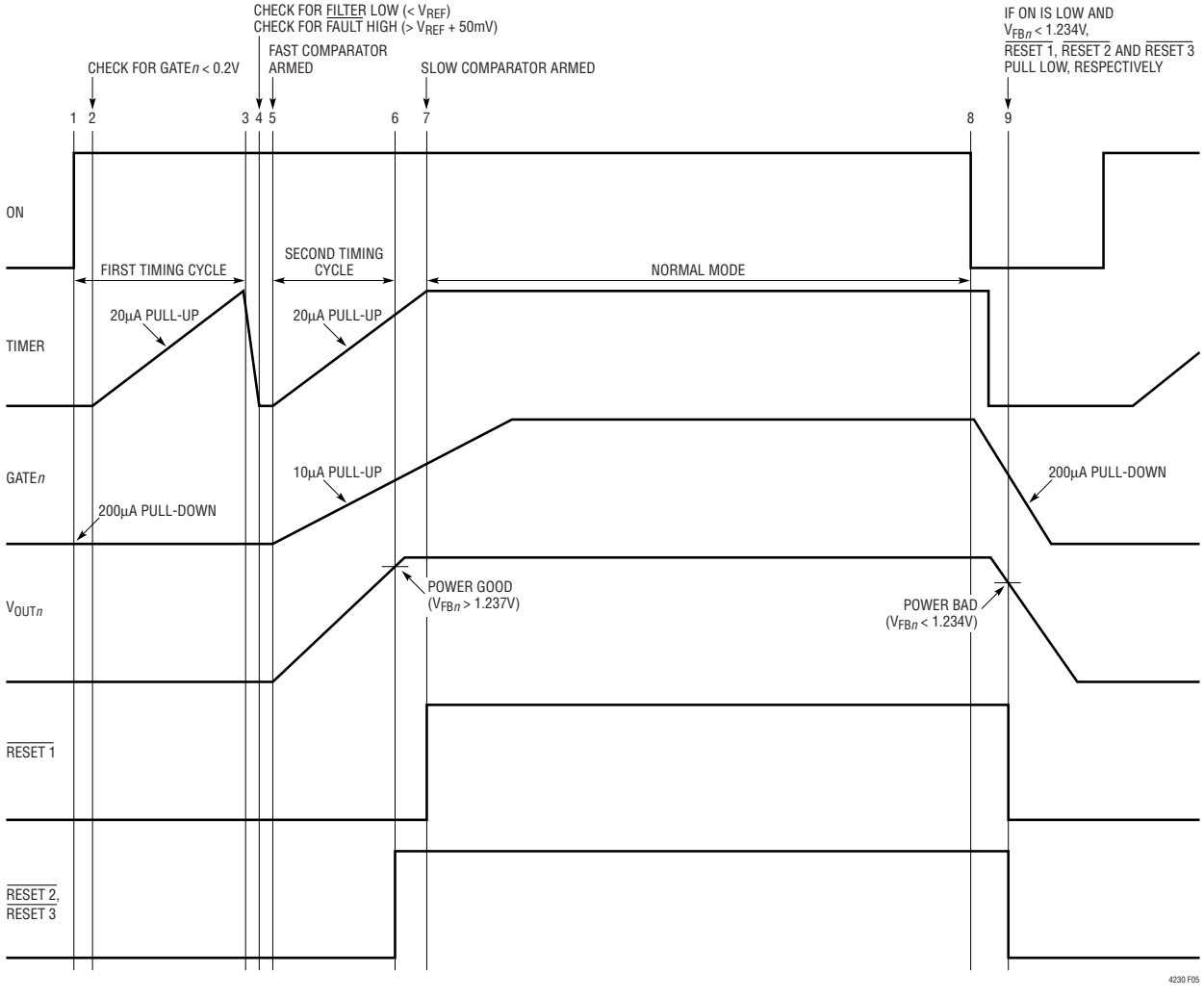

Figure 5. Normal Power-Up Sequence

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a start-up check to make sure the supply voltage is above its 2.3V UVLO threshold (see Time Point 1). If the input supply voltage is valid, the gate of the external pass transistor is pulled to ground by the internal 200µA current source connected at the GATE*n* pin. The TIMER pin is held low by an internal N-channel pull-down transistor (see M6, LTC4230 Block Diagram) and the FILTER pin voltage is pulled to ground by an internal 10µA current source.

Once V_{CC}*n* and ON (the ON pin is >1.314V) are valid, the LTC4230 checks to make sure that GATE*n* is OFF (V_{GATE}*n* < 0.25V) at Time Point 2. An internal timing circuit is enabled and the TIMER pin voltage ramps up at the rate described by Equation 1. At Time Point 3 (the timing period programmed by C_{TIMER}), the TIMER pin voltage equals V_{TMR} (1.234V). Next, the TIMER pin voltage ramps down to Time Point 4 where the LTC4230 performs two checks: (1) FILTER pin voltage is low (V_{FILTER} < 1.19V) and (2) $\overline{FAULT}$ pin voltage is high ($V_{\overline{FAULT}}$ > 1.284V). If both conditions are met, the LTC4230 begins a second timing (soft-start) cycle.

Second Timing (Soft-Start) Cycle

At the beginning of the second timing cycle (Time Point 5), the LTC4230's FAST COMP*n* is armed and an internal 10µA current source working with an internal charge pump provides the gate drive to the external pass transistor. An expression for the GATE*n* voltage slew rate is given by Equation 3:

$$V_{GATE}n \text{ Slew Rate}, \frac{dV_{GATE}n}{dt} = \frac{10\mu A}{C_{GATE}n} \quad (3)$$

where C_{GATE}*n* = Power MOSFET gate input capacitance (C_{ISS}) for Channel *n*.

For example, a Si4410DY (a 30V N-channel power MOSFET) exhibits an approximate C_{GATE} of 3300pF at V_{GS} = 10V. The LTC4230's GATE*n* voltage rate-of-change (slew rate) for this example would be:

$$V_{GATE}n \text{ Slew Rate}, \frac{dV_{GATE}n}{dt} = \frac{10\mu A}{3300pF} = 3.03\frac{V}{ms}$$

The inrush current being delivered to the load while the GATE*n* is ramping is dependent on C_{LOAD}*n* and C_{GATE}*n*. Equation 4 gives an expression for the inrush current during the second timing cycle:

$$I_{INRUSH} = \frac{dV_{GATE}n}{dt} \bullet C_{LOAD}n = 10\mu A \bullet \frac{C_{LOAD}n}{C_{GATE}n} \quad (4)$$

For example, if C_{GATE}*n* = 3300pF and C_{LOAD}*n* = 2000µF, the inrush current charging C_{LOAD}*n* is:

$$I_{INRUSH} = 10\mu A \bullet \frac{2000\mu F}{0.0033\mu F} = 6.06A \quad (5)$$

At Time Point 7, the output voltage trips FBCOMP*n*'s threshold, signaling an output voltage "power good" condition. $\overline{RESET\ 2}$ and $\overline{RESET\ 3}$ pull high. At Time Point 8, $\overline{RESET\ 1}$ asserts high, SLOW COMP is armed and the LTC4230 enters a fault monitor mode.

SOFT-START WITH CURRENT LIMITING

During the second timing cycle, the inrush current is described by Equation 4. Note that there is a one-to-one correspondence in the inrush current to C_{LOAD}*n*. If the inrush current is large enough to cause a voltage drop greater than 50mV across the sense resistor, an internal servo loop controls the operation of the 10µA current source at the GATE*n* pin to regulate the load current to:

$$I_{LIMIT(SOFTSTART)}n = \frac{50mV}{R_{SENSE}n} \quad (6)$$

For example, the inrush current is limited to 5A when R_{SENSE}*n* = 0.01Ω.

In this fashion, the inrush current is controlled and C_{LOAD}*n* is charged up slowly during the soft-start cycle.

The timing diagram in Figure 6 illustrates the operation of the LTC4230 in a normal power-up sequence with limited inrush current as described by Equation 6. At Time Point 5, the GATE pin voltage begins to ramp indicating that the power MOSFET is beginning to charge C_{LOAD}*n*. At Time Point 5, the inrush current causes a 50mV voltage drop across R_{SENSE}*n* and an internal servo loop engages, limiting the inrush current to a fixed level. At Time Point 6, the GATE*n* pin voltage continues to ramp as C_{LOAD}*n* charges until V_{OUT}*n* reaches its final value. The charging current

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reduces, and the internal servo loop disengages. At the end of the soft-start cycle (Time Point 8), all $\overline{\text{RESET}n}$ are high and all SLOW COMP*n* are armed.

Power-Off Cycle

As shown at Time Point 9, an external hard reset is initiated by pulling the ON pin low (V_{ON} < 1.234V). All GATE*n* pin voltages are ramped to ground by the internal 200µA current sources, discharging C_{GATEn} and turning off the pass transistors. As C_{LOADn} discharges, the output voltage crosses FBCOMP*n*'s threshold, signaling a "power bad" condition at Time Point 10. $\overline{\text{RESET}n}$ then asserts low.

FREQUENCY COMPENSATION AT SOFT-START

If the external gate input capacitance (C_{ISS}) is greater than 600pF, no external gate capacitor is required at GATE*n* to stabilize the internal current-limiting loop during soft-start. Otherwise, connect an external gate capacitor between the GATE*n* and GND pins to increase the total gate capacitance above 600pF. The servo loop that controls the external MOSFET during current limiting has a unity-gain frequency of about 105kHz and phase margin of 80° for external MOSFET gate input capacitances to 2.5nF.

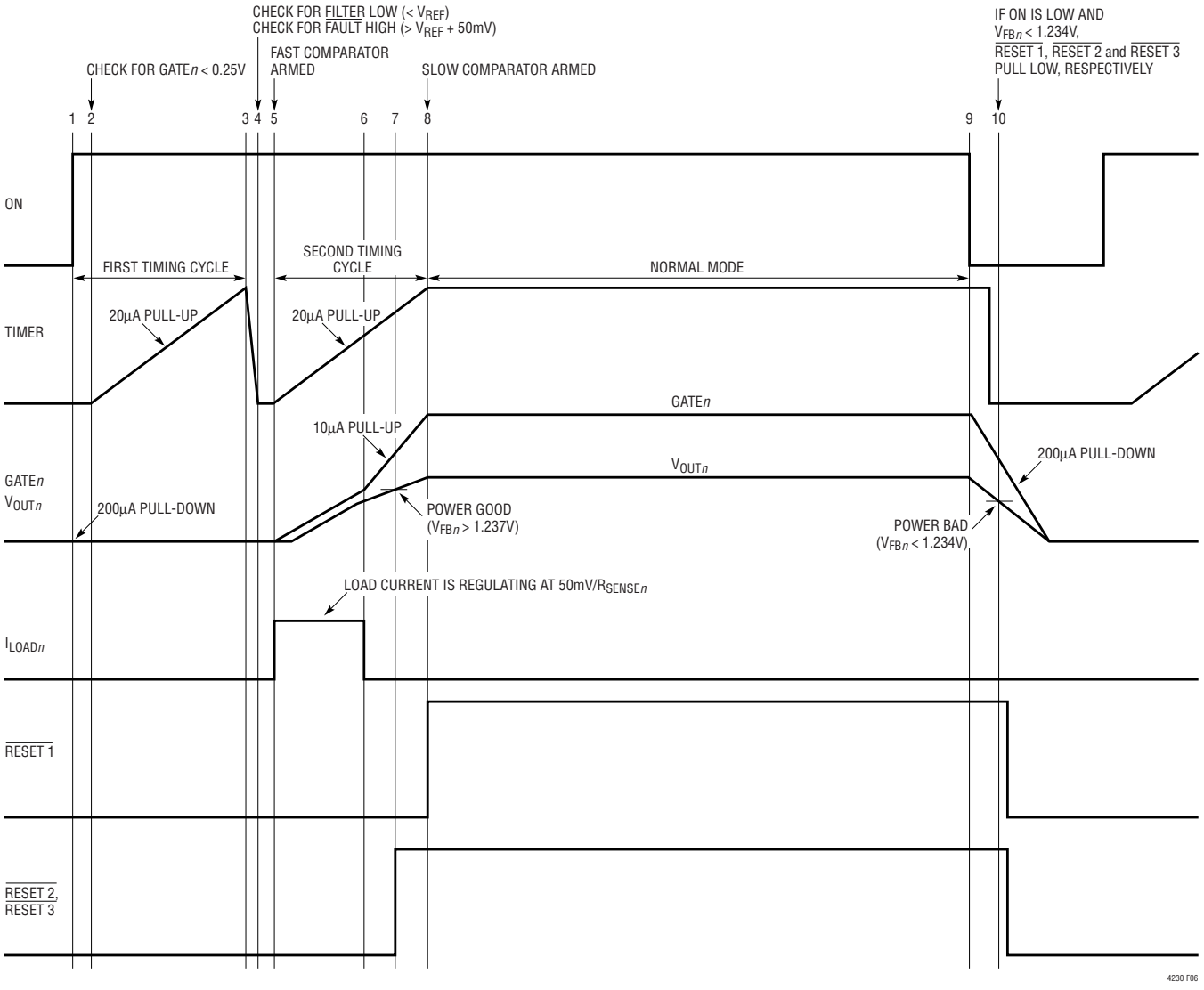

Figure 6. Normal Power-Up Sequence (with Current Limiting in Second Timing Cycle)

APPLICATIONS INFORMATION

USING AN EXTERNAL GATE CAPACITOR

The LTC4230 automatically limits the inrush current in one of two ways: by controlling the GATE*n* pin voltage slew rate or by actively limiting the inrush current. The LTC4230 uses GATE*n* voltage slew rate limiting when $C_{LOAD}n$ is small and/or the inrush current limit is set high. If GATE*n* voltage slew rate control is preferred with large $C_{LOAD}n$, an external capacitor (C_{GX}) can be used from GATE*n* to ground, as shown in Figure 7. According to Equation 3, adding C_{GX} slows the GATE*n* voltage slew rate at the expense of slower system turn-on and turn-off time. Should this technique be used, values for C_{GX} less than 150nF are recommended.

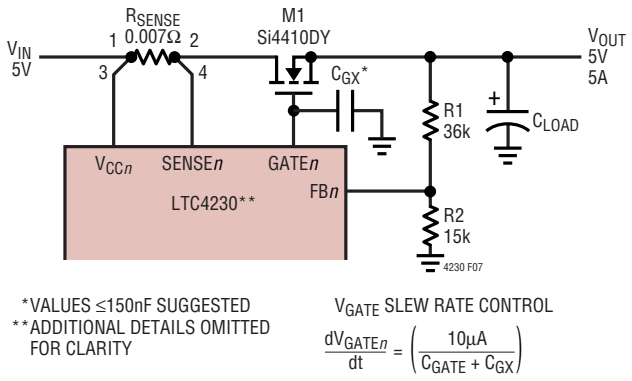

Figure 7. Using an External Capacitor at GATE for GATE Voltage Slew Rate Control and Large C_{LOAD}

An external gate capacitor may also be useful to decrease or eliminate current spikes through the MOSFET when power is first applied. At power-up, the instantaneous input voltage step attempts to pull the MOSFET gate up through the MOSFET's drain-to-gate capacitance. If the MOSFET's C_{ISS} is small, the gate can be pulled up high enough to turn on the MOSFET, thereby allowing a current spike to the output. This event occurs during the time that the LTC4230 is coming out of UVLO and getting its intelligence to hold the GATE pin low. An external capacitor attenuates the voltage to which the GATE is pulled up and eliminates the current spike. The value required is dependent on the MOSFET capacitance specifications. In typical applications, this capacitor is not required.

ELECTRONIC CIRCUIT BREAKER

The LTC4230 features an electronic circuit breaker function. It disconnects loads from power supplies when shorts or excessive load current conditions occur on any of the supplies and generates a FAULT signal. If a circuit breaker trips, its GATE*n* pin is immediately pulled to ground, the external N-channel MOSFET is quickly turned OFF and FAULT is latched low.

The circuit breaker trips whenever the voltage across the sense resistor exceeds two different levels, each level set by the LTC4230's SLOW COMP*n* and FAST COMP*n* (see Block Diagram). The SLOW COMP*n* trips the circuit breaker if the voltage across the SENSE*n* resistor ($V_{CC}n - V_{SENSE}n = V_{CB}$) is greater than 50mV for 10µs. There may be applications where this comparator's response time is not long enough, for example, because of excessive supply voltage noise. To adjust the response time of the SLOW COMP*n*, a capacitor is used at the LTC4230's FILTER pin (see section on Adjusting SLOW COMP*n*'s Response Time). The FAST COMP*n* trips the circuit breaker to protect against fast load overcurrents if the transient voltage across the sense resistor is greater than 150mV for 500ns. The response time of the LTC4230's FAST COMP*n* is fixed.

The timing diagram of Figure 6 illustrates when the LTC4230's electronic circuit breaker is armed. After the first timing cycle, the LTC4230's FAST COMP*n* is armed at Time Point 5. Arming FAST COMP*n* at Time Point 5 ensures that the system is protected against a short-circuit condition during the second timing cycle after $C_{LOAD}n$ has been fully charged. At Time Point 8, SLOW COMP*n* is armed when the internal control loop is disengaged.

The timing diagrams in Figures 8 and 9 illustrate the operation of the LTC4230 when the load current conditions exceed the thresholds of the FAST COMP*n* ($V_{CB(FAST)}$ > 150mV) and SLOW COMP*n* ($V_{CB(SLOW)}$ > 50mV), respectively.

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RESETTING THE ELECTRONIC CIRCUIT BREAKER

Once the LTC4230's circuit breaker is tripped, $\overline{\text{FAULT}}$ is asserted low and the GATE*n* pin is pulled to ground. The LTC4230 remains latched OFF in this fault state until the external fault is cleared. To clear the internal fault detect circuitry and to restart the LTC4230, its ON pin must be driven low (V_{ON} < 1.234V) for at least 30µs, after which time $\overline{\text{FAULT}}$ goes high. Toggling the ON pin from low to high (V_{ON} > 1.314V) initiates a restart sequence in the LTC4230. The timing diagram in Figure 10 illustrates a

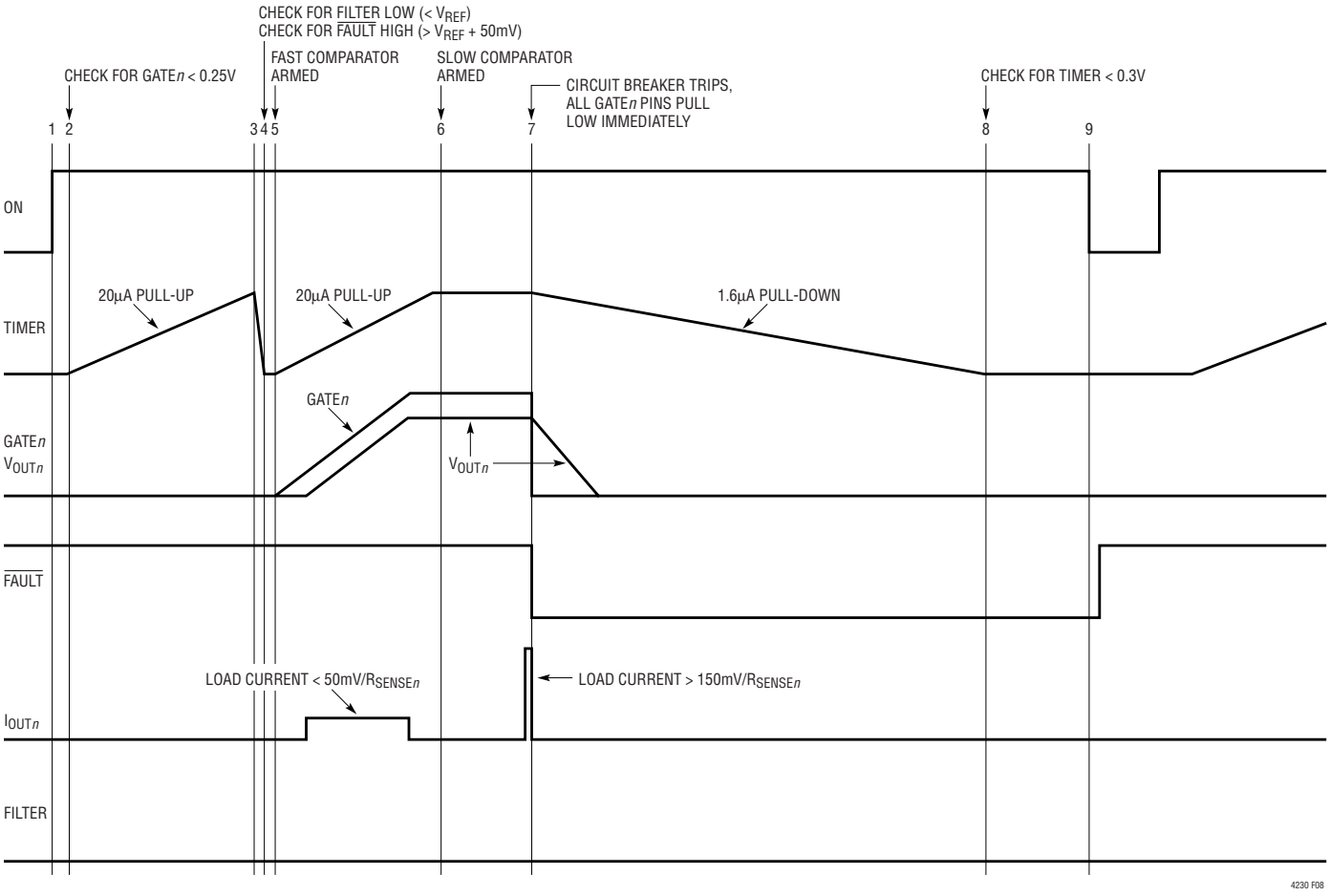

Figure 8. Output Short Circuit Causes Fast Comparator to Trip the Circuit Breaker

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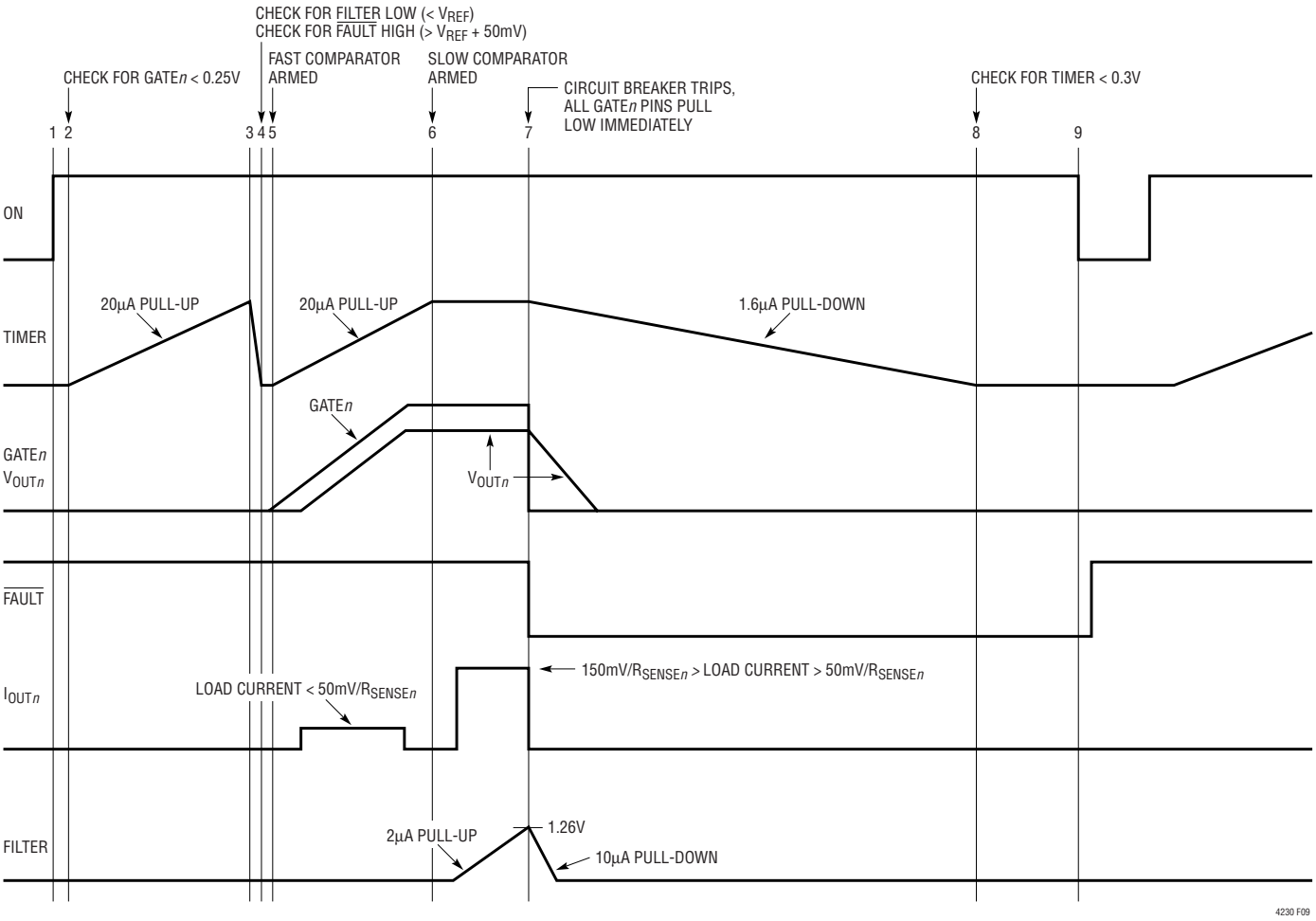

Figure 9. Output Short-Circuit Causes Slow Comparator to Trip Circuit Breaker

APPLICATIONS INFORMATION

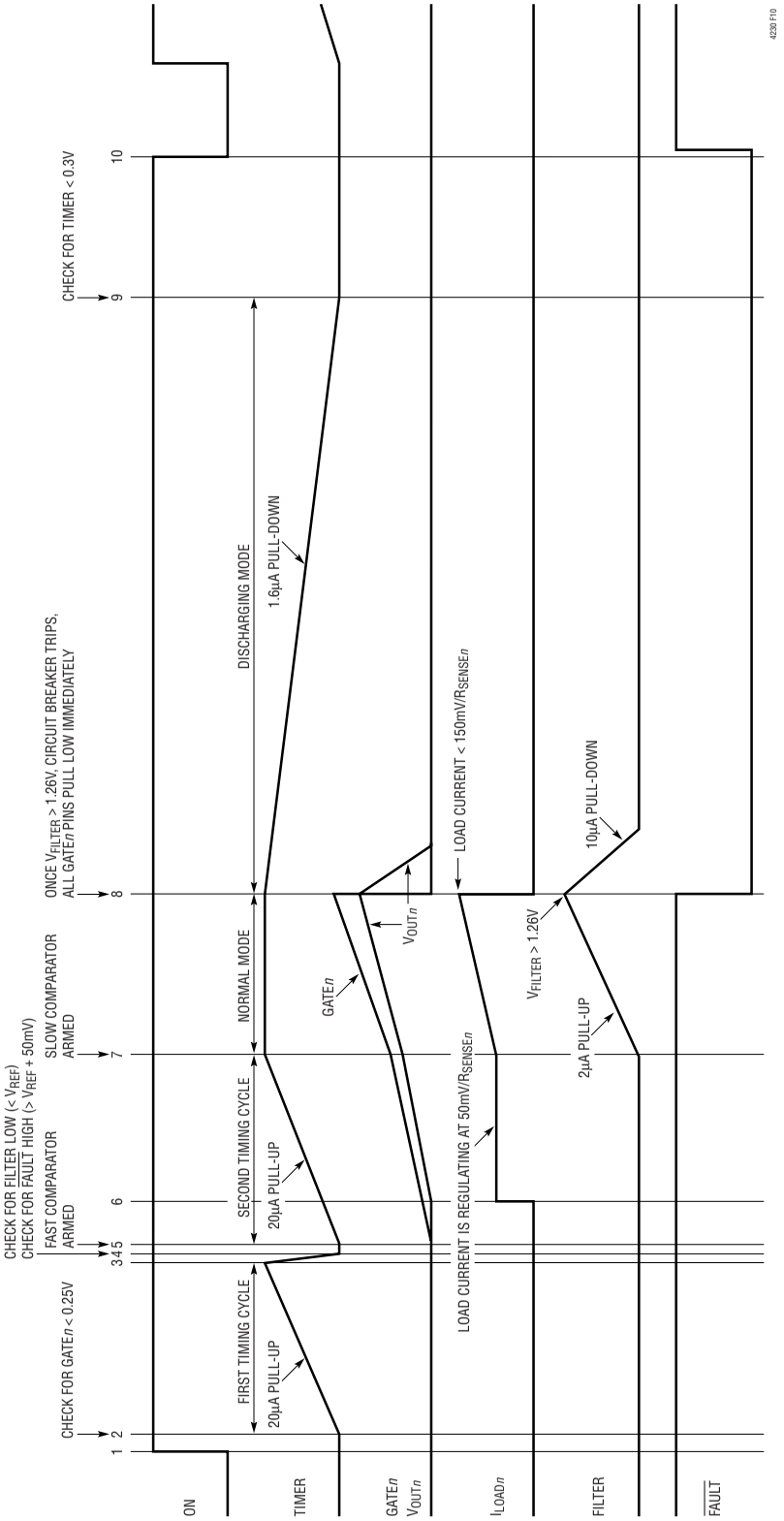

Figure 10. Power-Up into Dead Short in Overcurrent Condition

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start-up sequence where the LTC4230 is powered up into a load overcurrent condition. Note that the circuit breaker trips at Time Point 8 and is reset at Time Point 10.

ADJUSTING SLOW COMP*n*'S RESPONSE TIME

The response time of SLOW COMP*n* is adjusted using a capacitor connected from the LTC4230's FILTER pin to ground. If this pin is left unused, SLOW COMP*n*'s delay defaults to 10µs. During normal operation, the FILTER output pin is held low as an internal 10µA pull-down current source is connected to this pin by transistor M4. This pull-down current source is turned off when an overcurrent load condition is detected by SLOW COMP*n*. During an overcurrent condition, the internal 2µA pull-up current source is connected to the FILTER pin by transistor M5, thereby charging C_{FILTER}. As the charge on the capacitor accumulates, the voltage across C_{FILTER} increases. Once the FILTER pin voltage increases to 1.26V, the electronic circuit breaker trips and the LTC4230's GATE*n* pins are switched quickly to ground by transistor MF*n* (refer to the Block Diagram). After the circuit breaker is tripped, M5 is turned off, M4 is turned on and the 10µA pull-down current then holds the FILTER pin voltage low.

SLOW COMP*n*'s response time from an overcurrent fault condition to when the circuit breaker trips (GATE*n* OFF) is given by Equation 7:

$$t_{SLOWCOMPn} = 1.26V \bullet \frac{C_{FILTER}}{2\mu A} + 10\mu s \qquad (7)$$

For example, if C_{FILTER} = 1000pF, SLOW COMP*n*'s response time = 640µs. As a design aid, SLOW COMP*n*'s delay time ($t_{SLOW\ COMP}$) versus C_{FILTER} for standard values of C_{FILTER} from 100pF to 1000pF is illustrated in Table 2.

Table 2. $t_{SLOWCOMPn}$ vs C_{FILTER}

C_{FILTER}	$t_{SLOWCOMPn}$
100pF	73µs
220pF	149µs
330pF	218µs
470pF	306µs
680pF	438µs
820pF	527µs
1000pF	640µs

SENSE RESISTOR CONSIDERATIONS

The fault current level at which the LTC4230's internal electronic circuit breakers trip is determined by a sense resistor connected between the LTC4230's V_{CCn} and SENSE*n* pins and two separate trip points. The first trip point is set by the SLOW COMP*n*'s threshold, $V_{CB(SLOW)}$ = 50mV, and the trip occurs if a load current fault condition exist for more than 10µs. The current level at which the electronic circuit breaker trips is given by Equation 8:

$$I_{TRIP(SLOW)n} = \frac{V_{CB(SLOW)n}}{R_{SENSEn}} = \frac{50mV}{R_{SENSEn}} \qquad (8)$$

The second trip point is set by the FAST COMP*n*'s threshold, $V_{CB(FAST)}$ = 150mV, and occurs during fast load current transients that exist for 500ns or longer. The current level at which the circuit breaker trips in this case is given by Equation 9:

$$I_{TRIP(FAST)n} = \frac{V_{CB(FAST)n}}{R_{SENSEn}} = \frac{150mV}{R_{SENSEn}} \qquad (9)$$

As a design aid, the currents at which electronic circuit breaker trips for common values for R_{SENSE} are shown in Table 3.

Table 3. $I_{TRIP(SLOW)}$ and $I_{TRIP(FAST)}$ vs R_{SENSE}

R_{SENSE}	$I_{TRIP(SLOW)}$	$I_{TRIP(FAST)}$
0.005Ω	10A	30A
0.006Ω	8.3A	25A
0.007Ω	7.1A	21A
0.008Ω	6.3A	19A
0.009Ω	5.6A	17A
0.01Ω	5A	15A

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4230's V_{CCn} and SENSE*n* pins are strongly recommended. The drawing in Figure 11 illustrates the correct way of making connections between the LTC4230 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

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The power rating of the sense resistor should accommodate steady-state fault current levels so that the component is not damaged before the circuit breaker trips. Table 4 in the Appendix lists suggested sense resistors that can be used with the LTC4230's circuit breaker.

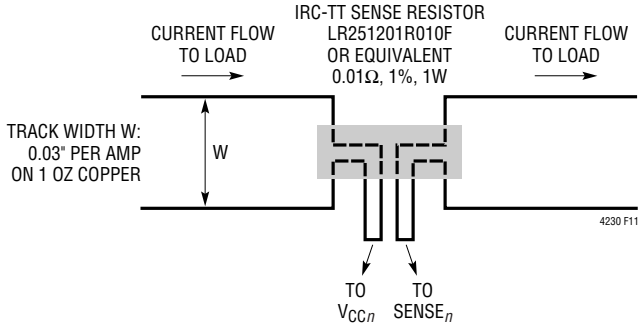

Figure 11. Making PCB Connections to the Sense Resistor

CALCULATING CIRCUIT BREAKER TRIP CURRENT

For a selected R_{SENSE} value, the nominal load current that trips the circuit breaker is given by Equation 10:

$$I_{TRIP(NOM)} = \frac{V_{CB(NOM)}}{R_{SENSE(NOM)}} = \frac{50mV}{R_{SENSE(NOM)}} \quad (10)$$

The minimum load current that trips the circuit breaker is given by Equation 11.

$$I_{TRIP(MIN)} = \frac{V_{CB(MIN)}}{R_{SENSE(MAX)}} = \frac{40mV}{R_{SENSE(MAX)}} \quad (11)$$

where

$$R_{SENSE(MAX)} = R_{SENSE(NOM)} \bullet \left[1+\left(\frac{R_{TOL}}{100}\right)\right]$$

The maximum load current that trips the circuit breaker is given in Equation 12.

$$I_{TRIP(MAX)} = \frac{V_{CB(MAX)}}{R_{SENSE(MIN)}} = \frac{60mV}{R_{SENSE(MIN)}} \quad (12)$$

where

$$R_{SENSE(MIN)} = R_{SENSE(NOM)} \bullet \left[1-\left(\frac{R_{TOL}}{100}\right)\right]$$

For example:

If a sense resistor with 7mΩ ±5% R_{TOL} is used for current limiting, the nominal trip current $I_{TRIP(NOM)}$ = 7.1A. From Equations 11 and 12, $I_{TRIP(MIN)}$ = 5.4A and $I_{TRIP(MAX)}$ = 9A respectively.

For proper operation and to avoid the circuit breaker tripping unnecessarily, the minimum trip current ($I_{TRIP(MIN)}$) must exceed the circuit's maximum operating load current. For reliability purposes, the operation at the maximum trip current ($I_{TRIP(MAX)}$) must be evaluated carefully. If necessary, two resistors with the same R_{TOL} can be connected in parallel to yield an $R_{SENSE(NOM)}$ value that fits the circuit requirements.

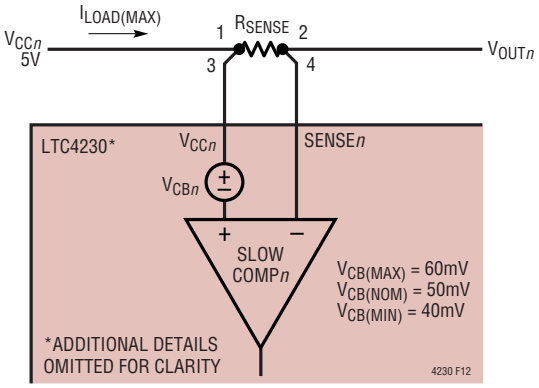

Figure 12. Circuit Breaker Equivalent Circuit for Calculating R_{SENSE}

POWER MOSFET SELECTION CRITERIA

To start the power MOSFET selection process, choose the maximum drain-to-source voltage, $V_{DS(MAX)}$, and the maximum drain current, $I_{D(MAX)}$ of the MOSFET. The $V_{DS(MAX)}$ rating must exceed the maximum input supply voltage (including surges, spikes, ringing, etc.) and the $I_{D(MAX)}$ rating must exceed the maximum short-circuit current in the system during a fault condition. In addition, consider three other key parameters: 1) the required gate-source (V_{GS}) voltage drive, 2) the voltage drop across the drain-to-source ON resistance, $R_{DS(ON)}$ and 3) the maximum junction temperature rating of the MOSFET.

Power MOSFETs are classified into two categories: standard MOSFETs ($R_{DS(ON)}$ specified at V_{GS} = 10V) and logic-level MOSFETs ($R_{DS(ON)}$ specified at V_{GS} = 5V). The absolute

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maximum rating for V_{GS} is typically ±20V for standard MOSFETs. However, the V_{GS} maximum rating for logic-level MOSFETs ranges from ±8V to ±20V depending upon the manufacturer and the specific part number. The LTC4230's gate overdrive as a function of V_{CC} is illustrated in the Typical Performance curves. Logic-level MOSFETs are recommended for low supply voltage applications and standard MOSFETs can be used for applications where supply voltage is greater than 4.75V.

Note that in some applications, the gate of the external MOSFET can discharge faster than the output voltage when the circuit breaker is tripped. This causes a negative V_{GS} voltage on the external MOSFET. Usually, the selected external MOSFET should have a $\pm V_{GS(MAX)}$ rating that is higher than the operating input supply voltage to ensure that the external MOSFET is not destroyed by a negative V_{GS} voltage. In addition, the $\pm V_{GS(MAX)}$ rating of the MOSFET must be higher than the gate overdrive voltage. Lower $\pm V_{GS(MAX)}$ rating MOSFETs can be used with the LTC4230 if the GATE*n* overdrive is clamped to a lower voltage. The circuit in Figure 13 illustrates the use of zener diodes to clamp the LTC4230's GATE*n* overdrive signal if lower voltage MOSFETs are used.

The $R_{DS(ON)}$ of the external pass transistor should be low to make its drain-source voltage (V_{DS}) a small percentage of V_{CC}. At a V_{CC} = 2.5V, $V_{DS} + V_{RSENSE}$ = 0.1V yields 4% error at the output voltage. This restricts the choice of MOSFETs to very low $R_{DS(ON)}$. At higher V_{CC} voltages, the V_{DS} requirement can be relaxed in which case MOSFET package dissipation (P_D and T_J) may limit the value of $R_{DS(ON)}$. Table 5 lists some power MOSFETs that can be used with the LTC4230.

Power MOSFET junction temperature is dependent on four parameters: current delivered to the load, I_{LOAD}, $R_{DS(ON)}$, junction-to-ambient thermal resistance, θ_{JA}, and the maximum ambient temperature to which the circuit will be exposed, $T_{A(MAX)}$. For reliable circuit operation, the maximum junction temperature ($T_{J(MAX)}$) for a power MOSFET should not exceed the manufacturer's recommended value. This includes normal mode operation, start-up, current-limit and autoretry mode in a fault condition. For a given set of conditions, the junction temperature of a power MOSFET is given by Equation 13:

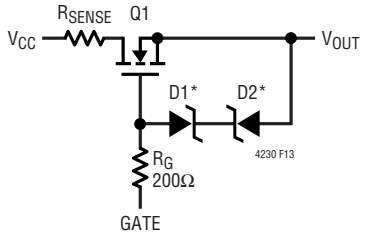
MOSFET Junction Temperature,

$$T_{J(MAX)} \leq (T_{A(MAX)} + \theta_{JA} \bullet P_D) \quad (13)$$

where

$$P_D = (I_{LOAD})^2 \bullet R_{DS(ON)}$$

PCB layout techniques for optimal thermal management of power MOSFET power dissipation help to keep device θ_{JA} as low as possible. See the section on PCB Layout Considerations for more information.



*USER SELECTED VOLTAGE CLAMP
(A LOW BIAS CURRENT ZENER DIODE IS RECOMMENDED)
1N4688 (5V)
1N4692 (7V): LOGIC-LEVEL MOSFET
1N4695 (9V)
1N4702 (15V): STANDARD-LEVEL MOSFET

Figure 13. Optional Gate Clamp for Lower $V_{GS(MAX)}$ MOSFETs

USING STAGGERED PIN CONNECTORS

The LTC4230 can be used on either a printed circuit board or on the backplane side of the connector, and examples for both are shown in Figure 14. Printed circuit board edge connectors with staggered pins are recommended as the insertion and removal of circuit boards do sequence the pin connections. Supply voltage and ground connections on the printed circuit board should be wired to the edge connector's long pins or blades. Control and status signals (like $\overline{\text{RESET}}$*n*, $\overline{\text{FAULT}}$ and ON) passing through the card's edge connector should be wired to short length pins or blades.

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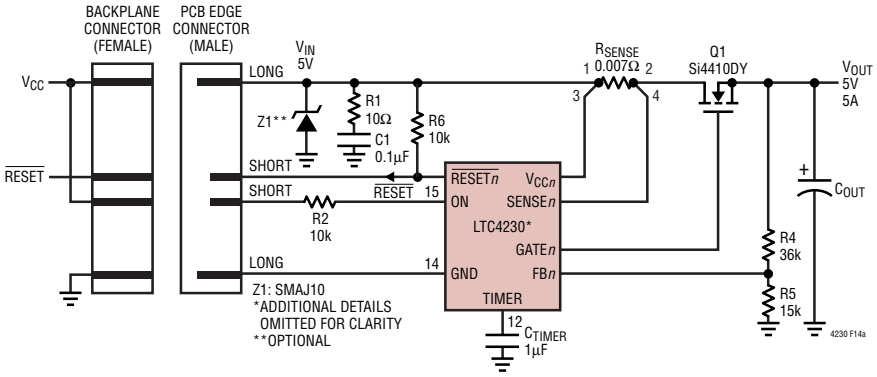
PCB CONNECTION SENSE

There are a number of ways to use the LTC4230's ON pin to detect whether the printed circuit board has been fully seated in the backplane before the LTC4230 commences a start-up cycle.

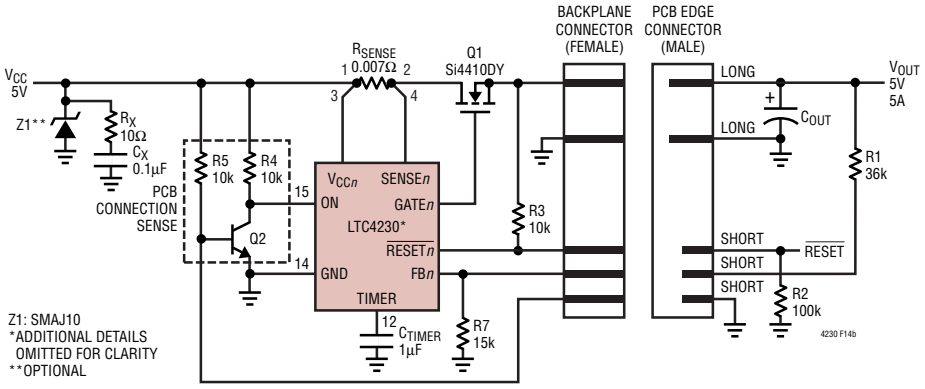
The first example is shown in the schematic on the front page of this data sheet. In this case, the LTC4230 is mounted on the PCB and a 10k resistive divider is connected to the ON pin. On the edge connector, R1 is wired to a short pin. Until the connectors are fully mated, the ON pin is held low, keeping the LTC4230 in an OFF state. Once the connectors are mated, the resistive divider is connected to V_{CC1}, $V_{ON} > 1.314V$ and the LTC4230 begins a start-up cycle.

In Figure 14a, an LTC4230 is illustrated in a basic configuration on a PCB daughter card. The ON pin is connected directly to V_{CC} on the backplane once the card is seated into the backplane. R2 is provided to bleed off any potential static charge which might exist on the backplane, the connector or during card installation.

A third example is shown in Figure 14b where the LTC4230 is mounted on the backplane. In this example, a 2N2222 transistor and a pair of resistors (R4, R5) form the PCB connection sense circuit. With the card out of the chassis, Q2's base is biased to V_{CC} through R5, biasing Q2 on and driving the LTC4230's ON pin low. The base of Q2 is also wired to a socket on the backplane connector. When a card is firmly seated into the backplane, the base of Q2 is then grounded through a short pin connection on the card. Q2 is biased off, the LTC4230's ON pin is pulled-up to V_{CC} and a start-up cycle begins.



(14a) Hot Swap Controller On Daughter Board



(14b) Hot Swap Controller on Backplane

Figure 14. Staggered Pin Connections