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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Multiple Supply Hot Swap Controller with I<sup>2</sup>C Compatible Monitoring

## FEATURES

- Allows Safe Insertion into Live CompactPCI™ or PCI Express™ Backplane
- 8-Bit ADC Monitors Current and Voltage
- I<sup>2</sup>C™/SMBus Interface
- di/dt Controlled Soft Start
- Simultaneous or Sequenced Turn-On
- ±20V Absolute Maximum Rating for ±12V Supplies
- No External Gate Capacitor Required
- Dual-Level Circuit Breaker and Current Limit
- Bus Precharge Output
- Power Good Input with Timeout
- Optional Latchoff or Autoretry After Faults
- Alerts Host After Faults
- Integrated LOCAL\_PCI\_RST# Logic
- 36-Pin SSOP and 38-Pin (5mm × 7mm) QFN Packages

## APPLICATIONS

- Live Board Insertion
- CompactPCI, CompactPCI Express, CompactTCA, PCI Express Systems

## DESCRIPTION

The LTC®4245 Hot Swap™ controller allows a board to be safely inserted and removed from a live backplane in multiple supply systems such as CompactPCI and PCI Express. Using four external N-channel pass transistors, the board supply voltages can be ramped up at an adjustable rate and in any desired sequence. An I<sup>2</sup>C interface and onboard ADC allow monitoring of board current, voltage and fault status for each supply.

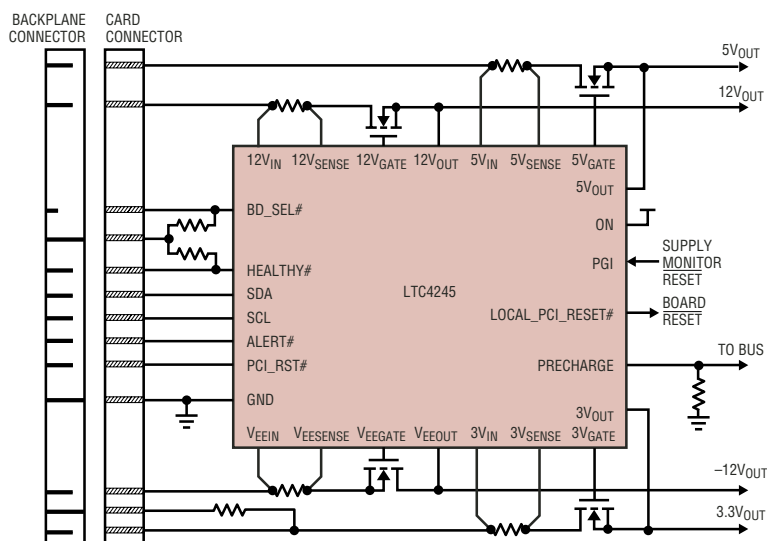
The device features adjustable di/dt controlled soft start and foldback limited inrush current. A dual-level timed circuit breaker and fast current limit protect each supply against overcurrent faults. A power good input with timeout allows a downstream supply monitor to disconnect the board supplies. The device can be configured to function without a -12V supply or with an extra 3.3V supply instead of a 5V supply.

The controller has additional features to interrupt the host when a fault has occurred, notify when output power is good, detect insertion of a load card and power-up in either the on or off state.

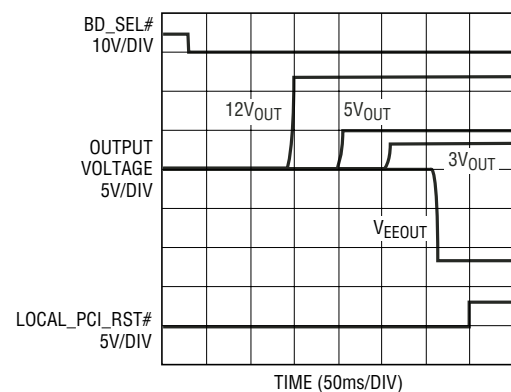
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## TYPICAL APPLICATION

CompactPCI Application



Sequenced Turn-On Waveform



4245 TA01b

# LTC4245

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

### Supply Voltages

12V <sub>IN</sub> .....	-0.3V to 20V
5V <sub>IN</sub> , 3V <sub>IN</sub> .....	-0.3V to 10V
V <sub>EEIN</sub> .....	-20V to 0.3V
INTV <sub>CC</sub> .....	-0.3V to 6.5V

### Input Voltages

BD_SEL#, ON, PGI .....	-0.3V to 12V
ADR0-3, CFG, SS, TIMER .....	-0.3V to INTV <sub>CC</sub> + 0.3V
PCI_RST#, SCL, SDA .....	-0.3V to 6.5V

### Output Voltages

ALERT#, GPIO1-3, HEALTHY#, LOCAL_PCI_RST# .....	-0.3V to 6.5V
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### Analog Voltages (n is 5V, 3V)

12V <sub>GATE</sub> .....	-0.3V to 25V
n <sub>GATE</sub> (Note 3) .....	-0.3V to 12V <sub>IN</sub> + 0.3V or 14V

V <sub>EEGATE</sub> - V <sub>EEIN</sub> (Note 4) .....	-0.3V to 5V
12V <sub>SENSE</sub> .....	-0.3V or 12V <sub>IN</sub> - 6V to 12V <sub>IN</sub> + 0.3V
n <sub>SENSE</sub> .....	-0.3V to n <sub>IN</sub> + 0.3V
V <sub>EESENSE</sub> .....	V <sub>EEIN</sub> - 0.3V to 0.3V
12V <sub>OUT</sub> - 12V <sub>GATE</sub> (Note 4) .....	-5V to 0.3V
n <sub>OUT</sub> - n <sub>GATE</sub> (Note 4) .....	-5V to 0.3V
V <sub>EEOUT</sub> (Note 5) .....	-20V to 0.3V
PRECHARGE .....	-0.3V to 3V <sub>IN</sub> + 0.3V

### Operating Temperature Range

LTC4245C .....	0°C to 70°C
LTC4245I .....	-40°C to 85°C

### Storage Temperature Range

G Package .....	-65°C to 150°C
UHF Package .....	-65°C to 125°C

### Lead Temperature (Soldering, 10 sec)

G Package .....	300°C
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## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>G PACKAGE 36-LEAD PLASTIC SSOP</p> <p>T<sub>JMAX</sub> = 125°C, θ<sub>JA</sub> = 95°C/W</p>	<p>TOP VIEW</p> <p>UHF PACKAGE 38-LEAD (5mm x 7mm) PLASTIC QFN</p> <p>T<sub>JMAX</sub> = 125°C, θ<sub>JA</sub> = 34°C/W EXPOSED PAD (PIN 39) PCB GND CONNECTION OPTIONAL</p>	
<p>ORDER PART NUMBER</p>	<p>ORDER PART NUMBER</p>	<p>UHF PART MARKING*</p>
<p>LTC4245CG LTC4245IG</p>	<p>LTC4245CUHF LTC4245IUHF</p>	<p>4245 4245</p>
<p><b>Order Options</b> Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: <a href="http://www.linear.com/leadfree/">http://www.linear.com/leadfree/</a></p>		

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{12VIN} = 12\text{V}$ ,  $V_{5VIN} = 5\text{V}$ ,  $V_{3VIN} = 3.3\text{V}$ ,  $V_{VEEIN} = -12\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Supplies</b>							
$I_{DD}$	Input Supply Current	$12V_{IN}$	●		3	5	mA
		$5V_{IN}$	●		0.5	1	mA
		$3V_{IN}$ , PRECHARGE Open	●		0.6	1	mA
		$V_{EEIN}$	●		-0.5	-1	mA
$V_{UVL}$	Supply Undervoltage Lockout	$12V_{IN}$	●	10.2	10.5	10.8	V
		$5V_{IN}$ , $V_{CFG} = 0\text{V}$ , Open	●	4.25	4.38	4.5	V
		$5V_{IN}$ When $V_{CFG} = V_{CC}$ , $3V_{IN}$	●	2.7	2.8	2.9	V
		$V_{EEIN}$ , $V_{CFG} = 0\text{V}$ $V_{CC}$ Falling	●	-10.2	-10.5	-10.8	V
$V_{CC}$	Internal Regulator Voltage		●	5	5.5	6	V
<b>Current Limit</b>							
$\Delta V_{SNS(CB)}$	Circuit Breaker Trip Sense Voltage ( $V_{12VIN} - V_{12VSENSE}$ ) ( $V_{5VIN} - V_{5VSENSE}$ ) ( $V_{3VIN} - V_{3VSENSE}$ ) ( $V_{VEESENSE} - V_{VEEIN}$ )	After Start-Up	●	45	50	55	mV
			●	22.5	25	27.5	mV
			●	22.5	25	27.5	mV
			●	40	50	60	mV
$\Delta V_{SNS(ACL)}$	Active Current Limit Sense Voltage ( $V_{12VIN} - V_{12VSENSE}$ ) ( $V_{5VIN} - V_{5VSENSE}$ ) ( $V_{3VIN} - V_{3VSENSE}$ ) ( $V_{VEESENSE} - V_{VEEIN}$ )	After Start-Up	●	130	150	170	mV
			●	60	75	90	mV
			●	60	75	90	mV
			●	130	150	170	mV
$\Delta V_{SNS(FBL)}$ , $\Delta V_{SNS(FBH)}$	Foldback Current Limit Sense Voltage ( $V_{12VIN} - V_{12VSENSE}$ )  ( $V_{5VIN} - V_{5VSENSE}$ )  ( $V_{3VIN} - V_{3VSENSE}$ )  ( $V_{VEESENSE} - V_{VEEIN}$ )	Start-Up, $V_{TIMER} = 0\text{V}$	●	10	15	20	mV
		$V_{12VOUT} = 0\text{V}$	●	40	50	60	mV
		$V_{12VOUT} = 12\text{V}$	●	4	7.5	11	mV
		$V_{5VOUT} = 0\text{V}$	●	22	25	29	mV
		$V_{5VOUT} = 5\text{V}$	●	4	7.5	11	mV
		$V_{3VOUT} = 0\text{V}$	●	22	25	29	mV
	$V_{3VOUT} = 3.3\text{V}$	●	11	16	21	mV	
	$V_{VEEOUT} = 0\text{V}$	●	40	50	60	mV	
	$V_{VEEOUT} = -12\text{V}$	●					
<b>Gate Drive</b>							
$\Delta V_{GATE}$	Gate Drive	Gate to Source	●	5	6.2	7.5	V
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, $\Delta V_{GATE} = 0\text{V}$	●	-16	-20	-24	$\mu\text{A}$
$I_{GATE(DN)}$	Gate Pull-Down Current $12V_{GATE}$ , $5V_{GATE}$ , $3V_{GATE}$ , $V_{EEGATE}$	Gate Drive Off, $\Delta V_{GATE} = 5\text{V}$	●	0.9	1.3	1.7	mA
		$V_{OUT} = V_{IN}$ $V_{VEEGATE} = -7\text{V}$	●	1.7	3.5	5.3	mA
$I_{GATE(FST)}$	Gate Fast Pull-Down Current $12V_{GATE}$ , $5V_{GATE}$ $3V_{GATE}$ $V_{EEGATE}$	Fast Turn Off, $\Delta V_{GATE} = 5\text{V}$	●	125	250	375	mA
		$V_{12VGATE} = 17\text{V}$ , $V_{5VGATE} = 10\text{V}$	●	155	310	465	mA
		$V_{3VGATE} = 8.3\text{V}$ $V_{VEEGATE} = -7\text{V}$	●	32	65	98	mA
<b>Input/Output Pins</b>							
$V_{ON, BD\_SEL\#(TH)}$	ON, $BD\_SEL\#$ Pin Threshold Voltage	$V_{ON}$ Rising, $V_{BD\_SEL\#}$ Rising	●	1.21	1.235	1.26	V
$\Delta V_{ON, BD\_SEL\#(HYST)}$	ON, $BD\_SEL\#$ Pin Hysteresis		●	70	120	170	mV
$I_{BD\_SEL\#(UP)}$	$BD\_SEL\#$ Pull-Up Current	$V_{BD\_SEL\#} = 0\text{V}$	●	-7	-10	-16	$\mu\text{A}$

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{12VIN} = 12\text{V}$ ,  $V_{5VIN} = 5\text{V}$ ,  $V_{3VIN} = 3.3\text{V}$ ,  $V_{VEEIN} = -12\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{PB(TH)}$	Power Bad Threshold Voltage	$12V_{OUT}$	●	10.8	11.1	11.4	V
		$5V_{OUT}$ , $V_{CFG} = 0\text{V}$ , Open	●	4.5	4.63	4.75	V
		$5V_{OUT}$ When $V_{CFG} = V_{CC}$ , $3V_{OUT}$	●	2.8	2.9	3.0	V
		$V_{EEOUT}$ , $V_{CFG} = 0\text{V}$	●	-10.8	-11.1	-11.4	V
$V_{IN(TH)}$	Logic Input Threshold	PGI, PCI_RST#, GPIO $n$	●	0.8	1.0	1.2	V
		SDA, SCL	●	1.6	1.8	2.0	V
$I_{IN}$	Pin Input Current	ON, PGI, PCI_RST#, $V = 1.2\text{V}$ SDA, SCL, ALERT#, GPIO $n$ , HEALTHY#, LOCAL_PCI_RST#, $V = 6\text{V}$	●	0	$\pm 1$	$\mu\text{A}$	
$V_{OL}$	Output Low Voltage	SDA, ALERT#, $I = 5\text{mA}$ ; GPIO $n$ , HEALTHY#, LOCAL_PCI_RST#, $I = 3\text{mA}$	●	0.2	0.4	V	
$V_{TRI(H)}$	ADR2, ADR3, CFG Input High Threshold		●	$V_{CC} - 0.8$	$V_{CC} - 0.4$	$V_{CC} - 0.2$	V
$V_{TRI(L)}$	ADR $n$ , CFG Input Low Threshold		●	0.2	0.4	0.8	V
$I_{TRI(IN,HL)}$	ADR2, ADR3, CFG High, Low Input Current	$V = 0\text{V}$ , $V_{CC}$	●		$\pm 80$	$\mu\text{A}$	
$I_{TRI(IN,Z)}$	ADR2, ADR3, CFG High Z Input Current	$V = 0.8\text{V}$ , $V_{CC} - 0.8\text{V}$	●	$\pm 10$		$\mu\text{A}$	
$I_{ADR01(IN)}$	ADR0, ADR1 Input Current	$V_{ADR0}$ , $V_{ADR1} = 0\text{V}$ , $V_{CC}$	●	-30	1	$\mu\text{A}$	
$I_{SENSE}$	Sense Pin Input Current $12V_{SENSE}$ , $5V_{SENSE}$ , $3V_{SENSE}$ $V_{EESENSE}$	After Start-Up	●	0.3	1	$\mu\text{A}$	
		$V_{SENSE} = V_{IN}$ $V_{VEESENSE} = -12\text{V}$	●	-30	-45	$\mu\text{A}$	
$I_{OUT(ON)}$	OUT Pin Input Current	$V_{12VOUT} = 12\text{V}$ , $V_{ON} = 2\text{V}$	●	200	280	$\mu\text{A}$	
		$V_{5VOUT} = 5\text{V}$ , $V_{ON} = 2\text{V}$	●	275	390	$\mu\text{A}$	
		$V_{3VOUT} = 3.3\text{V}$ , $V_{ON} = 2\text{V}$	●	75	105	$\mu\text{A}$	
		$V_{VEEOUT} = -12\text{V}$ , $V_{ON} = 2\text{V}$	●	-200	-280	$\mu\text{A}$	
$R_{OUT(DIS)}$	OUT Pin Discharge Resistance	$V_{12VOUT} = 6\text{V}$ , $V_{ON} = 0\text{V}$	●	650	1000	1800	$\Omega$
		$V_{5VOUT} = 3\text{V}$ , $V_{ON} = 0\text{V}$	●	125	180	325	$\Omega$
		$V_{3VOUT} = 2\text{V}$ , $V_{ON} = 0\text{V}$	●	130	190	340	$\Omega$
		$V_{VEEOUT} = -6\text{V}$ , $V_{ON} = 0\text{V}$	●	1300	1800	3200	$\Omega$
$I_{VEEOUT(UP)}$	$V_{EEOUT}$ Pull-Up Current	$V_{VEEOUT} = 0\text{V}$	●	-36	-54	$\mu\text{A}$	
$V_{PXG}$	PRECHARGE Voltage	$I_{PRECHARGE} = \text{Open}$ , -70mA (Note 6)	●	0.95	1	1.05	V
<b>Timer, Soft-Start</b>							
$V_{TIMER(H)}$	TIMER Pin High Threshold	$V_{TIMER}$ Rising	●	2.5	2.56	2.62	V
$V_{TIMER(L)}$	TIMER Pin Low Threshold	$V_{TIMER}$ Falling	●	0.1	0.23	0.4	V
$I_{TIMER}$	TIMER Pin Pull-Up Current	During Start-Up, $V_{TIMER} = 0\text{V}$	●	-80	-100	-120	$\mu\text{A}$
		During PGI Timeout, $V_{TIMER} = 0\text{V}$	●	-8	-10	-12	$\mu\text{A}$
		During Auto-Retry, $V_{TIMER} = 0\text{V}$	●	-1.5	-2	-2.5	$\mu\text{A}$
$K_{TMRATIO}$	TIMER Pin Current Ratio	$(I_{TIMER(RTRY)}/I_{TIMER(START)})$	●	1.6	2	2.7	%
$K_{TMCAP}$	Start-Up Time per TIMER Capacitance	$((V_{TIMER(H)} - V_{TIMER(L)})/I_{TIMER(START)})$	●	20	23.3	26	ms/ $\mu\text{F}$
$I_{SS}$	SS Pin Pull-Up Current	Fast Ramp, $V_{SS} = 0\text{V}$	●	-16	-20	-24	$\mu\text{A}$
		Slow Ramp, $V_{SS} = 2\text{V}$	●	-1.5	-2	-2.5	$\mu\text{A}$
$R_{TS(DIS)}$	TIMER, SS Discharge Resistance	$V_{TIMER} = 1.2\text{V}$ , $V_{SS} = 1.2\text{V}$	●	225	400	$\Omega$	
$G_{SS}$	Gain from SS Pin to Foldback Current Limit ( $\Delta V_{SNS(FB)}/\Delta V_{SS}$ )	$12V_{IN}$ , $V_{EEIN}$		46		mV/V	
		$5V_{IN}$ , $3V_{IN}$		23		mV/V	

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{12VIN} = 12\text{V}$ ,  $V_{5VIN} = 5\text{V}$ ,  $V_{3VIN} = 3.3\text{V}$ ,  $V_{VEEIN} = -12\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>ADC</b>							
RES	Resolution (No Missing Codes)	(Note 7)	●	8		Bits	
$V_{FS}$	Full-Scale Voltage ( $V_{FS} = 255\text{LSB}$ ) $12V_{IN}$ , $12V_{OUT}$ $12V_{IN} - 12V_{SENSE}$ , $V_{EESENSE} - V_{EEIN}$ $5V_{IN}$ , $5V_{OUT}$	(Note 6) $V_{CFG} = 0\text{V}$ , Open $V_{CFG} = V_{CC}$	●	13.744	14.025	14.306	V
			●	62.47	63.75	65.03	mV
	●		5.5	5.61	5.72	V	
	●		3.75	3.825	3.9	V	
	●		31.24	31.875	32.51	mV	
	●		3.75	3.825	3.9	V	
	$5V_{IN} - 5V_{SENSE}$ , $3V_{IN} - 3V_{SENSE}$ $3V_{IN}$ , $3V_{OUT}$ $V_{EEIN}$ , $V_{EEOUT}$ GPIO		●	-13.744	-14.025	-14.306	V
			●	2.5	2.55	2.6	V
INL	Integral Nonlinearity	$\Delta V_{SENSE}$ (Note 8) Other 9 Channels	●		$\pm 0.5$	$\pm 2$	LSB
			●		$\pm 0.2$	$\pm 1.25$	LSB
OE	Offset Error	$\Delta V_{SENSE}$ (Note 6) $V_{EEIN}$ , $V_{EEOUT}$ Other 7 Channels	●		$\pm 0.5$	$\pm 1.5$	LSB
			●		$\pm 0.5$	$\pm 1.25$	LSB
			●		$\pm 0.3$	$\pm 1$	LSB
FSE	Full-Scale Error		●		$\pm 5$	LSB	
TUE	Total Unadjusted Error		●		$\pm 5$	LSB	
$t_{ADC}$	Conversion Time	All 13 Channels Once $\Delta V_{SENSE}$ , $V_{EEIN}$ , $V_{EEOUT}$ Other 7 Channels			665		ms
					70		ms
					35		ms
<b>Delays</b>							
$t_D$	Turn-On Delay		●	60	100	150	ms
$t_{PLH(GATE)}$	Input High (ON) to Gates High Delay	SS Open	●		15	30	$\mu\text{s}$
$t_{PHL(GATE)}$	Input High (BD_SEL#), Input Low (ON) to Gates Low Propagation Delay	$C_{GATE} = 1\text{pF}$	●		0.3	1	$\mu\text{s}$
$t_{PHL(UVL)}$	Supply Low to Gates Low Delay	$12V_{IN}$ , $5V_{IN}$ , $3V_{IN}$ , $C_{GATE} = 1\text{pF}$ $V_{EEIN}$ , $C_{VEEGATE} = 1\text{pF}$	●	2.1	3.5	4.9	$\mu\text{s}$
			●	3.3	5.5	7.7	$\mu\text{s}$
$t_{CB}$	Circuit Breaker Filter Delay Time		●	16	22	28	$\mu\text{s}$
$t_{ACL}$	Active Current Limit Delay	$\Delta V_{12VSENSE} = 300\text{mV}$ , $C_{12VGATE} = 10\text{nF}$ $\Delta V_{5VSENSE} = 150\text{mV}$ , $C_{5VGATE} = 10\text{nF}$ $\Delta V_{3VSENSE} = 150\text{mV}$ , $C_{3VGATE} = 10\text{nF}$ $\Delta V_{VEESENSE} = 300\text{mV}$ , $C_{VEEGATE} = 10\text{nF}$	●		0.9	2.3	$\mu\text{s}$
			●		0.85	2.1	$\mu\text{s}$
			●		0.7	1.8	$\mu\text{s}$
			●		2	5	$\mu\text{s}$
$t_{PHL(PGI)}$	PGI Low to Gates Low	$C_{GATE} = 1\text{pF}$	●	12	20	28	$\mu\text{s}$
$t_{PHL(RST)}$	Output Low to LOCAL_PCI_RST# Low	$12V_{OUT}$ , $5V_{OUT}$ , $3V_{OUT}$ , $V_{PCI\_RST\#} = 2\text{V}$ $V_{EEOUT}$ , $V_{PCI\_RST\#} = 2\text{V}$	●	9	15	21	$\mu\text{s}$
			●	10.2	17	23.8	$\mu\text{s}$
$t_{P(RST)}$	PCI_RST# to LOCAL_PCI_RST# Delay		●		60	200	ns
<b>I<sup>2</sup>C Interface Timing (Note 7)</b>							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency	Operates with $f_{SCL} \leq f_{SCL(MAX)}$		400			kHz
$t_{BUF(MIN)}$	Min. Bus Free Time Between Stop/Start			0.12	1.3		$\mu\text{s}$
$t_{SU, STA(MIN)}$	Minimum Repeated Start Set-Up Time			10	600		ns
$t_{HD, STA(MIN)}$	Min. Hold Time After (Repeated) Start			140	600		ns
$t_{SU, STO(MIN)}$	Minimum Stop Condition Set-Up Time			10	600		ns

## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{SU, DAT(MIN)}}$	Minimum Data Set-Up Time Input			0	100	ns
$t_{\text{HD, DAT(MIN)}}$	Minimum Data Hold Time Input			-100	0	ns
$t_{\text{HD, DATO(MIN)}}$	Minimum Data Hold Time Output		300	500	900	ns
$t_{\text{SP(MAX)}}$	Maximum Suppressed Spike Pulse Width		50	110	250	ns
$C_X$	SCL, SDA Input Capacitance			5	10	pF
$t_{\text{of}}$	Data Output Fall Time	(Note 9)	$20 + 0.1C_b$		250	ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

**Note 3:** The  $5V_{\text{GATE}}$  and  $3V_{\text{GATE}}$  pins should not be driven beyond the lower of  $12V_{\text{IN}} + 0.3\text{V}$  and  $14\text{V}$ .

**Note 4:** An internal clamp limits the GATE pins to a minimum of  $5\text{V}$  above  $V_{\text{OUT}}$  ( $V_{\text{EEIN}}$  for  $V_{\text{EEGATE}}$ ). Driving this pin to voltages beyond the clamp may damage the device.

**Note 5:** The device pulls up the  $V_{\text{EEOUT}}$  pin to  $0.6\text{V}$  when pin is in open state.

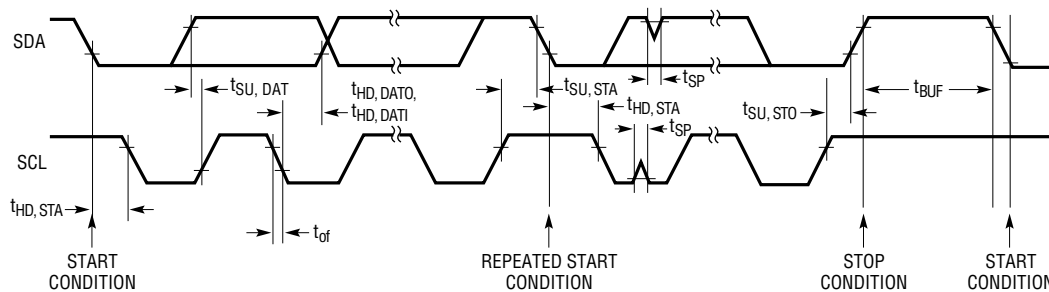
**Note 6:** UHF package specification limits are identical to G package limits and guaranteed by design and by correlation to wafer test measurements.

**Note 7:** Guaranteed by design and not subject to test.

**Note 8:** Integral Nonlinearity is defined as the deviation of a code from a precise analog input voltage. Maximum specifications are limited by the LSB step size and the single shot measurement. Typical specifications are measured from 1/4, 1/2, 3/4 areas of the quantization band.

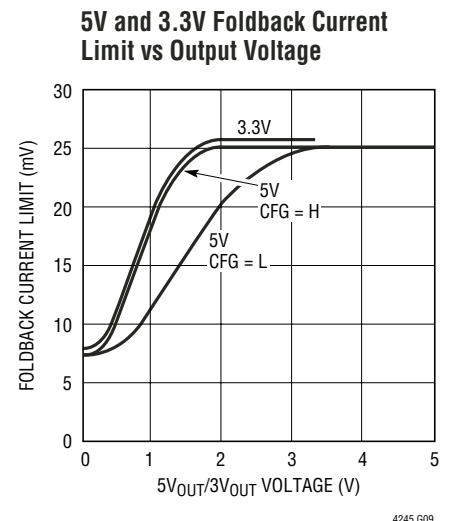
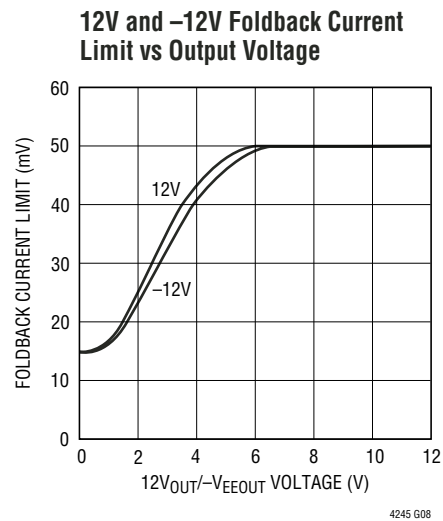
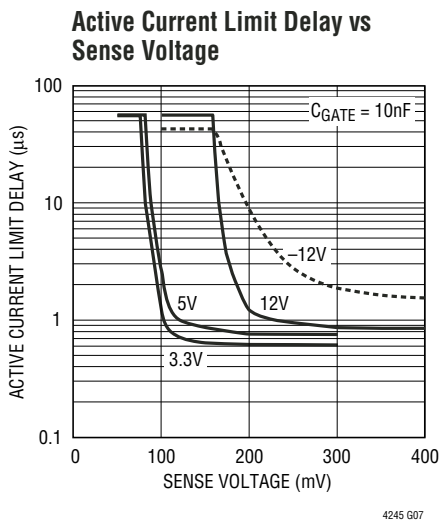
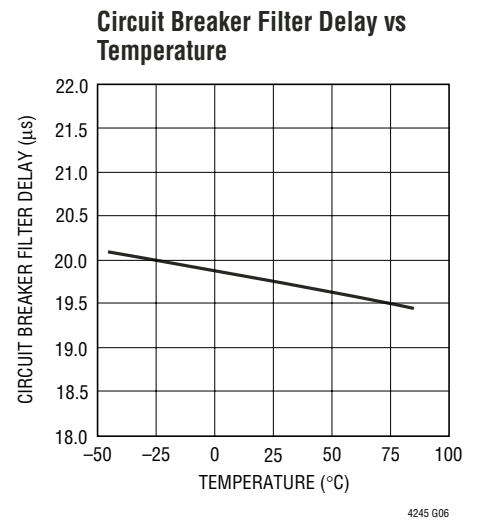
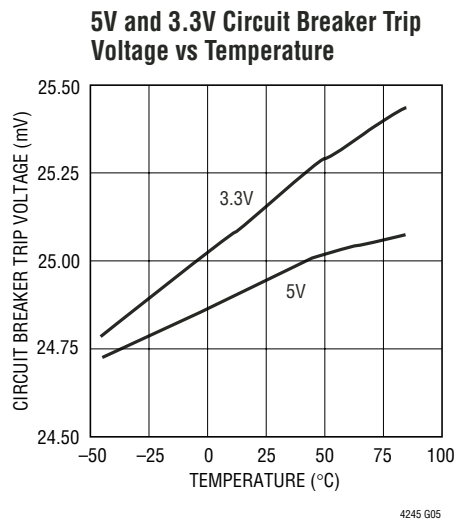
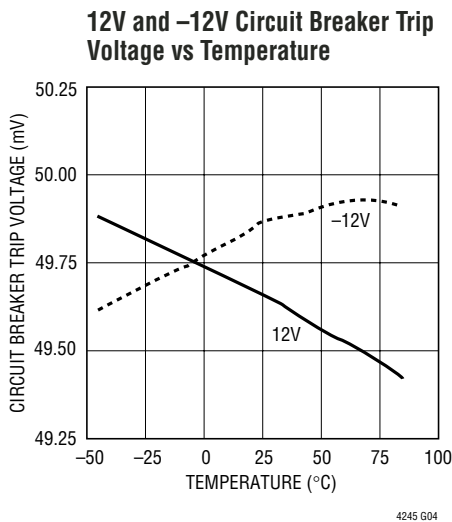
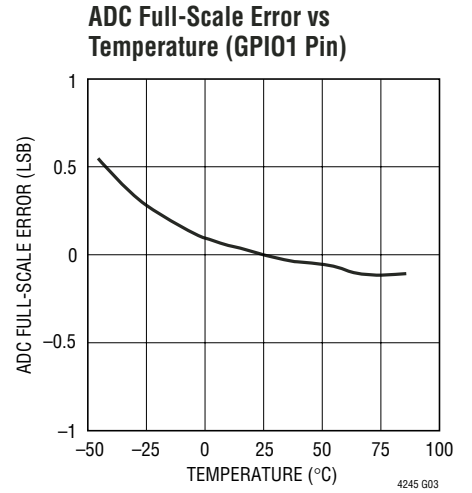
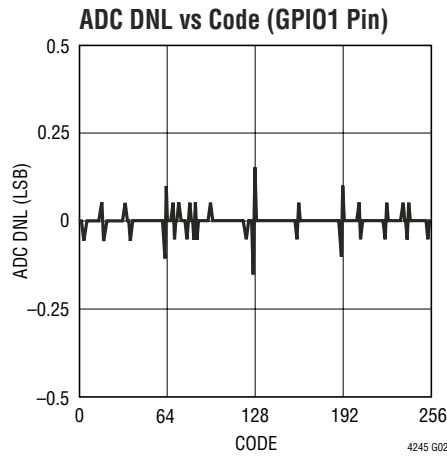
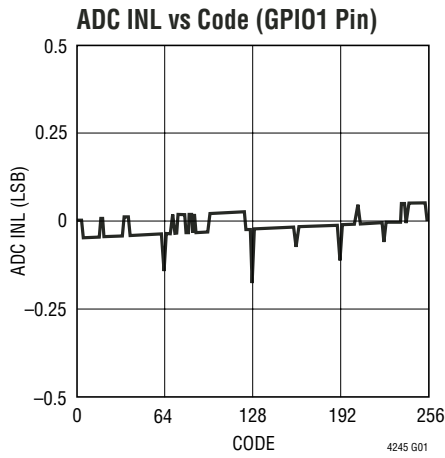
**Note 9:**  $C_b$  = total capacitance of one bus line in pF.

## TIMING DIAGRAM



4245 TD01

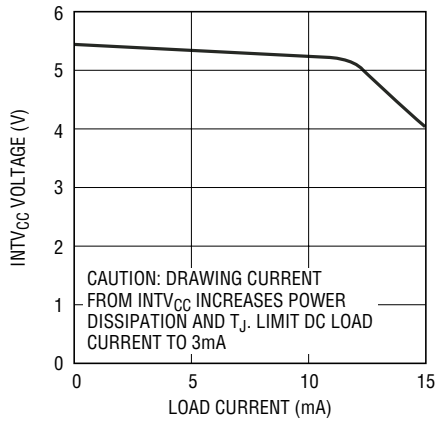
# TYPICAL PERFORMANCE CHARACTERISTICS





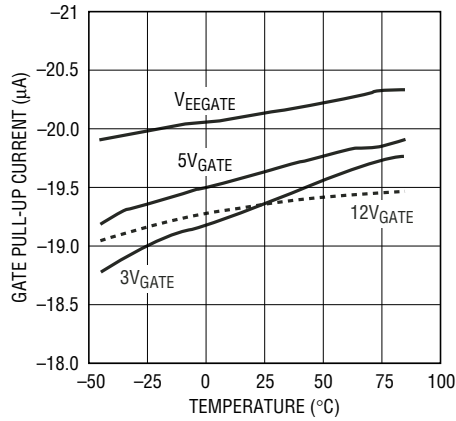
## TYPICAL PERFORMANCE CHARACTERISTICS

**INTV<sub>CC</sub> Voltage vs Load Current**



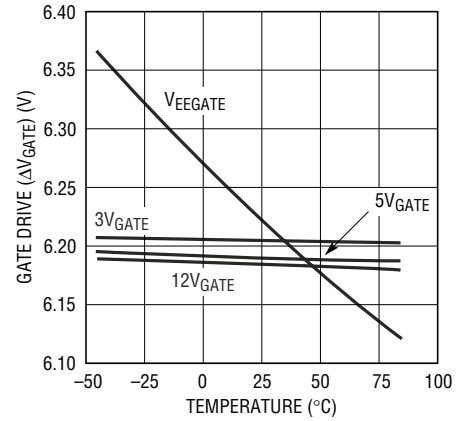
4245 G10

**Gate Pull-Up Current vs Temperature**



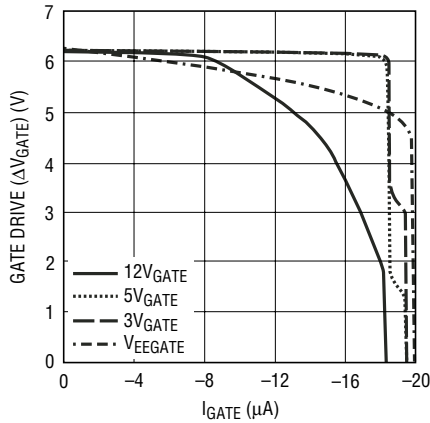
4245 G12

**Gate Drive vs Temperature**



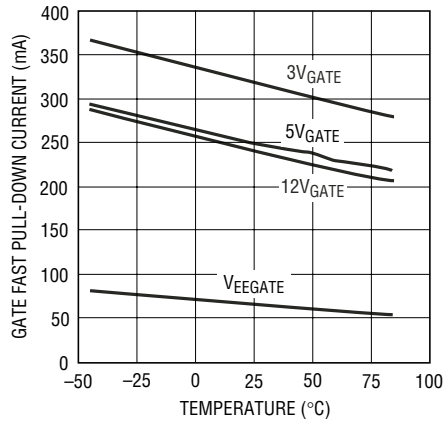
4245 G13

**Gate Drive vs I<sub>GATE</sub>**



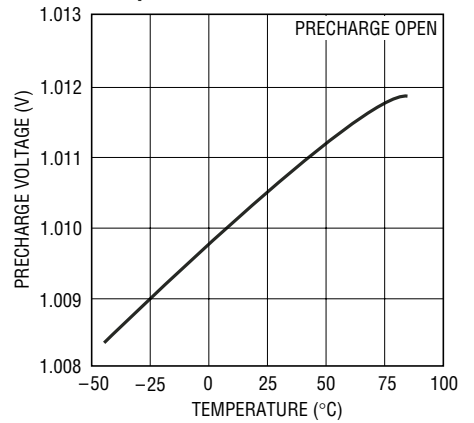
4245 G14

**Gate Fast Pull-Down Current vs Temperature**



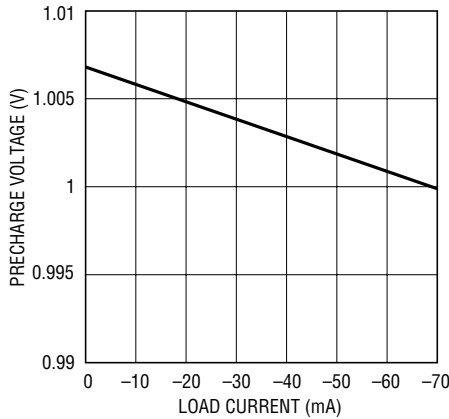
4245 G15

**PRECHARGE Voltage vs Temperature**



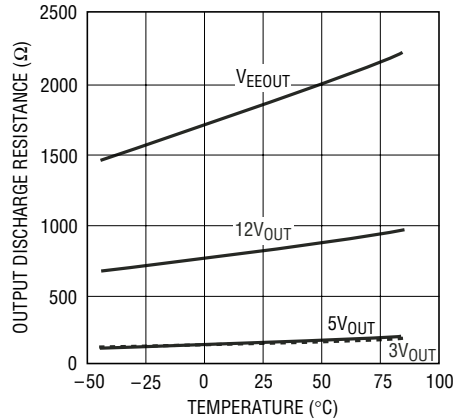
4245 G16

**PRECHARGE Voltage vs Load Current**



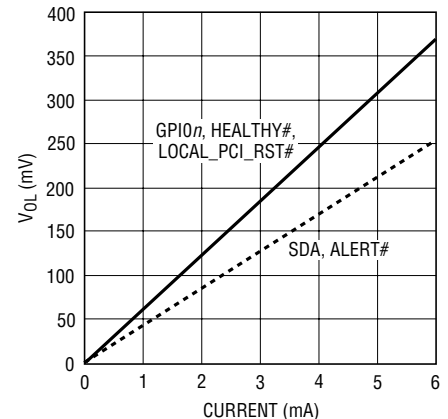
4245 G17

**Output Discharge Resistance vs Temperature**



4245 G18

**V<sub>OL</sub> vs Current**



4245 G21

## PIN FUNCTIONS

**12V<sub>GATE</sub>:** Gate Drive for 12V Supply External N-Channel MOSFET. An internal 20 $\mu$ A current source charges the gate of the external N-channel MOSFET. An internal clamp limits the gate voltage to 6.2V above 12V<sub>OUT</sub>. During turn-off a 1.3mA pull-down current discharges 12V<sub>GATE</sub> to ground. During short-circuit a 250mA pull-down current between 12V<sub>GATE</sub> and 12V<sub>OUT</sub> is activated.

**12V<sub>IN</sub>:** 12V Supply, Current Sense and ADC Input. The internal low voltage supply V<sub>CC</sub> is generated from 12V<sub>IN</sub>. An undervoltage lockout circuit, with 38mV hysteresis, prevents any external MOSFET from turning on when this pin is below 10.5V.

**12V<sub>OUT</sub>:** 12V Gate Drive Return; Foldback, ADC and Power Bad Input. Connect this pin to the source of the 12V supply external N-channel MOSFET switch for gate drive return. Power is considered bad if this pin drops below 11.1V. The comparator on this pin has a built-in hysteresis of 40mV. This pin is also an input to the ADC and the current limit foldback circuit. A 1000 $\Omega$  active pull-down discharges 12V<sub>OUT</sub> to ground when the external MOSFET is turned off.

**12V<sub>SENSE</sub>:** 12V Supply Current Sense and ADC Input. Connect this pin to the output of the 12V current sense resistor. The current limit circuit controls the 12V<sub>GATE</sub> pin to limit the sense voltage between the 12V<sub>IN</sub> and 12V<sub>SENSE</sub> pins to 50mV or less during start-up and 150mV thereafter. During start-up a foldback feature reduces the current limit to 15mV as the 12V<sub>OUT</sub> pin approaches ground. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 50mV for 22 $\mu$ s. To disable current limit, connect this pin to 12V<sub>IN</sub>.

**3V<sub>GATE</sub>:** Gate Drive for 3.3V Supply External N-Channel MOSFET. An internal 20 $\mu$ A current source charges the gate of the external N-channel MOSFET. An internal clamp limits the gate voltage to 6.2V above 3V<sub>OUT</sub>. During turn-off a 1.3mA pull-down current discharges 3V<sub>GATE</sub> to ground. During short-circuit a 310mA pull-down current between 3V<sub>GATE</sub> and 3V<sub>OUT</sub> is activated.

**3V<sub>IN</sub>:** 3.3V Supply, Current Sense and ADC Input. The 1V precharge circuit draws its power and reference voltage from 3V<sub>IN</sub>. An undervoltage lockout circuit, with 10mV hysteresis, prevents any external MOSFET from turning on when this pin is below 2.8V.

**3V<sub>OUT</sub>:** 3.3V Gate Drive Return; Foldback, ADC and Power Bad Input. Connect this pin to the source of the 3.3V supply external N-channel MOSFET switch for gate drive return. Power is considered bad if this pin drops below 2.9V. The comparator on this pin has a built-in hysteresis of 11mV. This pin is also an input to the ADC and the current limit foldback circuit. A 190 $\Omega$  active pull-down discharges 3V<sub>OUT</sub> to ground when the external MOSFET is turned off.

**3V<sub>SENSE</sub>:** 3.3V Supply Current Sense and ADC Input. Connect this pin to the output of the 3.3V current sense resistor. The current limit circuit controls the 3V<sub>GATE</sub> pin to limit the sense voltage between the 3V<sub>IN</sub> and 3V<sub>SENSE</sub> pins to 25mV or less during start-up and 75mV thereafter. During start-up a foldback feature reduces the current limit to 7.5mV as the 3V<sub>OUT</sub> pin approaches ground. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 25mV for 22 $\mu$ s. To disable current limit, connect this pin to 3V<sub>IN</sub>.

**5V<sub>GATE</sub>:** Gate Drive for 5V Supply External N-Channel MOSFET. An internal 20 $\mu$ A current source charges the gate of the external N-channel MOSFET. An internal clamp limits the gate voltage to 6.2V above 5V<sub>OUT</sub>. During turn-off a 1.3mA pull-down current discharges 5V<sub>GATE</sub> to ground. During short-circuit a 250mA pull-down current between 5V<sub>GATE</sub> and 5V<sub>OUT</sub> is activated.

**5V<sub>IN</sub>:** 5V Supply, Current Sense and ADC Input. An undervoltage lockout circuit, with 16mV or 10mV of hysteresis, prevents any external MOSFET from turning on when this pin is below 4.38V or 2.8V depending on the state of the CFG pin.

## PIN FUNCTIONS

**5V<sub>OUT</sub>**: 5V Gate Drive Return; Foldback, ADC and Power Bad Input. Connect this pin to the source of the 5V supply external N-channel MOSFET switch for gate drive return. Power is considered bad if this pin drops below 4.63V or 2.9V depending on the CFG pin. The comparator on this pin has a built-in hysteresis of 17mV or 11mV. This pin is also an input to the ADC and the current limit foldback circuit. A 180Ω active pull-down discharges 5V<sub>OUT</sub> to ground when the external MOSFET is turned off.

**5V<sub>SENSE</sub>**: 5V Supply Current Sense and ADC Input. Connect this pin to the output of the 5V current sense resistor. The current limit circuit controls the 5V<sub>GATE</sub> pin to limit the sense voltage between the 5V<sub>IN</sub> and 5V<sub>SENSE</sub> pins to 25mV or less during start-up and 75mV thereafter. During start-up a foldback feature reduces the current limit to 7.5mV as the 5V<sub>OUT</sub> pin approaches ground. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 25mV for 22μs. To disable current limit, connect this pin to 5V<sub>IN</sub>.

**ADR0 to ADR3**: Serial Bus Address Inputs. ADR0 and ADR1 are two-state inputs; ADR2 and ADR3 are three-state inputs. Tying these pins to ground, open or INTV<sub>CC</sub> configures one of 32 possible addresses. The addressing scheme is compatible with the CompactPCI geographic addressing for slot identification. See Table 5 in Applications Information.

**ALERT#**: Fault Alert Output. Open-drain logic output that can be pulled to ground, when a fault occurs, to alert the host controller. A fault alert is enabled by the ALERT register. This device is compatible with SMBus alert protocol. See Applications Information. Tie to ground if unused.

**BD\_SEL#**: Board Present Input. Ground this pin to enable the N-channel MOSFETs to turn on. When this pin is high, the MOSFETs are off. An internal 10μA current source pulls up this pin to INTV<sub>CC</sub>. Transitions on this pin will be recorded in the FAULT2 register. A high-to-low transition activates the logic to read the state of the ON pin and clear faults. See Applications Information.

**CFG**: Supply Configuration Three-State Input. When this pin is grounded, all four supply inputs must satisfy their undervoltage lockout levels to allow the external MOSFETs

to turn on. Floating this pin disables V<sub>EE</sub> undervoltage lockout and power bad functions, allowing other supplies to turn-on even when –12V supply is absent. Tying this pin to INTV<sub>CC</sub> not only disables V<sub>EE</sub>, but also converts the 5V<sub>IN</sub> undervoltage, power bad and ADC levels to 3.3V levels. This allows using an extra 3.3V supply instead of a 5V supply as in a PCI Express application.

**EXPOSED PAD (Pin 39, UHF Package)**: Exposed Pad may be left open or connected to device ground.

**GND**: Device Ground.

**GPIO1 to GPIO3 (GPIO2, GPIO3 on UHF package only)**: General Purpose Input/Output and ADC Input. Open-drain logic outputs and logic inputs. Any one of the three pins can be multiplexed to the GPIO channel of the internal ADC. GPIO1 has a state change fault associated with it. The GPIO register (Table 13) contains status and control bits for these pins.

**HEALTHY#**: Board Power Status Output. This pin is pulled low by an open-drain output when all supply outputs are above their power bad thresholds and when all external N-channel MOSFETs are on. When any supply output falls below its power bad threshold voltage, this pin will go high after a 15μs deglitching time.

**INTV<sub>CC</sub>**: Internal Low Voltage Supply Decoupling Output. Connect a 0.1μF capacitor from this pin to ground. When this pin falls below 3.8V, the internal registers are reset.

**LOCAL\_PCI\_RST#**: Reset Output. This pin is pulled low by an open-drain output whenever HEALTHY# is high or when the PCI\_RST# input is low. Tie to ground if unused.

**ON**: On Control Input. A rising edge turns on the external N-channel MOSFETs and a falling edge turns them off. This pin is also used to configure the state of the FET On control bits (and hence the external FETs) in the ON register. For example, if the ON pin is tied high, then one or all (depending on the Sequence control bit) FET On control bits will go high 100ms after power-up. Likewise if the ON pin is tied low then the part will remain off after power-up until the FET On control bits are set high using the I<sup>2</sup>C bus. If the Sequence control bit is set, taking ON pin high turns on the supplies in a 12V, 5V, 3.3V, –12V sequence. A high-to-low transition on this pin will clear faults.

## PIN FUNCTIONS

**PCI\_RST#:** Reset Input. Pulling this pin low causes LOCAL\_PCI\_RST# to pull low. When high, LOCAL\_PCI\_RST# is the logical inverse of HEALTHY#. Tie to INTV<sub>CC</sub> if unused.

**PGI:** Power Good Input. Tie this pin to the  $\overline{\text{RESET}}$  output of an external supply monitor or power good output of a DC/DC converter. When all supplies have been turned on, a timing cycle is started at the end of which the PGI pin is sampled. If it is low, all external MOSFETs are shut off. If the PGI Disable control bit C3 is not set, pulling this pin low for more than 20 $\mu$ s during normal operation will also shut off all MOSFETs. Tie to INTV<sub>CC</sub> if unused.

**PRECHARGE:** Bus Precharge Output. This pin can source 70mA at 1V as soon as 3V<sub>IN</sub> is powered-up. Leave it open if unused.

**SCL:** Serial Bus Clock Input. Data at the SDA pin is shifted in or out on rising edges of SCL. This is a high impedance pin that is generally driven by an open-collector output from a master controller.

**SDA:** Serial Bus Data Input and Output. This is a high impedance input when address, command or data bits are shifted in. It is an open-drain output when sending data back to the master controller or acknowledging a write operation. An external pull-up resistor or current source is required.

**SS:** Soft-Start Input. Connect a capacitor between this pin and ground to set the rate of increase of current limit during start-up for di/dt limited inrush current. When an external MOSFET is turned on, a 20 $\mu$ A pull-up current charges the capacitor. The voltage ramp on the capacitor is converted into an internal current limit increasing linearly with time. Leave it open if di/dt limited inrush is not required.

**TIMER:** Timer Input. A capacitor between this pin and ground sets the duration of the start-up, PGI and auto-retry timing cycles to be 23.3ms/ $\mu$ F, 233ms/ $\mu$ F and 1.17s/ $\mu$ F respectively. A timing cycle consists of TIMER being charged to 2.56V with an internal pull-up current source and then being reset by a switch to ground. The timing cycle ends when TIMER falls below 0.23V. The start-up, PGI and auto-retry timing cycles use 100 $\mu$ A, 10 $\mu$ A and 2 $\mu$ A pull-up current sources respectively.

**V<sub>EEGATE</sub>:** Gate Drive for -12V Supply External N-Channel MOSFET. An internal 20 $\mu$ A current source charges the gate of the external N-channel MOSFET. An internal clamp limits the gate voltage to 6.2V above V<sub>EEIN</sub>. During turn-off, a 3.5mA pull-down current discharges V<sub>EEGATE</sub> to V<sub>EEIN</sub>. During short-circuit a 65mA pull-down current between V<sub>EEGATE</sub> and V<sub>EEIN</sub> is activated. If a -12V supply is not available, connect V<sub>EEGATE</sub> to ground and use the CFG pin appropriately.

**V<sub>EEIN</sub>:** -12V Supply, Current Sense and ADC Input. An undervoltage lockout circuit, with 38mV hysteresis, prevents any external MOSFET from turning on when this pin is above -10.5V. The V<sub>EEIN</sub> undervoltage lockout can be disabled by using the CFG pin. If a -12V supply is not available, connect V<sub>EEIN</sub> to ground and use the CFG pin appropriately.

**V<sub>EEOUT</sub>:** -12V Supply Foldback, ADC and Power Bad Input. Connect this pin to the drain of the -12V supply external N-channel MOSFET switch. Power is considered bad if this pin rises above -11.1V. The comparator on this pin has a built-in hysteresis of 54mV. The V<sub>EEOUT</sub> power bad function can be disabled by using the CFG pin. This pin is also an input to the ADC and the current limit foldback circuit. A 1800 $\Omega$  active pull-up discharges V<sub>EEOUT</sub> to ground when the external MOSFET is turned off. If a -12V supply is not available, connect V<sub>EEOUT</sub> to ground and use the CFG pin appropriately.

**V<sub>EESENSE</sub>:** -12V Supply Current Sense and ADC Input. Connect this pin to the output of the -12V current sense resistor. The current limit circuit controls the V<sub>EEGATE</sub> pin to limit the sense voltage between the V<sub>EESENSE</sub> and V<sub>EEIN</sub> pins to 50mV or less during start-up and 150mV thereafter. During start-up a foldback feature lowers the current limit to 16mV as the V<sub>EEOUT</sub> pin approaches ground. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 50mV for 22 $\mu$ s. To disable current limit, connect this pin to V<sub>EEIN</sub>. If a -12V supply is not available, connect V<sub>EESENSE</sub> to ground and use the CFG pin appropriately.



## OPERATION

### Start-Up

The LTC4245 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane slot. When a supply turn-on command is received, current sources start pulling up the TIMER and SS pins. The  $100\mu\text{A}$   $I_{\text{TM}}R$  current and the external TIMER capacitor determine the time a supply can be in current limit during start-up. The gate of a supply's external N-channel MOSFET is servoed by an amplifier ( $\text{ACL}_n$ ) so that the current, as indicated by the sense resistor voltage drop, never exceeds an internal current limit. This current limit rises at a rate determined by  $I_{\text{SS}}$  and the capacitor at the SS pin. A foldback circuit determines the maximum value of the current limit and reduces it to 30% of the maximum when a supply's output is shorted to ground. When the TIMER pin crosses 2.56V it is reset to ground and the start-up timing cycle ends. If a supply is still in current limit all gates are turned off, an overcurrent fault is logged and the TIMER goes through a cool-down timing cycle using  $2\mu\text{A}$  for  $I_{\text{TM}}R$ . Otherwise, its circuit breaker ( $\text{ECB}_n$ ) is armed and the current limit is raised to 3 times the circuit breaker threshold. The SS pin is then reset by switch M2.

Any combination of the four supplies can be turned on together or one after another. Whenever a supply is ramping up, its output voltage will affect, through the foldback circuit, where the internal current limit ramp stops. The default configuration turns on all supplies together. If sequence control bit C6 (Table 9) is set, the supplies turn on in a 12V, 5V, 3.3V, -12V sequence. With this bit set, the end of a supply ramp-up triggers the start of the next one in the sequence. The I<sup>2</sup>C interface allows independent on and off control for each supply through its On control bit. Turn-off is simultaneous under fault conditions and when using the ON or BD\_SEL# pins.

At the end of the last start-up timing cycle, HEALTHY# is pulled low by M3 if all supply outputs are above their power bad thresholds. LOCAL\_PCI\_RST# which was held low (M4), now follows PCI\_RST#. The TIMER pin goes through a PGI timeout cycle using  $10\mu\text{A}$  for  $I_{\text{TM}}R$ . The PGI pin is sampled at the end of the cycle. If it is low, then all external MOSFETs are shut-off, a PGI fault is logged and TIMER goes through a cool-down cycle using  $2\mu\text{A}$

for  $I_{\text{TM}}R$ . If PGI is high, the part enters the normal mode of operation.

### Normal Operation

During normal operation, the gates of the MOSFETs are clamped about 6.2V above their sources. The 12V gate driver uses a charge pump, the 5V and 3.3V gate drive is derived from  $12V_{\text{IN}}$  and the -12V gate drive from  $\text{INTV}_{\text{CC}}$ . Each supply is continuously monitored for undervoltage, overcurrent and power bad conditions. Overcurrent monitoring consists of an electronic circuit breaker comparator ( $\text{ECB}_n$ ) and an active current limit circuit ( $\text{ACL}_n$ ) set at 3x the ECB threshold. Undervoltage and overcurrent faults cause all MOSFETs to be shut off. A power bad condition causes HEALTHY# to go high impedance and LOCAL\_PCI\_RST# to pull low, without shutting off the MOSFETs. If the PGI pin is not disabled (register bit C3 not set), then PGI pin going low will also shut off all MOSFETs.

### ADC

Included in the LTC4245 is an 8-bit A/D converter. The converter has a 13-input multiplexer to select between input, output and current sense voltage of each supply, and the GPIO channel. The ADC can either cycle through all channels or measure a channel on-demand.

### Serial Interface

An I<sup>2</sup>C interface is provided to read from or write to the status, control and A/D registers. It allows the host to poll the device and determine if faults have occurred. If the ALERT# line is used as an interrupt, the host can respond to a fault in real time. The LTC4245 I<sup>2</sup>C interface slave address is decoded using the ADR0 to ADR3 pins.

### Configuration, GPIO and Precharge

The three-state CFG pin can be used to disable the  $V_{\text{EE}}$  undervoltage lockout, power bad and foldback functions. It can also convert the 5V undervoltage, power bad and ADC levels to 3.3V levels. The GPIO1 to GPIO3 pins can be used as general purpose inputs or outputs (M5 to M7). One of the pins can also be multiplexed to the GPIO channel of the ADC. A 1V reference voltage derived from  $3V_{\text{IN}}$  is provided at the PRECHARGE pin. This can be used to pre-charge I/O lines on the board so as not to corrupt the backplane bus.

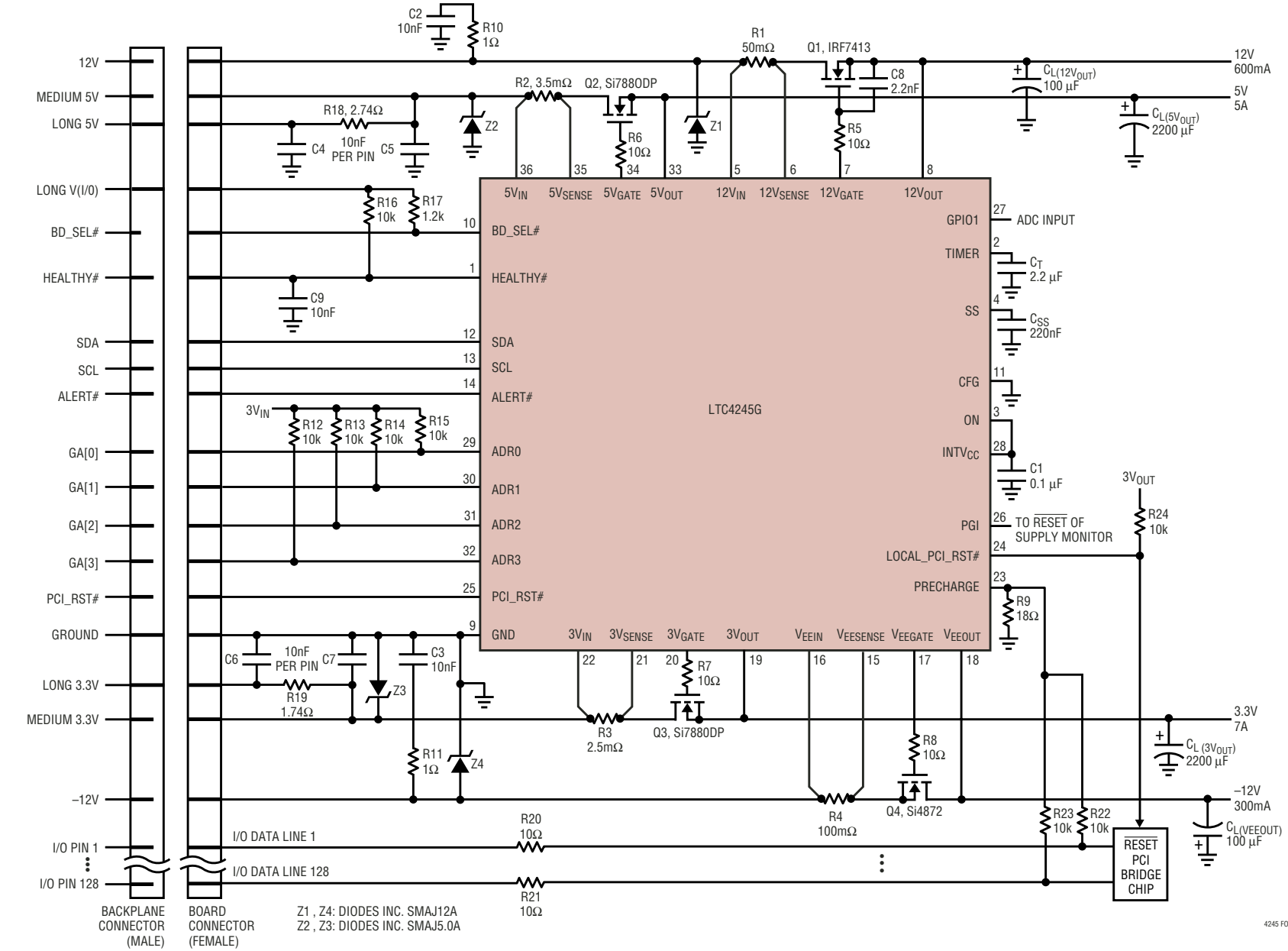


Figure 1. CompactPCI Application

4245 F01

## APPLICATIONS INFORMATION

The typical LTC4245 application is in a high availability system where boards using multiple supplies are hot plugged. The device enables the system to periodically monitor board power consumption and fault status over the I<sup>2</sup>C interface. Boards in CompactPCI and PCI Express systems typically utilize three to four supplies. Figure 1 shows the LTC4245 being used in a CompactPCI application.

The following sections describe the turn on, turn off and fault response behavior of the LTC4245. The ADC and I<sup>2</sup>C interface are discussed next. External component selection is discussed in detail in the Design Example section.

### CPCI Connection Pin Sequence

The staggered lengths of the CPCI male connector pins on the backplane ensures that all power supplies are physically connected to the LTC4245 before back-end power is allowed to ramp up (BD\_SEL# asserted low). The long pins, which include 5V, 3.3V, V(I/O) and GND, mate first. The short BD\_SEL# pin mates last. At least one long 3.3V power pin must be connected to the LTC4245 in order for the PRECHARGE pin voltage to be available before the CPCI bus pins mate.

The following is a typical hot plug sequence.

1. ESD clips make contact.
2. Long power and ground pins make contact and Early Power is established. The 1V precharge voltage becomes valid at this stage. Power is also applied to the pull-up resistors connected to the HEALTHY# and BD\_SEL# signals. LOCAL\_PCI\_RST# is held in reset. All power switches are held off at this stage of insertion.
3. Medium length pins make contact. The 12V and -12V connector pins make contact at this stage. The internal low voltage supply of the LTC4245 (INTV<sub>CC</sub>) powers up from the 12V supply. An internal 10μA pull-up from INTV<sub>CC</sub> to BD\_SEL# turns on. Other connector pins that mate are HEALTHY#, PCI\_RST# and the bus I/O pins (which are precharged to 1V).
4. Short pins make contact. If the BD\_SEL# signal is grounded on the backplane, the plug-in board power-up cycle may begin immediately. If the ON pin

is tied high then turn-on is automatic, else the LTC4245 waits for a serial bus turn-on command. System backplanes that do not ground the BD\_SEL# signal will instead have circuitry that detects when BD\_SEL# makes contact with the plug-in board. The system logic can then control the power up process by pulling BD\_SEL# low. The precharge potential may be optionally disconnected from the CPCI bus signals at this stage.

### Turn-On

The back-end power planes are isolated from the input power planes by external N-channel pass transistors Q1 through Q4. Sense resistors R1 to R4 provide current fault detection. Resistors R5 to R8 prevent high frequency oscillations in MOSFETs Q1 to Q4 respectively.

The following conditions must be satisfied for a duration of 100ms before the external switches can be turned on.

1. All input supplies and the internally generated supply, INTV<sub>CC</sub>, must exceed their undervoltage lockout thresholds. The V<sub>EE</sub> undervoltage lockout can be disabled by not tying the CFG pin low.
2. No undervoltage, overcurrent or PGI fault bits must be set unless the corresponding auto-retry is enabled. When 12V<sub>IN</sub> powers up for the first time, INTV<sub>CC</sub> rises above its undervoltage threshold which generates a 60μs to 120μs internal power-on-reset pulse. During reset, the fault registers are cleared and the control bits are initialized. If INTV<sub>CC</sub> is already up, then the I<sup>2</sup>C interface can be used to clear the fault bits or set the auto-retry bits.
3. The BD\_SEL# pin must be pulled low.

When these initial conditions are satisfied, the ON pin is checked. If it is high, the four FET On control bits (D0 to D3) are set either simultaneously (the default state) or in a 12V, 5V, 3.3V, -12V sequence (register bit C6 set). If ON is low, the external switches turn on when the ON pin is brought high or if a serial bus turn-on command is received. Figure 2 shows all supplies turning on after BD\_SEL# goes low.





## APPLICATIONS INFORMATION

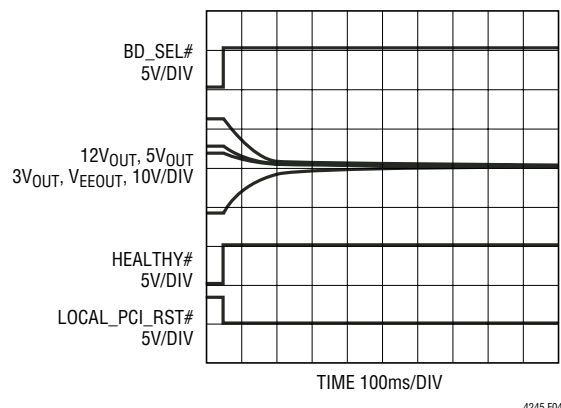


Figure 4. Normal Turn-Off Waveform

### Turn-Off

The switches can be turned off by a variety of conditions.

1. ON pin going low or BD\_SEL# going high turns off all switches.
2. Individual switches can be turned off by resetting the particular FET On control bit (D0 to D3) through the serial bus.
3. A variety of fault conditions will turn off all switches together. These include supply undervoltage, overcurrent circuit breaker and PGI faults.
4. Writing a logic one into the undervoltage, overcurrent or PGI fault bits will turn off all switches, if the corresponding autoretry is not enabled.

Normally the 12V, 5V and 3.3V switches are turned off with a 1.3mA current pulling down the gate to ground.  $V_{EEGATE}$  is pulled through a resistive switch to  $V_{EEIN}$ . All supply outputs are also discharged to ground through internal switches. When any MOSFET is shut off, the HEALTHY# signal pulls high and LOCAL\_PCI\_RST# will be asserted low. Figure 4 shows all supplies being turned off by BD\_SEL# going high.

### ON Register and Sequencing

The LTC4245 features an ON register (Table 10) consisting of four On control bits (D0 to D3) and four On status bits (D4 to D7). D0 to D3 provide independent on/off control for each supply through the I<sup>2</sup>C bus. Bits D4 to D7 report

the on status of each supply. Even though a supply may be commanded to turn-on by setting its On control bit, it may remain off (On status bit low) because the conditions to turn on, as listed in the Turn-On section, may not be present.

The sequence control bit, C6, determines whether the four supply MOSFETs turn-on together or in a fixed sequence. The default state is no sequencing. In this case taking the ON pin high sets all the four On control bits. If the start-up conditions are satisfied, all switches will turn on under the control of a single TIMER and SS cycle. Due to different input voltage offsets in the current limit amplifier of each supply, the gate turn-on of all MOSFETs will not occur at the same moment but will happen in random order depending on amplifier offset and soft-start ramp rate. The gate turn-ons will be truly simultaneous only if SS pin is left open.

If bit C6 is set, then the ON pin going high sets only the 12V On control bit, D0. The 12V back-end supply ramps up. The end of the TIMER and SS cycle sets the 5V On control bit, D1, starting the ramp of the 5V supply output. The end of the 5V timing cycle sets bit D2 and the end of the 3.3V ramp sets bit D3. In this way, the four On control

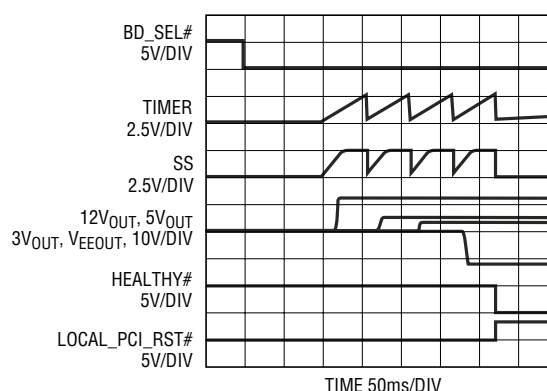


Figure 5. Sequential Turn-On Waveform

bits get set one after another, leading to a 12V, 5V, 3.3V, –12V start-up sequence. Figure 5 illustrates this. If C6 is set and any of the start-up conditions goes bad, all switches turn-off, and all On control bits except D0 are reset. This ensures that the part goes through a sequenced turn-on during auto-retry. D1 to D3 are also reset when BD\_SEL# goes low with C6 set.

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When the sequence bit C6 is set, setting the On control bit of a supply, through the I<sup>2</sup>C interface, starts the supply turn-on sequence from that supply onwards. For example, setting bit D1 will turn-on 5V, 3.3V, –12V supplies, in that order. A logic one can then be written to bit D0 to ramp the 12V supply. At the end of this ramp-up, bit D1 is set. But since 5V is already powered-up, the sequence stops there.

The I<sup>2</sup>C interface provides the most flexibility in turning supplies on and off. With bit C6 cleared, any supply or supplies can be turned on by setting their On control bits. The On control bits cannot be set when any supply is ramping (therefore using TIMER and SS pins). The SS busy bit, A1, indicates this blanking period. The On control bits can be reset though, even when a supply is ramping. Two or more On control bits may be set at the same time to ramp multiple supplies in the same timing cycle. When all supplies are turned on the LTC4245 goes through the PGI timing cycle.

### Supply Voltage Configuration

The CFG pin enables the LTC4245 to be used in non-CPCI applications. It is a three-state input pin. In a CPCI application with all four supplies, the CFG pin is tied to ground.

Floating the CFG pin disables the V<sub>EE</sub> undervoltage lockout (UVLO), start-up foldback and power bad functions. It also makes the ±12V turn-ons coincident by using the 12V FET On control bit, D0, to control the –12V supply MOSFET. This allows the three positive supplies to power-up and HEALTHY# to assert, even when a negative supply is either unavailable or does not meet the required thresholds. If unused the V<sub>EEIN</sub>, V<sub>EESENSE</sub>, V<sub>EEGATE</sub> and V<sub>EEOUT</sub> pins should be tied to ground. Since the circuit breaker and active current limit circuits are not disabled, a lower negative supply could be hot plugged. It would turn on whenever the 12V supply turns on. Care should be taken that the supply does not collapse under overcurrent conditions. At low supplies, the ECB and ACL circuits stop functioning. With the UVLO already disabled, the LTC4245 may not detect a fault condition on the V<sub>EE</sub> supply. Large currents, limited only by MOSFET and sense resistances, could flow, potentially damaging the board traces and connector pins.

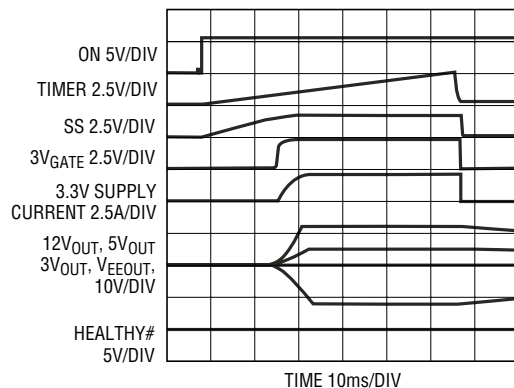
If the CFG pin is tied high, the 5V supply thresholds change to 3.3V levels, while keeping the floating state functionality. The 5V supply UVLO, power bad thresholds and foldback profile become similar to those of the 3.3V supply. The 5V<sub>IN</sub> and 5V<sub>OUT</sub> inputs to the ADC use the same LSB and full-scale as the 3V<sub>IN</sub> and 3V<sub>OUT</sub> pins. This allows the use of an extra 3.3V supply instead of a 5V supply as in a PCI Express application.

### Overcurrent Fault

The LTC4245 has different current limiting behavior during start-up, when supply ramps up under TIMER and SS control, and normal operation. As such it can generate an overcurrent fault during both phases of operation. Both set the faulting supply's overcurrent fault bit (bits E4 to E7) and shut off all external FETs.

During start-up when both TIMER and SS are ramping, the current limit is a function of SS pin voltage and the ramping supplies' output voltages. A supply could power up entirely in current limit depending on the bypass capacitor at the outputs of the ramping supplies. The TIMER pin sets the time duration for current limit during start-up. This time involves the TIMER charging up to 2.56V with a 100μA current source and then resetting to 0.23V with a switch. At the end of the timing cycle if the supply is still in current limit, i.e., the gate of it's external MOSFET is still being actively controlled, an overcurrent fault is declared for that supply and all MOSFETs are shut off (Figure 6). Therefore the maximum time a supply can stay in current limit at start-up is given by:

$$t_{\text{START}} = C_T \cdot K_{\text{TMCAP}} = C_T \cdot 23.3 \text{ [ms / } \mu\text{F]} \quad (4)$$



4245 F06

Figure 6. Start-Up Into a Short on 3.3V Output

4245fa

## APPLICATIONS INFORMATION

After the switches are turned off, the TIMER pin begins charging up with a  $2\mu\text{A}$  pull-up current. When it reaches  $2.56\text{V}$  it is reset to ground with a switch. During this cool-down cycle, the overcurrent fault bit cannot be reset. After this cycle, the switches will be allowed to turn on again if the overcurrent fault bit is cleared. However, if the overcurrent autoretry bit, C1, has been set then the switches turn on again automatically after the  $100\text{ms}$  turn-on delay (without resetting the overcurrent fault).

After start-up, a supply has dual-level glitch-tolerant protection against overcurrent faults. The sense resistor voltage drop is monitored by an electronic circuit breaker (ECB) and an active current limit (ACL). In the event that a supply's current exceeds the ECB threshold, an internal timer is started. If the supply is still overcurrent after  $22\mu\text{s}$ , the ECB trips and all supplies are turned off (Figure 7). An analog current limit loop prevents the supply current from exceeding  $3\times$  the ECB threshold in the event of a short circuit (Figure 8). The  $22\mu\text{s}$  filter delay and the higher ACL threshold prevents unnecessary resets of the board due to minor current surges. The LTC4245 will stay in the latched off state unless bit C1 is set, in which case the switches turn on after a  $100\text{ms}$  delay. Note that foldback is not active after start-up.

### Undervoltage Fault

An undervoltage fault occurs when any of the input supplies falls below its undervoltage threshold for more than  $3.5\mu\text{s}$  ( $5.5\mu\text{s}$  for  $V_{\text{EEIN}}$ ). This turns off all switches immediately and sets the undervoltage present bit A0 and the corresponding undervoltage fault bit (bits E0 to E3).

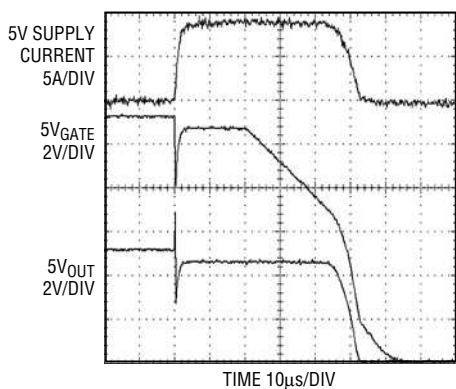


Figure 7. Overcurrent Fault on 5V Output

If the supply subsequently rises above the threshold for  $100\text{ms}$ , the switches will turn on again unless the undervoltage auto-retry has been disabled by clearing bit C0. When power is first applied to the device, if any supply is below its threshold after  $\text{INTV}_{\text{CC}}$  crosses its undervoltage lockout threshold, an undervoltage fault will be logged in the FAULT1 register.

### PGI Fault

The PGI pin can be used to shut off the board's input supplies in case downstream supplies fail to enter regulation in time. It can be tied to the reset output of a monitor IC or the powergood pin of a DC/DC converter.

After all supply outputs have been powered up, a timing cycle is started with a  $10\mu\text{A}$  current pulling up the TIMER pin. When TIMER reaches  $2.56\text{V}$  it is reset to ground by a switch. As TIMER falls below  $0.23\text{V}$ , the PGI pin is sampled. If it is low, the PGI fault bit F4 is set and all external FETs are shut off. A cool-down timing cycle is started using a  $2\mu\text{A}$  pull-up current on TIMER pin. Bit F4 cannot be reset during this time. After this cycle, the switches will be allowed to turn on again if the PGI fault bit is cleared. However, if the PGI autoretry bit, C4, has been set then the switches turn on again automatically after the  $100\text{ms}$  turn-on delay.

By default, the PGI pin is ignored during normal operation. It can be enabled by clearing PGI disable bit C3. Now, if PGI pin goes low for more than  $20\mu\text{s}$ , all FETs will be shut off. If bit C4 is set, the switches will turn on after the  $100\text{ms}$  turn-on delay.

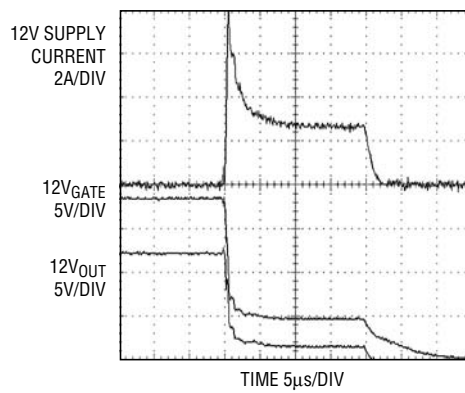


Figure 8. Short-Circuit Fault on 12V Output

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### Power Bad Fault

A power bad condition exists when any supply output drops below its power bad threshold for more than 15 $\mu$ s (17 $\mu$ s for  $V_{EEOUT}$ ). This sets bit A2 in the STATUS register. The HEALTHY# output goes high impedance, and LOCAL\_PCI\_RST# pin is pulled low. If the gate of the supply's MOSFET is enhanced, a power bad fault is logged in bits F0 to F3 of the FAULT2 register. A circuit will prevent power bad fault bits being set if the external MOSFET gate-to-source voltage is low, eliminating false power bad faults during power-up or power-down. If the supply output subsequently rises back above the threshold, bit A2 will be cleared, HEALTHY# will pull low and LOCAL\_PCI\_RST# will follow PCI\_RST#.

### BD\_SEL# Change of State

Whenever the BD\_SEL# pin toggles, bit F6 is set to indicate a change of state. When the BD\_SEL# pin goes high, indicating board removal, all switches turn off immediately. Bit A6 reports the current state of this pin. If the BD\_SEL# pin is pulled low, indicating a board insertion, all fault bits except F6 will be cleared. If the sequence bit C6 is set, then On control bits D1 to D3 are also cleared. If the BD\_SEL# pin remains low for 100ms the state of the ON pin will be captured in either D0 to D3 or only D0, depending on sequence bit C6. This turns on the switches if ON pin is tied high. There is an internal 10 $\mu$ A pull-up current source on the BD\_SEL# pin from INTV<sub>CC</sub>.

If the system shuts down due to a fault, it may be desirable to restart the system simply by removing and reinserting a load card. In cases where the LTC4245 and the switches reside on a backplane or midplane (as in a PCI Express application) and the load resides on a plug-in card, the BD\_SEL# pin can be used to detect when the plug-in card is removed (see Figure 9). Once the plug-in card is reinserted the two fault registers are cleared (except for F6). After 100ms the state of ON pin is latched into bits D0 to D3. At this point the system will start up again.

If a connection sense on the plug-in card is driving the BD\_SEL# pin, the insertion or removal of the card may cause the pin voltage to bounce. This will result in clearing the fault register when the card is removed. The pin

can be debounced using a filter capacitor,  $C_{BD\_SEL\#}$ , on the BD\_SEL# pin as shown in Figure 9. The filter time is given by:

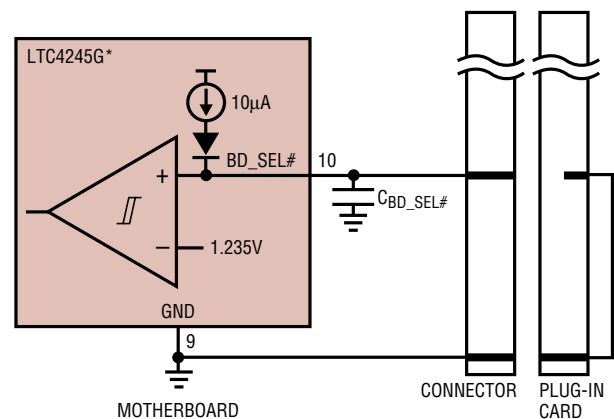
$$t_{\text{FILTER}} = C_{\text{BD\_SEL\#}} \cdot 123 \text{ [ms / } \mu\text{F]} \quad (5)$$

### FET Short Fault

A FET short fault will be reported if the data converter measures a supply's current sense voltage greater than 7 LSB while the supply's pass transistor is turned off. This condition sets the FET short present bit, A5, and the FET short fault bit F5. Reading the On status bits (D4 to D7) and the ADC current sense voltage data registers (J, M, P, S) can help debug which supply's MOSFET might be potentially shorted. A false FET short fault might be reported if an input supply power-up is delayed by more than 500ms after INTV<sub>CC</sub> is up.

### Fault Alerts

When any of the bits in fault registers E and F are set, an optional bus alert can be generated by setting the appropriate bit in the ALERT register B. This allows only selected faults to generate alerts. At power-up the default state is not to alert on faults. If an alert is enabled, the corresponding fault will cause the ALERT# pin to pull low. See the Alert Response Protocol section for more information.



\*ADDITIONAL DETAILS OMITTED FOR CLARITY

4245 F09

Figure 9. Plug-In Card Insertion/Removal

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### Resetting Faults

The two fault registers E and F can be reset in any of the following ways:

1. Writing zeros to the registers using the I<sup>2</sup>C bus.
2. Taking the ON pin high to low resets both registers.
3. INTV<sub>CC</sub> falling below its undervoltage lockout threshold.
4. Bringing BD\_SEL# from high to low clears all fault bits except bit F6. Bit F6, which indicates a BD\_SEL# change of state, will be set.

Note that faults that are still present cannot be cleared. Overcurrent and PGI faults are continuously set during their cool-down timing cycles and hence cannot be reset for that duration. The fault registers will not be cleared when auto-retrying. When autoretry is disabled the existence of an undervoltage (E0 to E3), overcurrent (E4 to E7) or PGI (F4) fault keeps the switches off. As soon as the fault is cleared, the switches will turn on.

### Precharge

The PRECHARGE pin provides a 1V voltage (using a divided down 3V<sub>IN</sub> as the reference) that is used to bias the CPCI bus connector pins during board insertion and extraction. The pin can source 70mA without losing regulation. An external 18Ω resistor from this pin to ground provides the current sink capability. At least one long 3.3V connector pin must be connected to 3V<sub>IN</sub> to provide early power to the precharge circuit.

Resistors are used to connect the 1V bias voltage to the CPCI bus signals. For 5V signaling this resistance must be greater than 10kΩ - 5% (Figure 1). For 3.3V signaling if the leakage current on the I/O line is greater than 2μA, the precharge resistors need to be disconnected during normal operation. Figure 10 shows a circuit that uses a bus switch to accomplish this. The connection is made when the voltage on the BD\_SEL# pin is pulled up to 5V, which occurs just after the long pins have made contact. The resistors are disconnected when the short BD\_SEL# connector pin makes contact and the BD\_SEL# voltage drops below 4.4V thus causing  $\overline{\text{OE}}$  to be pulled high by

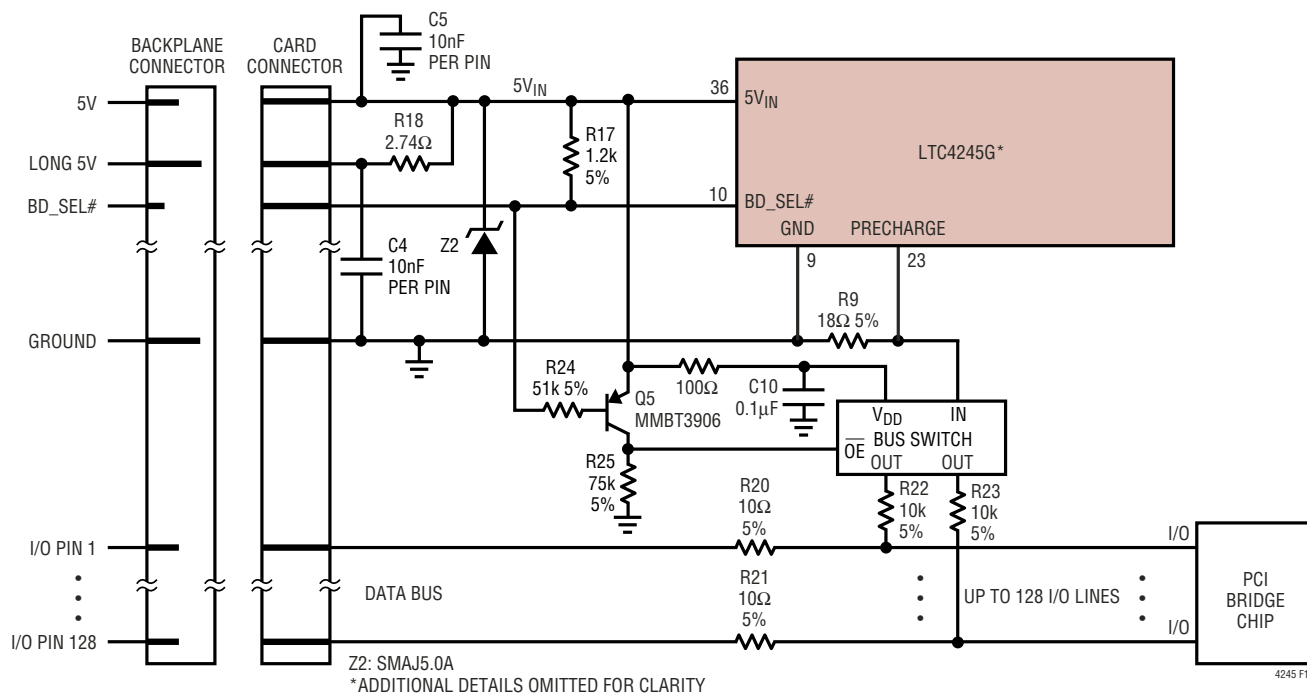


Figure 10. Precharge Bus Switch Application Circuit for 3.3V and Universal Hot Swap Boards

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Q5. The CPCI specification assumes that there is a diode to 3.3V on the circuit that is driving the BD\_SEL# pin. If the BD\_SEL# pin is being driven high, the actual voltage on the pin will fall to approximately 3.9V from 5V. This is still above the threshold of the LTC4245 BD\_SEL# pin, but low enough for Q5 to pull  $\overline{OE}$  high. Since the bus switch is powered off an early power plane, a 100 $\Omega$  resistor should be placed in series with its  $V_{DD}$ .

When the plug-in card is removed from the backplane, the BD\_SEL# connection is broken first, and the BD\_SEL# voltage pulls up to 5V. This causes Q5 to turn off, which re-enables the bus switch, and the precharge resistors are again connected to the PRECHARGE pin for the remainder of the extraction process.

### Data Converter

The LTC4245 incorporates an 8-bit data converter that continuously converts thirteen different channels. Twelve of these channels are used for each supply's input, current sense and output voltages. One of the three GPIO pins can be multiplexed to the thirteenth channel using bits G6 and G7. The results from each conversion are stored in registers I through U and are updated once every 665ms. Since the ADC is powered off  $INTV_{CC}$ , which is derived from  $12V_{IN}$ , it is not possible to convert  $12V_{IN}$  below about 8V as the ADC and serial bus are held in reset.

The ADC can also measure a particular channel on-demand. First the ADC needs to be taken out of its free-running mode by setting control bit C7. The ADC enters a quiescent state, which is indicated by the ADC busy bit, A7, going to logic zero. Writing the address of a channel to ADCADR register triggers the start of one conversion of that channel's voltage. Bit A7 goes high to indicate ADC activity. It goes low again after the ADC finishes the conversion and writes the result to the channel's data register. The same or different address can be written again to start a new conversion. The quiescent state of the ADC can also be used to read and write from the ADC data registers for software testing purposes. Resetting bit C7 allows the ADC to again start cycling through the thirteen channels starting with the first one.

### Digital Interface

The LTC4245 communicates with a bus master using a 2-wire interface compatible with the I<sup>2</sup>C bus and the SMBus, an I<sup>2</sup>C extension for low power devices.

The LTC4245 is a read-write slave device and supports SMBus Read Byte, Write Byte, Read Word and Write Word commands. The second word in a Read Word command will be identical to the first word. The second word in a Write Word command is ignored. The data formats for these commands are shown in Figures 12 to 15.

### START and STOP Conditions

When the bus is idle, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

### I<sup>2</sup>C Device Addressing

Thirty-two distinct bus addresses are configurable using the two-state ADRO, ADR1 pins and the three-state ADR2, ADR3 pins. Table 5 shows the correspondence between pin states and addresses. Note that address bits B7 and B6 are internally configured to (01)b. The first 16 addresses are compatible with the geographic addressing scheme used in CompactPCI to encode physical slot addresses. In addition, the LTC4245 will respond to two special addresses. Address (0010 111)b is a mass write address used to write to all LTC4245, regardless of their individual address settings. The mass write can be masked by setting register bit C5 to zero. Address (0001 100)b is the SMBus Alert Response Address. If the LTC4245 is pulling low on the ALERT# pin, it will acknowledge this address using the SMBus Alert Response Protocol.

### Acknowledge

The acknowledge signal is used for handshaking between the transmitter and the receiver to indicate that the last byte of data was received. The transmitter always releases the

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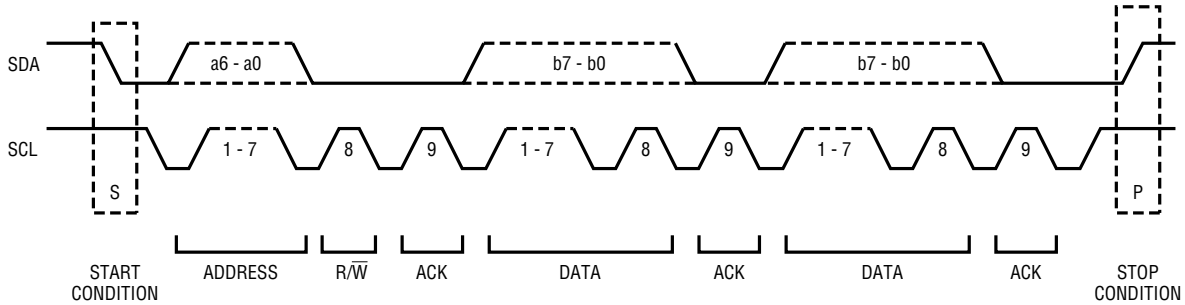
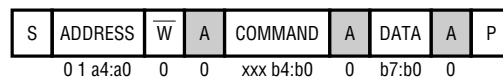


Figure 11. Data Transfer over I<sup>2</sup>C or SMBus

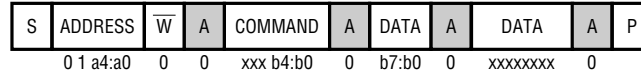
4245 F11



- FROM MASTER TO SLAVE
- FROM SLAVE TO MASTER
- A : ACKNOWLEDGE (LOW)
- $\overline{A}$  : NOT ACKNOWLEDGE (HIGH)
- R : READ BIT (HIGH)
- $\overline{W}$  : WRITE BIT (LOW)
- S : START CONDITION
- P : STOP CONDITION

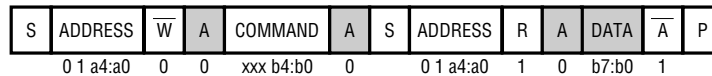
4245 F12

Figure 12. LTC4245 Serial Bus SDA Write Byte Protocol



4245 F13

Figure 13. LTC4245 Serial Bus SDA Write Word Protocol



4245 F14

Figure 14. LTC4245 Serial Bus SDA Read Byte Protocol

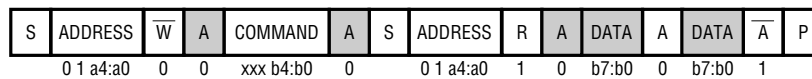
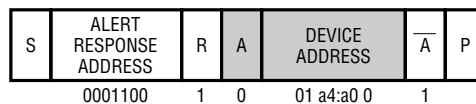


Figure 15. LTC4245 Serial Bus SDA Read Word Protocol



4245 F16

Figure 16. LTC4245 Serial Bus SDA Alert Response Protocol



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SDA line during the acknowledge clock pulse. When the slave is the receiver, it must pull down the SDA line so that it remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA HIGH, then the master can abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master must pull down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received, the master will leave the SDA line HIGH (not acknowledge) and issue a STOP condition to terminate the transmission.

### Write Protocol

The master begins communication with a START condition followed by the seven bit slave address and the  $\overline{R/W}$  bit set to zero. The addressed LTC4245 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to write. The LTC4245 acknowledges this and then latches the lower five bits of the command byte into its internal Register Address Pointer. The master then delivers the data byte and the LTC4245 acknowledges once more and latches the data into its internal register. The transmission is ended when the master sends a STOP condition. If the master continues sending a second data byte, as in a Write Word command, the second data byte will be acknowledged by the LTC4245 but ignored.

### Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address and the  $\overline{R/W}$  bit set to zero. The addressed LTC4245 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to read. The LTC4245 acknowledges this and then latches the lower five bits of the command byte into its internal Register Address Pointer. The master then sends a repeated START condition followed by the same seven bit address with the  $\overline{R/W}$  bit now set to one. The LTC4245 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, as in a Read Word command, the LTC4245 will repeat the requested register as the second data byte.

Note that the Register Address Pointer is not cleared at the end of the transaction. Thus the Receive Byte protocol can be used to repeatedly read a specific register.

### Alert Response Protocol

The LTC4245 implements the SMBus Alert Response Protocol as shown in Figure 16. If enabled to do so through the ALERT register B, the LTC4245 will respond to faults by pulling the ALERT# pin low. Multiple LTC4245s can share a common ALERT# line and the protocol allows a master to determine which LTC4245s are pulling the line low. The master begins by sending a START bit followed by the special Alert Response Address (0001 100)<sub>b</sub> with the  $\overline{R/W}$  bit set to one. Any LTC4245 that is pulling its ALERT# pin low will acknowledge and begin sending back its individual slave address.

An arbitration scheme ensures that the LTC4245 with the lowest address will have priority; all others will abort their response. The successful responder will then release its ALERT# pin while any others will continue to hold their ALERT# pins low. Polling may also be used to search for any LTC4245 that have detected faults. Any LTC4245 pulling its ALERT# pin low will have bit B3 in the ALERT register set. Writing a zero to this bit will release the ALERT# pin.

The ALERT# signal will not be pulled low again until the FAULT1 or FAULT2 register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate alerts until the associated fault register bit has been cleared. Also, a fault on one supply will not generate an alert if a fault bit of the same kind (undervoltage, overcurrent, power bad) is set for any other supply.

### General Purpose Input/Outputs (GPIOs)

The G36 package of the LTC4245 has one GPIO (GPIO1) pin while the UHF package has three (GPIO1 to GPIO3). Bits G0 to G2 in the GPIO register (Table 13) indicate whether a pin is above or below the 1V threshold voltage. Bits G3 to G5 control whether the open-drain output on a GPIO pin pulls low or is high impedance. This can be used to drive external pull-up resistors or LEDs. Register bits G6 and G7 control which one of the three pins is multiplexed to the GPIO channel of the ADC. Whenever the GPIO1 pin

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toggles, bit F7 is set to indicate a change of state. If the GPIO1 alert bit B7 is enabled, this feature can be used to alert the host system to a change in state of the board's ejector handles.

### Compensating the Active Current Loop

The four active current limit circuits of the LTC4245 are compensated internally and therefore do not require any RC network on the gate pins. The internal compensation should work for most pass transistors. If the gate capacitance is very small then the best method to compensate the loop is to add a 1nF to 5nF capacitor between the gate and source of the external MOSFET.

### Supply Collapse During Transients

The LTC4245 is designed to ride through supply transients caused by load steps. If there is a shorted load and the parasitic inductance back to the supply is significant, there is a chance that the supply could collapse before the active current limit circuit brings down the gate of the external MOSFET. In this case the undervoltage lockout circuit, which has a 3.5 $\mu$ s (5.5 $\mu$ s for  $V_{EEIN}$ ) filter time, turns off the pass transistors.

### Input Overvoltage Transient Protection

Hot-plugging a board into a backplane generates inrush currents from the backplane power supplies due to the charging of the plug-in board capacitance. To reduce this transient current to a safe level, the CPCI Hot Swap specification restricts the amount of unswitched capacitance used on the input side of the plug-in board. Each medium or long power pin connected to the CPCI female connector on the plug-in board is required to have a 10nF ceramic bypass capacitor to ground. Bulk capacitors are allowed on the switched output side of the LTC4245. Some bulk capacitance is allowed on the Early Power planes, but only because a current limiting resistor is assumed to decouple the connector pin from the bulk capacitance (e.g., see 100 $\Omega$  to Bus Switch  $V_{DD}$  in Figure 10).

Disallowing bulk capacitors on the input power pins tends to create a resonant circuit formed by the inductance of the backplane power supply trace and the parasitic capacitance of the plug-in board (mainly due to the large power

MOSFET). Upon board insertion, the ringing of this circuit can exhibit a peak overshoot of 2.5 times the steady-state voltage (>30V for 12V<sub>IN</sub>).

There are two methods for abating the effects of these high voltage transients: using voltage limiters to clip the transient to a safe level and snubber networks. Snubber networks are series RC networks whose time constants are experimentally determined based on the board's parasitic resonance circuits. As a starting point, the capacitors in these networks are chosen to be 10 $\times$  to 100 $\times$  the power MOSFET's  $C_{OSS}$  under bias. The series resistor is a value determined experimentally that ranges from 1 $\Omega$  to 50 $\Omega$ , depending on the parasitic resonance circuit. Note that in all LTC4245 circuit schematics, both transient voltage limiters and snubber networks have been added to the 12V<sub>IN</sub> and  $V_{EEIN}$  supply rails and should always be used. Snubber networks are not necessary on the 3V<sub>IN</sub> or the 5V<sub>IN</sub> supply lines since their absolute maximum ratings are 10V. Transient voltage limiters, however, are recommended as these devices provide large-scale transient protection for the LTC4245 in the event of abrupt changes in supply current. All protection networks should be mounted very close to the LTC4245's supply pins using short lead lengths to minimize the trace resistance and inductance. A recommended layout of the 5V and 12V transient protection devices around the LTC4245 is shown in Figure 18.

### Design Example

As a design example, consider a Hot Swap application with the following power supply requirements:

**Table 1. Example Power Supply Requirements**

VOLTAGE SUPPLY	MAXIMUM LOAD CURRENT	MAXIMUM INRUSH di/dt	LOAD CAPACITANCE
12V	600mA	150mA/ms	100 $\mu$ F
5V	5A	1.5A/ms	2200 $\mu$ F
3.3V	7A	1.5A/ms	2200 $\mu$ F
-12V	300mA	150mA/ms	100 $\mu$ F

1. Select the appropriate values of  $R_{SENSE}$  for the supplies. Calculating the value of  $R_{SENSE}$  is based on  $I_{LOAD(MAX)}$  and the lower limit for the circuit breaker threshold voltage,  $\Delta V_{SNS(CB)(MIN)}$ . If a 1% tolerance is assumed for the sense resistors, then the following values of resistances should suffice: