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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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High Power PD With Synchronous No-Opto Flyback Controller

FEATURES

- **Robust 35W PD Front End**
- **IEEE 802.3af Compliant**
- **Rugged 750mA Power MOSFET With Precision Dual Level Current Limit**
- **High Performance Synchronous Flyback Controller**
- **IEEE Isolation Obtained Without an Opto-Isolator**
- **Adjustable Frequency from 50kHz to 250kHz**
- **Tight Multi-Output Regulation With Load Compensation**
- Onboard 25k Signature Resistor
- Programmable Classification Current to 75mA
- Complete Thermal and Over-Current Protection
- Available in Compact 32-Pin 7mm × 4mm DFN Package

APPLICATIONS

- VoIP Phones With Advanced Display Options
- Dual-Radio Wireless Access Points
- PTZ Security Cameras
- RFID Readers
- Industrial Controls
- Magnetic Card Readers
- High Power PoE Systems

DESCRIPTION

The LTC®4268-1 is an integrated Powered Device (PD) controller and switching regulator intended for IEEE 802.3af and high power PoE applications up to 35W. By including a precision dual current limit, the LTC4268-1 keeps inrush below IEEE 802.3af current limit levels to ensure interoperability success while enabling high power applications with a 750mA operational current limit.

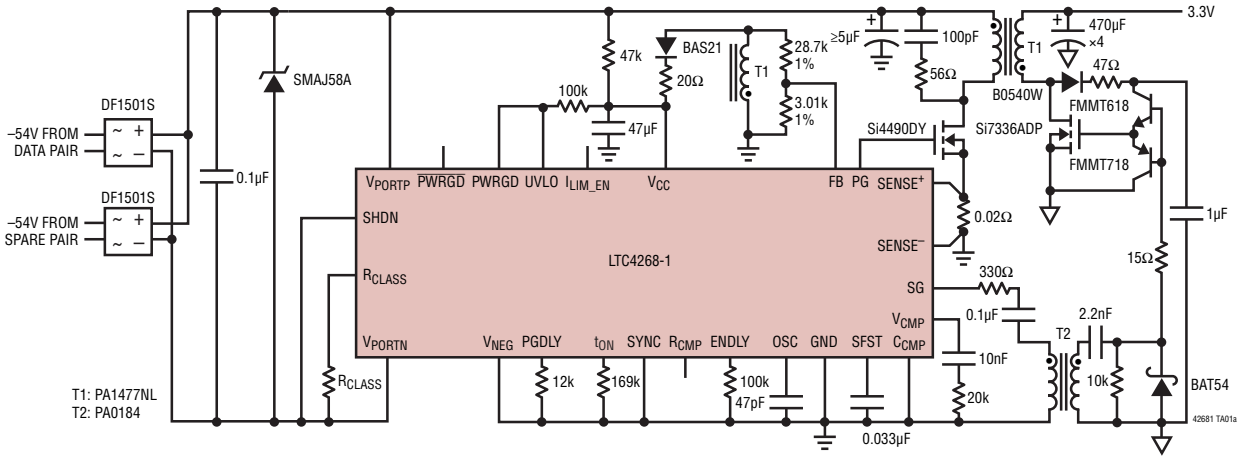
The LTC4268-1 synchronous, current-mode, flyback controller generates multiple supply rails in a single conversion providing for the highest system efficiency while maintaining tight regulation across all outputs. The LTC4268-1 includes Linear Technology's patented No-Opto feedback topology to provide full IEEE 802.3af isolation without the need of opto-isolator circuitry.

The oversized power path and high performance flyback controller of the LTC4268-1 combine to make the ultimate solution for power hungry PoE applications such as WAPs, PTZ security cameras, RFID readers and ultra-efficient 802.3af applications running near the 12.95W limit.

The LTC4268-1 is available in a space saving 32-pin DFN package.

TYPICAL APPLICATION

35W High Efficiency PD Solution

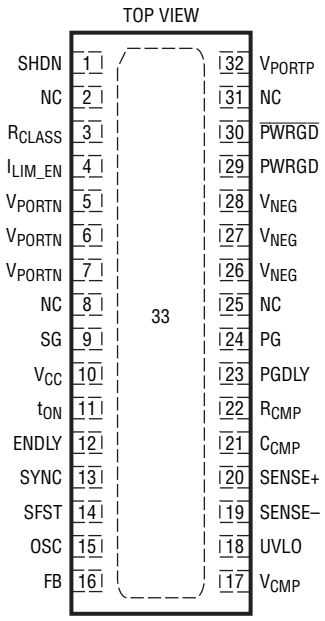


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{PORTN} Voltage ..... 0.3V to –90V
V_{NEG} Voltage ..... V_{PORTN} + 90V to V_{PORTN} –0.3V
V_{CC} to GND Voltage (Note 3)
  Low Impedance Source ..... –0.3V to 18V
  Current Fed ..... 30mA into V_{CC}
R_{CLASS}, I_{LIM_EN} Voltage .. V_{PORTN} + 7V to V_{PORTN} – 0.3V
SHDN Voltage ..... V_{PORTN} + 90V to V_{PORTN} – 0.3V
PWRGD Voltage (Note 3)
  Low Impedance Source .... V_{NEG} + 11V to V_{NEG} – 0.3V
  Current Fed 5mA
$\overline{PWRGD}$ Voltage ..... V_{PORTN} + 80V to V_{PORTN} – 0.3V
$\overline{PWRGD}$ Current 10mA
R_{CLASS} Current 100mA
$SENSE^-$, $SENSE^+$ Voltage ..... –0.5V to +0.5V
UVLO, SYNC Voltage ..... –0.3V to V_{CC}
FB Current ..... ±2mA
V_{CMP} Current ..... ±1mA
Operating Ambient Temperature Range (Notes 4, 5)
  LTC4268-1C ..... 0°C to 70°C
  LTC4268-1I ..... –40°C to 85°C
Junction Temperature (Note 5) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DKD32 PACKAGE
32-LEAD (7mm × 4mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 49°C/W, θ_{JC} = 4.7°C/W
EXPOSED PAD (PIN 33) MUST BE SOLDERED TO
HEAT SINKING PLANE THAT IS ELECTRICALLY CONNECTED TO GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4268CDKD-1#PBF	LTC4268CDKD-1#TRPBF	42681	32-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC4268IDKD-1#PBF	LTC4268IDKD-1#TRPBF	42681	32-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4268CDKD-1	LTC4268CDKD-1#TR	42681	32-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC4268IDKD-1	LTC4268IDKD-1#TR	42681	32-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 14V, SG open, V_{CMP} = 1.5V, V_{SENSE} = 0V, R_{CMP} = 1k, R_{tON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{PORT}	Supply Voltage	Voltage With Respect to V_{PORTP} Pin (Notes 6, 7, 8, 9, 10)					
	IEEE 802.3af System		●			–57	V
	Signature Range		●	–1.5		–10.1	V
	Classification Range		●	–12.5		–21	V
	UVLO Turn-On Voltage		●	–37.7	–38.9	–40.2	V
	UVLO Turn-Off Voltage		●	–29.8	–30.6	–31.5	V
V_{TURNON}	V_{CC} Turn-On Voltage	Voltage With Respect to GND	●	14	15.3	16.6	V
$V_{TURNOFF}$	V_{CC} Turn-Off Voltage	Voltage With Respect to GND	●	8	9.7	11	V
V_{HYST}	V_{CC} Hysteresis	$V_{TURNON} – V_{TURNOFF}$	●	4	5.6	7.2	V
V_{CLAMP}	V_{CC} Shunt Regulator Voltage	I_{VCC} = 15mA, V_{UVLO} = 0V, Voltage With Respect to GND	●	19.5	20.2		V
I_{VCC}	V_{CC} Supply Current	V_{CMP} = Open (Note 11)	●	4	6.4	10	mA
I_{VCC_START}	V_{CC} Start-Up Current	V_{CC} = 10V	●		180	400	µA
V_{FB}	Feedback Regulation Voltage		●	1.22	1.237	1.251	V
I_{FB_BIAS}	Feedback Pin Input Bias Current	R_{CMP} Open			200		nA
g_m	Feedback Amplifier Transconductance		●	700	1000	1400	A/V
I_{FB}	Feedback Amplifier Source or Sink Current		●	25	55	90	µA
$V_{FBCLAMP}$	Feedback Amplifier Clamp Voltage	V_{FB} = 0.9V V_{FB} = 1.4V			2.56 0.84		V V
$\%V_{REF}$	Reference Voltage Line Regulation	12V ≤ V_{CC} ≤ 18V	●		0.005	0.02	%/V
A_V	Feedback Amplifier Voltage Gain	V_{CMP} = 1.2V to 1.7V			1500		V/V
I_{SFST}	Soft-Start Charging Current	V_{SFST} = 1.5V		16	20	25	µA
I_{SFST}	Soft-Start Discharge Current	V_{SFST} = 1.5V, V_{UVLO} = 0V		0.8	1.3		mA
V_{CMP_THLD}	Control Pin Threshold (VCMP)	Duty Cycle = Min			1		V
V_{PG_HIGH}, V_{SG_HIGH}	PG, SG, Output High Level		●	6.6	7.4	8	V
V_{PG_LOW}, V_{SG_LOW}	PG, SG, Output Low Level		●		0.01	0.05	V
V_{PG_SHDN}, V_{SG_SHDN}	PG, SG, Output Shutdown Strength	V_{UVLO} = 0V; I_{PG}, I_{SG} = 20mA	●		1.4	2.3	V
t_{PG_RISE}, t_{SG_RISE}	PG, SG Rise Time	C_{PG}, C_{SG} = 1nF			15		ns
t_{PG_FALL}, t_{SG_FALL}	PG, SG Fall Time	C_{PG}, C_{SG} = 1nF			15		ns
V_{SENSE_LIM}	Switch Current Threshold at Maximum V_{CMP}	Measured at V_{SENSE+}	●	88	100	110	mV
$\Delta V_{SENSE}/\Delta V_{CMP}$	Sense Threshold vs V_{CMP}				0.07		V/V
V_{SENSE_OC}	Sense Pin Overcurrent Fault Voltage	V_{SENSE+}, V_{SFST} < 1V	●		205	230	mV
V_{IH_SHDN}	Shutdown High Level Input Voltage	With Respect to V_{PORTN} High Level = Shutdown (Note 12)	●	3		57	V
V_{IL_SHDN}	Shutdown Low Level Input Voltage	With Respect to V_{PORTN}	●			0.45	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 14V, SG open, V_{CMP} = 1.5V, V_{SENSE} = 0V, R_{CMP} = 1k, R_{tON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{INPUT_SHDN}	Shutdown Input Resistance	With Respect to V_{PORTN}	●	100			kΩ
V_{IH_ILIM}	I_{LIM_EN} High Level Input Voltage	With Respect to V_{PORTN} (Note 13) High Level Enables Current Limit	●	4			V
V_{IL_ILIM}	I_{LIM_EN} Low Level Input Voltage	With Respect to V_{PORTN} (Note 13)	●			1	V
I_{VPORTN}	V_{PORTN} Supply Current	V_{PORTN} = –54V	●			3	mA
I_{IN_CLASS}	IC Supply Current During Classification	V_{PORTN} = –17.5V, V_{NEG} Tied to V_{PORTP} (Note 14)	●	0.55	0.62	0.70	mA
ΔI_{CLASS}	Current Accuracy During Classification	10mA < I_{CLASS} < 75mA –12.5V ≤ V_{PORTN} ≤ –21V (Notes 15, 16)	●			±3.5	%
$R_{SIGNATURE}$	Signature Resistance	–1.5V ≤ V_{PORTN} ≤ –10.1V, SHDN Tied to V_{PORTN}, IEEE 802.3af Two-Point Measurement (Notes 8, 9)	●	23.25		26	kΩ
$R_{INVALID}$	Invalid Signature Resistance	–1.5V ≤ V_{PORTN} ≤ –10.1V, SHDN Tied to V_{PORTP}, IEEE 802.3af Two-Point Measurement (Notes 8, 9)			10	11.8	kΩ
$V_{\overline{PWRGD}\_OUT}$	Active Low Power Good Output Voltage	I = 1mA, V_{PORTN} = –54V, $\overline{PWRGD}$ Referenced to V_{PORTN}	●			0.5	V
$I_{\overline{PWRGD}\_LEAK}$	Active Low Power Good Output Leakage	V_{PORT} = 0V, $V_{\overline{PWRGD}}$ = 57V	●			1	µA
V_{PWRGD_OUT}	Active High Power Good Output Voltage	I = 0.5mA, V_{PORTN} = –52V, V_{NEG} = –4V PWRGD Referenced to V_{NEG} (Note 17)	●			0.35	V
V_{PWRGD_VCLAMP}	Active High Power Good Voltage Limiting Clamp	I = 2mA, V_{NEG} = 0V, PWRGD Referenced to V_{NEG} (Note 3)	●	12	14	16.5	V
I_{PWRGD_LEAK}	Active High Power Good Output Leakage	V_{PWRGD} = 11V With Respect to V_{NEG}, V_{NEG} = V_{PORTN} = –54V	●			1	µA
R_{ON}	On-Resistance	I = 700mA, V_{PORTN} = –48V, Measured from V_{PORTN} to V_{NEG} (Note 16)	●		0.5	0.6 0.8	Ω Ω
I_{OUT_LEAK}	V_{OUT} Leakage	V_{PORTN} = –57V, V_{PORTP} = SHDN = V_{NEG} = 0V (Note 15)	●			1	µA
I_{LIM_HI}	Input Current Limit, High Level	V_{PORTN} = –54V, V_{NEG} = –53V I_{LIM_EN} Floating (Notes 18, 19)	●	700	750	800	mA
I_{LIM_LO}	Input Current Limit, Low Level	V_{PORTN} = –54V, V_{NEG} = –53V (Notes 18, 19)	●	250	300	350	mA
I_{LIM_DISA}	Safeguard Current Limit When I_{LIM} is Disabled	V_{PORTN} = –54V, V_{NEG} = –52.5V I_{LIM_EN} Tied to V_{PORTN} (Notes 18, 19, 20)		1.2	1.45	1.65	A
f_{OSC}	Oscillator Frequency	C_{OSC} = 100pF	●	84	100	110	kHz
C_{OSC}	Oscillator Capacitor Value	(Note 21)		33		200	pF
$t_{ON(MIN)}$	Minimum Switch on Time				200		ns
t_{ENDLY}	Flyback Enable Delay Time				265		ns
t_{PGDLY}	PG Turn-On Delay Time				200		ns
$DC_{ON(MAX)}$	Maximum Switch Duty Cycle		●	85	88		%
V_{SYNC}	SYNC Pin Threshold		●		1.53	2.1	V
R_{SYNC}	SYNC Pin Input Resistance				40		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 14V, SG open, V_{CMP} = 1.5V, V_{SENSE} = 0V, R_{CMP} = 1k, R_{tON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LCOMP}	Feedback Pin Load Compensation Current	V_{RCMP} With V_{SENSE}^+ = 0V			20		µA
V_{LCOMP}	Load Comp to V_{SENSE} Offset Voltage	V_{SENSE+} = 20mV, V_{FB} = 1.23V			1		mV
V_{UVLO}	UVLO Pin Threshold		●	1.215	1.237	1.265	V
I_{UVLOL} I_{UVLOH}	UVLO Pin Bias Current	V_{UVLO} = 1.2V V_{UVLO} = 1.3V		–0.25 –4.50	0 –3.4	0.25 –2.5	µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to V_{PORTP} pin unless otherwise noted.

Note 3: Active High PWRGD internal clamp circuit self-regulates to 14V with respect to V_{NEG}. V_{CC} has internal 20V clamp with respect to GND.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: T_J is calculated from the ambient temperature T_A and power dissipation P_{DIS} according to the formula:

$$T_J = T_A + (P_{DIS} \bullet 49°C/W)$$

Note 6: The LTC4268-1 operates with a negative supply voltage in the range of –1.5V to –57V. To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude. Terms such as "maximum negative voltage" refer to the largest negative voltage and a "rising negative voltage" refers to a voltage that is becoming more negative.

Note 7: In IEEE 802.3af systems, the maximum voltage at the PD jack is defined to be –57V.

Note 8: The LTC4268-1 is designed to work with two polarity protection diodes in series with the input. Parameter ranges specified in the Electrical Characteristics are with respect to LTC4268-1 pins and are designed to meet IEEE 802.3af specifications when the drop from the two diodes is included. See Applications Information.

Note 9: Signature resistance is measured via the two-point ΔV/ΔI method as defined by IEEE 802.3af. The LTC4268-1 signature resistance is offset from 25k to account for diode resistance. With two series diodes, the total PD resistance will be between 23.75k and 26.25k and meet IEEE 802.3af specifications. The minimum probe voltages measured at the LTC4268-1 pins are –1.5V and –2.5V. The maximum probe voltages are –9.1V and –10.1V.

Note 10: The LTC4268-1 includes hysteresis in the UVLO voltages to preclude any start-up oscillation. Per IEEE 802.3af requirements, the LTC4268-1 will power up from a voltage source with 20Ω series resistance on the first trial.

Note 11: Supply current does not include gate charge current to the MOSFETs. See Application Information.

Note 12: To disable the 25k signature, tie SHDN to V_{PORTP} (±0.1V) or hold SHDN high with respect to V_{IN}. See Applications Information.

Note13: I_{LIM_EN} pin is pulled high internally and for normal operation should be left floating. To disable current limit, tie I_{LIM_EN} to V_{IN}. See Applications Information.

Note 14: I_{IN_CLASS} does not include classification current programmed at Pin 3. Total supply current in classification mode will be I_{IN_CLASS} + I_{CLASS} (See Note 15).

Note 15: I_{CLASS} is the measured current flowing through R_{CLASS}. ΔI_{CLASS} accuracy is with respect to the ideal current defined as I_{CLASS} = 1.237/R_{CLASS}. $T_{CLASSRDY}$ is the time for I_{CLASS} to settle to within ±3.5% of ideal. The current accuracy specification does not include variations in R_{CLASS} resistance. The total classification current for a PD also includes the IC quiescent current (I_{IN_CLASS}). See Applications Information.

Note 16: This parameter is assured by design and wafer level testing.

Note 17: Active high power good is referenced to V_{NEG} and is valid for $V_{PORTP} - V_{NEG} \geq 4V$.

Note 18: The LTC4268-1 includes a dual current limit. At turn on, before C1 is charged, the LTC4268-1 current level is set to I_{LIMIT_LOW}. After C1 is charged and with I_{LIM_EN} floating, the LTC4268-1 switches to I_{LIMIT_HIGH}. With I_{LIM_EN} pin tied low, the LTC4268-1 switches to I_{LIMIT_DISA}. The LTC4268-1 stays in I_{LIMIT_HIGH} or I_{LIMIT_DISA} until the input voltage drops below the UVLO turn-off threshold or a thermal overload occurs.

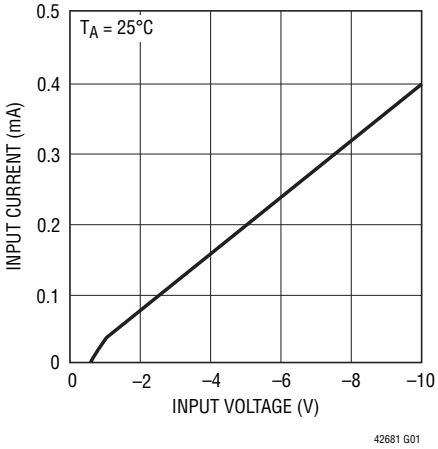
Note 19: The LTC4268-1 features thermal overload protection. In the event of an over temperature condition, the LTC4268-1 will turn off the power MOSFET, disable the classification load current, and present an invalid power good signal. Once the LTC4268-1 cools below the over temperature limit, the LTC4268-1 current limit switches to I_{LIMIT_LOW} and normal operation resumes.

Note 20: I_{LIMIT_DISA} is a safeguard current limit that is activated when the normal input current limit (I_{LIMIT_HIGH}) is defeated using the I_{LIM_EN} pin. Currents at or near I_{LIMIT_DISA} will cause significant package heating and may require a reduced maximum ambient operating temperature in order to avoid tripping the thermal overload protection.

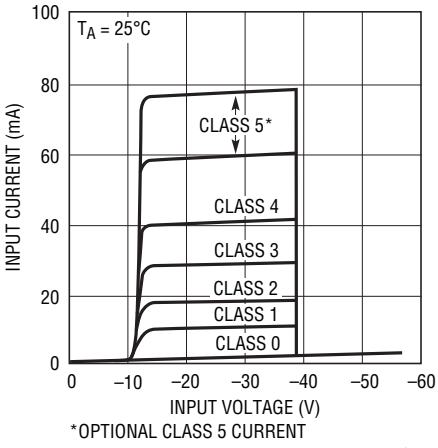
Note 21: Component value range guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

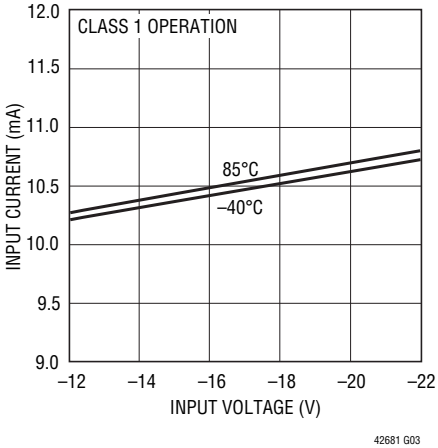
Input Current vs Input Voltage 25k Detection Range



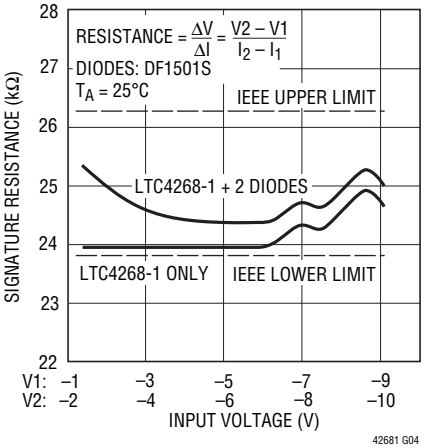
Input Current vs Input Voltage



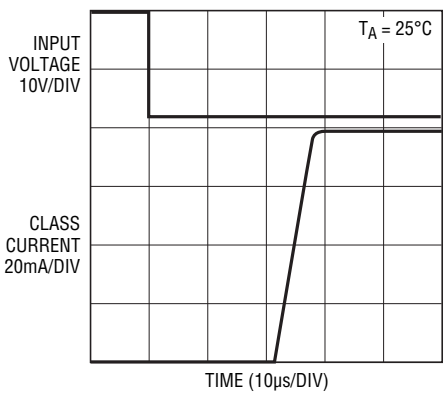
Input Current vs Input Voltage



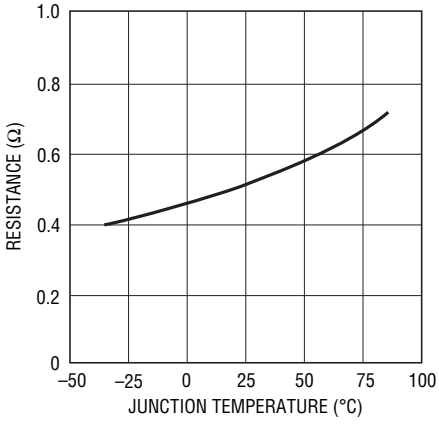
Signature Resistance vs Input Voltage



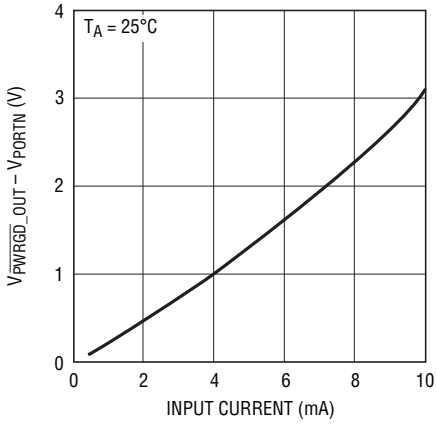
Class Operation vs Time



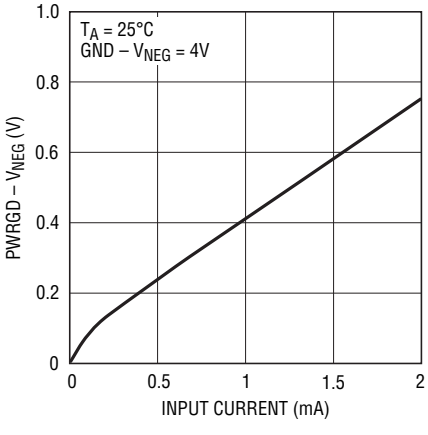
On Resistance vs Temperature



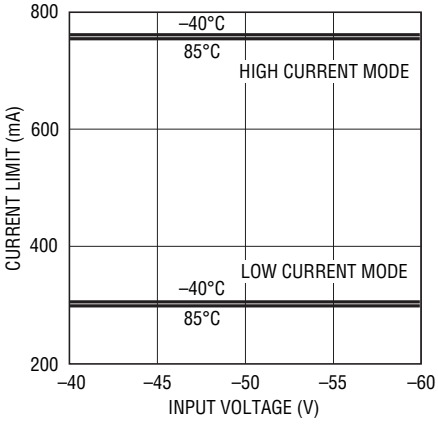
Active Low $\overline{PWRGD}$: Output Low Voltage vs Current



Active High PWRGD: Output Low Voltage vs Current

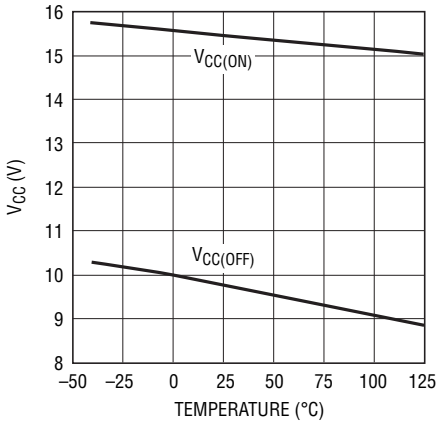


Current Limit vs Input Voltage



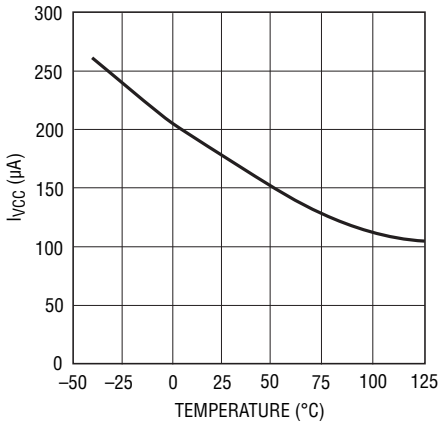
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC(ON)}$ and $V_{CC(OFF)}$ vs Temperature



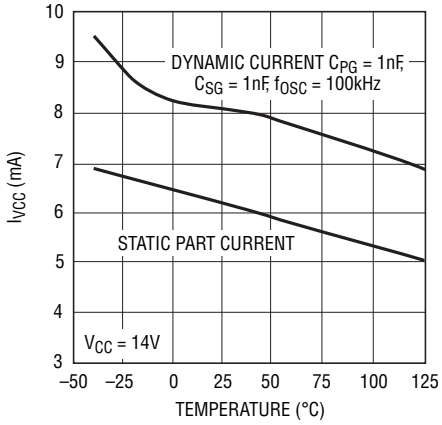
42681 G10

V_{CC} Start-Up Current vs Temperature



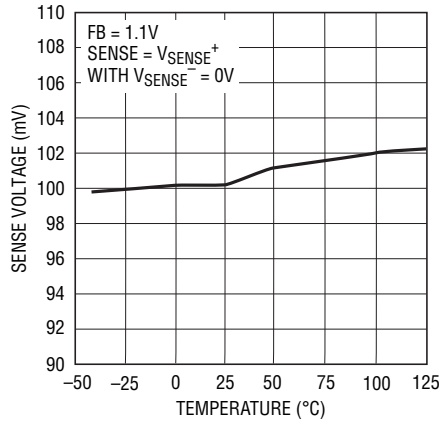
42681 G11

V_{CC} Current vs Temperature



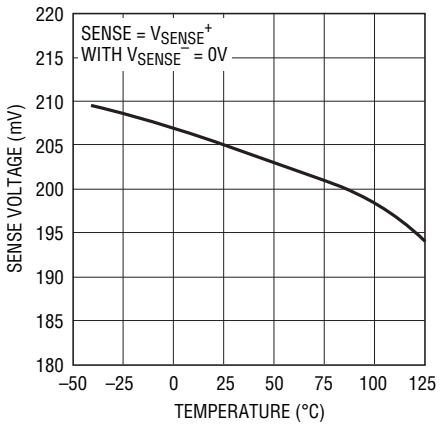
42681 G12

SENSE Voltage vs Temperature



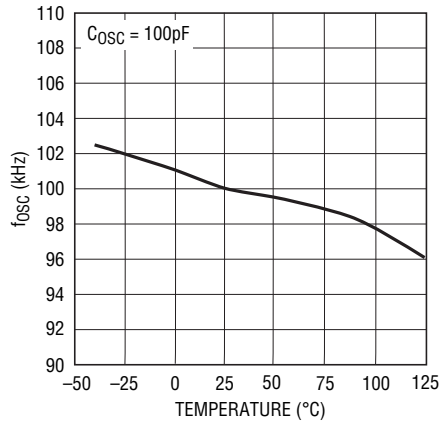
42681 G13

SENSE Fault Voltage vs Temperature



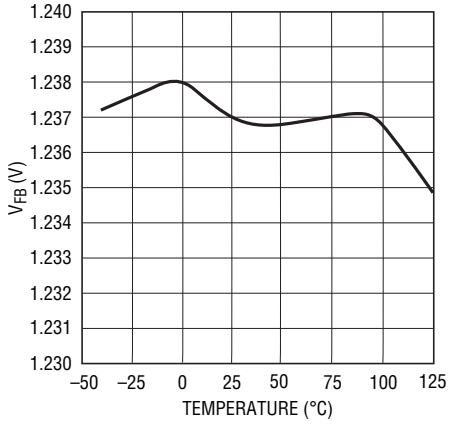
42681 G14

Oscillator Frequency vs Temperature



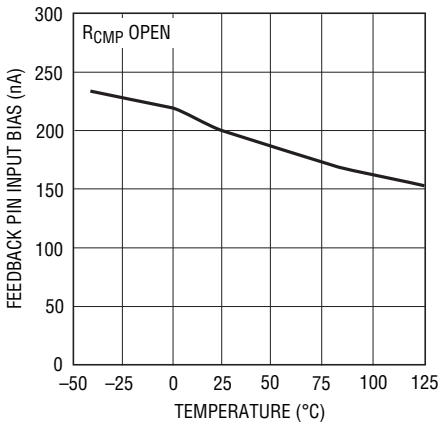
42681 G15

V_{FB} vs Temperature



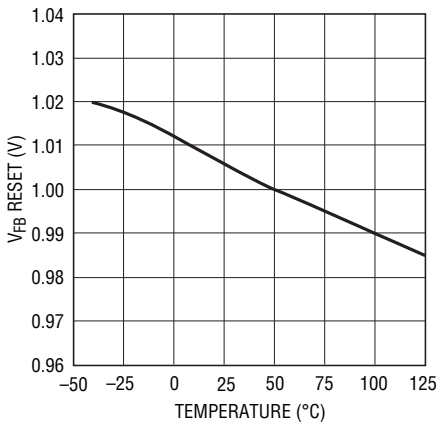
42681 G16

Feedback Pin Input Bias vs Temperature



42681 G17

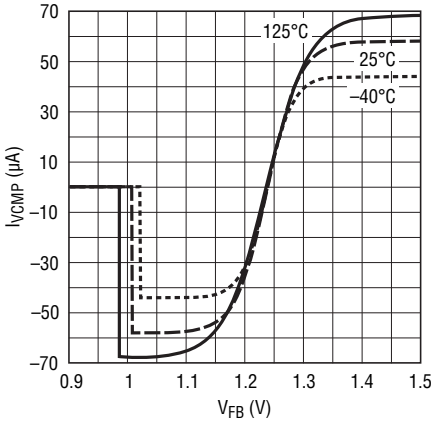
V_{FB} Reset vs Temperature



42681 G18

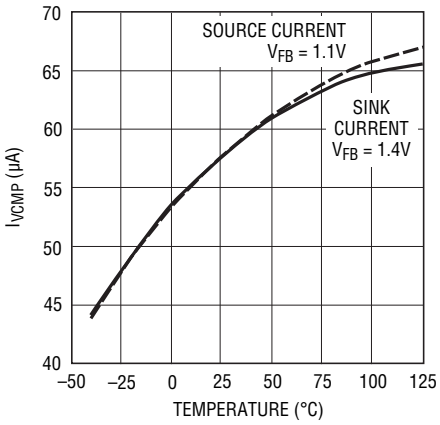
TYPICAL PERFORMANCE CHARACTERISTICS

Feedback Amplifier Output Current vs V_{FB}



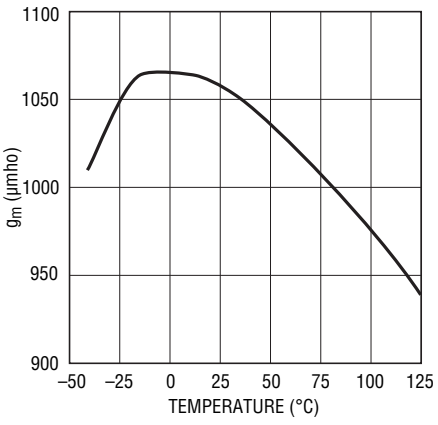
42681 G19

Feedback Amplifier Source and Sink Current vs Temperature



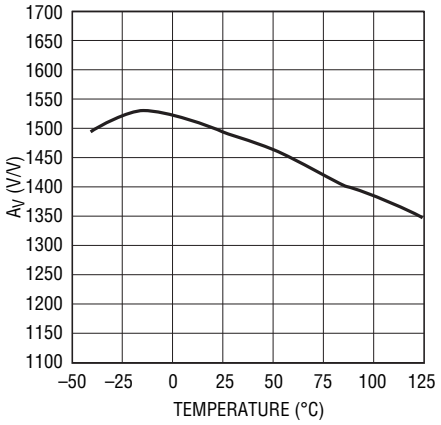
42681 G20

Feedback Amplifier g_m vs Temperature



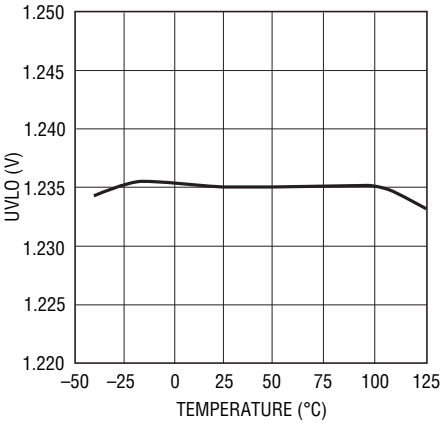
42681 G21

Feedback Amplifier Voltage Gain vs Temperature



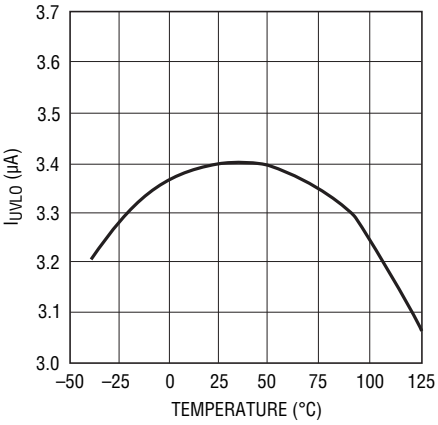
42681 G22

UVLO vs Temperature



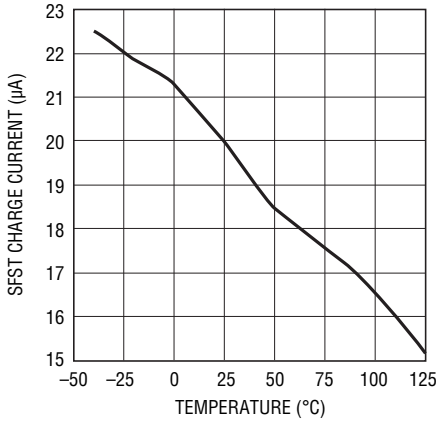
42681 G23

I_{UVLO} Hysteresis vs Temperature



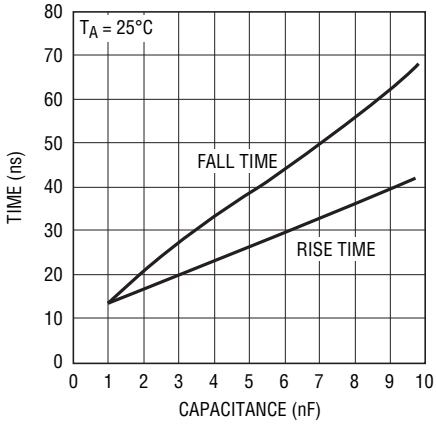
42681 G24

Soft-Start Charge Current vs Temperature



42681 G25

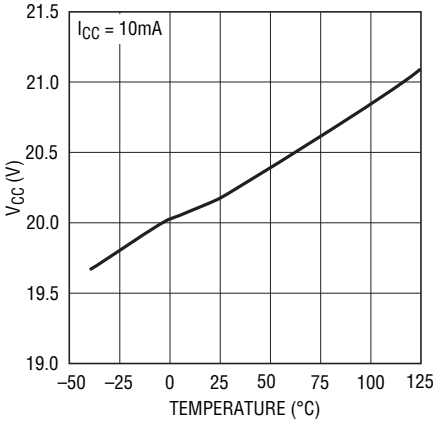
PG, SG Rise and Fall Times vs Load Capacitance



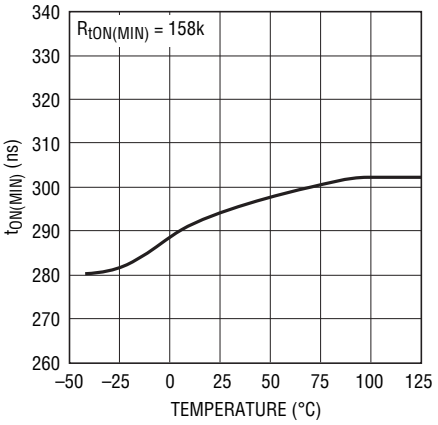
42681 G26

TYPICAL PERFORMANCE CHARACTERISTICS

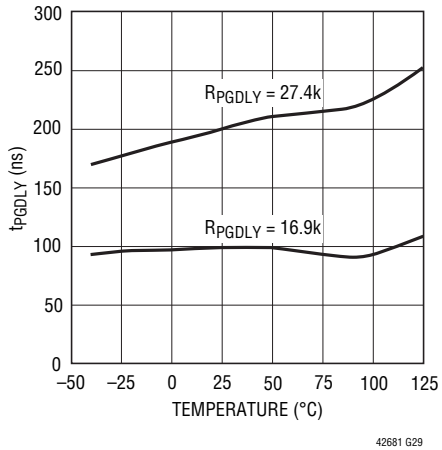
V_{CC} Clamp Voltage vs Temperature



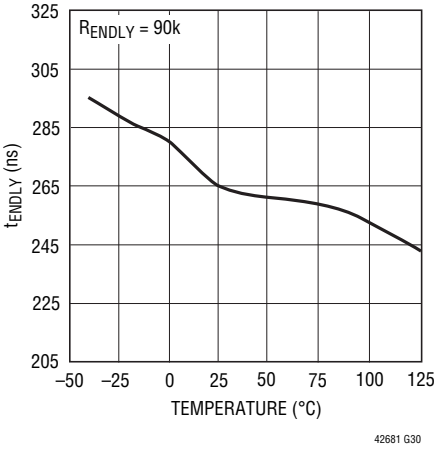
Minimum PG On Time vs Temperature



PG Delay Time vs Temperature



Enable Delay Time vs Temperature



PIN FUNCTIONS

SHDN (Pin 1): Shutdown Input. Used to command the LTC4268-1 to present an invalid signature and remain inactive. Connecting SHDN to V_{PORTP} lowers the signature resistance to an invalid value and disables the LTC4268-1 PD interface operations. If unused, tie SHDN to V_{PORTN}.

NC (Pin 2): No Internal Connection.

R_{CLASS} (Pin 3): Class Select Input. Used to set the current the LTC4268-1 maintains during classification. Connect a resistor between R_{CLASS} and V_{PORTN}. (See Table 2.)

I_{LIM_EN} (Pin 4): Input Current Limit Enable. Used for controlling the LTC4268-1 current limit behavior during powered operation. For normal operation, float I_{LIM_EN} to enable I_{LIMIT_HIGH} current. Tie I_{LIM_EN} to V_{PORTN} to disable input current limit. Note that the inrush current limit will always be active. See Applications Information.

V_{PORTN} (Pins 5, 6, 7): Power Input. Tie to the PD Input through the diode bridge. Pins 5, 6 and 7 must be electrically tied together.

NC (Pin 8): No Internal Connection.

SG (Pin 9): Secondary Gate Driver Output. This pin provides an output signal for a secondary-side synchronous switch. Large dynamic currents may flow during voltage transitions. See the Applications Information for details.

V_{CC} (Pin 10): Converter Voltage Supply. Bypass this pin to GND with 4.7µF or greater. This pin has a 20V clamp to ground. V_{CC} has an undervoltage lockout function that turns on when V_{CC} is approximately 15.3V and off at 9.7V. In a conventional "trickle-charge" bootstrapped configuration, the V_{CC} supply current increases significantly during turn-on causing a benign relaxation oscillation action on the V_{CC} pin if the part does not start normally.

t_{ON} (Pin 11): Primary Switch Minimum On Time Control. A programming resistor (R_{Ton}) to GND sets the minimum time for each cycle. See Applications Information for details.

ENDLY (Pin 12): Enable Delay Time Control. The enable delay time is set by a programming resistor (R_{ENDLY}) to GND and disables the feedback amplifier for a fixed time after the turn-off of the primary-side MOSFET. This allows the leakage inductance voltage spike to be ignored for flyback voltage sensing. See Applications Information for details.

SYNC (Pin 13): External Sync Input. This pin is used to synchronize the internal oscillator with an external clock. The positive edge of the clock causes the oscillator to discharge causing PG to go low (off) and SG high (on). The sync threshold is typically 1.5V. Tie to ground if unused. See Applications Information for details.

SFST (Pin 14): Soft-Start. This pin, in conjunction with a capacitor (C_{SFST}) to GND, controls the ramp-up of peak primary current through the sense resistor. It is also used to control converter inrush at start-up. The SFST clamps the V_{CMP} voltage and thus limits peak current until soft-start is complete. The ramp time is approximately 70ms per µF of capacitance. Leave SFST open if not using the soft-start function.

OSC (Pin 15): Oscillator. This pin in conjunction with an external capacitor (C_{OSC}) to GND defines the controller oscillator frequency. The frequency is approximately 100kHz • 100/C_{OSC} (pF).

FB (Pin 16): Feedback Amplifier Input. Feedback is usually sensed via a third winding and enabled during the flyback period. This pin also sinks additional current to compensate for load current variation as set by the R_{CMP} pin. Keep the Thevenin equivalent resistance of the feedback divider at roughly 3k.

V_{CMP} (Pin 17): Frequency Compensation Control. V_{CMP} is used for frequency compensation of the switcher control loop. It is the output of the feedback amplifier and the input to the current comparator. Switcher frequency compensation components are normally placed on this pin to GND. The voltage on this pin is proportional to the peak primary switch current. The feedback amplifier output is enabled during the synchronous switch on time.

UVLO (Pin 18): Undervoltage Lockout. A resistive divider from V_{IN} to this pin sets an undervoltage lockout based upon V_{IN} level (not V_{CC}). When the UVLO pin is below its threshold, the gate drives are disabled, but the part draws its normal quiescent current from V_{CC}. The V_{CC} undervoltage lockout supersedes this function so V_{CC} must be great enough to start the part. The bias current on this pin has hysteresis such that the bias current is sourced when UVLO threshold is exceeded. This introduces a hysteresis at the pin equivalent to the bias current change times the imped-

PIN FUNCTIONS

ance of the upper divider resistor. The user can control the amount of hysteresis by adjusting the impedance of the divider. Tie the UVLO pin to V_{CC} if you are not using this function. See the Applications Information for details. This pin is used for the UVLO function of the switching regulator. The PD interface section has an UVLO defined by the IEEE 802.3af specification.

SENSE–, SENSE+ (Pins 19, 20): Current Sense Inputs. These pins are used to measure primary side switch current through an external sense resistor. Peak primary side current is used in the converter control loop. Make Kelvin connections to the sense resistor R_{SENSE} to reduce noise problems. SENSE– connects to the GND side. At maximum current (V_{CMP} at its maximum voltage) SENSE pins have 100mV threshold. The signal is blanked (ignored) during the minimum turn-on time.

C_{CMP} (Pin 21): Load Compensation Capacitive Control. Connect a capacitor from C_{CMP} to GND in order to reduce the effects of parasitic resistances in the feedback sensing path. A 0.1µF ceramic capacitor suffices for most applications. Short this pin to GND in less demanding applications.

R_{CMP} (Pin 22): Load Compensation Resistive Control. Connect a resistor from R_{CMP} to GND in order to compensate for parasitic resistances in the feedback sensing path. In less demanding applications, this resistor is not needed and this pin can be left open. See Applications Information for details.

PGDLY (Pin 23): Primary Gate Delay Control. Connect an external programming resistor (R_{PGDLY}) to set delay from synchronous gate turn-off to primary gate turn-on. See Applications Information for details.

PG (Pin 24): Primary Gate Drive. PG is the gate drive pin for the primary side MOSFET Switch. Large dynamic currents flow during voltage transitions. See the Applications Information for details.

NC (Pin 25): No Internal Connection.

V_{NEG} (Pins 26, 27, 28): System Negative Rail. Tie to the GND pin to supply power to the flyback controller through the internal power MOSFET. V_{NEG} is high impedance until the input voltage rises above the UVLO turn-on threshold. The output is then connected to V_{PORTN} through a current-limited internal MOSFET switch. Pins 26, 27 and 28 must be electrically tied together.

PWRGD (Pin 29): Active High Power Good Output, Open-Collector. Signals to the flyback controller that the LTC4268-1 MOSFET is on and that the flyback controller can start operation. High impedance indicates power is good. PWRGD is referenced to V_{NEG} and is low impedance during inrush and in the event of a thermal overload. PWRGD is clamped to 14V above V_{NEG}.

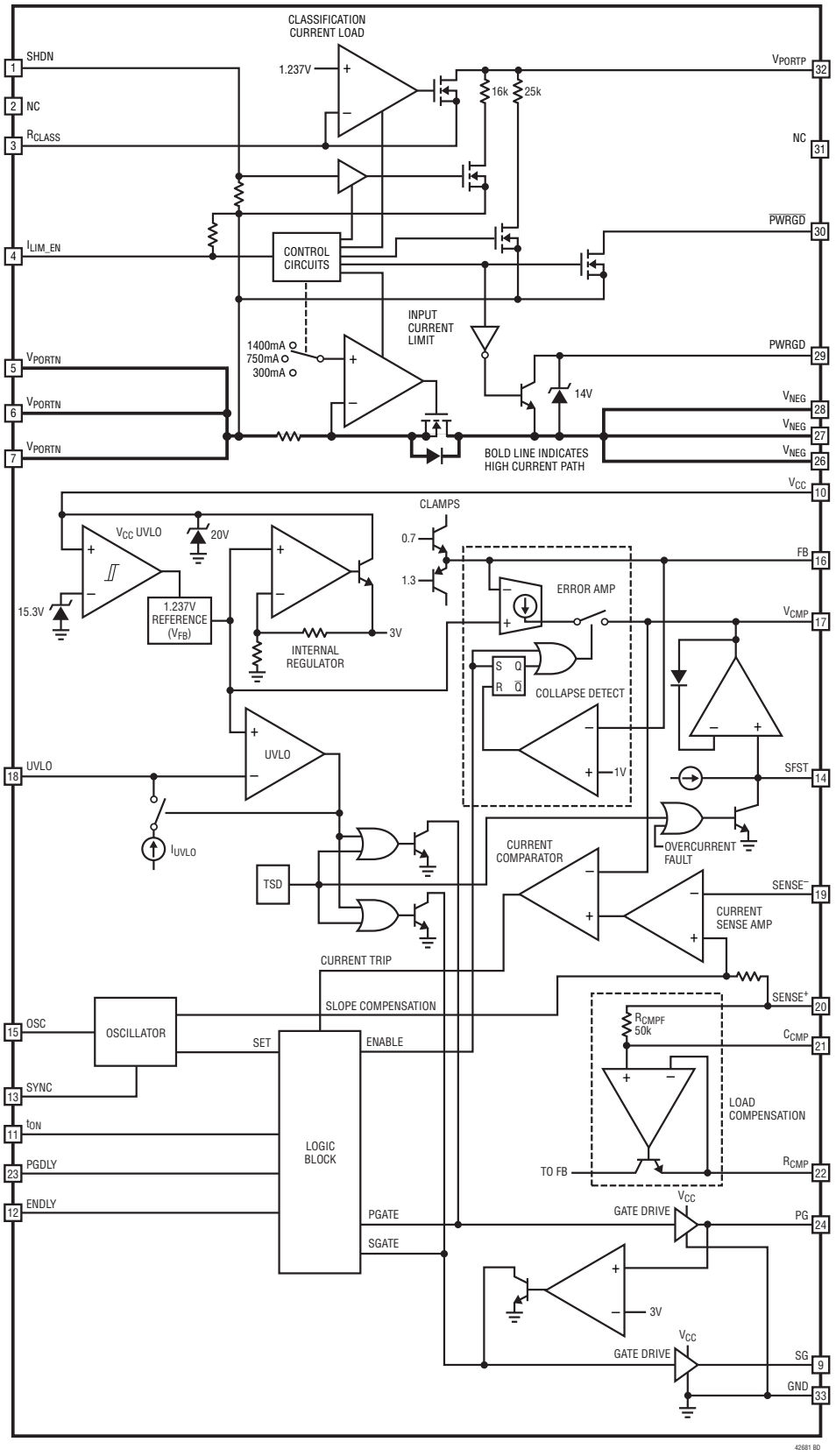
$\overline{\text{PWRGD}}$ (Pin 30): Active Low Power Good Output, Open-Drain. Signals to the DC/DC converter that the LTC4268-1 MOSFET is on and that the converter can start operation. Low impedance indicates power is good. $\overline{\text{PWRGD}}$ is referenced to V_{PORTN} and is high impedance during detection, classification and in the event of a thermal overload. $\overline{\text{PWRGD}}$ has no internal clamps.

NC (Pin 31): No Internal Connection.

V_{PORTP} (Pin 32): Positive Power Input. Tie to the input port power return through the input diode bridge.

GND (Pin 33): Ground. This is the negative rail connection for both signal ground and gate driver grounds. This pin should be connected to V_{NEG}. Careful attention must be paid to layout. See the Applications Information for details.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as an increasing number of products are taking advantage of having DC power and high speed data available from a single RJ45 connector. As PoE is becoming established in the marketplace, Powered Device (PD) equipment vendors are running into the 12.95W power limit established by the IEEE 802.3af standard. To solve this problem and expand the application of PoE, the LTC4268-1 breaks the power barrier by allowing custom PoE applications to deliver up to 35W for power hungry PoE applications such as dual band access points, RFID readers and PTZ security cameras.

The LTC4268-1 is designed to be a complete solution for PD applications with power requirements up to 35W. The LTC4268-1 interfaces with custom Power Sourcing Equipment (PSE) using a high efficiency flyback topology for maximum power delivery without the need for opto-isolator feedback. Off-the-shelf high power PSEs are available today from a variety of vendors for use with the LTC4268-1 to allow quick implementation of a custom system.

OPERATION

Note: Please refer to the simplified application circuit (Figure 1) for voltage naming conventions used in this data sheet.

The LTC4268-1 high power PD interface controller and switching regulator has several modes of operation depending on the applied V_{PORT} voltage as shown in Figure 2 and summarized in Table 1. These various modes satisfy the requirements defined in the IEEE 802.3af specification. The input voltage is applied to the V_{PORTN} pin with reference to the V_{PORTP} pin and is always negative.

SERIES DIODES

The IEEE 802.3af-defined operating modes for a PD reference the input voltage at the RJ45 connector on the PD. In this data sheet port voltage is normally referenced to the pins of the LTC4268-1. Note that the voltage ranges specified in the LTC4268-1 Electrical Specifications are referenced with respect to the IC pins.

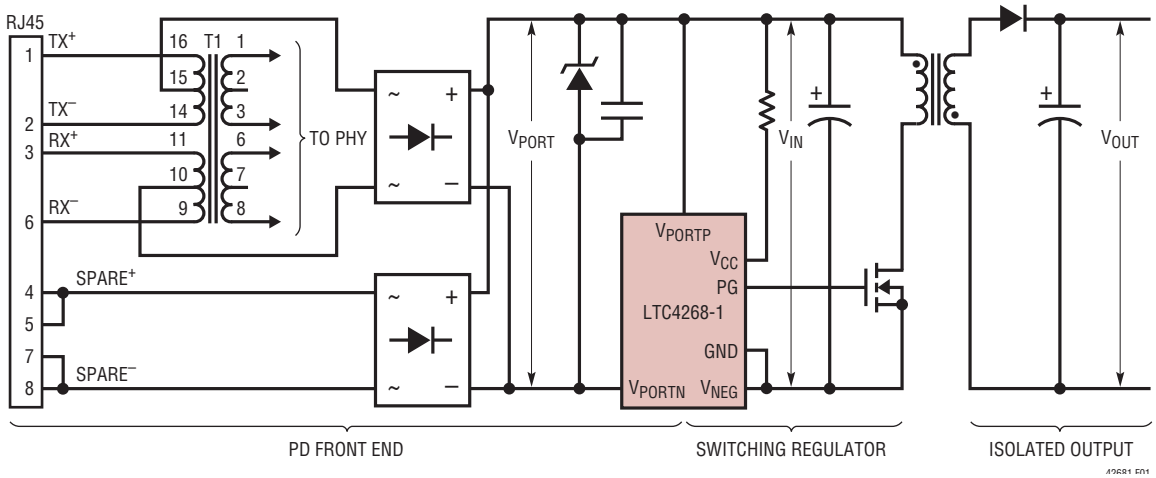


Figure 1. Simplified Application Circuit With Voltage Naming Conventions

APPLICATIONS INFORMATION

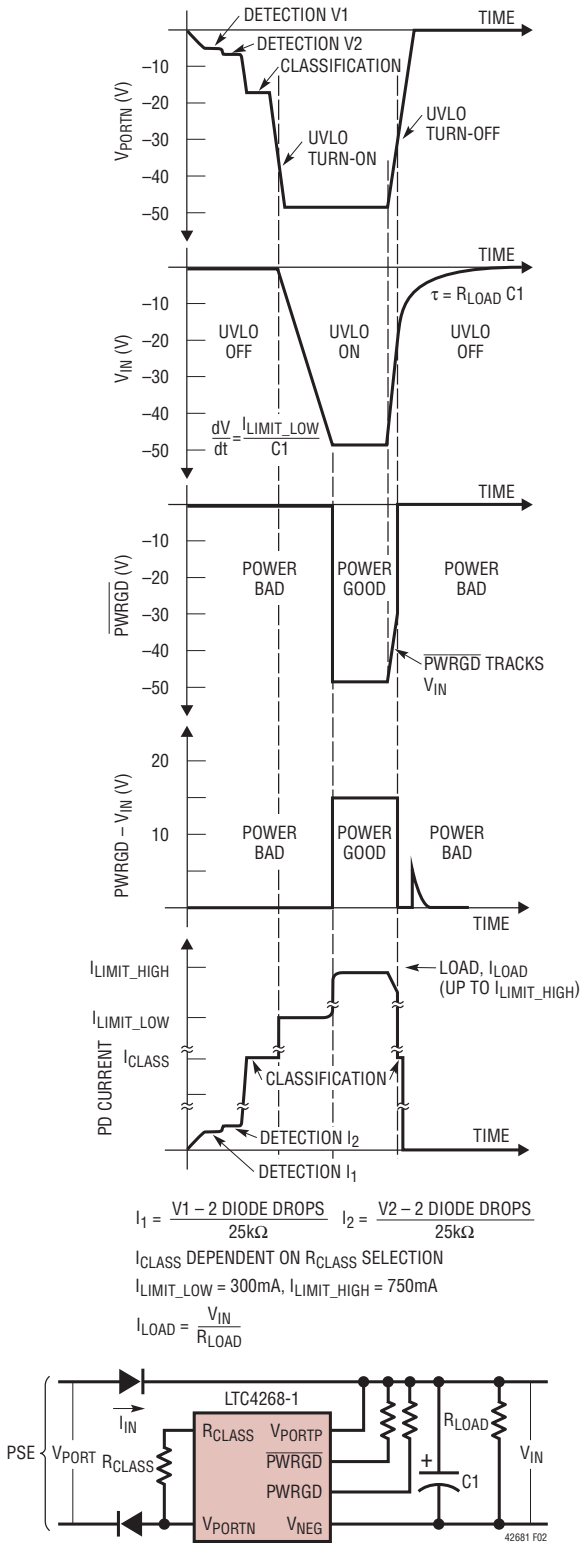


Figure 2. V_{IN} Voltage, $\overline{PWRGD}$, PWRGD and PD Current as a Function of Port Voltage

The PD must be able to handle power received in either polarity. For this reason, it is common to install diode bridges between the RJ45 connector and the LTC4268-1 (Figure 3). The diode bridges introduce an offset that affects the threshold points for each range of operation. The LTC4268-1 meets the IEEE 802.3af-defined operating modes by compensating for the diode drops in the threshold points. For the signature, classification, and the UVLO thresholds, the LTC4268-1 extends two diode drops below the IEEE 802.3af specifications. The LTC4268-1 threshold points support the use of either traditional or Schottky diode bridges.

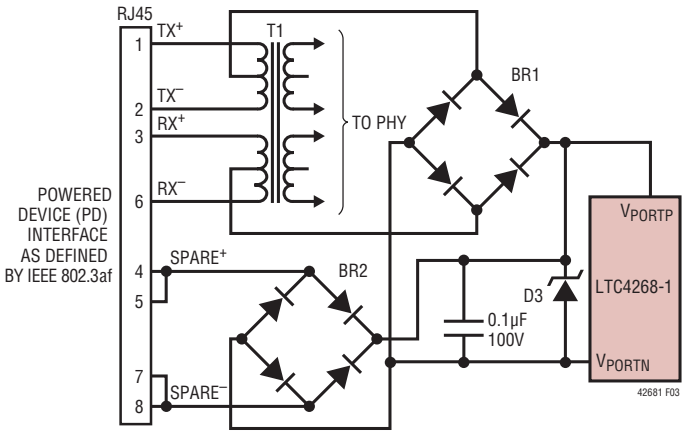


Figure 3. PD Front End Using Diode Bridges on Main and Spare Inputs

DETECTION

During detection, the PSE will apply a voltage in the range of –2.8V to –10V on the cable and look for a 25k signature resistor. This identifies the device at the end of the cable as a PD. With the PSE voltage in the detection range, the LTC4268-1 presents an internal 25k resistor between the V_{PORTP} and V_{PORTN} pins. This precision, temperature-compensated resistor provides the proper characteristics to alert the PSE that a PD is present and requests power to be applied.

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Table 1. LTC4268-1 Operational Mode as a Function of V_{PORT} Voltage

V_{PORT}	MODE OF OPERATION
0V to –1.4V	Inactive
–1.5V to –10.1V	25k Signature Resistor Detection
–10.3V to –12.4V	Classification Load Current Ramps Up from 0% to 100%
–12.5V to UVLO*	Classification Load Current Active
UVLO* to –57V	Power Applied to PD Load

*UVLO includes hysteresis.
Rising input threshold ≅ –38.9V
Falling input threshold ≅ –30.6V

The IEEE 802.3af specification requires the PSE to use a ΔV/ΔI measurement technique to keep the DC offset voltage of the diode bridge from affecting the signature resistance measurement. However, the diode resistance appears in series with the signature resistor and must be included in the overall signature resistance of the PD.

The LTC4268-1 compensates for the two series diodes in the signature path by offsetting the internal resistance so that a PD built with the LTC4268-1 meets the IEEE 802.3af specification.

In some designs that include an auxiliary power option, such as an external wall adapter, it is necessary to control whether or not the PD is detected by a PSE. With the LTC4268-1, the 25k signature resistor can be enabled or disabled with the SHDN pin (Figure 4). Taking the SHDN pin high will reduce the signature resistor to 10k which is an invalid signature per the IEEE 802.3af specifications. This will prevent a PSE from detecting and powering the PD. This invalid signature is present in the PSE probing range of –2.8V to –10V. When the input rises above –10V, the signature resistor reverts to 25k to minimize power dissipation in the LTC4268-1. To disable the signature, tie SHDN to V_{PORTP}. Alternately, the SHDN pin can be driven high with respect to V_{PORTN}. When SHDN is high, all functions are disabled. For normal operation tie SHDN to V_{PORTN}.

CLASSIFICATION

Once the PSE has detected a PD, the PSE may optionally classify the PD. Classification provides a method for more efficient allocation of power by allowing the PSE to identify lower-power PDs and assign the appropriate power level to these devices. For each class, there is an associated load current that the PD asserts onto the line during classification probing. The PSE measures the PD load current in order to assign the proper PD classification. Class 0 is included in the IEEE 802.3af specification to cover PDs that do not support classification. Class 1-3 partition PDs into three distinct power ranges as shown in Table 2.

Table 2. Summary of IEEE 802.3af Power Classifications and LTC4268-1 R_{CLASS} Resistor Selection

CLASS	USAGE	MAXIMUM POWER LEVELS AT INPUT OF PD (W)	NOMINAL CLASSIFICATION LOAD CURRENT (mA)	LTC4268-1 RCLASS RESISTOR (Ω, 1%)
0	Default	0.44 to 13.0	<5	Open
1	Optional	0.44 to 3.84	10.5	124
2	Optional	3.84 to 6.49	18.5	69.8
3	Optional	6.49 to 13.0	28	45.3
4	Reserved by IEEE. See Apps		40	30.9
5	Undefined by IEEE. See Apps		56	22.1

Class 4 was reserved by the IEEE 802.3af committee for future use and has been reassigned as a high power indicator by IEEE 802.3at. The new Class 5 defined here is available for system vendors to implement a unique

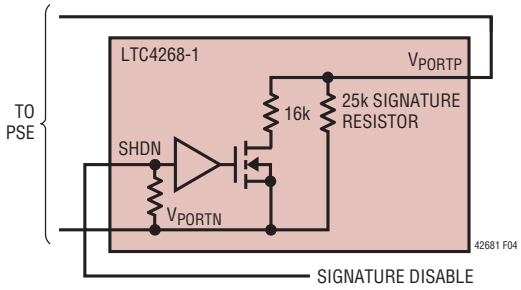

Figure 4. 25k Signature Resistor With Disable

APPLICATIONS INFORMATION

classification for use in closed systems and is not defined or supported by the IEEE 802.3af. With the extended classification range available in the LTC4268-1, it is possible for system designers to define multiple classes using load currents between 40mA and 75mA.

During classification, the PSE presents a fixed voltage between –15.5V and –20.5V to the PD (Figure 5). With the input voltage in this range, the LTC4268-1 asserts a load current from the V_{PORTP} pin through the R_{CLASS} resistor. The magnitude of the load current is set with the selection of the R_{CLASS} resistor. The resistor value associated with each class is shown in Table 2.

A substantial amount of power is dissipated in the LTC4268-1 during classification. The IEEE 802.3af specification limits the classification time to 75ms in order avoid excessive heating. The LTC4268-1 is designed to handle the power dissipation during the probe period. If the PSE probing exceeds 75ms, the LTC4268-1 may overheat. In this situation, the thermal protection circuit will engage and disable the classification current source, protecting the LTC4268-1 from damage. When the die cools, classification is automatically resumed.

Classification presents a challenging stability problem for the PSE due to the wide range of loads possible. The LTC4268-1 has been designed to avoid PSE interoperability problems by maintaining a positive I-V slope throughout the signature and classification ranges up to UVLO turn on as shown in Figure 6. The positive I-V slope avoids areas of negative resistance and helps prevent the PSE from power cycling or getting "stuck" during signature or classification probing. In the event a PSE overshoots beyond the classification voltage range, the available load current aids in returning the PD back into the classification voltage range. (The PD input may otherwise be "trapped" by a reverse-biased diode bridge and the voltage held by the 0.1µF capacitor.) By gently ramping the classification current on and maintaining a positive I-V slope until UVLO turn-on, the LTC4268-1 provides a well behaved load, assuring interoperability with any PSE.

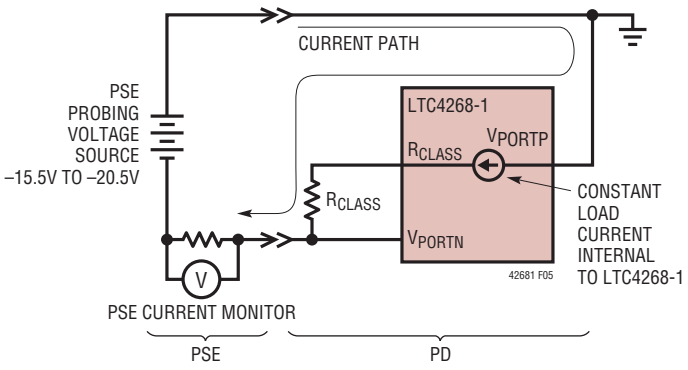

Figure 5. PSE Probing PD During Classification

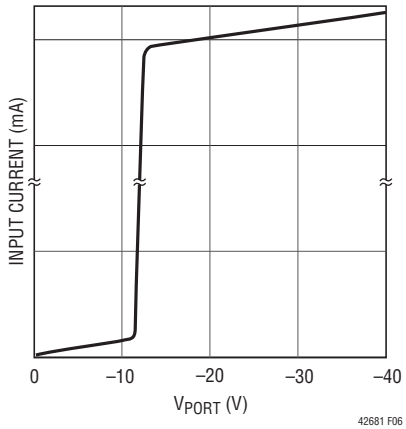

Figure 6. LTC4268-1 Positive I-V Slope

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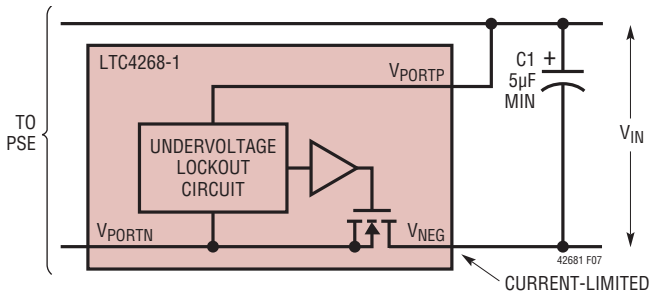
UNDERVOLTAGE LOCKOUT

The IEEE 802.3af specification dictates a maximum turn-on voltage of 42V and a minimum turn-off voltage of 30V for the PD. In addition, the PD must maintain large on-off hysteresis to prevent current-resistance (I-R) drops in the wiring between the PSE and the PD from causing start-up oscillation. The LTC4268-1 incorporates an undervoltage lockout (UVLO) circuit that monitors line voltage at V_{PORTN} to determine when to apply power to the PD load (Figure 7). Before power is applied to the load, the V_{NEG} pin is high impedance and there is no charge on capacitor C1. When the input voltage rises above the UVLO turn-on threshold, the LTC4268-1 removes the classification load current and turns on the internal power MOSFET. C1 charges up under LTC4268-1 inrush current limit control and the V_{NEG} pin transitions from 0V to V_{PORTN} as shown in Figure 2. The LTC4268-1 includes a hysteretic UVLO circuit on V_{PORTN} that keeps power applied to the load until the magnitude of the input voltage falls below the UVLO turn-off threshold. Once V_{PORTN} falls below UVLO turn-off, the internal power MOSFET disconnects V_{NEG} from V_{PORTN} and the classification current is re-enabled. C1 will discharge through the PD circuitry and the V_{NEG} pin will go to a high impedance state.

INPUT CURRENT LIMIT

IEEE 802.3af specifies a maximum inrush current and also specifies a minimum load capacitor between the V_{PORTP} and V_{NEG} pins. To control turn-on surge currents in the system the LTC4268-1 integrates a dual current limit circuit using an onboard power MOSFET and sense resistor to provide a complete inrush control circuit without additional external components. At turn-on, the LTC4268-1 will limit the inrush current to I_{LIMIT_LOW}, allowing the load capacitor to ramp up to the line voltage in a controlled manner without interference from the PSE current limit. By keeping the PD current limit below the PSE current limit, PD power up characteristics are well controlled and independent of PSE behavior. This ensures interoperability regardless of PSE output characteristics.

After load capacitor C1 is charged up, the LTC4268-1 switches to the high input current limit, I_{LIMIT_HIGH}. This allows the LTC4268-1 to deliver up to 35W to the PD load for high power applications. To maintain compatibility with IEEE 802.3af power levels, it is necessary for the PD designer to ensure the PD steady-state power consumption remains below the limits shown in Table 2. The LTC4268-1 maintains the high input current limit until the port voltage drops below the UVLO turn-off threshold.



V_{PORT} VOLTAGE	LTC4268-1 POWER MOSFET
0V TO UVLO*	OFF
>UVLO*	ON

*UVLO INCLUDES HYSTERESIS
RISING INPUT THRESHOLD ≅ –38.9V
FALLING INPUT THRESHOLD ≅ –30.6V

Figure 7. LTC4268-1 Undervoltage Lockout

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During the inrush event as C1 is being charged, a large amount of power is dissipated in the MOSFET. The LTC4268-1 is designed to accept this load and is thermally protected to avoid damage to the onboard power MOSFET. If a thermal overload does occur, the power MOSFET turns off, allowing the die to cool. Once the die has returned to a safe temperature, the LTC4268-1 automatically switches to I_{LIMIT_LOW}, and load capacitor C1 charging resumes.

The LTC4268-1 has the option of disabling the normal operating input current limit, I_{LIMIT_HIGH}, for custom high power PoE applications. To disable the current limit, connect I_{LIM_EN} to V_{PORTN}. To protect the LTC4268-1 from damage when the normal current limit is disabled, a safeguard current limit, I_{LIMIT_DISA} keeps the current below destructive levels, typically 1.4A. Note that continuous operation at or near the safeguard current limit will rapidly overheat the LTC4268-1, engaging the thermal protection circuit. For normal operations, float the I_{LIM_EN} pin. The LTC4268-1 maintains the I_{LIMIT_LOW} inrush current limit for charging the load capacitor regardless of the state of I_{LIM_EN}. The operation of the I_{LIM_EN} pin is summarized in Table 3.

Table 3. Summary of IEEE 802.3af Power Classifications and LTC4268-1 R_{CLASS} Resistor Selection

STATE OF I_{LIM_EN}	INRUSH CURRENT LIMIT	OPERATING INPUT CURRENT LIMIT
Floating	I_{LIMIT_LOW}	I_{LIMT_HIGH}
Tied to V_{PORTN}	I_{LIMIT_LOW}	I_{LIMIT_DISA}

POWER GOOD

The LTC4268-1 includes complementary power good outputs (Figure 8) to simplify connection to any DC/DC converter. Power Good is asserted at the end of the inrush event when load capacitor C1 is fully charged and the DC/DC converter can safely begin operation. The power good signal stays active during normal operation and is de-asserted at power off when the port drops below the UVLO threshold or in the case of a thermal overload event. For PD designs that use a large load capacitor and also

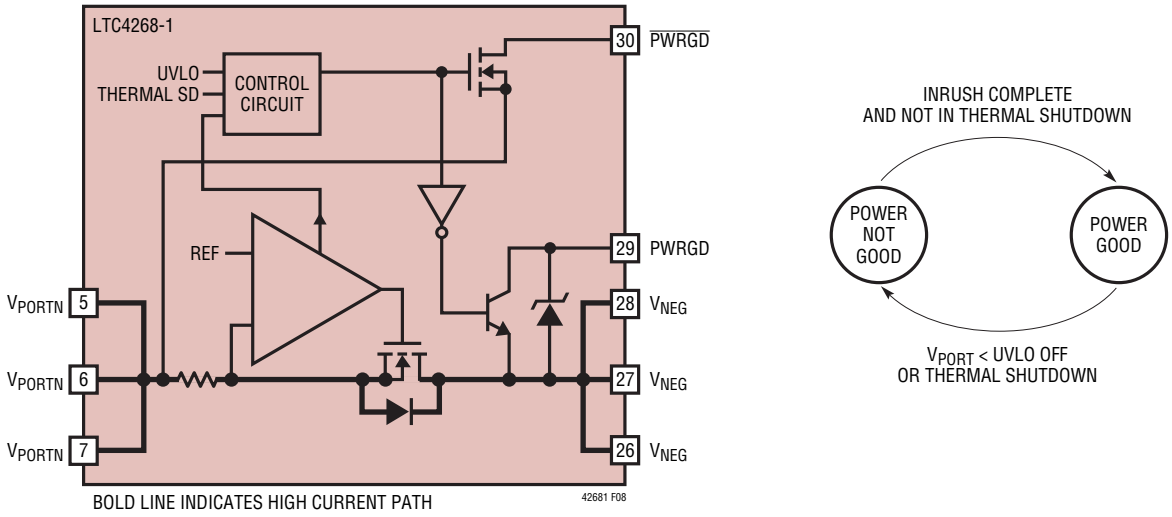

Figure 8. LTC4268-1 Power Good Functional and State Diagram

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consume a lot of power, it is important to delay activation of the DC/DC converter with the power good signal. If the converter is not disabled during the current-limited turn-on sequence, the DC/DC converter will rob current intended for charging up the load capacitor and create a slow rising input, possibly causing the LTC4268-1 to go into thermal shutdown.

The active high PWRGD pin features an internal, open-collector output referenced to V_{NEG}. During inrush, the active high PWRGD pin becomes valid when C1 reaches –4V and pulls low until the load capacitor is fully charged. At that point, PWRGD becomes high impedance, indicating the switching regulator may begin running. The active high PWRGD pin interfaces directly to the UVLO pin of the LTC4268-1 with the aid of an external pull-up resistor to Vcc. The PWRGD pin includes an internal 14V clamp to V_{NEG}. During a power supply ramp down event, PWRGD becomes low impedance when V_{PORT} drops below the 30V PD UVLO turn-off threshold, then goes high impedance when the V_{PORT} voltages fall to within the detection voltage range. Figure 11 shows a typical connection scheme for the active high PWRGD pin.

The LTC4268-1 also includes an active low $\overline{PWRGD}$ pin for system level use. $\overline{PWRGD}$ is referenced to the V_{PORTN} pin and when active will be near the V_{PORTN} potential. The negative rail (GND) of the internal switching regulator will typically be referenced to V_{NEG} and care must be taken to ensure that the difference in potential of the $\overline{PWRGD}$ pin does not cause a problem for the switcher.

THERMAL PROTECTION

The LTC4268-1 includes thermal overload protection in order to provide full device functionality in a miniature package while maintaining safe operating temperatures. At turn-on, before load capacitor C1 has charged up, the instantaneous power dissipated by the LTC4268-1 can be as high as 20W. As the load capacitor charges, the power dissipation in the LTC4268-1 will decrease until it reaches a steady-state value dependent on the DC load current. The LTC4268-1 can also experience device heating after turn-on if the PD experiences a fast input voltage rise. For example, if the PD input voltage steps from –37V to –57V, the instantaneous power dissipated by the LTC4268-1 can be as high as 16W. The LTC4268-1 protects itself from damage by monitoring die temperature. If the die exceeds the overtemperature trip point, the power MOSFET and classification transistors are disabled until the part cools down. Once the die cools below the overtemperature trip point, all functions are enabled automatically. During classification, excessive heating of the LTC4268-1 can occur if the PSE violates the 75ms probing time limit. In addition, the IEEE 802.3af specification requires a PD to withstand application of any voltage from 0V to 57V indefinitely. To protect the LTC4268-1 in these situations, the thermal protection circuitry disables the classification circuit and the input current if the die temperature exceeds the overtemperature trip point. When the die cools down, classification and input current are enabled.

Once the LTC4268-1 has charged up the load capacitor and the PD is powered and running, there will be some residual heating due to the DC load current of the PD flowing through the internal MOSFET. In some high current applications, the LTC4268-1 power dissipation may be significant. The LTC4268-1 uses a thermally enhanced DFN package that includes an exposed pad which should be soldered to the GND plane for heat sinking on the printed circuit board.

MAXIMUM AMBIENT TEMPERATURE

The LTC4268-1 I_{LIM_EN} pin allows the PD designer to disable the normal operating current limit. With the normal current limit disabled, it is possible to pass currents as high as 1.4A through the LTC4268-1. In this mode, significant package heating may occur. Depending on the current, voltage, ambient temperature, and waveform characteristics, the LTC4268-1 may shut down. To avoid nuisance trips of the thermal shutdown, it may be necessary to limit the maximum ambient temperature. Limiting the die temperature to 125°C will keep the LTC4268-1 from hitting thermal shutdown. For DC loads the maximum ambient temperature can be calculated as:

$$T_{MAX} = 125 – \theta_{JA} \bullet PWR\ (°C)$$

where T_{MAX} is the maximum ambient operating temperature, θ_{JA} is the junction-to-ambient thermal resistance (49°C/W), and PWR is the power dissipation for the LTC4268-1 in Watts ($I_{PD}^2 \bullet R_{ON}$).

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EXTERNAL INTERFACE AND COMPONENT SELECTION

Transformer

Nodes on an Ethernet network commonly interface to the outside world via an isolation transformer (Figure 9). For powered devices, the isolation transformer must include a center tap on the media (cable) side. Proper termination is required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions. For high power applications beyond IEEE 802.3af limits, the increased current levels increase the current imbalance in the magnetics. This imbalance reduces the perceived inductance and can interfere with data transmission. Transformers specifically designed for high current applications are required. Transformer vendors such as Bel Fuse, Coilcraft, Halo, Pulse, and Tyco (Table 4) can provide assistance with selection of an appropriate isolation transformer and proper termination methods. These vendors have transformers specifically designed for use in high power PD applications.

Table 4. Power over Ethernet Transformer Vendors

V_{PORT}	MODE OF OPERATION
Bel Fuse Inc.	206 Van Vorst Street Jersey City, NJ 07302 Tel: 201-432-0463 www.belfuse.com
Coilcraft Inc.	1102 Silver Lake Road Gary, IL 60013 Tel: 847-639-6400 www.coilcraft.com
Halo Electronics	1861 Landings Drive Mountain View, CA 94043 Tel: 650-903-3800 www.haloelectronics.com
Pulse Engineering	12220 World Trade Drive San Diego, CA 92128 Tel: 858-674-8100 www.pulseeng.com
Tyco Electronics	308 Constitution Drive Menlo Park, CA 94025-1164 Tel: 800-227-7040 www.circuitprotection.com

IEEE 802.3af allows power wiring in either of two configurations on the TX/RX wires, and power can be applied to the PD via the spare wire pair in the RJ45 connector. The

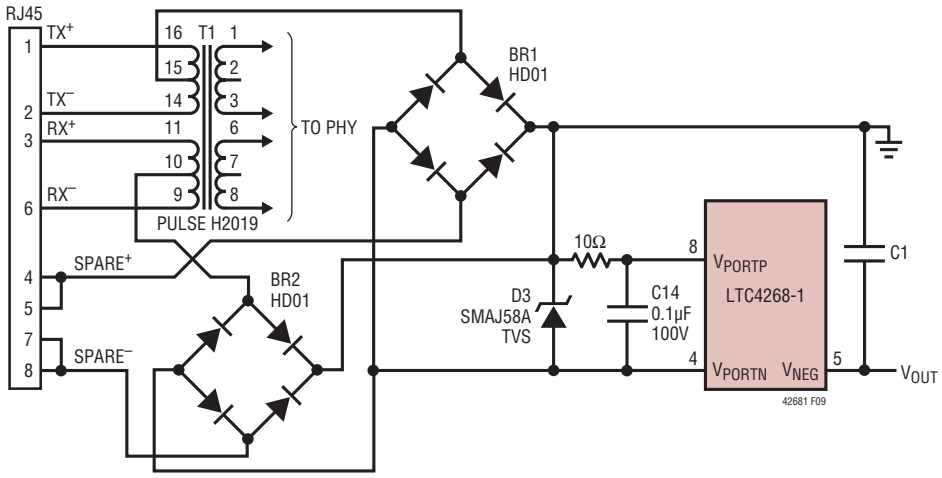

Figure 9. PD Front-End Isolation Transformer, Diode Bridges, Capacitors and TVS

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PD is required to accept power in either polarity on both the data and spare inputs; therefore it is common to install diode bridges on both inputs in order to accommodate the different wiring configurations. Figure 9 demonstrates an implementation of the diode bridges to minimize heating. The IEEE 802.3af specification also mandates that the leakage back through the unused bridge be less than 28µA when the PD is powered with 57V.

The LTC4268-1 has several different modes of operation based on the voltage present between the V_{PORTN} and V_{PORTP} pins. The forward voltage drop of the input diodes in a PD design subtracts from the input voltage and will affect the transition point between modes.

The input diode bridge of a PD can consume over 4% of the available power in some applications. Schottky diodes can be used in order to reduce power loss. The LTC4268-1 is designed to work with both standard and Schottky diode bridges while maintaining proper threshold points for IEEE 802.3af compliance.

Input Capacitor

The IEEE 802.3af/at standard includes an impedance requirement in order to implement the AC disconnect function. A 0.1µF capacitor (C14 in Figure 9) is used to meet the AC impedance requirement.

Input Series Resistance

Linear Technology has seen the customer community cable discharge requirements increase by nearly 500,000 times the original test levels. The PD must survive and operate reliably not only when an initially charged cable connects and dissipates the energy through the PD front end, but also when the electrical power system grounds are subject to very high energy events (e.g., lightning strikes).

In these high energy events, adding 10Ω series resistance into the V_{PORTP} pin greatly improves the robustness of the LTC4268-1 based PD (see Figure 9). The TVS limits the voltage across the port while the 10Ω and 0.1µF capacitance reduces the edge rate the LT4268-1 encounters across its pin. The added 10Ω series resistance does not operationally affect the LTC4268-1 PD Interface, nor does it affect its compliance with the IEEE 802.3 standard.

Transient Voltage Suppressor

The LTC4268-1 specifies and absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events. However, the pins that interface to the outside world can routinely see excessive peak voltages. To protect the LTC4268-1, install a transient voltage suppressor (D3) between the input diode bridge and the LTC4268-1, as shown in Figure 9. An SMAJ58A is recommended for typical PD applications. However, an SMBJ58A may be preferred in applications where the PD front end must absorb higher energy discharge events.

Auxiliary Power Source

In some applications, it may be necessary to power the PD from an auxiliary power source such as a wall adapter. The auxiliary power can be injected into the PD at several locations and various trade-offs exist. Figure 10 demonstrates four methods of connecting external power to a PD.

Option 1 in Figure 10 inserts power before the LTC4268-1 interface controller. In this configuration, it is necessary for the wall adapter to exceed the LTC4268-1 UVLO turn-on requirement. This option provides input current limit for the adapter, provides a valid power good signal and simplifies power priority issues. As long as the adapter applies power to the PD before the PSE, it will take priority and the PSE will not power up the PD because the external power source will corrupt the 25k signature. If the PSE is already powering the PD, the adapter power will be in parallel with the PSE. In this case, priority will be given to the higher supply voltage. If the adapter voltage is higher, the PSE may remove the port voltage since no current will be drawn from the PSE. On the other hand, if the adapter voltage is lower, the PSE will continue to supply power to the PD and the adapter will not be used. Proper operation will occur in either scenario.

Option 2 applies power directly to the DC/DC converter. In this configuration the adapter voltage does not need to exceed the LTC4268-1 turn-on UVLO requirement and can be selected based solely on the PD load requirements. It is necessary to include diode D9 to prevent the adapter from applying power to the LTC4268-1. Power priority issues require more intervention. If the adapter voltage is below the PSE voltage, then the priority will be given

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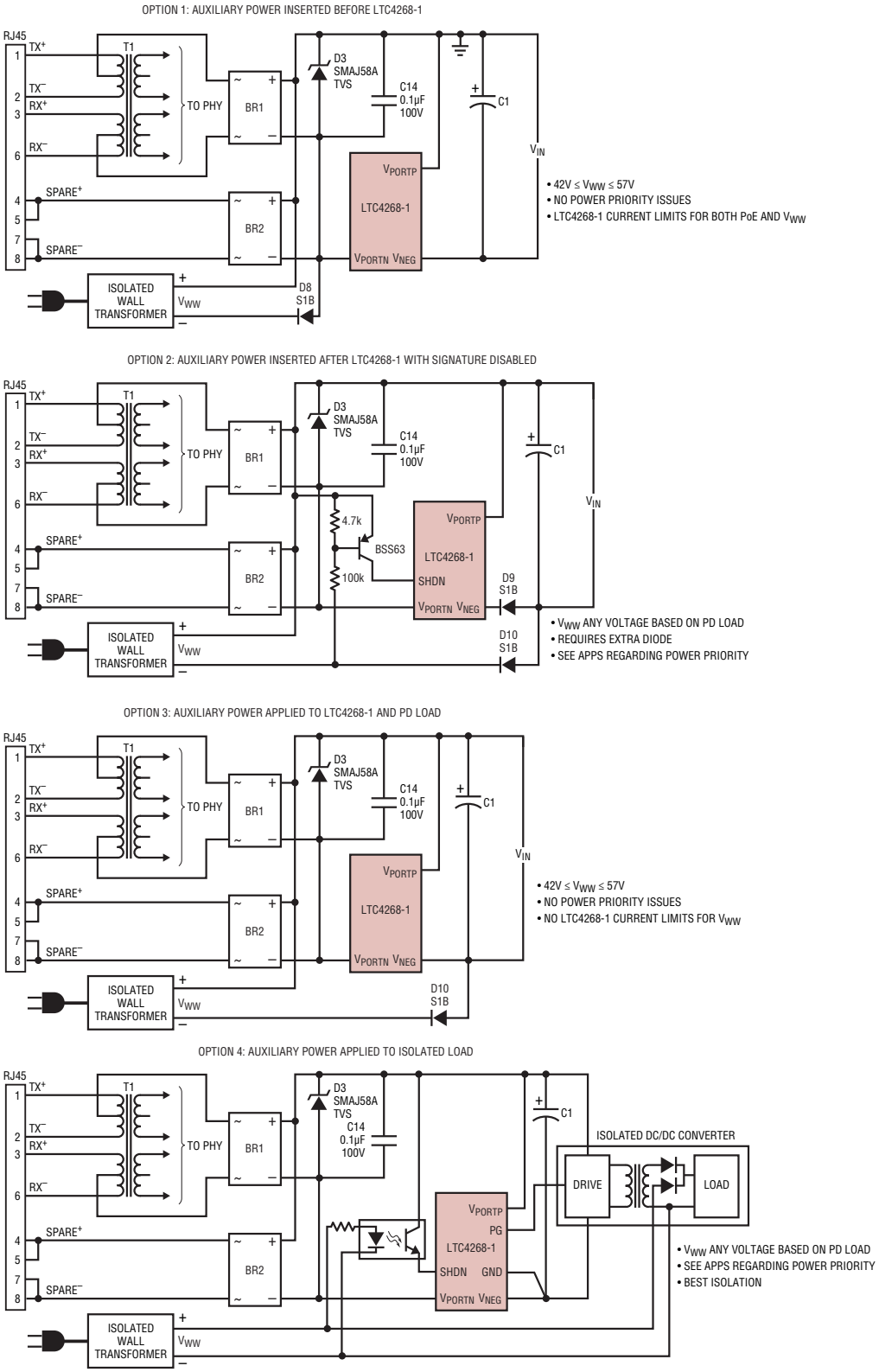

Figure 10. Interfacing Auxiliary Power Source to the PD

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to the PSE power. The PD will draw power from the PSE while the adapter will remain unused. This configuration is acceptable in a typical PoE system. However, if the adapter voltage is higher than the PSE voltage, the PD will draw power from the adapter. In this situation, it is necessary to address the issue of power cycling that may occur if a PSE is present. The PSE will detect the PD and apply power. If the PD is being powered by the adapter, then the PD will not meet the minimum load requirement and the PSE may subsequently remove power. The PSE will again detect the PD and power cycling will start. With an adapter voltage above the PSE voltage, it is necessary to either disable the signature as shown in option 2, or install a minimum load on the output of the LTC4268-1 to prevent power cycling. A 3k, 1W resistor connected between V_{PORTP} and V_{NEG} will present the required minimum load.

Option 3 applies power directly to the DC/DC converter bypassing the LTC4268-1 and omitting diode D9. With the diode omitted, the adapter voltage is applied to the LTC4268-1 in addition to the DC/DC converter. For this reason, it is necessary to ensure that the adapter maintain the voltage between 42V and 57V to keep the LTC4268-1 in its normal operating range. The third option has the advantage of corrupting the 25k signature resistance when the external voltage exceeds the PSE voltage and thereby solving the power priority issue.

Option 4 bypasses the entire PD interface and injects power at the output of the low voltage power supply. If the adapter output is below the low voltage output there are no power priority issues. However, if the adapter is above the internal supply, then option 4 suffers from the same power priority issues as option 2 and the signature should be disabled or a minimum load should be installed. Shown in option 4 is one method to disable to the signature while maintaining isolation.

If employing options 1 through 3, it is necessary to ensure that the end-user cannot access the terminals of the auxiliary power jack on the PD since this would compromise IEEE 802.3af isolation requirements and may violate local safety codes. Using option 4 along with an isolated power supply addresses the isolation issue and it is no longer necessary to protect the end-user from the power jack.

The above power cycling scenarios have assumed the PSE is using DC disconnect methods. For a PSE using AC disconnect, a PD with less than minimum load will continue to be powered.

Wall adapters have been known to generate voltage spikes outside their expected operating range. Care should be taken to ensure no damage occurs to the LTC4268-1 or any support circuitry from extraneous spikes at the auxiliary power interface.

Classification Resistor Selection (R_{CLASS})

The IEEE 802.3af specification allows classifying PDs into four distinct classes with class 4 being reserved for future use (Table 2). The LTC4268-1 supports all IEEE classes and implements an additional Class 5 for use in custom PoE applications. An external resistor connected from R_{CLASS} to V_{PORTN} (Figure 6) sets the value of the load current. The designer should determine which class the PD is to advertise and then select the appropriate value of R_{CLASS} from Table 2. If a unique load current is required, the value of R_{CLASS} can be calculated as:

$$R_{CLASS} = 1.237V/(I_{LOAD} – I_{IN\_CLASS})$$

I_{IN_CLASS} is the LTC4268-1 IC supply current during classification given in the electrical specifications. The R_{CLASS} resistor must be 1% or better to avoid degrading the overall accuracy of the classification circuit. Resistor power dissipation will be 100mW maximum and is transient so heating is typically not a concern. In order to maintain loop stability, the layout should minimize capacitance at the R_{CLASS} node. The classification circuit can be disabled by floating the R_{CLASS} pin. The R_{CLASS} pin should not be shorted to V_{PORTN} as this would force the LTC4268-1 classification circuit to attempt to source very large currents. In this case, the LTC4268-1 will quickly go into thermal shutdown.

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Power Good Interface

The LTC4268-1 provides complimentary power good signals to simplify the DC/DC converter interface. Using the power good signal to delay converter operation until the load capacitor is fully charged is recommended as this will help ensure trouble free start-up.

The active high PWRGD pin is controlled by an open collector transistor referenced to V_{NEG} while the active low $\overline{PWRGD}$ pin is controlled by a high voltage, open-drain MOSFET referenced to V_{PORTN}. The PWRGD pin is designed to interface directly to the UVLO pin with the aid of a pull-up resistor to Vcc. An example interface circuit is shown in Figure 11.

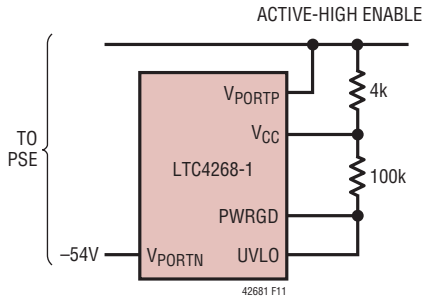

Figure 11. Power Good Interface Example

Port Voltage Lockout

PoE applications require the PD interface to turn on below 42V and turn off above 30V. The LTC4268-1 includes an internal port voltage lockout circuit to implement this basic chip on/off control. Additionally, the LTC4268-1 includes an enable/lockout function for the DC/DC converter that is controlled by the UVLO pin and is intended to be driven by PWRGD to ensure proper start-up. (Refer to Power Good Interface.) Users have the ability to implement higher turn-on voltages if necessary by connecting the UVLO pin to an external resistive divider between V_{PORTP} and V_{PORTN}. The UVLO pin also includes a bias current allowing implementation of hysteresis. When UVLO is below 1.24V, gate drivers are disabled and the converter sits idle. When the pin rises above the lockout threshold a small current is sourced out of the UVLO pin, increasing the pin voltage and thus creating hysteresis. As the pin voltage drops below this threshold, the current is disabled, further dropping the UVLO pin voltage. If not used, the UVLO pin can be disabled by tying to V_{CC}.

Shutdown Interface

To disable the 25k signature resistor, connect SHDN to the V_{PORTP} pin. Alternately, the SHDN pin can be driven high with respect to V_{PORTN}. Examples of interface circuits that disable the signature and all LTC4268-1 functions are shown in Figure 10, options 2 and 4. Note that the SHDN input resistance is relatively large and the threshold voltage is fairly low. Because of high voltages present on the printed circuit board, leakage currents from the V_{PORTP} pin could inadvertently pull SHDN high. To ensure trouble-free operation, use high voltage layout techniques in the vicinity of SHDN. If unused, connect SHDN directly to V_{PORTN}.

Load Capacitor

The IEEE 802.3af specification requires that the PD maintain a minimum load capacitance of 5µF. It is permissible to have a much larger load capacitor and the LTC4268-1 can charge very large load capacitors before thermal issues become a problem. However, the load capacitor must not be too large or the PD design may violate IEEE 802.3af requirements. If the load capacitor is too large, there can be a problem with inadvertent power shutdown by the PSE. For example, if the PSE is running at –57V (IEEE 802.3af maximum allowed) and the PD is detected and powered up, the load capacitor will be charged to nearly –57V. If for some reason the PSE voltage is suddenly reduced to –44V (IEEE 802.3af minimum allowed), the input bridge will reverse bias and the PD power will be supplied by the load capacitor. Depending on the size of the load capacitor and the DC load of the PD, the PD will not draw any power from the PSE for a period of time. If this period of time exceeds the IEEE 802.3af 300ms disconnect delay, the PSE will remove power from the PD. For this reason, it is necessary to evaluate the load current and capacitance to ensure that inadvertent shutdown cannot occur. Refer also to Thermal Protection in this data sheet for further discussion on load capacitor selection.

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MAINTAIN POWER SIGNATURE

In an IEEE 802.3af system, the PSE uses the maintain power signature (MPS) to determine if a PD continues to require power. The MPS requires the PD to periodically draw at least 10mA and also have an AC impedance less than 26.25k in parallel with 0.05µF. If either the DC current is less than 10mA or the AC impedance is above 26.25k, the PSE may disconnect power. The DC current must be less than 5mA and the AC impedance must be above 2M to guarantee power will be removed. The PD application circuits shown in this data sheet present the required AC impedance necessary to maintain power.

IEEE 802.3at Interoperability

In anticipation of the IEEE 802.3at standard release, the LTC4268-1 can be combined with a simple external circuit to be fully interoperable with an IEEE 802.3at-compliant PSE. For more information, please contact Linear Technology's Application Engineering.

SWITCHING REGULATOR OVERVIEW

The LTC4268-1 includes a current mode converter designed specifically for use in an isolated flyback topology employing synchronous rectification. The LTC4268-1 operation is similar to traditional current mode switchers. The major difference is that output voltage feedback is derived via sensing the output voltage through the transformer. This precludes the need of an opto-isolator in isolated designs greatly improving dynamic response and reliability. The LTC4268-1 has a unique feedback amplifier that samples a transformer winding voltage during the flyback period and uses that voltage to control output voltage. The internal blocks are similar to many current mode controllers. The differences lie in the feedback amplifier and load compensation circuitry. The logic block also contains circuitry to control the special dynamic requirements of flyback control. For more information on the basics of current mode switcher/controllers and isolated flyback converters see Application Note 19.

Feedback Amplifier—Pseudo DC Theory

For the following discussion refer to the simplified Flyback Amplifier diagram(Figure 12). When the primary side MOSFET switch MP turns off, its drain voltage rises above the V_{PORTP} rail. Flyback occurs when the primary MOSFET is off and the synchronous secondary MOSFET is on. During flyback the voltage on nondriven transformer pins is determined by the secondary voltage. The amplitude of this flyback pulse as seen on the third winding is given as:

$$V_{FLBK} = \frac{V_{OUT} + I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)}{N_{SF}}$$

$R_{DS(ON)}$ = on resistance of the synchronous MOSFET MS

I_{SEC} = transformer secondary current

ESR = impedance of secondary circuit capacitor, winding and traces

N_{SF} = transformer effective secondary-to-flyback winding turns ratio (i.e., N_S/N_{FLBK})

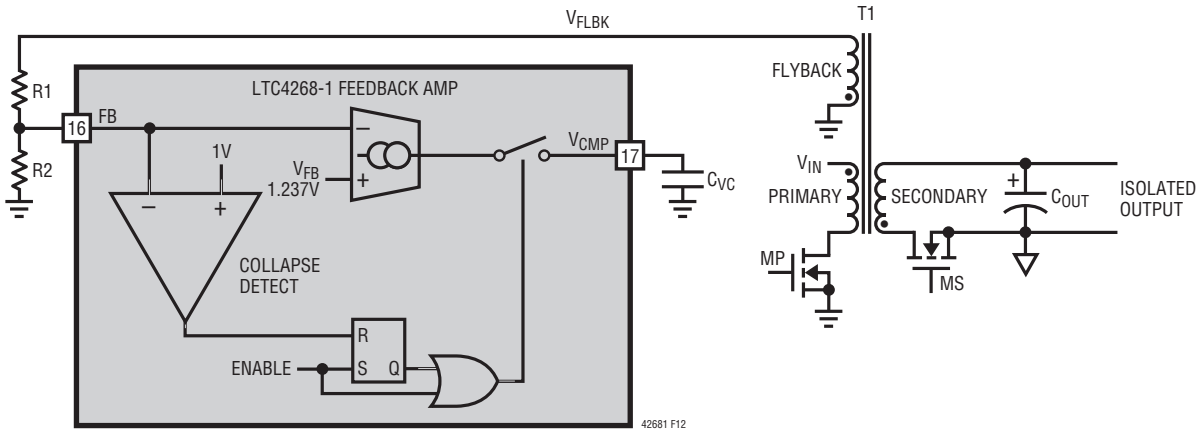

Figure 12. LTC4268-1 Switching Regulator Feedback Amplifier