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Hot Swap Controller with I²C Compatible Monitoring

FEATURES

- **Allows Safe Board Insertion Into Live Backplane**
- **12-/16-Bit ADC with ±0.7% Total Unadjusted Error**
- **Monitors Current, Voltage, Power and Energy**
- **Internal EEPROM for Nonvolatile Configuration**
- **Wide Operating Voltage Range: 2.9V to 33V**
- **I²C/SMBus Digital Interface (Coexists with PMBus Devices)**
- 12V Gate Drive for Lower MOSFET $R_{DS(ON)}$
- Programmable Current Limit with 2% Accuracy
- MOSFET Power Limiting with Current Foldback
- Continuously Monitors MOSFET Health
- Stores Minimum and Maximum Measurements
- Alerts When Alarm Thresholds Exceeded
- Reboots on I²C Command
- Input Overvoltage/Undervoltage Protection
- Three General Purpose Input/Outputs
- Internal ±5% or External Timebases
- 28-Pin 4mm × 5mm QFN Package

APPLICATIONS

- Enterprise Servers and Data Storage Systems
- Network Routers and Switches
- Base Stations
- Platform Management

DESCRIPTION

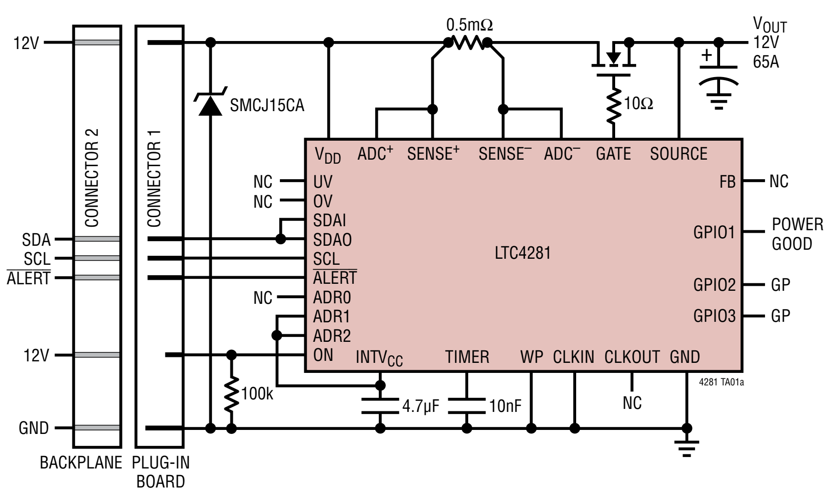
The LTC®4281 Hot Swap controller allows a board to be safely inserted and removed from a live backplane. Using an external N-channel pass transistor, board supply voltage and inrush current are ramped up at an adjustable rate. An I²C interface and onboard ADC allows for monitoring of board current, voltage, power, energy and fault status.

The device features analog foldback current limiting to limit the MOSFET power to a constant value. A wide input voltage operating range comfortably allows applications from 2.9V to 33V.

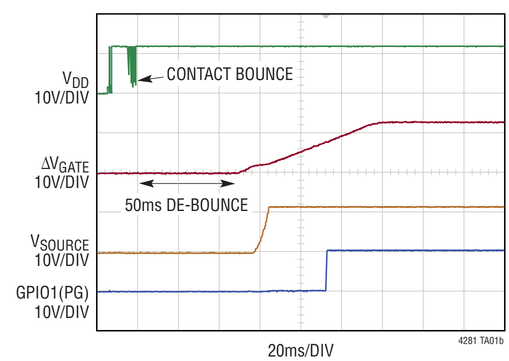
The LTC4281 is well suited to high power applications because the precise monitoring capability and accurate current limiting reduce the extremes in which both loads and power supplies must safely operate. Non-volatile configuration allows for flexibility in the autonomous generation of alerts and response to faults.

TYPICAL APPLICATION

12V, 65A Plug-In Board Resident Application



Start-Up Waveforms

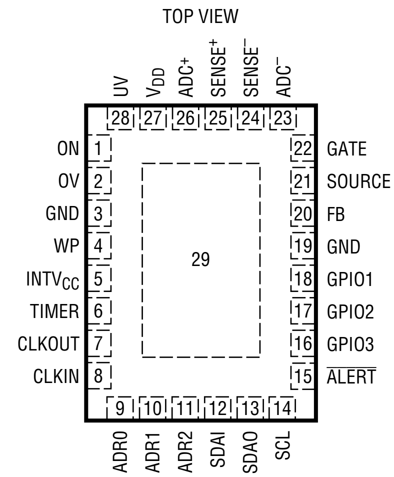


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage V_{DD} .... –0.3V to 45V
Input Voltages
GATE – SOURCE (Note 3) .... –0.3V to 10V
$SENSE^+$, ADC^+, $SENSE^–$ ...... V_{DD} – 4.5V to V_{DD} + 0.3V
$ADC^–$ .... –0.3V to V_{DD} + 0.3V
SOURCE .... –0.3V to 45V
ADR0-2, TIMER .... –0.3V to $INTV_{CC}$ + 0.3V
CLKIN. .... –0.3V to 5.5V
UV, OV, FB, WP, ON, GPIO1-3,
SCL, SDAI ....–0.3V to 45V
Output Voltages
GATE, GPIO1-3, $\overline{ALERT}$, SDAO .... –0.3V to 45V
CLKOUT .... –0.3 to $INTV_{CC}$ + 0.3V
Output Current $INTV_{CC}$ (V_{DD} > 4V) 25mA
Operating Ambient Temperature Range
LTC4281C .... 0°C to 70°C
LTC4281I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 125°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) PCB CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4281CUFD#PBF	LTC4281CUFD#TRPBF	4281	28-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4281IUFD#PBF	LTC4281IUFD#TRPBF	4281	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{DD}	Input Supply Range		●	2.9		33	V
I_{DD}	Input Supply Current		●		3.5	8	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	2.65	2.7	2.75	V
$V_{DD(HYST)}$	Input Supply Undervoltage Lockout Hysteresis		●	15	40	75	mV
$INTV_{CC}$	Internal Regulator Voltage		●	3.1	3.3	3.5	V
$INTV_{CC(UVL)}$	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising	●	2.45	2.6	2.7	V
$INTV_{CC(HYST)}$	$INTV_{CC}$ Undervoltage Lockout Hysteresis		●	50	110	175	mV
Current Limit							
ΔV_{SENSE}	Current Limit Voltage DAC Zero-Scale	V_{FB} = 1.3V, I_{LIM} = 000 V_{FB} = 0V, I_{LIM} = 000	● ●	12.25 3.4	12.5 3.75	12.75 4.1	mV mV
	Current Limit Voltage DAC Full-Scale	V_{FB} = 1.3V, I_{LIM} = 111 V_{FB} = 0V, I_{LIM} = 111	● ●	32.88 8.81	34.37 10.31	35.87 11.81	mV mV
	Current Limit Voltage DAC INL		●	–0.05	0	0.05	LSB
	Fast Current Limit Comparator Offset		●		0	±15	mV
I_{SENSE^-}	$SENSE^-$ Pin Input Current	V_{SENSE^-} = 12V	●		0	±1	µA
I_{SENSE^+}	$SENSE^+$ Pin Input Current	V_{SENSE^+} = 12V	●	0	90	130	µA
Gate Drive							
ΔV_{GATE}	Gate Drive (V_{GATE} – V_{SOURCE}) (Note 3)	V_{DD} = 2.9V to 33V, I_{GATE} = –1µA	●	10	12.5	13.5	V
I_{GATE}	Gate Pull-Up Current	Gate On, V_{GATE} = 0V	●	–15	–20	–30	µA
	Gate Pull-Down Current	Gate Off, V_{GATE} = 10V	●	0.5	1.3	3	mA
	Gate Fast Pull-Down Current	ΔV_{SENSE} =100mV, ΔV_{GATE} = 10V	●	0.3	0.9	3	A
$t_{PHL(FAST)}$	Overcurrent to GATE Low	ΔV_{SENSE} =0mV Step to 100mV, C = 10nF	●		0.5	1	µs
V_{GATE}	ΔV_{GATE} FET Off Threshold		●	5	8	10	V
Comparator Inputs							
I_{IN}	UV, OV, FB, ON WP Input Current	V = 1.2V	●		0	±1	µA
V_{TH-R}	V_{DD}, SOURCE Rising Threshold Voltages for UV, Power Good (Note 6)	5% 10% 15%	● ● ●	–5 –10 –15	–7.5 –12.5 –17.5	–10 –15 –20	% % %
V_{TH-F}	V_{DD}, SOURCE Falling Threshold Voltages for UV, Power Good (Note 6)	5% 10% 15%	● ● ●	–10 –15 –20	–12.5 –17.5 –22.5	–15 –20 –25	% % %
V_{TH-R}	V_{DD} Rising Threshold Voltages of OV (Note 6)	5% 10% 15%	● ● ●	10 15 20	12.5 17.5 22.5	15 20 25	% % %
V_{TH-F}	V_{DD} Falling Threshold Voltages of OV (Note 6)	5% 10% 15%	● ● ●	5 10 15	7.5 12.5 17.5	10 15 20	% % %
V_{TH}	UV, OV, FB, ON Rising Threshold		●	1.26	1.28	1.3	V
V_{HYST}	UV, OV, FB, ON Hysteresis		●	23	43	63	mV
V_{TH}	FET-Bad FAULT V_{DS} Threshold		●	150	200	270	mV
V_{TH}	WP Pin Threshold Voltage	Falling	●	1.26	1.28	1.3	V
V_{HYST}	WP Pin Hysteresis		●	2	20	35	mV
t_{PHL}	Turn-Off Propagation Delay	ON, UV, OV Turn-Off	●	10	25	45	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PHL}	Fast Turn On Propagation Delay	ON Pin Turn On	●	10	25	45	µs
t_D	Debounced Turn On Propagation Delay	UV, OV Turn On	●	45	50	55	ms
Crystal Oscillator							
V_{TH}	CLKIN Pin Rising Threshold		●	0.4	1	2	V
f_{MAX}	Maximum CLKIN Pin Input Frequency		●			25	MHz
I_{CLKIN}	CLKIN Pin Input Current	V = 0V to 3.3V	●	–10		10	µA
I_{CLKOUT}	CLKOUT Pin Output Current	V = 0V to 3.3V	●	–150		150	µA
GPIO Pin Functions							
V_{TH}	GPIO, $\overline{\text{ALERT}}$ Threshold	Falling	●	1.26	1.28	1.31	V
V_{HYST}	GPIO, $\overline{\text{ALERT}}$ Hysteresis		●	2	20	35	mV
V_{OL}	GPIO, $\overline{\text{ALERT}}$ Output Low Voltage	I = 3mA	●		0.3	0.4	V
I_{OH}	GPIO, $\overline{\text{ALERT}}$ Leakage Current	V = 33V	●		0	±1	µA
t_{PHL}	Stress Condition to GPIO2 Low Propagation Delay	GATE Low or V_{DS} = 1V	●	5	13	35	µs
TIMER Pin Functions							
V_{TH}	TIMER Low Threshold	Falling	●	0.11	0.15	0.19	V
	TIMER High Threshold	Rising	●	1.25	1.28	1.31	V
I_{TIMER}	TIMER Pull-Up Current	V = 0V	●	–18	–20	–22	µA
	TIMER Pull-Down Current	V = 1.3V	●	3	5	7	µA
Doc	Overcurrent Auto-Retry Duty Cycle		●	0.045	0.08	0.11	%
SOURCE, ADC Pin Currents							
I_{SOURCE}	SOURCE Input Current	V = 12V	●	70	180	350	µA
I_{ADC-}	ADC^- Input Current	V_{ADC-} = 33V	●		0	±1	µA
I_{ADC+}	ADC^+ Input Current	V_{ADC+} = 33V	●		25	110	µA
ADC							
RESOLUTION	ADC Resolution (No Missing Codes)		●	12/16			Bits
V_{OS}	ADC Offset Error, Percent of Full-Scale		●			±0.25	%
TUE	ADC Total Unadjusted Error (Note 5)	ΔV_{ADC}, SOURCE, V_{DD}, GPIO POWER ENERGY (Internal Timebase) ENERGY (Crystal/External Timebase)	● ● ● ●			±0.7 ±1.0 ±5.1 ±1.0	% % % %
FSE	ADC Full-Scale Error	ΔV_{ADC}, SOURCE, V_{DD}, GPIO POWER ENERGY (Internal Timebase) ENERGY (Crystal/External Timebase)	● ● ● ●			±0.7 ±1.0 ±5.1 ±1.0	% % % %
V_{FS}	ADC Full-Scale Range	$\Delta V_{ADC} = ADC^+ – ADC^-$ SOURCE/V_{DD} = 24V Range SOURCE/V_{DD} = 12V Range SOURCE/V_{DD} = 5V Range SOURCE/V_{DD} = 3.3V Range GPIO			40 33.28 16.64 8.32 5.547 1.28		mV V V V V V
INL	ADC Integral Nonlinearity, 12-Bit Mode		●		0.2	±5	LSB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FS}	Alarm Threshold Full-Scale Range (256 • V_{LSB})	ΔV_{ADC} SOURCE/V_{DD} = 24V SOURCE/V_{DD} = 12V SOURCE/V_{DD} = 5V SOURCE/V_{DD} = 3.3V GPIO			40 33.28 16.64 8.32 5.547 1.28		mV V V V V V
R_{GPIO}	GPIO ADC Sampling Resistance	V = 1.28V	●	1	2		MΩ
f_{CONV}	Conversion Rate	12-Bit Mode, Internal Clock 16-Bit Mode, Internal Clock	● ●	14.5 0.906	15.26 0.954	16 1	Hz Hz
I^2C Interface							
$V_{ADR(H)}$	ADR*n* Input High Threshold		●	$INTV_{CC}$ – 0.8	$INTV_{CC}$ – 0.5	$INTV_{CC}$ – 0.2	V
$I_{ADR(IN,Z)}$	ADR*n* Allowable Leakage in Open State		●			±3	µA
$V_{ADR(L)}$	ADR*n* Input Low Threshold		●	0.2	0.5	0.8	V
$I_{ADR(IN)}$	ADR*n* Input Current	ADR = 0V, ADR = $INTV_{CC}$	●			±80	µA
$V_{SDA,SCL(TH)}$	SDAI, SCL Input Threshold		●	1.5	1.7	2.0	V
$I_{SDA,SCL(OH)}$	SDAI, SCL Input Current	SCL, SDA = 5.0V	●			±1	µA
$V_{SDAO(OL)}$	SDAO, Output Low Voltage	I = 3mA	●		0.3	0.4	V
$I_{SDAO(OH)}$	SDAO, Pin Input Leakage Current	V_{SDAO} = 33V	●		0	±1	µA
I^2C Interface Timing							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●	400	1000		kHz
$t_{BUF(MIN)}$	Bus Free Time Between STOP/START Condition		●		0.12	1.3	µs
$t_{HD,STA(MIN)}$	Hold Time After (Repeated) START Condition		●		30	600	us
$t_{SU,STA(MIN)}$	Repeated START Condition Set-Up Time		●		30	600	ns
$t_{SU,STO(MIN)}$	STOP Condition Set-Up Time		●		140	600	ns
$t_{HD,DATI(MIN)}$	Data Hold Time (Input)		●		30	100	ns
$t_{HD,DATO}$	Data Hold Time (Output)		●	300	500	900	ns
$t_{SU,DAT(MIN)}$	Data Set-Up Time		●		30	600	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width		●	50	110	250	ns
C_X	SCL, SDA Input Capacitance	(Note 4)	●			10	pF
$t_{D(STUCK)}$	I^2C Stuck Bus Timeout		●	25	30	35	ms
EEPROM Characteristics							
Endurance		(Notes 7, 8)	●	10,000			Cycles
Retention		(Notes 7, 8)	●	20			Years
t_{WRITE}	Write Operation Time		●	1	2.2	4	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a minimum of 11V above SOURCE. Driving this pin to voltages beyond the clamp may damage the device.

Note 4: Guaranteed by design and not subject to test.

Note 5: TUE is the maximum ADC error for any code, given as a percentage of full scale.

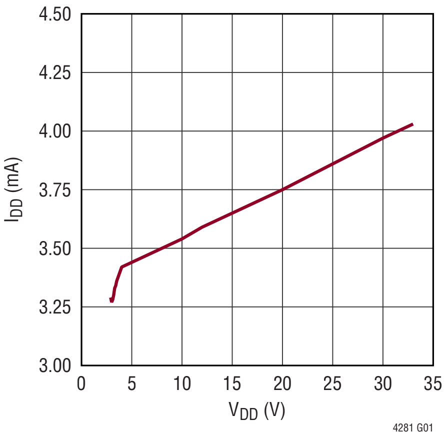
Note 6: UV, OV and FB internal thresholds are given as a percent difference from the configured operating voltage.

Note 7: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls.

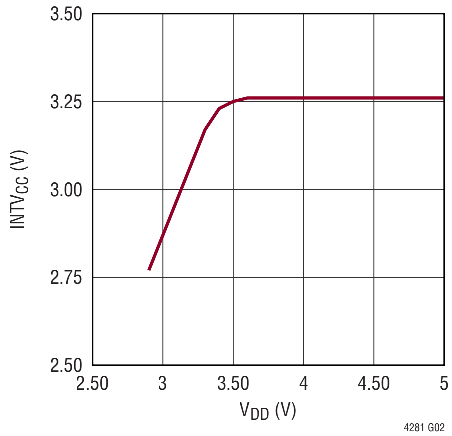
Note 8: EEPROM endurance and retention will be degraded when T_J > 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = 12V$ unless otherwise noted.

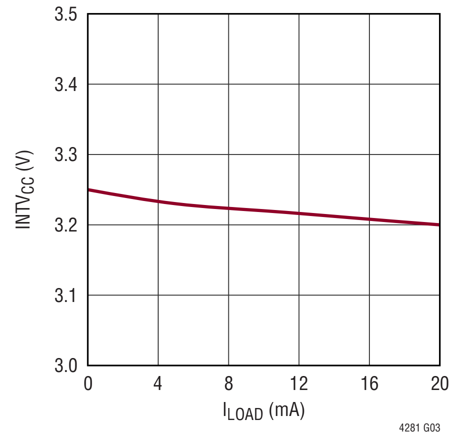
Supply Current vs Voltage



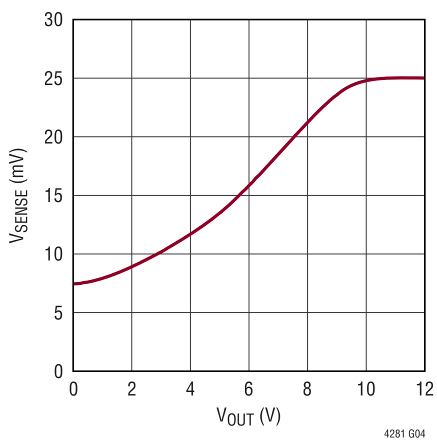
3.3V Output Supply vs Voltage



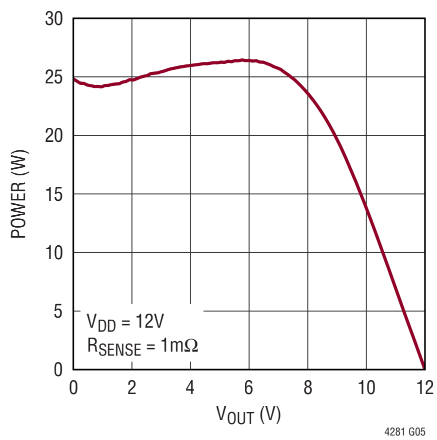
3.3V Output Supply vs Load Current for V_{DD} = 12V



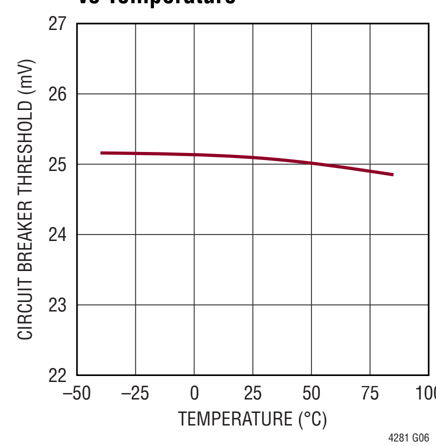
Current Limit Foldback Profile



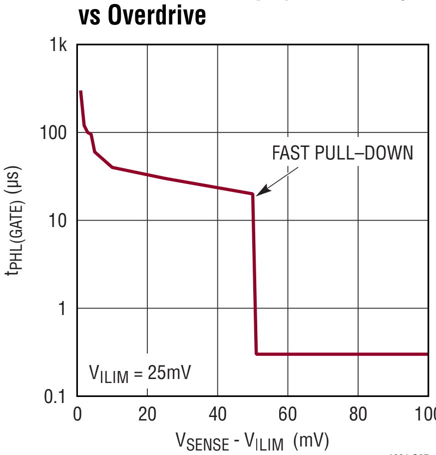
MOSFET Power Limit



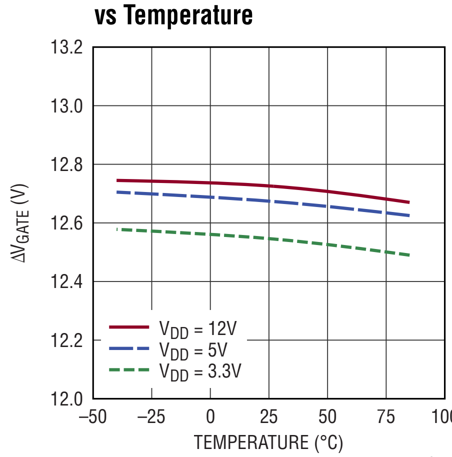
Current Limit Threshold vs Temperature



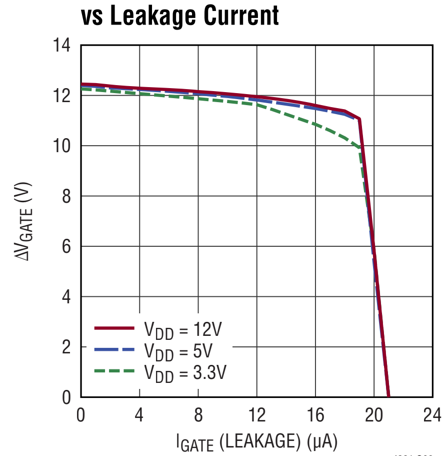
Current Limit Propagation Delay vs Overdrive



External MOSFET Gate Drive vs Temperature

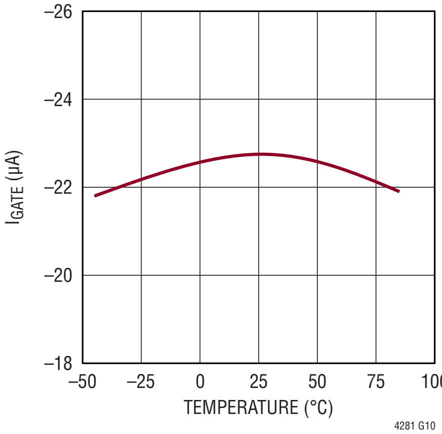


External MOSFET Gate Drive vs Leakage Current

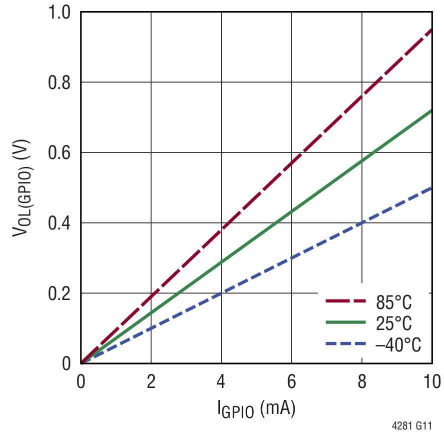


TYPICAL PERFORMANCE CHARACTERISTICS

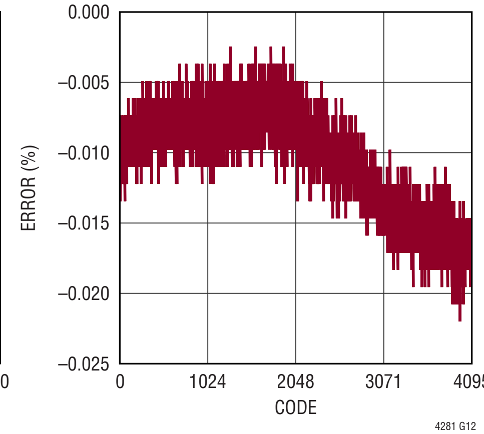
External MOSFET Gate Drive Current vs Temperature (I_{GATE} Current vs Temperature)



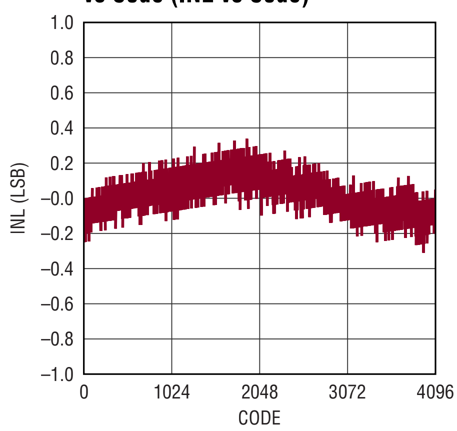
GPIO Pin Output Low Voltage vs Load ($V_{OL(GPIO)}$ vs I_{GPIO})



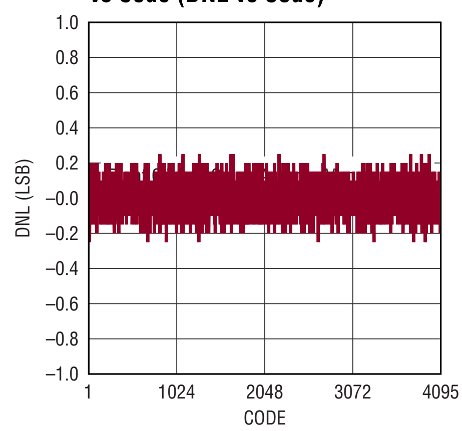
ADC Total Unadjusted Error vs Code (TUE vs Code)



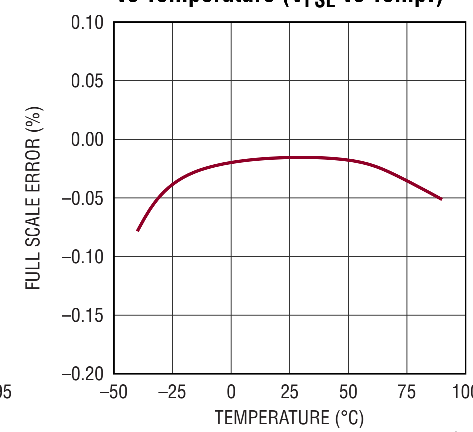
ADC Integral Non-Linearity vs Code (INL vs Code)



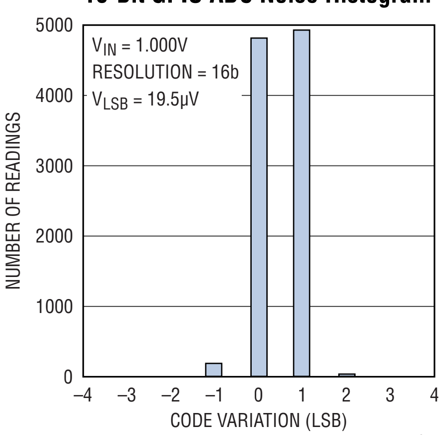
ADC Differential Non-Linearity vs Code (DNL vs Code)



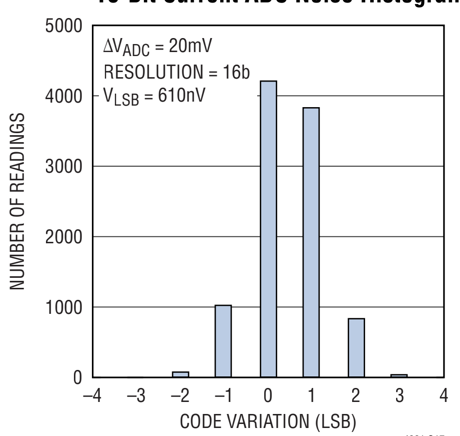
ADC Full-Scale Error vs Temperature (V_{FSE} vs Temp.)



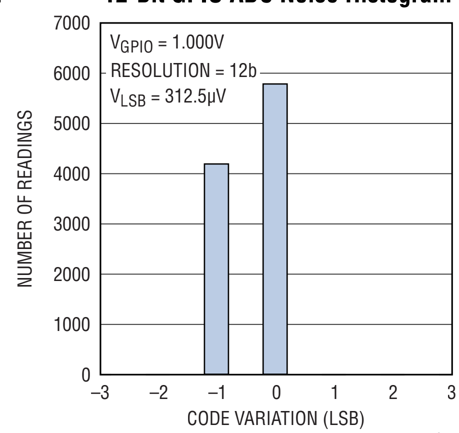
16-Bit GPIO ADC Noise Histogram



16-Bit Current ADC Noise Histogram



12-Bit GPIO ADC Noise Histogram



PIN FUNCTIONS

ADC⁺: Positive Kelvin ADC Current Sense Input. Connect this pin to the input side of the current sense resistor. Must be connected to the same trace as V_{DD} or a resistive averaging network which adds up to 1Ω to V_{DD}.

ADC⁻: Negative Kelvin ADC Current Sense Input. Connect this pin to the output of the current sense resistor or a resistive averaging network.

ADR0-ADR2: Serial Bus Address Inputs. Tying these pins to ground (L), open (NC), or $INTV_{CC}$ (H) configures one of 27 possible addresses. See Table 1 in the Applications Information section.

$\overline{\text{ALERT}}$: I^2C Bus $\overline{\text{ALERT}}$ Output or General Purpose Input/Output. Configurable to $\overline{\text{ALERT}}$ output, general purpose output or logic input. Tie to ground if unused.

CLKIN: Clock Input. Connect to an optional external crystal oscillator circuit or drive with an external clock. Tie to ground if unused.

CLKOUT: Clock Output. Connect to an optional external crystal oscillator circuit. Can be configured in non-volatile memory to output the internal clock or a low pulse when the ADC finishes a conversion. Float if unused.

FB: Foldback Current Limit and Power Good Input. A resistive divider from the output is tied to this pin. When the voltage at this pin drops below 1.28V, power is not considered good. The power bad condition may result in the GPIO1 pin pulling low or going high impedance depending on the configuration of GPIO_CONFIG register 0x07 bits 4 and 5, also a power bad fault is logged in this condition if the GATE pin is high. The start-up current limit folds back to 30% as the FB pin voltage drops from 1.3V to 0V.

GATE: Gate Drive for External N-Channel MOSFET. An internal 20μA current source charges the gate of the MOSFET. No compensation capacitor is required on the GATE pin, but a resistor and capacitor network from this pin to ground may be used to set the output voltage slew rate. During turn-off there is a 1mA pull-down current. During a short-circuit or undervoltage lockout (V_{DD} or $INTV_{CC}$), a 900mA pull-down between GATE and SOURCE is activated.

GND: Device Ground.

GPIO1: General Purpose Input/Open-Drain Output. Configurable to general purpose output, logic input, and power good or power bad signal. Tie to ground if unused.

GPIO2: General Purpose Input/Open-Drain Output. Configurable to general purpose output, logic input, MOSFET stress output, or data converter input. Tie to ground if unused.

GPIO3: General Purpose Input/ Open-Drain Output. Configurable to general purpose output, logic input, or data converter input. Tie to ground if unused.

$INTV_{CC}$: 3.3V Supply Decoupling Output. Connect a 1μF capacitor from this pin to ground. To ensure fault logging after power is lost a 4.7μF capacitor should be used. 25mA may be drawn from this pin to power 3.3V application circuitry. Increase capacitance by 1μF/mA external load if fault logging is used. This pin should not be driven and is not current limited.

ON: On Control Input. Used to monitor a connection sense pin on the backplane connector. The default polarity is high = on, but may be reconfigured to low = on by setting CONTROL1 register 0x00 bit 5 low. A on-to-off transition on this pin clears the fault register if CONTROL1 register 0x00 bit 7 is set high. The ON pin has a precise 1.28V threshold, allowing it to double as a supply monitor.

OV: Overvoltage Input Pin. An overvoltage condition is present when this pin is above the configured threshold. Connect a resistive divider when the internal divider is disabled, otherwise leave open.

SCL: Serial Bus Clock Input. Data at the SDA pin is shifted in or out on rising edges of SCL. This is a high impedance pin that is generally driven by an open-drain output from a master controller. An external pull-up resistor or current source is required.

SDAI: Serial Bus Data Input. A high impedance input for shifting in address, command or data bits. Normally tied to SDAO to form the SDA line.

PIN FUNCTIONS

SDAO: Serial Bus Data Output. Open-drain output for sending data back to the master controller or acknowledging a write operation. Normally tied to SDAI to form the SDA line. An external pull-up resistor or current source is required.

SENSE$^+$: Positive Kelvin Current Sense Input. Connect this pin to the input of the current sense resistor or an averaging network in the case of multiple sense resistors. The parallel resistance of an averaging network should not exceed 1Ω. Must operate at the same potential as V_{DD}.

SENSE$^–$: Negative Kelvin Current Sense Input. Connect this pin to the output of the current sense resistor. The current limit circuit controls the GATE pin to limit the sense voltage between the SENSE$^+$ and SENSE$^–$ pins to the value selected in the ILIM register or less.

SOURCE: N-Channel MOSFET Source and ADC Input. Connect to the source of the external N-channel MOSFET. This pin provides a return for the gate pull-down circuit and also serves as the ADC input to monitor the output voltage.

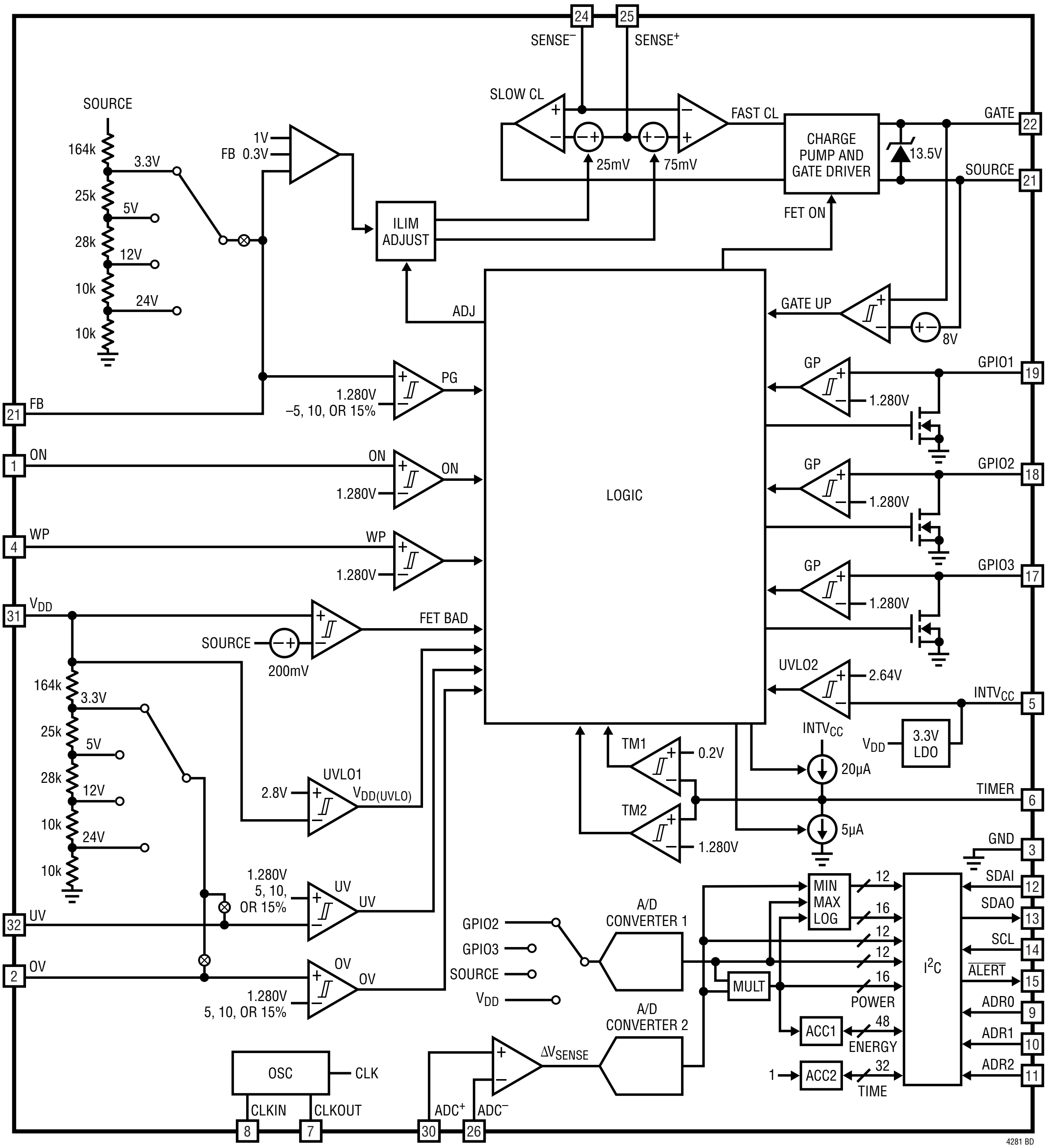
TIMER: Current Limit and Retry Timer Input. Connect a capacitor between this pin and ground to set a 64ms/µF duration for current limit, after which an overcurrent fault is logged and GATE is pulled low. The duration of the off time is 73s/µF when overcurrent auto-retry is enabled, resulting in a 0.08% duty cycle.

UV: Undervoltage Input. An undervoltage condition is present whenever this pin is below the configured threshold. Connect a resistive divider when the internal divider is disabled. A capacitor may be placed on this pin to filter brief UV glitches on the input supply.

V_{DD}: Supply Voltage Input and UV/OV Input. This pin has an undervoltage lockout threshold of 2.7V. The UV and OV thresholds are also measured at this pin, and the ADC may be configured to read the voltage at this pin.

WP: EEPROM Write Protect. All writes to the EEPROM except fault logging are blocked when WP is high.

FUNCTIONAL DIAGRAM



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OPERATION

The LTC4281 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. During normal operation, the gate driver turns on an external N-channel MOSFET to pass power to the load. The gate driver uses a charge pump that derives its power from the V_{DD} pin. Also included in the gate driver is 12.5V GATE-to-SOURCE clamp to protect the oxide of the external MOSFET. During start-up the inrush current is tightly controlled by using current limit foldback.

The current limit (CL) amplifier monitors the load current with a current sense resistor connected between the $SENSE^+$ and $SENSE^–$ pins. The CL amplifier limits the current in the load by pulling back on the GATE-to-SOURCE voltage in an active control loop when the sense voltage exceeds the commanded value.

An overcurrent fault at the output may result in excessive MOSFET power dissipation during active current limiting. To limit this power, the CL amplifier regulates the voltage between the $SENSE^+$ and $SENSE^–$ pins at the value set in the ILIM register. When the output (SOURCE pin) is low, power dissipation is further reduced by folding back the current limit to 30% of nominal.

The TIMER pin ramps up with 20µA when the current limit circuit is active. The LTC4281 turns off the GATE and registers a fault when the TIMER pin reaches its 1.28V threshold. At this point the TIMER pin ramps down using a 5µA current source until the voltage drops below 0.2V (comparator TM1). The TIMER pin will then ramp up and down 256 times with 20µA/5µA before indicating that the external MOSFET has cooled and it is safe to turn on again, provided overcurrent auto-retry is enabled.

The output voltage is monitored using the SOURCE pin and the power good (PG) comparator to determine if the power is available for the load. The power good condition can be signaled by the GPIO1 pin. The GPIO1 pin may also be configured to signal power bad, as a general purpose input (GP comparator), or a general purpose open-drain output.

GPIO2 and GPIO3 may also be configured as general purpose inputs or general purpose open-drain outputs. Additionally, the ADC measures these pins with a 1.28V full-scale. GPIO2 may be configured to pull low to indicate that the external MOSFET is in a state of stress when the MOSFET is commanded to be on and either the gate voltage is lower than it should be or the DRAIN-to-SOURCE voltage exceeds 200mV.

The Functional Diagram shows the monitoring blocks of the LTC4281. The group of comparators on the left side includes the undervoltage (UV), overvoltage (OV), and (ON) comparators. These comparators determine if the external conditions are valid prior to turning on the GATE. But first the two undervoltage lockout circuits, UVLO1 and UVLO2, validate the input supply and the internally generated 3.3V supply, $INTV_{CC}$. UVLO2 also generates the power-up initialization to the logic circuits and copies the contents of the EEPROM to operating memory after $INTV_{CC}$ crosses this rising threshold.

Included in the LTC4281 is a pair of 12 to 16-bit A/D converters. One data converter continuously monitors the ADC^+ to $ADC^–$ voltage, sampling every 16µs and producing a 12-bit result of the average current sense voltage every 65ms. The other data converter is synchronized to the first one and measures the GPIO voltage and SOURCE voltage during the same time period. Every time the ADCs finish taking a measurement, the current sense voltage is multiplied by the measurement of the SOURCE pin to provide a power measurement. Every time power is measured, it is added to an energy accumulator which keeps track of how much energy has been transmitted to the load. The energy accumulator can generate an optional alert upon overflow, and can be preset to allow it to overflow after a given amount of energy has been transmitted. A time accumulator also keeps track of how many times the power meter has been incremented; dividing the results of the energy accumulator by the time accumulator gives the average system power. The minimum and maximum measurements of GPIO, SOURCE, ADC^+ to $ADC^–$ and POWER are stored, and optional alerts may be generated if a measurement is above or below user configurable 8-bit thresholds.

An internal EEPROM provides nonvolatile configuration of the LTC4281's behavior, records fault information and provides four bytes of uncommitted memory for general purpose storage.

OPERATION

An I^2C interface is provided to read the A/D data registers. It also allows the host to poll the device and determine if faults have occurred. If the $\overline{ALERT}$ pin is configured as an $\overline{ALERT}$ interrupt, the host is enabled to respond to faults in real time. The I^2C device address is decoded using the ADR0-ADR2 pins. These inputs have three states each that decode into a total of 27 device addresses, as shown in Table 1.

APPLICATIONS INFORMATION

A typical LTC4281 application is a high availability system in which a positive voltage supply is distributed to power individual hot-swapped cards. The device measures card voltages and currents and records past and present fault conditions. The LTC4281 stores min and max ADC measurements, calculates power and energy, and can be configured to generate alerts based on measurement results, avoiding the need for the system to poll the device on a regular basis. The LTC4281 is configured with nonvolatile EEPROM memory, allowing it to be configured during board level testing and avoid having to configure the Hot Swap controller at every insertion.

A basic LTC4281 application circuit is shown in Figure 1. The following sections cover turn-on, turn-off and various faults that the LTC4281 detects and acts upon. External component selection is discussed in detail in the Design Example section.

Turn-On Sequence

The power supply on a board is controlled by using an N-channel pass transistor, Q1, placed in the power path. Resistor R_S senses current through Q1. Resistors R1, R2 and R3 define undervoltage and overvoltage levels. R4 prevents high frequency self-oscillations in Q1, capacitors C4 and C5 form a resonator network with crystal Y1 to provide an accurate time base.

Several conditions must be present before the external MOSFET turns on. First the external supply, V_{DD}, must exceed its 2.7V undervoltage lockout level. Next the internally generated supply, $INTV_{CC}$, must cross its 2.6V undervoltage threshold. This generates a 1ms power-on-reset pulse. During reset the fault registers are cleared and the control registers are loaded with the data held in the corresponding EEPROM registers.

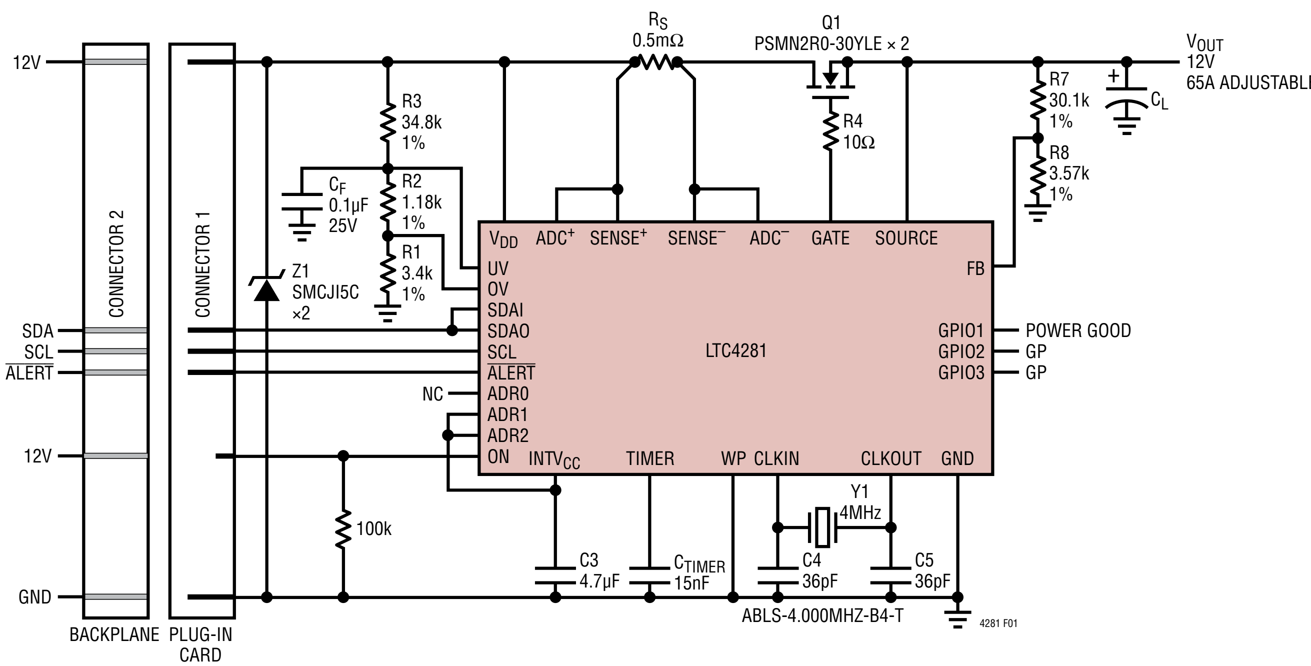

Figure 1. Typical Application

APPLICATIONS INFORMATION

After a power-on-reset pulse, the UV and OV pins verify that input power is within the acceptable range. The state of the UV and OV comparators is indicated by STATUS register 0x1E bits 1 and 2 and must be stable for at least 50ms to qualify for turn-on. The ON pin is checked to see that a connection sense (“short”) pin has asserted to the correct state. By default the ON pin has no delay, but a 50ms debounce delay may be added by setting CONTROL register 0x00 bit 6 high. When these conditions are satisfied, turn-on is initiated. Figure 4 shows connection sense configurations for both high- and low-going short pins. The ON pin has a precise 1.28V threshold, allowing it to also monitor a voltage through the short pin, such as a housekeeping or auxiliary supply delivered by the backplane. Use of the UV/OV divider for short pin detection in high current applications is not recommended, as voltage drops in the connector and fuse will impair the accuracy of the intended function.

The MOSFET is then turned on by charging up the GATE pin with a 20µA current source. When the GATE pin voltage reaches the MOSFET threshold voltage, the MOSFET begins to turn on and the SOURCE voltage then follows the GATE voltage as it increases.

While the MOSFET is turning on, the power dissipation in the MOSFET is limited to a fixed value by the current limit foldback profile as shown in Figure 2. As the SOURCE voltage rises, the FB pin follows as set by R7 and R8. Once the GATE pin crosses its 8V ΔV_{GATE} threshold and the FB pin has exceeded its 1.28V threshold, the GPIO1 pin (in its power good configuration) releases high to indicate power is good and the load may be activated.

At the minimum input supply voltage of 2.9V, the minimum GATE-to-SOURCE drive voltage is 10V. The GATE-to-SOURCE voltage is clamped below 13.5V to protect the gates of 20V N-channel MOSFETs. A curve of GATE-to-SOURCE drive (ΔV_{GATE}) versus V_{DD} is shown in the Typical Performance Characteristics.

Turn-Off Sequence

A normal turn-off sequence is initiated by card withdrawal when the backplane connector short pin opens, causing the ON pin to change state. Turn-off may be also initiated by writing a 0 to CONTROL register 0x00 bit 3. Additionally, several fault conditions turn off the GATE pin. These include an input overvoltage, input undervoltage, overcurrent or

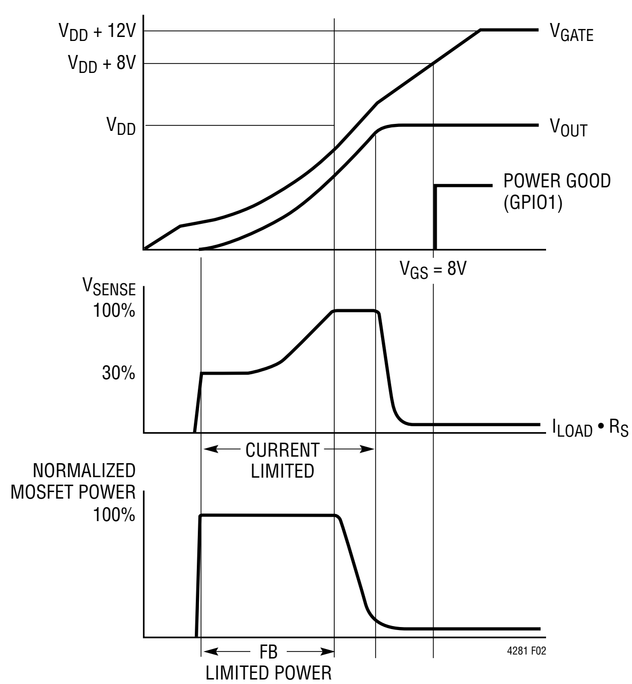

Figure 2. Power-Up Waveforms

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FET-BAD fault. Setting high any of the UV, OV , OC or FET-BAD fault bits (bits 0-2 and 6 of the FAULT_LOG register 0x04, also latches off the GATE pin if the associated auto-retry bits are set low.

The MOSFET is turned off with a 1mA current pulling down the GATE pin to ground. With the MOSFET turned off, the SOURCE and FB voltages drop as the load capacitance discharges. When the FB voltage crosses below its threshold, GPIO1 pulls low to indicate that the output power is no longer good if configured to indicate power good. If the V_{DD} pin falls below 2.66V for greater than 2µs or $INTV_{CC}$ drops below 2.49V for greater than 2µs, a fast shut down of the MOSFET is initiated. The GATE pin is then pulled down with a 900mA current to the SOURCE pin.

Current Limit Adjustment

The current limit sense voltage of the LTC4281 is adjustable between 12.5mV and 34.4mV in 3.1mV steps via the I^2C interface with bits 7-5 of the ILIM_ADJUST register 0x11. Default values are stored in the onboard EEPROM. This can be used to adjust the sense voltage to achieve a given current limit using the limited selection of standard sense resistor values available around 1mΩ. It also allows the LTC4281 to reduce available current for light loads or increase it in anticipation of a surge. This feature also enables the use of board trace as a sense resistors by trimming the sense voltage to match measured copper resistance during final test. The measured copper resistance may be written to the undedicated scratch pad area of the EEPROM so that it is available to scale ADC current measurements.

Current Limit Stability

For most applications the LTC4281 current limit loop is stable without additional components. However there are certain conditions where additional components may be needed to improve stability. The dominant pole of the current limit circuit is set by the capacitance at the gate of the external MOSFET, and larger gate capacitance makes the current limit loop more stable. Usually a total of 8nF GATE-to-SOURCE capacitance is sufficient for stability and is provided by inherent MOSFET C_{GS}. The stability of the loop is degraded by reducing the size of the resistor on a gate RC network if one is used, which may necessitate additional GATE-to-SOURCE capacitance. Board level short-circuit testing is highly recommended as board layout can also affect transient performance, the worst-case condition for current limit stability occurs when the output is shorted to ground after a normal start-up.

Parasitic MOSFET Oscillations

Not all circuit oscillations can be ascribed to the current limit loop. Some higher frequency oscillations can arise from the MOSFET itself. There are two possible parasitic oscillation mechanisms. The first type of oscillation occurs at high frequencies, typically above 1MHz. This high frequency oscillation is easily damped with gate resistor R4 as shown in Figure 1. In some applications, one may find that this resistor helps in short-circuit transient recovery as well. However, too large of a resistor will slow down the turn-off time. The recommended R4 range is between 5Ω and 500Ω. 10Ω provides stability without affecting turn-off time. This resistor must be located at the MOSFET package with no other components connected to the MOSFET gate pin.

A second type of parasitic oscillation occurs at frequencies between 200kHz and 800kHz when the MOSFET source is loaded with less than 10µF, and the drain is fed with an inductive impedance such as contributed by wiring inductance. To prevent this second type of oscillation load the source with more than 10µF and bypass the input supply with a 10Ω, 100nF snubber to ground.

Overcurrent Fault

The LTC4281 features an adjustable current limit with foldback that protects the MOSFET from excessive load current. To protect the MOSFET during active current limit, the available current is reduced as a function of the output voltage sensed by the FB pin such that the power dissipated by the MOSFET is constant. A graph in the Typical Performance Characteristics shows the current limit and power versus FB voltage.

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An overcurrent fault occurs when the current limit circuitry has been engaged for the MOSFET for longer than the time-out delay set by the TIMER capacitor. Current limiting begins when the current sense voltage between the $SENSE^+$ and $SENSE^–$ pins reaches the current limit level (which depends on foldback and the current limit configuration). The GATE pin is then pulled down and regulated in order to limit the current sense voltage to the current limit value. When the GATE pin regulator is in current limit, the circuit breaker time delay starts by charging the external timer capacitor from the TIMER pin with a 20µA pull-up current. If the TIMER pin reaches its 1.28V threshold, the external switch turns off with a 1mA current from GATE to ground. If the GATE pin stops current limiting before the TIMER pin reaches the 1.28V threshold, the TIMER pin will discharge with 5µA. For a given circuit breaker time delay, t_{CB}, the equation for setting the timing capacitor's value is as follows:

$$C_T = t_{CB} \bullet 0.016[\mu F/ms]$$

If an overcurrent fault is detected the MOSFET is turned off and the TIMER pin begins discharging with a 5µA pull-down current. When the TIMER pin reaches its 0.15V threshold, it will cycle up and down with 20µA and 5µA 256 times to allow the MOSFET time to cool down. When automatically retrying, the resulting overcurrent duty cycle is 0.08%. The final time the TIMER pin falls below its 0.15V lower threshold the switches are allowed to turn on again if the overcurrent auto-retry bit is set or the overcurrent fault bit has been reset by the I^2C interface.

The waveform in Figure 3 shows how the output turns off following a short circuit.

Overvoltage Fault

An overvoltage fault occurs when the OV pin rises above the OV threshold for longer than 15µs. This shuts off the GATE pin with a 1mA current to ground and sets the overvoltage present and overvoltage fault bits (Bit 0) in STATUS and FAULT_LOG registers 0x1E and 0x04. If the voltage subsequently falls back below the threshold for 50ms, the GATE pin is allowed to turn on again unless overvoltage auto-retry has been disabled by clearing the OV auto-retry bit (Bit 0) in CONTROL register 0x00. If an external resistive divider is used, the OV threshold is 1.28V on the OV pin. When using the internal dividers the OV threshold is referenced to the V_{DD} pin.

Undervoltage Fault

An undervoltage fault occurs when the UV pin falls below its 1.28V threshold for longer than 15µs. This shuts off the GATE pin with a 1mA current to ground and sets the undervoltage present and undervoltage fault bits (Bit 0) in STATUS and FAULT_LOG registers 0x1E and 0x04. If

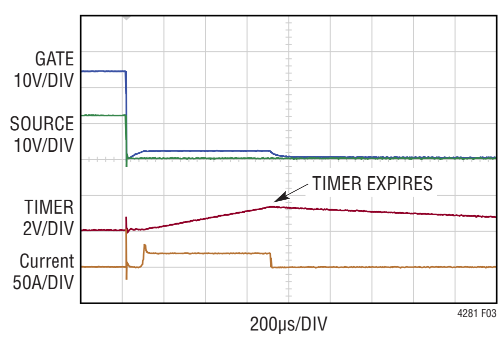

Figure 3. Short-Circuit Waveform

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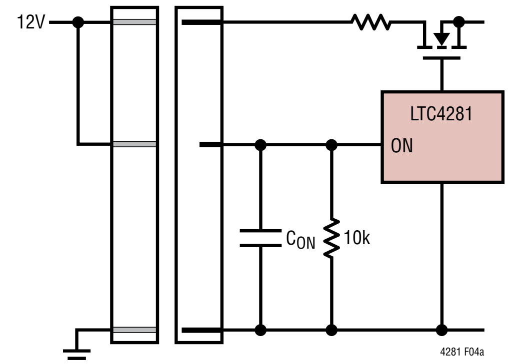
the voltage subsequently rises back above the threshold for 50ms, the GATE pin is allowed to turn on again unless undervoltage auto-retry has been disabled by clearing the UV auto-retry bit in CONTROL register 0x00. For the internal thresholds, the UV and OV signals may be filtered by placing a capacitor on the UV pin.

ON/OFF Control

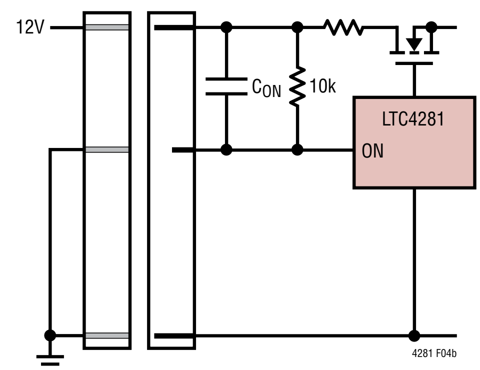
The ON pin can be configured active high or active low with CONTROL register 0x00 bit 5 (1 for active high). In the active high configuration it is a true ON input, in the active low configuration it can be used as an $\overline{\text{ENABLE}}$ input to detect card insertion with a grounded short pin. The delay from the ON pin commanding the part to turn on until the GATE pin begins to rise is set by CONTROL registers 0x00 bit 6. If this bit is low the GATE pin turns on immediately, and if it is high it turns on after a 50ms debounce delay. Whenever the ON pin toggles, bit 4 in FAULT_LOG register 0x04 is set to indicate a change of state and the other bits in FAULT register 0x04 are reset unless the ON_FAULT_MASK bit 7 in CONTROL register 0x00 is set.

The FET_ON bit, bit 3 of CONTROL register 0x00, is set or reset by the rising and falling edges of the ON pin and by I^{2}C write commands. When the LTC4281 comes out of UVLO the default state for bit 3 is read out of the EEPROM. If it is a 0, the part is configured to stay off after power-up and ignore the state of the ON pin. If it is a 1 the condition of the ON pin will be latched to bit 3 after the debounce period and the part will turn the GATE on if the ON pin is in the ON state.

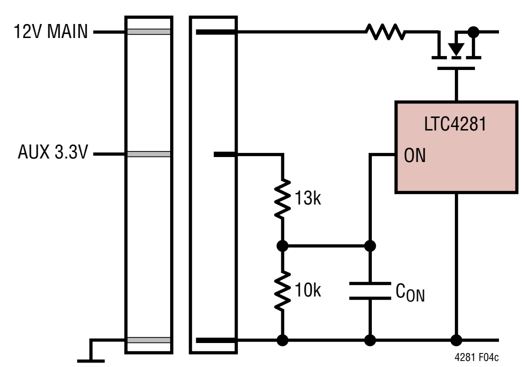
If the system shuts down due to a fault, it may be desirable to restart the system simply by removing and reinserting a load card. In cases where the LTC4281 and the switch reside on a backplane or midplane and the load resides on a plug-in card, the ON pin detects when the plug-in card is removed. Figure 4 shows an example where the ON pin is used to detect insertion. Once the plug-in card is reinserted the FAULT_LOG register 0x04 is cleared (except for bit 5,



(a) ON Configured Active High (Default) CONTROL Register 0x00 Bit 5=1



(b) ON Configured Active Low CONTROL Register 0x00 Bit 5=0



(c) ON Pin Sensing of AUX Supply ON Pin Configured Active High (Default)

Figure 4. Connection Sense Configurations with the ON Pin

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which indicates the ON pin changed state). After the ON pin turn-on delay, the system is allowed to start up again.

If a connection sense on the plug-in card is driving the ON pin, insertion or removal of the card may cause the pin voltage to bounce. This results in clearing the FAULT_LOG register when the card is removed. The pin may be debounced using a filter capacitor, C_{ON}, on the ON pin as shown in Figure 4. Note that the polarity of the ON pin is inverted with CONTROL Register 0x00 bit 5 set to 0.

FET-Bad Fault

In a Hot Swap application several things can prevent the MOSFET from turning on and reaching a low impedance state. A damaged MOSFET may have leakage from gate to drain or have degraded $R_{DS(ON)}$. Debris on the board may also produce leakage or a short from the GATE pin to the SOURCE pin, the MOSFET drain, or to ground. In these conditions the LTC4281 may not be able to pull the GATE pin high enough to fully enhance the MOSFET, or the MOSFET may not reach the intended $R_{DS(ON)}$ when the GATE pin is fully enhanced. This can put the MOSFET in a condition where the power in the MOSFET is higher than its continuous power capability, even though the current is below the current limit. The LTC4281 monitors the integrity of the MOSFET in two ways, and acts on both of them in the same manner.

First, the LTC4281 monitors the voltage between the MOSFET V_{DD} and SOURCE pins. The LTC4281 has a comparator that detects a bad DRAIN-to-SOURCE voltage (V_{DS}) whenever the V_{DS} is greater than 200mV.

Second, the LTC4281 monitors the GATE voltage. The GATE voltage may not fully enhance with a damaged MOSFET, and a severely damaged MOSFET most often has GATE, DRAIN and SOURCE all shorted together. If the LTC4281 is in the ON state, but the GATE pin does not come up to its 8V threshold above SOURCE, a FET-bad condition is detected.

When either FET-bad condition is present while the MOSFET is commanded on, an internal FET-bad fault timer starts. When the timer reaches the threshold set in FET_BAD_FAULT_TIME register 0x06 (1ms per LSB for a maximum of 255ms), a FET-bad fault condition is set, the part turns off, and the GATE pin is pulled low with a 1mA current. In the case of a GAIN-to-DRAIN short, it may be impossible for the LTC4281 to turn off the MOSFET. In this case the LTC4281 can be configured to signal power-bad to the load so the load goes into a low current state and send a FET-bad fault alert to the controller that may be able to shut down upstream supplies and/or flag the card for service.

The LTC4281 treats a FET-bad fault similar to an overcurrent fault, and will auto-retry after 256 timer cycles if the overcurrent auto-retry bit is set. Note that during start-up, the FET-bad condition is present because the voltage from DRAIN to SOURCE is greater than 200mV and the GATE pin is not fully enhanced, thus the FET-bad timeout must be long enough to allow for the largest allowable load to start up. FET-bad faults are disabled by setting the FET_BAD_FAULT_TIMER value to 0x00.

FET Short Fault

A FET short fault is reported if the data converter measures a current sense voltage greater than or equal to 0.25mV while the GATE pin is turned off. This condition sets the FET_SHORT bit 5 in status register 0x1E, and FET_SHORT_FAULT bit 5 in fault register 0x04.

Power-Bad Fault

The POWER_GOOD status bit, bit 3 in STATUS register 0x1E, is set when the FB pin voltage rises above its 1.28V threshold. To indicate POWER_GOOD on the GPIO1 pin, the GATE pin must first exceed the 8V V_{GS} thresholds after start-up, this requirement prevents POWER_GOOD from asserting during start-up when the FB pin first crosses its

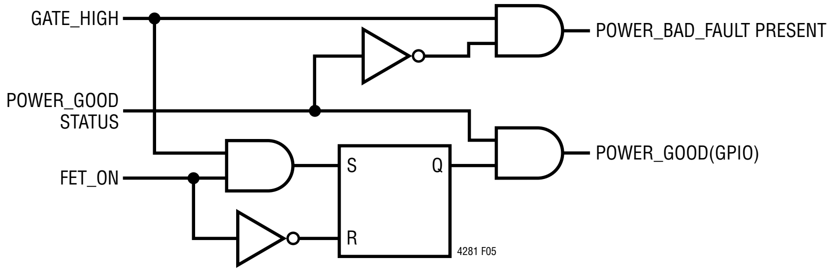

Figure 5. POWER_GOOD Logic

threshold. After start-up the GPIO1 pin will output the value of the FB comparator so that POWER_GOOD stays high even in cases such as an input voltage step that causes the GATE pins to briefly dip below 8V V_{GS}. See Figure 5.

A power bad fault is generated when the FB pin is low and the GATE pin is high, preventing power-bad faults during power-up or power-down.

Fault Alerts

A fault condition sets the corresponding fault bit in FAULT_LOG register 0x04, ADC_ALERT_LOG register 0x05, and TIMER_OVERFLOW_PRESENT (Bit 1) and METER_OVERFLOW_PRESENT (Bit 2) in the STATUS register 0x1F. Fault bits are reset by writing a 0 and the overflow status bits are reset by resetting the energy meter by setting and resetting ADC_CONTROL register 0x1D bit 6. A fault condition can also generate an alert ($\overline{\text{ALERT}}$ asserts low) by setting the corresponding bit in the alert mask registers: ALERT registers 0x02 and 0x03, and GPIO_CONFIG register bit 0. A low on $\overline{\text{ALERT}}$ may be generated upon completion of an ADC measurement by setting bit 2 in the GPIO_CONFIG register 0x07. This condition does not have a corresponding fault bit. Faults with enabled alerts set bit 7 in the ALERT_CONTROL register 0x1C, which controls the state of the $\overline{\text{ALERT}}$ pin. Clearing this bit will cause the $\overline{\text{ALERT}}$ pin to go high and setting this bit causes it to go low. Alert masking stored in EEPROM is transferred into registers at power up.

After the bus master controller broadcasts the Alert Response Address, the LTC4281 responds with its address on the SDA line and releases $\overline{\text{ALERT}}$ as shown in Figure 16. If there is a collision between two LTC4281s responding with their addresses simultaneously, then the device with the lower address wins arbitration and releases its $\overline{\text{ALERT}}$ pin. The devices that lost arbitration will still hold the $\overline{\text{ALERT}}$ pin low and will respond with their addresses and release $\overline{\text{ALERT}}$ as the I^2C master broadcasts additional Alert Response protocols until $\overline{\text{ALERT}}$ is release by all devices. The $\overline{\text{ALERT}}$ pin can also be released by clearing ALERT_CONTROL bit 7 in register 0x1C with the I^2C interface.

The $\overline{\text{ALERT}}$ pin can also be used as a GPIO pin, which pulls low by setting ALERT_CONTROL bit 6 in register 0x1C. The $\overline{\text{ALERT}}$ pin input status is located in STATUS register 0x1F bit 4.

Once the $\overline{\text{ALERT}}$ signal has been released from a fault, it will pull low again if the corresponding fault reoccurs, but not if the fault remains continuously present.

Resetting Faults in FAULT_LOG

The faults in FAULT_LOG register 0x04 may cause the part to latch off if their corresponding auto-retry bits are not set. In backplane resident applications it is desirable to latch off if a card has produced a failure and start up normally if the card is replaced. To allow this function the ON pin must be used as a connection sense input. When

APPLICATIONS INFORMATION

CONTROL bit 7 in register 0x00 is not set, a turn-off signal from the ON pin (card removed) will clear the FAULT_LOG register except for bit 4 (ON changed state). The entire FAULT_LOG register also cleared when the $INTV_{CC}$ pin falls below it's 2.49V threshold (UVLO), and individual bits may be cleared manually via the I^2C interface. Note that faults that are still present, as indicated in STATUS register 0x1E, cannot be cleared.

The FAULT_LOG register is not cleared when auto-retrying. When auto-retry is disabled the existence of a logged fault keeps the MOSFET off. As soon as the FAULT_LOG is cleared, the MOSFET turns on. If auto-retry is enabled, then a high status bit keeps the MOSFET off and the FAULT_LOG bit is ignored. Subsequently, when the FAULT_LOG bit is cleared by removal of the fault condition, the MOSFET is allowed to turn on again even though the fault bit remains set as a record of the previous fault condition.

Reboot

The LTC4281 features a reboot command bit, located in bit 7 of ADC_CONTROL register 0x1D. Setting this bit will cause the LTC4281 to reset and copy the contents of the EEPROM to operating memory the same as after initial power-up. The 50ms debounce before the part restarts is lengthened to 3.2s for reboot in order to allow load capacitance to discharge and reset before the LTC4281 turns back on. On systems where the Hot Swap controller supplies power to the I^2C master, this allows the master to issue a command that power cycles the entire board, including itself.

Data Converters

The LTC4281 incorporates a pair of sigma-delta A/D converters that are configurable to 12 or 16 bits. One converter continuously samples the current sense voltage, while the other monitors the input/output voltage and the voltage on a GPIO input. The sigma-delta architecture inherently averages signal noise during the measurement period.

The data converters may be run in a 12-bit or 16-bit mode, as selected by bit 1 in ILIM_ADJUST register 0x11. The second data converter may be configured to measure V_{IN} at the V_{DD} pin or V_{OUT} at the SOURCE pin by setting bit 3, and can select between measuring GPIO2 or GPIO3 with bit 2. The data converter full-scale is 40mV for the current sense voltage, a choice of 33.28V, 16.64V, 8.32V or 5.547V for V_{DD} and V_{SOURCE}, and 1.28V for GPIO.

The ADC^+ and $ADC^–$ pins allow the ADC to measure the voltage across the sense resistor. Some applications may use two or more sense resistors in parallel to limit the power in each resistor or achieve a specific parallel resistance or tolerance unavailable in a single sense resistor. In this case averaging resistors can be used to accurately measure the current by choosing averaging resistors with the same ratio as the sense resistors they connect to. See Figure 6. In this case the effective ADC sense resistor is R_S in parallel with $k \bullet R_S$ for the current limit. Scaling the averaging resistors, R_A, by the same scaling factor, k, allows the ADC to measure the correct sense voltage for this effective sense resistor. The smallest averaging resistor should not exceed 1Ω.

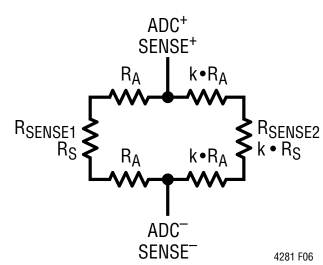

Figure 6. Weighted Averaging Sense Voltages

The two data converters are synchronized, and after each current measurement conversion, the measured current is multiplied by the measured V_{DD} or V_{SOURCE} to yield input or output power. After each conversion the measurement results and power are compared to the recorded min and max values. If the measurement is a new min or max, then

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those registers are updated. The measurements are also compared to the min/max alarm thresholds in registers 0x08 to 0x0F and will set the corresponding ADC alert bit in ADC_ALERT_LOG register 0x05 and generate an alert if configured to do so in ALERT register 0x03.

After each measurement, calculated power is added to an accumulator that meters energy. Since the current is continuously monitored by a dedicated ADC, the current is sampled every 16µs, ensuring that the energy meter will accurately meter noisy loads up to 62.5kHz noise frequency. The 6-byte energy meter is capable of accumulating 20 days of power at full scale, which is several months at a nominal power level. An optional alert may be generated when the meter overflows. To measure coulombs, the energy meter may be configured to accumulate current rather than power by setting CLK_DIVIDER register 0x10 bit 7.

A time counter keeps track of how many times power has been added into the energy meter. Dividing the energy by the number in the counter will yield the average power over the accumulated interval. When metering coulombs dividing the metered charge by the counter produces the average current over the accumulation interval. The 4-byte time counter will keep count for 10 years in the 12-bit mode before overflowing, and can generate an alert at full scale to indicate that the counter is about to roll over. Multiplying the value in the counter by t_{CONV} yields the time that the energy meter has been accumulating.

Both the energy accumulator and time counter are writable, allowing them to be pre-loaded with a given energy and/or time before overflow so that the LTC4281 will generate an overflow alert after either a specified amount of energy has been delivered or time has passed.

The following formulas are used to convert the values in the ADC result registers into physical units. The data in the 12-bit mode is left justified, so the same equations apply to the 12-bit mode and the 16-bit mode.

To calculate GPIO voltage:

$$V = \frac{CODE(word) \bullet 1.280}{2^{16} - 1}$$

To calculate input/output voltage:

$$V = \frac{CODE(word) \bullet V_{FS(OUT)}}{2^{16} - 1}$$

where $V_{FS(OUT)}$ is 33.28V, 16.64V, 8.32V or 5.547V depending on the part being in 24V, 12V, 5V or 3.3V mode, respectively.

To calculate current in amperes:

$$I = \frac{CODE(word) \bullet 0.040V}{\left(2^{16} - 1\right) \bullet R_{SENSE}}$$

To calculate power in watts:

$$P = \frac{CODE(word) \bullet 0.040V \bullet V_{FS(OUT)} \bullet 2^{16}}{\left(2^{16} - 1\right)^2 \bullet R_{SENSE}}$$

To calculate energy in joules:

$$E = \frac{CODE(48\ bits) \bullet 0.040V \bullet V_{FS(OUT)} \bullet t_{CONV} \bullet 2^{8}}{\left(2^{16} - 1\right)^2 \bullet R_{SENSE}}$$

To calculate coulombs:

$$C = \frac{CODE(48\ Bits) \bullet 0.040V \bullet t_{CONV}}{(2^{16} - 1) \bullet R_{SENSE}}$$

where t_{CON} = ($1/f_{CONV}$) is 0.065535s for 12-bit mode and 1.0486s for 16-bit mode.

To calculate average power over the energy accumulation period:

$$P(AVG) = \frac{E}{t_{CONV} \bullet CODE(COUNTER)}$$

$$I(AVG) = \frac{C}{t_{CONV} \bullet CODE(COUNTER)}$$

To calculate GPIO voltage alarm thresholds:

$$V = \frac{CODE(byte) \bullet 1.280}{255}$$

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To calculate input/output voltage alarm thresholds:

$$V_{ALARM} = \frac{CODE(byte) \cdot V_{FS(OUT)}}{255}$$

where $V_{FS(OUT)}$ is 33.28V, 16.64V, 8.32V or 5.5467V depending on the part being in 24V, 12V, 5V or 3.3V mode, respectively.

To calculate current alarm thresholds in amperes:

$$I = \frac{CODE(byte) \cdot 0.040V}{255 \cdot R_{SENSE}}$$

To calculate power alarm threshold in watts:

$$P = \frac{CODE(byte) \cdot 0.040V \cdot V_{FS(OUT)} \cdot 2^8}{R_{SENSE} \cdot 255 \cdot 255}$$

Note that falling alarm thresholds use CODE(byte)+1 in the above equations since they trip at the top edge of the code, which is 1LSB higher than the rising threshold.

CLKIN, CLKOUT: Crystal Oscillator/External Clock

Accurately measuring energy by integrating power requires a precise integration period. The on-chip clock of the LTC4281 is trimmed to 1.5% and specified over temperature to 5% and is invoked by grounding CLKIN. For increased accuracy a crystal oscillator or external precision clock may be used on the CLKIN and CLKOUT pins. A 4MHz crystal oscillator or resonator may be connected to the two CLK pins as shown in Figure 1.

Crystal oscillators are sensitive to noise and parasitic capacitance. Care should be taken in layout to minimize trace length between the LTC4281 and the crystal. Keep noisy traces away from the crystal traces, or shield the crystal traces with a ground trace.

Alternatively, an external clock may be applied to CLKIN with CLKOUT left unconnected. The LTC4281 can accept an external clock between 250kHz and 15.5MHz, with clocks faster than 250kHz reduced to 250kHz by a programmable divider, the clock frequency is divided by twice the value in CLK_DIVIDER register 0x10 bits 0-4. Code 00000 passes the clock through without division while code 01000 divides a 4MHz clock down to 250kHz. The divided external clock may differ from 250kHz by 5% without affecting other specifications.

Configuring the GPIO Pins

The LTC4281 has three GPIO pins and an $\overline{ALERT}$ pin, all of which can be used as general purpose input/output pins. The GPIO1 pin is configured using the GPIO_CONFIG register 0x07 bits 5-4. GPIO2 will pull low to indicate MOSFET stress if GPIO_CONFIG bit 1 is set and pulls low if bit 6 is low. GPIO3 pulls low if GPIO_CONFIG bit 7 is set and is otherwise high impedance. The $\overline{ALERT}$ pin can be used as a GPIO pin by setting all the alert enable bits to 0 to disable alerts, then setting bit 6 in ALERT_CONTROL register 0x1C. Bit 7 in ALERT_CONTROL can also be set to pull the $\overline{ALERT}$ pin low, but bit 7 will cause the part to respond to the alert response protocol, while bit 6 will not.

GPIO1-GPIO3 and $\overline{ALERT}$ all have comparators monitoring the voltage on these pins with a threshold of 1.28V when the pins are serving as outputs. The results may be read from the second byte of the STATUS register, 0x1F, bits 4-7.

Supply Transients

In card-resident applications, output short circuits working against the inductive nature of the supply can easily cause the input voltage to dip below the UV threshold.

In severe cases where the supply inductance is 500nH or more, the input can dip below the V_{DD} undervoltage lockout threshold of 2.66V. Because the current passing through the sense resistor changes no faster than a rate of V_{SUPPLY}/L_{SUPPLY}, such as 12V/500nH = 24A/μs, it is possible for the UV comparator and in particular, the V_{DD} UVLO circuit to respond before the current reaches the current limit threshold. The V_{DD} UVLO circuit responds after a 2μs filter delay, pulling the GATE pin to SOURCE with 900mA. Once the MOSFET turns off, V_{DD} will return

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to its nominal voltage and the part initiates a new startup sequence. The UV comparator responds after a 15μs filter delay, making it less likely that this path will engage before current limiting commences; adding a 100nF filter capacitor to the UV pin ensures this. The fast current limit amplifier engages at 3x the current limit threshold, and has a propagation delay of 500ns. If the supply inductance is less than 500nH in a 12V application, it is unlikely that the V_{DD} UVLO threshold will be breached and the fast di/dt rate allows the current to rise to the 3x level long before the UV pin responds.

Once the fast current limit amplifier begins to arrest the short-circuit current, the input voltage rapidly recovers and even overshoots its DC value. The LTC4281 is safe from damage up to 45V. To minimize spikes in backplane-resident applications, bypass the LTC4281 input supply with an electrolytic capacitor between V_{DD} and GND. In card-resident applications clamp the V_{DD} pin with a surge suppressor Z1, as shown in Figure 7.

Supply Transient Protection

The worst-case Z1 current is that which triggers the fast current limit circuit. Several 1500W surge suppressors may be required to clamp this current for high power applications. Many 20V to 30V MOSFETs enter avalanche breakdown before 45V. In those cases the MOSFET can act as a surge suppressor and protect the Hot Swap controller from inductive input voltage surges. In applications where a high current ground is not available to connect the surge suppressor, the surge suppressor may be connected from input to output, allowing the output capacitance to absorb spikes.

Design Example

As a design example, consider the following specifications: V_{IN} = 12V, I_{MAX} = 50A, C_L = 3300μF, $V_{UV(ON)}$ = 10.75V, $V_{OV(OFF)}$ = 14.0V, $V_{PWRGD(UP)}$ = 11.6V, and I^2C address = 1010011, with overcurrent threshold set to 25mV. This completed design is shown in Figure 7.

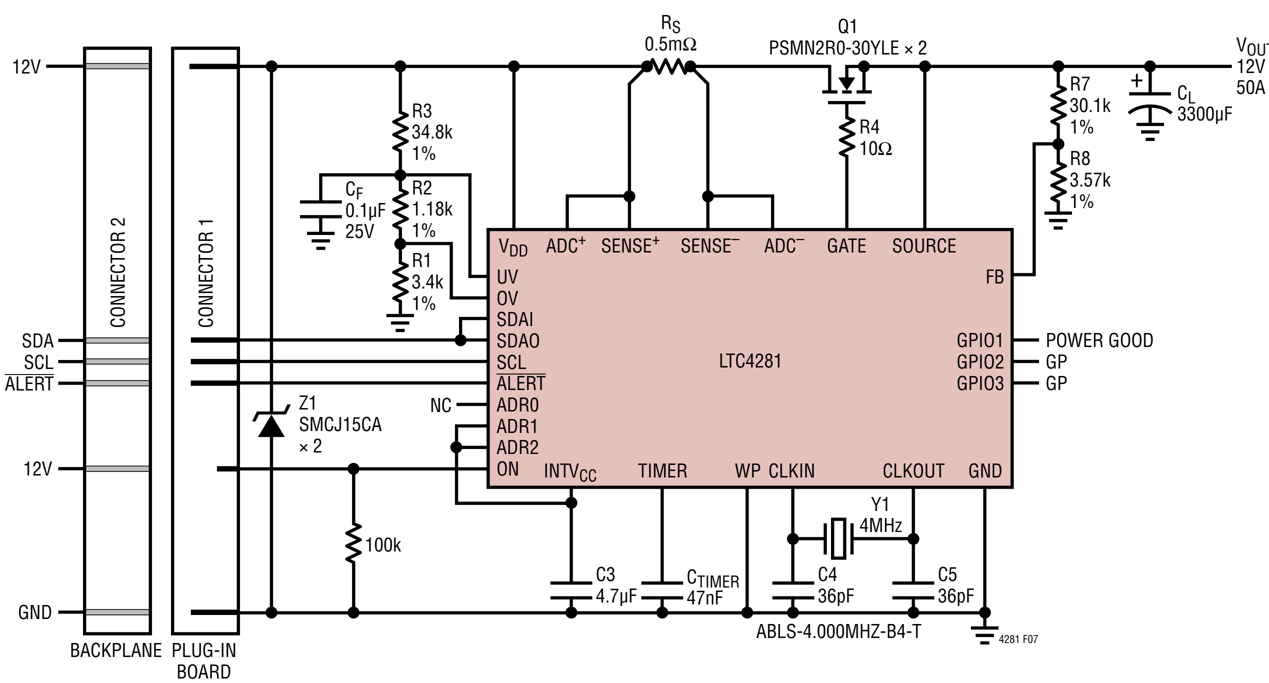

Figure 7. Design Example

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Selection of the sense resistor, R_S, is set by the current limit threshold of 25mV:

$$R_S = \frac{25mV}{I_{MAX}} = 0.5m\Omega$$

The MOSFET is sized to handle the power dissipation during inrush when output capacitor C_{OUT} is being charged.

A method to determine power dissipation during inrush is based on the principle that:

Energy in C_L = Energy in Q1

where:

$$\text{Energy in } C_L = \frac{1}{2}CV^2 = \frac{1}{2}(3.3mF)(12)^2 = 0.24J$$

During inrush, current limit foldback will limit the power dissipation in the MOSFET to:

$$P_{DISS} = \frac{7.5mV \bullet 12V}{R_S} = 180W$$

Calculate the time it takes to charge up C_{OUT}:

$$t_{STARTUP} = \frac{\text{Energy in } C_L}{P_{DISS}} = \frac{0.24J}{180W} = 1.33ms$$

The SOA (safe operating area) curves of candidate MOSFETs must be evaluated to ensure that the heat capacity of the package tolerates 180W for 1.33ms. The SOA curve of the NXP PSMN2R0-30YLE shows 200W for 80ms, satisfying this requirement. Additional MOSFETs in parallel may be required to keep the MOSFET temperature or power dissipation within limits at maximum load current. This depends on board layout, airflow and efficiency requirements. To get the maximum DC dissipation below 2W per MOSFET, a pair of PSMN2RO-30YLE is required for Q1. Since the PSMN2R0-30YLE has 10nF of gate capacitance it is likely to be stable, but the short-circuit stability of the current limit should be checked and improved by adding capacitors from GATE to SOURCE if needed.

For a start-up time of 1.33ms with a 2x safety margin we choose:

$$C_{TIMER} = 2 \bullet \frac{t_{STARTUP}}{64ms/\mu F} = 2 \bullet \frac{1.33ms}{64ms/\mu F} \cong 47nF$$

In the event that the circuit attempts to start up into a short circuit the current will be 30% of 50A, 15A, and the voltage across the MOSFET will be 12V which the MOSFET will carry for 1.33ms. This is within the SOA of the PSMN2R0-30YLE, so the application will safely survive this fault condition.

The UV and OV resistor string values can be solved in the following method. To keep the error due to 1µA of leakage to less than 1% choose a divider current of at least 200µA. R1 < 1.28V/200µA = 6.4kΩ. Then calculate the following equations:

$$R2 = \frac{V_{OV(OFF)}}{V_{UV(ON)}} \bullet R1 \bullet \frac{UV_{TH(RISING)}}{OV_{TH(FALLING)}} - R1$$

$$R3 = \frac{V_{UV(ON)} \bullet (R1 + R2)}{UV_{TH(RISING)}} - R1 - R2$$

In our case we choose R1 to be 3.4kΩ to give a resistor string current greater than 200µA. Then solving the equations results in R2 = 1.18kΩ and R3 = 34.8kΩ.

The FB divider is solved by picking R8 and solving for R7, choosing 3.57kΩ for R8 we get:

$$R7 = \frac{V_{PWRGD(UP)} \bullet R8}{FB_{TH(RISING)}} - R8$$

Resulting in R7 = 30.1kΩ.

Since this application uses external resistive dividers for UV, OV and FB, and the operating voltage is 12V, the CONTROL register 0x01 is set to 0x02 to disable the internal thresholds and set the ADC to the 12V range. The EEPROM CONTROL register 0x21 is also set to 0x02 so the part will boot in the proper configuration.

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Since the start-up time is 1.33ms, the FET_BAD_FAULT_TIME is set to 3ms for a ≥ 2x safety margin by writing 0x03 to the FET_BAD_FAULT_TIME register 0x06.

A 0.1µF capacitor, C_F, is placed on the UV pin to prevent supply glitches from turning off the GATE via UV or OV.

The address is set with the help of Table 1, which indicates binary address 1010011 (0xA6). Address 0xA6 is set by setting ADR2 high, ADR1 open and ADR0 high.

Next the value of R4 is chosen to be the default value of 10Ω as discussed in the Current Limit Stability section.

A 4MHz crystal is placed between the CLKIN and CLKOUT pins. The specified part requires 18pF load capacitance which is provided by C4 and C5. To generate an internal clock of 250kHz, 1000b is written to the CLOCK_DIVIDER register 0x10 to divide the 4MHz crystal frequency by 16.

Since the fast pull-down is engaged at 150A, the input TVS needs to be capable of clamping a 150A surge at a voltage above the OV threshold but below the 45V absolute maximum rating of the LTC4281 for about 1µs. The SMCJ15CA clamps 61.5A at 24V for 8.3ms, and can dissipate 30kW for 1µs. One SMCJ15CA will meet these requirements.

In addition a 4.7µF ceramic bypass capacitor is placed on the $INTV_{CC}$ pin. No bypass capacitor is required on the V_{DD} pin.

Layout Considerations

To achieve accurate current sensing, Kelvin connections are required. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/□. Small resistances add up quickly in high current applications.

To improve noise immunity, put the resistive dividers to the UV, OV and FB pins close to the device and keep traces to V_{DD} and GND short. It is also important to put the bypass capacitor C3 as close as possible between $INTV_{CC}$ and GND. A 0.1µF capacitor from the UV pin (and OV pin through resistor R2) to GND also helps reject supply noise. Figure 8 shows a layout that addresses these issues. Note that a surge suppressor, Z1, is placed between supply and ground using wide traces.

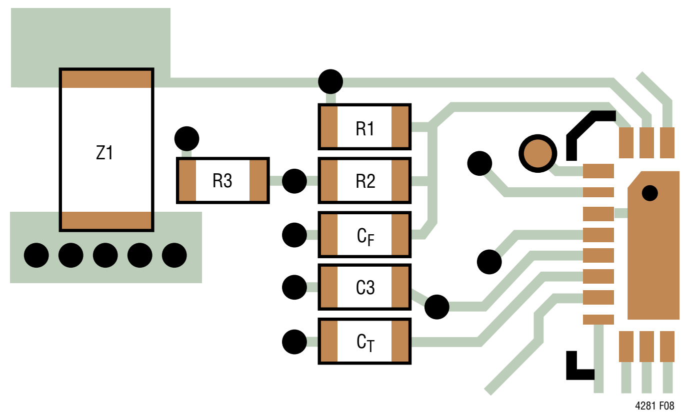

Figure 8. Recommended Layout

It is ill advised to place the ground plane under the power MOSFETs. If they fail and overheat that could result in a catastrophic failure as the input gets shorted to ground when the insulation between them fails.

Digital Interface

The LTC4281 communicates with a bus master using a 2-wire interface compatible with I^2C Bus and SMBus, an I^2C extension for low power devices. The LTC4281 is a read-write slave device and supports SMBus Read Byte, Write Byte, Read Word and Write Word commands, as well as I^2C continuous read and continuous write commands. Data formats for these commands are shown in Figures 9 through 16.

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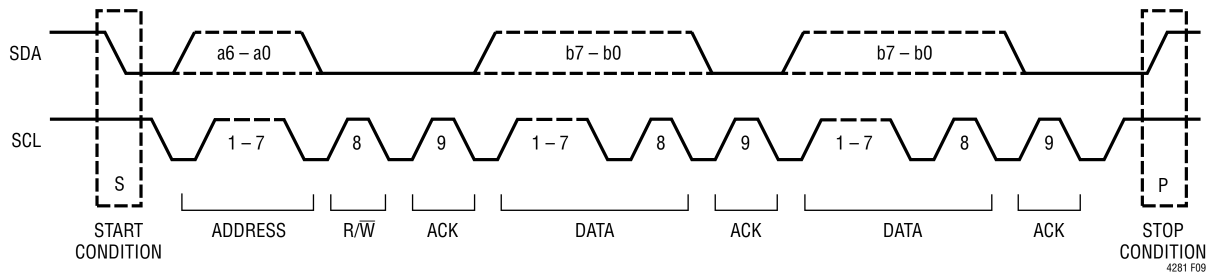

Figure 9. Data Transfer Over I²C or SMBus

S	ADDRESS	$\overline{\text{W}}$	A	COMMAND	A	DATA	A	P
	1 0 a4:a0	0	0	b7:b0	0	b7:b0	0	

4281 F10

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{\text{A}}$: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
$\overline{\text{W}}$: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

Figure 10. LTC4281 Serial Bus SDA Write Byte Protocol

S	ADDRESS	$\overline{\text{W}}$	A	COMMAND	A	DATA	A	DATA	A	P
	1 0 a4:a0	0	0	b7:b0	0	b7:b0	0	b7:b0	0	

4281 F11

Figure 11. LTC4281 Serial Bus SDA Write Word Protocol

S	ADDRESS	$\overline{\text{W}}$	A	COMMAND	A	DATA	A	DATA	A	• • •	DATA	A	P
	1 0 a4:a0	0	0	b7:b0	0	b7:b0	0	b7:b0	0		b7:b0	0	

4281 F12

Figure 12. LTC4281 Serial Bus SDA Continuous Write Protocol

S	ADDRESS	$\overline{\text{W}}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	$\overline{\text{A}}$	P
	1 0 a4:a0	0	0	b7:b0	0		1 0 a4:a0	1	0	b7:b0	1	

4281 F13

Figure 13. LTC4281 Serial Bus SDA Read Byte Protocol