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Low-Power SoC (System-on-Chip) with MCU, Memory, Sub-1 GHz RF Transceiver, and USB Controller

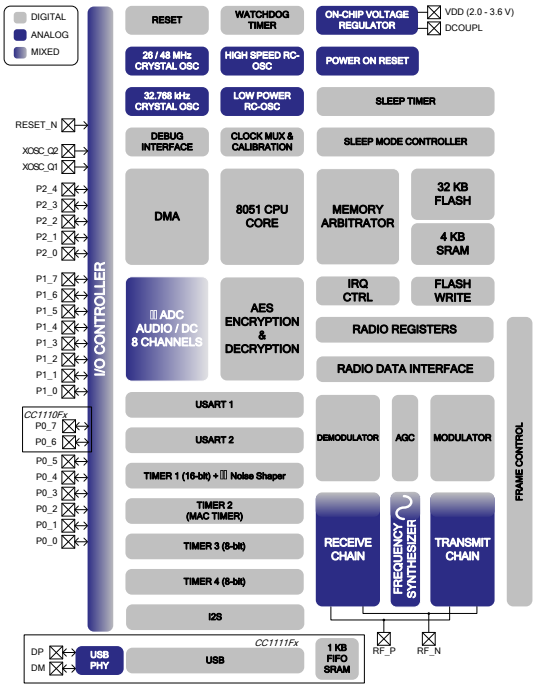
Applications

- *Low-power SoC wireless applications operating in the 315/433/868/915 MHz ISM/SRD bands*
- *Wireless alarm and security systems*
- *Industrial monitoring and control*
- *Wireless sensor networks*
- *AMR - Automatic Meter Reading*
- *Home and building automation*
- *Low power telemetry*
- ***CC1111Fx**: USB dongles*

Product Description

The ***CC1110Fx/CC1111Fx*** is a true low-power sub-1 GHz system-on-chip (SoC) designed for low-power wireless applications. The ***CC1110Fx/CC1111Fx*** combines the excellent performance of the state-of-the-art RF transceiver ***CC1101*** with an industry-standard enhanced 8051 MCU, up to 32 kB of in-system programmable flash memory and up to 4 kB of RAM, and many other powerful features. The small 6x6 mm package makes it very suited for applications with size limitations.

The ***CC1110Fx/CC1111Fx*** is highly suited for systems where very low power consumption is required. This is ensured by several advanced low-power operating modes. The ***CC1111Fx*** adds a full-speed USB 2.0 interface to the feature set of the ***CC1110Fx***. Interfacing to a PC using the USB interface is quick and easy, and the high data rate (12 Mbps) of the USB interface avoids the bottlenecks of RS-232 or low-speed USB interfaces.



Key Features

- **Radio**
  - High-performance RF transceiver based on the market-leading ***CC1101***
  - Excellent receiver selectivity and blocking performance
  - High sensitivity (−110
  - dBm at 1.2 kBaud)
  - Programmable data rate up to 500 kBaud
  - Programmable output power up to 10 dBm for all supported frequencies
  - Frequency range: 300 - 348 MHz, 391 - 464 MHz and 782 - 928 MHz
  - Digital RSSI / LQI support
- **Low Power**
  - Low current consumption (RX: 16.2 mA @ 1.2 kBaud, TX: 15.2 mA @ −6 dBm output power)
  - 0.3 µA in PM3 (the operating mode with the lowest power consumption)
  - 0.5 µA in PM2 (operating mode with the second lowest power consumption, timer or external interrupt wakeup)
- **MCU, Memory, and Peripherals**
  - High performance and low power 8051 microcontroller core.
  - Powerful DMA functionality
  - 8/16/32 KB in-system programmable flash, and 1/2/4 KB RAM
  - Full-Speed USB Controller with 1 KB FIFO (***CC1111Fx***)
  - 128-bit AES security coprocessor
  - 7 - 12 bit ADC with up to eight inputs
  - I^2S interface
  - Two USARTs
  - 16-bit timer with DSM mode
  - Three 8-bit timers
  - Hardware debug support
  - 21 (***CC1110Fx***) or 19 (***CC1111Fx***) GPIO pins
  - SW compatible with ***CC2510Fx/CC2511Fx***
- **General**
  - Wide supply voltage range (2.0V - 3.6V)
  - RoHS compliant 6x6 mm QFN 36 package

Table of Contents

Abbreviation

ΔΣ	Delta-Sigma
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
ARIB	Association of Radio Industries and Businesses
ASK	Amplitude Shift Keying
BCD	Binary Coded Decimal
BER	Bit Error Rate
BOD	Brown Out Detector
CBC	Cipher Block Chaining
CBC-MAC	Cipher Block Chaining Message Authentication Code
CCA	Clear Channel Assessment
CCM	Counter mode + CBC-MAC
CFB	Cipher Feedback
CFR	Code of Federal Regulations
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CTR	Counter mode (encryption)
DAC	Digital to Analog Converter
DMA	Direct Memory Access
DSM	Delta-Sigma Modulator
ECB	Electronic Code Book
EM	Evaluation Module
ENOB	Effective Number of Bits
EP{0 - 5}	USB Endpoints 0 - 5
ESD	Electro Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standard Institute
FCC	Federal Communications Commission
FIFO	First In First Out
GPIO	General Purpose Input / Output
HSSD	High Speed Serial Debug
HW	Hardware
I/O	Input / Output
I/Q	In-phase / Quadrature-phase
I^2S	Inter-IC Sound
IF	Intermediate Frequency
IOC	I/O Controller
ISM	Industrial, Scientific and Medical
ISR	Interrupt Service Routine
IV	Initialization Vector
JEDEC	Joint Electron Device Engineering Council
KB	Kilo Bytes (1024 bytes)
kbps	kilo bits per second
LFSR	Linear Feedback Shift Register
LNA	Low-Noise Amplifier
LO	Local Oscillator
LQI	Link Quality Indication
LSB	Least Significant Bit / Byte
MAC	Medium Access Control
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit / Byte
NA	Not Applicable
OFB	Output Feedback (encryption)
OOK	On-Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PER	Packet Error Rate
PLL	Phase Locked Loop
PM{0 - 3}	Power Mode 0 -3
PMC	Power Management Controller
POR	Power On Reset
PQI	Preamble Quality Indicator
PWM	Pulse Width Modulator
QLP	Quad Leadless Package
RAM	Random Access Memory
RCOSC	RC Oscillator
RF	Radio Frequency
RoHS	Restriction on Hazardous Substances
RSSI	Receive Signal Strength Indicator
RX	Receive
SCK	Serial Clock
SFD	Start of Frame Delimiter
SFR	Special Function Register
SINAD	Signal-to-noise and distortion ratio
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SW	Software
T/R	Transmit / Receive
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
WDT	Watchdog Timer
XOSC	Crystal Oscillator

1 Register Conventions

Each SFR is described in a separate table. The table heading is given in the following format:

REGISTER NAME (SFR Address) - Register Description.

Each RF register is described in a separate table. The table heading is given in the following format:

XDATA Address: REGISTER NAME - Register Description

All register descriptions include a symbol denoted R/W describing the accessibility of each bit in the register. The register values are always given in binary notation unless prefixed by '0x', which indicates hexadecimal notation.

Symbol	Access Mode
R/W	Read/write
R	Read only
R0	Read as 0
R1	Read as 1
W	Write only
W0	Write as 0
W1	Write as 1
H0	Hardware clear
H1	Hardware set

Table 1: Register Bit Conventions

2 Key Features (in more details)

2.1 High-Performance and Low-Power 8051-Compatible Microcontroller

- Optimized 8051 core which typically gives 8x the performance of a standard 8051
- Two data pointers
- In-circuit interactive debugging is supported by the IAR Embedded Workbench through a simple two-wire serial interface
- SW compatible with *CC2510Fx/CC2511Fx*

2.2 8/16/32 KB Non-volatile Program Memory and 1/2/4 kB Data Memory

- 8, 16, or 32 KB of non-volatile flash memory, in-system programmable through a simple two-wire interface or by the 8051 core
- Minimum flash memory endurance: 1000 write/erase cycles
- Programmable read and write lock of portions of flash memory for software security
- 1, 2, or 4 kB of internal SRAM

2.3 Full-Speed USB Controller (*CC1111Fx*)

- 5 bi-directional endpoints in addition to control endpoint 0
- Full-Speed, 12 Mbps transfer rate
- Support for Bulk, Interrupt, and Isochronous endpoints
- 1024 bytes of dedicated endpoint FIFO memory
- 8 - 512 byte data packet size supported
- Configurable FIFO size for IN and OUT direction of endpoint

2.4 I^2S Interface

- Industry standard I^2S interface for transfer of digital audio data
- Full duplex
- Mono and stereo support
- Configurable sample rate and sample size
- Support for μ-law compression and expansion

- Typically used to connect to external DAC or ADC

2.5 Hardware AES Encryption/Decryption

- 128-bit AES supported in hardware coprocessor

2.6 Peripheral Features

- Powerful DMA Controller
- Power On Reset/Brown-Out Detection
- ADC with eight individual input channels, single-ended or differential (*CC1111Fx* has six channels) and configurable resolution
- Programmable watchdog timer
- Five timers: one general 16-bit timer with DSM mode, two general 8-bit timers, one MAC timer, and one sleep timer
- Two programmable USARTs for master/slave SPI or UART operation
- 21 configurable general-purpose digital I/O-pins (*CC1111Fx* has 19)
- Random number generator

2.7 Low Power

- Four flexible power modes for reduced power consumption
- System can wake up on external interrupt or when the Sleep Timer expires
- 0.5 µA current consumption in PM2, where external interrupts or the Sleep Timer can wake up the system
- 0.3 µA current consumption in PM3, where external interrupts can wake up the system
- Low-power fully static CMOS design
- System clock source is either a high speed crystal oscillator (26 - 27 MHz for *CC1110Fx* and 48 MHz f*or* *CC1111Fx*) or a high speed RC oscillator (13 - 13.5 MHz for *CC1110Fx* and 12 MHz f*or* *CC1111Fx*). The high speed crystal oscillator must be used when the radio is active.
- Clock source for ultra-low power operation can be either a low-power RC oscillator or an optional 32.768 kHz crystal oscillator
- Very fast transition to active mode from power modes enables ultra low average power consumption in low duty-cycle systems

2.8 Sub-1 GHz Radio with Baseband Modem

- Based on the industry leading *CC1101* radio core
- Few external components: On-chip frequency synthesizer, no external filters or RF switch needed
- Flexible support for packet oriented systems: On-chip support for sync word detection, address check, flexible packet length, and automatic CRC handling
- Supports use of DMA for both RX and TX resulting in minimal CPU intervention even on high data rates
- Programmable channel filter bandwidth
- 2-FSK, GFSK, MSK, ASK, and OOK modulation formats supported
- Optional automatic whitening and de-whitening of data
- Programmable Carrier Sense (CS) indicator
- Programmable Preamble Quality Indicator (PQI) for detecting preambles and improved protection against sync word detection in random noise
- Support for automatic Clear Channel Assessment (CCA) before transmitting (for listen-before-talk systems)
- Support for per-package Link Quality Indication (LQI)

3 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 2 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Min	Max	Units	Condition
Supply voltage (VDD)	−0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	−0.3	VDD + 0.3, max 3.9	V	
Voltage on the pins RF_P, RF_N and DCOUPL	−0.3	2.0	V	
Voltage ramp-up rate		120	kV/µs	
Input RF level		10	dBm	
Storage temperature range	−50	150	°C	Device not programmed
Solder reflow temperature		260	°C	According to IPC/JEDEC J-STD-020D
ESD CC1110Fx		1000	V	According to JEDEC STD 22, method A114, Human Body Model (HBM)
ESD CC1110Fx		750	V	According to JEDEC STD 22, C101C, Charged Device Model (CDM)
ESD CC1111x		750	V	According to JEDEC STD 22, method A114, Human Body Model (HBM)
ESD CC1111x		750	V	According to JEDEC STD 22, C101C, Charged Device Model (CDM)

Table 2: Absolute Maximum Ratings

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

4 Operating Conditions

4.1 CC1110Fx Operating Conditions

The operating conditions for CC1110Fx are listed in Table 3 below.

Parameter	Min	Max	Unit	Condition
Operating ambient temperature, T_A	−40	85	°C	
Operating supply voltage (VDD)	2.0	3.6	V	All supply pins must have the same voltage

Table 3: Operating Conditions for CC1110Fx

4.2 CC1111Fx Operating Conditions

The operating conditions for CC1111Fx are listed in Table 4 below.

Parameter	Min	Max	Unit	Condition
Operating ambient temperature, T_A	0	85	°C	
Operating supply voltage (VDD)	3.0	3.6	V	All supply pins must have the same voltage

Table 4: Operating Conditions for CC1111Fx

5 General Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition/Note
Radio part					
Frequency range	300		348	MHz	
	391		464	MHz	
	782		928	MHz	
Data rate	1.2		500	kBaud	2-FSK (500 kBaud only characterized @ 915 MHz on CC1110Fx)
	1.2		250	kBaud	GFSK, OOK, and ASK
	26		500	kBaud	(Shaped) MSK (also known as differential offset QPSK) 500 kBaud only characterized @ 915 MHz Optional Manchester encoding (the data rate in kbps will be half the baud rate)
Wake-Up Timing					
PM1 → Active Mode		4		µs	Digital regulator on. HS RCOSC and high speed crystal oscillator off. 32.768 kHz XOSC or low power RCOSC running. SLEEP.OSC_PD=1 and CLKCON.OSC=1
PM2/3→ Active Mode		100		µs	Digital regulator off. HS RCOSC and high speed crystal oscillator off. 32.768 kHz XOSC or low power RCOSC running (PM2). No crystal oscillators or RC oscillators are running in PM3 SLEEP.OSC_PD=1 and CLKCON.OSC=1

Table 5: General Characteristics

6 Electrical Specifications

6.1 Current Consumption

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1110EM reference design ([1]).

Parameter	Min	Typ	Max	Unit	Condition
Active mode, full speed (high speed crystal oscillator)[1]. Low CPU activity.		5.0 4.8		mA mA	System clock running at 26 MHz. System clock running at 24 MHz. Digital regulator on. High speed crystal oscillator and low power RCOSC running. No peripherals running. Low CPU activity: No flash access (i.e. only cache hit), no RAM access
Active mode, full speed (HS RCOSC)[1]. Low CPU activity.		2.5		mA	System clock running at 13 MHz. Digital regulator on. HS RCOSC and low power RCOSC running. No peripherals running. Low CPU activity: No flash access (i.e. only cache hit), no RAM access
Active mode with radio in RX, 315 MHz					Digital regulator on. High speed crystal oscillator and low power RCOSC running. Radio in RX mode (sensitivity optimized `MDMCFG2.DEM_DCFILT_OFF=0`)
		19 19.5 16.2		mA mA mA	1.2 kBaud, input at sensitivity limit, system clock running at 26 MHz. 1.2 kBaud, input at sensitivity limit, system clock running at 24 MHz 1.2 kBaud, input at sensitivity limit, system clock running at 203 kHz.
		19 19.4		mA mA	1.2 kBaud, input well above sensitivity limit, system clock running at 26 MHz 1.2 kBaud, input well above sensitivity limit, system clock running at 24 MHz
		19 16.2		mA mA	38.4 kBaud, input at sensitivity limit, system clock running at 26 MHz. 38.4 kBaud, input at sensitivity limit, system clock running at 203 kHz.
		19		mA	38.4 kBaud, input well above sensitivity limit, system clock running at 26 MHz.
		20 21 17.2		mA mA mA	250 kBaud, input at sensitivity limit, system clock running at 26 MHz 250 kBaud, input at sensitivity limit, system clock running at 24 MHz. 250 kBaud, input at sensitivity limit, system clock running at 1.625 MHz.
		20 20		mA mA	250 kBaud, input well above sensitivity limit, system clock running at 26 MHz. 250 kBaud, input well above sensitivity limit, system clock running at 24 MHz.

[1] *Note: In order to reduce the current consumption in active mode, the clock speed can be reduced by setting `CLKCON.CLKSPD`≠000 (see section 12.1 for details).Figure 1 shows typical current consumption in active mode for different clock speeds*

Parameter	Min	Typ	Max	Unit	Condition
Active mode with radio in RX, 433 MHz					Digital regulator on. High speed crystal oscillator and low power RCOSC running. Radio in RX mode (sensitivity optimized MDMCFG2.DEM_DCFILT_OFF=0)
		19.8		mA	1.2 kBaud, input at sensitivity limit, system clock running at 26 MHz.
		19.7		mA	1.2 kBaud, input at sensitivity limit, system clock running at 24 MHz.
		17.1		mA	1.2 kBaud, input at sensitivity limit, system clock running at 203 kHz.
		19.8		mA	1.2 kBaud, input well above sensitivity limit, system clock running at 26 MHz.
		19.7		mA	1.2 kBaud, input well above sensitivity limit, system clock running at 24 MHz.
		19.8		mA	38.4 kBaud, input at sensitivity limit, system clock running at 26 MHz.
		17.1		mA	38.4 kBaud, input at sensitivity limit, system clock running at 203 kHz
		19.8		mA	38.4 kBaud, input well above sensitivity limit, system clock running at 26 MHz.
		20.5		mA	250 kBaud, input at sensitivity limit, system clock running at 26 MHz.
		21.5		mA	250 kBaud, input at sensitivity limit, system clock running at 24 MHz.
		18.1		mA	250 kBaud, input at sensitivity limit, system clock running at 1.625 MHz.
		20.5		mA	250 kBaud, input well above sensitivity limit, system clock running at 26 MHz.
		20.2		mA	250 kBaud, input well above sensitivity limit, system clock running at 24 MHz
					See Figure 2 for typical variation over operating conditions
Active mode with radio in RX, 868, 915 MHz					Digital regulator on. High speed crystal oscillator and low power RCOSC running. Radio in RX mode (sensitivity optimized MDMCFG2.DEM_DCFILT_OFF=0). 24 MHz system clock not measured
		19.7		mA	1.2 kBaud, input at sensitivity limit, system clock running at 26 MHz.
		17.0		mA	1.2 kBaud, input at sensitivity limit, system clock running at 203 kHz.
		18.7		mA	1.2 kBaud, input well above sensitivity limit, system clock running at 26 MHz.
		19.7		mA	38.4 kBaud, input at sensitivity limit, system clock running at 26 MHz.
		17.0		mA	38.4 kBaud, input at sensitivity limit, system clock running at 203 kHz.
		18.7		mA	38.4 kBaud, input well above sensitivity limit, system clock running at 26 MHz.
		20.4		mA	250 kBaud, input at sensitivity limit, system clock running at 26 MHz.
		18.0		mA	250 kBaud, input at sensitivity limit, system clock running at 1.625 MHz.
		19.1		mA	250 kBaud, input well above sensitivity limit, system clock running at 26 MHz.
Active mode with radio in TX, 315 MHz					System clock running at 26 MHz or 24 MHz. Digital regulator on. High speed crystal oscillator and low power RCOSC running. Radio in TX mode
		31.5		mA	10 dBm output power (PA_TABLE0=0xC2)
		19		mA	0 dBm output power (PA_TABLE0=0x51)
		18		mA	−6 dBm output power (PA_TABLE0=0x2A)

Parameter	Min	Typ	Max	Unit	Condition
Active mode with radio in TX, 433 MHz					System clock running at 26 MHz or 24 MHz. Digital regulator on. High speed crystal oscillator and low power RCOSC running. Radio in TX mode
		33.5		mA	10 dBm output power (PA_TABLE0=0xC0)
		20		mA	0 dBm output power (PA_TABLE0=0x60)
		19		mA	−6 dBm output power (PA_TABLE0=0x2A)
Active mode with radio in TX, 868, 915 MHz					System clock running at 26 MHz or 24 MHz. Digital regulator on. High speed crystal oscillator and low power RCOSC running. Radio in TX mode
		36.2		mA	10 dBm output power (PA_TABLE0=0xC2). See Table 7 for typical variation over operating conditions
		21		mA	0 dBm output power (PA_TABLE0=0x50)
		20		mA	−6 dBm output power (PA_TABLE0=0x2B)
Power mode 0		4.3		mA	Same as active mode, but the CPU is not running (see 12.1.2.2 for details). System clock at 26 MHz or 24 MHz
Power mode 1		220		µA	Digital regulator on. HS RCOSC and high speed crystal oscillator off. 32.768 kHz XOSC or low power RCOSC running (see 12.1.2.3 for details)
Power mode 2		0.5		µA	Digital regulator off. HS RCOSC and high speed crystal oscillator off. Low power RCOSC running (see 12.1.2.4 for details)
Power mode 3		0.3	1.0	µA	Digital regulator off. No crystal oscillators or RC oscillators are running (see 12.1.2.5 for details)
Peripheral Current Consumption					Add to the figures above if the peripheral unit is activated
Timer 1		2.7		µA/MHz	When running
Timer 2		1.3		µA/MHz	When running
Timer 3		1.6		µA/MHz	When running
Timer 4		2		µA/MHz	When running
ADC		1.2		mA	During conversion

Table 6: Current Consumption

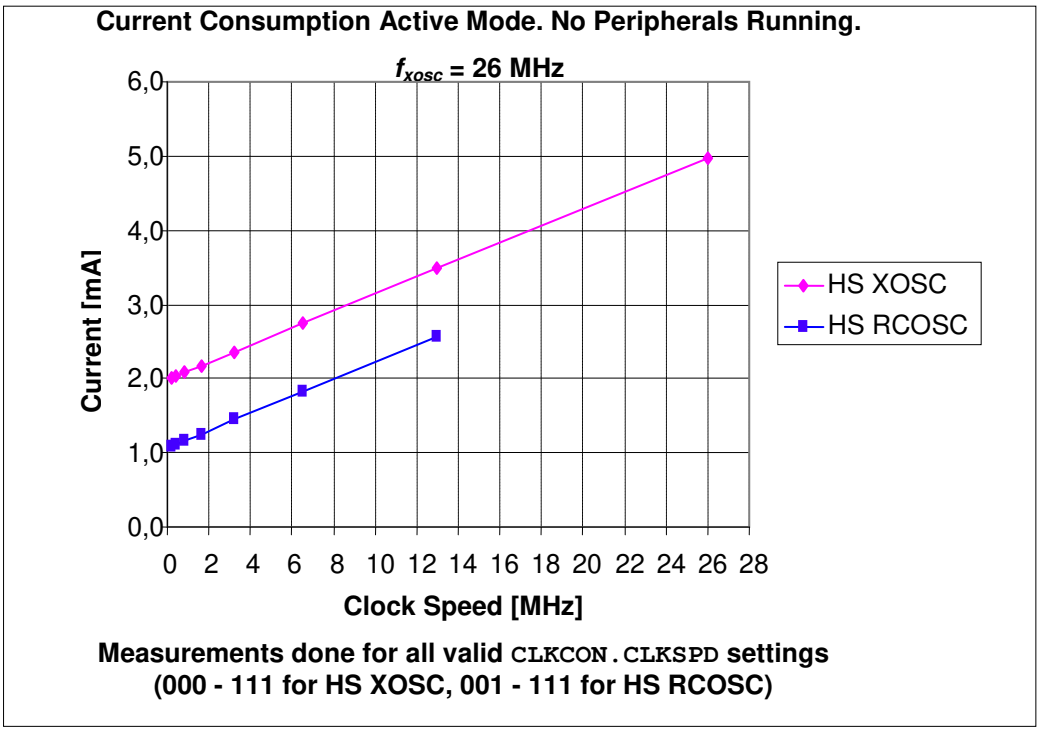


Figure 1: Current Consumption (Active Mode) vs. Clock Speed

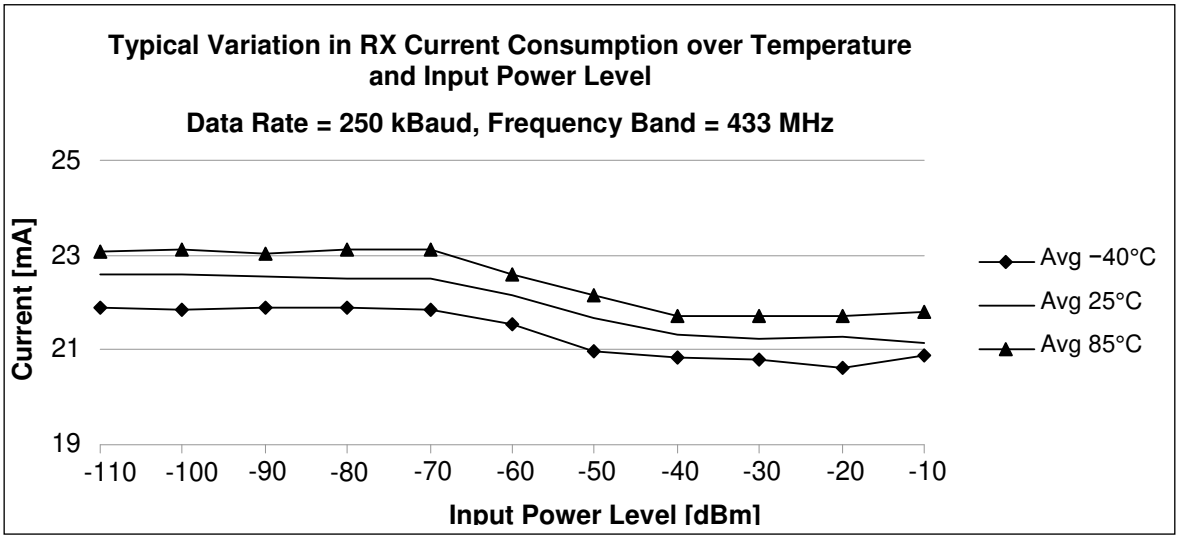


Figure 2: Typical Variation in RX Current Consumption over Temperature and Input Power Level. Data Rate = 250 kBaud, Frequency Band = 433 MHz

	Supply Voltage, VDD = 2 V			Supply Voltage, VDD = 3 V			Supply Voltage, VDD = 3.6 V		
Temperature [°C]	−40	25	85	−40	25	85	−40	25	85
Current [mA]	37	36	35.4	37.2	36.2	35.6	37.5	36.4	35.8

Table 7: Typical Variation in TX Current Consumption over Temperature and Supply Voltage, @ 868 MHz and 10 dBm Output Power.

6.2 RF Receive Section

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1110EM reference design ([1]) if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Digital channel filter bandwidth	58		812	kHz	User programmable (see Section 13.6). The bandwidth limits are proportional to crystal frequency (given values assume a 26 MHz system clock).
315 MHz, 1.2 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (GSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		−110 −112		dBm dBm	System clock running at 26 MHz System clock running at 24 MHz The RX current consumption can be reduced by approximately 2.0 mA by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical sensitivity is then −107 dBm.
315 MHz, 38.4 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (GSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		−102 −103		dBm dBm	System clock running at 26 MHz System clock running at 24 MHz The RX current consumption can be reduced by approximately 2.1 mA by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical sensitivity is then −99 dBm.
315 MHz, 250 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (MDMCFG2.DEM_DCFILT_OFF=1 cannot be used for data rates > 100 kBaud) (GSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		−94 −94		dBm dBm	System clock running at 26 MHz System clock running at 24 MHz
433 MHz, 1.2 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (GSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		−110 −110		dBm dBm	System clock running at 26 MHz System clock running at 24 MHz The RX current consumption can be reduced by approximately 2.6 mA by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical sensitivity is then −107 dBm.
433 MHz, 38.4 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (GSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		−102 −101		dBm dBm	System clock running at 26 MHz System clock running at 24 MHz The RX current consumption can be reduced by approximately 2.7 mA by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical sensitivity is then −99 dBm.
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Condition/Note**
433 MHz, 250 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (MDMCFG2.DEM_DCFILT_OFF=1 cannot be used for data rates > 100 kBaud) (GSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		−95 −93		dBm dBm	System clock running at 26 MHz System clock running at 24 MHz See Table 9 for typical variation over operating conditions

Parameter	Min	Typ	Max	Unit	Condition/Note
868 MHz, 1.2 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (GSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		−110 −110		dBm dBm	System clock running at 26 MHz Tested conducted on [4] CC1111 USB-Dongle Reference Design, 24 MHz clock The RX current consumption can be reduced by approximately 2.0 mA by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical sensitivity is then −107 dBm.
Saturation		−14		dBm	MCSM0.CLOSE_IN_RX=00
Adjacent channel rejection		38		dB	Desired channel 3 dB above the sensitivity limit. 100 kHz channel spacing
Alternate channel rejection		35		dB	Desired channel 3 dB above the sensitivity limit. 100 kHz channel spacing
					See Figure 58 for plot of selectivity versus frequency offset
Image channel rejection, 868 MHz		33		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit.
868 MHz, 38.4 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (GSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		−102 −101		dBm dBm	System clock running at 26 MHz Tested conducted on [4] CC1111 USB-Dongle Reference Design, 24 MHz clock The RX current consumption can be reduced by approximately 2.2 mA by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical sensitivity is then −100 dBm.
Saturation		−14		dBm	MCSM0.CLOSE_IN_RX=00
Adjacent channel rejection		19		dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing
Alternate channel rejection		32		dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing
					See Figure 59 for plot of selectivity versus frequency offset
Image channel rejection, 868 MHz		28		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit.

Parameter	Min	Typ	Max	Unit	Condition/Note
868 MHz, 250 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (MDMCFG2.DEM_DCFILT_OFF=1 cannot be used for data rates > 100 kBaud) (GSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		−94 −91		dBm dBm	System clock running at 26 MHz Tested conducted on [4] CC1111 USB-Dongle Reference Design, 24 MHz clock
Saturation		−16		dBm	MCSM0.CLOSE_IN_RX=00
Adjacent channel rejection		27		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing
Alternate channel rejection		36		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing
					See Figure 60 for plot of selectivity versus frequency offset
Image channel rejection, 868 MHz		17		dB	IF frequency 304 kHz Desired channel 3 dB above the sensitivity limit.
915 MHz, 1.2 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (2-FSK, 5.2 kHz deviation, 1% packet error rate, 20 bytes packet length, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		−108 −110		dBm dBm	System clock running at 26 MHz Tested conducted on [4] CC1111 USB-Dongle Reference Design, 24 MHz clock The RX current consumption can be reduced by approximately 2.0 mA by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical sensitivity is then −107 dBm.
915 MHz, 38.4 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (2-FSK, 1% packet error rate, 20 bytes packet length, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		−100 −100		dBm dBm	System clock running at 26 MHz Tested conducted on [4] CC1111 USB-Dongle Reference Design, 24 MHz clock The RX current consumption can be reduced by approximately 2.1 mA by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical sensitivity is then −99 dBm.
915 MHz, 250 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (MDMCFG2.DEM_DCFILT_OFF=1 cannot be used for data rates > 100 kBaud) (MSK, 1% packet error rate, 20 bytes packet length, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		–93 –91		dBm dBm	System clock running at 26 MHz Tested conducted on [4] CC1111 USB-Dongle Reference Design, 24 MHz clock
915 MHz, 500 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (MDMCFG2.DEM_DCFILT_OFF=1 cannot be used for data rates > 100 kBaud) (MSK, 1% packet error rate, 20 bytes packet length, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		–86		dBm	System clock running at 26 MHz. Not tested on [4] CC1111 USB-Dongle Reference Design, 24 MHz clock

Parameter	Min	Typ	Max	Unit	Condition/Note
Blocking					
Blocking at ±2 MHz offset, 1.2 kBaud, 868 MHz		−45		dBm	Desired channel 3 dB above the sensitivity limit.
Blocking at ±2 MHz offset, 250 kBaud, 868 MHz		−50		dBm	Desired channel 3 dB above the sensitivity limit
Blocking at ±10 MHz offset, 1.2 kBaud, 868 MHz		−33		dBm	Desired channel 3 dB above the sensitivity limit.
Blocking at ±10 MHz offset, 250 kBaud, 868 MHz		−40		dBm	Desired channel 3 dB above the sensitivity limit.
General					
Spurious emissions					Conducted measurement in a 50 Ω single ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66. Numbers are from ***CC1101*** (same radio on ***CC1110*** and ***CC1111***) Typical radiated spurious emission is −49 dB measured at the VCO frequency.
25 MHz - 1 GHz		−68	−57	dBm	Maximum figure is the ETSI EN 300 220 limit
Above 1 GHz		−66	−47	dBm	Maximum figure is the ETSI EN 300 220 limit

Table 8: RF Receive Section

	Supply Voltage, VDD = 2 V			Supply Voltage, VDD = 3 V			Supply Voltage, VDD = 3.6 V		
Temperature [°C]	−40	25	85	−40	25	85	−40	25	85
Sensitivity [dBm]	−96.4	−94.9	−92.6	−96.1	−95.0	−92.2	−96.1	−94.5	−92.2

Table 9: Typical Variation in Sensitivity over Temperature and Supply Voltage @ 433 MHz and 250 kBaud Data Rate

6.3 RF Transmit Section

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1110EM reference designs ([1]) if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance 315 MHz 433 MHz 868/915 MHz		 122 + j31 116 + j41 86.5 + j43		 Ω	Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC1110EM reference designs ([1], [2] and [3]) available from the TI website.
Output power, highest setting		10		dBm	Output power is programmable, and full range is available in all frequency bands Output power may be restricted by regulatory limits. See AN050 [13]. Note that this application note is for CC1101 but the same limitations apply to CC1110Fx and CC1111Fx as well. For CC1111Fx see in addition DN016 [14] for information on antenna solution and additional regulatory restrictions See Figure 3 for typical variation over operating conditions Delivered to 50 Ω single-ended load via CC1110EM reference design [3] RF matching network.
Output power, lowest setting		−30		dBm	Output power is programmable and is available across the entire frequency band Delivered to 50 Ω single-ended load via CC1110EM reference design [3] RF matching network.
Harmonics, radiated 2nd Harm, 433 MHz 3rd Harm, 433 MHz 2nd Harm, 868 MHz 3rd Harm, 868 MHz		 −51 −42 −37 −43		 dBm dBm dBm dBm	Measured on CC1110EM reference designs ([2] and [3]) with CW, 10 dBm output power The antennas used during the radiated measurements (SMAFF-433 from R.W. Badland and Nearson S331 868/915) play a part in attenuating the harmonics
Harmonics, radiated 2nd Harm, 868 MHz 3rd Harm, 868 MHz		 −55 −55		 dBm dBm	Measured on [4] CC1111 USB-Dongle Reference Design, with CW, 10 dBm output power. The chip antenna used during the radiated measurements play a part in attenuating the harmonics
Harmonics, conducted					Measured on CC1110EM reference designs ([1], [2] and [3]) with CW, 10 dBm output power, TX frequency at 315.00 MHz, 433.00 MHz, 868.00 MHz, or 915.00 MHz
315 MHz		< −35 < −52		dBm	Frequencies below 960 MHz Frequencies above 960 MHz
433 MHz		< −44 < −35		dBm	Frequencies below 1 GHz Frequencies above 1 GHz
868 MHz		< −35		dBm	Frequencies above 1 GHz
915 MHz		< −34		dBm	Frequencies above 1 GHz

Parameter	Min	Typ	Max	Unit	Condition/Note
Spurious emissions radiated, Harmonics not included					Measured on CC1110EM reference designs ([1], [2] and [3]) with 10 dBm CW, TX frequency at 315.00 MHz, 433.00 MHz, 868.00 or 915.00 MH. For CC1111Fx see DN016 [14] Please refer to register TEST1 on Page 226 for required settings in RX and TX
315 MHz		< −58 < −53		dBm	Frequencies below 960 MHz Frequencies above 960 MHz
433 MHz		< −50 < −54 < −56		dBm	Frequencies below 1 GHz Frequencies above 1 GHz Frequencies within 47 - 74, 87.5 - 118, 174 - 230, 470 - 862 MHz
868 MHz		< −56 < −54 < −56		dBm	Frequencies below 1 GHz Frequencies above 1 GHz Frequencies within 47 - 74, 87.5 - 118, 174 - 230, 470 - 862 MHz.
915 MHz		< −51 < −60		dBm	Frequencies below 960 MHz Frequencies above 960 MHz

Table 10: RF Transmit Section

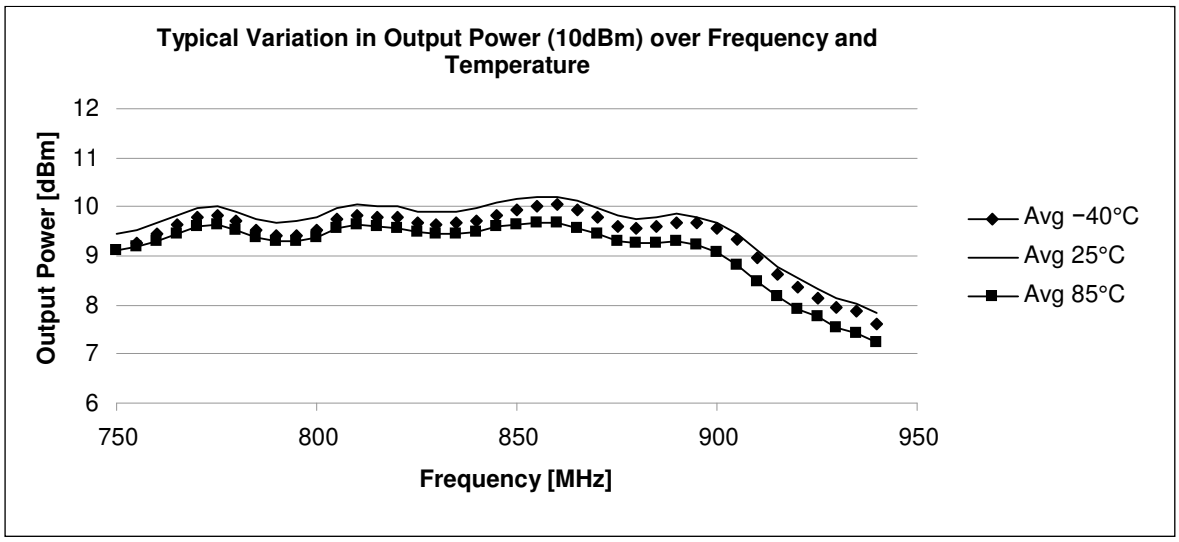


Figure 3: Typical Variation in Output Power over Frequency and Temperature (10 dBm output power)

6.4 Crystal Oscillators

6.4.1 CC1110Fx Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	27	MHz	Referred to as f_{XOSC}.
Crystal frequency accuracy requirement		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging, and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
C_0	1	5	7	pF	Simulated over operating conditions
Load capacitance	10	13	20	pF	Simulated over operating conditions
ESR			100	Ω	Simulated over operating conditions
Start-up time		250		µs	f_{XOSC} = 26 MHz *Note: A Ripple counter of 12 bit is included to ensure duty-cycle requirements. Start-up time includes ripple counter delay until* `SLEEP.XOSC_STB` *is asserted*
Power Down Guard Time	3			ms	The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power down guard time can vary with crystal type and load. Minimum figure is valid for reference crystal NDK, AT-41CD2 and load capacitance according to Table 29. If power down guard time is violated, one of the consequences can be increased PER when using the radio immediately after the crystal oscillator has been reported stable.

Table 11: CC1110Fx Crystal Oscillator Parameters

6.4.2 CC1111Fx Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency		48		MHz	Referred to as f_{XOSC}. 48 MHz crystal gives a system clock of 24 MHz. Please note that there is restricted usage in the frequency bands 863 - 870 MHz (due to spurious emission). See DN016 Compact Antenna Solutions for 868/915 MHz [14]
Crystal frequency accuracy requirement		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging, and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
C_0					
Fundamental	0.85	1	1.15	pF	Simulated over operating conditions. Variation given by reference crystal NX2520SA from NDK (fundamental).
Load capacitance	15	16	17	pF	Simulated over operating conditions
ESR			60	Ω	Simulated over operating conditions
Start-up time					*Note: A Ripple counter of 14 bit is included to ensure duty-cycle requirements. Start-up time includes ripple counter delay until* `SLEEP.XOSC_STB` *is asserted*
Fundamental		650		µs	

Table 12: CC1111Fx Crystal Oscillator Parameters

6.5 32.768 kHz Crystal Oscillator

T_A = 25°C, VDD = 3.0V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency		32.768		kHz	
C_0		0.9	2.0	pF	Simulated over operating conditions
Load capacitance		12	16	pF	Simulated over operating conditions
ESR		40	130	kΩ	Simulated over operating conditions
Start-up time		400		ms	Value is simulated

Table 13: 32.768 kHz Crystal Oscillator Parameters

6.6 Low Power RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency[2]	34.7 32.0	34.7 32.0	36.0 32.0	kHz	CC1110Fx CC1111Fx Calibrated low power RC oscillator frequency is f_{Ref} / 750
Frequency accuracy after calibration			±1	%	
Temperature coefficient		+0.5		%/°C	Frequency drift when temperature changes after calibration
Supply voltage coefficient		+3		%/V	Frequency drift when supply voltage changes after calibration
Initial calibration time		2		ms	When the low power RC oscillator is enabled, calibration is continuously done in the background as long as the high speed crystal oscillator is running.

Table 14: Low Power RC Oscillator Parameters

[2] $f_{Ref} = f_{XOSC}$ for CC1110Fx and $f_{Ref} = f_{XOSC}$ /2 for CC1111Fx
For CC1110Fx Min figures are given using f_{XOSC} = 26 MHz. Typ figures are given using f_{XOSC} = 26 MHz, and Max figures are given using f_{XOSC} = 27 MHz. For CC1111Fx, f_{XOSC} = 48 MHz

6.7 High Speed RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency[2]	12	13	13.5	MHz	Calibrated HS RCOSC frequency is f_{XOSC} / 2
Uncalibrated frequency accuracy		±15		%	
Calibrated frequency accuracy			±1	%	
Start-up time			10	µs	
Temperature coefficient			−325	ppm/°C	Frequency drift when temperature changes after calibration
Supply voltage coefficient			28	ppm/V	Frequency drift when supply voltage changes after calibration
Calibration time		65		µs	The HS RCOSC will be calibrated once when the high speed crystal oscillator is selected as system clock source (CLKCON.OSC is set to 0), and also when the system wakes up from PM{1 - 3} if CLKCON.OSC was set to 0 when entering PM{1 - 3}. See 12.1.5.1 for details).

Table 15: High Speed RC Oscillator Parameters

6.8 Frequency Synthesizer Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1110EM reference designs ([1]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution[3]	397 366	397 366	412 366	Hz	CC1110Fx CC1111Fx Frequency resolution = f_{Ref}/ 2^{16}
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing.
RF carrier phase noise		−92		dBc/Hz	@ 50 kHz offset from carrier
RF carrier phase noise		−93		dBc/Hz	@ 100 kHz offset from carrier
RF carrier phase noise		−93		dBc/Hz	@ 200 kHz offset from carrier
RF carrier phase noise		−98		dBc/Hz	@ 500 kHz offset from carrier
RF carrier phase noise		−107		dBc/Hz	@ 1 MHz offset from carrier
RF carrier phase noise		−113		dBc/Hz	@ 2 MHz offset from carrier
RF carrier phase noise		−119		dBc/Hz	@ 5 MHz offset from carrier
RF carrier phase noise		−129		dBc/Hz	@ 10 MHz offset from carrier

[3] $f_{Ref} = f_{XOSC}$ for CC1110Fx and $f_{Ref} = f_{XOSC}$ /2 for CC1111Fx
For CC1110Fx Min figures are given using f_{XOSC} = 26 MHz. Typ figures are given using f_{XOSC} = 26 MHz, and Max figures are given using f_{XOSC} = 27 MHz. For CC1111Fx, f_{XOSC} = 48 MHz

Parameter	Min	Typ	Max	Unit	Condition/Note
PLL turn-on / hop time[4]	72.4 81.4	75.2 81.4	75.2 81.4	µs	***CC1110Fx*** ***CC1111Fx*** Time from leaving the IDLE state until arriving in the RX, FSTXON, or TX state, when not performing calibration. Crystal oscillator running.
RX to TX switch[4]	29.0 32.6	30.1 32.6	30.1 32.6	µs	***CC1110Fx*** ***CC1111Fx*** Settling time for the 1·IF frequency step from RX to TX
TX to RX switch[4]	30.0 33.6	31.1 33.6	31.1 33.6	µs	***CC1110Fx*** ***CC1111Fx*** Settling time for the 1·IF frequency step from TX to RX
PLL calibration time[4]	707 796	735 796	735 796	µs	***CC1110Fx*** ***CC1111Fx*** Calibration can be initiated manually or automatically before entering or after leaving RX/TX. *Note: This is the PLL calibration time given that* `TEST0=0x0B` *and* `FSCAL3.CHP_CURR_CAL_EN=10` *(max calibration time). Please see DN110 [15] for more details*

Table 16: Frequency Synthesizer Parameters

6.9 Analog Temperature Sensor

T_A= 25°C, VDD = 3.0V if nothing else stated. All measurement results are obtained using the CC1110EM reference designs ([1]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at −0°C		0.660		V	
Output voltage at 0°C		0.755		V	
Output voltage at 40°C		0.859		V	
Output voltage at 80°C		0.958		V	
Temperature coefficient		2.47		mV/°C	Fitted from −20°C to 80°C
Error in calculated temperature, calibrated	−2 *	0	2 *	°C	From –20°C to 80°C when using 2.47 mV/°C, after 1-point calibration at room temperature * The indicated minimum and maximum error with 1-point calibration is based on measured values for typical process parameters
Current consumption increase when enabled		0.3		mA	

Table 17: Analog Temperature Sensor Parameters

[4] $f_{Ref} = f_{XOSC}$ for ***CC1110Fx*** and $f_{Ref} = f_{XOSC}/2$ for ***CC1111Fx***
For ***CC1110Fx*** Min figures are given using f_{XOSC} = 27 MHz. Typ figures are given using f_{XOSC} = 26 MHz, and Max figures are given using f_{XOSC} = 26 MHz. For ***CC1111Fx***, f_{XOSC} = 48 MHz The system clock frequency is equal to f_{Ref} and the data rate is 250 kBaud. No PA ramping is used. See DN110 [15] for more details.

6.10 7 - 12 bit ADC

T_A = 25°C, VDD = 3.0 V if nothing else stated. The numbers given here are based on tests performed in accordance with IEEE Std 1241-2000 [8]. The ADC data are from CC2430 characterization. As the CC1110Fx/C1111Fx uses the same ADC, the numbers listed in Table 18 should be good indicators of the performance to be expected from CC1110Fx and CC1111Fx. Note that these numbers will apply for 24 MHz operated systems (CC1111Fx using a 48 MHz crystal). Performance will be slightly different for other crystal frequencies (e.g. 26 MHz and 27 MHz).

Parameter	Min	Typ	Max	Unit	Condition/Note
Input voltage	0		VDD	V	VDD is the voltage on the AVDD pin (2.0 - 3.6 V)
External reference voltage	0		VDD	V	VDD is the voltage on the AVDD pin (2.0 - 3.6 V)
External reference voltage differential	0		VDD	V	VDD is the voltage on the AVDD pin (2.0 - 3.6 V)
Input resistance, signal		197		kΩ	Simulated using 4 MHz clock speed (see Section 12.10.2.7)
Full-Scale Signal[5]		2.97		V	Peak-to-peak, defines 0 dBFS
ENOB[5]		5.7		bits	7-bits setting
Single ended input		7.5			9-bits setting
		9.3			10-bits setting
		10.8			12-bits setting
ENOB[5]		6.5		bits	7-bits setting
Differential input		8.3			9-bits setting
		10.0			10-bits setting
		11.5			12-bits setting
Useful Power Bandwidth		0 - 20		kHz	7-bits setting, both single and differential
THD[5]					
-Single ended input		−75.2		dB	12-bits setting, −6 dBFS
-Differential input		−86.6			12-bits setting, −6 dBFS
Signal To Non-Harmonic Ratio[5]					
-Single ended input		70.2		dB	12-bits setting
-Differential input		79.3			12-bits setting
Spurious Free Dynamic Range[5]					
-Single ended input		78.8		dB	12-bits setting, -6 dBFS
-Differential input		88.9			12-bits setting, -6 dBFS
CMRR, differential input		<−84		dB	12- bit setting, 1 kHz Sine (0 dBFS), limited by ADC resolution
Crosstalk, single ended input		<−84		dB	12- bit setting, 1 kHz Sine (0 dBFS), limited by ADC resolution
Offset		−3		mV	Mid. Scale
Gain error		0.68		%	
DNL[5]		0.05		LSB	12-bits setting, mean
		0.9			12-bits setting, max
INL[5]		4.6		LSB	12-bits setting, mean
		13.3			12-bits setting, max

[5] Measured with 300 Hz Sine input and VDD as reference.

Parameter	Min	Typ	Max	Unit	Condition/Note
SINAD[5]		35.4		dB	7-bits setting
Single ended input		46.8		dB	9-bits setting
(−THD+N)		57.5			10-bits setting
		66.6			12-bits setting
SINAD[5]		40.7		dB	7-bits setting
Differential input		51.6			9-bits setting
(−THD+N)		61.8			10-bits setting
		70.8			12-bits setting
Conversion time		20		µs	7-bits setting
		36			9-bits setting
		68			10-bits setting
		132			12-bits setting
Current consumption		1.2		mA	

Table 18: 7 - 12 bit ADC Characteristics

6.11 Control AC Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1110EM reference designs ([1]).

Parameter	Min	Typ	Max	Unit	Condition/Note		
System clock, f_{SYSCLK} t_{SYSCLK}= 1/ f_{SYSCLK}					***CC1110Fx***		
	0.1875	26	27	MHz	High speed crystal oscillator used as source (HS XOSC).		
	0.1875	13	13.5	MHz	Calibrated HS RCOSC used as source.		
						HS XOSC	HS RCOSC
					Min: f_{XOSC} = 24 MHz, `CLKCON.CLKSPD` =	`111`	`111`
					Typ: f_{XOSC} = 26 MHz, `CLKCON.CLKSPD` =	`000`	`001`
					Max: f_{XOSC} = 27 MHz, `CLKCON.CLKSPD` =	`000`	`001`
					CC1111Fx		
	0.1875	24	24	MHz	High speed crystal oscillator used as source		
	0.1875	12	12	MHz	HS RCOSC used as source		
						HS XOSC	HS RCOSC
					Min: f_{XOSC} = 48 MHz, `CLKCON.CLKSPD` =	`111`	`111`
					Typ: f_{XOSC} = 48 MHz, `CLKCON.CLKSPD` =	`000`	`001`
					Max: f_{XOSC} = 48 MHz, `CLKCON.CLKSPD` =	`000`	`001`
RESET_N low width	250			ns	See item 1, Figure 4. This is the shortest pulse that is guaranteed to be recognized as a reset pin request. *Note: Shorter pulses may be recognized but will not lead to complete reset of all modules within the chip.*		
Interrupt pulse width	t_{SYSCLK}				See item 2, Figure 4. This is the shortest pulse that is guaranteed to be recognized as an interrupt request. In PM2/3 the internal synchronizers are bypassed so this requirement does not apply in PM2/3.		

Table 19: Control Inputs AC Characteristics

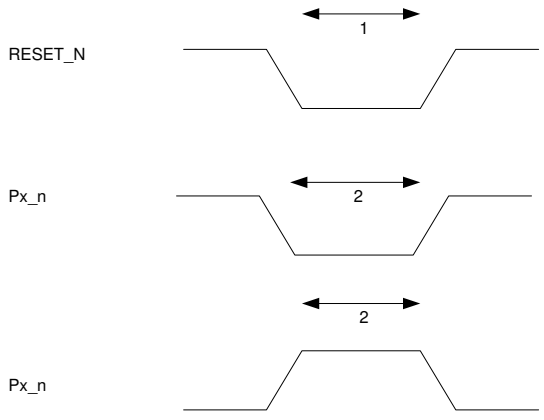


Figure 4: Control Inputs AC Characteristics