Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Matched Dual-Channel 6GHz RMS Power Detector

## FEATURES

- Frequency Range: 40MHz to 6GHz
- Linear Dynamic Range: Up to 60dB
- ±0.5dB (Typ) Accuracy Over Temperature
- 40dB Channel-to-Channel Isolation at 2GHz Even with Single-Ended RF Inputs
- Matched Dual-Channel Outputs: <1.25dB (Typ)
- Single-Ended RF Inputs—No Transformer Required
- Accurate RMS Power Measurement of High Crest Factor Modulated Waveforms
- Difference Output Provides VSWR Measurement
- Fast Envelope Detector Outputs
- Fast Response Time: 140ns Rise Time
- Small 4mm × 4mm QFN24 Package

## APPLICATIONS

- VSWR Monitor
- MIMO Transmit Power Control
- Basestation PA Control
- Transmit and Receive Gain Control
- RF Instrumentation



## DESCRIPTION

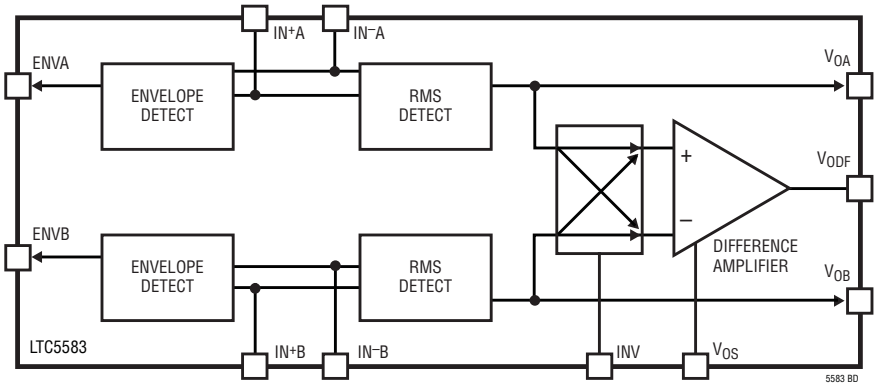
The LTC®5583 is a dual-channel RMS power detector, capable of measuring two AC signals with wide dynamic range, from –59dBm to 4dBm, depending on frequency. Each AC signal's power in decibel-scaled value is precisely converted to a DC voltage on a linear scale, independent of the crest factor of the input signal waveforms. The LTC5583 is suitable for precision power measurement and level control for a variety of RF standards, including LTE, EDGE, W-CDMA, CDMA2000, TD-SCDMA, and WiMAX.

Good channel-to-channel isolation is necessary for operating the dual channels simultaneously. For applications where the two input signals are at the same frequency (e.g. measuring VSWR), the LTC5583 provides 40dB isolation at 2.14GHz even with single-ended inputs. No baluns are needed. When the two input signals are at different frequencies, the isolation can be as high as 50dB. The isolation can be improved to >55dB with differential inputs.

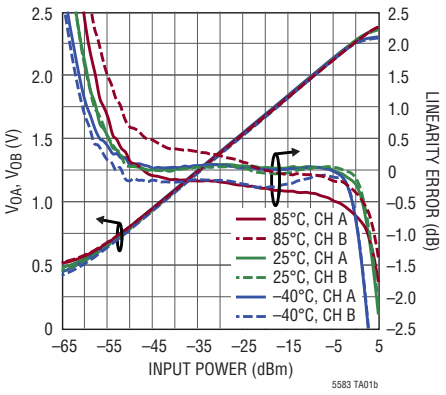
The power difference of the two input signals is provided at a difference output pin. Each channel also has a fast envelope detector, which tracks the RF input signal's envelope and outputs a voltage directly proportional to the signal's instantaneous power. The envelope detectors can be disabled to reduce power consumption.

## TYPICAL APPLICATION

**Block Diagram**




**Output Voltage and Linearity Error vs RF Input Power, 2140MHz CW Inputs, Single-Ended Drive**

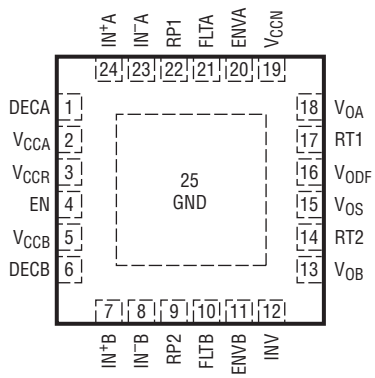


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltage ..... 3.8V
Enable Voltage ..... –0.3V to $V_{CC}$ + 0.3V
$V_{OS}$ Voltage ..... –0.3V to $V_{CC}$ + 0.3V
INV Voltage ..... –0.3V to 3.6V
Input Signal Power (Single-Ended, 50Ω) ..... 18dBm
Input Signal Power (Differential, 50Ω) ..... 24dBm
$T_{JMAX}$ ..... 125°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

## PIN CONFIGURATION




UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 37°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC5583IUF#PBF | LTC5583IUF#TRPBF | 5583 | 24-Lead (4mm × 4mm) Plastic QFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, –40°C to 85°C, otherwise specifications are at $T_A$ = 25°C, $V_{CC}$ = 3.3V, EN = 3.3V. Test circuits are shown in Figures 1 and 2 (Note 2).**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **AC Input** | | | | | | |
| Input Frequency Range | (Note 4) | | | 40 to 6000 | | MHz |
| Input Impedance | Differential | | | 400//0.5 | | Ω//pF |
| **$f_{RF}$ = 450MHz (Single-Ended Inputs)** | | | | | | |
| Linear Dynamic Range | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | 63 | | dB |
| | | ● | | 57 | | dB |
| RF Input Power Range | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | –59 to 4 | | dBm |
| Output Slope | | | | 29.6 | | mV/dB |
| Logarithmic Intercept | (Note 3) | | | –78.5 | | dBm |
| Deviation from CW Response | 11dB Peak to Average Ratio (3-Carrier CDMA2K)<br>12dB Peak to Average Ratio (4-Carrier WCDMA) | | | 0.7<br>0.4 | | dB<br>dB |
| Input A to Input B Isolation | Single-Ended Inputs | | | 77 | | dB |
| Input A to Output B Isolation<br>Input B to Output A Isolation | Single-Ended Inputs<br>(Notes 6, 7) | Frequency Separation = 0Hz<br>Frequency Separation = 1MHz<br>Frequency Separation = 10MHz | | 50<br>>55<br>>55 | | dB<br>dB<br>dB |
| **$f_{RF}$ = 880MHz (Single-Ended Inputs)** | | | | | | |
| Linear Dynamic Range | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | 61 | | dB |
| | | ● | | 56 | | dB |
| RF Input Power Range | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | –58 to 3 | | dBm |
| Output Slope | | | | 29.7 | | mV/dB |
| Logarithmic Intercept | (Note 3) | | | –77.8 | | dBm |
| Deviation from CW Response | 11dB Peak to Average Ratio (3-Carrier CDMA2K)<br>12dB Peak to Average Ratio (4-Carrier WCDMA) | | | 0.7<br>0.4 | | dB<br>dB |
| Input A to Input B Isolation | Single-Ended inputs | | | 68 | | dB |
| Input A to Output B Isolation<br>Input B to Output A Isolation | Single-Ended inputs<br>(Notes 6, 7) | Frequency Separation = 0Hz<br>Frequency Separation = 1MHz<br>Frequency Separation = 10MHz | | 41<br>52<br>51 | | dB<br>dB<br>dB |
| **$f_{RF}$ = 2140MHz (Single-Ended Inputs)** | | | | | | |
| Linear Dynamic Range | CW, 50Ω, ±1dB Linearity Error (Note 5) | | 50 | 60 | | dB |
| | | ● | | 55 | | dB |
| RF Input Power Range | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | –58 to 2 | | dBm |
| Output Slope | | | 26 | 29.6 | 34 | mV/dB |
| Logarithmic Intercept | (Note 3) | | –90 | –77.4 | –64 | dBm |
| Channel Mismatch | Input Power = 0dBm to Both Channels | | | <1.25 | | dB |
| Deviation from CW Response | 11dB Peak to Average Ratio (3-Carrier CDMA2K)<br>12dB Peak to Average Ratio (4- Carrier WCDMA) | | | 0.6<br>0.3 | | dB<br>dB |
| Input A to Input B Isolation | Single-Ended Inputs | | | 54 | | dB |
| Input A to Output B Isolation<br>Input B to Output A Isolation | Single-Ended Inputs<br>(Notes 6, 7) | Frequency Separation = 0Hz<br>Frequency Separation = 1MHz<br>Frequency Separation = 10MHz | | 40<br>52<br>51 | | dB<br>dB<br>dB |
| | Differential Inputs<br>(Notes 6, 7) | Frequency Separation = 0Hz<br>Frequency Separation = 1MHz<br>Frequency Separation = 10MHz | | >55<br>>55<br>>55 | | dB<br>dB<br>dB |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, –40°C to 85°C, otherwise specifications are at $T_A$ = 25°C, $V_{CC}$ = 3.3V, EN = 3.3V. Test circuits are shown in Figures 1 and 2 (Note 2).**

| PARAMETER | | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **$f_{RF}$ = 2700MHz (Single-Ended Inputs)** | | | | | | | | |
| Linear Dynamic Range | | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | | 59 | | dB |
| | | | | ● | | 52 | | dB |
| RF Input Power Range | | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | | –56 to 3 | | dBm |
| Output Slope | | | | | | 30.0 | | mV/dB |
| Logarithmic Intercept | | (Note 3) | | | | –74.9 | | dBm |
| Deviation from CW Response | | 12dB Peak to Average Ratio (WiMAX OFDM) | | | | 0.6 | | dB |
| Input A to Input B Isolation | | Single-Ended Inputs | | | | 52 | | dB |
| Input A to Output B Isolation<br>Input B to Output A Isolation | | Singled-Ended Inputs<br>(Notes 6, 7) | Frequency Separation = 0Hz<br>Frequency separation = 1MHz<br>Frequency separation = 10MHz | | | 33<br>45<br>44 | | dB<br>dB<br>dB |
| | | Differential Inputs<br>(Notes 6, 7) | Frequency Separation = 0Hz<br>Frequency separation = 1MHz<br>Frequency separation = 10MHz | | | 50<br>>55<br>>55 | | dB<br>dB<br>dB |
| **$f_{RF}$ = 3600MHz (Differential Inputs)** | | | | | | | | |
| Linear Dynamic Range | | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | | 56 | | dB |
| | | | | ● | | 49 | | dB |
| RF Input Power Range | | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | | –53 to 3 | | dBm |
| Output Slope | | | | | | 30.2 | | mV/dB |
| Logarithmic Intercept | | (Note 3) | | | | –73.1 | | dBm |
| Deviation from CW Response | | 12dB Peak to Average Ratio (WiMAX OFDM) | | | | 0.4 | | dB |
| Input A to Input B Isolation | | Differential Inputs | | | | 70 | | dB |
| Input A to Output B Isolation<br>Input B to Output A Isolation | | Differential Inputs<br>(Notes 6, 7) | Frequency Separation = 0Hz<br>Frequency Separation = 1MHz<br>Frequency Separation = 10MHz | | | 47<br>>55<br>>55 | | dB<br>dB<br>dB |
| **$f_{RF}$ = 5800MHz (Differential Inputs)** | | | | | | | | |
| Linear Dynamic Range | | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | | 49 | | dB |
| | | | | ● | | 44 | | dB |
| RF Input Power Range | | CW, 50Ω, ±1dB Linearity Error (Note 5) | | | | –44 to 5 | | dBm |
| Output Slope | | | | | | 31.3 | | mV/dB |
| Logarithmic Intercept | | (Note 3) | | | | –63.2 | | dBm |
| Deviation from CW Response | | 12dB Peak to Average Ratio (WiMAX OFDM) | | | | 0.5 | | dB |
| Input A to Input B Isolation | | Differential Inputs | | | | 50 | | dB |
| Input A to Output B Isolation<br>Input B to Output A Isolation | | Differential Inputs<br>(Notes 6, 7) | Frequency Separation = 0Hz<br>Frequency Separation = 1MHz<br>Frequency Separation = 10MHz | | | 30<br>42<br>41 | | dB<br>dB<br>dB |
| **Output Interface** | | | | | | | | |
| $V_{OA}$, $V_{OB}$ | Output DC Voltage | No RF Signal Present | | | | 0.45 | | V |
| | Output Impedance | | | | | 50 | | Ω |
| | $I_{OUT}$ | Source/Sink | | | | 5/5 | | mA |
| | Rise Time, 10% to 90% | 0.5V to 2.2V, $f_{RF}$ = 100MHz, $C_{FLTRA}$ = $C_{FLTRB}$ = 8.2nF | | | | 140 | | ns |
| | Fall Time, 90% to 10% | 2.2V to 0.5V, $f_{RF}$ = 100MHz, $C_{FLTRA}$ = $C_{FLTRB}$ = 8.2nF | | | | 3.5 | | µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, –40°C to 85°C, otherwise specifications are at $T_A$ = 25°C, $V_{CC}$ = 3.3V, EN = 3.3V. Test circuits are shown in Figures 1 and 2 (Note 2).**

| PARAMETER | | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{ODF}$ | Output DC Voltage | No RF Signal Present, $V_{OS}$ = 0V | | | 0.05 | | V |
| | Output Impedance | | | | 5 | | Ω |
| | $I_{OUT}$ | Source/Sink | | | 5/5 | | mA |
| | Rise Time, 10% to 90% | 50mV to 1.8V, $f_{RF}$ = 100MHz, $C_{FLTRA}$ = $C_{FLTRB}$ = 8.2nF | | | 170 | | ns |
| | Fall Time, 90% to 10% | 1.8V to 50mV, $f_{RF}$ = 100MHz, $C_{FLTRA}$ = $C_{FLTRB}$ = 8.2nF | | | 3.5 | | µs |
| ENVA<br>ENVB | Output DC Voltage | No RF Signal Present | | | 2.15 | | V |
| | Output Impedance | | | | 140 | | Ω |
| | $I_{OUT}$ | Source/Sink | | | 4.0/1.8 | | mA |
| | Rise Time, 10% to 90% | 0.9V to 2.1V | | | 11 | | ns |
| | Fall Time, 90% to 10% | 2.1V to 0.9V | | | 11 | | ns |
| | –3dB Bandwidth | | | | 50 | | MHz |
| **Control Interface** | | | | | | | |
| EN | Input High Voltage | | ● | 2 | | | V |
| | Input Low Voltage | | ● | | | 0.3 | V |
| | Input Current | Applied Voltage = 3.3V | | | 100 | 180 | µA |
| INV | Input High Voltage | | | 2 | | | V |
| | Input Low Voltage | | | | | 1 | V |
| | Input Current | Applied Voltage = 3.3V | | | 0 | | µA |
| $V_{OS}$ | Input Voltage Range | | | 0 | | 2.4 | V |
| | Input Current | Applied Voltage = 2.4V | | | 77 | | µA |
| **Power Supply** | | | | | | | |
| Supply Voltage | | | | 3.1 | 3.3 | 3.5 | V |
| Supply Current | | Envelope Detectors Turned Off | | | 80.5 | 100 | mA |
| Supply Current | | Envelope Detectors Turned On | | | 90.1 | | mA |
| Shutdown Current | | EN = 0V, $V_{CC}$ = 3.5V | | | 0.1 | 20 | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC5583 is guaranteed functional over the temperature range from –40°C to 85°C.

**Note 3:** Logarithmic Intercept is an extrapolated input power level from the best-fit log-linear straight line, where the output voltage is 0V.

**Note 4:** Operation over a wider frequency range is possible with reduced performance. Consult the factory for information and assistance.

**Note 5:** Linearity error is the difference in dB between the actual output and the best-fit straight line at 25°C (using linear regression between $P_{IN}$ = –50dBm and 0dBm for 450MHz, 880MHz, 2140MHz, 2700MHz; between $P_{IN}$ = –40dBm and 0dBm for 3600MHz, 5800MHz). The dynamic range is defined as the range of input power over which the linearity error is within ±1dB.

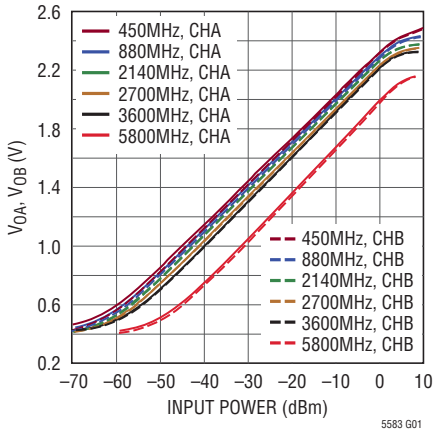
**Note 6:** Input A to Output B (Channel A to Channel B) isolation is defined as the ratio of input power levels at the two channels when the interfering channel (Channel A with higher power) results in a 1dB output deviation in the interfered channel (Channel B with lower power) and vice versa. Sweep one channel input power level while holding the other channel input at –45dBm for 450MHz, 880MHz, 2140MHz, 2700MHz, 3600MHz, and at –35dBm for 5800MHz.

**Note 7:** For frequency separation = 0Hz between the two input signals, channel-to-channel isolation is a function of the phase difference between these two signals. The worst-case isolation is assumed.

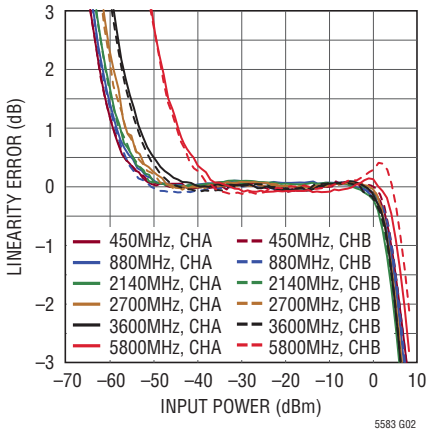
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 3.3V, EN = 3.3V, $T_A$ = 25°C, unless otherwise noted. Test circuits shown in Figures 1 and 2.**

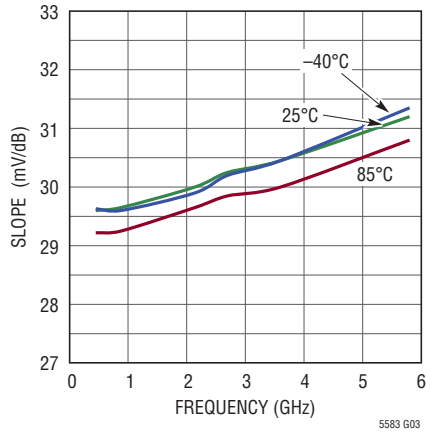
### Output Voltage vs RF Input Power CW Input at Various Frequencies



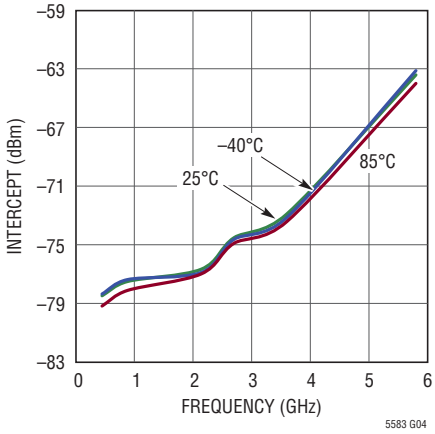

### Linearity Error vs RF Input Power CW Input at Various Frequencies



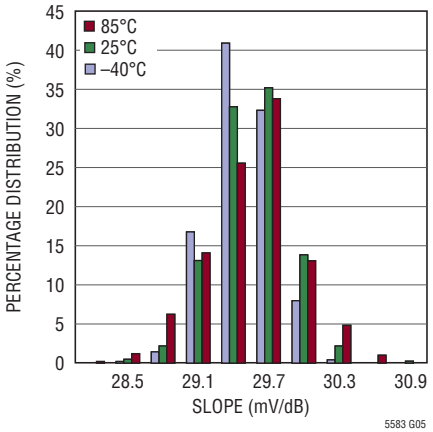

### Slope vs Frequency



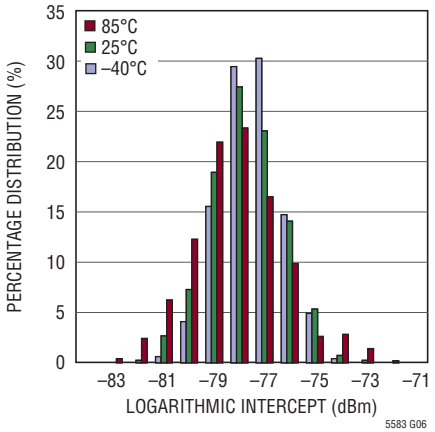

### Logarithmic Intercept vs Frequency




### Slope Distribution vs Temperature 2140MHz CW Input



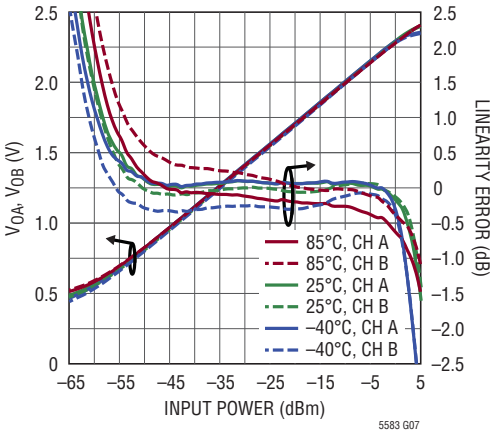

### Intercept Distribution vs Temperature 2140MHz CW Input



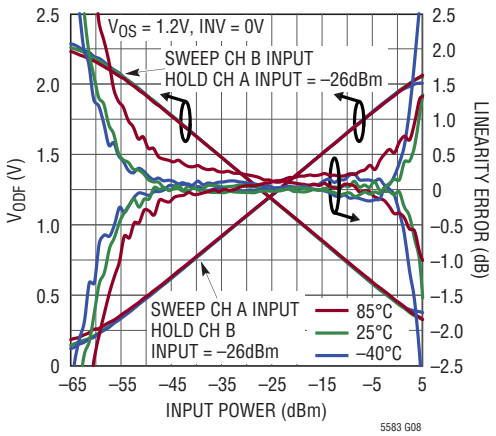
# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 3.3V, EN = 3.3V, $T_A$ = 25°C, unless otherwise noted. For temperature compensation of logarithmic intercept at 880MHz, set $R_{P1}$ = Open, $R_{P2}$ = 0, $R_{T1}$ = 11.5kΩ, $R_{T2}$ = 1.13kΩ. See Figure 1.**

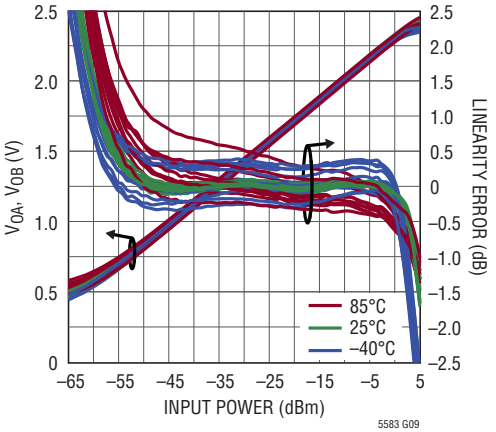
**Output Voltage and Linearity Error vs RF Input Power, 880MHz CW Inputs, Single-Ended Drive**



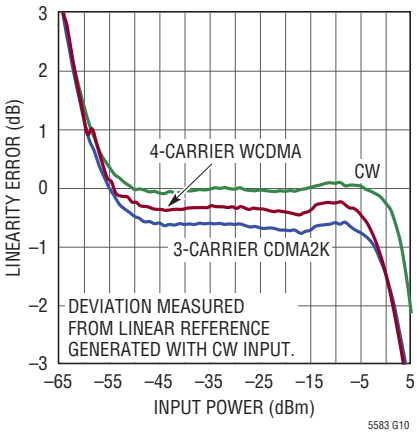

**Difference Output and Linearity Error vs RF Input Power, 880MHz CW Inputs, Single-Ended Drive**



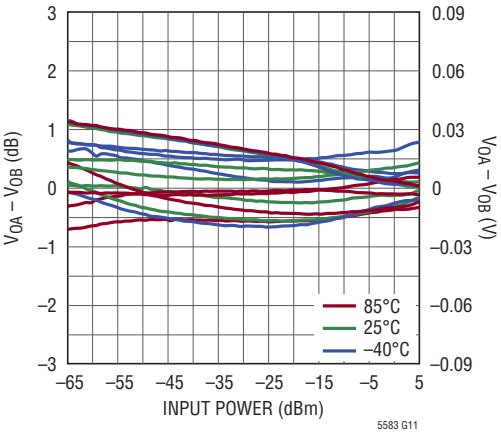

**Output Voltage and Linearity Error vs RF Input Power, 880MHz CW Inputs, Single-Ended Drive, 5 Devices**



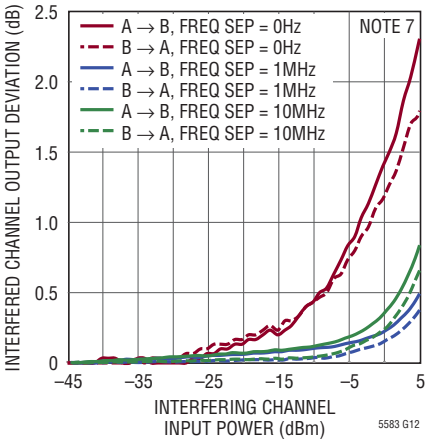

**Modulation Deviation vs RF Input Power, 880MHz Inputs, Single-Ended Drive**




**Channel Matching vs RF Input Power, 880MHz CW Inputs, Single-Ended Drive, 5 Devices**




**Input A to Output B Isolation, Input B to Output A Isolation, 880MHz CW Inputs, Single-Ended Drive**




A → B INDICATES:
CH A = INTERFERING CHANNEL
CH B = INTERFERED CHANNEL

B → A INDICATES:
CH B = INTERFERING CHANNEL
CH A = INTERFERED CHANNEL

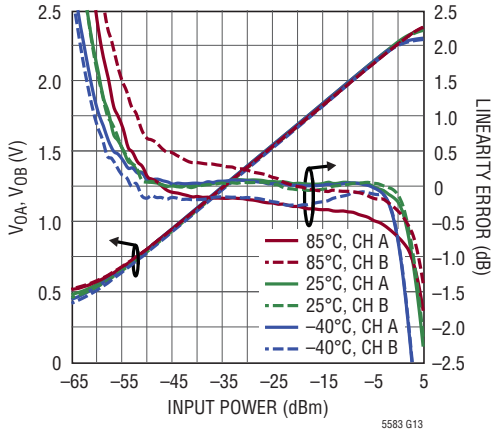
INTERFERED CHANNEL INPUT = –45dBm, INTERFERING CHANNEL INPUT SWEPT

FREQ SEP = FREQUENCY SEPARATION BETWEEN CH A INPUT AND CH B INPUT

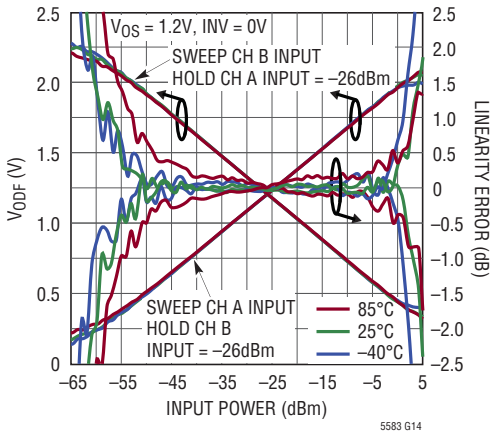
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 3.3V, EN = 3.3V, $T_A$ = 25°C, unless otherwise noted. For temperature compensation of logarithmic intercept at 2140MHz, set $R_{P1}$ = Open, $R_{P2}$ = 0, $R_{T1}$ = 9.76kΩ, $R_{T2}$ = 1.1kΩ. See Figure 1.**

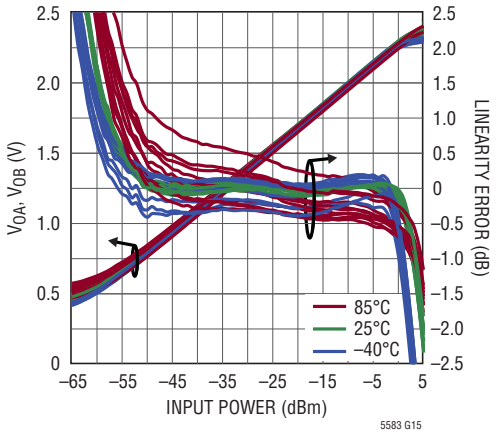
**Output Voltage and Linearity Error vs RF Input Power, 2140MHz CW Inputs, Single-Ended Drive**



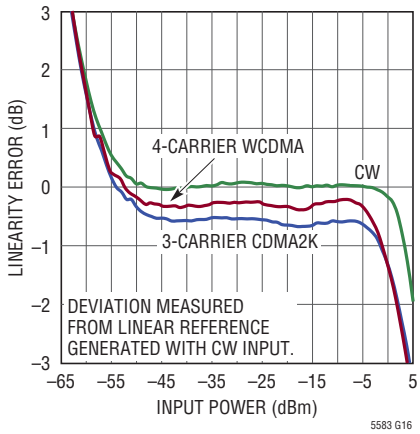

**Difference Output and Linearity Error vs RF Input Power, 2140MHz CW Inputs, Single-Ended Drive**



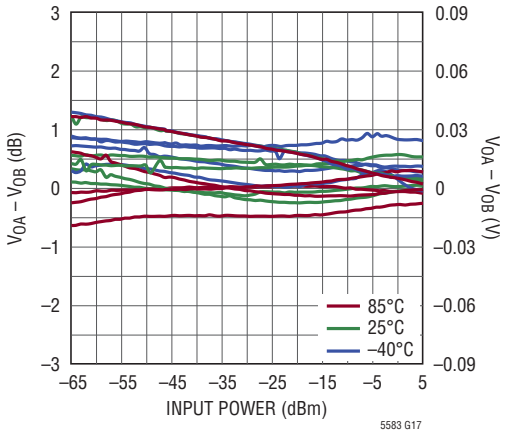

**Output Voltage and Linearity Error vs RF Input Power, 2140MHz CW Inputs, Single-Ended Drive, 5 Devices**



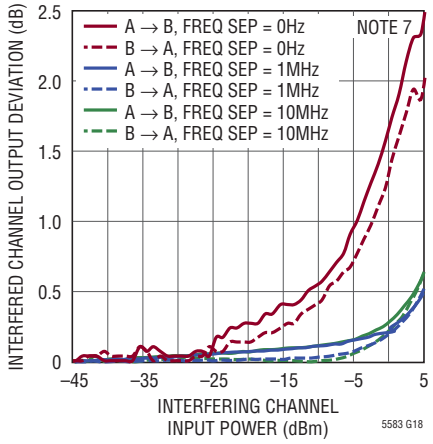

**Modulation Deviation vs RF Input Power, 2140MHz Inputs, Single-Ended Drive**




**Channel Matching vs RF Input Power, 2140MHz CW Inputs, Single-Ended Drive, 5 Devices**




**Input A to Output B Isolation, Input B to Output A Isolation, 2140MHz CW Inputs, Single-Ended Drive**




A → B INDICATES:
CH A = INTERFERING CHANNEL
CH B = INTERFERED CHANNEL

B → A INDICATES:
CH B = INTERFERING CHANNEL
CH A = INTERFERED CHANNEL

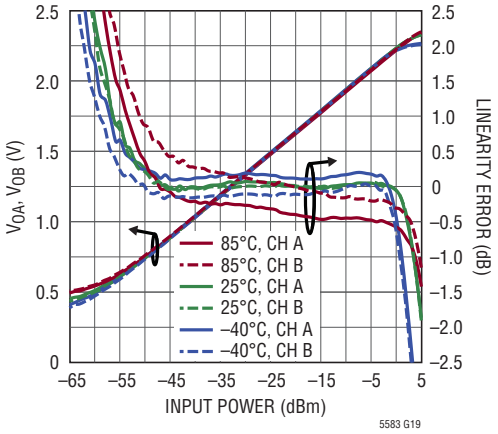
INTERFERED CHANNEL INPUT = –45dBm, INTERFERING CHANNEL INPUT SWEPT

FREQ SEP = FREQUENCY SEPARATION BETWEEN CH A INPUT AND CH B INPUT

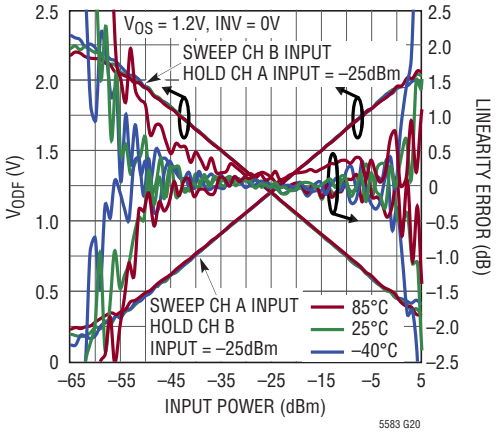
# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 3.3V, EN = 3.3V, $T_A$ = 25°C, unless otherwise noted. For temperature compensation of logarithmic intercept at 2700MHz, set $R_{P1}$ = Open, $R_{P2}$ = 0, $R_{T1}$ = 8.87kΩ, $R_{T2}$ = 1.21kΩ. See Figure 1.**

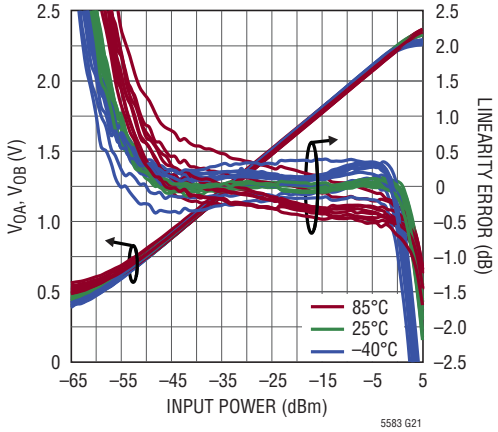
**Output Voltage and Linearity Error vs RF Input Power, 2700MHz CW Inputs, Single-Ended Drive**



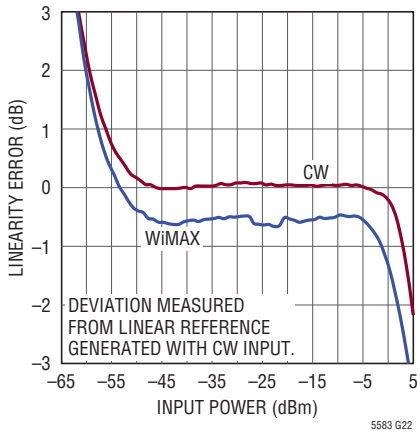

**Difference Output and Linearity Error vs RF Input Power, 2700MHz CW Inputs, Single-Ended Drive**



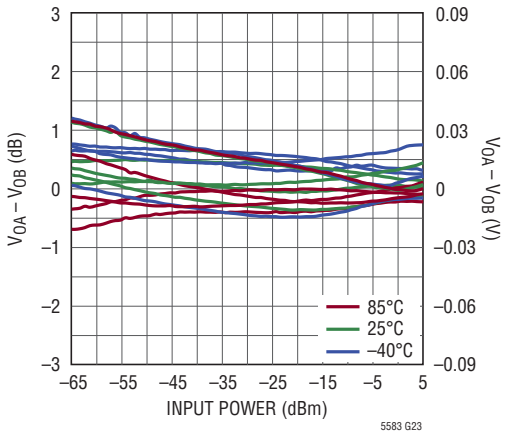

**Output Voltage and Linearity Error vs RF Input Power, 2700MHz CW Inputs, Single-Ended Drive, 5 Devices**



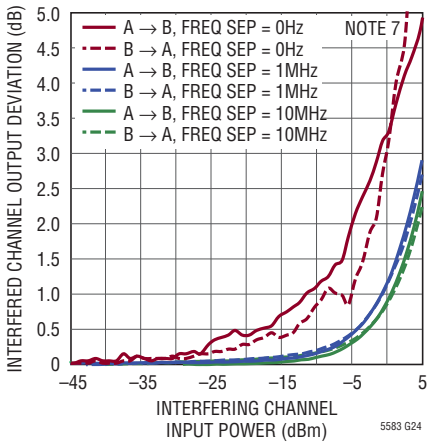

**Modulation Deviation vs RF Input Power, 2700MHz Inputs, Single-Ended Drive**




**Channel Matching vs RF Input Power, 2700MHz CW Inputs, Single-Ended Drive, 5 Devices**




**Input A to Output B Isolation, Input B to Output A Isolation, 2700MHz CW Inputs, Single-Ended Drive**




A → B INDICATES:
CH A = INTERFERING CHANNEL
CH B = INTERFERED CHANNEL

B → A INDICATES:
CH B = INTERFERING CHANNEL
CH A = INTERFERED CHANNEL

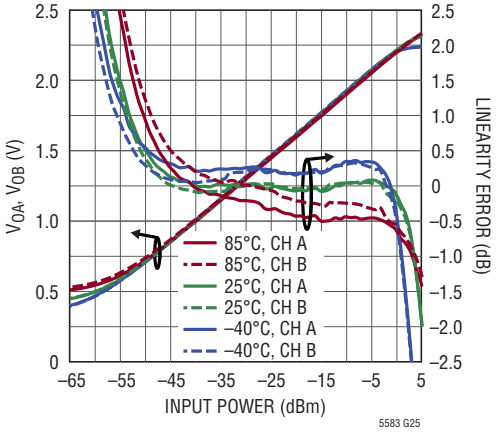
INTERFERED CHANNEL INPUT = –45dBm, INTERFERING CHANNEL INPUT SWEPT

FREQ SEP = FREQUENCY SEPARATION BETWEEN CH A INPUT AND CH B INPUT

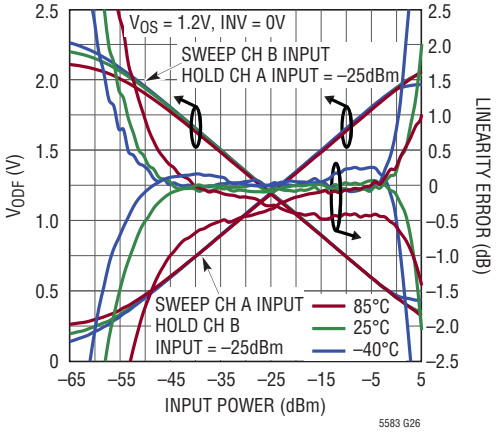
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 3.3V, EN = 3.3V, $T_A$ = 25°C, unless otherwise noted. For temperature compensation of logarithmic intercept at 3600MHz, set $R_{P1}$ = Open, $R_{P2}$ = 0, $R_{T1}$ = 10.2kΩ, $R_{T2}$ = 1.65kΩ. See Figure 2.**

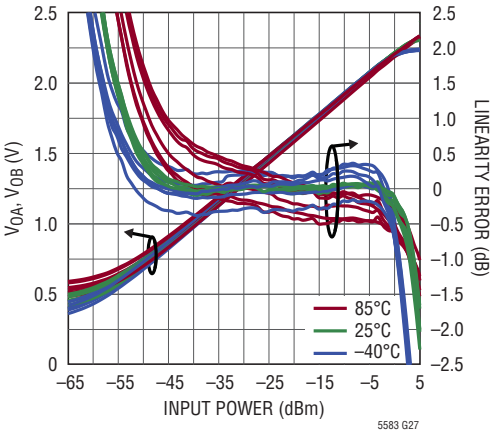
**Output Voltage and Linearity Error vs RF Input Power, 3600MHz CW Inputs, Differential Drive**



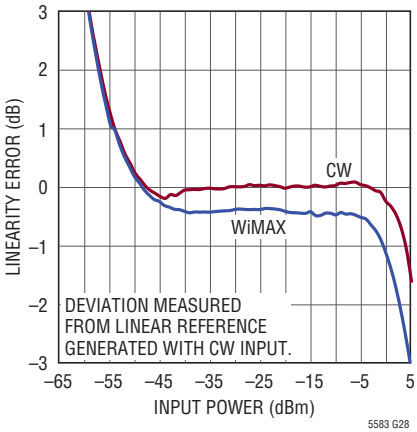

**Difference Output and Linearity Error vs RF Input Power, 3600MHz CW Inputs, Differential Drive**



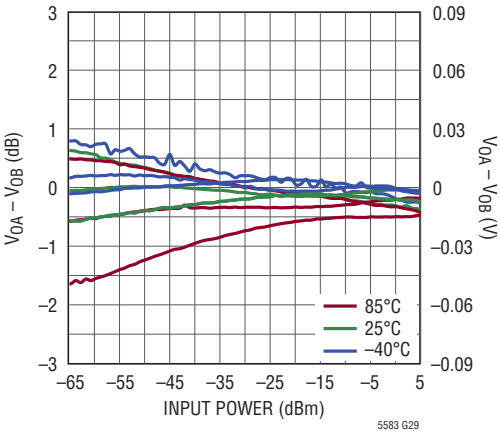

**Output Voltage and Linearity Error vs RF Input Power, 3600MHz CW Inputs, Differential Drive, 3 Devices**



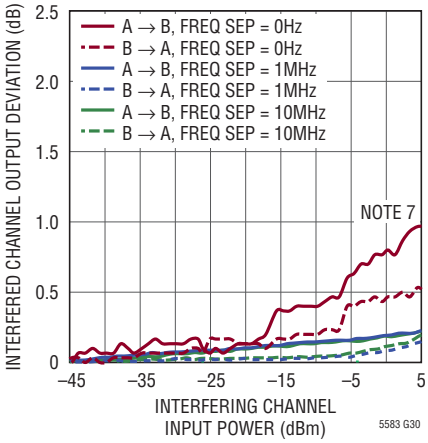

**Modulation Deviation vs RF Input Power, 3600MHz Inputs, Differential Drive**




**Channel Matching vs RF Input Power, 3600MHz CW Inputs, Differential Drive, 3 Devices**




**Input A to Output B Isolation, Input B to Output A Isolation, 3600MHz CW Inputs, Differential Drive**




A → B INDICATES:
CH A = INTERFERING CHANNEL
CH B = INTERFERED CHANNEL

B → A INDICATES:
CH B = INTERFERING CHANNEL
CH A = INTERFERED CHANNEL

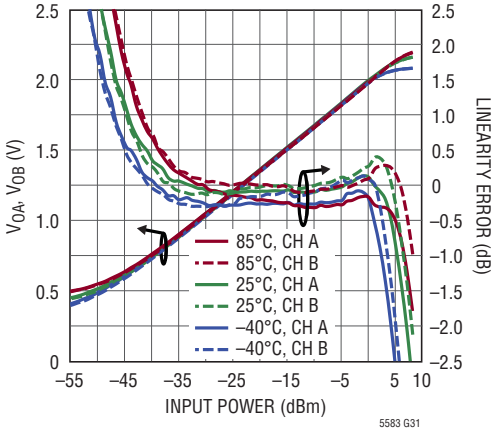
INTERFERED CHANNEL INPUT = –45dBm, INTERFERING CHANNEL INPUT SWEPT

FREQ SEP = FREQUENCY SEPARATION BETWEEN CH A INPUT AND CH B INPUT

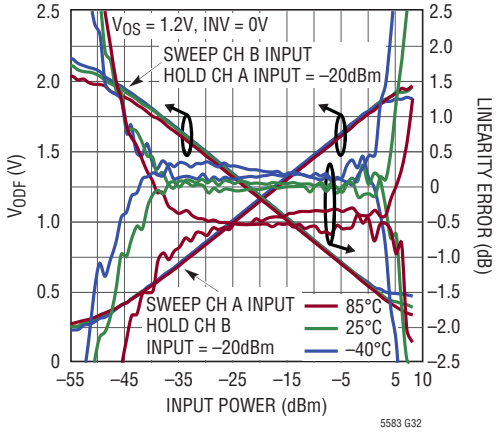
# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 3.3V, EN = 3.3V, $T_A$ = 25°C, unless otherwise noted. For temperature compensation of logarithmic intercept at 5800MHz, set $R_{P1}$ = Open, $R_{P2}$ = 0, $R_{T1}$ = 10kΩ, $R_{T2}$ = 1.47kΩ. See Figure 2.**

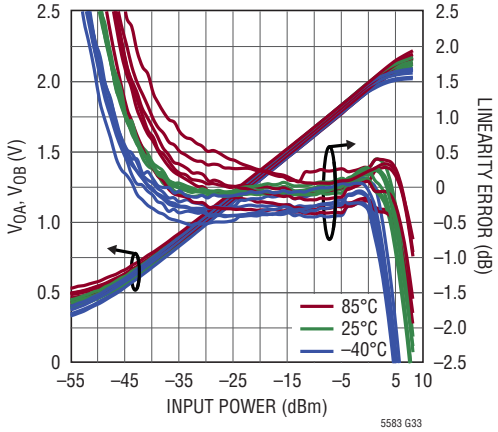
**Output Voltage and Linearity Error vs RF Input Power, 5800MHz CW Inputs, Differential Drive**



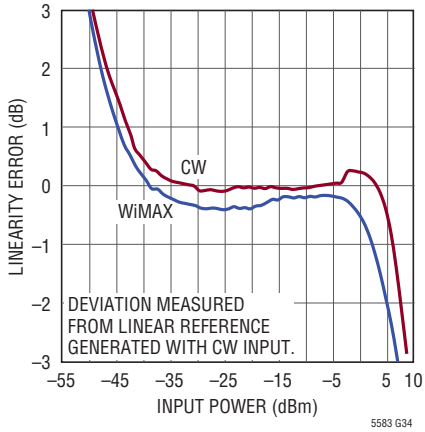

**Difference Output and Linearity Error vs RF Input Power, 5800MHz CW Inputs, Differential Drive**



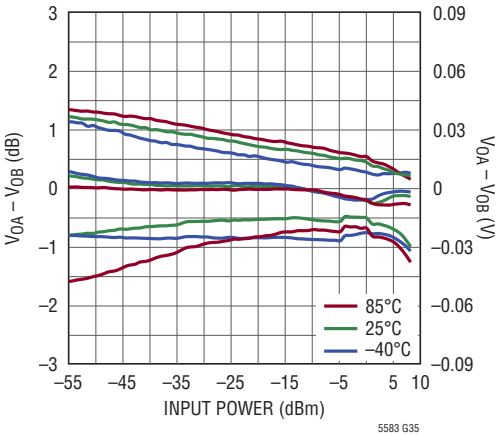

**Output Voltage and Linearity Error vs RF Input Power, 5800MHz CW Inputs, Differential Drive, 3 Devices**



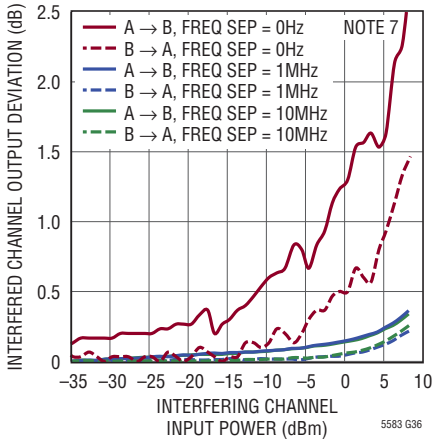

**Modulation Deviation vs RF Input Power, 5800MHz Inputs, Differential Drive**




**Channel Matching vs RF Input Power, 5800MHz CW Inputs, Differential Drive, 3 Devices**




**Input A to Output B Isolation, Input B to Output A Isolation, 5800MHz CW Inputs, Differential Drive**




A → B INDICATES:
CH A = INTERFERING CHANNEL
CH B = INTERFERED CHANNEL

B → A INDICATES:
CH B = INTERFERING CHANNEL
CH A = INTERFERED CHANNEL

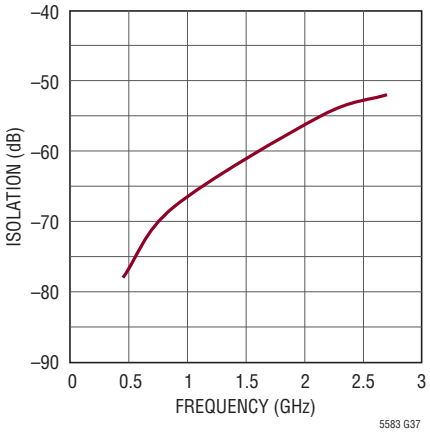
INTERFERED CHANNEL INPUT = –35dBm, INTERFERING CHANNEL INPUT SWEPT

FREQ SEP = FREQUENCY SEPARATION BETWEEN CH A INPUT AND CH B INPUT

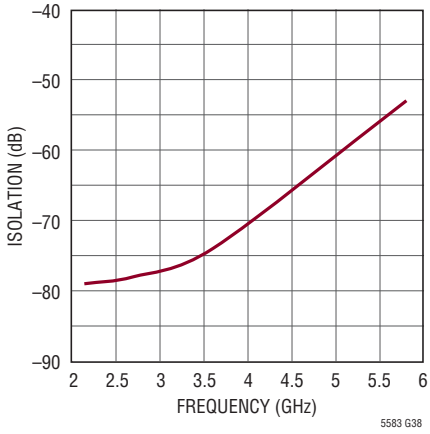
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 3.3V, EN = 3.3V, $T_A$ = 25°C, unless otherwise noted. Test circuits shown in Figures 1 and 2.**

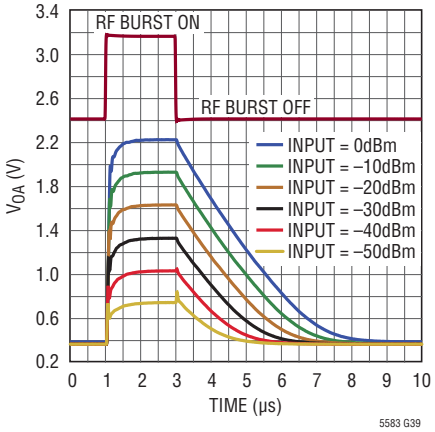
**Input A to Input B Isolation, Single-Ended Inputs**



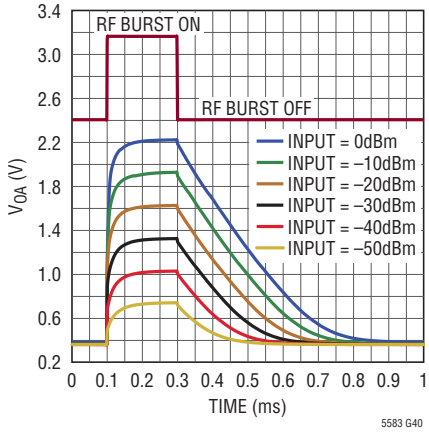

**Input A to Input B Isolation, Differential Inputs**



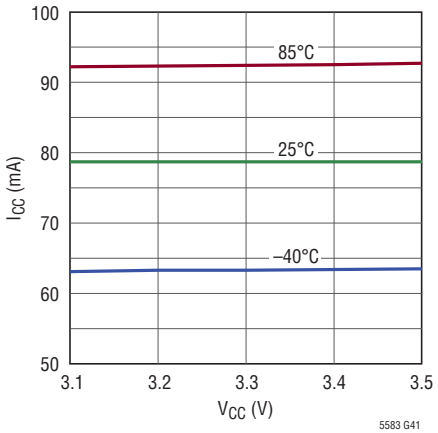

**Output Response to RF Burst Input, 100MHz CW Input, $C_{FLTRA}$ = $C_{FLTRB}$ = 8.2nF**



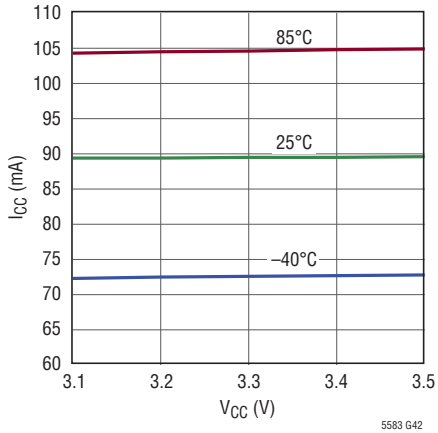

**Output Response to RF Burst Input, 100MHz CW Input, $C_{FLTRA}$ = $C_{FLTRB}$ = 1µF**




**Supply Current vs Supply Voltage Envelope Detectors Disabled**



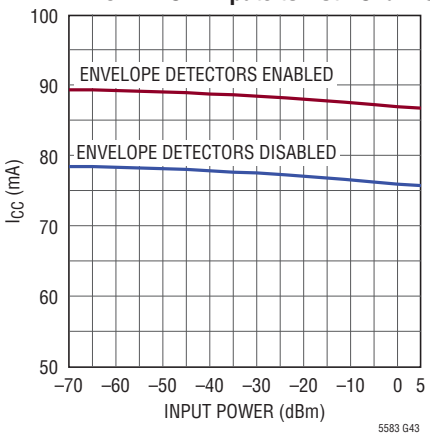

**Supply Current vs Supply Voltage Envelope Detectors Enabled**



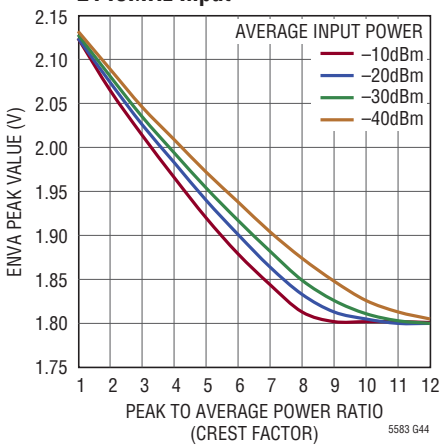
# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 3.3V, EN = 3.3V, $T_A$ = 25°C, unless otherwise noted. Test circuits shown in Figures 1 and 2.**

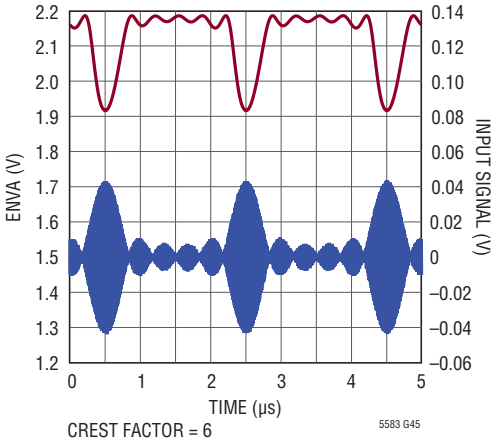
**Supply Current vs RF Input Power, 2140MHz CW Inputs to Both Channels**




**Envelope Detector Peak Output Voltage vs Crest Factor, 2140MHz Input**

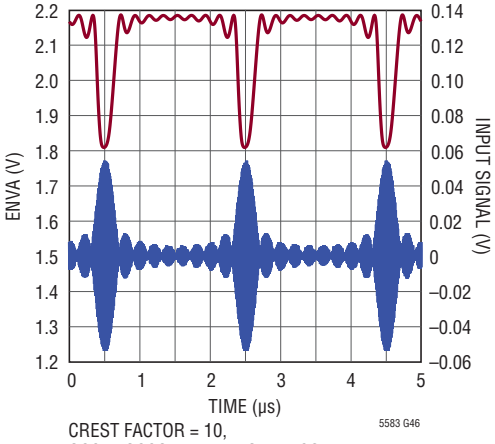



**Envelope Detector Output and Input Signal Envelope, 100MHz Input Average Power = –30dBm**



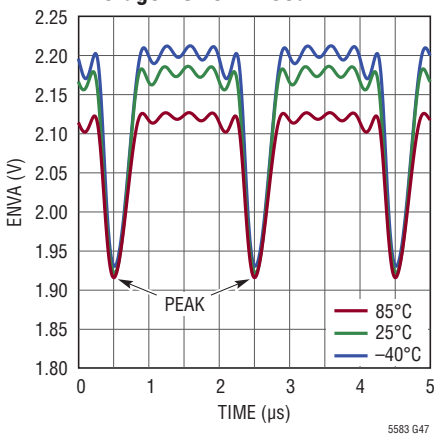

CREST FACTOR = 6
OSCILLOSCOPE WAVEFORM ACQUIRED IN AVERAGE MODE

**Envelope Detector Output and Input Signal Envelope, 100MHz Input Average Power = –30dBm**



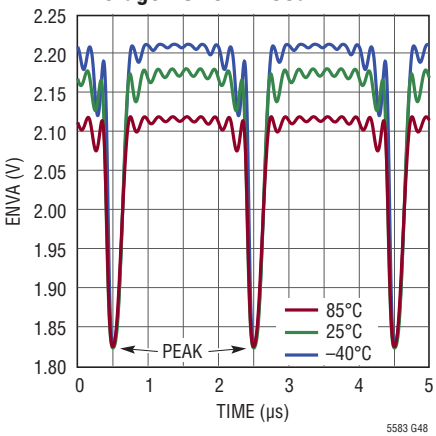

CREST FACTOR = 10,
OSCILLOSCOPE WAVEFORM ACQUIRED IN AVERAGE MODE

**Envelope Detector Output Over Temperature, 2140MHz Input Average Power = –30dBm**




CREST FACTOR = 6
OSCILLOSCOPE WAVEFORM ACQUIRED IN AVERAGE MODE

**Envelope Detector Output Over Temperature, 2140MHz Input Average Power = –30dBm**




CREST FACTOR = 10
OSCILLOSCOPE WAVEFORM ACQUIRED IN AVERAGE MODE

## PIN FUNCTIONS

**DECA, DECB (Pins 1, 6):** Input Common Mode Decoupling Pins for Channel A and Channel B. These pins are internally biased to 1.6V. The input impedance is 1.75kΩ in parallel with a 40pF internal shunt capacitor to ground. The impedance between DECA and $IN^+A$ (or $IN^-A$) is 200Ω. The pin can be connected to the center tap of an external balun or to a capacitor to ground.

**$V_{CCA}$, $V_{CCB}$, $V_{CCR}$ (Pins 2, 5, 3):** Power Supply Pins for Channel A, Channel B, and Bias Circuits. Typical total current consumption of these pins is 81mA. Each of these pins should be bypassed with 1nF and 1µF capacitors, placed as close to the IC as possible.

**EN (Pin 4):** Enable Input Pin. An applied voltage above 2V will activate the bias for the IC. For an applied voltage below 0.3V, the circuit will be shut down (disabled) with a corresponding reduction in power supply current. If the enable function is not required, then this pin can be connected to $V_{CC}$. The applied voltage to this pin should not exceed $V_{CC}$ by more than 0.3V.

**RP2 (Pin 9):** Pin for Setting Polarity of Second Order Output Temperature Compensation. Connect this pin to ground to change the output voltage inversely proportional to ambient temperature. Float this pin to change the output voltage proportional to ambient temperature.

**INV (Pin 12):** Control Input Pin to Invert the Polarity of the Difference Output $V_{ODF}$.

**RT2 (Pin 14):** Second Order Output Temperature Compensation Pin for Both Channels. Connect this pin to ground to disable. The output voltage will increase or decrease with the ambient temperature by connecting this pin to ground via an off-chip resistor, depending on the polarity set by RP2 pin.

**$V_{OS}$ (Pin 15):** Input Pin for Setting the DC Offset of the Difference Output $V_{ODF}$. It is recommended to set this DC offset such that $V_{ODF}$ does not fall below 100mV.

**$V_{ODF}$ (Pin 16):** DC Difference Output. This voltage is equal to the difference of the two channels' output voltages, plus a DC offset:

$V_{ODF} = (V_{OA} – V_{OB}) + V_{OS}$, if INV pin is held low, (<1V)

$V_{ODF} = (V_{OB} – V_{OA}) + V_{OS}$, if INV pin is held high, (>2V)

**RT1 (Pin 17):** First Order Output Temperature Compensation Pin for Both Channels. Connect this pin to ground to disable. The output voltage will increase or decrease with the ambient temperature by connecting this pin to ground via an off-chip resistor, depending on the polarity set by RP1 pin.

**$V_{OA}$, $V_{OB}$ (Pins 18, 13):** DC Output of Channel A and Channel B, respectively.

**$V_{CCN}$ (Pin 19):** Power Supply Pin for the Envelope Detectors in Both Channels. Typical total current consumption of this pin is 9.6mA. This pin should be bypassed with 1nF and 1µF capacitors. Connect this pin to ground to disable the envelope detectors.

**ENVA, ENVB (Pins 20, 11):** Envelope Detector Output Pins for Channel A and Channel B, respectively. Each output tracks the input signal's RF envelope and outputs a DC voltage directly proportional to the signal power, normalized to the average power.

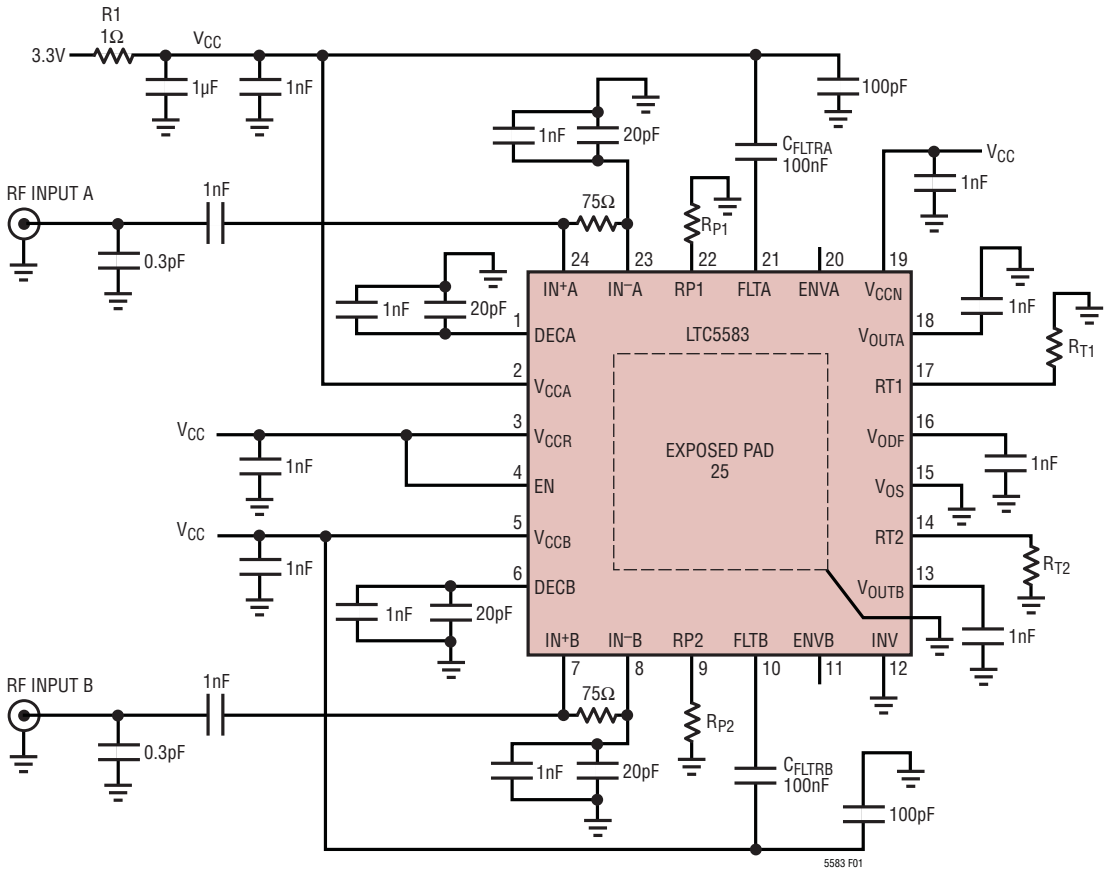
**FLTA, FLTB (Pins 21, 10):** Connection for an External Filtering Capacitor for Channel A and Channel B, respectively. A minimum 8nF capacitor is required for stable AC average power measurement. Each capacitor should be connected between FLTA and $V_{CCA}$, and between FLTB and $V_{CCB}$.

**RP1 (Pin 22):** Pin for Setting Polarity of First Order Output Temperature Compensation. Connect this pin to ground to change the output voltage proportional to ambient temperature. Float this pin to change the output voltage inversely proportional to ambient temperature.

**$IN^+A$, $IN^-A$, $IN^+B$, $IN^-B$ (Pins 24, 23, 7, 8):** Differential RF Input Signal Pins for Channel A and Channel B. Each channel can be driven with a single-ended or differential signal. These pins are internally biased to 1.6V and should be DC-blocked externally. The differential impedance is 400Ω.

**GND (Exposed Pad Pin 25):** Circuit Ground Return for the Entire IC. This must be soldered to the printed circuit board ground plane.

## TEST CIRCUITS

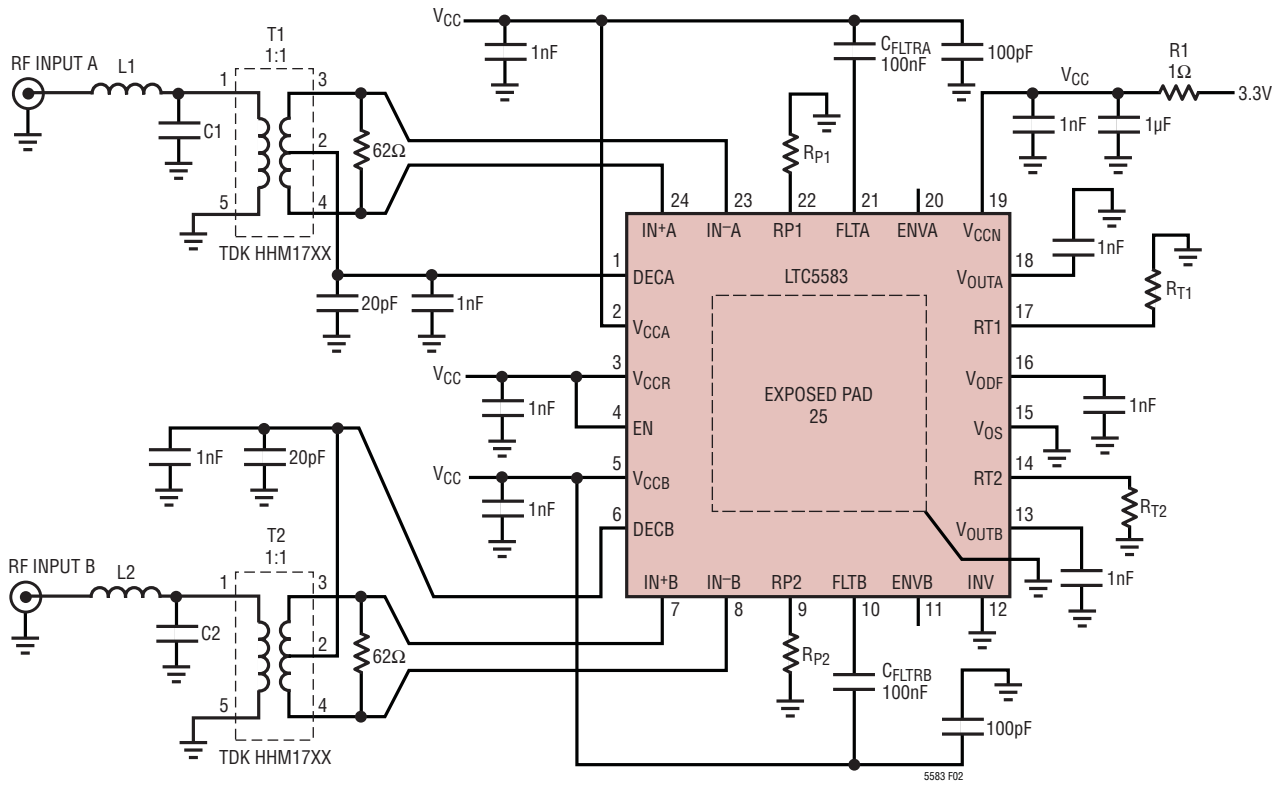



| COMP | VALUE | SIZE | PART NUMBER |
|---|---|---|---|
| C | 20pF | 0402 | Murata GRM1555CIH200JB01 |
| C | 100pF | 0402 | Murata GRM1555CIH101JDO1B |
| C | 1nF | 0402 | Murata GRM155R71H102KA01D |
| C | 100nF | 0402 | Murata GRM155R61A104KA01 |
| C | 1µF | 0402 | Murata GRM155R60J105KE19 |
| R | 75Ω | 0402 | Vishay CRCW040275R0FKED |

| FREQUENCY | RP1 | RP2 | RT1 | RT2 | INPUT RETURN LOSS |
|---|---|---|---|---|---|
| 450MHz | Open | 0Ω | 11.5kΩ | 1.13kΩ | 21dB |
| 880MHz | Open | 0Ω | 11.5kΩ | 1.13kΩ | 14dB |
| 2140MHz | Open | 0Ω | 9.76kΩ | 1.10kΩ | 14dB |
| 2700MHz | Open | 0Ω | 8.87kΩ | 1.21kΩ | 14dB |

**Figure 1. Test Circuit Optimized for 40MHz to 3GHz Operation in Single-Ended Input Configuration**

## TEST CIRCUITS




| COMP | VALUE | SIZE | PART NUMBER |
|---|---|---|---|
| C | 20pF | 0402 | Murata GRM1555CIH200JB01 |
| C | 100pF | 0402 | Murata GRM1555CIH101JD01B |
| C | 1nF | 0402 | Murata GRM155R71H102KA01D |
| C | 100nF | 0402 | Murata GRM155R61A104KA01 |
| C | 1µF | 0402 | Murata GRM155R60J105KE19 |
| R | 62Ω | 0402 | Vishay CRCW040262R0FKED |

| FREQUENCY | L1, L2 | C1, C2 | T1, T2 | RP1 | RP2 | RT1 | RT2 | INPUT RETURN LOSS |
|---|---|---|---|---|---|---|---|---|
| 2140MHz | 2.7nH | 1pF | Murata LDB212G1005C-001 | Open | 0 | 9.76kΩ | 1.10kΩ | 15dB |
| 2700MHz | 1.5nH | X | TDK_HHM1710J1 | Open | 0 | 8.87kΩ | 1.21kΩ | 15dB |
| 3600MHz | 1.2nH | 0.3pF | TDK_HHM1727D1 | Open | 0 | 10.2kΩ | 1.65kΩ | 17dB |
| 5800MHz | Short | 0.3pF | TDK_HHM1733B1 | Open | 0 | 10.0kΩ | 1.47kΩ | 11dB |

**Figure 2. Test Circuit Optimized for 2GHz to 6GHz Operation in Differential Input Configuration**

## TEST CIRCUITS

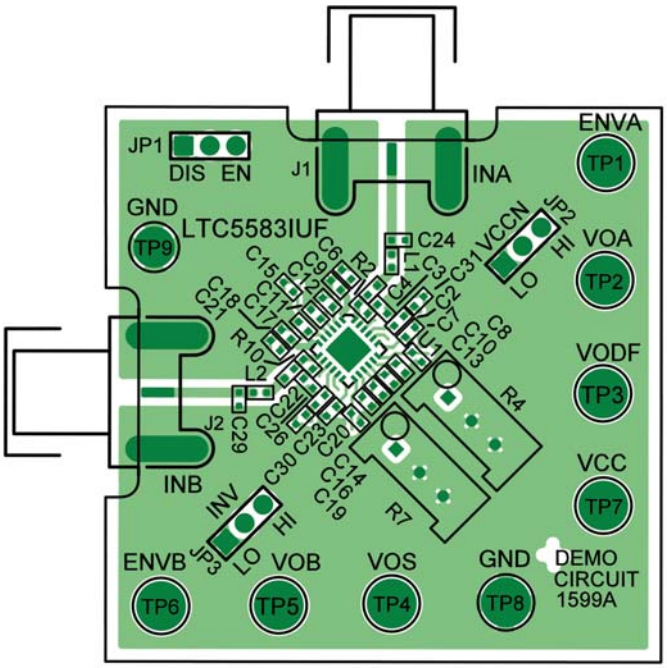



**Figure 3. Top Side of Evaluation Board for Single-Ended Input Configuration**

## APPLICATIONS INFORMATION

The LTC5583 is a dual-channel true RMS power detector, capable of measuring two RF signals over the frequency range from 40MHz to 6GHz, independent of input waveforms with different crest factors such as CW, CDMA2K, WCDMA, LTE and WiMAX signals. Up to 60dB dynamic range is achieved with very stable output over the full temperature range from –40°C to 85°C. Input sensitivity can be as low as –56dBm up to 2.7GHz even with single-ended 50Ω input termination.

### RF Inputs

The differential RF inputs are internally biased at 1.6V. The differential impedance is about 400Ω. These pins should be DC blocked when connected to ground or other matching components.

The LTC5583 can be driven in a single-ended configuration. The single-ended input impedance vs frequency is given in Table 1. Figure 4 shows the simplified circuit of this single-ended configuration for each channel. The DECA pin can be either left floating or AC-coupled to ground via an external capacitor. While the RF signal is applied to the $IN^+A$ (or $IN^-A$) pin, the other pin, $IN^-A$ (or $IN^+A$), should be AC-coupled to ground. By simply terminating the signal side of the inputs with a 75Ω resistor in front of the AC-blocking capacitor and coupling the other side to ground using a 1nF capacitor, a broadband 50Ω input match can be achieved with typical input return loss better than 14dB from 40MHz to 2.7GHz. At higher RF frequencies, additional matching components may be needed. Contact LTC Applications for more information.

**Table 1. Single-Ended Input Impedance**

| FREQUENCY (MHz) | INPUT IMPEDANCE (Ω) | S11 | |
|---|---|---|---|
| | | MAG | ANGLE (°) |
| 40 | 207.4 – j15.5 | 0.613 | –2.2 |
| 100 | 193.0 – j34.0 | 0.599 | –5.4 |
| 200 | 188.9 – j56.8 | 0.611 | –8.9 |
| 400 | 151.6 – j68.7 | 0.576 | –15.2 |
| 600 | 127.8 – j62.8 | 0.530 | –19.5 |
| 800 | 107.6 – j66.0 | 0.513 | –26.2 |
| 1000 | 96.1 – j61.5 | 0.485 | –30.3 |
| 1200 | 85.6 – j59.2 | 0.467 | –35.4 |
| 1400 | 76.2 – j57.4 | 0.455 | –41.0 |
| 1600 | 67.7 – j55.0 | 0.445 | –47.1 |
| 1800 | 60.4 – j52.0 | 0.435 | –53.5 |
| 2000 | 54.9 – j48.7 | 0.423 | –59.4 |
| 2200 | 50.3 – j45.6 | 0.414 | –65.2 |
| 2400 | 46.5 – j42.7 | 0.406 | –70.8 |
| 2600 | 43.7 – j39.8 | 0.396 | –76.0 |
| 2800 | 41.6 – j37.0 | 0.384 | –80.8 |
| 3000 | 40.2 – j34.5 | 0.371 | –84.9 |
| 3200 | 39.3 – j32.0 | 0.356 | –88.8 |
| 3400 | 37.8 – j30.1 | 0.350 | –93.1 |
| 3600 | 35.6 – j26.4 | 0.336 | –101.5 |
| 3800 | 35.0 – j23.3 | 0.314 | –107.4 |
| 4000 | 34.4 – j19.8 | 0.291 | –115.0 |
| 4200 | 33.6 – j16.7 | 0.275 | –123.2 |
| 4400 | 32.9 – j14.2 | 0.264 | –130.6 |
| 4600 | 31.7 – j11.1 | 0.260 | –141.0 |
| 4800 | 30.5 – j8.0 | 0.261 | –152.0 |
| 5000 | 29.3 – j5.1 | 0.268 | –162.5 |
| 5200 | 28.0 – j2.1 | 0.283 | –173.0 |
| 5400 | 26.7 + j0.5 | 0.304 | 178.4 |
| 5600 | 25.4 + j2.7 | 0.328 | 171.7 |
| 5800 | 24.2 + j4.8 | 0.353 | 165.8 |
| 6000 | 23.1 + j6.6 | 0.377 | 161.1 |

## APPLICATIONS INFORMATION

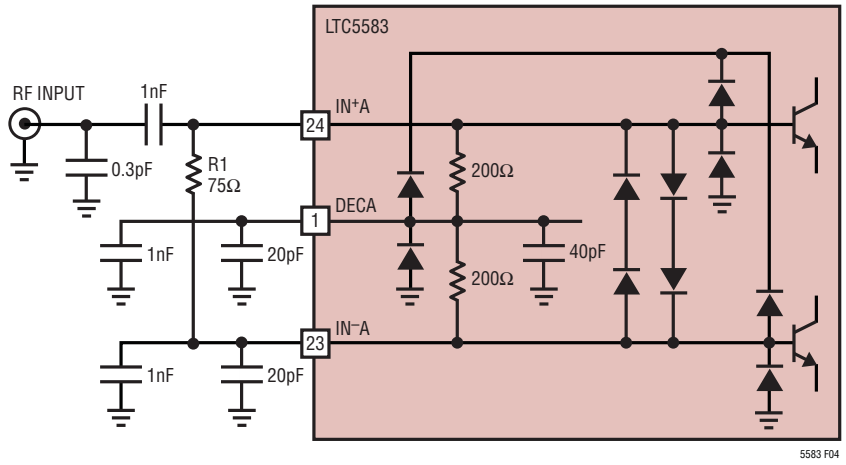



**Figure 4. Single-Ended Input Configuration**

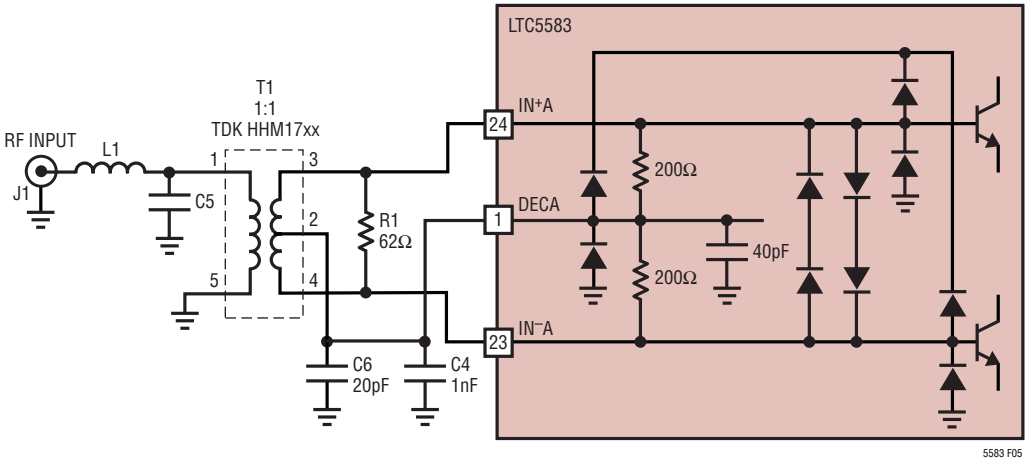



**Figure 5. Differential Input Configuration**

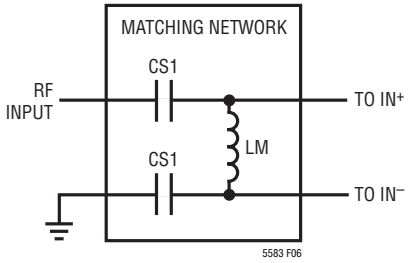



**Figure 6. Single-Ended to Differential Conversion**

## APPLICATIONS INFORMATION

The LTC5583 differential inputs can also be driven from a fully balanced source as shown in Figure 5. When the two input sources are single-ended, conversion to differential signals can improve channel-to-channel isolation to obtain accurate outputs from the dual channels, particularly at very high frequencies (i.e. 3.6GHz and above). This can be achieved using a 1:1 balun to match the chip's internal 400Ω input impedance to the 50Ω source by adding a 62Ω resistor (R1) at the differential inputs as shown in Figure 5. Since there is no voltage conversion gain from impedance transformation in this case, the sensitivity of the detector is similar to the one using single-ended inputs as shown in Figure 4.

If better sensitivity is needed, a 1:4 balun can be used and R1 should be increased to 400Ω correspondingly to match 200Ω input impedance to the 50Ω source. This impedance transformation results in 6dB voltage gain, thus 6dB improvement in sensitivity is obtained while the overall dynamic range remains the same. At high frequency, additional LC elements may be needed for input impedance matching due to the parasitics of the transformer and PCB traces.

Alternatively, a narrowband LC matching network can be used for the conversion of a single-ended signal to a balanced signal. Such a matching network is shown in Figure 6. By this means, the sensitivity and overall linear dynamic range of the detector can be similar to the one using a 1:4 RF input balun, as described above.

For a 50Ω input termination, the approximate RF input power range of the LTC5583 is from –58dBm to 4dBm, even with high crest factor signals such as a 4-carrier W-CDMA waveform, but the minimum detectable RF power level varies as the input RF frequency increases. The linear dynamic range can also be shifted to tailor to a particular application. By simply inserting an attenuator in front of the RF input, the power range is shifted higher by the amount of the attenuation.

The sensitivity of LTC5583 is dictated by the broadband input noise power, which also determines the output DC offset voltage. When the inputs are terminated differently, the DC output voltage may vary slightly. When the input noise power is minimized, the DC offset voltage is also reduced to a minimum, and the sensitivity and dynamic range are improved accordingly.

### External Filtering Capacitors at FLTA and FLTB Pins

These pins are internally biased at $V_{CC}$ – 0.43V via a 1.2k resistor from the $V_{CCA}$ and $V_{CCB}$ voltage supply. To ensure stable operation of the LTC5583, an external capacitor with a value of 8nF or higher is required to connect the FLTA pin to $V_{CCA}$, and the FLTB pin to $V_{CCB}$, respectively. Do not connect these filter capacitors to ground or any other low voltage reference to prevent an abnormal start-up condition.

The value of these two filtering capacitors has a dominant effect on the output transient response. The lower the capacitance, the faster the output rise and fall times. For signals with AM content such as W-CDMA, ripple can be observed when the loop bandwidth set by the filtering capacitors is close to the modulation bandwidth of the signal.

In general, the LTC5583 output ripple remains relatively constant regardless of the RF input power level for a fixed filtering capacitor and modulation format of the RF signal. Typically, this capacitor must be selected to average out the ripple to achieve the desired accuracy of RF power measurement.

## APPLICATIONS INFORMATION

### RMS Power Detector Output: $V_{OA}$, $V_{OB}$

The output buffer amplifier of the LTC5583 is shown in Figure 7. This Class-AB buffer amplifier can output ±5mA current to the load. The output impedance is determined primarily by the 50Ω series resistor connected to the buffer amplifier inside the chip. This will prevent any overstress on the internal devices in the event that the output is shorted to ground.

The –3dB small-signal bandwidth of the buffer amplifier is about 22.4MHz and the full-scale rise/fall time can be as fast as 140ns, limited by the slew rate of the internal circuit instead. When the output is resistively terminated or open, the fastest output transient response is achieved when a large signal is applied to the RF input. The rise time of the LTC5583 is about 140ns and the fall time is 3.5µs, respectively, for full-scale pulsed RF input power with 8.2nF filtering capacitors. The speed of the output transient response is dictated mainly by the filtering capacitors (at least 8nF) at the FLTA and FLTB pins. See the detailed output transient response in the Typical Performance Characteristics section. When the RF input has AM content, residual ripple may be present at the output depending upon the low frequency content of the modulated RF signal. This ripple can be reduced with a larger filtering capacitor at the expense of a slower transient response.

Since the output buffer amplifier of the LTC5583 is capable of driving an arbitrary capacitive load, the residual ripple can be further filtered at the output with a series resistor $R_{SS}$ and a large shunt capacitor $C_{LOAD}$ (see Figure 7). This lowpass filter also reduces the output noise by limiting the output noise bandwidth. When this RC network is designed properly, a fast output transient response can be maintained with reduced residual ripple. For example, we can estimate $C_{LOAD}$ with an output voltage swing of 1.7V at 2140MHz. In order to not allow the maximum 5mA sourcing current to limit the fall time (about 5µs), the maximum value of $C_{LOAD}$ can be chosen as follows:

$$C_{LOAD} \leq 5mA \bullet \text{Allowable Additional Time}/1.7V$$
$$= 5mA \bullet 0.25\mu s/1.7V = 735pF$$

Once $C_{LOAD}$ is determined, $R_{SS}$ can be chosen properly to form an RC low-pass filter with a corner frequency of $1/[2\pi \bullet (R_{SS} + 50) \bullet C_{LOAD}]$.

In general, the rise time of the LTC5583 is much shorter than the fall time. However, when the output RC filter is used, the rise time may be dominated by the time constant of this filter. Accordingly, the rise time becomes very similar to the fall time. Although the maximum sinking capability of the LTC5583 is 5mA, it is recommended that the output load resistance should be greater than 1.2k in order to achieve the full output voltage swing.

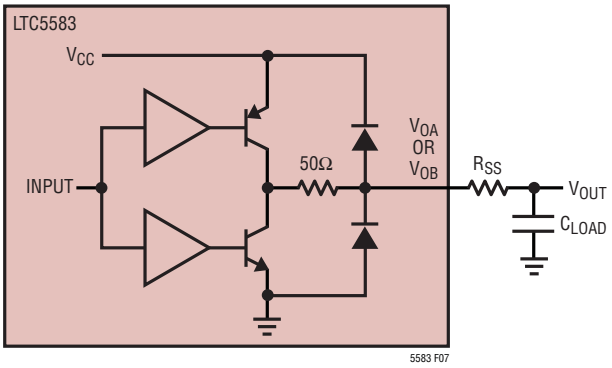



**Figure 7. Simplified Circuit Schematic of the RMS Power Detector Output Interface**

## APPLICATIONS INFORMATION

### Temperature Compensation of Logarithmic Intercept

The simplified interface schematics of the intercept temperature compensation are shown in Figure 8 and Figure 9. The adjustment of the output voltage can be described by the following equation with respect to the ambient temperature:

$$\Delta V_{OUT} = TC1 \bullet (T_A - t_{NOM}) + TC2 \bullet (T_A - t_{NOM})^2 + detV1 + detV2$$

where TC1 and TC2 are the first order and second order temperature compensation coefficients, respectively; $T_A$ is the actual ambient temperature; and $t_{NOM}$ is the reference room temperature 25°C; detV1 and detV2 are the output voltage variation when $R_{T1}$ and $R_{T2}$ are not set to zero.

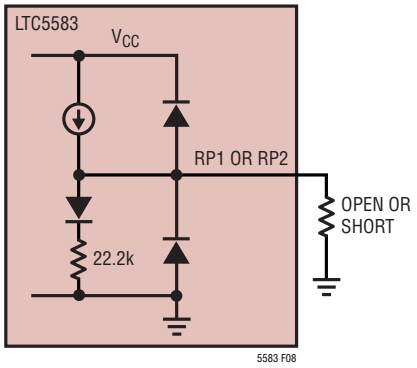



**Figure 8. Simplified Interface Circuit Schematic of the Polarity Pins RP1 and RP2**

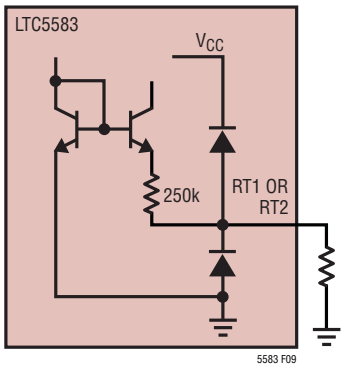



**Figure 9. Simplified Interface Circuit Schematic of the Control Pins RT1 and RT2**

## APPLICATIONS INFORMATION

The temperature coefficients TC1 and TC2 are shown as functions of the tuning resistors $R_{T1}$ and $R_{T2}$ in Figure 10 and Figure 11.

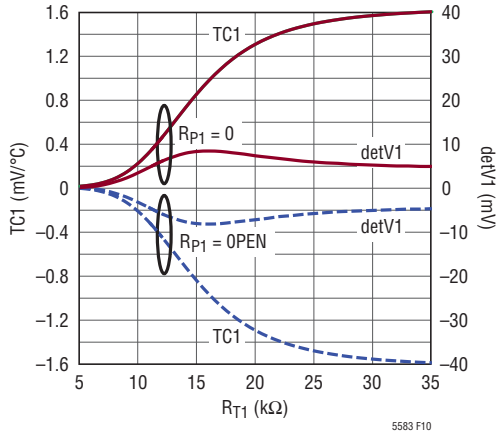



**Figure 10. First Order Temperature Compensation Coefficient TC1 vs External RT1 Value**

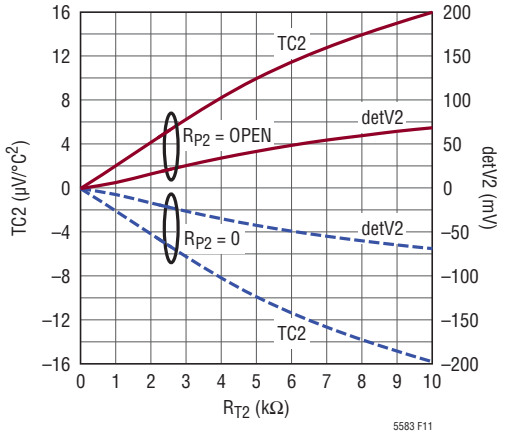



**Figure 11. Second Order Temperature Compensation Coefficient TC2 vs External RT2 Value**

When pins RT1 and RT2 are shorted to ground, the temperature compensation circuit is disabled automatically. Polarity of the temperature coefficient TC1 (or TC2), can be selected by either shorting the RP1 pin (or RP2 pin) to ground or leaving it open, while the coefficients' values can be controlled by external resistors $R_{T1}$ and $R_{T2}$ independently, according to Figures 10 and 11. At a given RF frequency, the polarities and optimal values of TC1 and TC2 can be chosen to ensure a stable output over the operating temperature range. Table 2 lists the suggested $R_{P1}$, $R_{P2}$, $R_{T1}$ and $R_{T2}$ values at various RF frequencies for the best output performance over temperature.

**Table 2. Suggested $R_P$ and $R_T$ Values for Optimal Temperature Performance vs RF Frequency**

| Frequency (MHz) | $R_{P1}$ | $R_{T1}$ (kΩ) | $R_{P2}$ | $R_{T2}$ (kΩ) |
|---|---|---|---|---|
| 450 | Open | 11.5 | 0 | 1.13 |
| 880 | Open | 11.5 | 0 | 1.13 |
| 2140 | Open | 9.76 | 0 | 1.10 |
| 2700 | Open | 8.87 | 0 | 1.21 |
| 3600 | Open | 10.2 | 0 | 1.65 |
| 5800 | Open | 10.0 | 0 | 1.47 |

## APPLICATIONS INFORMATION

### Envelope Detector Output: ENVA, ENVB

Each envelope detector output linearly follows the instantaneous input power level, tracking the input signal's RF envelope. ENVA and ENVB also indicate the peak-to-average power ratio (crest factor). Thus, reading both $V_{OA}$ and ENVA provides the average power, peak-to-average power ratio, peak power, and RF envelope of the input signal to Channel A. Reading $V_{OB}$ and ENVB provides the same information for Channel B.

### Enable: EN

A simplified schematic of the EN pin interface is shown in Figure 13. The enable voltage necessary to turn on the LTC5583 is 2V. To disable or turn off the chip, set this voltage below 0.3V. It is important that the voltage applied to the EN pin should never exceed $V_{CC}$ by more than 0.3V. Otherwise, the supply current may be sourced through the upper ESD protection diode connected at the EN pin. Under no circumstances should voltage be applied to the EN pin before the supply pins ($V_{CCA}$, $V_{CCB}$, $V_{CCR}$, $V_{CCN}$). If this occurs, damage to the IC may result.

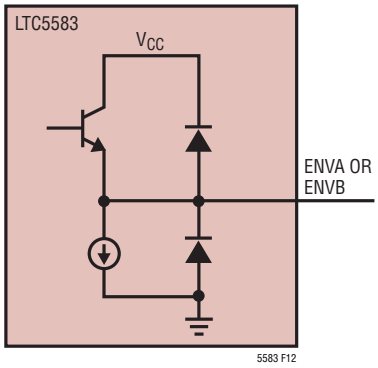



**Figure 12. Simplified Schematic of the ENVA and ENVB Pin**

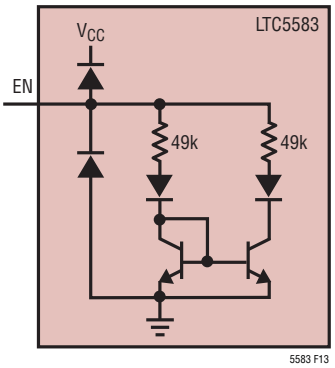



**Figure 13. Simplified Schematic of the Enable Pin**

## APPLICATIONS INFORMATION

### Difference Output: $V_{ODF}$

This voltage is equal to the difference of the two channels' output voltages, plus a DC offset:

$V_{ODF} = (V_{OA} - V_{OB}) + V_{OS}$
if INV voltage < 1V.

$V_{ODF} = (V_{OB} - V_{OA}) + V_{OS}$
if INV voltage > 2V.

A simplified schematic of the $V_{ODF}$ interface is shown in Figure 14. The low 5Ω output impedance at this pin is due to internal feedback circuitry.

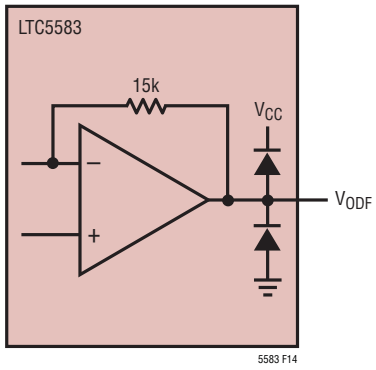



**Figure 14. Simplified Schematic of the $V_{ODF}$ Pin**

Figure 15 shows a simplified schematic of the INV pin interface. INV determines the sign of the difference function at the $V_{ODF}$ output.

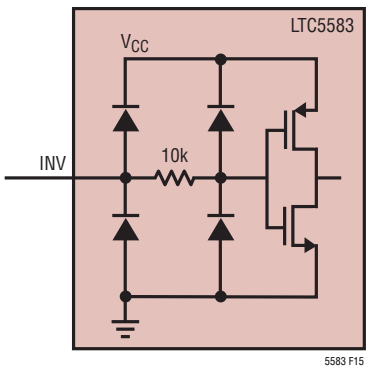



**Figure 15. Simplified Schematic of the INV Pin**

A simplified schematic of the $V_{OS}$ pin interface is shown in Figure 16. The output range of $V_{ODF}$ is from 50mV to $V_{CC}$ – 50mV; it cannot go below 50mV. If $V_{OA} - V_{OB}$ is negative (for INV = low), a positive offset voltage $V_{OS}$ is needed. Similarly, if $V_{OB} - V_{OA}$ is negative (for INV = high), a positive offset voltage $V_{OS}$ is needed.

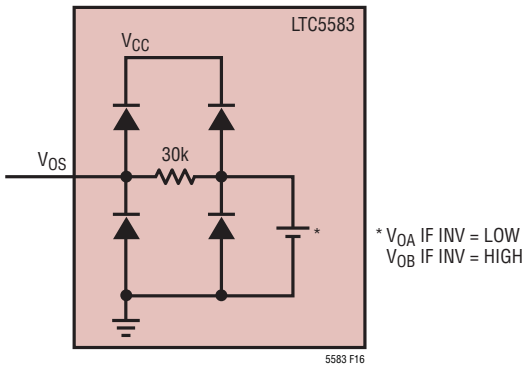



**Figure 16. Simplified Schematic of the $V_{OS}$ Pin**

### Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage overshoot at initial turn-on that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended. In case this voltage ramp time is not controllable, a small (i.e. 1Ω) series resistor can be inserted between $V_{CC}$ pin and the supply voltage source to mitigate the problem and protect the IC. The R1 shown in Figures 1 and 2 serves this purpose.