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Wideband IQ Demodulator with IIP2 and DC Offset Control

FEATURES

- **400MHz to 4GHz Operating Frequency**
- **High IIP3: 28.7dBm at 700MHz, 25.7dBm at 1.95GHz**
- **High IIP2: 70dBm at 700MHz, 60dBm at 1.95GHz**
- **User Adjustable IIP2 Up to 80dBm**
- **User Adjustable DC Offset Null**
- **High Input P1dB: 16dBm at 1950MHz**
- **I/Q Bandwidth of 530MHz or Higher**
- **Image Rejection: 43dB at 1950MHz**
- Noise Figure: 13.5dB at 700MHz
  12.7dB at 1.95GHz
- Conversion Gain: 2.0dB at 700MHz
  2.4dB at 1.95GHz
- Single-Ended RF with On-Chip Transformer
- Shutdown Mode
- Operating Temperature Range (T_C): –40°C to 105°C
- 24-Lead 4mm × 4mm QFN Package

APPLICATIONS

- LTE/W-CDMA/TD-SCDMA Base Station Receivers
- Wideband DPD Receivers
- Point-To-Point Broadband Radios
- High Linearity Direct Conversion I/Q Receivers
- Image Rejection Receivers

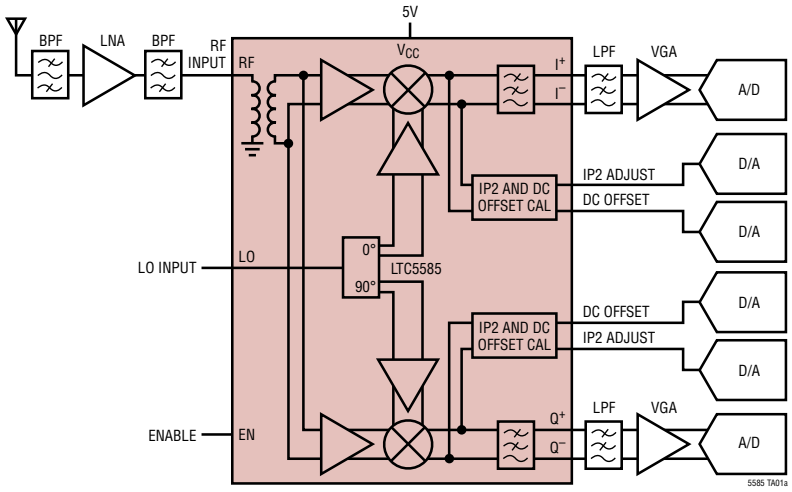
DESCRIPTION

The LTC®5585 is a direct conversion quadrature demodulator optimized for high linearity receiver applications in the 400MHz to 4GHz frequency range. It is suitable for communications receivers where an RF signal is directly converted into I and Q baseband signals with bandwidth of 530MHz or higher. The LTC5585 incorporates balanced I and Q mixers, LO buffer amplifiers and a precision, high frequency quadrature phase shifter. The integrated on-chip broadband transformer provides a single-ended interface at the RF input with simple off-chip L-C matching. In addition, the LTC5585 provides four analog control voltage interface pins for IIP2 and DC offset correction, greatly simplifying system calibration.

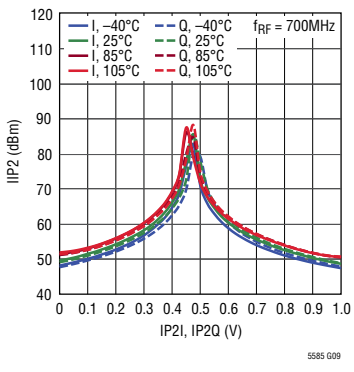
The high linearity of the LTC5585 provides excellent spur-free dynamic range for the receiver. This direct conversion demodulator can eliminate the need for intermediate frequency (IF) signal processing, as well as the corresponding requirements for image filtering and IF filtering. These I/Q outputs can interface directly to channel-select filters (LPFs) or to baseband amplifiers.

TYPICAL APPLICATION

Direct Conversion Receiver with IIP2 and DC Offset Calibration



IIP2 vs IP2I, IP2Q Trim Voltage

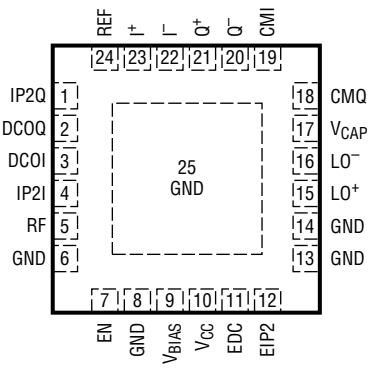


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Supply Voltage ..... –0.3V to 5.5V
V_{CAP} Voltage ..... V_{CC} ±0.05V
I^-, I^+, Q^+, Q^-, CMI, CMQ Voltage .....2.5V to V_{CC} + 0.3V
Voltage on Any Other Pin .....–0.3V to V_{CC} + 0.3V
LO^+, LO^-, RF Input Power 20dBm
RF Input DC Voltage..... ±0.1V
Maximum Junction Temperature (T_{JMAX}) ..... 150°C
Operating Temperature Range (T_C) ..... –40°C to 105°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 7°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5585IUF#PBF	LTC5585IUF#TRPBF	5585	24-Lead (4mm x 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

T_C = 25°C, V_{CC} = 5V, EN = 5V, EDC = EIP2 = 0V, REF = IP2I = IP2Q = DCOI = DCOQ = 0.5V, P_{RF} = –5dBm (–5dBm/tone for 2-tone IIP2 and IIP3 tests), P_{LO} = 6dBm, unless otherwise noted. (Notes 2, 3, 5, 6, 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$f_{RF(RANGE)}$	RF Input Frequency Range	(Note 12)		0.4 to 4.0		GHz
$f_{LO(RANGE)}$	LO Input Frequency Range	(Note 12)		0.4 to 4.0		GHz
$P_{LO(RANGE)}$	LO Input Power Range	(Note 12)		0 to 10		dBm
f_{RF1} = 700MHz, f_{RF2} = 701MHz, f_{LO} = 690MHz, L6 = 2.7pF, C19 = 1.0pF, L5 = 12nH, C14 = 5.6pF						
$f_{RF(MATCH)}$	RF Input Frequency Range	Return Loss > 10dB		680 to 870		MHz
$f_{LO(MATCH)}$	LO Input Frequency Range	Return Loss > 10dB		690 to 820		MHz
G_V	Voltage Conversion Gain	Loaded with 100Ω Pull-Up (Note 8)		2.0		dB
NF	Noise Figure	Double-Side Band (Note 4)		13.5		dB
$NF_{BLOCKING}$	Noise Figure Under Blocking Conditions	Double-Side Band, P_{RF} = 0dBm (Note 7)		15.5		dB
IIP3	Input 3rd Order Intercept			28.7		dBm
IIP2	Input 2nd Order Intercept	Unadjusted, EIP2 = 0V		70		dBm
$IIP2_{OPT}$	Optimized Input 2nd Order Intercept	EIP2 = 5V, IP2I, IP2Q Adjusted for Minimum IM2		80		dBm
P1dB	Input 1dB Compression			16		dBm

ELECTRICAL CHARACTERISTICS

T_C = 25°C, V_{CC} = 5V, EN = 5V, EDC = EIP2 = 0V, REF = IP2I = IP2Q = DCOI = DCOQ = 0.5V, P_{RF} = –5dBm (–5dBm/tone for 2-tone IIP2 and IIP3 tests), P_{LO} = 6dBm, unless otherwise noted. (Notes 2, 3, 5, 6, 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC_{OFFSET}	DC Offset at I/Q Outputs	Unadjusted, EDC = 0V (Note 13)		4		mV
ΔG	I/Q Gain Mismatch			0.05		dB
Δϕ	I/Q Phase Mismatch			0.3		Deg
IRR	Image Rejection Ratio	(Note 10)		48		dB
LO-RF	LO to RF Leakage			–64		dBm
RF-LO	RF to LO Isolation			60		dB
f_{RF1} = 1950MHz, f_{RF2} = 1951MHz, f_{LO} = 1940MHz, L6 = 1.2pF, C19 = 5.1nH, L5 = 1.0pF, C13 = 5.1nH						
$f_{RF(MATCH)}$	RF Input Frequency Range	Return Loss > 10dB		1.6 to 2.1		GHz
$f_{LO(MATCH)}$	LO Input Frequency Range	Return Loss > 10dB		1.85 to 2.05		GHz
G_V	Voltage Conversion Gain	Loaded with 100Ω Pull-Up (Note 8)		2.4		dB
NF	Noise Figure	Double-Side Band (Note 4)		12.7		dB
IIP3	Input 3rd Order Intercept			25.7		dBm
IIP2	Input 2nd Order Intercept	Unadjusted, EIP2 = 0V		60		dBm
$IIP2_{OPT}$	Optimized Input 2nd Order Intercept	EIP2 = 5V, IP2I, IP2Q Adjusted for Minimum IM2		80		dBm
P1dB	Input 1dB Compression			16		dBm
DC_{OFFSET}	DC Offset at I/Q Outputs	Unadjusted, EDC = 0V (Note 13)		7		mV
ΔG	I/Q Gain Mismatch			0.05		dB
Δϕ	I/Q Phase Mismatch			0.7		Deg
IRR	Image Rejection Ratio	(Note 10)		43		dB
LO-RF	LO to RF Leakage			–49		dBm
RF-LO	RF to LO Isolation			58		dB
f_{RF1} = 2150MHz, f_{RF2} = 2151MHz, f_{LO} = 2140MHz, C17 = 1.5pF, L6 = 4.7nH, C19 = 0.5pF, L5 = 5.1nH, C14 = 0.7pF						
$f_{RF(MATCH)}$	RF Input Frequency Range	Return Loss > 10dB		2.03 to 2.36		GHz
$f_{LO(MATCH)}$	LO Input Frequency Range	Return Loss > 10dB		2.05 to 2.18		GHz
G_V	Voltage Conversion Gain	Loaded with 100Ω Pull-Up (Note 8)		2.3		dB
NF	Noise Figure	Double-Side Band (Note 4)		13.0		dB
$NF_{BLOCKING}$	Noise Figure Under Blocking Conditions	Double-Side Band, P_{RF} = 0dBm (Note 7)		14.6		dB
IIP3	Input 3rd Order Intercept			25.9		dBm
IIP2	Input 2nd Order Intercept	Unadjusted, EIP2 = 0V		56		dBm
$IIP2_{OPT}$	Optimized Input 2nd Order Intercept	EIP2 = 5V, IP2I, IP2Q Adjusted for Minimum IM2		80		dBm
P1dB	Input 1dB Compression			15		dBm
DC_{OFFSET}	DC Offset at I/Q Outputs	Unadjusted, EDC = 0V (Note 13)		6		mV
ΔG	I/Q Gain Mismatch			0.05		dB
Δϕ	I/Q Phase Mismatch			1.0		Deg
IRR	Image Rejection Ratio	(Note 10)		40		dB
LO-RF	LO to RF Leakage			–50		dBm
RF-LO	RF to LO Isolation			60		dB
f_{RF1} = 2600MHz, f_{RF2} = 2601MHz, f_{LO} = 2590MHz, C17 = 0.5pF, L6 = 2.7nH, L5 = 1.2nH, C14 = 1pF						
$f_{RF(MATCH)}$	RF Input Frequency Range	Return Loss > 10dB		2.35 to 3.1		GHz
$f_{LO(MATCH)}$	LO Input Frequency Range	Return Loss > 10dB		2.47 to 2.65		GHz
G_V	Voltage Conversion Gain	Loaded with 100Ω Pull-Up (Note 8)		2.3		dB

ELECTRICAL CHARACTERISTICS

T_C = 25°C, V_{CC} = 5V, EN = 5V, EDC = EIP2 = 0V, REF = IP2I = IP2Q = DCOI = DCOQ = 0.5V, P_{RF} = –5dBm (–5dBm/tone for 2-tone IIP2 and IIP3 tests), P_{LO} = 6dBm, unless otherwise noted. (Notes 2, 3, 5, 6, 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
NF	Noise Figure	Double-Side Band (Note 4)		13.6		dB
$NF_{BLOCKING}$	Noise Figure Under Blocking Conditions	Double-Side Band, P_{RF} = 0dBm (Note 7)		15.2		dB
IIP3	Input 3rd Order Intercept			27.5		dBm
IIP2	Input 2nd Order Intercept	Unadjusted, EIP2 = 0V		60		dBm
$IIP2_{OPT}$	Minimum Input 2nd Order Intercept	EIP2 = 5V, IP2I, IP2Q Adjusted for Minimum IM2		80		dBm
P1dB	Input 1dB Compression			15.5		dBm
DC_{OFFSET}	DC Offset at I/Q Outputs	Unadjusted, EDC = 0V (Note 13)		8		mV
ΔG	I/Q Gain Mismatch			0.05		dB
Δϕ	I/Q Phase Mismatch			1.0		Deg
IRR	Image Rejection Ratio	(Note 10)		40		dB
LO-RF	LO to RF Leakage			–46		dBm
RF-LO	RF to LO Isolation			55		dB
f_{RF1} = 3500MHz, f_{RF2} = 3501MHz, f_{LO} = 3490MHz, C17 = 0.6pF, L6 = 1.0nH, C13 = 0.7pF, L5 = Short, C14 = Open, Single-Ended LO (See Figure 14)						
$f_{RF(MATCH)}$	RF Input Frequency Range	Return Loss > 10dB		2.88 to 3.97		GHz
$f_{LO(MATCH)}$	LO Input Frequency Range	Return Loss > 10dB		2.97 to 3.96		GHz
G_V	Voltage Conversion Gain	Loaded with 100Ω Pull-Up (Note 8)		0.3		dB
NF	Noise Figure	Double-Side Band (Note 4)		17.1		dB
IIP3	Input 3rd Order Intercept			28.1		dBm
IIP2	Input 2nd Order Intercept	Unadjusted, EIP2 = 0V		52.5		dBm
$IIP2_{OPT}$	Minimum Input 2nd Order Intercept	EIP2 = 5V, IP2I, IP2Q Adjusted for Minimum IM2		65.9		dBm
P1dB	Input 1dB Compression			17.1		dBm
DC_{OFFSET}	DC Offset at I/Q Outputs	Unadjusted, EDC = 0V (Note 13)		16.5		mV
ΔG	I/Q Gain Mismatch			0.04		dB
Δϕ	I/Q Phase Mismatch			1.8		Deg
IRR	Image Rejection Ratio	(Note 10)		36		dB
LO-RF	LO to RF Leakage			–34.7		dBm
RF-LO	RF to LO Isolation			44.5		dB
Power Supply and Other Parameters						
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
I_{CC}	Supply Current	EDC = EIP2 = 5V	180	200	220	mA
$I_{CC(LOW)}$	Supply Current	EDC = EIP2 = 0V	170	190	210	mA
$I_{CC(OFF)}$	Shutdown Current	EN < 0.3V		11	900	µA
t_{ON}	Turn-On Time	EN Transition from Logic Low to High (Note 14)		0.2		µs
t_{OFF}	Turn-Off Time	EN Transition from Logic High to Low (Note 15)		0.8		µs
V_{EH}	EN, EDC, EIP2 Input High Voltage (On)		2.0			V
V_{EL}	EN, EDC, EIP2 Input Low Voltage (Off)				0.3	V
I_{ENH}	EN Pin Input Current	EN = 5.0V		52		µA
I_{EDCH}	EDC Pin Input Current	EDC = 5.0V		33		µA

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{EIP2H}	EIP2 Pin Input Current	EIP2 = 5.0V		50		µA
V_{REF}	REF Pin Voltage	With REF Pin Unloaded		0.5		V
$V_{REF(RANGE)}$	REF Pin Voltage Range	When Driven with External Source		0.4 to 0.7		V
Z_{REF}	REF Input Impedance	(Note 11)		2||1		kΩ||pF
	DCOI, DCOQ, IP2I, IP2Q Pin Voltage	Unloaded		0.5		V
	DCOI, DCOQ, IP2I, IP2Q Voltage Range	When Driven with External Source		0 to $2V_{REF}$		V
	DCOI, DCOQ, IP2I, IP2Q Impedance	(Note 11)		8||1		kΩ||pF
	DCOI, DCOQ, IP2I, IP2Q Settling Time	For Step Input, Output with 90% of Final Value		20		ns
	DC Offset Adjustment Range	DCOI, DCOQ Swept from 0V to 1V, EDC = 5V		±20		mV
	DC Offset Drift Over Temperature	Unadjusted, EDC = 0V		20		µV/°C
V_{CM}	I^+, I^-, Q^+, Q^- Common Mode Voltage			V_{CC} – 1.5		V
Z_{OUT}	I^+, I^-, Q^+, Q^- Output Impedance	Single Ended		100||6		Ω||pF
BW_{BB}	I^+, I^-, Q^+, Q^- Output Bandwidth	100Ω External Pull-Up, –3dB Corner Frequency		530		MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Tests are performed with the test circuit of Figure 1.

Note 3: The LTC5585 is guaranteed to be functional over the –40°C to 105°C case temperature operating range.

Note 4: DSB noise figure is measured at the baseband frequency of 15MHz with a small-signal noise source without any filtering on the RF input and no other RF signal applied.

Note 5: Performance at the RF frequencies listed is measured with external RF and LO impedance matching, as shown in the table of Figure 1.

Note 6: The complementary outputs (I^+, I^- and Q^+, Q^-) are combined using a 180° phase-shift combiner.

Note 7: Noise figure under blocking conditions ($NF_{BLOCKING}$) is measured at an output frequency of 60MHz with RF input signal at f_{LO} + 1MHz. Both RF and LO input signals are appropriately filtered, as well as the baseband output. $NF_{BLOCKING}$ measured at 840MHz, 2140MHz and 2500MHz only.

Note 8: Voltage conversion gain is calculated from the average measured power conversion gain of the I and Q outputs using the test circuit shown in Figure 1. Power conversion gain is measured with a 100Ω differential load impedance on the I and Q outputs.

Note 9: Baseband outputs have a 100Ω external pull-up resistor to V_{CC} as shown in the test circuit shown in Figure 1.

Note 10: Image rejection is calculated from the measured gain error and phase error using the method listed in the appendix.

Note 11: The DCOI, DCOQ, IP2I, IP2Q pins have an 8k internal resistor to ground. The REF pin has a 2k internal resistor to ground. If unconnected, these pins will float up to 500mV through internal current sources. A low output resistance voltage source is recommended for driving these pins.

Note 12: This is the recommended operating range, operation outside the listed range is possible with degraded performance to some parameters.

Note 13: DC offset measured differentially between I^+ and I^- and between Q^+ and Q^-. The reported value is the mean of the absolute values of the characterization data distribution.

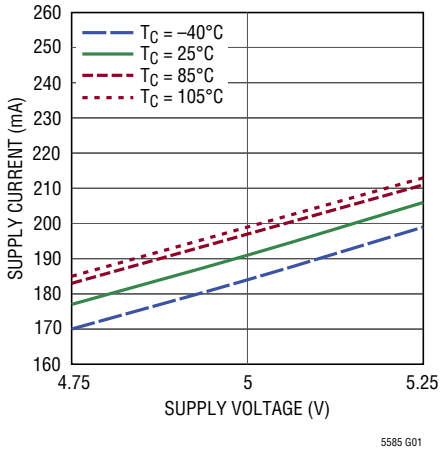
Note 14: Baseband amplitude is within 10% of final value.

Note 15: Baseband amplitude is at least 30dB down from its on state.

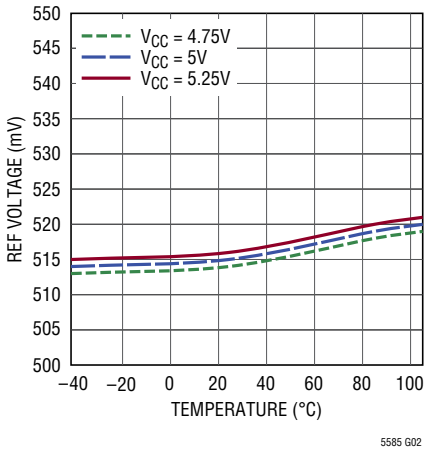
DC PERFORMANCE CHARACTERISTICS

EN = 5V, EDC = 0V and EIP2 = 0V. Test circuit shown in Figure 1

Supply Current vs Supply Voltage



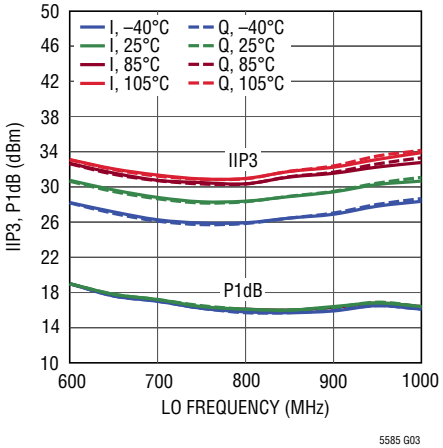
REF Voltage vs Temperature



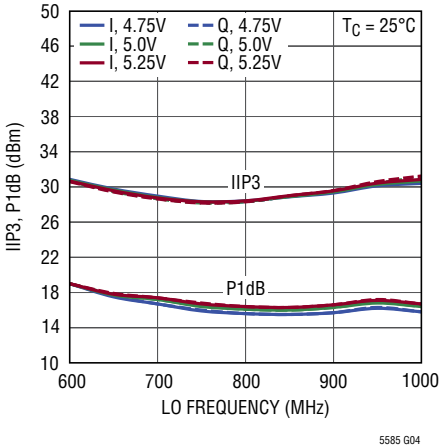
TYPICAL PERFORMANCE CHARACTERISTICS

700MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, EIP2 = 0V, REF = 0.5V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 690MHz, f_{RF1} = 700MHz, f_{RF2} = 701MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

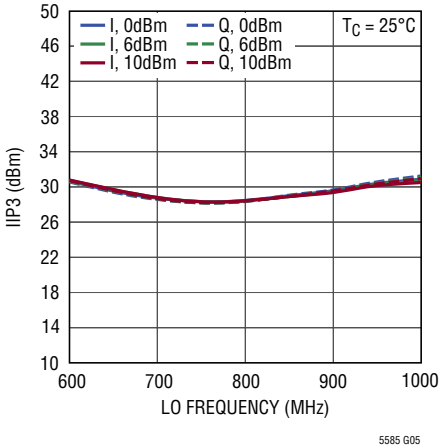
IIP3, P1dB vs Temperature (T_C)



IIP3, P1dB vs Supply Voltage (V_{CC})



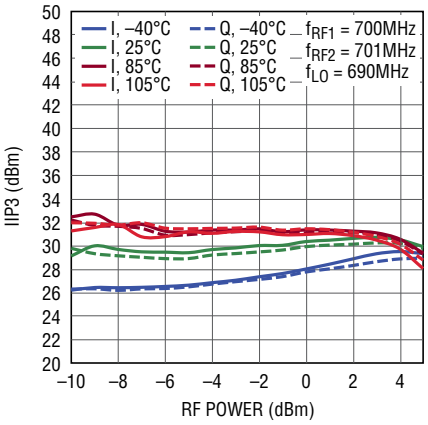
IIP3 vs LO Power



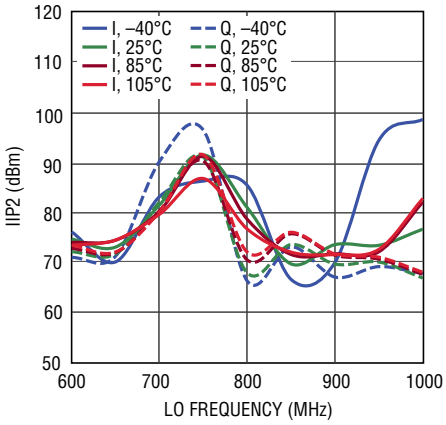
TYPICAL PERFORMANCE CHARACTERISTICS

700MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, EIP2 = 0V, REF = 0.5V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 690MHz, f_{RF1} = 700MHz, f_{RF2} = 701MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

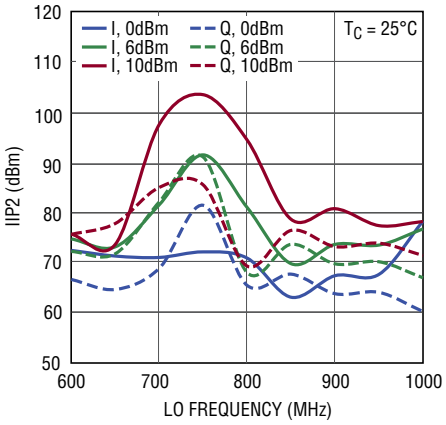
2-Tone IIP3 vs RF Power



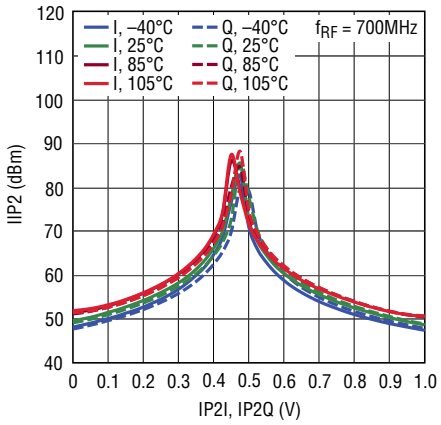
Uncalibrated IIP2 vs Temperature (T_C)



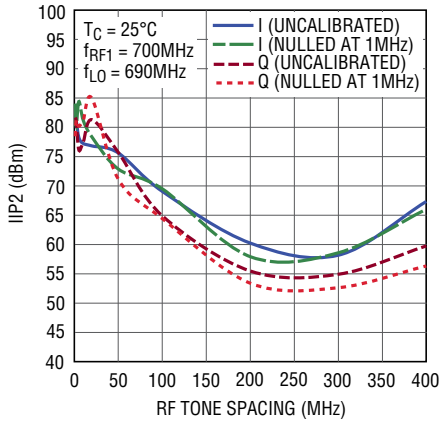
Uncalibrated IIP2 vs LO Power



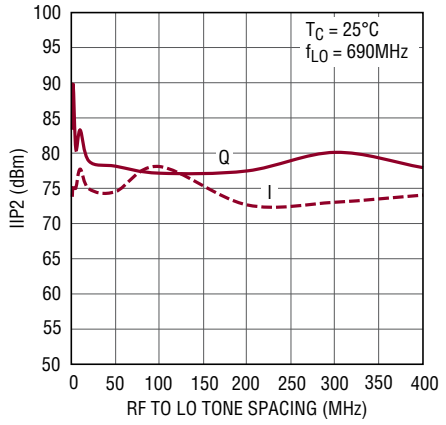
IIP2 vs IP2I, IP2Q Trim Voltage



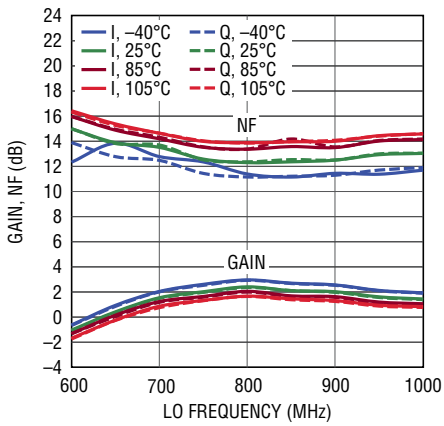
IIP2 vs RF Tone Spacing



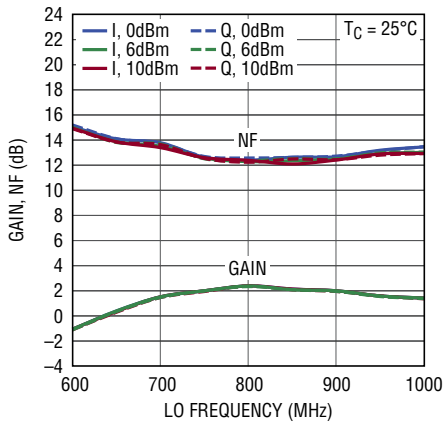
2x2 Half-IF IIP2 vs RF to LO Tone Spacing



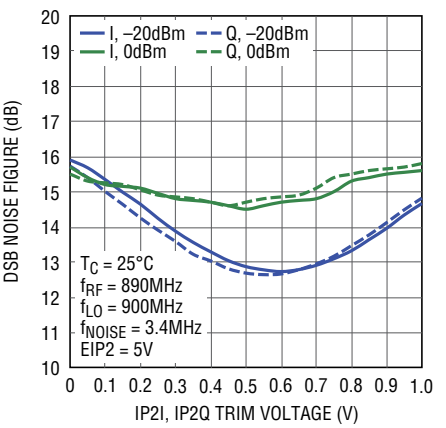
Noise Figure and Conversion Gain vs Temperature (T_C)



Noise Figure and Conversion Gain vs LO Power



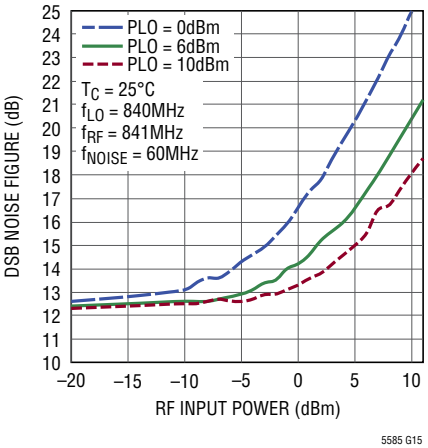
Noise Figure vs RF Power and IP2I, IP2Q Trim Voltage



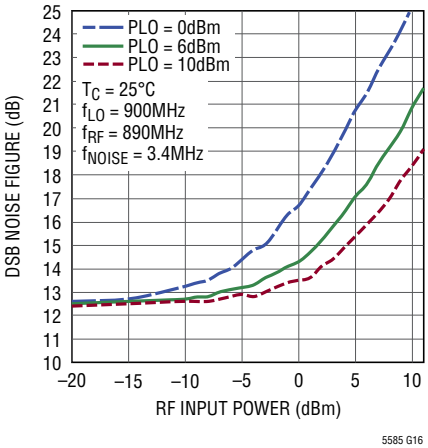
TYPICAL PERFORMANCE CHARACTERISTICS

700MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, EIP2 = 0V, REF = 0.5V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 690MHz, f_{RF1} = 700MHz, f_{RF2} = 701MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

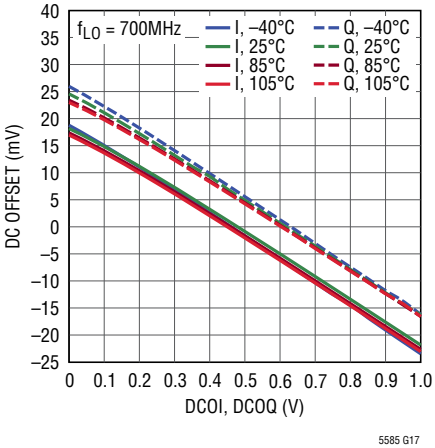
Noise Figure vs RF Input Power with f_{NOISE} = 60MHz



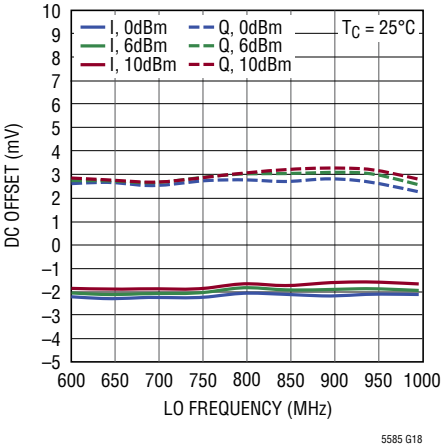
Noise Figure vs RF Input Power with f_{NOISE} = 3.4MHz



DC Offset vs DCOI, DCOQ Control Voltage



DC Offset vs LO Power



LO to RF Leakage and RF to LO Isolation

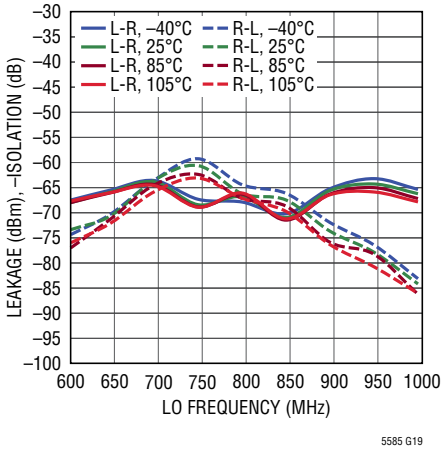
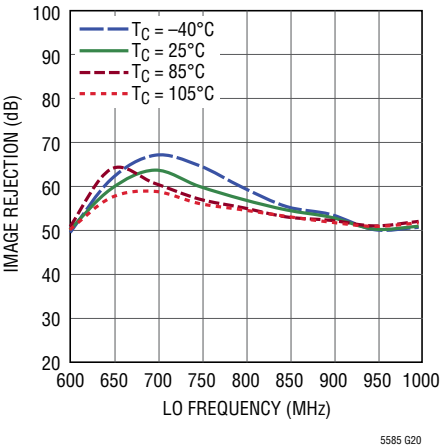


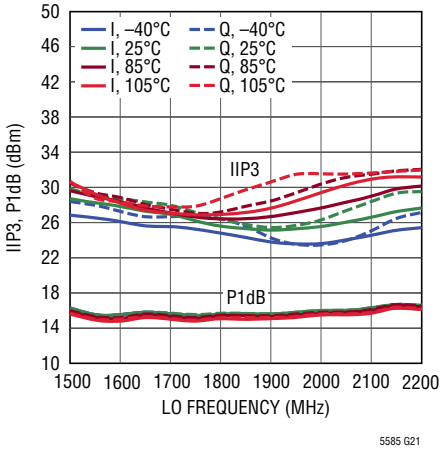
Image Rejection vs Temperature (Note 10)



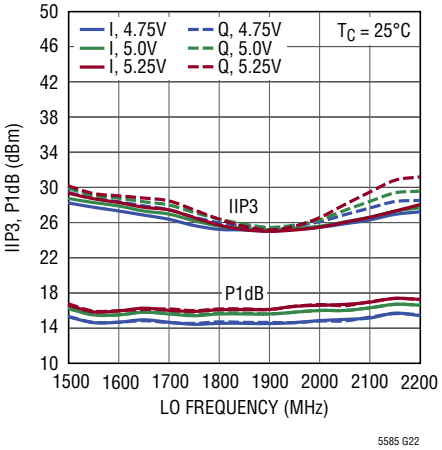
TYPICAL PERFORMANCE CHARACTERISTICS

1950MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, REF = 0.5V, EIP2 = 0V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 1940MHz, f_{RF1} = 1950MHz, f_{RF2} = 1951MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

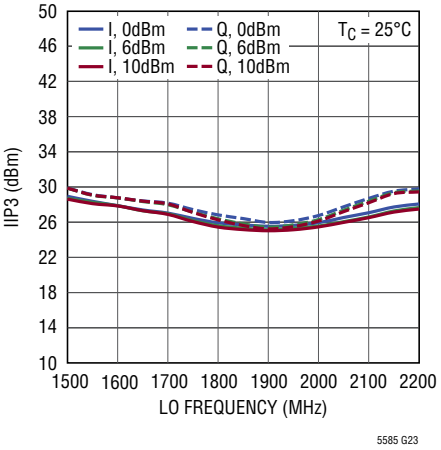
IIP3, P1dB vs Temperature (T_C)



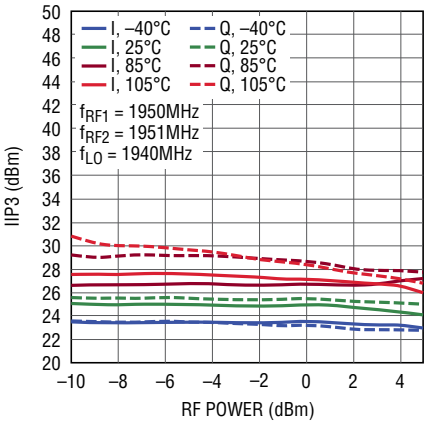
IIP3, P1dB vs Supply Voltage



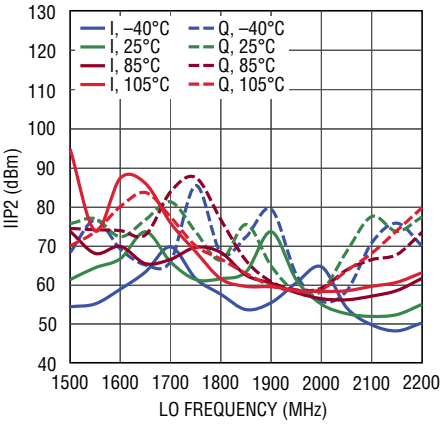
IIP3 vs LO Power



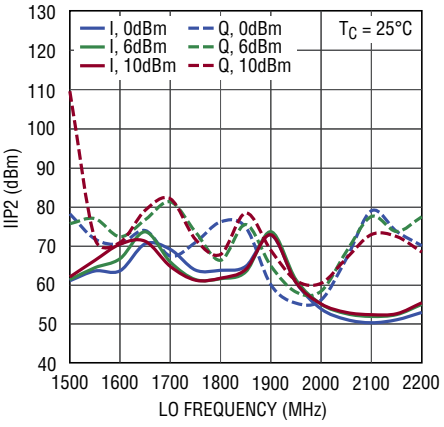
2-Tone IIP3 vs RF Power



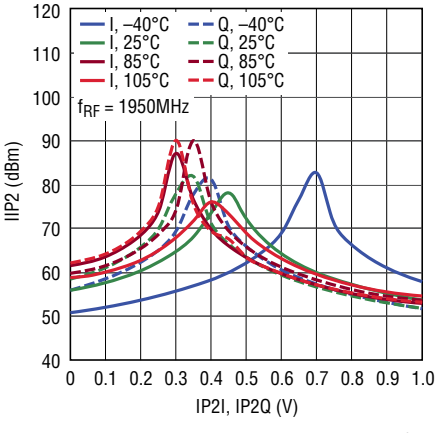
Uncalibrated IIP2 vs Temperature (T_C)



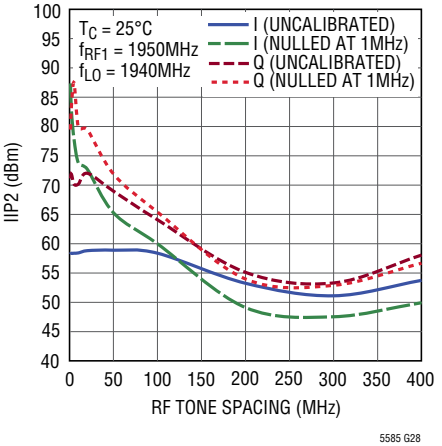
Uncalibrated IIP2 vs LO Power



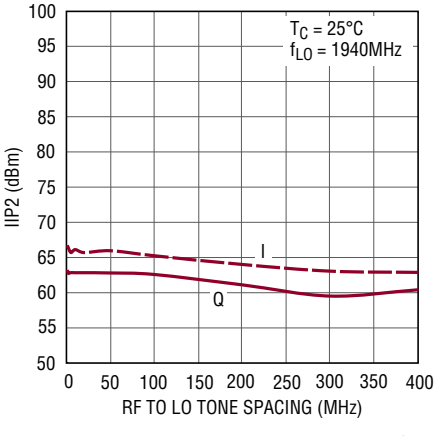
IIP2 vs IP2I, IP2Q Trim Voltage



IIP2 vs RF Tone Spacing



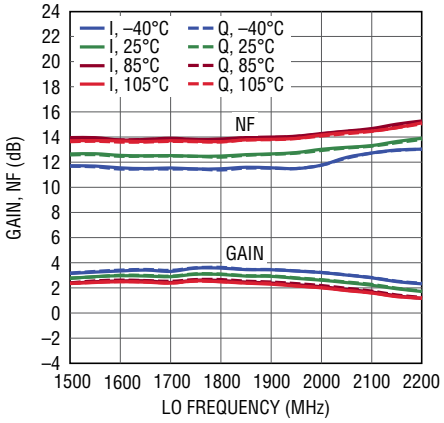
2x2 Half-IF IIP2 vs RF to LO Tone Spacing



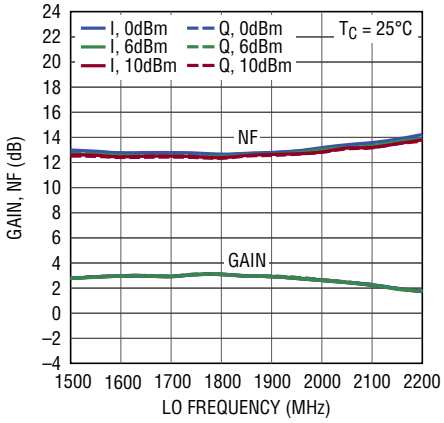
TYPICAL PERFORMANCE CHARACTERISTICS

1950MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, REF = 0.5V, EIP2 = 0V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 1940MHz, f_{RF1} = 1950MHz, f_{RF2} = 1951MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

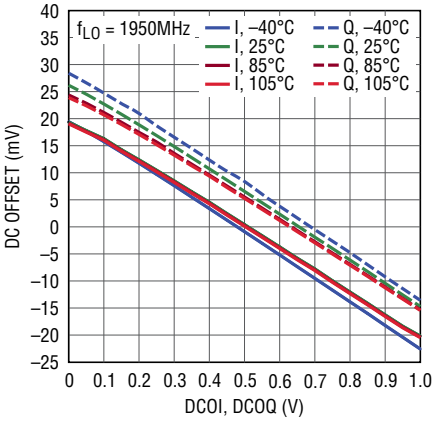
Noise Figure and Conversion Gain vs Temperature (T_C)



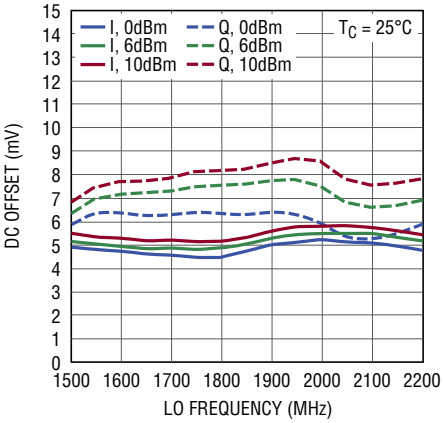
Noise Figure and Conversion Gain vs LO Power



DC Offset vs DCOI, DCOQ Control Voltage



DC Offset vs LO Power



LO to RF Leakage and RF to LO Isolation

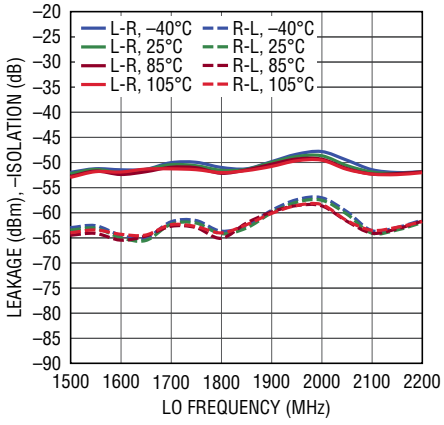
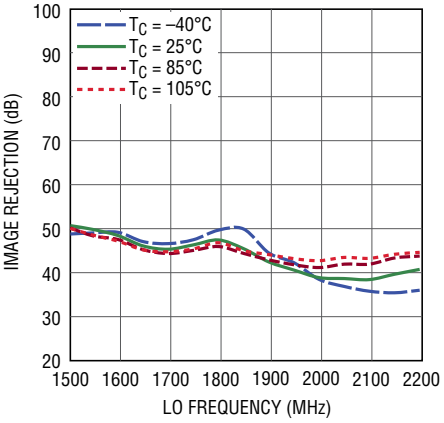
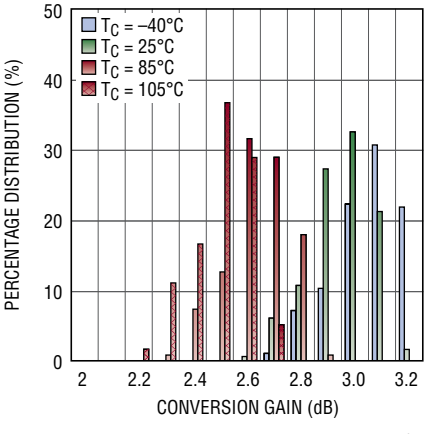


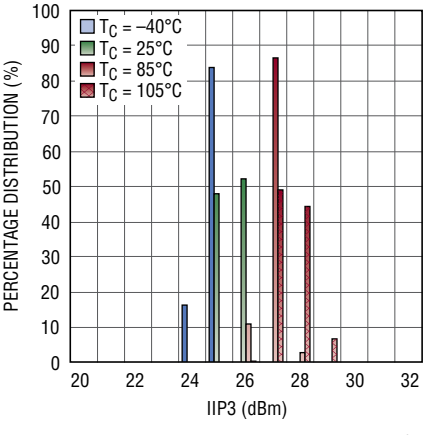
Image Rejection vs Temperature (Note 10)



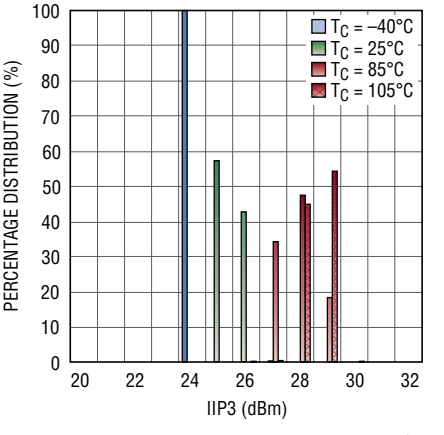
Conversion Gain Distribution



IIP3 Distribution, I Side



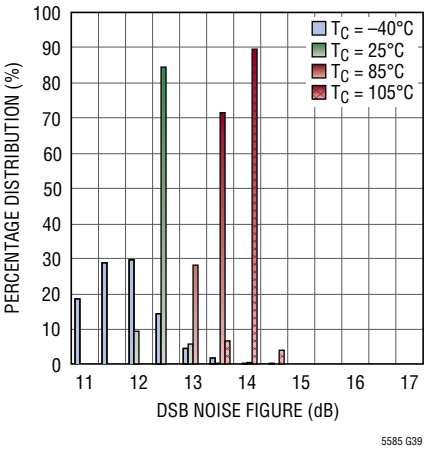
IIP3 Distribution, Q Side



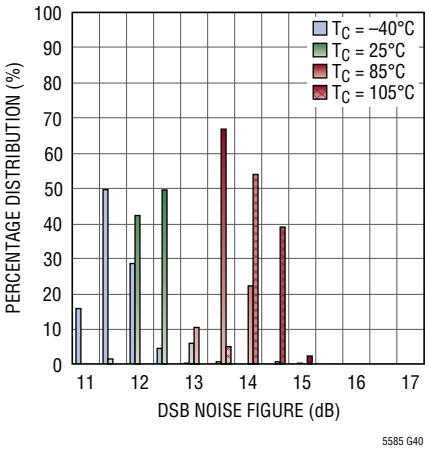
TYPICAL PERFORMANCE CHARACTERISTICS

1950MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, REF = 0.5V, EIP2 = 0V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 1940MHz, f_{RF1} = 1950MHz, f_{RF2} = 1951MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

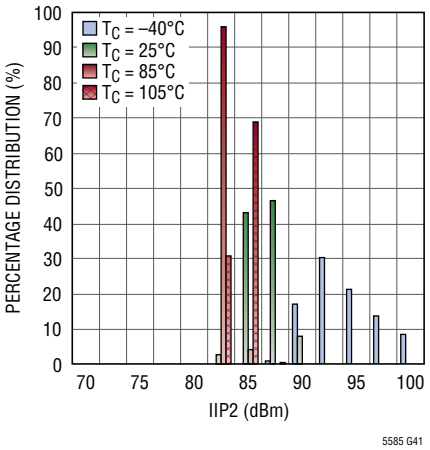
DSB Noise Figure Distribution, I Side



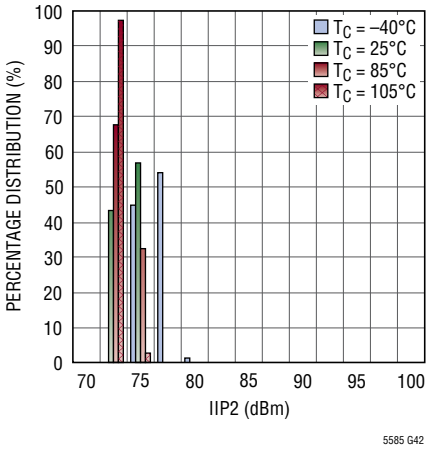
DSB Noise Figure Distribution, Q Side



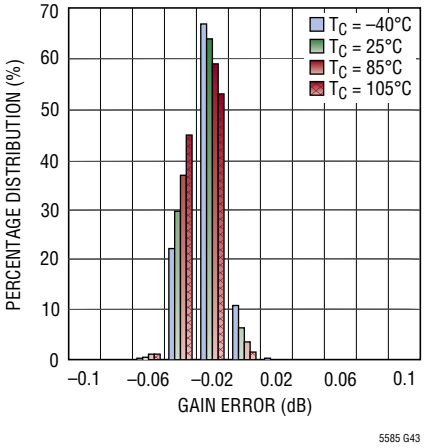
IIP2 Distribution, I Side



IIP2 Distribution, Q Side



Gain Error Distribution



Phase Error Distribution

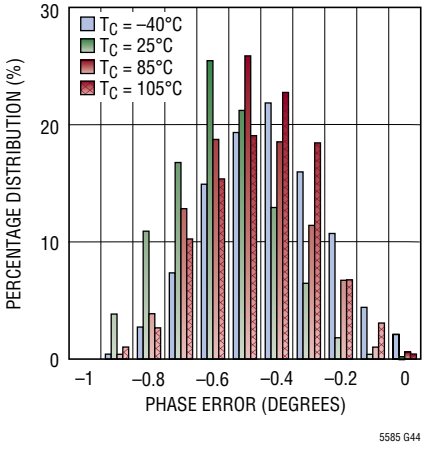
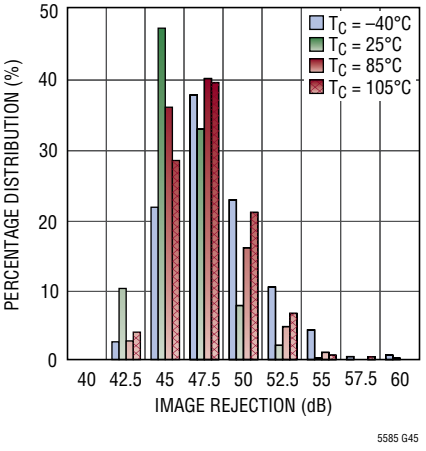


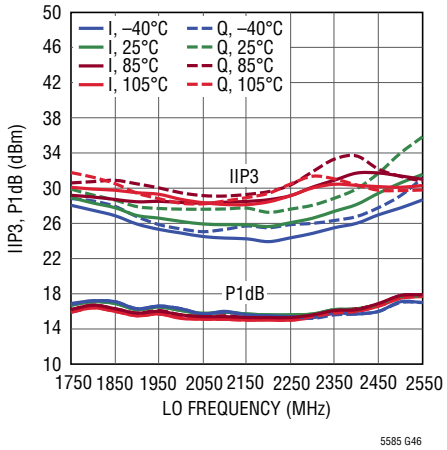
Image Rejection Distribution (Note 10)



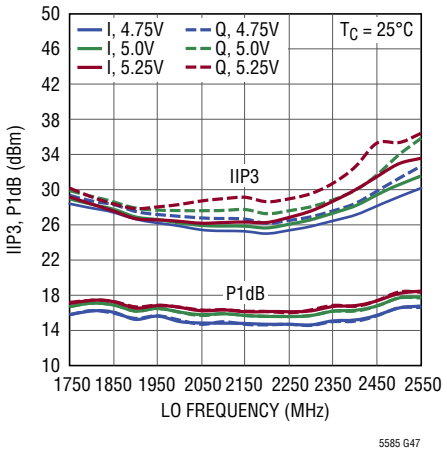
TYPICAL PERFORMANCE CHARACTERISTICS

2150MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, EIP2 = 0V, REF = 0.5V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 2140MHz, f_{RF1} = 2150MHz, f_{RF2} = 2151MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

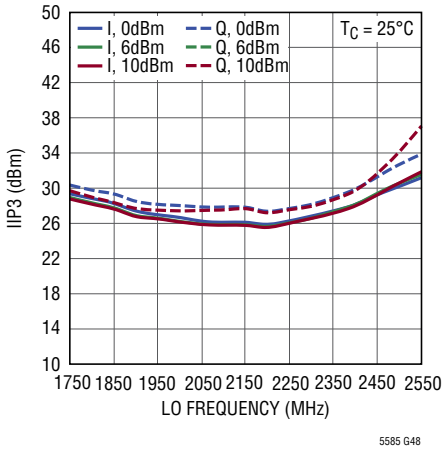
IIP3, P1dB vs Temperature (T_C)



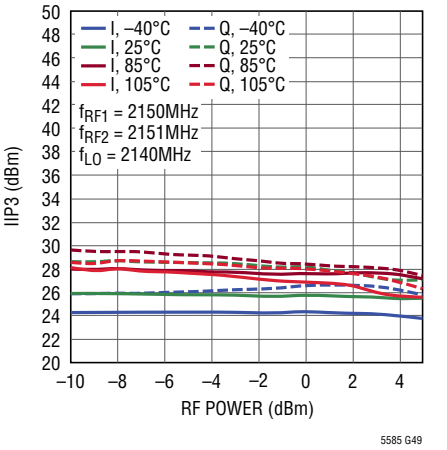
IIP3, P1dB vs Supply Voltage (V_{CC})



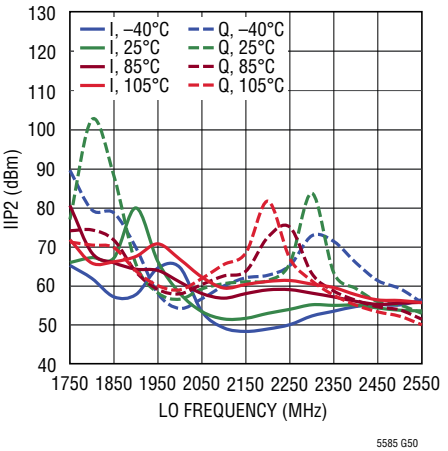
IIP3 vs LO Power



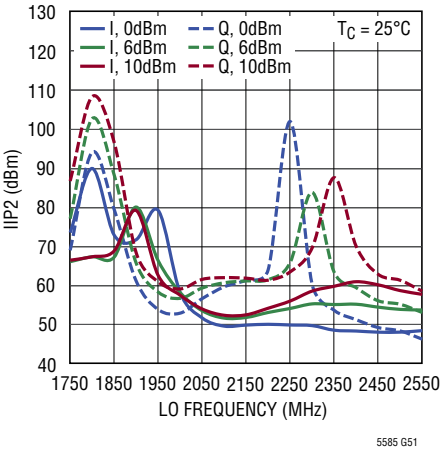
2-Tone IIP3 vs RF Power



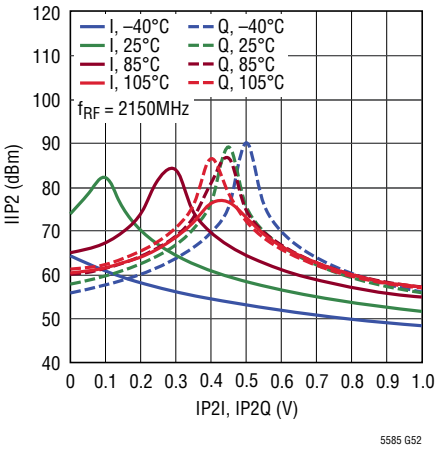
Uncalibrated IIP2 vs Temperature (T_C)



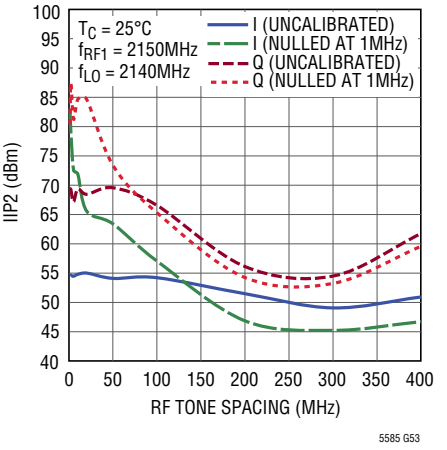
Uncalibrated IIP2 vs LO Power



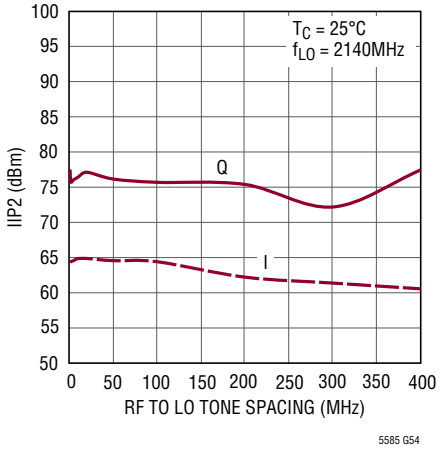
IIP2 vs IP2I, IP2Q Trim Voltage



IIP2 vs RF Tone Spacing



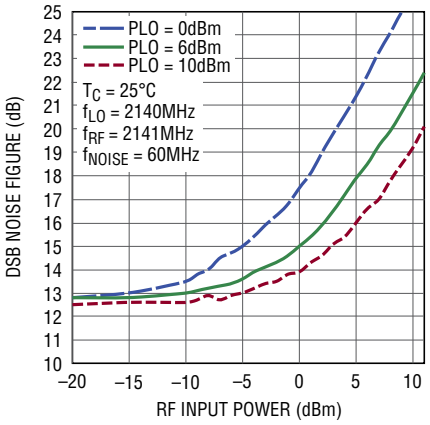
2x2 Half-IF IIP2 vs RF to LO Tone Spacing



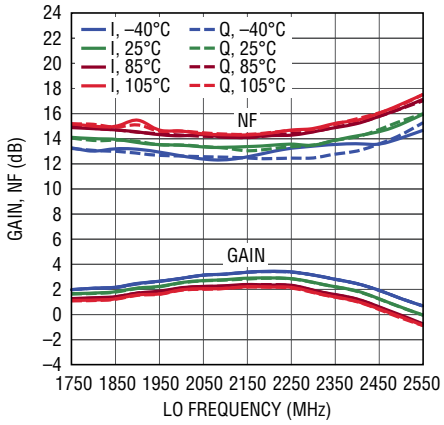
TYPICAL PERFORMANCE CHARACTERISTICS

2150MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, EIP2 = 0V, REF = 0.5V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 2140MHz, f_{RF1} = 2150MHz, f_{RF2} = 2151MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

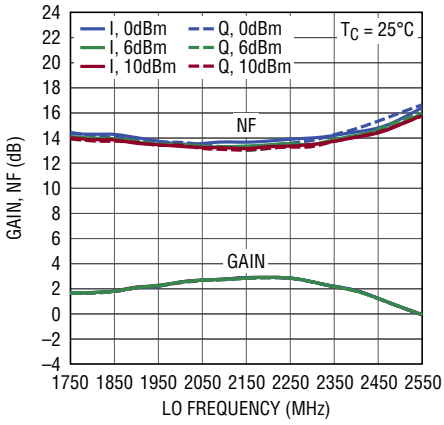
Noise Figure vs RF Input Power



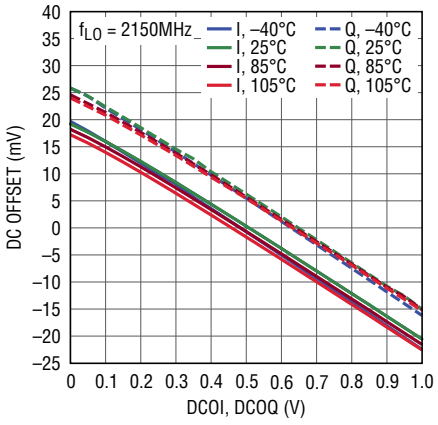
Noise Figure and Conversion Gain vs Temperature (T_C)



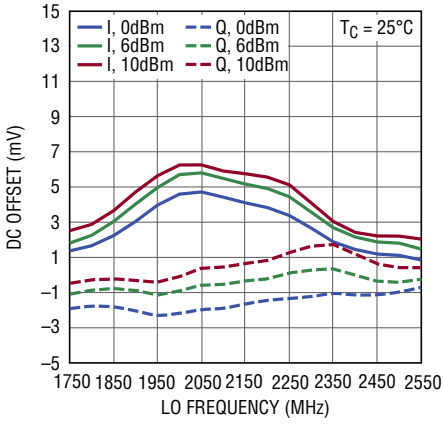
Noise Figure and Conversion Gain vs LO Power



DC Offset vs DCOI, DCOQ Control Voltage



DC Offset vs LO Power



LO to RF Leakage and RF to LO Isolation

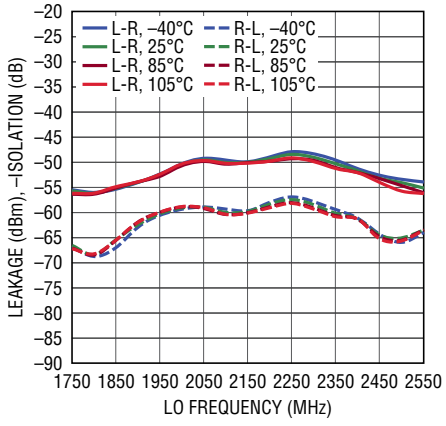
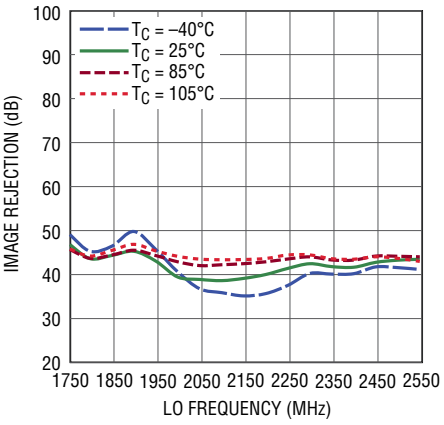


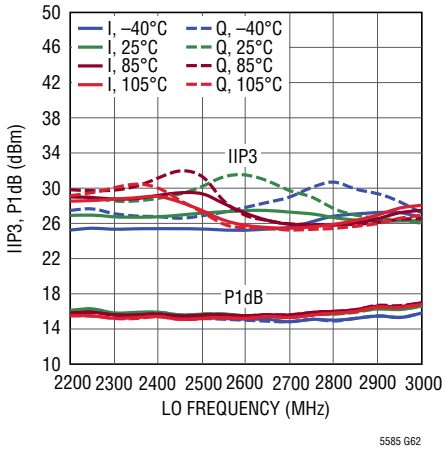
Image Rejection vs Temperature (Note 10)



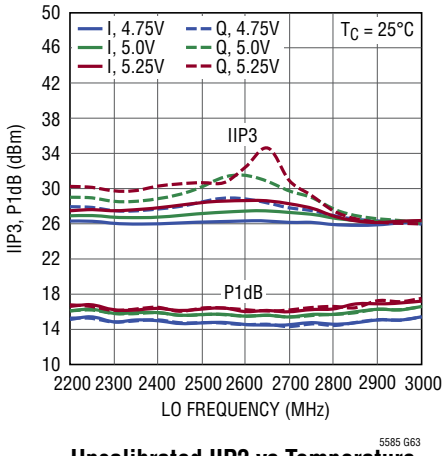
TYPICAL PERFORMANCE CHARACTERISTICS

2600MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, EIP2 = 0V, REF = 0.5V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 2590MHz, f_{RF1} = 2600MHz, f_{RF2} = 2601MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

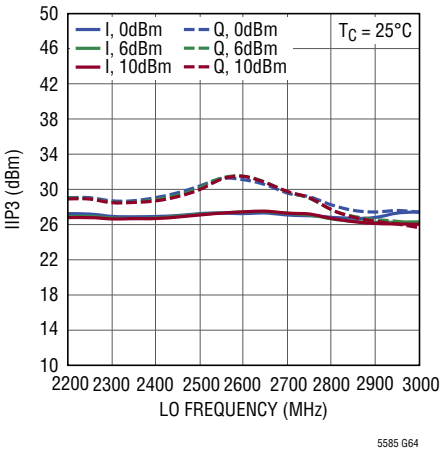
IIP3, P1dB vs Temperature (T_C)



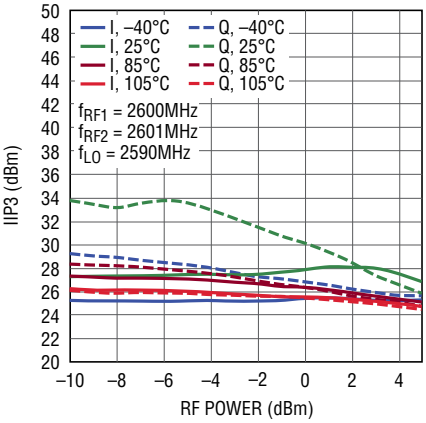
IIP3, P1dB vs Supply Voltage (V_{CC})



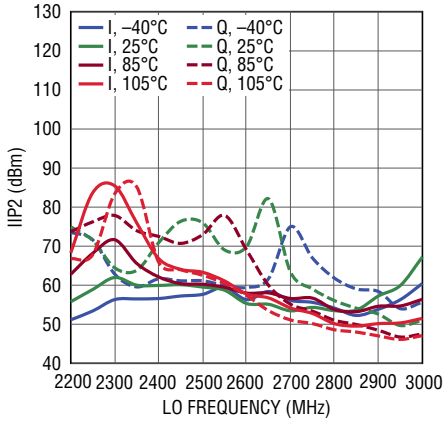
IIP3 vs LO Power



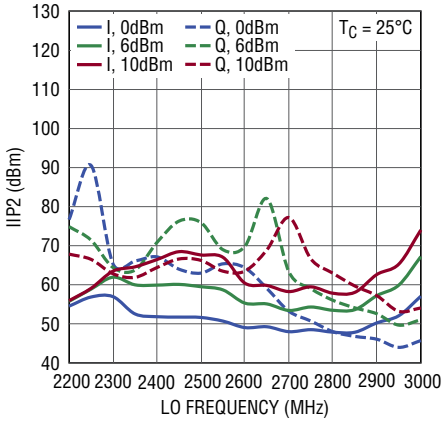
2-Tone IIP3 vs RF Power



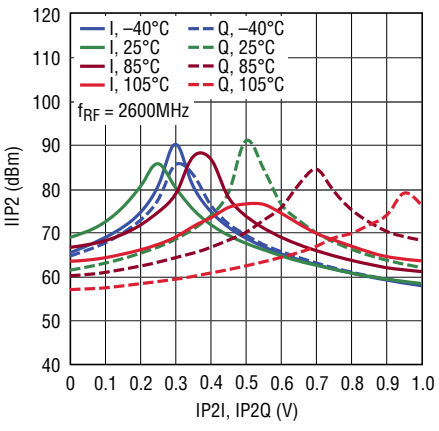
Uncalibrated IIP2 vs Temperature (T_C)



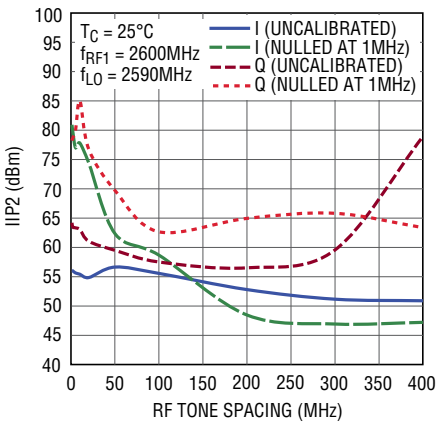
Uncalibrated IIP2 vs LO Power



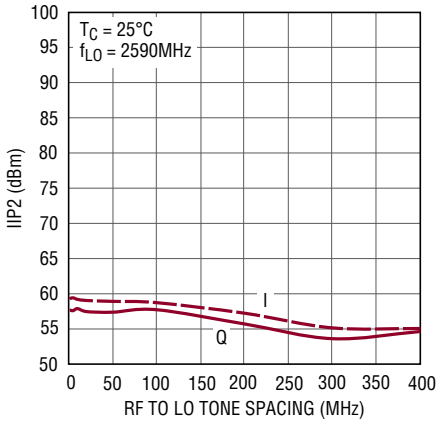
IIP2 vs IP2I, IP2Q Trim Voltage



IIP2 vs RF Tone Spacing



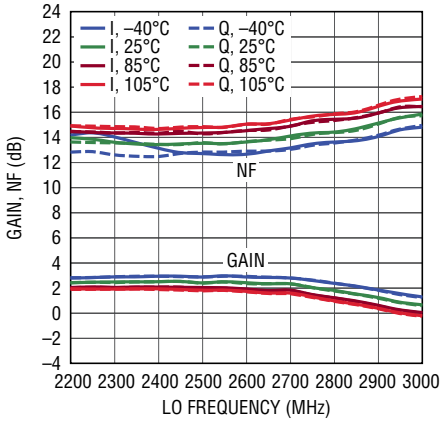
2x2 Half-IF IIP2 vs RF to LO Tone Spacing



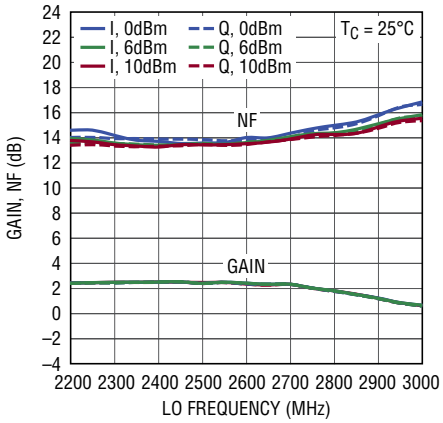
TYPICAL PERFORMANCE CHARACTERISTICS

2600MHz application. V_{CC} = 5V, EN = 5V, EDC = 0V, EIP2 = 0V, REF = 0.5V, T_C = 25°C, P_{LO} = 6dBm, f_{LO} = 2590MHz, f_{RF1} = 2600MHz, f_{RF2} = 2601MHz, f_{BB} = 10MHz, P_{RF1} = P_{RF2} = –5dBm, DC Blocks and Mini-Circuits PSCJ-2-1 180° combiner at baseband outputs de-embedded from measurement unless otherwise noted. Test circuit with RF and LO ports impedance matched as in Figure 1.

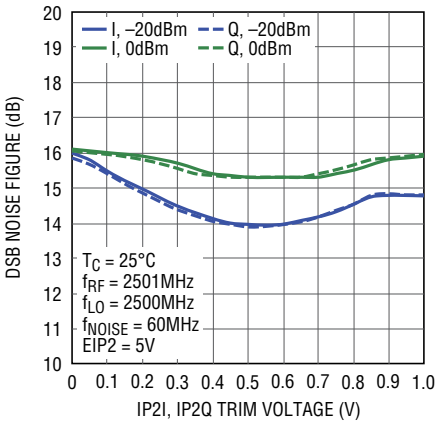
Noise Figure and Conversion Gain vs Temperature (T_C)



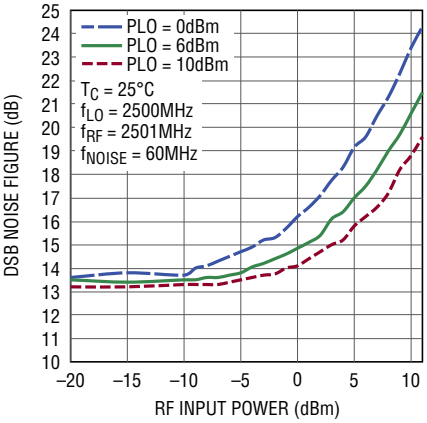
Noise Figure and Conversion Gain vs LO Power



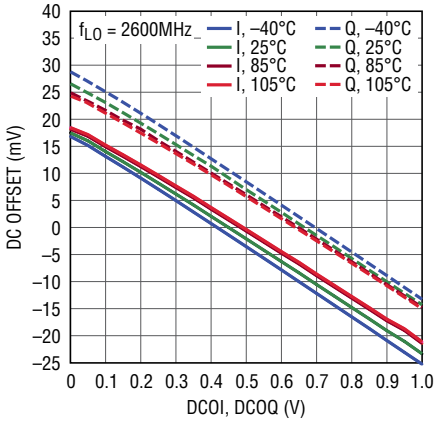
Noise Figure vs RF Power and IP2I, IP2Q Trim Voltage



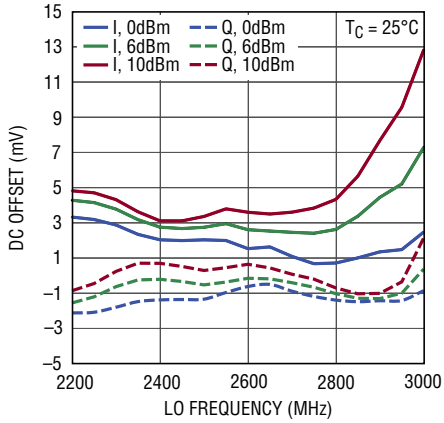
Noise Figure vs RF Input Power



DC Offset vs DCOI, DCOQ Control Voltage



DC Offset vs LO Power



LO to RF Leakage and RF to LO Isolation

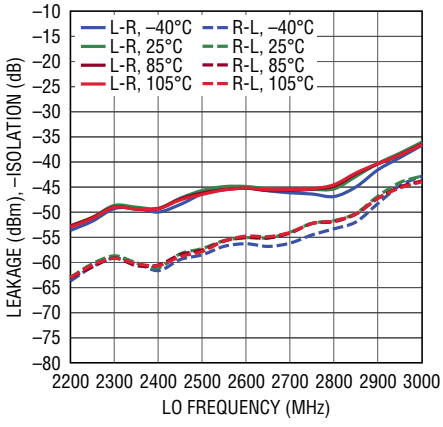
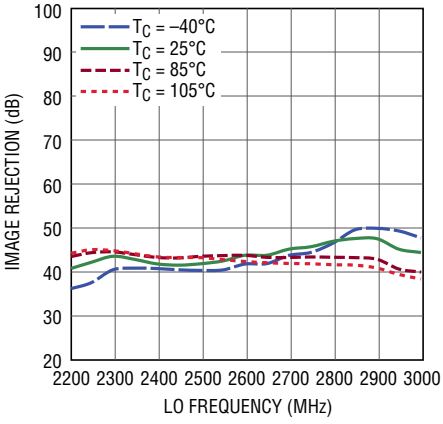


Image Rejection vs Temperature (Note 10)



PIN FUNCTIONS

IP2Q, IP2I (Pin 1, Pin 4): IIP2 Adjustment Analog Control Voltage Input for Q and I Channel. A decoupling capacitor is recommended on this pin. A low output resistance voltage source is recommended for driving these pins. These pins should be left floating if unused.

DCOQ, DCOI (Pin 2, Pin 3): DC Offset Analog Control Voltage Input for Q and I Channel. A decoupling capacitor is recommended on this pin. A low output resistance voltage source is recommended for driving these pins. These pins should be left floating if unused.

RF (Pin 5): RF Input. External matching is used to obtain good return loss across the RF input frequency range. The RF pin is internally shorted to ground through internal transformer windings. The RF pin should be DC-blocked with a 1000pF coupling capacitor.

GND (Pins 6, 8, 13, 14, Exposed Pad Pin 25): Ground. These pins must be soldered to the RF ground plane on the circuit board. The backside exposed pad ground connection should have a low inductance connection and good thermal contact to the printed circuit board ground plane using many through-hole vias. See Figures 2 and 3.

EN (Pin 7): Enable Pin. When the voltage on the EN pin is a logic high, the chip is completely turned on; the chip is completely turned off for a logic low. An internal 200k pull-down resistor ensures the chip remains disabled if there is no connection to the pin (open-circuit condition).

V_{BIAS} (Pin 9): This pin can be pulled to ground through a resistor to lower the current consumption of the chip. See Applications Information.

V_{CC} (Pin 10): Positive Supply Pin. This pin should be bypassed with shunt 1000pF and 1µF capacitors.

EDC (Pin 11): DC Offset Adjustment Mode Enable Pin. When the voltage on the EDC pin is a logic high, the DC offset control circuitry is enabled. The circuitry is disabled for a logic low. An internal 200k pull-down resistor ensures the circuitry remains disabled if there is no connection to the pin (open-circuit condition).

EIP2 (Pin 12): IP2 Offset Adjustment Mode Enable Pin. When the voltage on the EIP2 pin is a logic high, the IP2 adjustment circuitry is enabled. The circuitry is disabled for a logic low. An internal 200k pull-down resistor ensures the circuitry remains disabled if there is no connection to the pin (open-circuit condition).

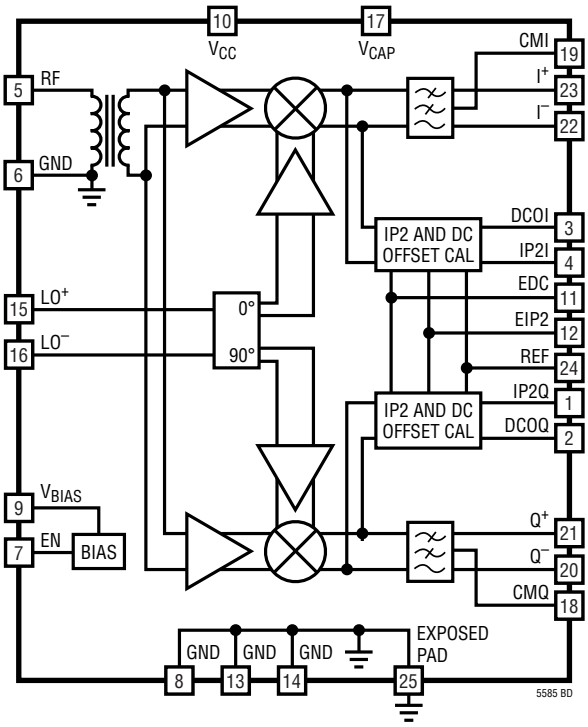
LO^+,LO^- (Pin 15, Pin 16): LO Inputs. External matching is required to obtain good return loss across the LO input frequency range. Can be driven single ended or differentially with an external transformer. The LO pins should be DC-blocked with a 1000pF coupling capacitor.

V_{CAP}, CMQ, CMI (Pin 17, Pin 18, Pin 19): Common Mode Bypass Capacitor Pins. It is recommended that CMI and CMQ be connected to V_{CAP} through 0.1µF capacitors. Nothing else should be connected to V_{CAP} since it is connected to V_{CC} inside the chip.

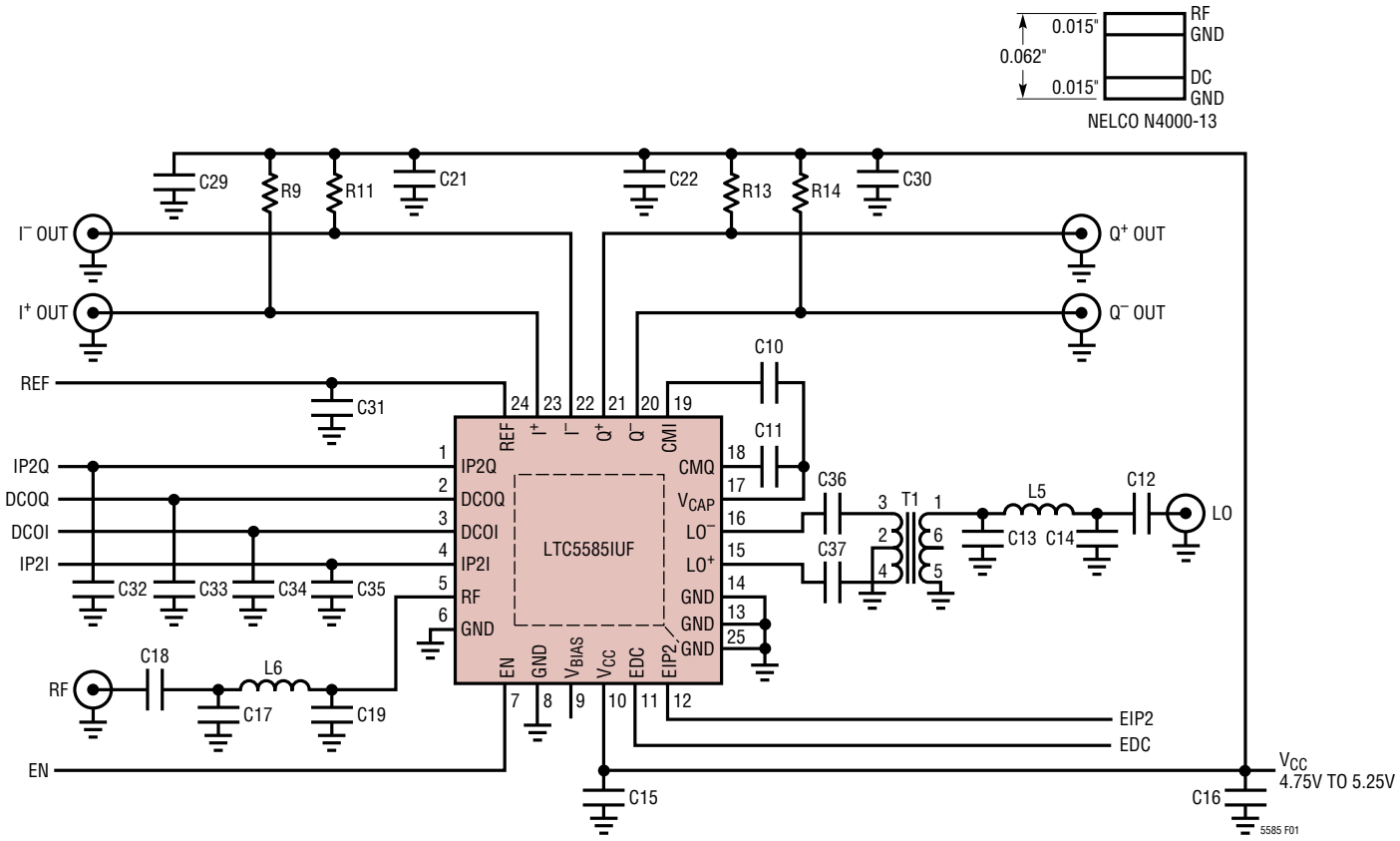
I^+, I^-, Q^+, Q^- (Pin 23, Pin 22, Pin 21, Pin 20): Differential Baseband Output Pins for the I Channel and Q Channel. The DC bias point is V_{CC} – 1.5V for each pin. These pins must have an external 100Ω or an inductor pull-up to V_{CC}.

REF (Pin 24): Voltage Reference Input for Analog Control Voltage Pins. A decoupling capacitor is recommended on this pin. A low output resistance voltage source is recommended for driving this pin. This pin should be left floating if unused.

BLOCK DIAGRAM



TEST CIRCUIT



	RF MATCH			LO MATCH		
FREQUENCY RANGE	C17	L6	C19	C13	L5	C14
700MHz		2.7pF	1.0pF		12nH	5.6pF
1950MHz		1.2pF	5.1nH	5.1nH	1.0pF	
2150MHz	1.5pF	4.7nH	0.5pF		5.1nH	0.7pF
2600MHz	0.5pF	2.7nH			1.2nH	1pF

REF DES	VALUE	SIZE	VENDOR	REF DES	VALUE	SIZE	VENDOR
C10, C11, C31-C35	0.1µF	0402	Murata	L5, L6	See Table	0402	Murata
C12, C15, C18, C36, C37	1000pF	0402	Murata	R9, R11, R13, R14	100Ω	0402	Vishay
C13, C14, C17, C19	See Table	0402	Murata	T1	4:1	0805	Anaren BD0826J50200A00
C16, C21, C22, C29, C30	1µF	0402	Murata				

Figure 1. Test Circuit Schematic

TEST CIRCUIT

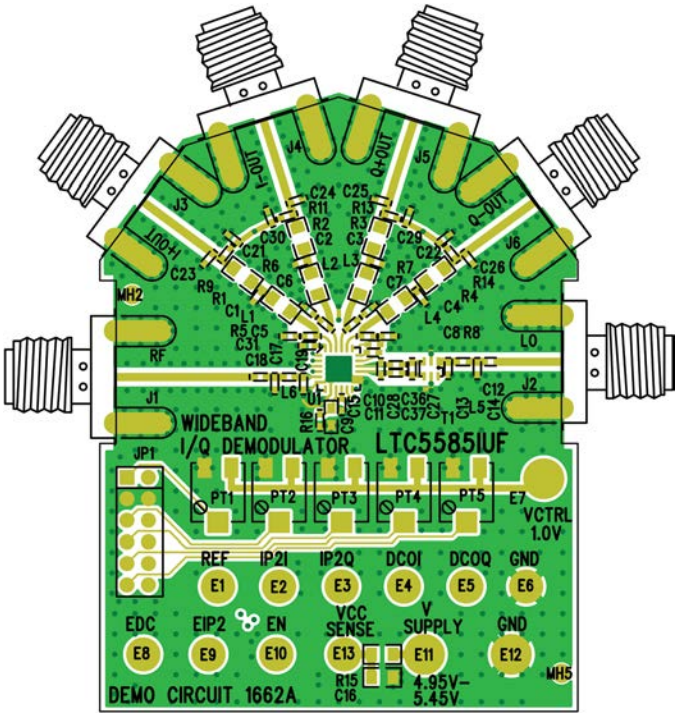


Figure 2. Component Side of Evaluation Board

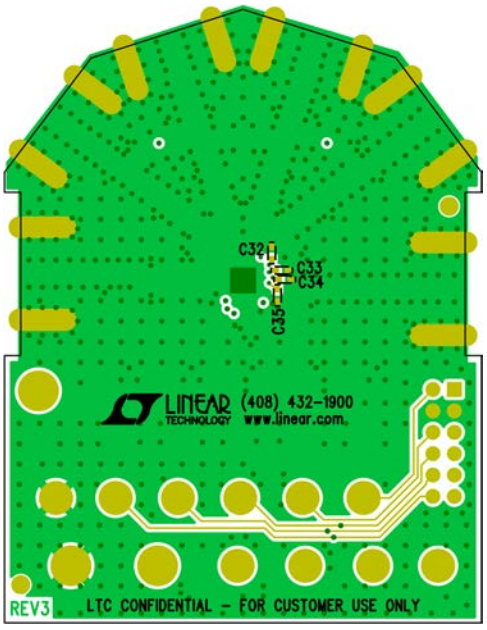


Figure 3. Bottom Side of Evaluation Board

APPLICATIONS INFORMATION

The LTC5585 is an IQ demodulator designed for high dynamic range receiver applications. It consists of RF transconductance amplifiers, I/Q mixers, quadrature LO amplifiers, IIP2 and DC offset correction circuitry, and bias circuitry.

Operation

As shown in the Block Diagram for the LTC5585, the RF signal is applied to the inputs of the RF transconductor V-to-I converters and is then demodulated into I/Q baseband signals using quadrature LO signals which are internally generated by a precision 90° phase shifter. The demodulated I/Q signals are lowpass filtered on-chip with a –3dB bandwidth of 530MHz. The differential outputs of the I-channel and Q-channel are well matched in amplitude and their phases are 90° apart.

RF Input Port

Figure 4 shows the demodulator's RF input which consists of an integrated transformer and high linearity transconductance amplifiers (V-I converters). The primary side of the transformer is connected to the RF input pin. The secondary side of the transformer is connected to the

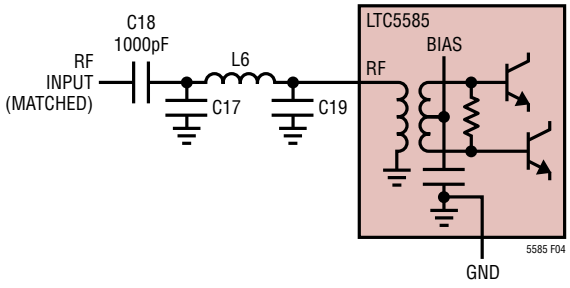


Figure 4: Simplified Schematic of the RF Pin Interface

APPLICATIONS INFORMATION

differential inputs of the transconductance amplifiers. External DC voltage should not be applied to the RF input pin. DC current flowing into the primary side of the transformer may cause damage to the integrated transformer. A series DC blocking capacitor should be used to couple the RF input pin to the RF signal source.

The RF input port can be externally matched over the operating frequency range with simple L-C matching. An input return loss better than 10dB can be obtained over a bandwidth of better than 16% with this method. Figure 5 shows the RF input return loss for various matching component values. Table 1 shows the impedance and input reflection coefficient for the RF input without using any external matching components. The input transmission line length is de-embedded from the measurement.

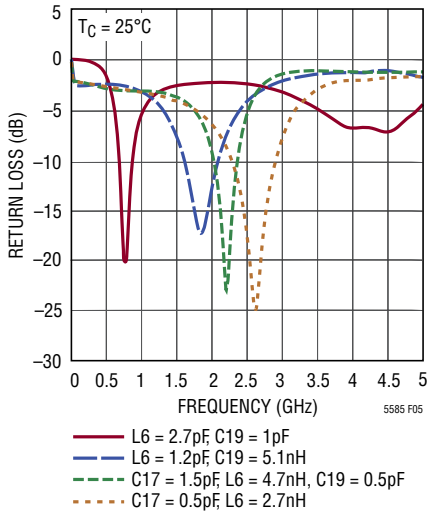


Figure 5. RF Input Return Loss

Larger bandwidths can be obtained by using multiple L-C sections. For example Figure 6 shows a 2-section L-C match having a bandwidth of about 38% where return loss is >10dB. Figure 7 shows the RF input return loss for the wide bandwidth match.

Broadband Performance

To get an idea of the broadband performance of the LTC5585, a 6dB pad can be put on the RF and LO ports, and the ports can be left unmatched. The measured RF performance for this configuration is shown in Figures 8, 9, 10 and 11 with the 6dB pad de-embedded. The RF

Table 1. RF Input Impedance

FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)	S11	
		MAG	ANGLE (°)
400	6.98 + j25.09	0.800	125.98
600	10.43 + j39.74	0.775	101.55
800	16.76 + j56.73	0.751	80.01
1000	28.55 + j77.15	0.727	61.05
1200	51.47 + j101.03	0.706	44.29
1400	96.49 + j122.28	0.686	29.33
1600	171.91 + j112.37	0.667	15.81
1800	229.92 + j30.89	0.648	3.45
2000	202.21 – j58.84	0.630	–8.00
2200	145.32 – j91.23	0.612	–18.71
2400	104.82 – j91.69	0.594	–28.49
2600	78.33 – j83.38	0.575	–38.22
2800	61.86 – j73.64	0.557	–47.49
3000	51.27 – j64.65	0.538	–56.32
3200	43.83 – j56.56	0.519	–65.15
3400	38.86 – j49.72	0.500	–73.40
3600	35.17 – j43.6	0.481	–81.68
3800	32.46 – j38.21	0.463	–89.79
4000	30.48 – j33.41	0.444	–97.76

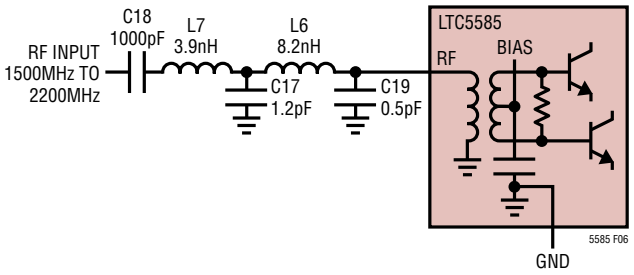


Figure 6. Wide Bandwidth RF Input Match

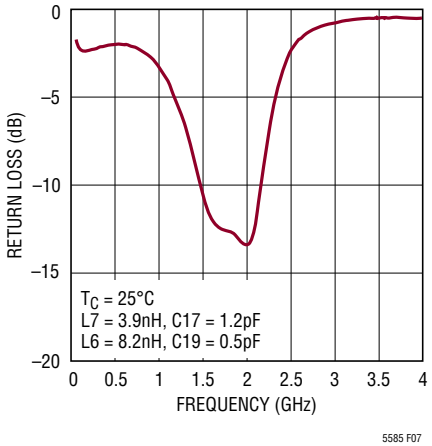


Figure 7. RF Input Return Loss for Wideband Match

APPLICATIONS INFORMATION

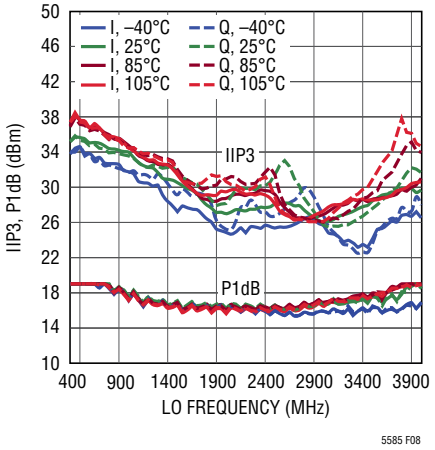


Figure 8. Broadband IIP3 and IP1dB

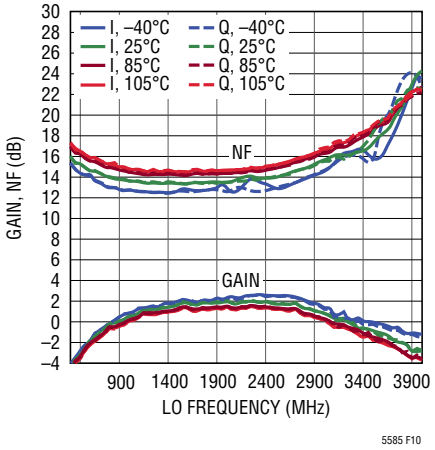


Figure 10. Broadband NF and Gain

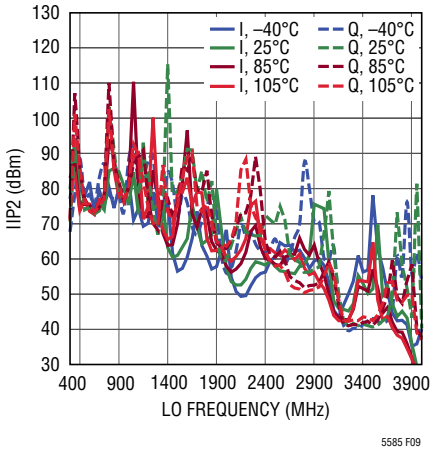


Figure 9. Broadband IIP2

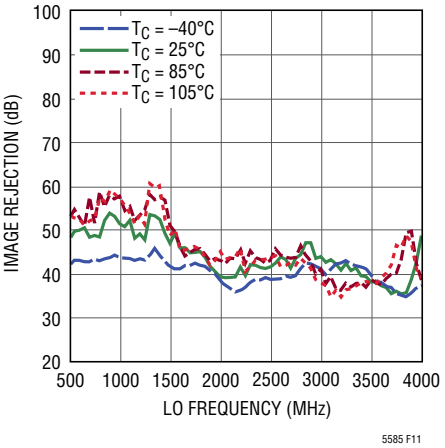


Figure 11. Broadband Image Rejection

tone spacing is 1MHz, and f_{LO} is 10MHz lower than f_{RF}. The conversion gain is lower than under the impedance matched condition, and correspondingly the P1dB, IIP3, and NF are higher. As shown, the part can be used at frequencies outside its specified operating range with reduced conversion gain and higher NF.

LO Input Port

The demodulator's LO input interface is shown in Figure 12. The input consists of a high precision quadrature phase shifter which generates 0° and 90° phase shifted LO signals for the LO buffer amplifiers to drive the I/Q mixers. DC blocking capacitors are required on the LO^+ and LO^- inputs.

The differential LO input impedance and S parameters with the input transmission lines and balun de-embedded are listed in Table 2.

Figure 13 shows LO input return loss using the ANAREN BD0826J50200A00 4:1 balun with various matching component values.

For optimum IIP2 and large-signal NF performance the LO inputs should be driven differentially with a 4:1 balun such as the ANAREN BD0826J50200A00 or BD2425J50200AHF. As shown in Figure 14, the LO input can also be driven single-ended from either the LO^+ or LO^- input. The unused port should be DC-blocked and terminated with a 50Ω load. Figure 15 compares the uncalibrated IIP2 performance of single ended versus differential LO drive.

APPLICATIONS INFORMATION

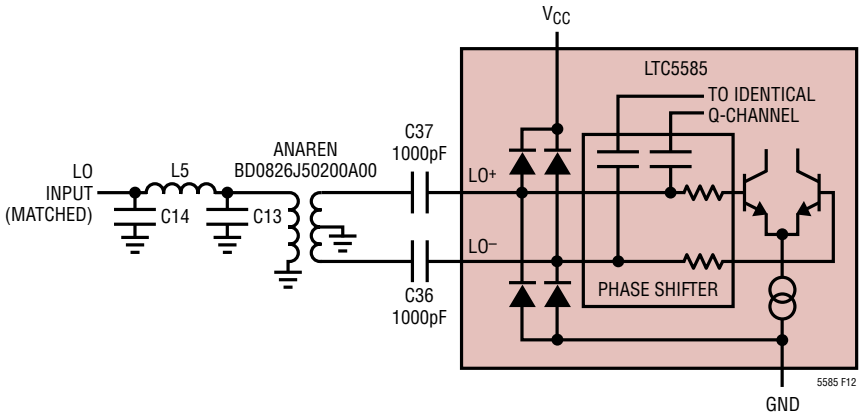


Figure 12. Simplified Schematic of LO Input Interface with External Matching Components

Table 2. LO Input Impedance (Differential)

FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)	S11	
		MAG	ANGLE (°)
400	118.18 – j120.02	0.668	–24.89
600	94.18 – j99.93	0.623	–31.42
800	78.00 – j85.06	0.583	–38.17
1000	67.21 – j73.16	0.544	–44.79
1200	59.71 – j63.49	0.507	–51.25
1400	54.22 – j55.46	0.471	–57.63
1600	50.06 – j48.59	0.437	–64.02
1800	46.80 – j42.69	0.405	–70.49
2000	44.10 – j37.42	0.374	–77.28
2200	41.86 – j32.61	0.345	–84.47
2400	39.98 – j28.16	0.317	–92.21
2600	38.39 – j23.98	0.291	–100.65
2800	37.05 – j20.01	0.267	–109.95
3000	35.92 – j16.21	0.246	–120.29
3200	34.99 – j12.53	0.228	–131.76
3400	34.22 – j8.95	0.214	–144.37
3600	33.61 – j5.45	0.206	–157.88
3800	33.15 – j2.0	0.204	–171.85
4000	32.82 + j1.4	0.208	174.35

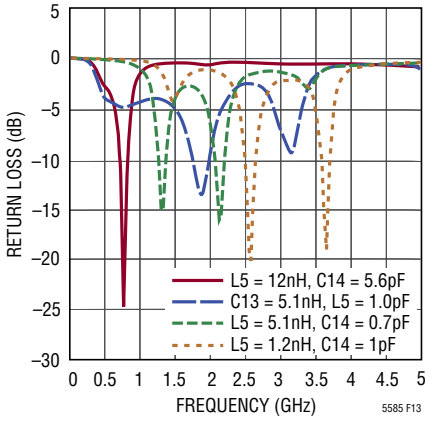


Figure 13. LO Input Return Loss

APPLICATIONS INFORMATION

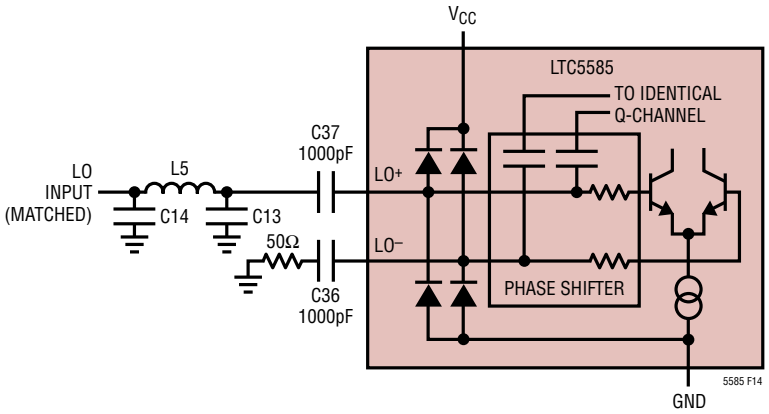


Figure 14. Recommended Single-Ended LO Input Configuration

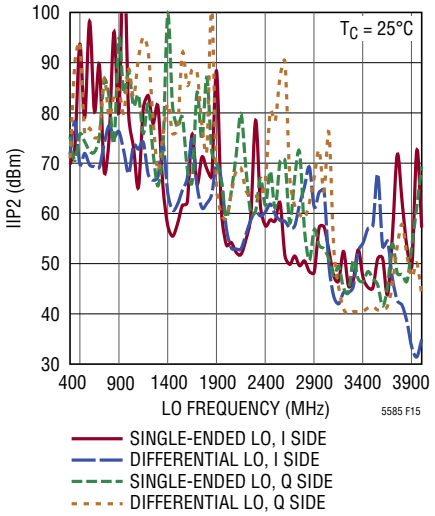


Figure 15. Broadband IIP2 with Differential and Single-Ended LO Drive

I-Channel and Q-Channel Outputs

The phase relationship between the I-channel output signal and the Q-channel output signal is fixed. When the LO input frequency is higher (or lower) than the RF input frequency, the Q-channel outputs (Q^+, Q^-) lag (or lead) the I-channel outputs (I^+, I^-) by 90°.

Each of the I-channel and Q-channel outputs is internally connected to V_{CC} through a 100Ω resistor. In order to maintain an output DC bias voltage of V_{CC} – 1.5V, external 100Ω pull-up resistors or equivalent 15mA DC current sources are required. Each single-ended output has an impedance of 100Ω in parallel with a 6pF internal capacitor. With an external 100Ω pull-up resistor this forms a lowpass filter with a –3dB corner frequency at 530MHz. The outputs can be DC coupled or AC coupled to external loads. The voltage conversion gain is reduced by the external load by:

$$20\text{Log}_{10}\left(\frac{1}{2}+\frac{50\Omega}{R_{PULL\text{-}UP}\,||\,R_{LOAD(SE)}}\right)\text{dB}$$

when the output port is terminated by $R_{LOAD(SE)}$. For instance, the gain is reduced by 6dB when each output pin is connected to a 50Ω load (or 100Ω differentially). The output should be taken differentially (or by using differential-to-single-ended conversion) for best RF performance, including NF and IIP2. When no external filtering or matching components are used, the output response is determined by the loading capacitance and the total resistance loading the outputs. The –3dB corner frequency, f_C, is given by the following equation:

$$f_C = [2\pi(R_{LOAD(SE)}||100\Omega||R_{PULL\text{-}UP})\ (6\text{pF})]^{-1}$$

Figure 16 shows the actual measured output response with various load resistances.

Figure 17 shows a simplified model of the I, Q outputs with a 100Ω differential load and 100Ω pull-ups. The –1dB bandwidth in this configuration is about 520MHz, or about twice the –1dB bandwidth with no load.

APPLICATIONS INFORMATION

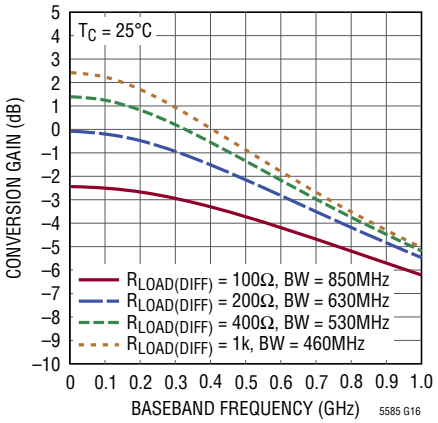


Figure 16. Conversion Gain Baseband Output Response with $R_{LOAD(DIFF)}$ = 100Ω, 200Ω, 400Ω and 1k and $R_{PULL-UP}$ = 100Ω

Figure 18 shows a simplified model of the I, Q outputs with a L-C matching network for bandwidth extension. Capacitor C_S serves to filter common mode LO switching noise immediately at the demodulator outputs. Capacitor C_C in combination with inductor L_S is used to peak the output response to give greater bandwidth of 650MHz. In this case, capacitor C_C was chosen as a common mode capacitor instead of a differential mode capacitor to increase rejection of common mode LO switching noise.

When AC output coupling is used, the resulting highpass filter's –3dB roll-off frequency, f_C, is defined by the R-C constant of the external AC coupling capacitance, C_{AC}, and the differential load resistance, $R_{LOAD(DIFF)}$:

$$f_C = [2\pi \bullet R_{LOAD(DIFF)} \bullet C_{AC}]^{-1}$$

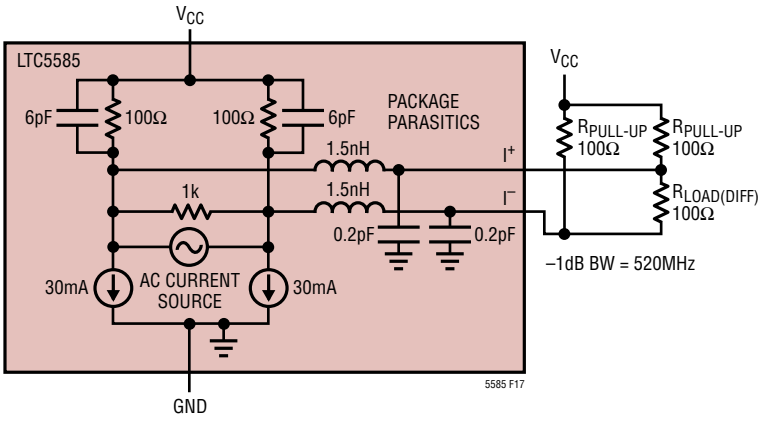


Figure 17. Simplified Model of the Baseband Output

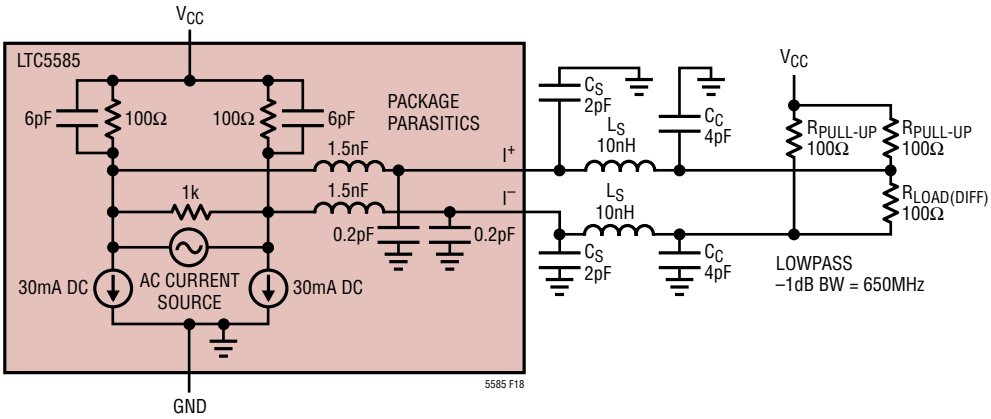


Figure 18. Simplified Model of the Baseband Output Showing Bandwidth Extension with External L, C Matching

APPLICATIONS INFORMATION

Care should be taken when the demodulator's outputs are DC coupled to the external load to make sure that the I/Q mixers are biased properly. If the current drain from the outputs exceeds about 6mA, there can be significant degradation of the linearity performance. Keeping the common mode output voltage of the demodulator above 3.15V, with a 5V supply, will ensure optimum performance. Each output can sink no more than 30mA when the outputs are connected to an external load with a DC voltage higher than V_{CC} – 1.5V.

In order to achieve the best IIP2 performance, it is important to minimize high frequency coupling among the baseband outputs, RF port, and LO port. Although it may increase layout complexity, routing the baseband output traces on the backside of the PCB can improve uncalibrated IIP2 performance. Figure 19 shows the alternate layout having the baseband outputs on the backside of the PCB.

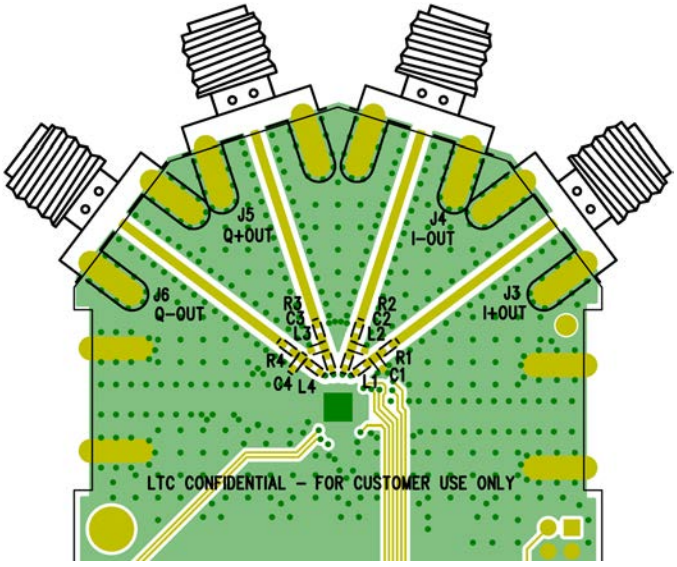


Figure 19. Alternate Layout of PCB with Baseband Outputs on the Backside

Analog Control Voltage Pins

Figure 20 shows the equivalent circuit for the DCOI, DCOQ, IP2I, and IP2Q pins. Internal temperature compensated 62.5µA current sources keep these pins biased at a nominal 500mV through 8k resistors. A low impedance voltage source with a source resistance of less than 200Ω is recommended to drive these pins.

As shown in Figure 21, the REF pin is similar to the DCOI pin, but the bias current source is 250µA, and the internal resistance is 2k. If this pin is left disconnected, it will self-bias to 500mV. A low impedance voltage source with a source resistance of less than 200Ω is recommended to drive this pin. The control voltage range of the DCOI, DCOQ, IP2I and IP2Q pins is set by the REF pin. This range is equal to 0V to twice the voltage on the REF pin, whether internally or externally applied.

It is recommended to decouple any AC noise present on the signal lines that connect to the analog control-voltage inputs. A shunt capacitor to ground placed close to these pins can provide adequate filtering. For instance, a value of 1000pF on the DCOI, DCOQ, IP2I and IP2Q pins will provide a corner frequency of around 6 to 7MHz. A similar corner frequency can be obtained on the REF pin with a value of 3900pF. Using larger capacitance values such as 0.1µF is recommended on these pins unless a faster control

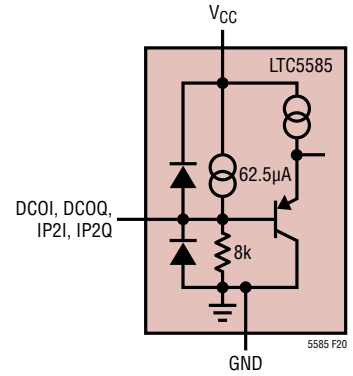


Figure 20. Simplified Schematic of the Interface for the DCOI, DCOQ, IP2I and IP2Q Pins

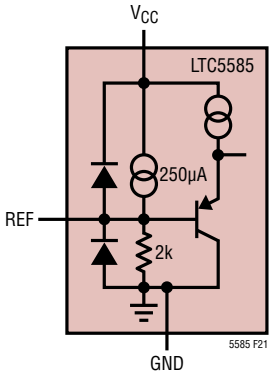


Figure 21. Simplified Schematic of the REF Pin Interface