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700MHz to 6GHz Low Power Direct Quadrature Modulator

FEATURES

- **Frequency Range: 700MHz to 6GHz**
- **Low Power: 2.7V to 3.6V Supply; 29.5mA**
- **Low LO Carrier Leakage: –43dBm at 1.8GHz**
- **Side-Band Suppression: –50dBc at 1.8GHz**
- **Output IP3: 19dBm at 1.8GHz**
- **Low RF Output Noise Floor: –157dBm/Hz at 30MHz Offset, P_{RF} = 1.8dBm, f_{RF} = 2.17GHz**
- **Sine Wave or Square Wave LO Drive**
- **SPI Control:**
  Adjustable Gain: 19dB in 1dB Steps
  Effecting Supply Current from 9mA to 39mA
  I/Q Offset Adjust: –64dBm LO Carrier Leakage
  I/Q Gain/Phase Adjust: –61dBc Side-Band Suppressed
- **24-Lead 4mm × 4mm Plastic QFN Package**

APPLICATIONS

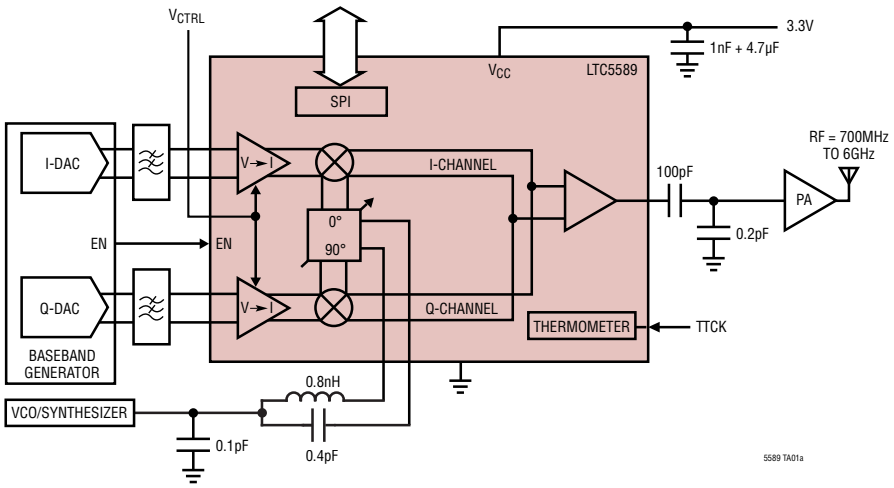
- Wireless Microphones
- Battery Powered Radios
- Vector Modulator
- 2.45GHz and 5.8GHz Transmitters
- Software Defined Radios (SDR)
- Military Radios

DESCRIPTION

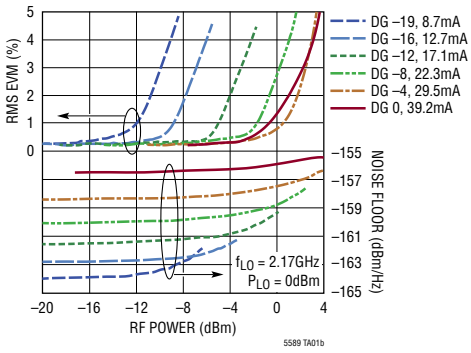
The LTC®5589 is a direct conversion I/Q modulator designed for low power wireless applications that enables direct modulation of differential baseband I and Q signals on an RF carrier. Single side-band modulation or side-band suppressed upconversion can be achieved by applying 90° phase-shifted signals to the I and Q inputs. The I/Q baseband input ports can be either AC or DC coupled to a source with a common mode voltage level of about 1.4V. The SPI interface controls the supply current, modulator gain, and allows adjustments of I and Q gain and phase imbalance to optimize the LO carrier feedthrough and side-band suppression. The LO port can be driven with sine wave or square wave LO drive. A fixed LC network on the LO and RF ports covers 700MHz to 6GHz operating range. An on-chip thermometer can be activated to compensate for gain-temperature variations. More accurate temperature measurements can be made using an on-chip diode. In addition, a continuous analog gain control (V_{CTRL}) pin can be used for fast power control.

TYPICAL APPLICATION

700MHz to 6GHz Direct Conversion Transmitter Application



EVM and Noise Floor vs RF Output Power and Digital Gain Setting with 1Ms/s 16-QAM Signal

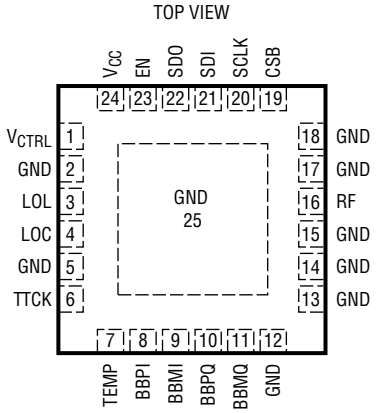


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 3.8V
Common Mode Voltage of BBPI, BBMI, and BBPQ, BBMQ 2V
LOL, LOC DC Voltage ..... ±50mV
LOL, LOC Input Power (Note 15) 20dBm
Output Current TEMP, SDO 10mA
Voltage on Any Pin (Note 16) ..... –0.3V to V_{CC} + 0.3V
T_{JMAX} ..... 150°C
Case Operating Temperature Range ..... –40°C to 105°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 7°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC5589#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5589IUF#PBF	LTC5589IUF#TRPBF	5589	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges..

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

Please refer to: http://www.linear.com/designtools/packaging/ for the most recent package drawings.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{LO} = 800MHz, f_{RF1} = 797.9MHz, f_{RF2} = 798MHz, Register 0x00 = 0x70 (Decimal 112), L1 = 4.7nH, C5 = 2pF, C18 = 0.2pF							
$S_{22(ON)}$	RF Port Return Loss				–24		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			0.74 to 1.97		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}/V_{IN(DIFF)(I or Q)}$)			–10.5		dB
P_{OUT}	Absolute Output Power	1$V_{P-P(DIFF)}$ CW Signal, I and Q			–6.5		dBm
OP1dB	Output 1dB Compression				4.1		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			70.6		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			19.9		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–159.6		dBm/Hz
SB	Side-Band Suppression	(Note 7)			–48		dBc

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–46 –71		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–62.5		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–49.1		dBc
3LOFT	LO Feedthrough at 3xLO				–57.9		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–10.6		dBc
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			43		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			91		MHz
f_{LO} = 1800MHz, f_{RF1} = 1797.9MHz, f_{RF2} = 1798MHz, Register 0x00 = 0x4B (Decimal 75), L1 = 4.7nH, C5 = 2pF, C18 = 0.2pF							
$S_{22(ON)}$	RF Port Return Loss				–21		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			0.84 to 5.8		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}/V_{IN(DIFF)(I or Q)}$)			–9.7		dB
P_{OUT}	Absolute Output Power	1$V_{P-P(DIFF)}$ CW Signal, I and Q			–5.7		dBm
OP1dB	Output 1dB Compression				4.6		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			60.4		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			19		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–158.8		dBm/Hz
SB	Side-Band Suppression	(Note 7)			–50		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–43 –52		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–61.3		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–47		dBc
3LOFT	LO Feedthrough at 3xLO				–73.8		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–18.6		dBc
	Gain from LO to RF	BBPI = BBPQ = 1.9V			10		dB
	LO Input Noise Figure	BBMI = BBMQ = 0.9V			12.5		dB
	LO Input 3rd Order Intercept	(Vector Modulator)			–2		dBm
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			92		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			168		MHz
f_{LO} = 2500MHz, f_{RF1} = 2497.9MHz, f_{RF2} = 2498MHz, Register 0x00 = 0x3F (Decimal 63), L1 = 4.7nH, C5 = 2pF, C18 = 0.2pF							
$S_{22(ON)}$	RF Port Return Loss				–21		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			0.86 to 6		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}/V_{IN(DIFF)(I or Q)}$)			–10.2		dB
P_{OUT}	Absolute Output Power	1$V_{P-P(DIFF)}$ CW Signal, I and Q			–6.2		dBm
OP1dB	Output 1dB Compression				3.9		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			62		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			17.5		dBm

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3) P_{OUT} = 1.8dBm (Note 17)			–158.1 –157		dBm/Hz dBm/Hz
SB	Side-Band Suppression	(Note 7)			–41.5		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–40.2 –50		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–65.4		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–48.8		dBc
3LOFT	LO Feedthrough at 3xLO				–77.2		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–25.9		dBc
BW1dB$_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			65		MHz
BW3dB$_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			167		MHz
f_{LO} = 3500MHz, f_{RF1} = 3497.9MHz, f_{RF2} = 3498MHz, Register 0x00 = 0x2F (Decimal 47), L1 = 0.8nH, C5 = 0.4pF, C18 = 0.1pF (5.8GHz LO Match)							
$S_{22(ON)}$	RF Port Return Loss				–25		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			1.2 to 6		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}/V_{IN(DIFF)(I or Q)}$)			–12.7		dB
P_{OUT}	Absolute Output Power	1$V_{P-P(DIFF)}$ CW Signal, I and Q			–8.7		dBm
OP1dB	Output 1dB Compression	(Note 18)			1.1		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			41.8		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			14.6		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–159.6		dBm/Hz
SB	Side-Band Suppression	(Note 7)			–43		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–34.5 –39.8		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–66.5		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–46.3		dBc
3LOFT	LO Feedthrough at 3xLO				–71.4		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–31.7		dBc
BW1dB$_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			76		MHz
BW3dB$_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			173		MHz
f_{LO} = 4500MHz, f_{RF1} = 4497.9MHz, f_{RF2} = 4498MHz, Register 0x00 = 0x24 (Decimal 36), L1 = 0.8nH, C5 = 0.4pF, C18 = 0.1pF (5.8GHz LO Match)							
$S_{22(ON)}$	RF Port Return Loss				–20		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			1.3 to 6		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}/V_{IN(DIFF)(I or Q)}$)			–16.3		dB
P_{OUT}	Absolute Output Power	1$V_{P-P(DIFF)}$ CW Signal, I and Q			–12.3		dBm
OP1dB	Output 1dB Compression	(Note 18)			–2.2		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			35.2		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			11.2		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–161.3		dBm/Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SB	Side-Band Suppression	(Note 7)			–44		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–33 –34		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–67		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–45		dBc
3LOFT	LO Feedthrough at 3xLO				–73		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–42		dBc
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			98		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			176		MHz
f_{LO} = 5800MHz, f_{RF1} = 5797.9MHz, f_{RF2} = 5798MHz, Register 0x00 = 0x1A (Decimal 26), L1 = 0.8nH, C5 = 0.4pF, C18 = 0.1pF (5.8GHz LO Match)							
$S_{22(ON)}$	RF Port Return Loss				–14.8		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			1.3 to 6		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}/V_{IN(DIFF)(I or Q)}$)			–21		dB
P_{OUT}	Absolute Output Power	$1V_{P-P(DIFF)}$ CW Signal, I and Q			–17		dBm
OP1dB	Output 1dB Compression	(Note 18)			–7.1		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			28.3		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			7		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–162.7		dBm/Hz
SB	Side-Band Suppression	(Note 7)			–31		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–37.6 –29.9		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–72.5		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–46.9		dBc
3LOFT	LO Feedthrough at 3xLO				–78.6		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–53.3		dBc
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			100		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			181		MHz
Analog Variable Gain Control (V_{CTRL})							
$V_{CTRL}R$	Gain Control Voltage Range	Set Bit 6 in Register 0x01			0.9 to 3.3		V
G_{CTRL}	Gain Control Gain Range	Set Bit 6 in Register 0x01			–73 to –10		dB
τ_{CTRL}	Gain Control Response Time	Set Bit 6 in Register 0x01 (Note 8)			20		ns
Z_{CTRL}	Gain Control Input Impedance	Set Bit 6 in Register 0x01			10		pF
I_{CTRL}	DC Input Current	Set Bit 6 in Register 0x01 Clear Bit 6 in Register 0x01			2.55 0		mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Baseband Inputs (BBPI, BBMI, BBPQ, BBMQ)							
V_{CMBB}	DC Common Mode Voltage	Internally Generated			1.41		V
$R_{IN(DIFF)}$	Input Resistance	Differential			1.8		kΩ
$R_{IN(CM)}$	Common Mode Input Resistance	Four Baseband Pins Shorted			350		Ω
$I_{BB(OFF)}$	Baseband Leakage Current	Four Baseband Pins Shorted, EN = Low			1.3		nA
V_{SWING}	Amplitude Swing	No Hard Clipping, Single-Ended, Digital Gain (DG) = –10			1.2		V_{P-P}
Power Supply (V_{CC})							
V_{CC}	Supply Voltage Range		●	2.7		3.6	V
$V_{RET(MIN)}$	Minimum Data Retention Voltage	(Note 14)	●	1.8	1.5		V
$I_{CC(ON)}$	Supply Current	EN = High		20	29.5	37	mA
$I_{CC(RANGE)}$	Supply Current Range	EN = High, Register 0x01 = 0x00			39		mA
		EN = High, Register 0x01 = 0x13			9		mA
$I_{CC(OFF)}$	Supply Current, Sleep Mode	EN = 0V			0.6	9	µA
t_{ON}	Turn-On Time	EN = Low to High (Notes 8, 12)			30		ns
t_{OFF}	Turn-Off Time	EN = High to Low (Notes 9, 12)			33		ns
t_{SB}	Side-Band Suppression Settling	Register 0x00 Change, <–50dBc (Notes 12, 18)			350		ns
t_{LO}	LO Suppression Settling	Register 0x02 Change, <–60dBm (Note 12)			125		ns
Serial Port (CSB, SCLK, SDI, SDO), Enable (EN) and TTCK, SCLK = 20MHz							
V_{IH}	Input High Voltage		●	1.1			V
V_{IL}	Input Low Voltage		●			0.2	V
I_{IH}	Input High Current				0.02		nA
I_{IL}	Input Low Current				–0.4		nA
V_{OH}	Output High Voltage	(Note 13)	●	V_{CC_L} – 0.2			V
V_{OL}	Output Low Voltage	I_{SINK} = 8mA (Note 10)	●			0.7	V
I_{OH}	SDO Leakage Current	for SDO = High			0.5		nA
V_{HYS}	Input Trip Point Hysteresis				110		mV
t_{CKH}	SCLK High Time		●	22.5			ns
t_{CSS}	CSB Setup Time		●	20			ns
t_{CSH}	CSB High Time		●	30			ns
t_{CS}	SDI to SCLK Setup Time		●	20			ns
t_{CH}	SDI to SCLK Hold Time		●	10			ns
t_{DO}	SCLK to SDO Time		●	45			ns
$t_{C\%}$	SCLK Duty Cycle		●	45	50	55	%
f_{CLK}	Maximum SCLK Frequency		●	20			MHz
V_{TEMP}	Temperature Diode Voltage	I_{TEMP} = 100µA			772		mV
	Temperature Slope	I_{TEMP} = 100µA			–1.5		mV/°C

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5589 is guaranteed functional over the operating case temperature range from –40°C to 105°C.

Note 3: At 6MHz offset from the LO signal frequency. 100nF between BBPI and BBMI, 100nF between BBPQ and BBMQ.

Note 4: The Default Register Settings are listed in Table 1.

Note 5: IM2 is measured at f_{LO} – 4.1MHz.

Note 6: IM3 is measured at f_{LO} – 2.2MHz and f_{LO} – 1.9MHz. OIP3 = lowest of (1.5 • P{f_{LO} – 2.1MHz} – 0.5 • P{f_{LO} – 2.2MHz}) and (1.5 • P{f_{LO} – 2MHz} – 0.5 • P{f_{LO} – 1.9MHz}).

Note 7: Without side-band or LO feedthrough nulling (unadjusted).

Note 8: RF power is within 10% of final value.

Note 9: RF power is at least 30dB down from its ON state.

Note 10: V_{OL} voltage scales linear with current sink. For example for $R_{PULL-UP}$ = 1kΩ, V_{CC_L} = 3.3V the SDO sink current is about (3.3 – 0.2) /1kΩ = 3.1mA. Max V_{OL} = 0.7 • 3.1/8 = 0.271V, with $R_{PULL-UP}$ the SDO pull-up resistor and V_{CC_L} the digital supply voltage to which $R_{PULL-UP}$ is connected to.

Note 11: I and Q baseband Input signal = 2MHz CW, 0.8$V_{P-P,\ DIFF}$ each, I and Q 0° shifted.

Note 12: f_{LO} = 1800MHz, P_{LO} = 0dBm, C4 = 10pF

Note 13: Maximum V_{OH} is derated for capacitive load using the following formula: V_{CC_L} • exp (–0.5 • T_{CLK}/($R_{PULL-UP}$ • C_{LOAD}), with T_{CLK} the time of one SCLK cycle, $R_{PULL-UP}$ the SDO pull-up resistor, V_{CC_L} the digital supply voltage to which $R_{PULL-UP}$ is connected to, and C_{LOAD} the capacitive load at the SDO pin. For example for T_{CLK} = 100ns (10MHz SCLK), $R_{PULL-UP}$ = 1kΩ, C_{LOAD} = 10pF and V_{CC_L} = 3.3V the derating is 3.3 • exp(–5) = 22.2mV, thus maximum V_{OH} = 3.3V – 0.1 – 0.0222 = 3.177V.

Note 14: Minimum V_{CC} in order to retain register data content.

Note 15: Guaranteed by design and characterization. This parameter is not tested.

Note 16: RF pin guaranteed by design while using a 100pF coupling capacitor. The RF pin is not tested.

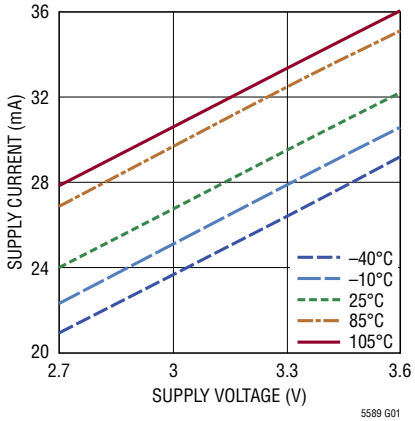
Note 17: f_{LO} = 2.17GHz, f_{NOISE} = 2.14GHz, f_{BB} = 2kHz. 100nF between BBPI and BBMI, 100nF between BBPQ and BBMQ.

Note 18: Using 2.14GHz bandpass filter with BW = 5MHz, f_{BB} = 25MHz, f_{LO} = 2.115GHz, measured from parallel load (see Figure 7).

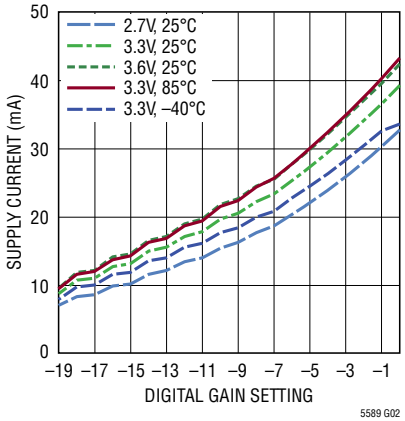
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

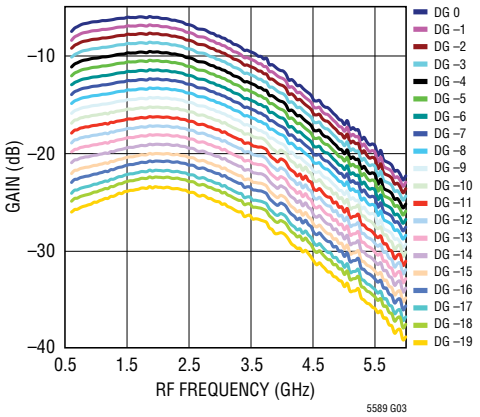
Supply Current vs Supply Voltage



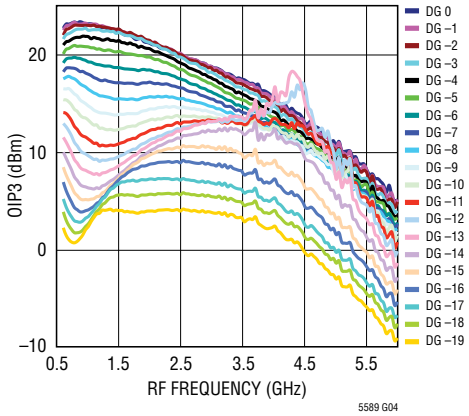
Supply Current vs Digital Gain Setting



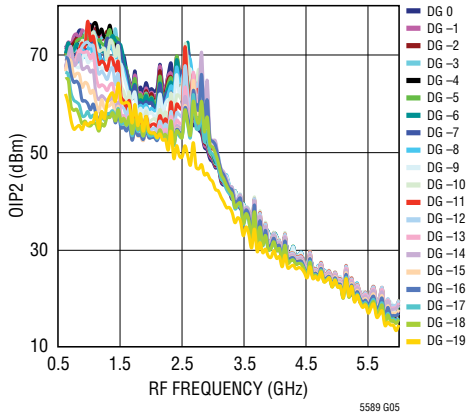
Gain vs RF Frequency and Digital Gain Setting



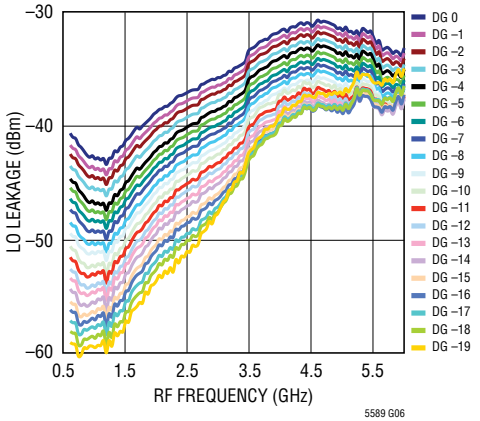
Output IP3 vs RF Frequency and Digital Gain Setting



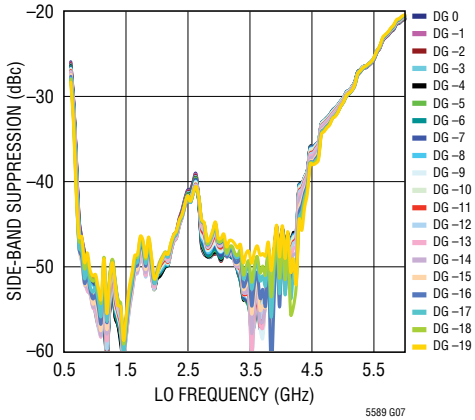
Output IP2 vs RF Frequency and Digital Gain Setting



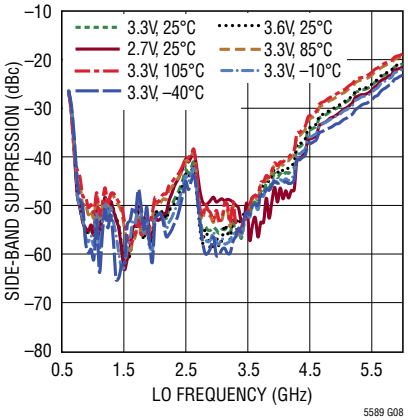
LO Leakage vs RF Frequency and Digital Gain Setting



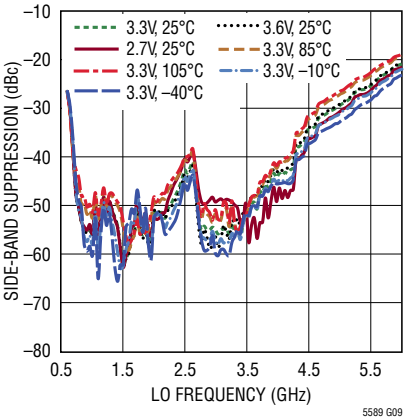
Side-Band Suppression vs LO Frequency and Digital Gain Setting



Side-Band Suppression vs LO Frequency for Gain TempComp Off



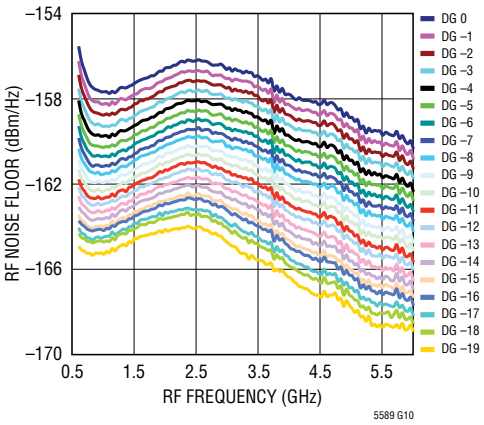
Side-Band Suppression vs LO Frequency for Gain TempComp On



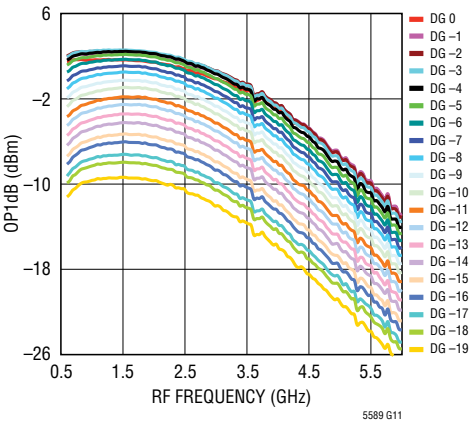
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

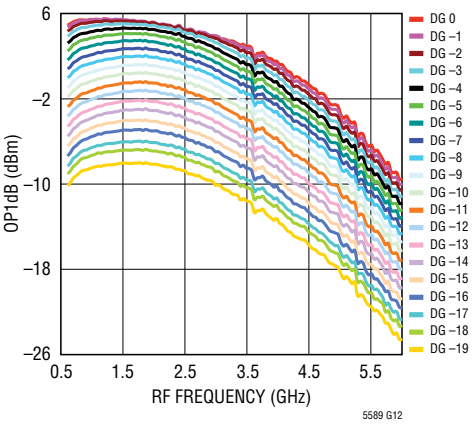
Noise Floor vs RF Frequency and Digital Gain Setting



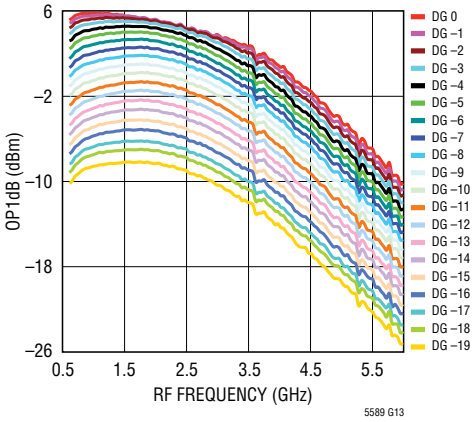
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting and 2.7V Supply



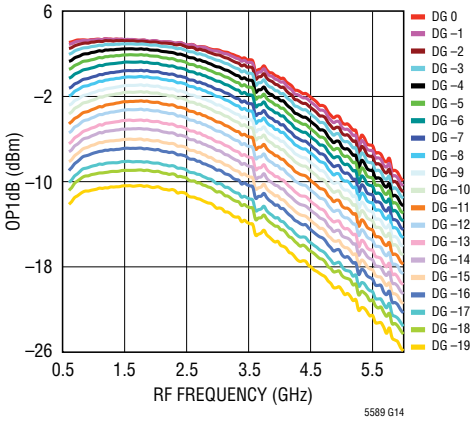
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting and 3.3V Supply



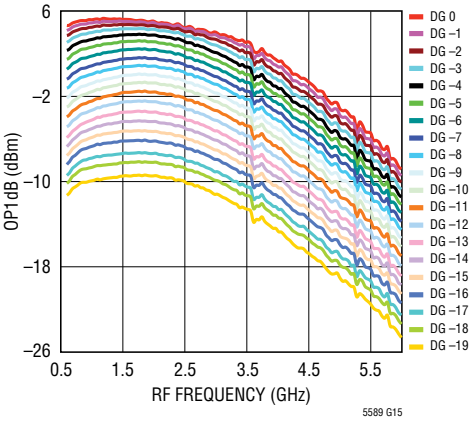
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting and 3.6V Supply



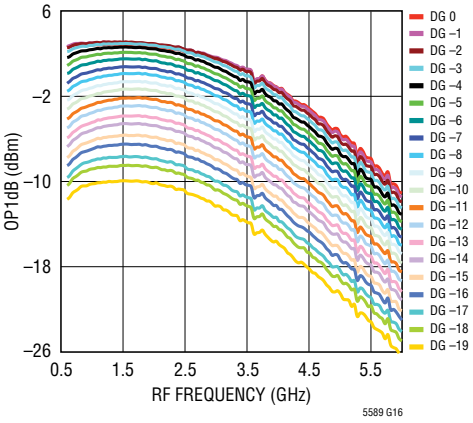
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 2.7V Supply, –40°C



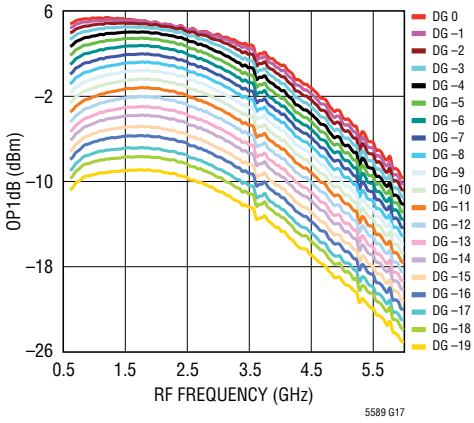
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 3.3V Supply, –40°C



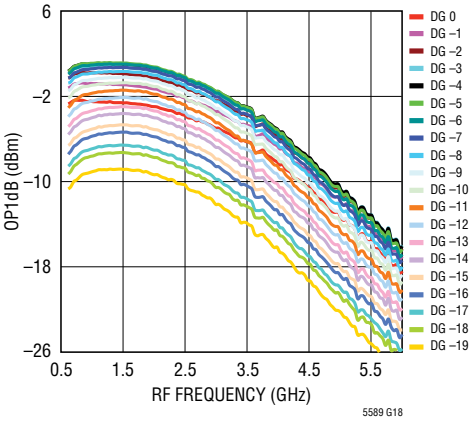
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 2.7V Supply, –10°C



Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 3.3V Supply, –10°C



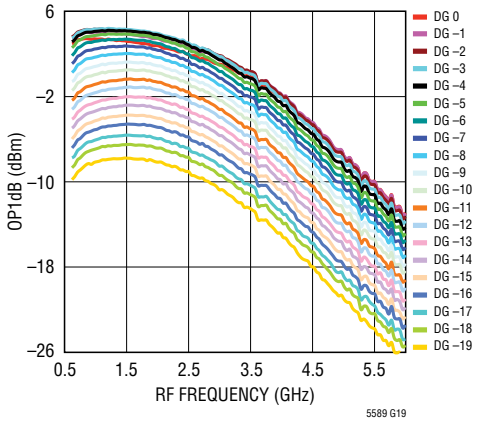
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 2.7V Supply, 85°C



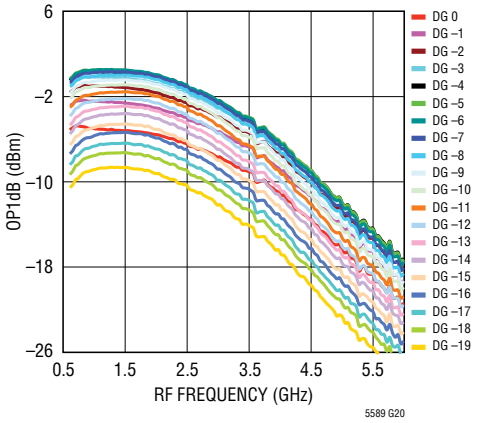
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

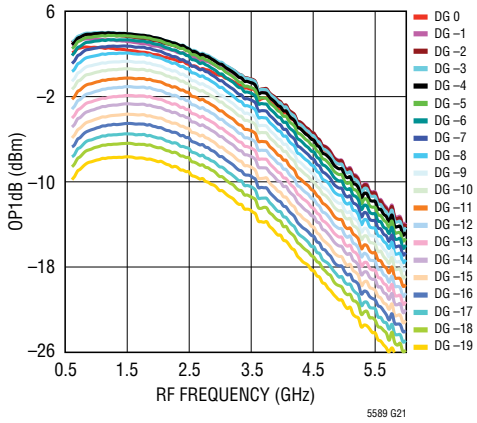
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 3.3V Supply, 85°C



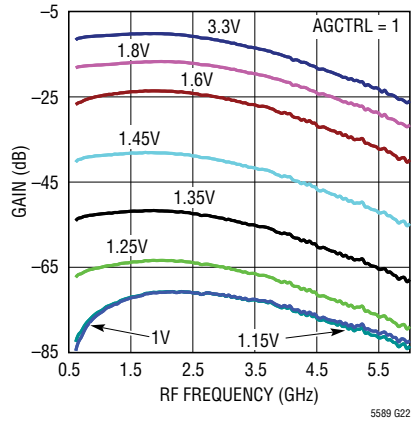
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 2.7V Supply, 105°C



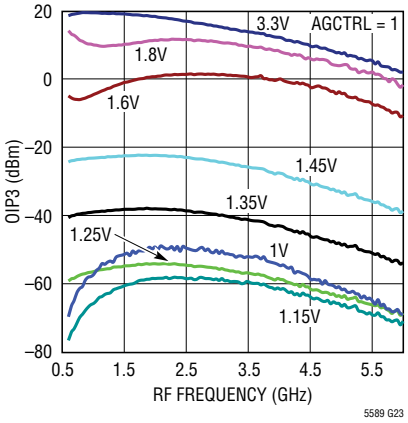
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 3.3V Supply, 105°C



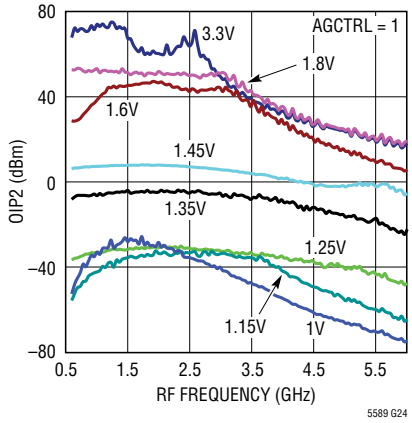
Gain vs RF Frequency and V_{CTRL}



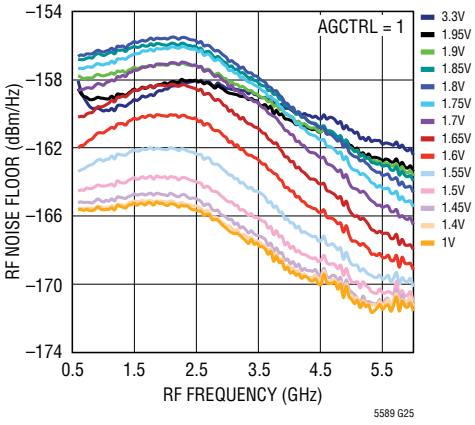
Output IP3 vs RF Frequency and V_{CTRL}



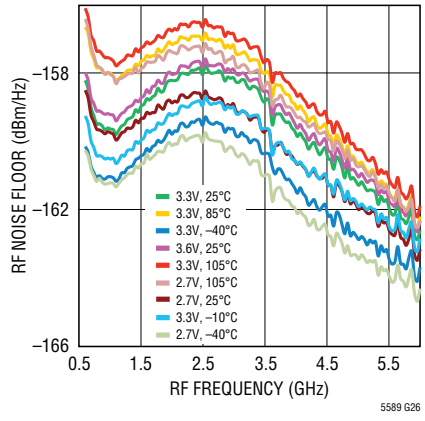
Output IP2 vs RF Frequency and V_{CTRL}



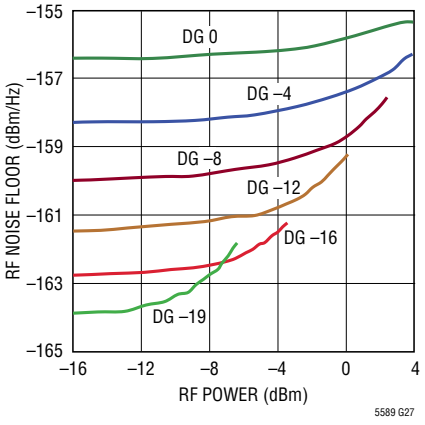
Noise Floor vs RF Frequency and V_{CTRL}



Noise Floor vs RF Frequency



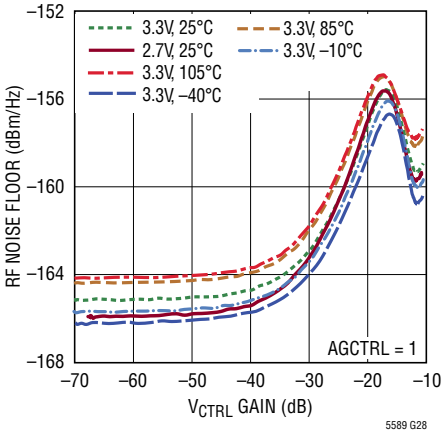
Noise Floor vs RF Power



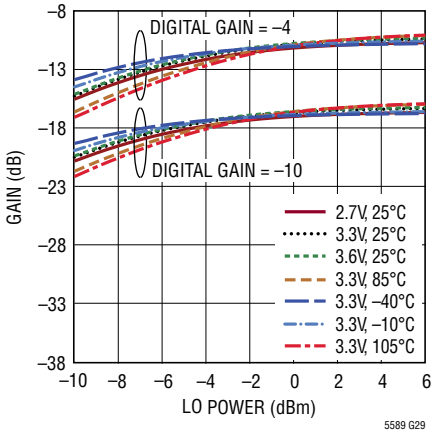
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

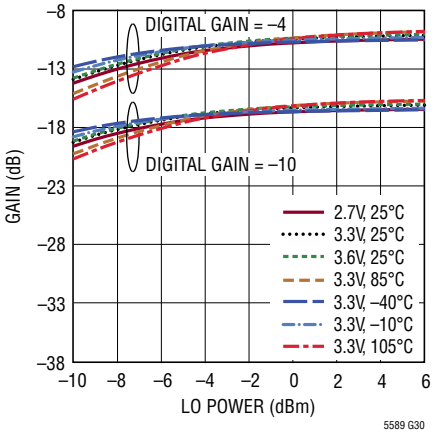
Noise Floor vs V_{CTRL} Gain



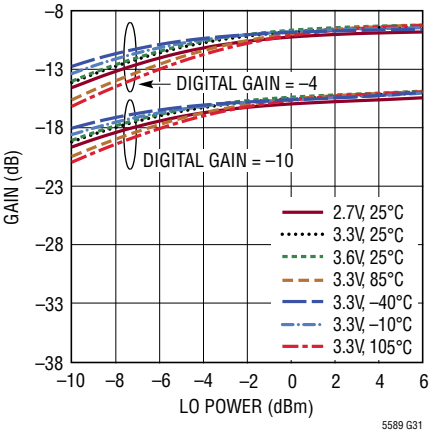
Gain vs LO Power at f_{LO} = 700MHz



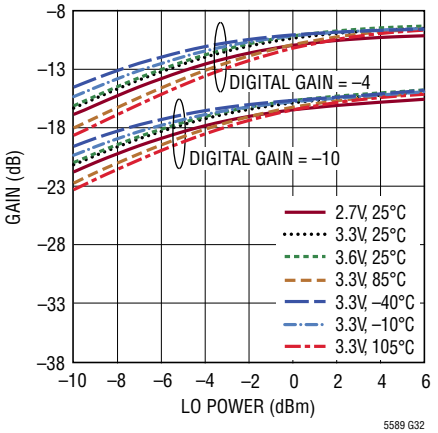
Gain vs LO Power at f_{LO} = 900MHz



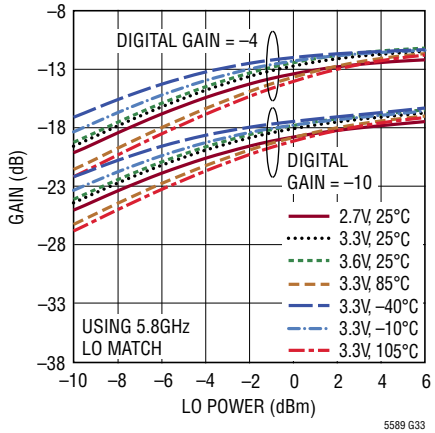
Gain vs LO Power at f_{LO} = 1800MHz



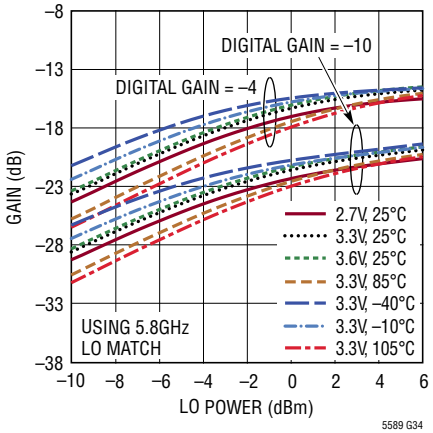
Gain vs LO Power at f_{LO} = 2500MHz



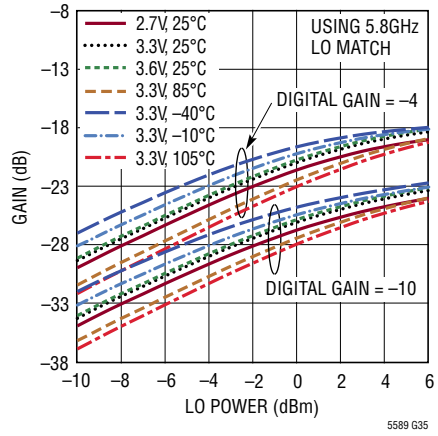
Gain vs LO Power at f_{LO} = 3500MHz



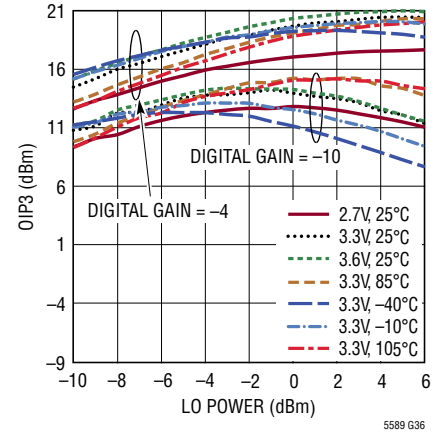
Gain vs LO Power at f_{LO} = 4500MHz



Gain vs LO Power at f_{LO} = 5800MHz



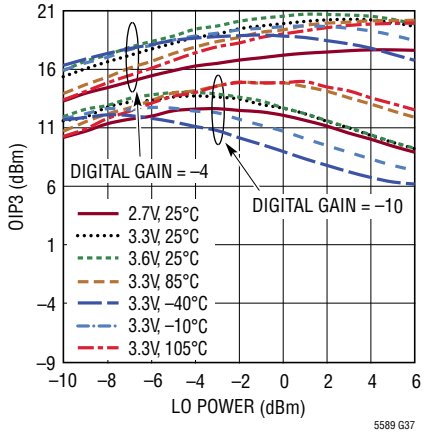
Output IP3 vs LO Power at f_{LO} = 700MHz



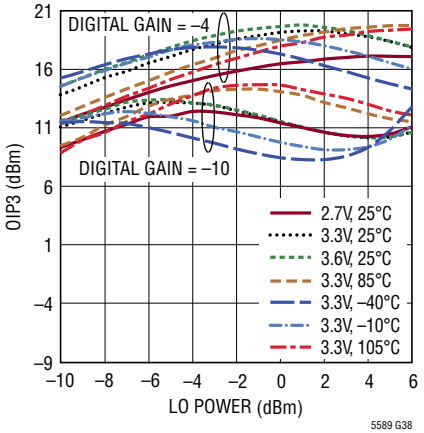
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

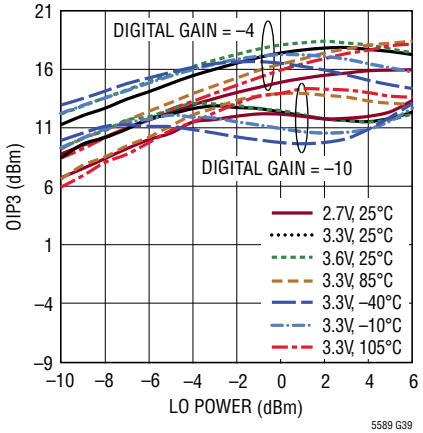
Output IP3 vs LO Power at f_{LO} = 900MHz



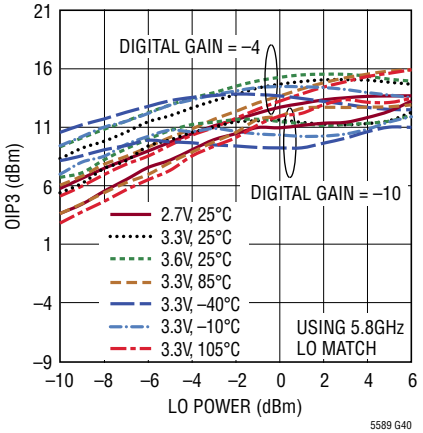
Output IP3 vs LO Power at f_{LO} = 1800MHz



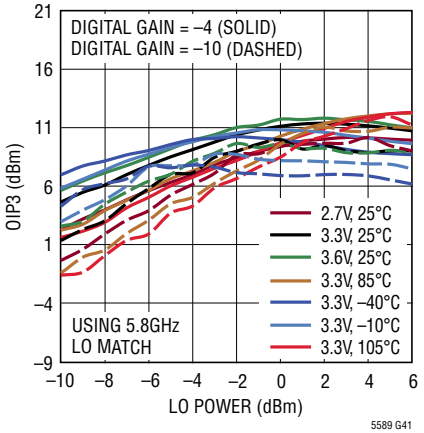
Output IP3 vs LO Power at f_{LO} = 2500MHz



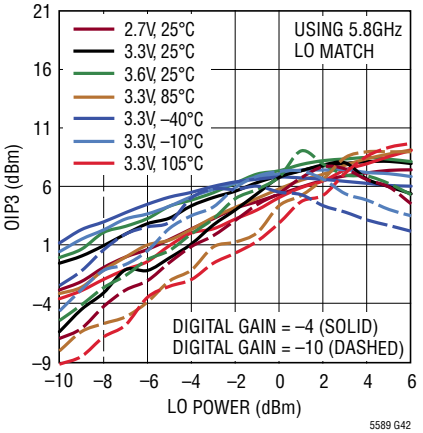
Output IP3 vs LO Power at f_{LO} = 3500MHz



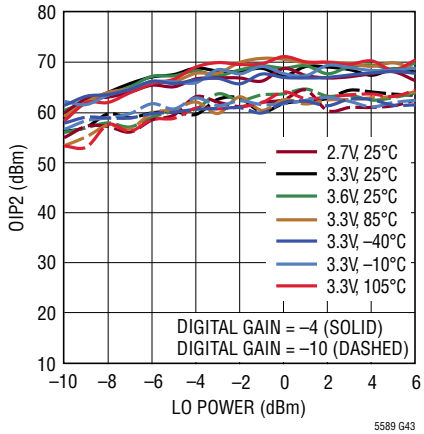
Output IP3 vs LO Power at f_{LO} = 4500MHz



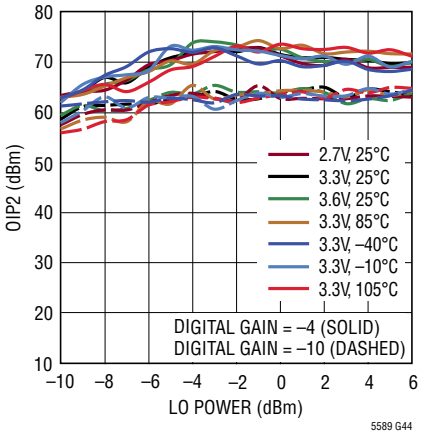
Output IP3 vs LO Power at f_{LO} = 5800MHz



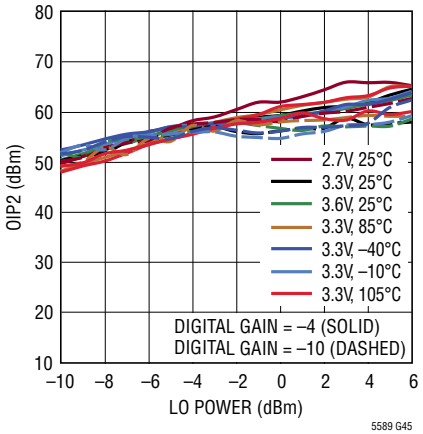
Output IP2 vs LO Power at f_{LO} = 700MHz



Output IP2 vs LO Power at f_{LO} = 900MHz



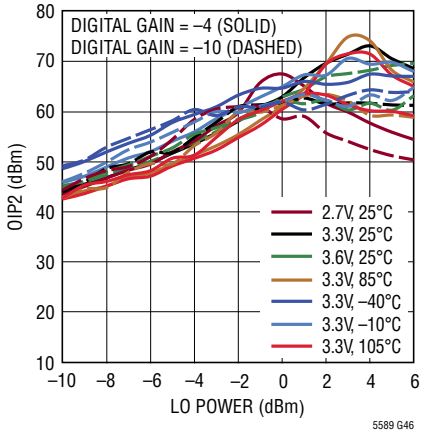
Output IP2 vs LO Power at f_{LO} = 1800MHz



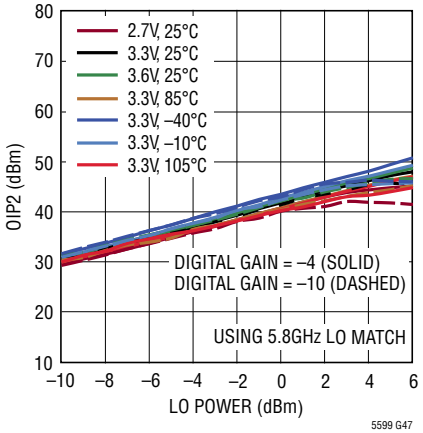
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

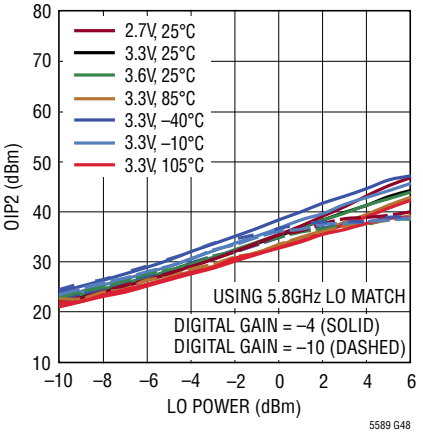
Output IP2 vs LO Power at f_{LO} = 2500MHz



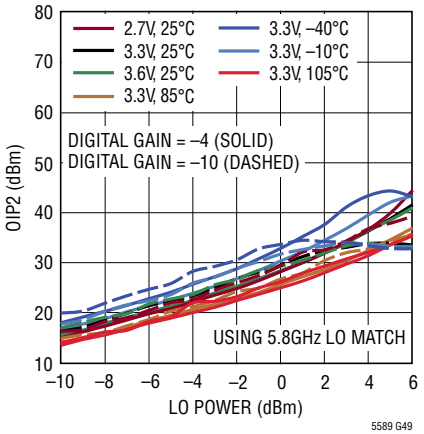
Output IP2 vs LO Power at f_{LO} = 3500MHz



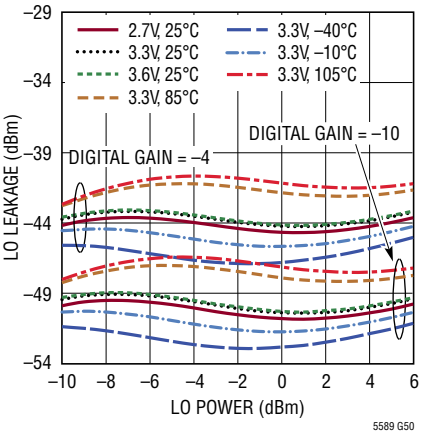
Output IP2 vs LO Power at f_{LO} = 4500MHz



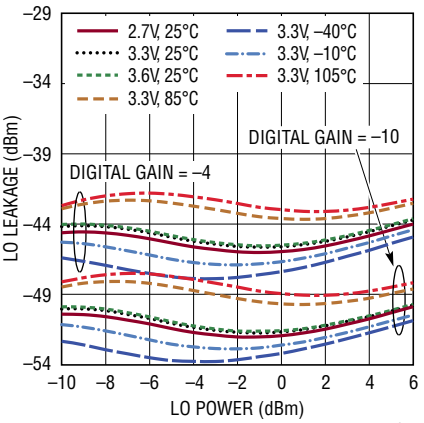
Output IP2 vs LO Power at f_{LO} = 5800MHz



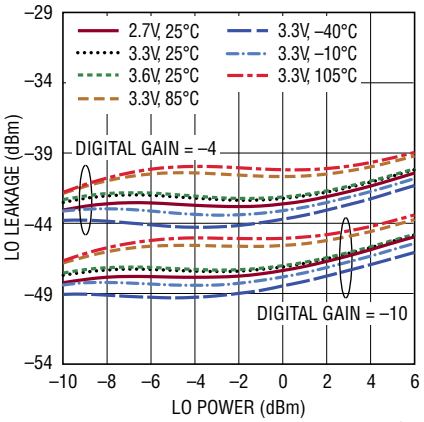
LO Leakage vs LO Power at f_{LO} = 700MHz



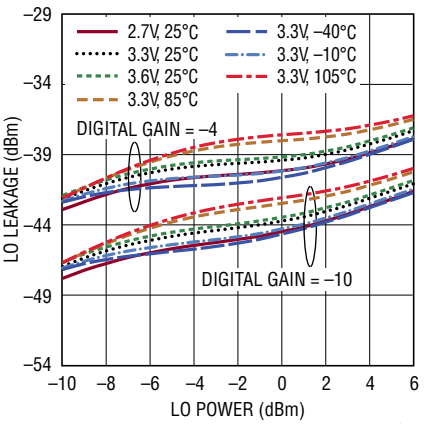
LO Leakage vs LO Power at f_{LO} = 900MHz



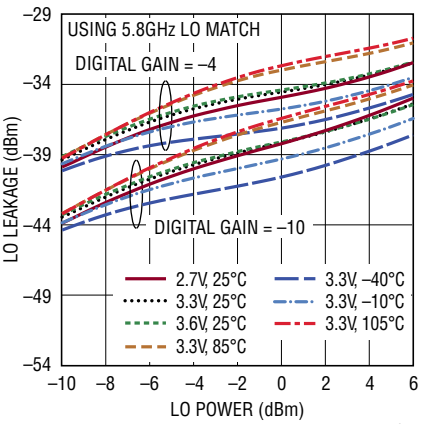
LO Leakage vs LO Power at f_{LO} = 1800MHz



LO Leakage vs LO Power at f_{LO} = 2500MHz



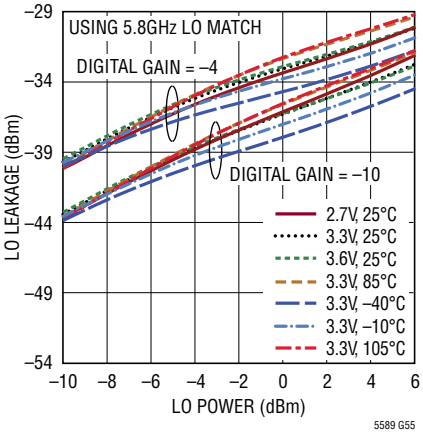
LO Leakage vs LO Power at f_{LO} = 3500MHz



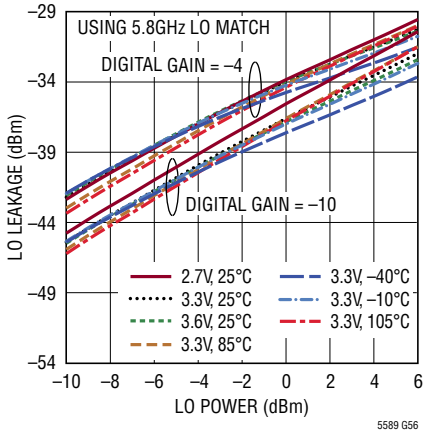
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

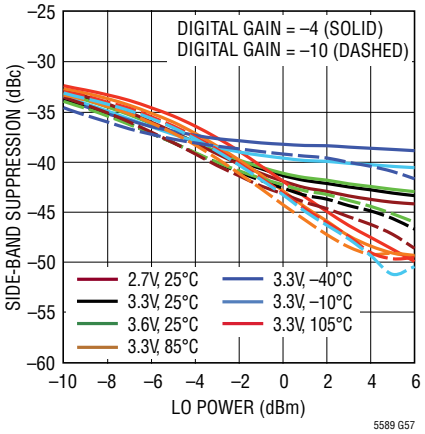
LO Leakage vs LO Power at f_{LO} = 4500MHz



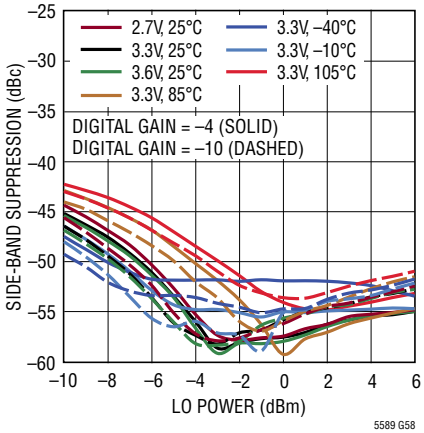
LO Leakage vs LO Power at f_{LO} = 5800MHz



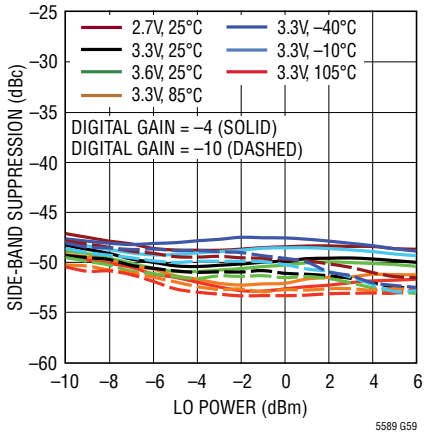
Side-Band Suppression vs LO Power at f_{LO} = 700MHz



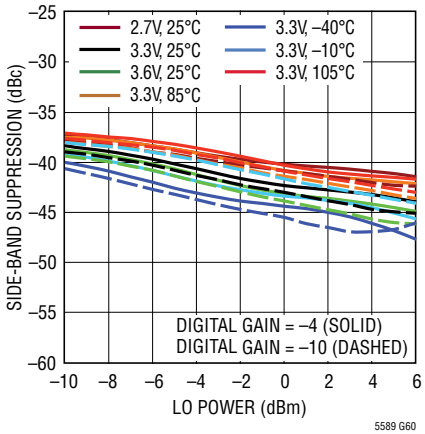
Side-Band Suppression vs LO Power at f_{LO} = 900MHz



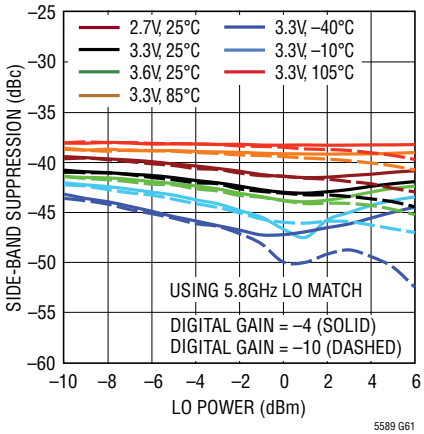
Side-Band Suppression vs LO Power at f_{LO} = 1800MHz



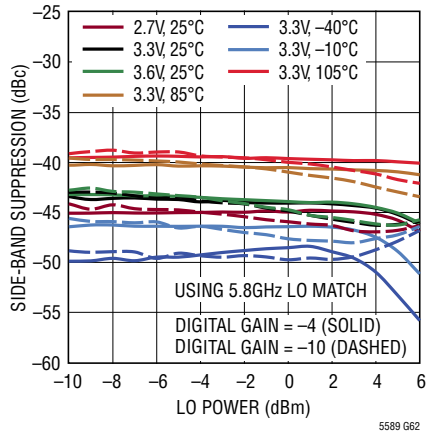
Side-Band Suppression vs LO Power at f_{LO} = 2500MHz



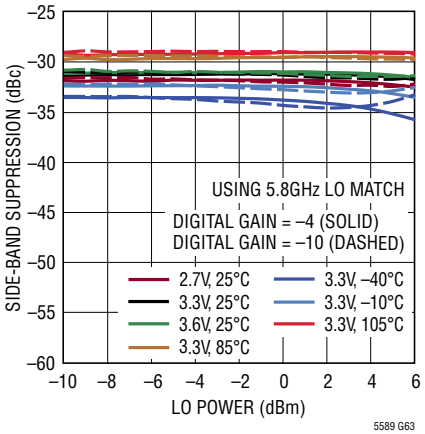
Side-Band Suppression vs LO Power at f_{LO} = 3500MHz



Side-Band Suppression vs LO Power at f_{LO} = 4500MHz



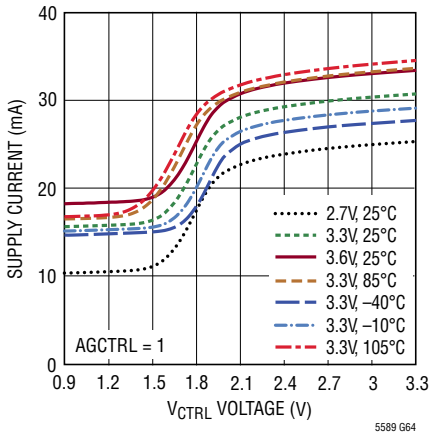
Side-Band Suppression vs LO Power at f_{LO} = 5800MHz



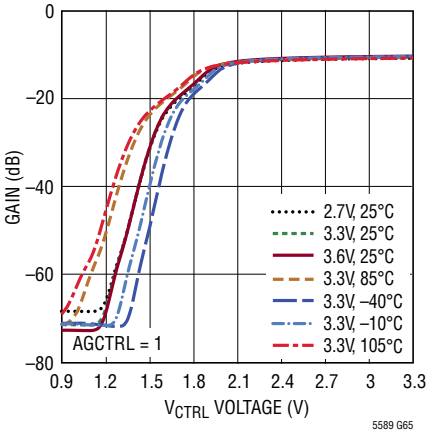
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

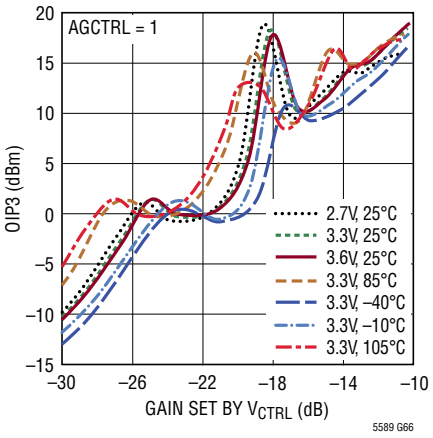
Supply Current vs V_{CTRL} Voltage



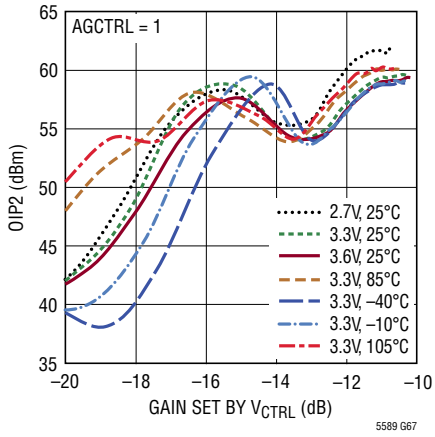
Gain vs V_{CTRL} Voltage



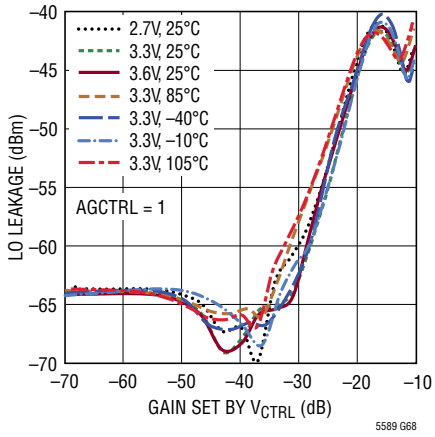
Output IP3 vs V_{CTRL} Gain



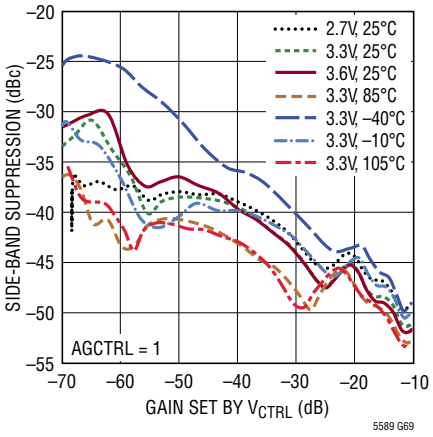
Output IP2 vs V_{CTRL} Gain



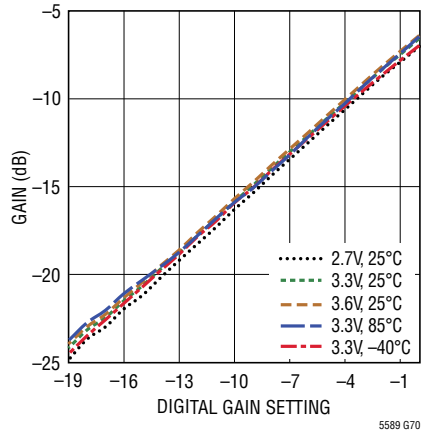
LO Leakage vs V_{CTRL} Gain



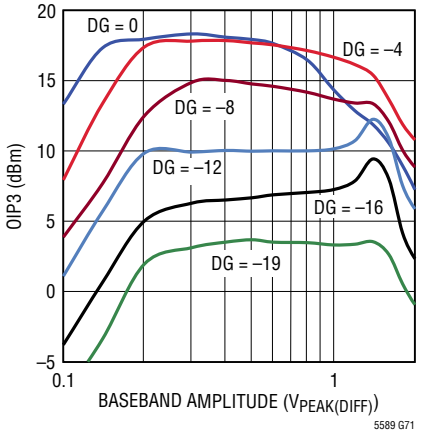
Side-Band Suppression vs V_{CTRL} Gain



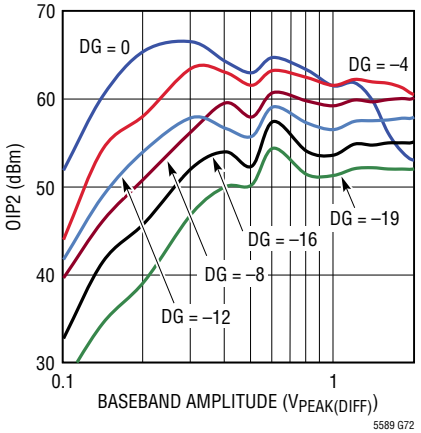
Gain vs Digital Gain Setting



Output IP3 vs Baseband Amplitude



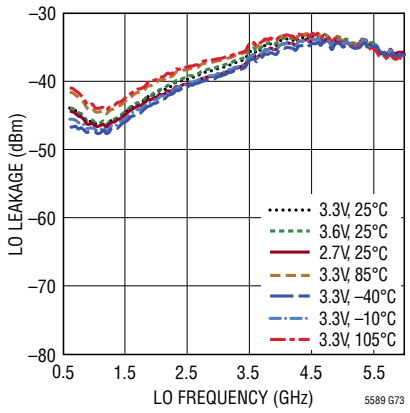
Output IP2 vs Baseband Amplitude



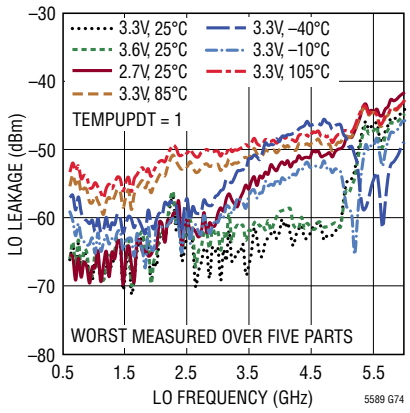
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

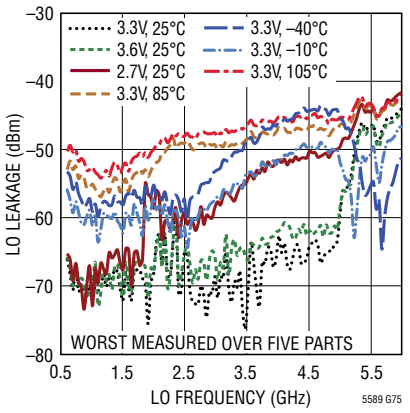
LO Leakage vs LO Frequency for Gain TempComp On



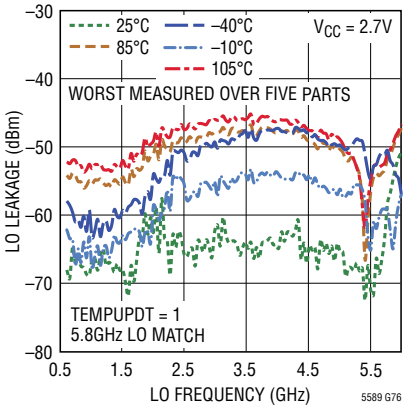
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration Using Reg. 0x02 and 0x03, Gain TempComp Off



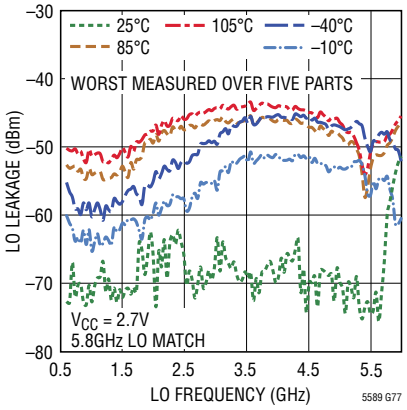
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration Using Reg. 0x02 and 0x03, Gain TempComp On



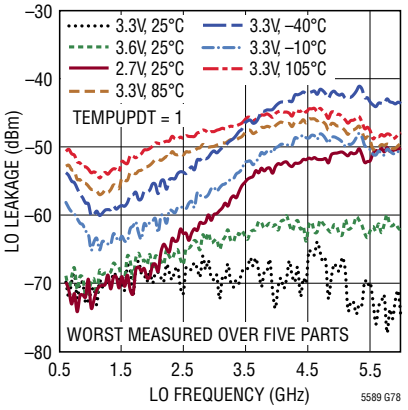
LO Leakage vs LO Frequency After 25°C, 2.7V Calibration Using Reg. 0x02 and 0x03, Gain TempComp Off



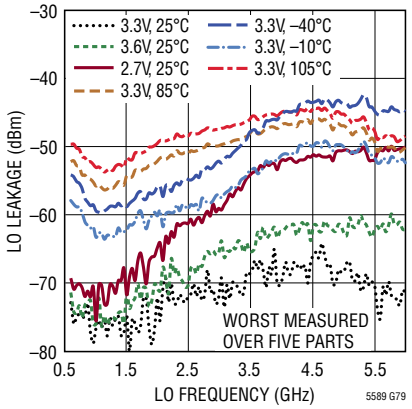
LO Leakage vs LO Frequency After 25°C, 2.7V Calibration Using Reg. 0x02 and 0x03, Gain TempComp On



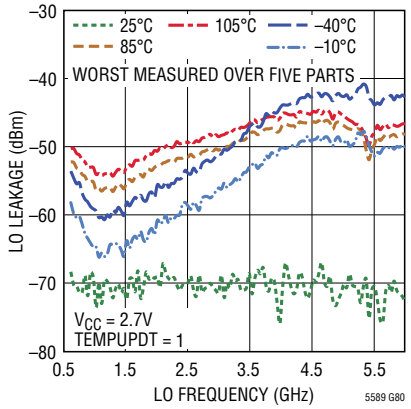
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration Using I and Q Offset, Gain TempComp Off



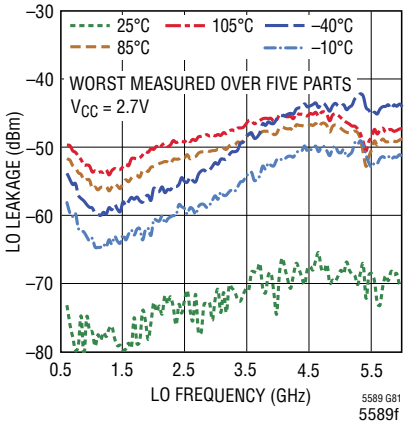
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration Using I and Q Offset, Gain TempComp On



LO Leakage vs LO Frequency After 25°C, 2.7V Calibration Using I and Q Offset, Gain TempComp Off



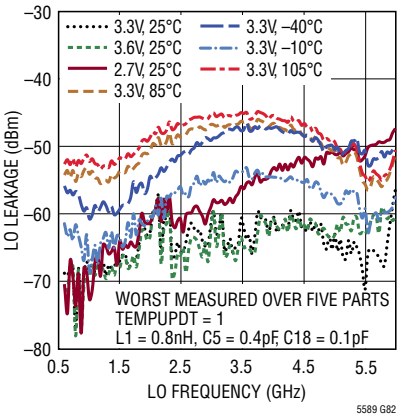
LO Leakage vs LO Frequency After 25°C, 2.7V Calibration Using I and Q Offset, Gain TempComp On



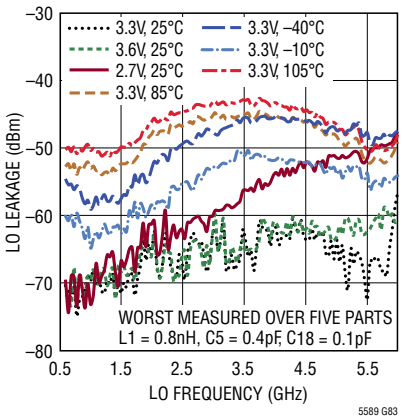
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

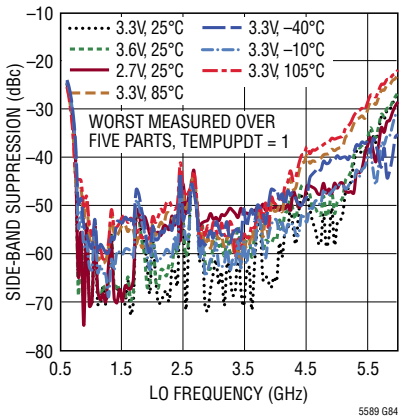
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration with 5.8GHz Match Using Reg. 0x02 and 0x03, Gain TempComp Off



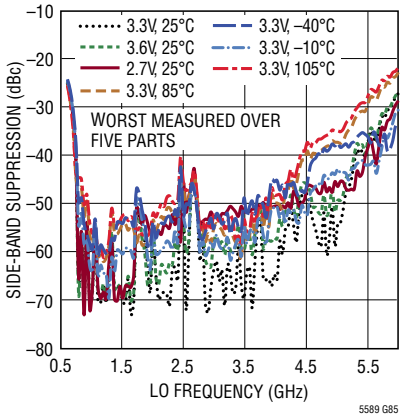
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration with 5.8GHz Match Using Reg. 0x02 and 0x03, Gain TempComp On



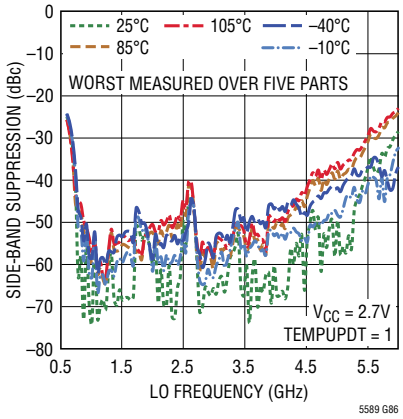
Side-Band Suppression vs LO Frequency After 25°C, 3.3V Calibration, Gain TempComp Off



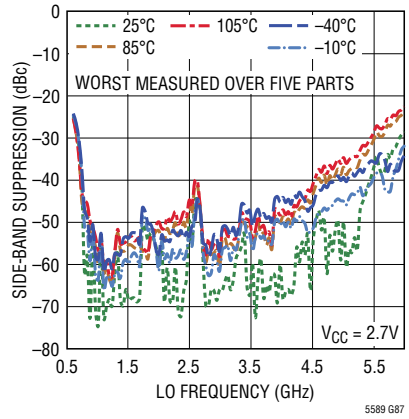
Side-Band Suppression vs LO Frequency After 25°C, 3.3V Calibration, Gain TempComp On



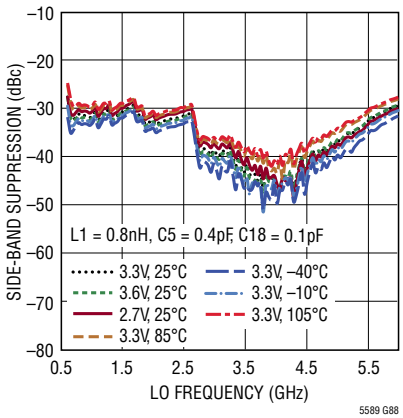
Side-Band Suppression vs LO Frequency After 25°C, 2.7V Calibration, Gain TempComp Off



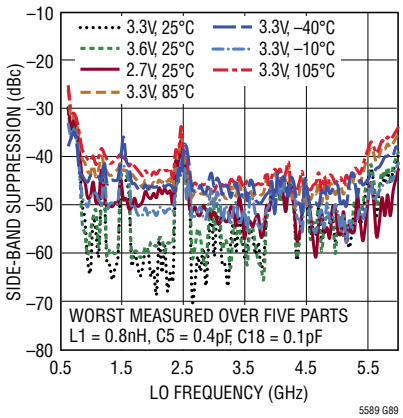
Side-Band Suppression vs LO Frequency After 25°C, 2.7V Calibration, Gain TempComp On



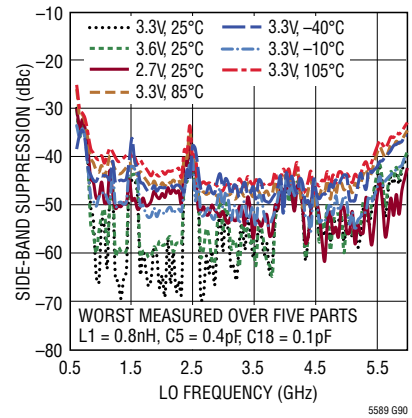
Side-Band Suppression vs LO Frequency Using 5.8GHz Match



Side-Band Suppression vs LO Frequency After 25°C, 3.3V Calibration with 5.8GHz Match Using Reg. 0x02 and 0x03, Gain TempComp Off



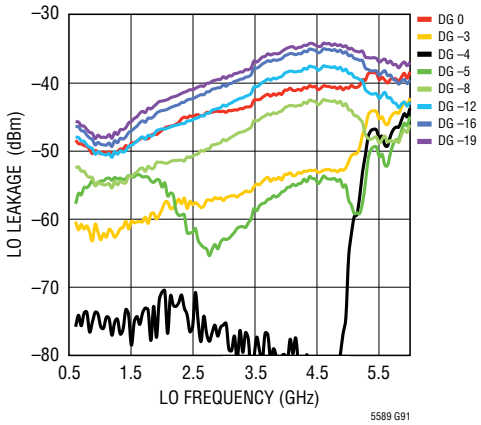
Side-Band Suppression vs LO Frequency After 25°C, 3.3V Calibration with 5.8GHz Match Using Reg. 0x02 and 0x03, Gain TempComp On



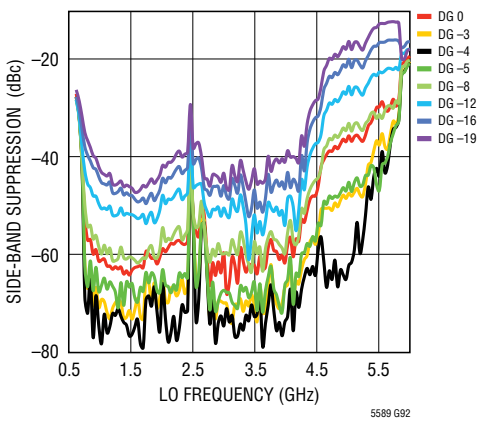
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

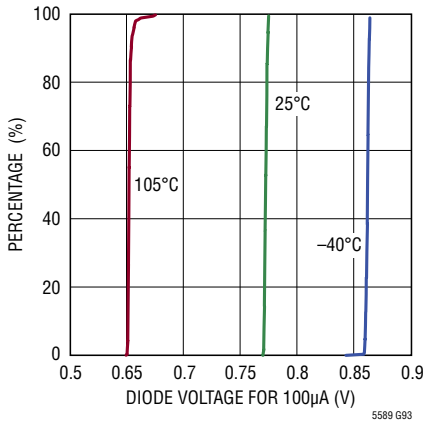
LO Leakage vs LO Frequency and Digital Gain Setting After Calibration Using Reg. 0x02 and 0x03 at Digital Gain = –4



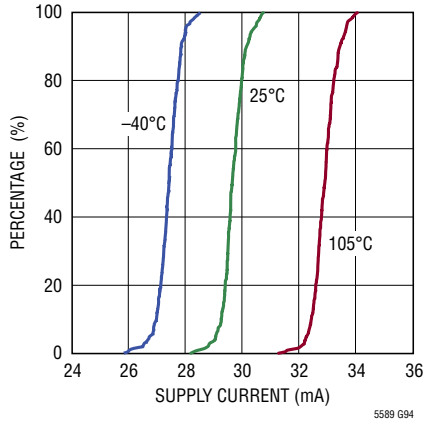
Side-Band Suppression vs LO Frequency and Digital Gain Setting After Calibration at Digital Gain = –4



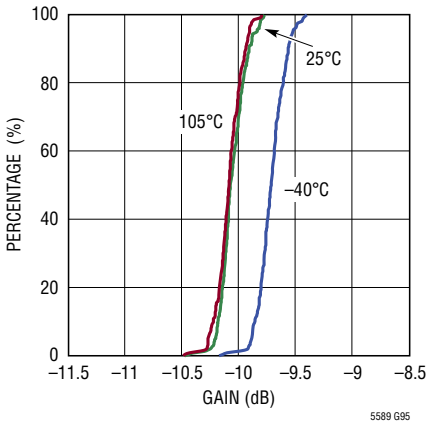
Temperature Sensing Diode Voltage Cumulative Distribution



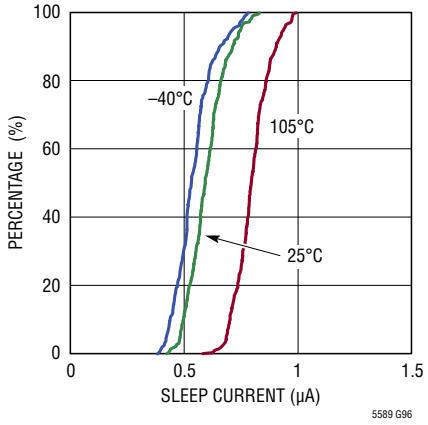
Supply Current Cumulative Distribution



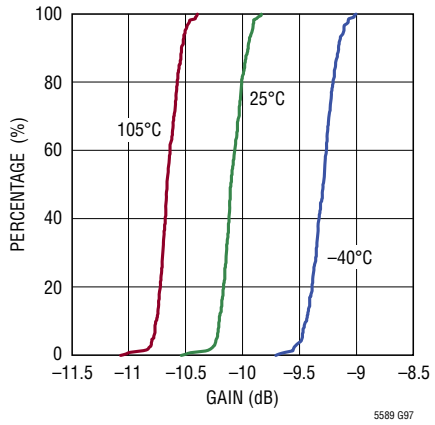
Gain Cumulative Distribution for Gain TempComp On



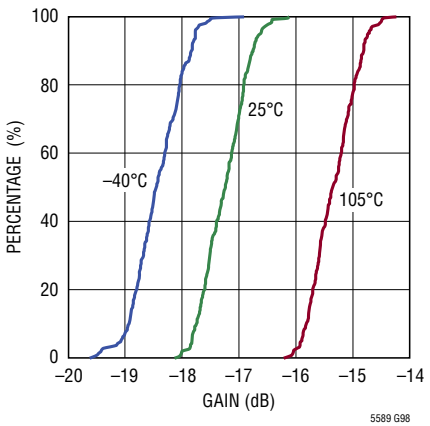
Sleep Current Cumulative Distribution



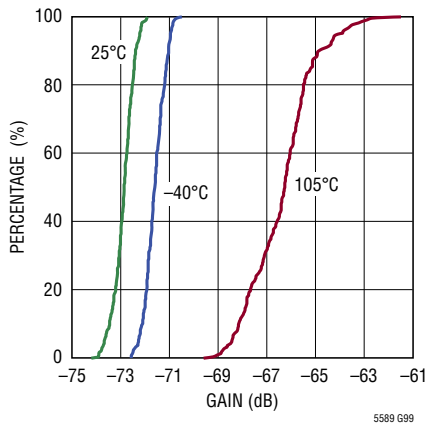
Gain Cumulative Distribution for Gain TempComp Off



Gain Cumulative Distribution for V_{CTRL} = 1.75V



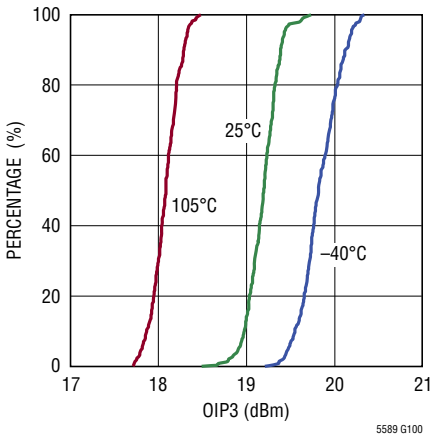
Gain Cumulative Distribution for V_{CTRL} = 1V



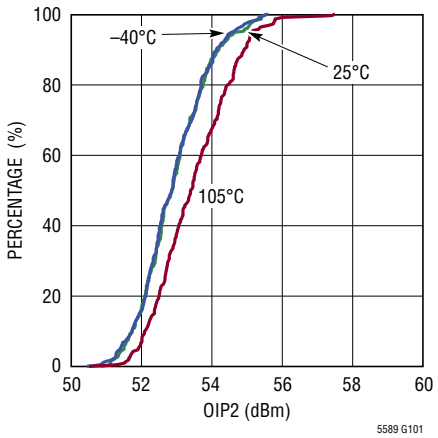
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

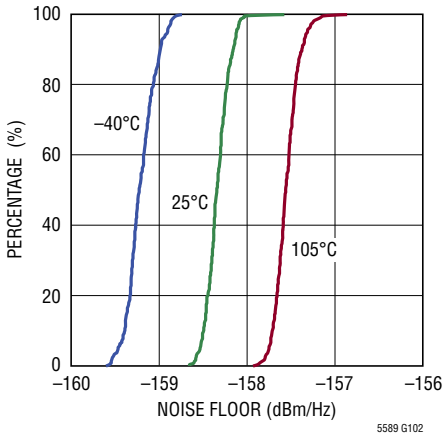
Output IP3 Cumulative Distribution



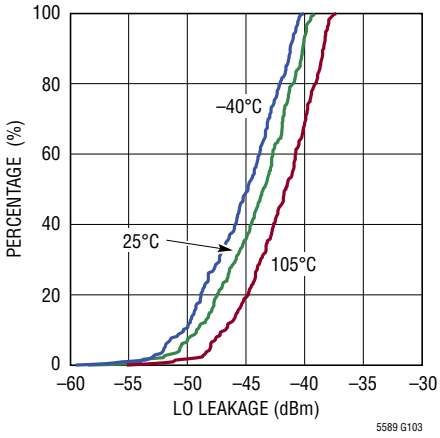
Output IP2 Cumulative Distribution



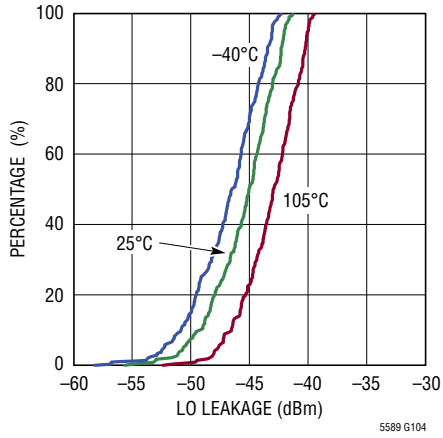
Output Noise Floor Cumulative Distribution



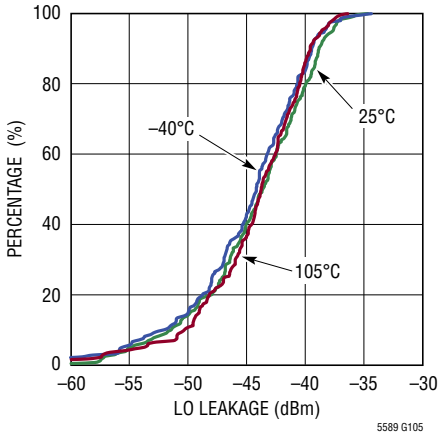
LO Leakage Cumulative Distribution for Floating Baseband Pins



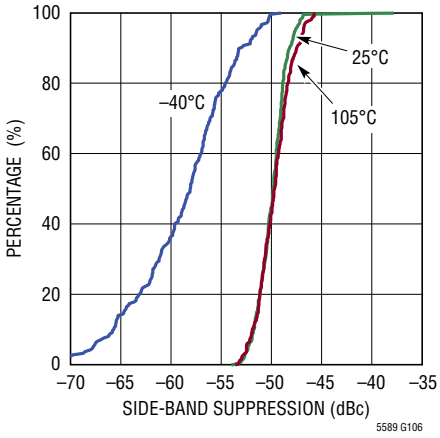
LO Leakage Cumulative Distribution



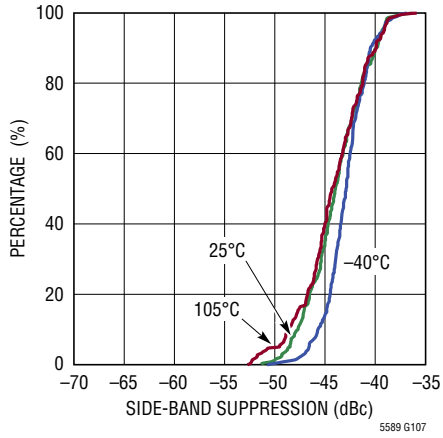
LO Leakage Cumulative Distribution for V_{CTRL} = 1.75V



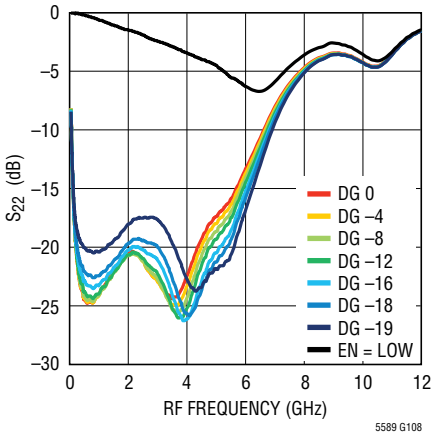
Side-Band Suppression Cumulative Distribution



Side-Band Suppression Cumulative Distribution for V_{CTRL} = 1.75V



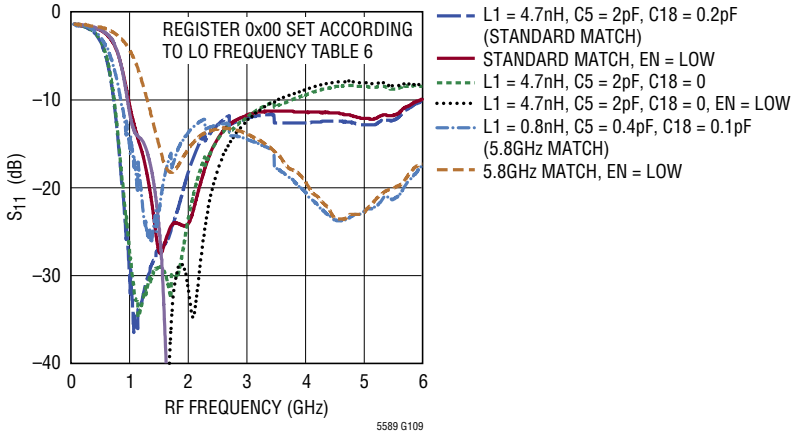
RF Return Loss



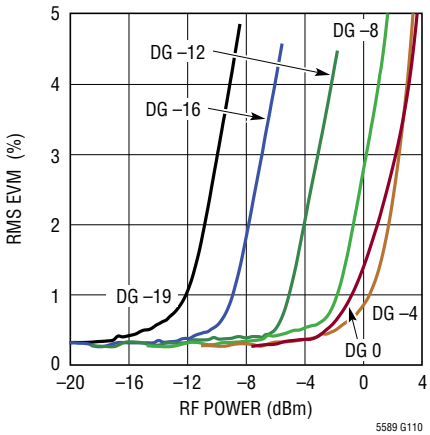
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

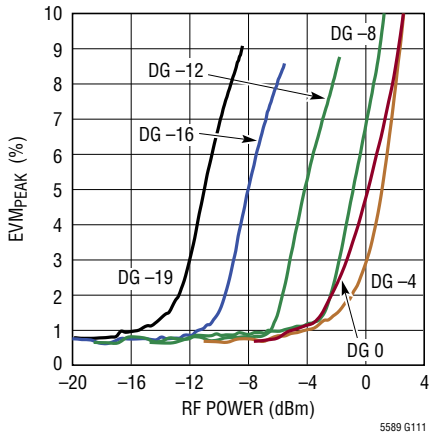
LO Return Loss



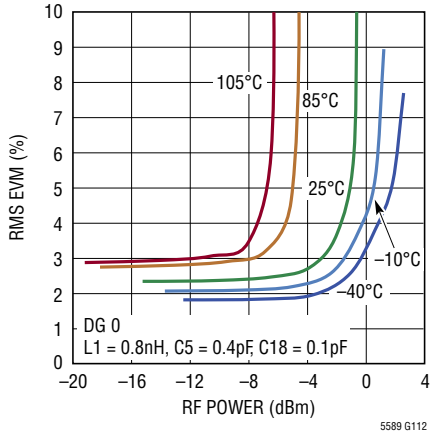
RMS EVM vs RF Output Power at f_{LO} = 2.17GHz with 1Ms/s 16-QAM Signal



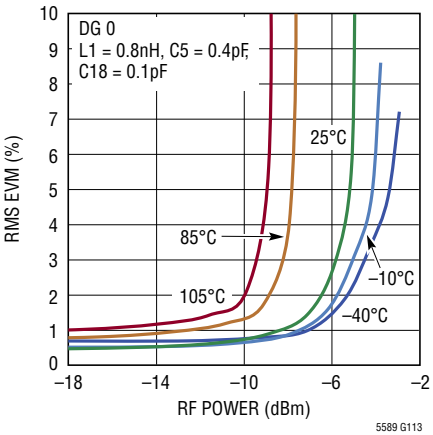
Peak EVM vs RF Output Power at f_{LO} = 2.17GHz with 1Ms/s 16-QAM Signal



RMS EVM vs RF Output Power at f_{LO} = 5.8GHz with 1Ms/s 16-QAM Signal



RMS EVM vs RF Output Power at f_{LO} = 5.8GHz with 1Ms/s 16-QAM Signal After 25°C, 3.3V Calibration



PIN FUNCTIONS

V_{CTRL} (Pin 1): Variable Gain Control Input. This analog control pin sets the gain. Write a "1" to bit 6 in register 0x01 (AGCTRL = 1) to activate this pin, resulting in about 2.5mA current draw from a positive supply. Typical V_{CTRL} voltage range is 0.9V to 3.3V. Gain transfer function is not linear-in-dB. Tie to V_{CC} when not used.

GND (Pins 2, 5, 12, 13, 14, 15, 17, 18, Exposed Pad 25): Ground. All these pins are connected together internally. For best RF performance all ground pins should be connected to RF ground.

LOL, LOC (Pins 3, 4): LO Inputs. This is not a differential input. Both pins are 50Ω inputs. An LC diplexer is recommended to be used at these pins (see Figure 12). AC-coupling capacitors are required at these pins if the applied DC level is higher than ±50mV.

TTCK (Pin 6): Temperature Update. When the TTCK temperature update mode is selected in register 0x01 (bit 7 = High, TEMPUPDT = 1), the temperature readout and digital gain compensation vs temperature can be updated through a logic low to logic high transition at this pin. Do not float.

TEMP (Pin 7): Temperature Sensing Diode. This pin is connected to the anode of a diode that may be used to measure the die temperature, by forcing a current and measuring the voltage. This diode is not part of the on-chip thermometer.

BBPI, BBMI (Pins 8, 9): Baseband Inputs of the I-Channel. The input impedance of each input is about 1kΩ. It should be externally biased to a 1.4V common mode level, or AC-coupled. Do not apply common mode voltage beyond $2V_{DC}$.

BBPQ, BBMQ (Pins 10, 11): Baseband Inputs of the Q-Channel. The input impedance of each input is about 1kΩ. It should be externally biased to a 1.4V common mode level, or AC-coupled. Do not apply common mode voltage beyond $2V_{DC}$. Float if Q-channel is disabled.

RF (Pin 16): RF Output. The output impedance at RF frequencies is 50Ω. Its DC output voltage is about 1.7V if enabled. An AC-coupling capacitor should be used at this pin with a recommended value of 100pF.

CSB (Pin 19): Serial Port Chip Select. This CMOS input initiates a serial port transaction when driven low, ending the transaction when driven back high. Do not float.

SCLK (Pin 20): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. Do not float.

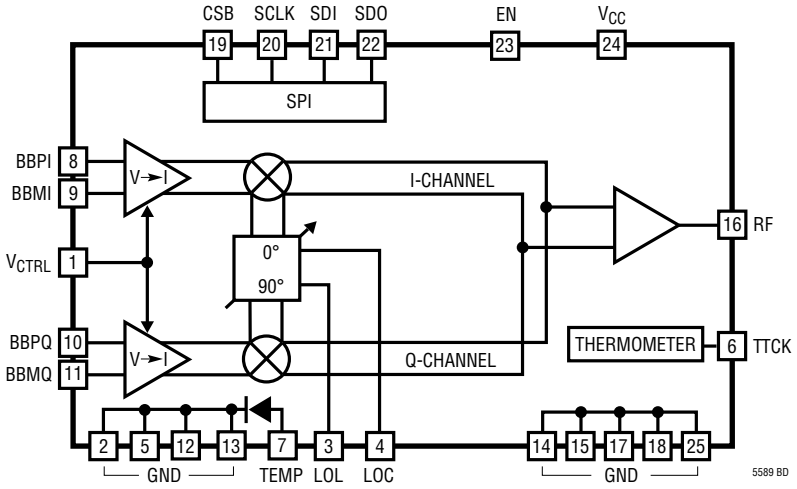
SDI (Pin 21): Serial Port Data Input. The serial port uses this CMOS input for data. Do not float.

SDO (Pin 22): Serial Port Data Output. This NMOS output presents data from the serial port during a read transaction. Connect this pin to the digital supply voltage through a pull-up resistor of sufficiently large value, to ensure that the current does not exceed 10mA when pulled low.

EN (Pin 23): Enable Pin. The chip is completely turned on when a logic high voltage is applied to this pin, and completely turned off for a logic low voltage. Do not float.

V_{CC} (Pin 24): Power Supply. It is recommended to use 1nF and 4.7µF capacitors for decoupling to ground on this pin.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC5589 consists of I and Q input differential voltage-to-current converters, I and Q upconverting mixers, an RF output buffer and an LO quadrature phase generator. An SPI bus addresses nine control registers, enabling optimization of side-band suppression, LO leakage, and adjustment of the modulator gain. See Table 1 for a summary of the writable registers and their default values. A full map of all the registers in the LTC5589 is listed in Table 8 and Table 9 in the Appendix.

Table 1. SPI Writable Registers and Default Register Values.

ADDRESS	DEFAULT VALUE	SETTING	REGISTER FUNCTION
0x00	0x3E	2.56GHz	LO Frequency Tuning
0x01	0x84	DG = –4	Gain
0x02	0x80	0mV	Offset I-Channel
0x03	0x80	0mV	Offset Q-Channel
0x04	0x80	0dB	I/Q Gain Ratio
0x05	0x10	0°	I/Q Phase Balance
0x06	0x50	OFF	LO Port Matching Override
0x07	0x06	OFF	Temperature Correction Override
0x08	0x00	NORMAL	Operating Mode

Without using the SPI the registers will use the default values which may not result in the optimum side-band suppression (SB). For example: for LO frequency from about 2.44GHz to about 2.72GHz, the SB is about –40dBc; from 1.7GHz to 2.44GHz and 2.72GHz to 2.93GHz it falls to about –35dBc.

Aside of powering up the LTC5589, the register values can be reset to the default values by setting SRESET = 1 (bit 3, register 0x08). After about 50ns SRESET is automatically set back to 0.

External I and Q baseband signals are applied to the differential baseband input pins: BBPI, BBMI and BBPQ, BBMQ. These voltage signals are converted to currents and translated to RF frequency by means of double-balanced upconverting mixers. The mixer outputs are combined at the inputs of the RF output buffer, which also transforms the output impedance to 50Ω. The center frequency of the resulting RF signal is equal to the LO signal frequency.

The LO inputs drive a phase shifter which splits the LO signal into in-phase and quadrature signals which drive the upconverting mixers. In most applications, the LOL input is driven by the LO source via a 4.7nH inductor, while the LOC input is driven by the LO source via a 2pF capacitor. This inductor and capacitor form a diplexer circuit tuned to 1.4GHz. The RF output is single-ended and internally 50Ω matched across a wide RF frequency range from 55MHz to 6.6GHz with better than 10dB return loss using C4 = 100pF and C17 = 0.2pF. See Figure 12.

Baseband Interface

The baseband inputs (BBPI, BBMI, BBPQ, BBMQ) present a differential input impedance of about 1.8kΩ, as depicted in Figure 1. The baseband bandwidth depends on the source impedance and the frequency setting (register 0x00). It is recommended to compensate the baseband input impedance in the baseband lowpass filter design in order to achieve best gain flatness vs baseband frequency. The S-parameters for (each of) the baseband inputs are given in Table 2 for various LO frequency and gain settings.

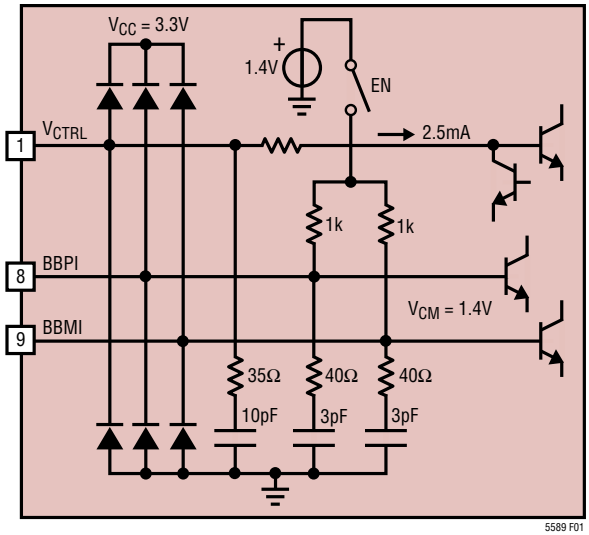


Figure 1. Simplified Circuit Schematic of the Base Band Input Interface (Only One Channel Is Shown).

APPLICATIONS INFORMATION

Table 2. Differential Baseband (BB) Input Impedance vs Frequency for EN = High and V_{CMBB} = 1.4V

BB FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)		REFL COEFFICIENT	
	REAL*	IMAG* (CAP)	MAG	ANGLE(°)
LO FREQUENCY = 0.8GHz (REG. 0x00 = 0x70), DIGITAL GAIN = –4dB				
1	1.84k	–12.8k (12pF)	0.897	–0.9
10	1.76k	–1.4k (11.3pF)	0.893	–8.2
20	1.55k	–705 (11.2pF)	0.881	–16
40	1.08k	–360(11pF)	0.841	–31
100	368	–157 (9.8pF)	0.680	–68
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = –4dB				
1	1.84k	–16.8k (9.2pF)	0.897	–0.7
10	1.79k	–1.74k (9.1pF)	0.895	–6.6
20	1.65k	–876 (9pF)	0.887	–13
40	1.27	–444 (8.9pF)	0.860	–26
100	501	–186 (8.3pF)	0.733	–58
200	204	–113 (6.9pF)	0.591	–91
LO FREQUENCY = 2.5GHz (REG. 0x00 = 0x3F), DIGITAL GAIN = –4dB				
1	1.84k	–17.7k (8.7pF)	0.897	–0.6
10	1.8k	–1.84k (8.6pF)	0.895	–6.2
20	1.67k	–924 (8.5pF)	0.888	–12
40	1.31k	–468 (8.5pF)	0.864	–24
100	539	–194 (7.9pF)	0.745	–56
200	219	–116 (6.7pF)	0.602	–89
400	100	–81 (4.8pF)	0.524	–122
LO FREQUENCY = 3.8GHz (REG. 0x00 = 0x2B), DIGITAL GAIN = –4dB				
1	1.84k	–18.8k (8.2pF)	0.897	–0.6
10	1.8k	–1.96k (8.1pF)	0.895	–5.9
20	1.69k	–985 (8pF)	0.889	–12
40	1.36k	–499 (7.9pF)	0.868	–23
100	585	–206 (7.5pF)	0.758	–53
200	238	–120 (6.4pF)	0.616	–85
400	106	–83 (4.7pF)	0.528	–119
LO FREQUENCY = 5.8GHz (REG. 0x00 = 0x1A), DIGITAL GAIN = –4dB				
1	1.84k	–19.6k (7.8pF)	0.897	–0.6
10	1.81k	–2k (7.8pF)	0.895	–5.7
20	1.69k	–1.02 (7.7pF)	0.890	–11
40	1.38k	–516 (7.7pF)	0.869	–22
100	611	–212 (7.2pF)	0.765	–51
200	250	–123 (6.3pF)	0.623	–84
400	110	–84 (4.6pF)	0.530	–118

Table 2. Differential Baseband (BB) Input Impedance vs Frequency for EN = High and V_{CMBB} = 1.4V (continued)

BB FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)		REFL COEFFICIENT	
	REAL*	IMAG* (CAP)	MAG	ANGLE(°)
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = 0dB				
1	1.78k	–16.9k (9.1pF)	0.902	–0.7
10	1.73k	–1.75k (9pF)	0.891	–6.6
20	1.6k	–878 (9pF)	0.884	–13
40	1.24k	–445 (8.9pF)	0.857	–25
100	497	–186 (8.3pF)	0.732	–58
200	203	–113 (6.8pF)	0.590	–91
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = –19dB				
1	1.94k	–16.7k (9.2pF)	0.893	–0.7
10	1.88k	–1.74k (9.1pF)	0.899	–6.6
20	1.72k	–874 (9pF)	0.892	–13
40	1.31k	–443 (8.9pF)	0.865	–26
100	507	–185 (8.3pF)	0.736	–58
200	205	–112 (6.9pF)	0.592	–91
EN = Low (Chip Disabled)				
1	1.96k	–20.1k (7.6pF)	0.903	–0.6
10	1.92k	–2.08k (7.6pF)	0.901	–5.5
20	1.8k	–1.05k (7.5pF)	0.895	–11
40	1.46k	–530 (8.9pF)	0.876	–21
100	639	–218 (8.3pF)	0.772	–50
200	260	–126 (6.1pF)	0.629	–82

*Parallel Equivalent

In Table 3 the common-mode S-parameters of the differential baseband inputs are given. The circuit is optimized for a common mode voltage of 1.4V which can be internally or externally applied. In case of AC-coupling to the baseband pins (1.4V internally generated bias) make sure that the high pass filter corner is not affecting the low frequency components of the baseband signal. Even a small error for low baseband frequencies can result in degraded EVM.

The baseband input offset voltage depends on the source resistance. In case of AC-coupling the 1 sigma offset is about 1.7mV, resulting in about –43.7dBm LO leakage. For shorted baseband pins (0Ω source resistance), the LO leakage improves to about –45.6dBm. In case of AC-coupling the LO leakage can be reduced by connecting a resistor in parallel with the baseband inputs, thus

APPLICATIONS INFORMATION

Table 3. Common-Mode Baseband (BB) Input Impedance vs Frequency for EN = High and V_{CMBB} = 1.4V

BB FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)		REFL COEFFICIENT	
	REAL*	IMAG* (CAP)	MAG	ANGLE(°)
LO FREQUENCY = 0.8GHz (REG. 0x00 = 0x70), DIGITAL GAIN = –4dB				
1	536	–5.82k (25pF)	0.911	–0.5
10	534	–605 (24.9pF)	0.911	–4.7
20	541	–301 (25pF)	0.912	–9.5
40	447	–145 (26pF)	0.897	–20
100	165	–61 (24.2pF)	0.771	–46
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = –4dB				
1	536	–8.71k (16.8pF)	0.911	–0.3
10	547	–907 (16.6pF)	0.913	–3.2
20	599	–445 (16.9pF)	0.920	–6.4
40	620	–203 (18.7pF)	0.924	–14
100	322	–78 (18.9pF)	0.869	–36
200	135	–41 (18.1pF)	0.764	–64
LO FREQUENCY = 2.5GHz (REG. 0x00 = 0x3F), DIGITAL GAIN = –4dB				
1	537	–9.76k (15pF)	0.911	–0.3
10	550	–1.02k (14.8pF)	0.913	–2.8
20	609	–496 (15.2pF)	0.921	–5.8
40	654	–223 (17pF)	0.927	–13
100	380	–84 (17.4pF)	0.886	–33
200	167	–43 (17pF)	0.799	–61
400	55	–22 (16.6pF)	0.697	–102
LO FREQUENCY = 3.8GHz (REG. 0x00 = 0x2B), DIGITAL GAIN = -4dB				
1	537	–11.2k (13pF)	0.911	–0.3
10	551	–1.17k (12.8pF)	0.913	–2.4
20	617	–571 (13.1pF)	0.922	–5
40	685	–252 (15pF)	0.930	–11.3
100	449	–94 (15.6pF)	0.901	–30
200	217	–48 (15.5pF)	0.835	–56
400	71	–24 (15.7pF)	0.722	–97
LO FREQUENCY = 5.8GHz (REG. 0x00 = 0x1A), DIGITAL GAIN = –4dB				
1	537	–12.3k (11.9pF)	0.911	–0.2
10	552	–1.28k (11.8pF)	0.913	–2.2
20	620	–620 (12.2pF)	0.923	–4.6
40	698	–271 (14pF)	0.931	–11
100	486	–101 (14.6pF)	0.908	–28
200	249	–51 (14.6pF)	0.851	–53
400	83	–25 (14.9pF)	0.745	–93

Table 3. Common-Mode Baseband (BB) Input Impedance vs Frequency for EN = High and V_{CMBB} = 1.4V (continued)

BB FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)		REFL COEFFICIENT	
	REAL*	IMAG* (CAP)	MAG	ANGLE(°)
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = 0dB				
1	515	–8.6k (17pF)	0.907	–0.3
10	523	–895 (16.8pF)	0.909	–3.2
20	564	–443 (17pF)	0.915	–6.5
40	587	–203 (18.7pF)	0.919	–14
100	313	–78 (18.9pF)	0.865	–36
200	133	–41 (18.1pF)	0.762	–64
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = –19dB				
1	569	–8.94k (16.4pF)	0.916	–0.3
10	587	–929 (16.2pF)	0.918	–3.1
20	663	–447 (16.8pF)	0.928	–6.4
40	675	–203 (18.7pF)	0.930	–14
100	337	–78 (18.9pF)	0.874	–36
200	138	–41 (18pF)	0.768	–64
EN = Low (Chip Disabled)				
1	1.01k	–10.6k (14.2pF)	0.952	–0.3
10	1.07k	–1.08k (13.9pF)	0.952	–2.6
20	975	–546 (13.8pF)	0.950	–5.2
40	898	–275 (13.8pF)	0.946	–10
100	612	–108 (13.6pF)	0.925	–26
200	314	–54 (13.6pF)	0.877	–50

*Parallel Equivalent

lowering baseband input impedance and offset. Further, the low combined baseband input leakage current of 1.3nA in shutdown mode retains the voltage over the coupling capacitors, which helps to settle faster when the part is enabled again. It is recommended to drive the baseband inputs differentially to maintain the linearity. When a DAC is used as the signal source, a reconstruction filter should be placed between the DAC output and the LTC5589 baseband inputs to avoid aliasing.

Internal Gain Trim DACs

Four internal gain trim DACs (one for each baseband pin) are configured as 11-bit each. The usable DAC input value range is integer continuous from 64 to 2047 and 0 for shutdown. The DACs are not intended for baseband signal generation but for gain and offset setting only, because there are no reconstruction filters between the DACs and the mixer core, and there is only indirect access between