Four-Channel Multiplexed Transimpedance Amplifier with Output Multiplexing

FEATURES

- **220MHz –3dB Bandwidth with 2pF Input Capacitance**
- **Single-Ended Output**
- **74kΩ Transimpedance Gain**
- **4.5pA/$\sqrt{Hz}$ Input Current Noise Density at 200MHz (2pF)**
- **56nA_{RMS} Integrated Input Current Noise Over 200MHz (2pF)**
- **Linear Input Range 0µA to 30µA**
- Overload Current > ±400mA Peak
- Fast Overload Recovery 12ns, 1mA
- Fast Channel Switchover < 50ns
- Single 5V Supply
- 220mW Power Dissipation for 4 Channels
- 2V_{P-P} Output Swing on 100Ω Load
- 4mm × 4mm, 24-Lead QFN Package
- Output MUX Combines Multiple 4-Channel Devices to Create 4, 8,12,16, 24, 32 Channel Solutions

APPLICATIONS

- LIDAR Receiver
- Industrial Imaging

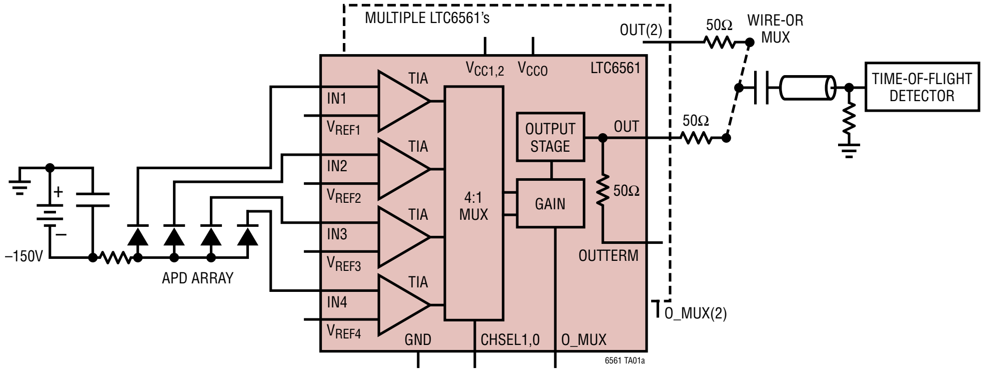
DESCRIPTION

The LTC®6561 is a low-noise, four-channel, transimpedance amplifier (TIA) with 220MHz bandwidth. The LTC6561 multi-channel transimpedance amplifier's low noise, high transimpedance, and low power dissipation are ideal for LIDAR receivers using Avalanche Photodiodes (APDs). The amplifier features 74kΩ transimpedance gain and 30µA linear input current range. Using an APD input circuit with a total capacitance of 2pF, the input current noise density is 4.5pA/$\sqrt{Hz}$ at 200MHz. With lower capacitance, noise and bandwidth improve further. Only a 5V single supply is needed and the device consumes only 220mW. Utilizing the internal 4-to-1 MUX along with the LTC6561's output MUX; multiple 4-channel LTC6561 devices can be combined to directly interface with 12-, 16- and 32-channel APD arrays. The LTC6561's fast overload recovery and fast channel switchover make it well suited for LIDAR receivers with multiple APDs. Its single-ended output can swing 2V_{P-P} on a 100Ω load while its low impedance opamp-style output can drive back-terminated 50Ω cables.

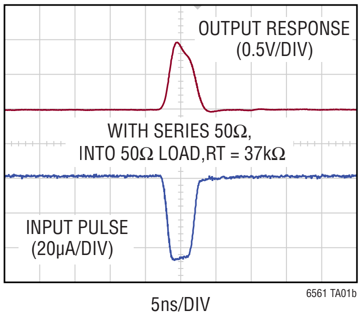
The LTC6561 is packaged in a compact 4mm × 4mm 24-pin leadless QFN package with an exposed pad for thermal management and low inductance.

TYPICAL APPLICATION

Typical Application with DC-Coupled Inputs Driving a Time-to-Digital Converter with Back-Terminated Cable



Pulse Response Overload Region (40µA)

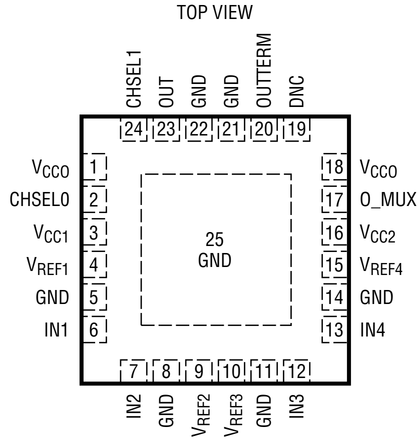


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC1}, V_{CC2}, V_{CCO} to GND)......5.5V
Input Current (CHSEL0, CHSEL1, O_MUX)...........–10mA
Amplifier Reference Current (V_{REF1}, V_{REF2},
V_{REF3}, V_{REF4}) .... ±10mA
Amplifier Input Current (IN1, IN2,
IN3, IN4) ....±400mA RMS ±2A Transient (10ns)
Amplifier Output Current (OUT, OUTTERM)........ +80mA
Operating Temperature Range
LTC6561I (Note 2)................................–40°C to 85°C
Storage Temperature Range ....–65°C to 150°C
Junction Temperature .... 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 47°C/W, θ_{JC} = 4.5°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6561IUF#PBF	LTC6561IUF#TRPBF	6561	24-LEAD (4mm × 4mm) PLASTIC QFN	–40°C to 85°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, $V_{CC1,2}$ = V_{CCO} = 5V, O_MUX = 0V, GND = 0V, Z_{LOAD} = 100Ω. Output is AC-coupled. Output taken from OUT pin.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BW	–3dB Bandwidth	200mV$_{P-P,OUT}$ and $C_{IN,TOT}$ = 2pF			220		MHz
R_T	Small Signal Transimpedance	I_{IN} < 2µA$_{P-P}$		63	74	85	kΩ
			●	47.7		93	
R_{IN}	Input Resistance	f = 100kHz			236		Ω
R_{OUT}	Output Resistance	f = 100kHz			3		Ω
I_n	Input Current Noise Density	f = 100MHz, $C_{IN,TOT}$ = 2pF			3.8		pA/√Hz
		f = 200MHz, $C_{IN,TOT}$ = 2pF			4.5		pA/√Hz
	Integrated Input Current Noise	f = 0.1MHz to 100MHz, $C_{IN,TOT}$ = 2pF			39		nA$_{RMS}$
		f = 0.1MHz to 200MHz, $C_{IN,TOT}$ = 2pF			56		nA$_{RMS}$
	Adjacent Channel to Channel Isolation	f = 100MHz			–45		dB
	Non Adjacent Channel Isolation	f = 100MHz			–65		dB
$t_{RECOVER}$	Overload Recovery Time	Input pulse <1mA			15		ns
t_{SWITCH}	Channel Switchover Time				50		ns

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, $V_{CC1,2}$ = V_{CCO} = 5V, O_MUX = 0V, GND = 0V, Z_{LOAD} = 100Ω. Output is AC-coupled. Output taken from OUT pin.

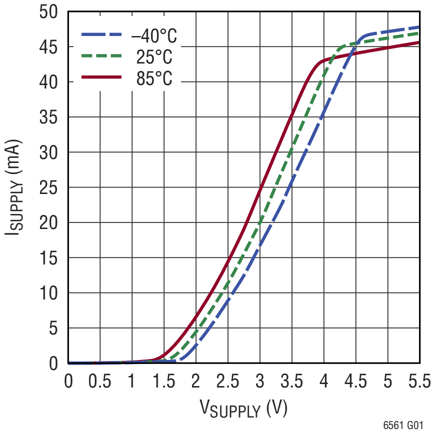
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN1,2,3,4 Pins and $V_{REF1,2,3,4}$ Pins							
V_{IN}	Input Bias Voltage	Active Channel		1.42	1.55	1.64	V
			●	1.32		1.74	V
		Inactive Channel		0.89	0.93	0.96	V
			●	0.79		1.06	V
V_{REF}	Input Reference Voltage	Active Channel		1.43	1.55	1.63	V
		Inactive Channel		1.34	1.50	1.67	V
Offset	V_{IN} – V_{REF}	Active Channel		–12		13.8	mV
		Inactive Channel		–727		–420	mV
OUT Pin							
V_{OUT}	Output Default Voltage	O_MUX = 0V		0.83	1.10	1.45	V
			●	0.79		1.67	V
		O_MUX = 3.3V, Standalone Device		0.32	0.60	0.88	V
			●	0.28		0.92	V
OVR	Output Voltage Range	I_{IN} Current Range= 0 to –50µA		1.22	1.90	2.58	V_{P-P}
			●	0.98		2.80	V_{P-P}
OUTTERM	Internal Series Resistor for Optional Output			48.6	50	70.8	Ω
CHSEL0, CHSEL1, O_MUX Pins with Internal Pull-Down Resistors							
V_{IL}						0.8	V
V_{IH}				1.5			V
I_{IL}	Pin Voltage = 0.8V			16.9	20.7	26.0	µA
			●	15.4		28.0	µA
I_{IH}	Pin Voltage = 1.5V			39.3	34.6	50.0	µA
			●	38.0		55.0	µA
C_{IN}					1.5		pF
R_{IN}				25	29	32	kΩ
			●	23		34	kΩ
Power Supply							
V_S	Operating Supply Range			4.75	5	5.25	V
$I_{CC1,2}$	Input Supply Current	V_{CC1} & V_{CC2} are Internally Tied Together		38.0	43	49.0	mA
			●	37.0		50.0	mA
I_{CCO}	Output Supply Current	Both V_{CCO} pins are Internally Tied Together		2.1	2.6	2.8	mA
			●	2.0		2.9	mA
I_S	Total Supply Current ($I_{S(VCC1,2)}$ + $I_{S(VCCO)}$)			40.1	45.6	51.8	mA
			●	39.0		52.9	mA
PSRR($V_{CC1,2}$)	Input Power Supply Rejection Ratio	$V_{CC1,2}$ = 4.75V to 5.25V, V_{CCO} = 5V		22	25		dB
			●	15			dB
PSRR(V_{CCO})	Output Power Supply Rejection Ratio	V_{CCO} = 4.75V to 5.25V, $V_{CC1,2}$ = 5V		34	40		dB
			●	33			dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

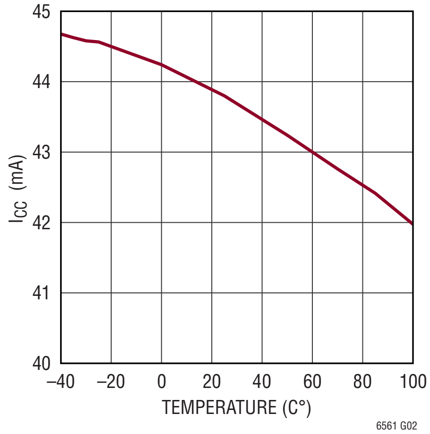
Note 2: The LTC6561I is guaranteed to meet specified performance from –40°C to 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS

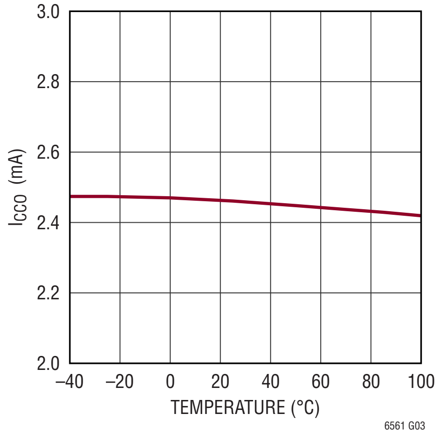
I_{SUPPLY} vs V_{SUPPLY} Over Temperature



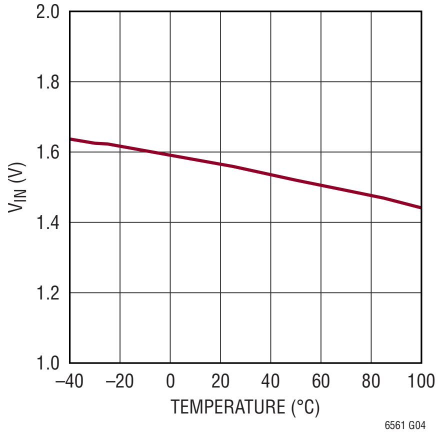
I_{CC} vs Temperature



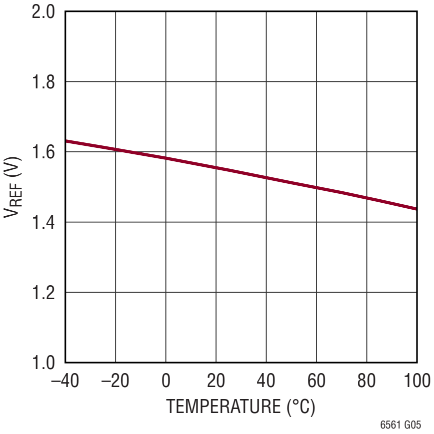
I_{CCO} vs Temperature



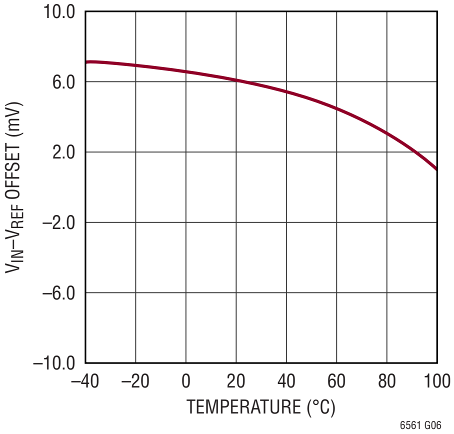
V_{IN} vs Temperature



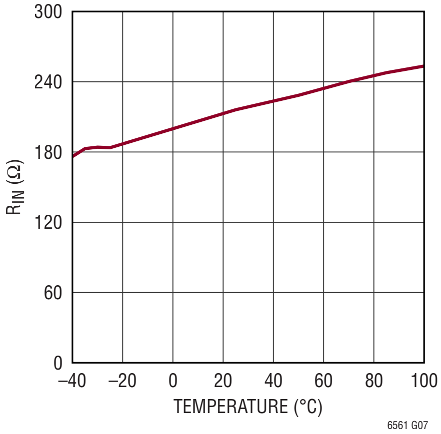
V_{REF} vs Temperature



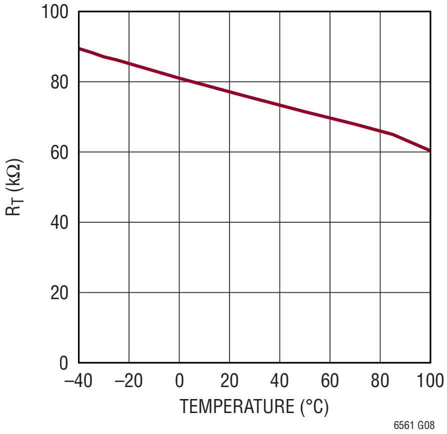
V_{IN}–V_{REF} Offset vs Temperature



R_{IN} vs Temperature

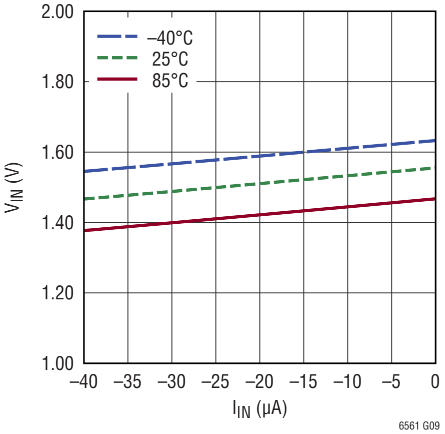


R_T Transpedance vs Temperature

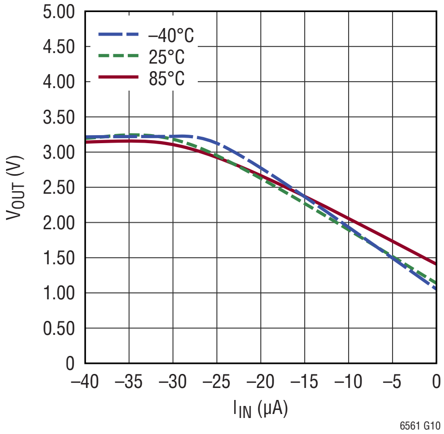


TYPICAL PERFORMANCE CHARACTERISTICS

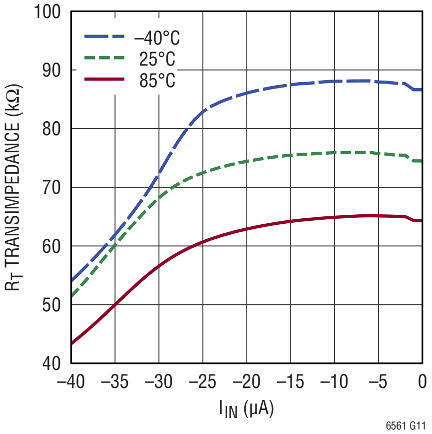
V_{IN} vs I_{IN} Over Temperature



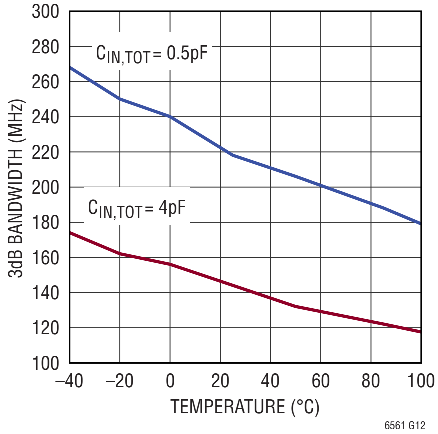
V_{OUT} vs I_{IN} Over Temperature



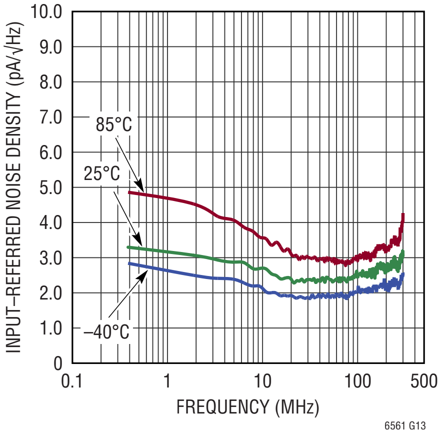
R_T Transimpedance vs I_{IN} Over Temperature



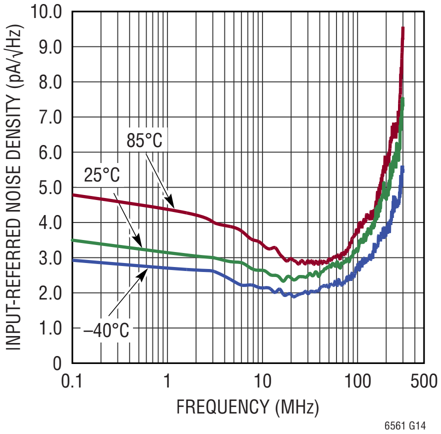
3dB Bandwidth vs Temperature Over $C_{IN,TOT}$



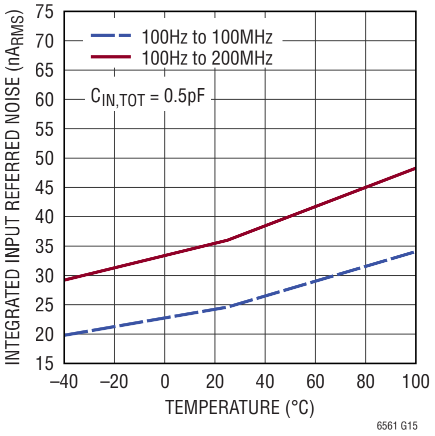
Input–Referred Noise Density with $C_{IN,TOT}$ = 0.5pF



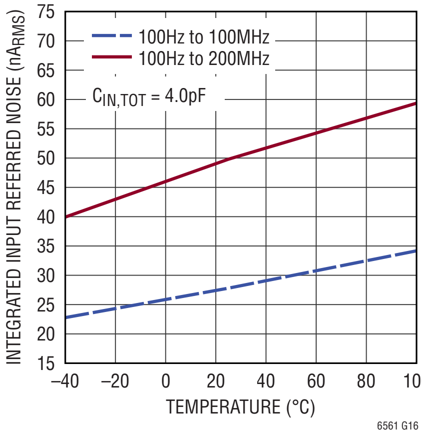
Input–Referred Noise Density with $C_{IN,TOT}$ = 4.0pF



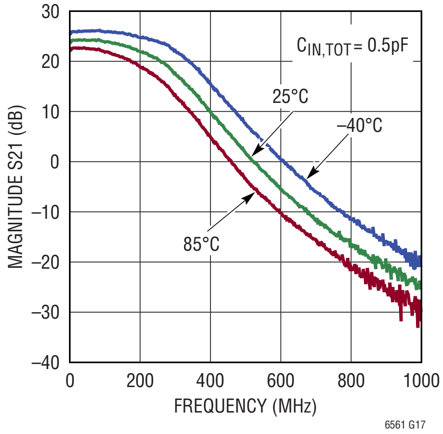
Integrated Input–Referred Noise vs Temperature with $C_{IN,TOT}$ = 0.5pF



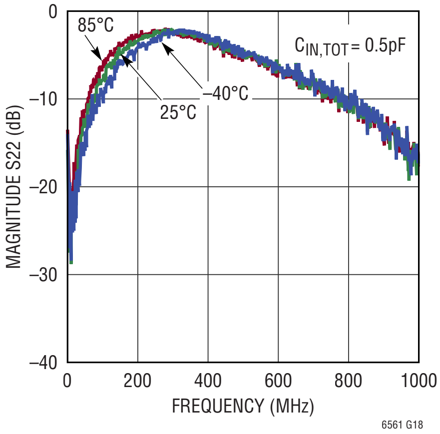
Integrated Input–Referred Noise vs Temperature with $C_{IN,TOT}$ = 4.0pF



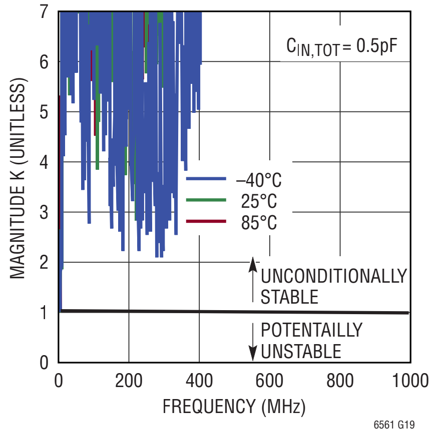
TYPICAL PERFORMANCE CHARACTERISTICS



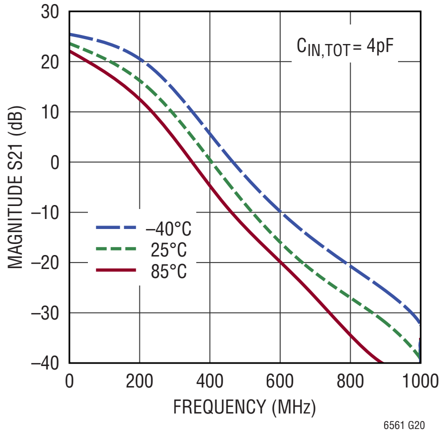
S21(Gain) vs Frequency Over Temperature



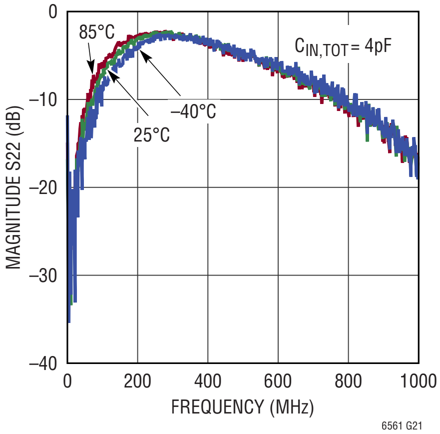
S22 vs Frequency Over Temperature



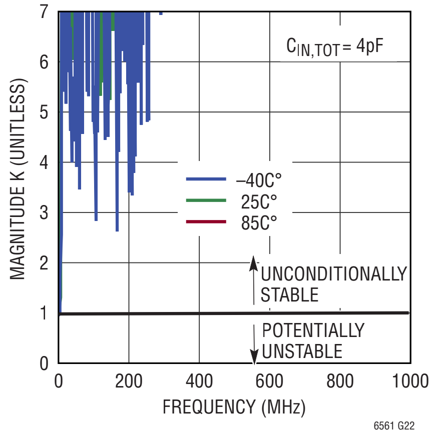
Stability Factor K vs Frequency Over Temperature



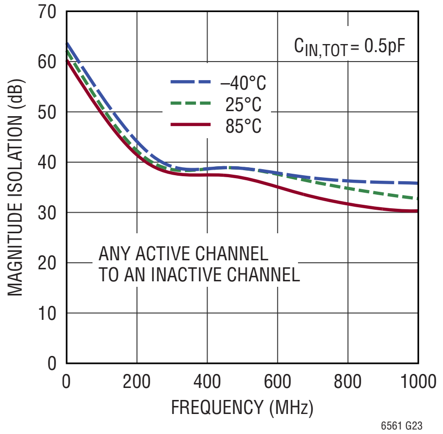
S21(Gain) vs Frequency Over Temperature



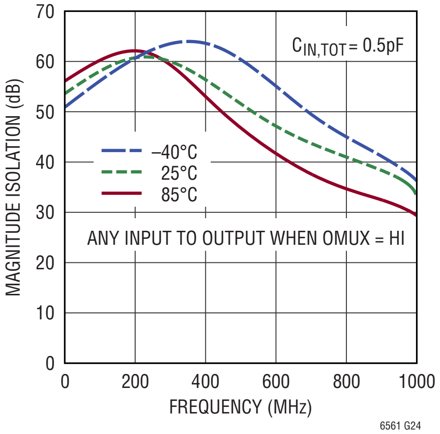
S22 vs Frequency Over Temperature



Stability Factor K vs Frequency Over Temperature



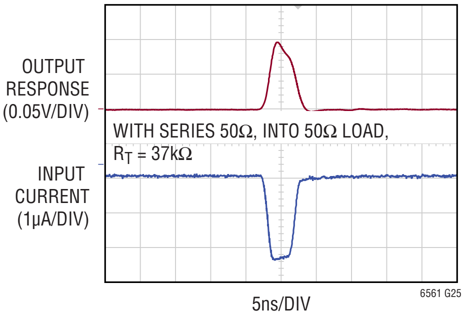
Ch to Ch Isolation vs Frequency Over Temperature



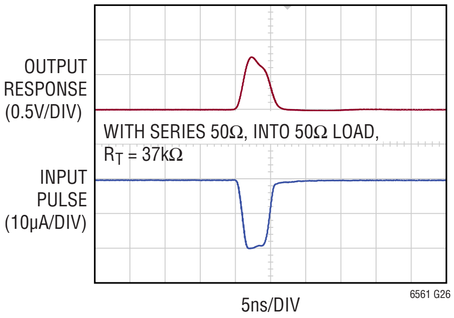
O_MUX Isolation vs Frequency Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

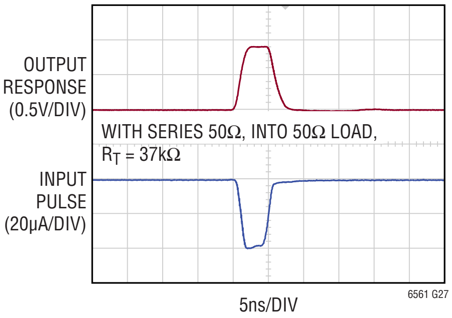
Pulse Response
Linear Range (2.5µA)



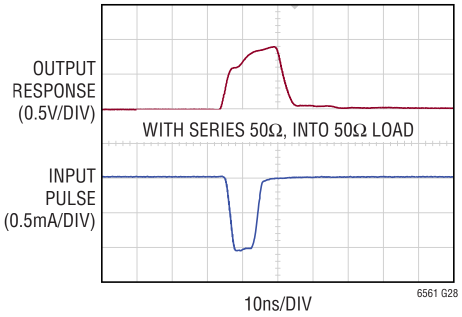
Pulse Response
Linear Range (20µA)



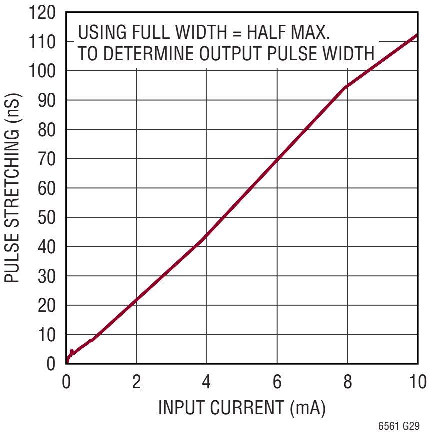
Pulse Response
Overload Region (40µA)



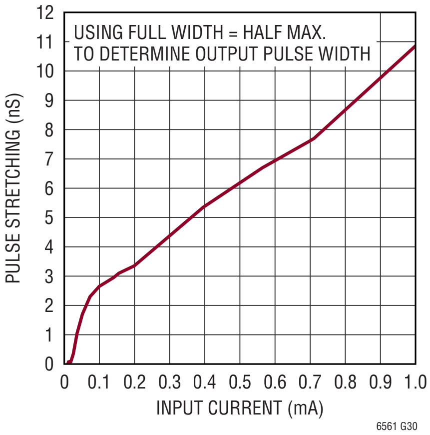
Pulse Response
Overload Region (1mA)



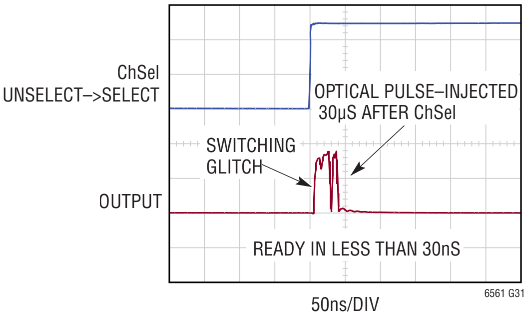
Pulse Stretching
T = 25°C, Using FWHM



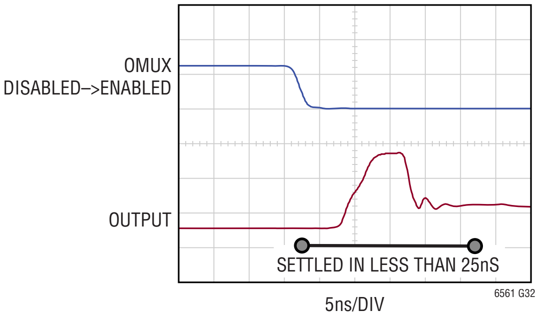
Pulse Stretching Detailed
T = 25°C, Using FWHM



Channel Select
Switching Time



O_MUX Switching Time



PIN FUNCTIONS

V_{CCO} (Pins 1, 18): Positive Power Supply for the Output Stage. Typically 5V. V_{CCO} can be tied to V_{CC1} or V_{CC2} for single supply operation. Between the positive supply and ground, bypass capacitors of 1000pF and 0.1µF should be placed as close to the part as possible. V_{CCO} pins are internally tied together.

CHSEL0 (Pin 2): LSB for Channel Selection. CMOS input. The CHSEL0 pin has a 29kΩ internal pulldown resistor. Default value is 0V.

V_{CC1}, V_{CC2} (Pins 3, 16): Positive Power Supply. Typically 5V. Between the positive supply and ground, bypass capacitors of 1000pF and 0.1µF should be placed as close to the part as possible. V_{CC1} (Pin 3) and V_{CC2} (Pin 16) are internally tied together.

V_{REF1}, V_{REF2}, V_{REF3}, V_{REF4} (Pins 4, 9, 10, 15): Reference Voltage Pin for Transimpedance Amplifier in Channel 1, 2, 3, and 4 Respectively. This pin sets the input DC voltage for each transimpedance amplifier. The V_{REF} pin has a Thevenin equivalent resistance of approximately 1.4k and can be overdriven by an external voltage. If no voltage is applied to V_{REF}, it will float to a default voltage of approximately 1.55V on a 5V supply. Each V_{REF} pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.1µF. The bypass cap should be located close to its V_{REF} pin.

GND (Pins 5, 8, 11, 14, 21, 22, Exposed Pad Pin 25): Negative Power Supply. Normally tied to ground. All GND pins and the exposed pad must be tied to the same voltage. The exposed pad (pin 25) should have multiple via holes to an underlying ground plane for low inductance and good heat transfer.

IN1, IN2, IN3, IN4 (Pin 6, 7, 12, 13): Input Pin for Transimpedance Amplifier for Channels 1, 2, 3, and 4 respectively. This pin is internally biased to 1.55V. See the applications section for specific recommendations.

O_MUX (Pin 17): Output MUX. CMOS Input. This pin is functional when multiple LTC6561s are combined at the output. When O_MUX is low, the output is enabled. When O_MUX is high, all 4 inputs are decoupled from the output. Default value is 0V. This MUX pin is ineffective unless a 2nd LTC6561 is DC-coupled at the output. See Applications section on how to use O_MUX to expand the channel count with multiple LTC6561's. The O_MUX pin has a 29kΩ internal pulldown resistor.

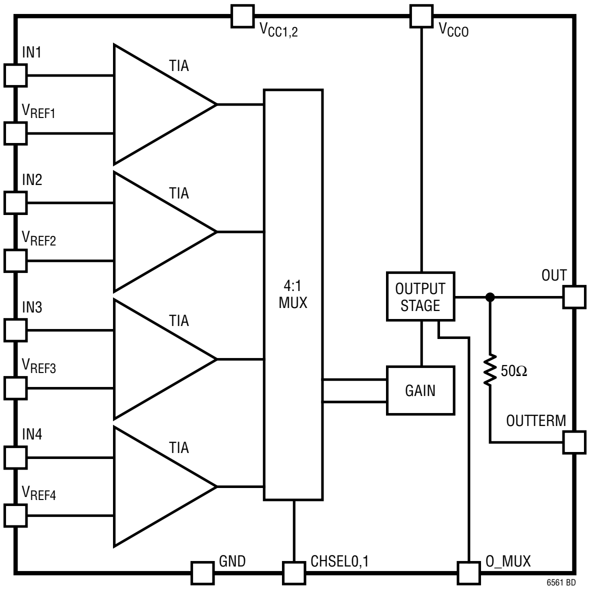
DNC (Pin 19): Do not connect.

OUTTERM (Pin 20): TIA Output with an Internal Series 50Ω Resistor.

OUT (Pin 23): TIA Output without an internal series 50Ω Resistor.

CHSEL1 (Pin 24): MSB for Channel Selection. CMOS input. The CHSEL1 pin has a 29kΩ internal pulldown resistor. Default value is 0V.

BLOCK DIAGRAM



OPERATION

The LTC6561 is a four channel transimpedance amplifier (TIA) with an integrated 4-to-1 multiplexer. Each of the transimpedance amplifiers converts a current to voltage. The integrated multiplexer simplifies the system design while saving space and power. In addition, the Output Multiplexer capability (O_MUX) allows multiple 4-channel LTC6561 devices to be combined. 8, 12, 16 or 32 input channels are easily multiplexed into a single output.

In typical LIDAR applications, the TIA amplifies the output current of an Avalanche Photo Diode. APD's have high optical conversion gain. During operation, the APD is biased near breakdown and under intense optical illumination it can conduct large currents, often in excess of 1A. The LTC6561 survives and quickly recovers from large overload currents. During the recovery time, the TIA is blinded from subsequent pulses. The LTC6561 recovers from 1mA saturation events in less than 15ns without phase reversal, minimizing data loss. As the level of input current increases beyond the linear range, the output pulse width will widen. However, the recovery time remains in the 10's of nS. See Figure 3a. and Figure 4a for plots of pulse stretching versus input current.

Internally the LTC6561 consists of multiple stages. The first stage is a transimpedance amplifier. The second stage is a multiplexer, followed by a third gain stage. A final output buffer can drive a $2V_{P-P}$ swing on a 100Ω load. With a 50Ω load, the output swing will be limited to $1V_{P-P}$

To increase the LIDAR's spatial resolution many APDs are deployed, often in an array. To achieve maximum bandwidth each APD pixel must have a dedicated TIA as increasing Cin will reduce bandwidth. The LTC6561 multiplexing capability allows compact multichannel designs without external multiplexers. The use of multiple LTC6561's works well with an APD array to minimize trace capacitance and solution size.

Channel Selection

CHSEL1	CHSEL0	O_MUX	ACTIVE CHANNEL
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4
X	X	1	High Z

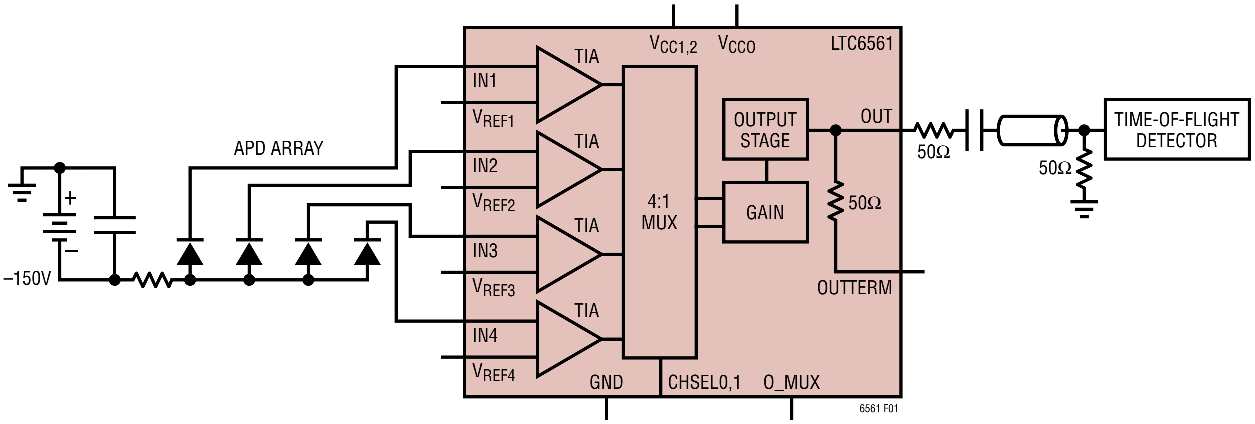


Figure 1. Typical Application with DC-Coupled Inputs Driving a TDC with Back-Terminated Cable

APPLICATIONS INFORMATION

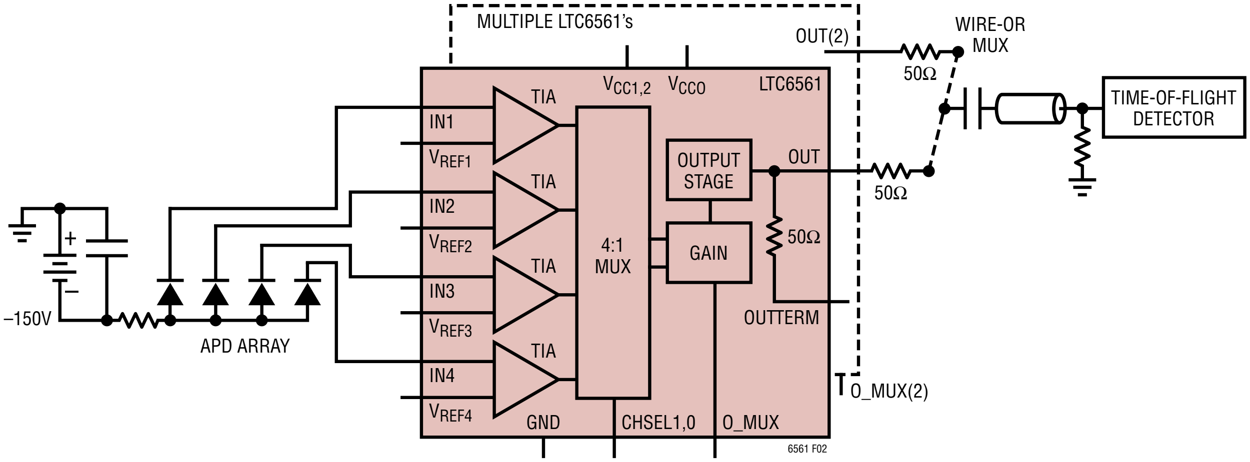


Figure 2. Typical Application with Multiplexed Output

PCB LAYOUT

The LTC6561 has separate supply pins for input ($V_{CC1,2}$) and output (V_{CCO}). V_{CC1} (pin 3) and V_{CC2} (pin 16) are internally tied together. V_{CCO} pins (pin 1 & 18) are internally tied together as well. Duplicate supply pins are provided to ease layout. One set of supply pins should be bypassed with 1000pF and 0.1µF capacitors to ground. For best operation, the output and input supplies should be set to the same voltage.

At each V_{REF} pin the LTC6561 has small internal bypass capacitors connected between pin and ground to ensure low input noise. For the lowest possible input noise, the V_{REF} pin at each TIA should be bypassed with a high quality 0.1µF ceramic capacitor to ground. This bypass cap should be located physically close to each V_{REF} pin and far from input pins to avoid unintentional coupling to the output.

INPUT CONSIDERATIONS AC- OR DC-COUPLING

To maximize dynamic range, the LTC6561's input is limited to negative current pulses (current flowing out of the LTC6561). When using a negatively biased APD, the TIA input can be taken directly off of the cathode. When using a positively biased APD, the input must be AC-coupled off of the APD's cathode. AC-coupling is not recommended as it will increase channel switching time see Channel Selection. Typical Si APDs will offer lower capacitance when negatively biased than when positively biased. On the other hand, DC-coupling will introduce DC currents due to ambient light or dark current which can diminish dynamic range. The user should consider these trade-offs carefully.

OUTPUT CONSIDERATIONS

The LTC6561's output stage is a low impedance driver. When using the OUT pin, a series 47.5Ω resistor must be added to match to 50Ω transmission lines and equipment. If the OUTTERM pin is utilized, the 47.5Ω resistor is internal and not needed externally. Only one of the outputs should be utilized. At the single ended output, the default voltage is approximately 1.0V. Loaded with 100Ω or higher load, the output can swing to 3V. This is equivalent to a $2V_{P-P}$ swing. If loaded with 50Ω only a $1V_{P-P}$ swing is possible since half of the voltage is dropped across the series output resistor. The output must be terminated with a low impedance load <400Ω. If the output is measured directly into a high impedance oscilloscope, the output falling edge will be distorted as the LTC6561 has limited ability to sink current. When monitoring the output, be sure to set the oscilloscope's input termination to 50Ω.

APPLICATIONS INFORMATION

CHANNEL SELECTION

There are four TIA inputs to the LTC6561. The active channel is selected using the two channel selection bits CHSEL0 and CHSEL1. When a channel is selected, its DC input voltage is approximately 1.5V; when deselected its input voltage drops to 1.0V. A reselected channel will not be active until its AC-coupling cap is recharged to 1.5V, leading to slow switching times. With an AC-coupling cap, switching time can stretch into the multiple µS. When DC-coupled, the LTC6561 will switch channels in less than 50nS. Inactive channels have more than 45dB of isolation to the active channel to prevent cross-talk. It is critical to route adjacent channel input lines with ground isolation between them to minimize channel to channel coupling.

OUTPUT MUXing

The Output MUX (O_MUX) requires at least one additional LTC6561 devices to operate in a master/slave relationship. To MUX multiple LTC6561's they need to share a DC connection at their outputs. One LTC6561 output must be selected at all times by asserting its O_MUX pin low. To disable the rest of the outputs, drive the other O_MUX pins high. The chosen LTC6561 effectively commands the others. It is recommended to DC couple the outputs after the series 40-50Ω resistor as this will limit reflection from unselected outputs. At least one LTC6561 output must be selected at all times.

In its default mode O_MUX is low, so the LTC6561 output is enabled. Obviously, if there is only one LTC6561, then setting the O_MUX pin high will not MUX anything, however the output will be isolated from all the inputs.

INPUT CAPACITANCE

As with most TIAs, bandwidth and rise time of the output pulse are a strong function of the input capacitance. To receive narrow pulses, a low capacitance APD sensor is recommended. As well, trace capacitance and parasitic pad capacitance should be minimized at the input. All LTC6561 plots reference $C_{IN,TOT}$ which is the total input capacitance including APD sensor, trace routing and parasitics. The LTC6561's MUX capability allows short input coupling to individual APDs and a more compact solution size for APD arrays.

Internal protection circuitry at each TIA input can protect the LTC6561 even under strong overdrive conditions. Most application circuits will not need external protection diodes which add to the total input capacitance and slow the rise time. Output rise time can be estimated from the amplifier bandwidth using the following relationship:

$$\text{RISETIME} = \frac{0.35}{\text{BW}}$$

APD BIASING

Proper APD biasing is key to producing a high fidelity output and protecting both the APD and TIA. As suggested earlier a negatively biased APD provides the lowest input capacitance and allows the APD to be DC coupled to the TIA. To keep the optical gain stable the APD bias should be temperature compensated. Quenching resistors in series are required to limit the maximum current, thereby protecting the APD and TIA from damage. An example of a typical APD bias network is shown in Figure 5. Starting at the Negative bias input, two physically large 10KW resistors can dissipate the maximum pulse power. They are decoupled with a 1nF capacitor. Moving towards the APD, a second smaller quenching resistor 50Ω is decoupled by two 0.047µF capacitors. This smaller quenching resistor acts to dampen ringing especially under high slew rates due to large optical inputs pulses. All capacitors must be rated for high voltage as APD bias voltages can run above 200V.

Dramatically Improving the LTC6561's Dynamic Range

While the LTC6561's 30µA of linear input range is quite respectable, it is possible to dramatically improve the range over which input current can be accurately measured. The measurement range can be increased from 30µA to at least 3mA, a 100X improvement in current measurement range! As the input current exceeds the linear range, the output pulse amplitude saturates. Once in saturation, the pulse width widens in a predictable manner.

APPLICATIONS INFORMATION

This behavior is demonstrated using the FT2563 evaluation board. This evaluation board uses a series 2k resistor to convert a voltage pulse to a current pulse as it is difficult to obtain a fast current pulse generator. The input is terminated in 50Ω so that current pulses of known quantity are generated at the TIA input using a voltage source. Sweeping the TIA pulse input current from 2.8μA to 3mA, we see that as the current surpasses the 30μA saturation point, the output pulse width increases (Figure 3b).

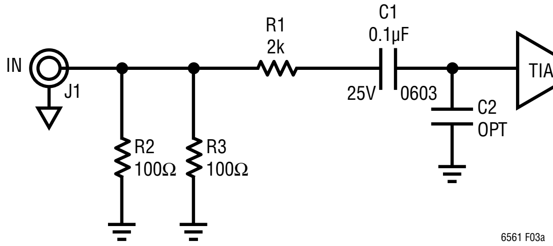


Figure 3a.

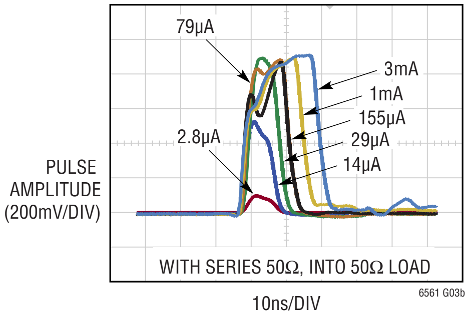


Figure 3b. Output Pulse Over Input Current

When we plot the pulse stretching (Output response width – input pulse width), we see that the stretching is linearly proportional to the input current. Below, the saturation point of 30μA the pulse stretching falls to zero. Here we have used the simple FWHM (Full Width Half Max) criteria to establish the pulse width. The pulse width is taken at half of the maximum swing usually around 0.45V. A more sophisticated algorithm could be used to gain greater accuracy assuming the pulse shape is accurately captured by an ADC. A plot of pulse stretching vs input current is shown in Figure 4a and Figure 4b showing greater detail at low input currents.

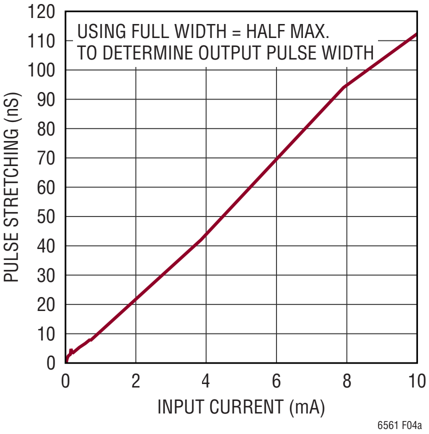


Figure 4a. Pulse Stretching T = 25°C, Using FWHM

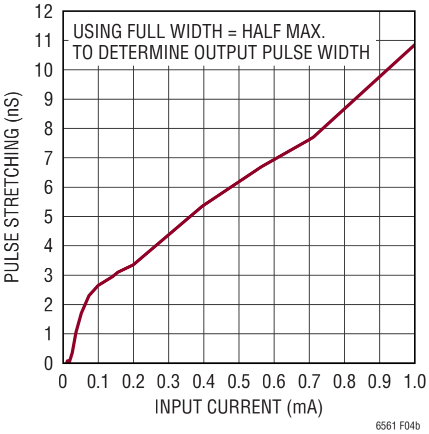


Figure 4b. Pulse Stretching Detailed T = 25°C, Using FWHM

The same pulse stretching has been demonstrated using optical excitation. Independently measuring the current generated during an optical pulse impinging on an APD is quite difficult. The parasitics of any measuring device will impair the actual pulse input (Figure 5). Using a balun across series resistor R48 feeding the APD, we can get an independent determination of APD current to the TIA for moderate laser input powers. Again, when this APD current is plotted versus pulse stretching, we find a nearly linear relationship under moderate illumination

APPLICATIONS INFORMATION

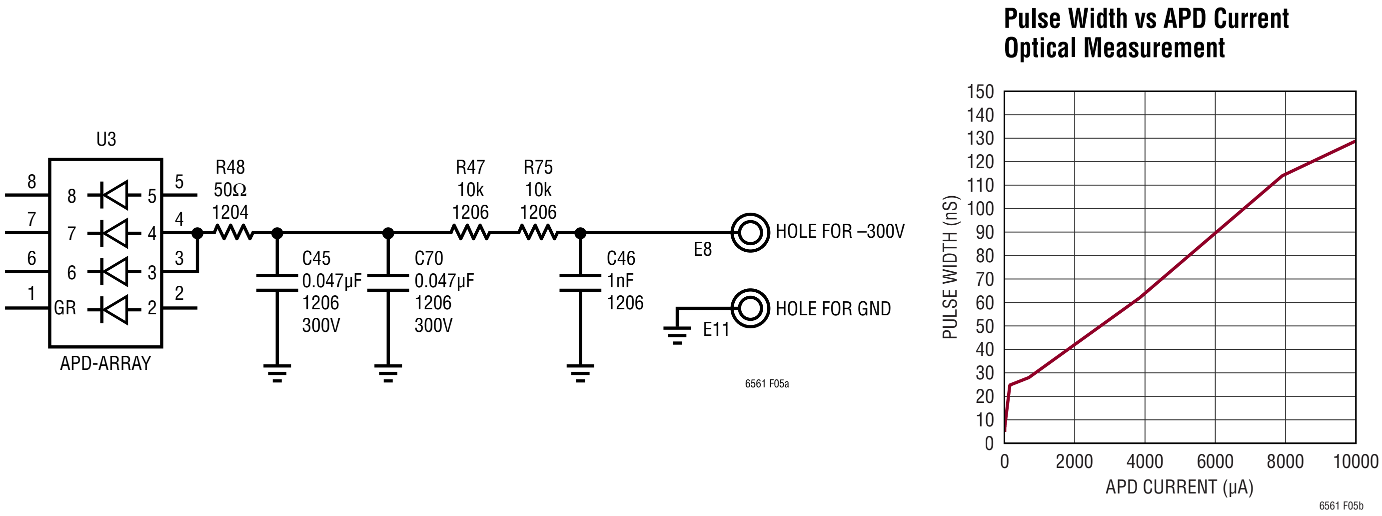


Figure 5. Typical APD Bias Circuit

Using a calibrated laser source we find that pulse stretching continues even at extremely high laser power levels of 50 Watts! At high illumination levels, the relationship no longer appears perfectly linear, but the potential to measure these high power levels is possible. Of course, with any system, a calibration of optical input power to pulse stretching should be done as the optical gain is a strong function of the APD reverse bias, temperature and the choice of APD.

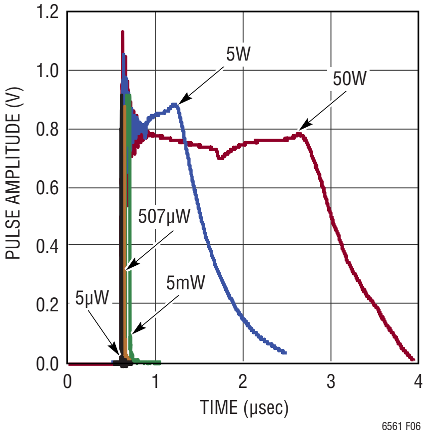
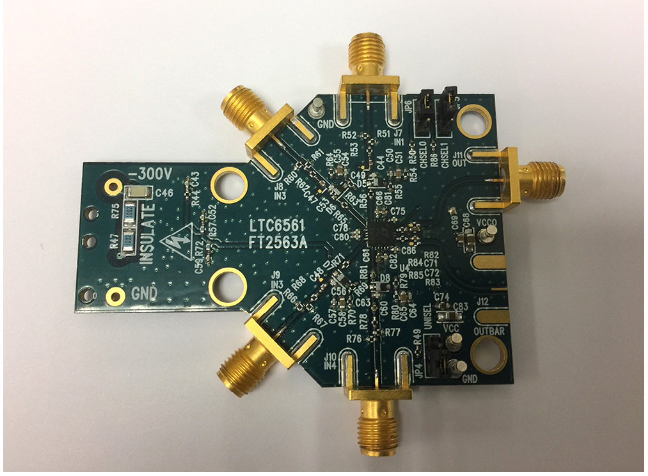
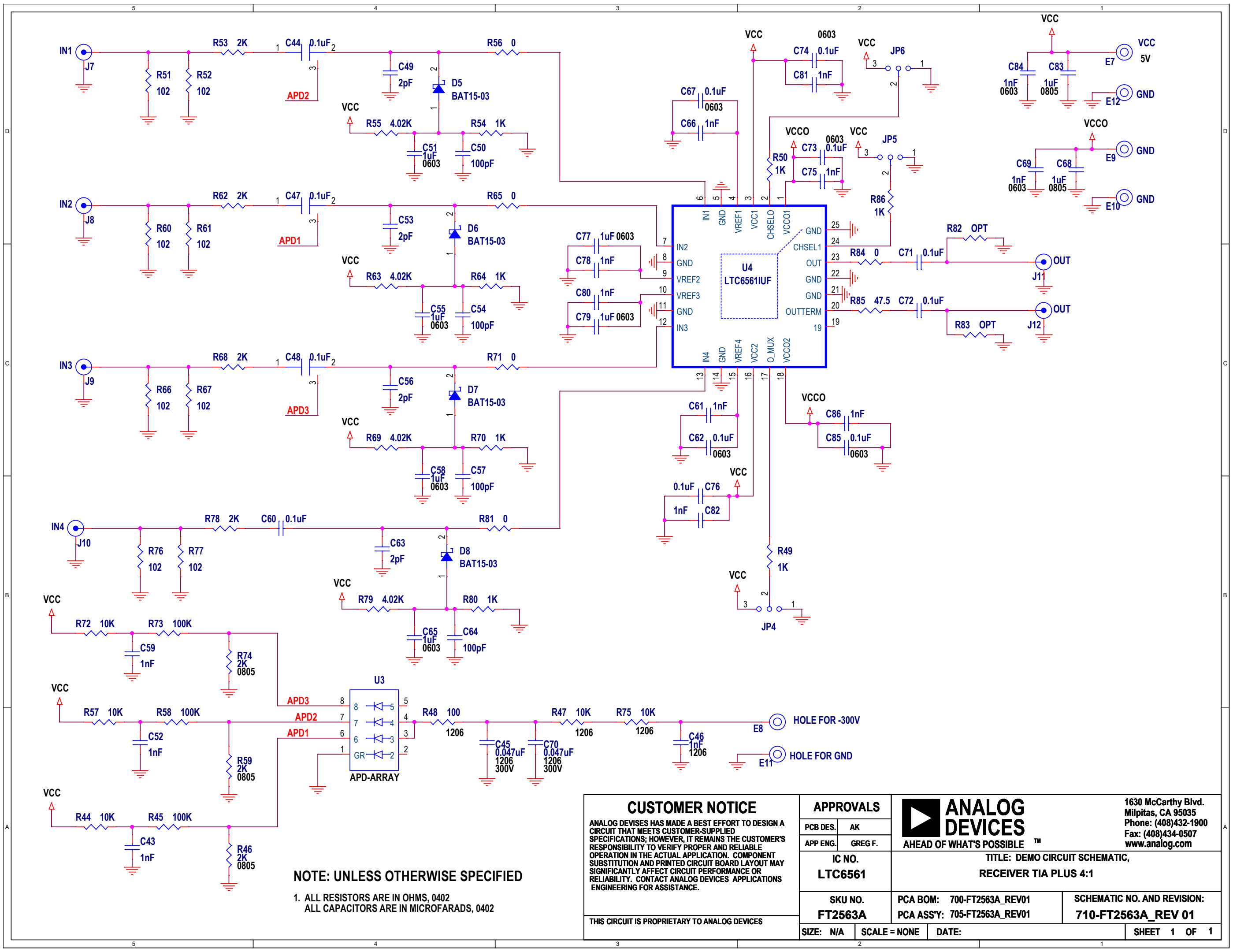


Figure 6. Pulse Width vs Input Hi Power Optical

APPLICATIONS INFORMATION

FT2563A 4-Channel Demonstration Circuit for Optical or Electrical Evaluation





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APPROVALS

PCB DES.	AK
APP ENG.	GREG F.

IC NO. LTC6561

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TITLE: DEMO CIRCUIT SCHEMATIC,
RECEIVER TIA PLUS 4:1

SKU NO. FT2563A

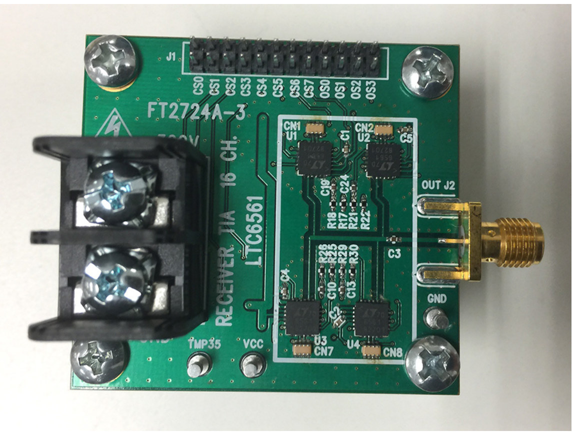
PCA BOM: 700-FT2563A_REV01
PCA ASS'Y: 705-FT2563A_REV01

SCHEMATIC NO. AND REVISION: 710-FT2563A_REV 01

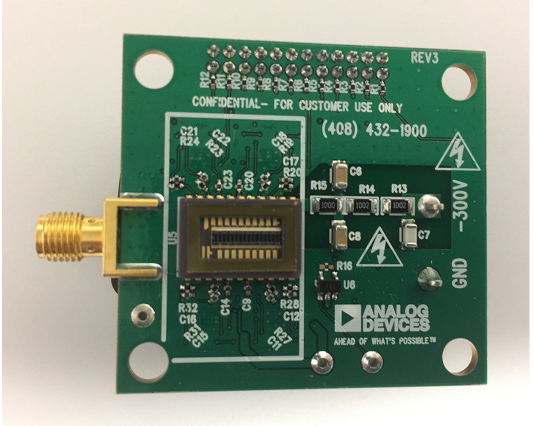
SIZE: N/A SCALE = NONE DATE: SHEET 1 OF 1

APPLICATIONS INFORMATION

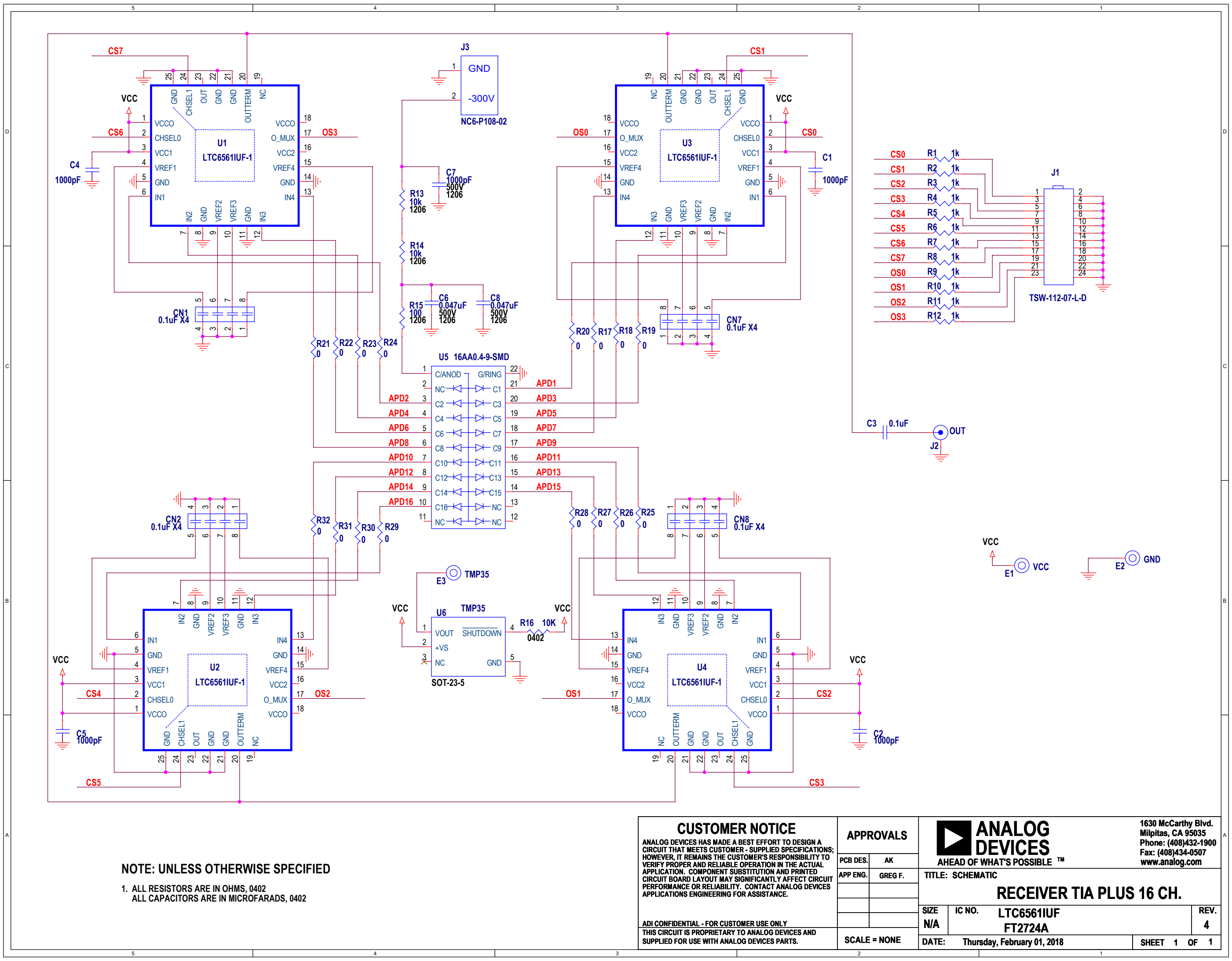
FT2724 16-Channel Demonstration Circuit for Optical Evaluation



FT2724 Front Side



FT2724 Back Side



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APP ENG.	GREG F.

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TITLE: SCHEMATIC

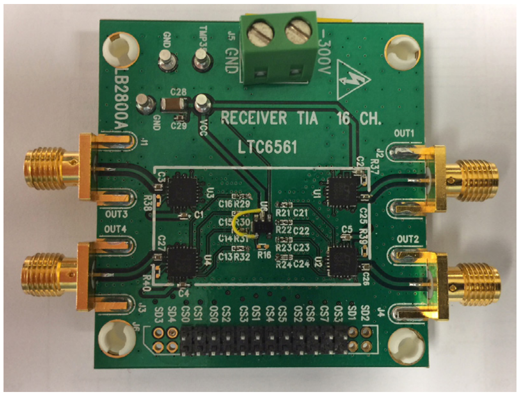
RECEIVER TIA PLUS 16 CH.

SIZE N/A
IC NO. LTC6561IUF
FT2724A
REV. 4

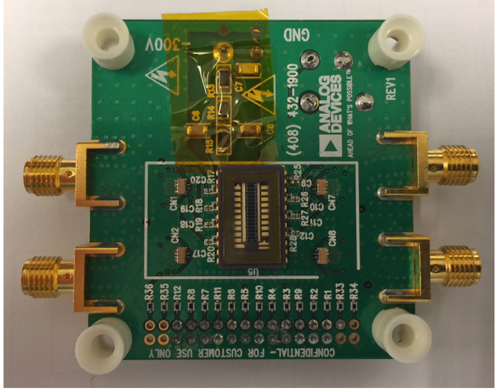
DATE: Thursday, February 01, 2018
SHEET 1 OF 1

APPLICATIONS INFORMATION

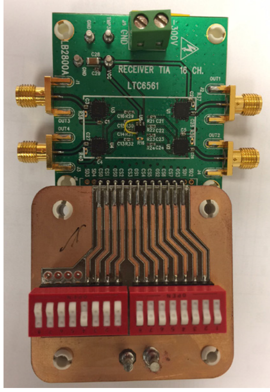
LB2800 16:4 Channel Demonstration Circuit for Optical Evaluation



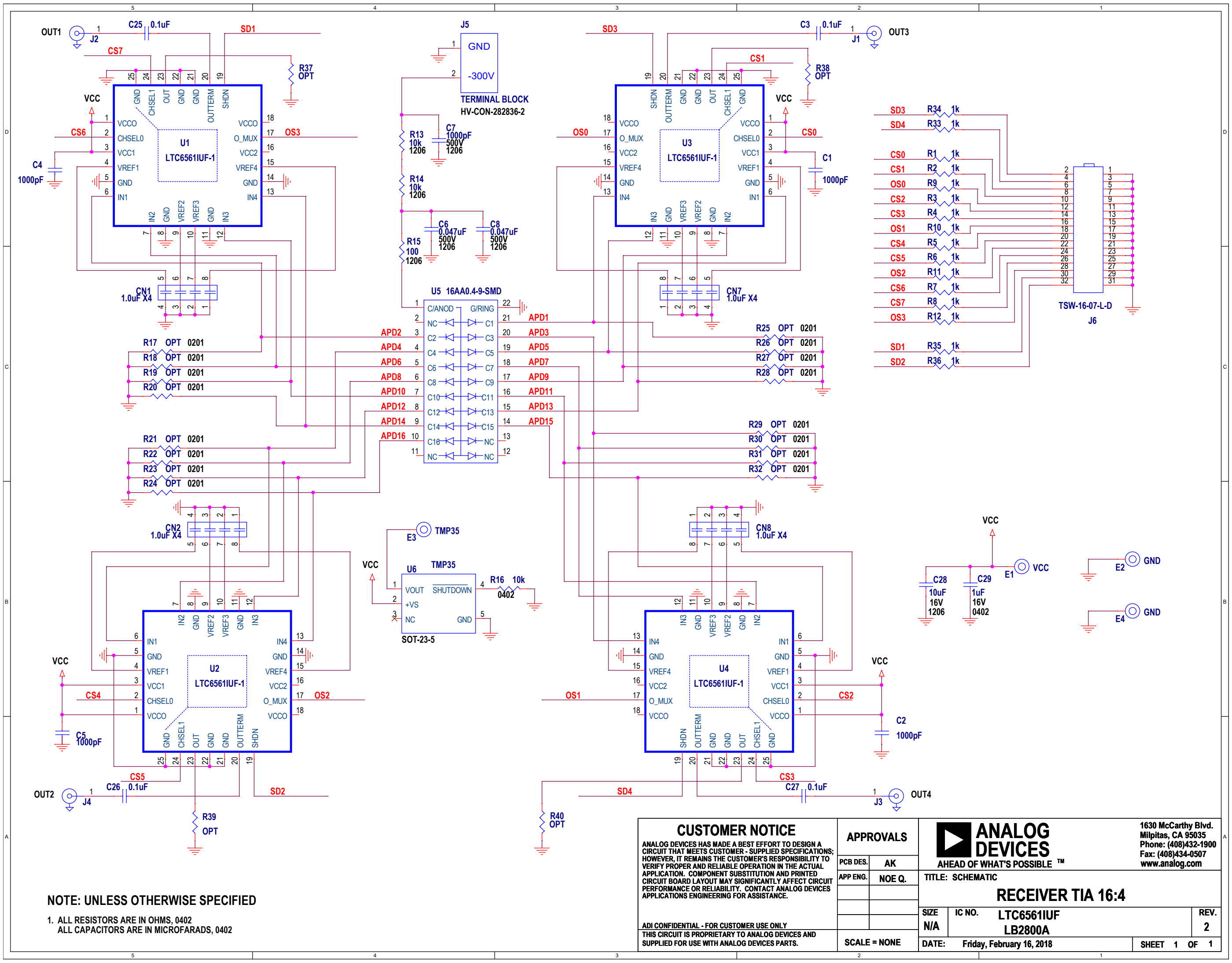
LB2800 Front Side



LB2800 Back Side



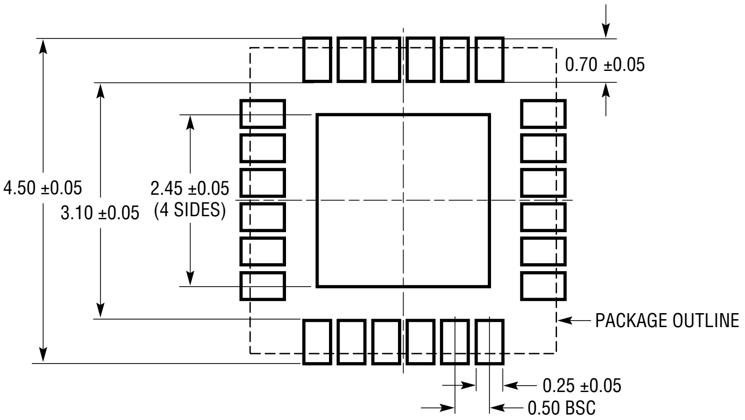
FT2724 with Switch Board



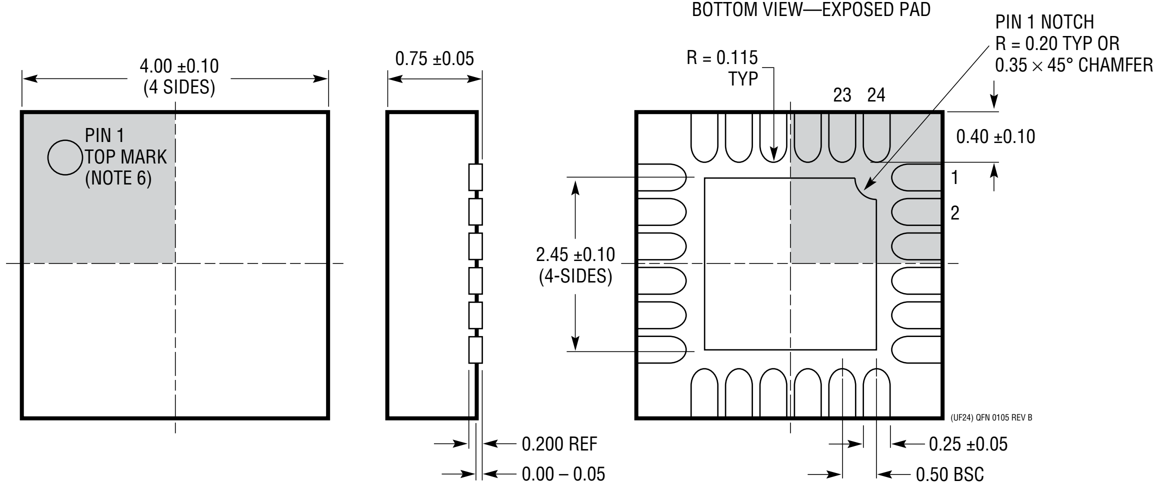
Rev 0

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



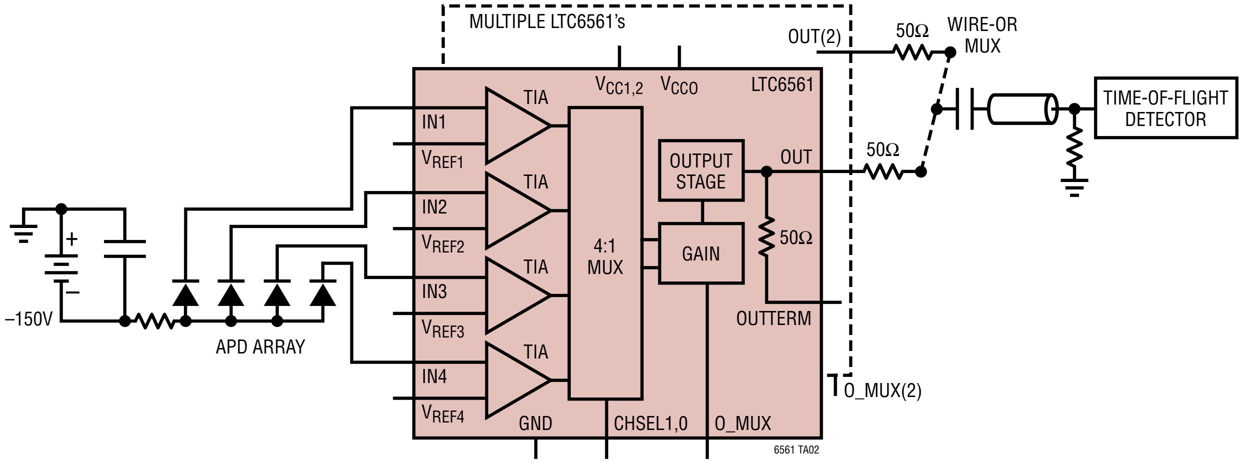
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Typical Application with Multiplexed Output



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6268	500MHz Ultra Low Bias Current FET Input Op Amp	GBW = 500MHz, –3dB BW = 350MHz, Ib = ±3FA
LTC6268-10	4GHz Ultra Low Bias Current FET Input Op Amp	De-Comped Version of the LTC6268, GBW = 4GHz
LTC6244	Dual 50MHz, Low Noise, Rail-to-Rail CMOS Op Amp	GBW = 50MHz, Ib = 1pA
LTC6240/LTC6241/ LTC6242	Single/Dual/Quad 18MHz, Low Noise, Rail-to-Rail Output CMOS Op Amps	GBW = 18MHz, Ib = 0.2pA, 0.1Hz-10Hz, Noise $550nV_{P-P}$
LTC6409	10GHz Bandwidth, 1.1nV/$\sqrt{Hz}$ Differential Amplifier/ADC Driver	GBW = 10GHz, en = 1.1nV/$\sqrt{Hz}$