Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Multicell Battery Stack Monitor

FEATURES

- **Measures Up to 12 Battery Cells in Series**
- **Stackable Architecture**
- **Supports Multiple Battery Chemistries and Supercapacitors**
- **Individually Addressable Serial Interface**
- **0.25% Maximum Total Measurement Error**
- **Engineered for ISO26262 Compliant Systems**
- 13ms to Measure All Cells in a System
- Passive Cell Balancing:
  - Integrated Cell Balancing MOSFETs
  - Ability to Drive External Balancing MOSFETs
- Onboard Temperature Sensor and Thermistor Inputs
- 1MHz Serial Interface with Packet Error Checking
- Safe with Random Connection of Cells
- Built-In Self Tests
- Delta-Sigma Converter With Built-In Noise Filter
- Open-Wire Connection Fault Detection
- 12µA Standby Mode Supply Current
- High EMI Immunity
- 44-Lead SSOP Package

APPLICATIONS

- Electric and Hybrid Electric Vehicles
- High Power Portable Equipment
- Backup Battery Systems
- Electric Bicycles, Motorcycles, Scooters

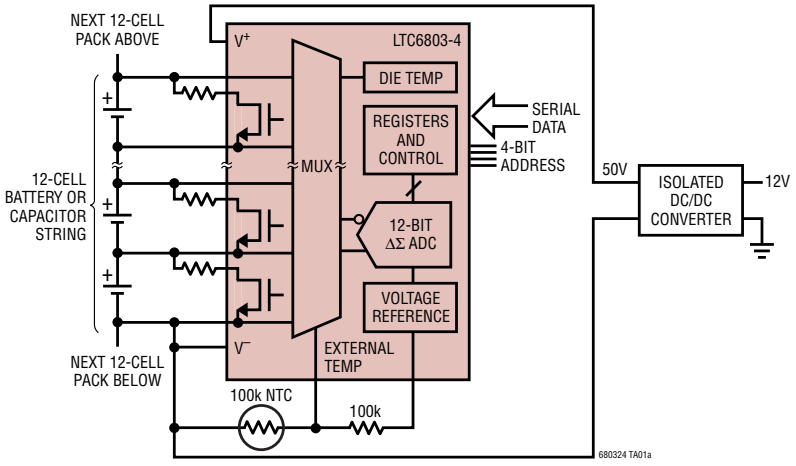
DESCRIPTION

The LTC®6803 is a 2nd generation, complete battery monitoring IC that includes a 12-bit ADC, a precision voltage reference, a high voltage input multiplexer and a serial interface. Each LTC6803 can measure up to 12 series connected battery cells or supercapacitors. Many LTC6803 devices can be stacked to measure the voltage of each cell in a long battery string. Each LTC6803-2/LTC6803-4 has an individually addressable serial interface, allowing up to 16 LTC6803-2/LTC6803-4 devices to interface to one control processor and operate simultaneously. Each cell input has an associated MOSFET switch for discharging overcharged cells. The LTC6803-2 connects the bottom of the stack to V^- internally. It is pin compatible with the LTC6802-2, providing a drop-in upgrade. The LTC6803-4 separates the bottom of the stack from V^-, improving cell 1 measurement accuracy.

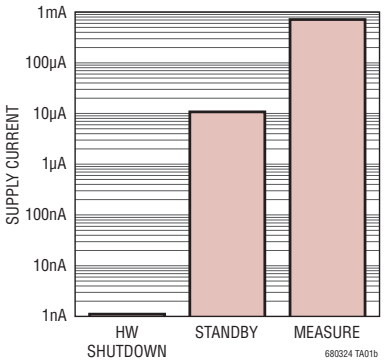
The LTC6803 provides a standby mode to reduce supply current to 12µA. Furthermore, the LTC6803 can be powered from an isolated supply, providing a technique to reduce battery stack current draw to zero.

The related LTC6803-1 and LTC6803-3 offer a serial interface that allows the serial ports of multiple LTC6803-1 or LTC6803-3 devices to be daisy chained without optocouplers or isolators.

TYPICAL APPLICATION



Supply Current vs Modes of Operation



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 75V
Input Voltage (Relative to V^-)
- C0 ..... –0.3V to 8V
- C12 ..... –0.3V to 75V
- C*n* (Note 5) ..... –0.3V to Min (8 • *n*, 75V)
- S*n* (Note 5) ..... –0.3V to Min (8 • *n*, 75V)
- All Other Pins ..... –0.3V to 7V

Voltage Between Inputs
- C*n* to C*n* – 1 ..... –0.3V to 8V
- S*n* to C*n* – 1 ..... –0.3V to 8V
- C12 to C8 ..... –0.3V to 25V
- C8 to C4 ..... –0.3V to 25V
- C4 to C0 ..... –0.3V to 25V

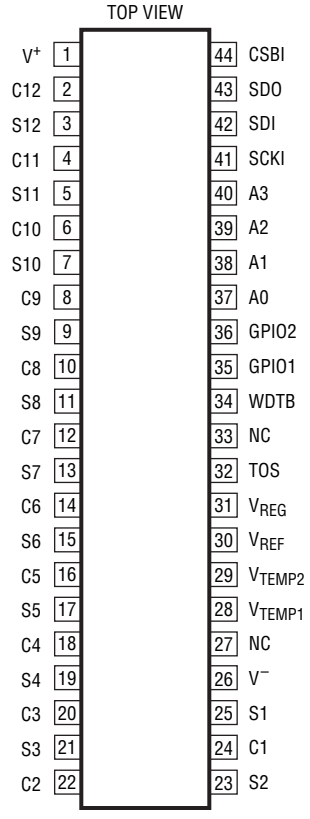
Operating Temperature Range
- LTC6803I ..... –40°C to 85°C
- LTC6803H ..... –40°C to 125°C

Specified Temperature Range
- LTC6803I ..... –40°C to 85°C
- LTC6803H ..... –40°C to 125°C

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Note: *n* = 1 to 12

PIN CONFIGURATION

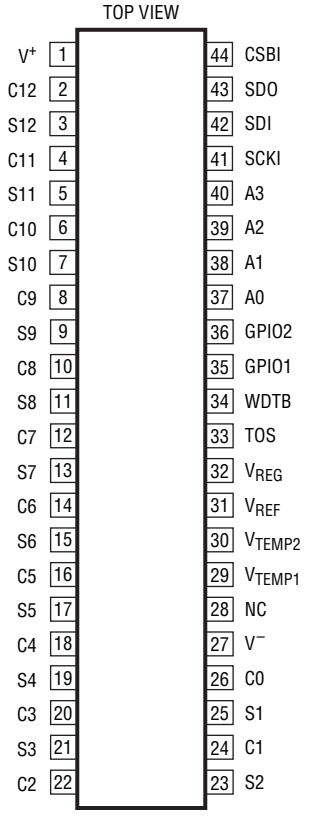
LTC6803-2



G PACKAGE
44-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

LTC6803-4



G PACKAGE
44-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6803IG-2#PBF	LTC6803IG-2#TRPBF	LTC6803G-2	44-Lead Plastic SSOP	–40°C to 85°C
LTC6803IG-4#PBF	LTC6803IG-4#TRPBF	LTC6803G-4	44-Lead Plastic SSOP	–40°C to 85°C
LTC6803HG-2#PBF	LTC6803HG-2#TRPBF	LTC6803G-2	44-Lead Plastic SSOP	–40°C to 125°C
LTC6803HG-4#PBF	LTC6803HG-4#TRPBF	LTC6803G-4	44-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 43.2V, V^- = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Specifications							
V_S	Supply Voltage, V^+ Relative to V^-	V_{ERR} Specification Met Timing Specification Met	● ●	10 4		55 55	V V
V_{LSB}	Measurement Resolution	Quantization of the ADC	●		1.5		mV/Bit
	ADC Offset	(Note 2)	●	–0.5		0.5	mV
	ADC Gain Error	(Note 2)	 ●	–0.12 –0.22		0.12 0.22	% %
V_{ERR}	Total Measurement Error	(Note4) V_{CELL} = –0.3V V_{CELL} = 2.3V V_{CELL} = 2.3V V_{CELL} = 3.6V V_{CELL} = 3.6V, LTC6803IG V_{CELL} = 3.6V, LTC6803HG V_{CELL} = 4.2V V_{CELL} = 4.2V, LTC6803IG V_{CELL} = 4.2V, LTC6803HG V_{CELL} = 5V 2.3V < V_{TEMP} < 4.2V, LTC6803IG 2.3V < V_{TEMP} < 4.2V, LTC6803HG	 ● ● ● ● ● ● ●	 –2.8 –5.1 –4.3 –7.9 –9 –5 –9.2 –10 –9.2 –10	 ±2.5 ±3 	 2.8 5.1 4.3 7.9 9 5 9.2 10 9.2 10	 mV mV mV mV mV mV mV mV mV mV mV mV
V_{CELL}	Cell Voltage Range	Full-Scale Voltage Range		–0.3		5	V
V_{CM}	Common Mode Voltage Range Measured Relative to V^-	Range of Inputs C*n* < 0.25% Gain Error, *n* = 2 to 11, LTC6803IG	●	1.8		5 • *n*	V
		Range of Inputs C0, C1 < 0.25% Gain Error, LTC6803IG	●	0		5	V
		Range of Inputs C*n* < 0.5% Gain Error, *n* = 2 to 11, LTC6803HG	●	1.8		5 • *n*	V
		Range of Inputs C0, C1 < 0.5% Gain Error, LTC6803HG	●	0		5	V
	Die Temperature Measurement Error	Error in Measurement of 125°C			5		°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 43.2V, V^- = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Pin Voltage	R_{LOAD} = 100k to V^-	 ●	3.020 3.015	3.065 3.065	3.110 3.115	V V
	Reference Voltage Temperature Coefficient				8		ppm/°C
	Reference Voltage Thermal Hysteresis	25°C to 85°C and 25°C to –40°C			100		ppm
	Reference Voltage Long-Term Drift				60		ppm/√kHr
V_{REF2}	2nd Reference Voltage		 ●	2.25 2.1	2.5 2.5	2.75 2.9	V V
V_{REG}	Regulator Pin Voltage	10V < V^+ < 50V, No Load I_{LOAD} = 4mA	● ●	4.5 4.5	5.0 5.0	5.5	V V
	Regulator Pin Short-Circuit Limit		●	8			mA
I_B	Input Bias Current	In/Out of Pins C1 Through C12 When Measuring Cell When Not Measuring Cell		 –10	 1	 10	 µA nA
I_S	Supply Current, Measure Mode (Note 7)	Current Into the V^+ Pin When Measuring Continuous Measuring (CDC = 2) Continuous Measuring (CDC = 2) Measure Every 130ms (CDC = 5) Measure Every 500ms (CDC = 6) Measure Every 2 Seconds (CDC = 7)	 ● ● ● ●	 620 600 190 140 55	 780 780 250 175 70	 1000 1150 360 250 105	 µA µA µA µA µA
I_{QS}	Supply Current, Standby	Current Into V^+ Pin When In Standby, All Serial Port Pin at Logic "1" LTC6803IG LTC6803HG	 ● ●	8 6 6	12 12 12	16.5 18 19	µA µA µA
I_{SD}	Supply Current, Hardware Shutdown	Current Out of V^-, V_{C12} = 43.2V, V^+ Floating (Note 8)	●		0.001	1	µA
	Discharge Switch-On Resistance	V_{CELL} > 3V (Note 3)	●	10		20	Ω
I_{OW}	Current Used for Open-Wire Detection		●	70	110	140	µA
	Thermal Shutdown Temperature				145		°C
	Thermal Shutdown Hysteresis				5		°C
Voltage Mode Timing Specifications							
t_{CYCLE}	Measurement Cycling	Time Required to Measure 12 Cells Time Required to Measure 10 Cells Time Required to Measure 3 Temperatures Time Required to Measure 1 Cell or Temperature	● ● ● ●	11 9 2.8 1.0	13 11 3.4 1.2	15 13 4.1 1.4	ms ms ms ms
t_1	SDI Valid to SCKI Rising Setup		●	10			ns
t_2	SDI Valid to SCKI Rising Hold		●	250			ns
t_3	SCKI Low		●	400			ns
t_4	SCKI High		●	400			ns
t_5	CSBI Pulse Width		●	400			ns
t_6	CSBI Falling to SCKI Rising		●	100			ns
t_7	CSBI Falling to SDO Valid		●	100			ns
t_8	SCKI Falling to SDO Valid		●			250	ns
	Clock Frequency		●			1	MHz
	Watchdog Timer Timeout Period		●	1		2.5	Seconds

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 43.2V, V^- = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Mode Digital I/O							
V_{IH}	Digital Input Voltage High	Pins SCKI, SDI and CSBI	●	2			V
V_{IL}	Digital Input Voltage Low	Pins SCKI, SDI and CSBI	●			0.8	V
V_{OL}	Digital Output Voltage Low	Pin SDO, Sinking 500µA	●			0.3	V
I_{IN}	Digital Input Current	V_{MODE}, TOS, SCKI, SDI, CSBI	●			10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error (V_{ERR}) specification.

Note 3: Due to the contact resistance of the production tester, this specification is tested to relaxed limits. The 20Ω limit is guaranteed by design.

Note 4: V_{CELL} refers to the voltage applied across C*n* to C*n* – 1 for *n* = 1 to 12. V_{TEMP} refers to the voltage applied from V_{TEMP1} or V_{TEMP2} to V^-.

Note 5: These absolute maximum ratings apply provided that the voltage between inputs do not exceed the absolute maximum ratings.

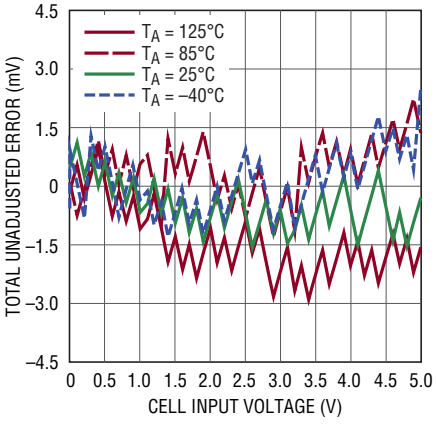
Note 6: Supply current is tested during continuous measuring. The supply current during periodic measuring (130ms, 500ms, 2s) is guaranteed by design.

Note 7: The CDC = 5, 6 and 7 supply currents are not measured. They are guaranteed by the CDC = 2 supply current measurement.

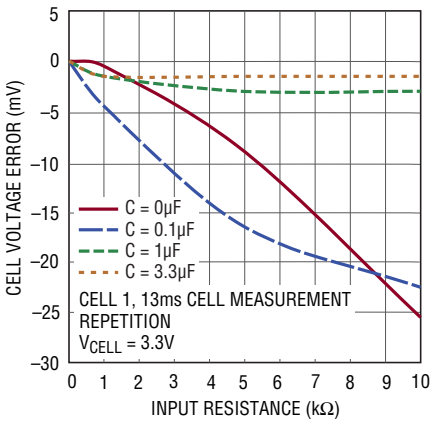
Note 8: Limit is determined by high speed automated test capability.

TYPICAL PERFORMANCE CHARACTERISTICS

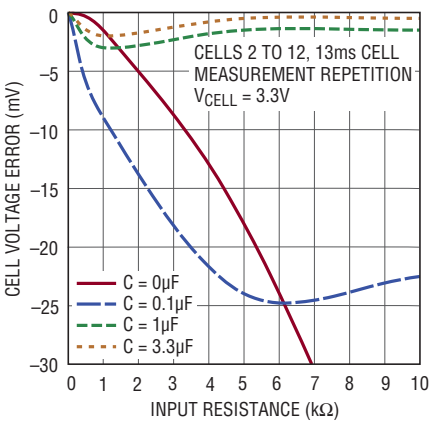
Cell Measurement Error vs Cell Input Voltage



Cell Measurement Error vs Input RC Values

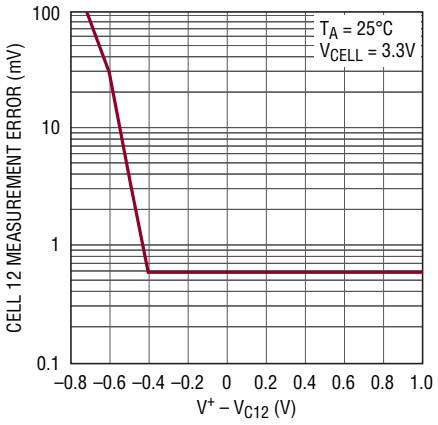


Cell Measurement Error vs Input RC Values



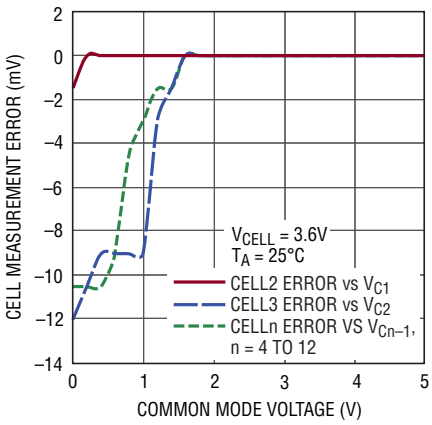
TYPICAL PERFORMANCE CHARACTERISTICS

Cell 12 Measurement Error vs V+



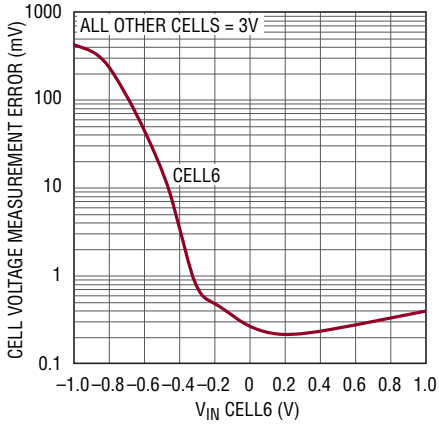
680324 G04

Cell Voltage Measurement Error vs Common Mode Voltage



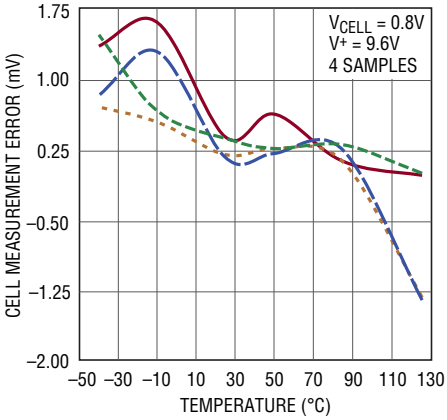
680324 G05

Cell Measurement Error vs Cell Voltage



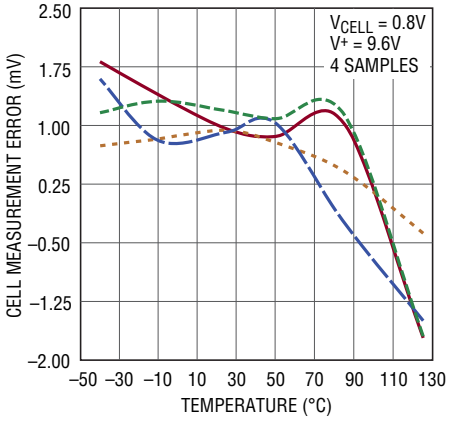
680324 G06

Cell 1 Voltage Measurement Error vs Temperature



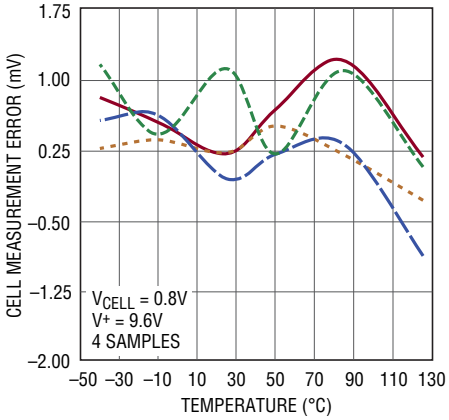
680324 G07

Cell 2 Voltage Measurement Error vs Temperature



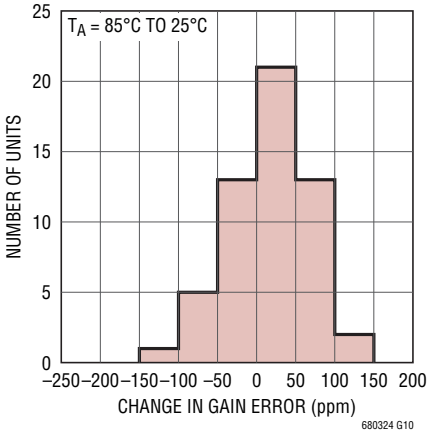
680324 G08

Cell 3 to Cell 12 Voltage Measurement Error vs Temperature



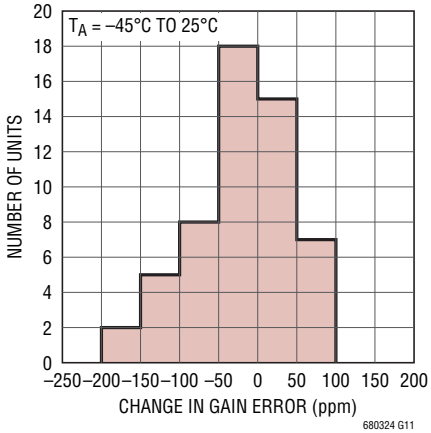
680324 G09

Measurement Gain Error Hysteresis



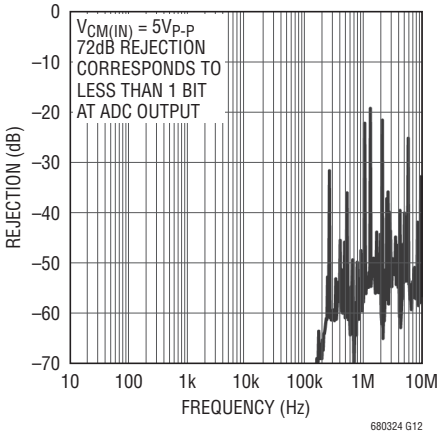
680324 G10

Measurement Gain Error Hysteresis



680324 G11

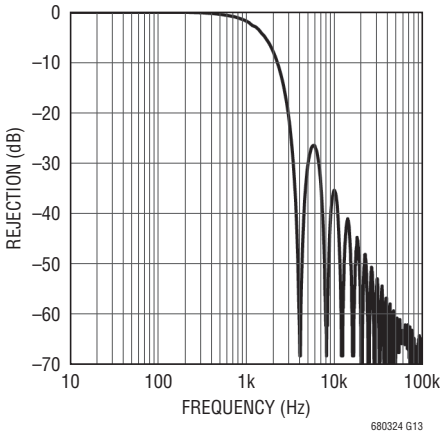
Cell Measurement Common Mode Rejection



680324 G12

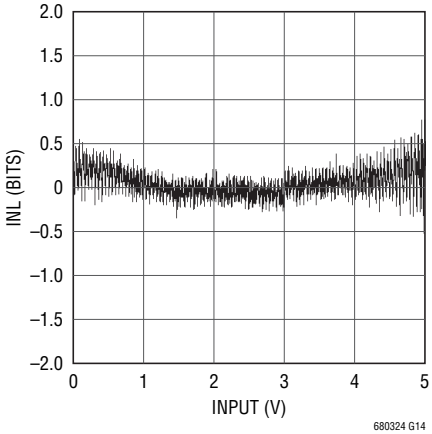
TYPICAL PERFORMANCE CHARACTERISTICS

ADC Normal Mode Rejection vs Frequency



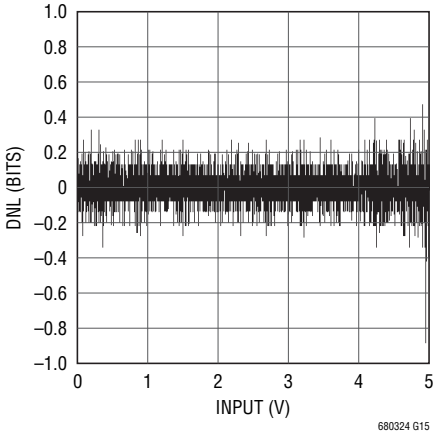
680324 G13

ADC INL



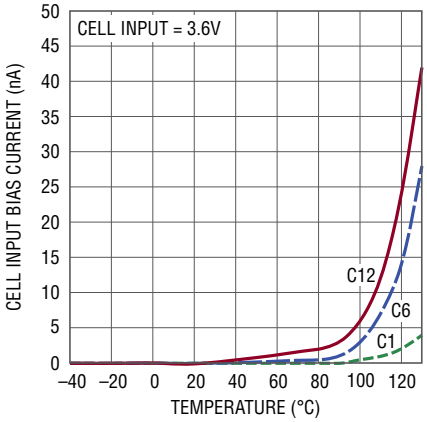
680324 G14

ADC DNL



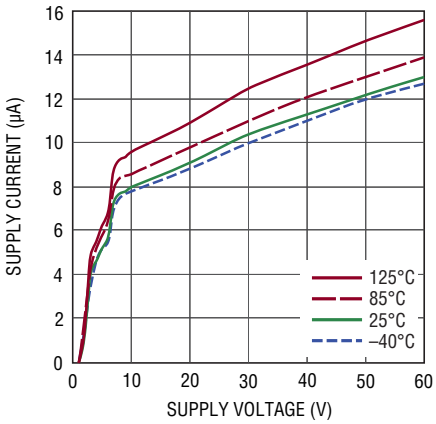
680324 G15

Cell Input Bias Current During Standby and Hardware Shutdown



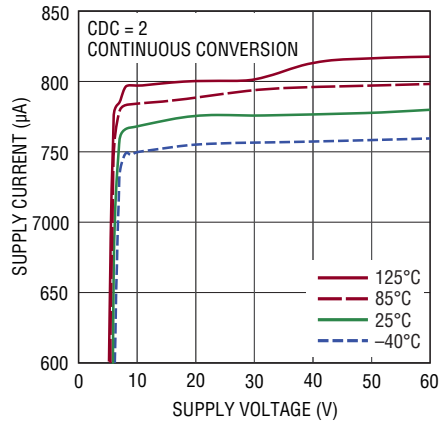
680324 G16

Standby Supply Current vs Supply Voltage



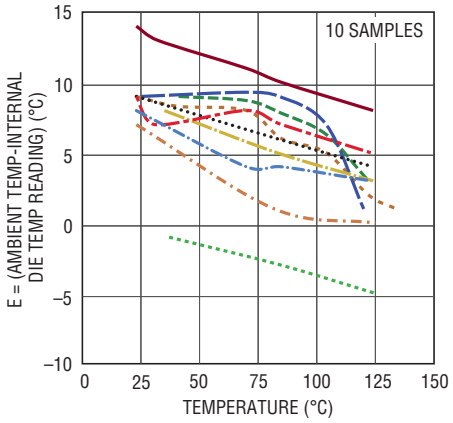
680324 G17

Supply Current vs Supply Voltage During Continuous Conversions



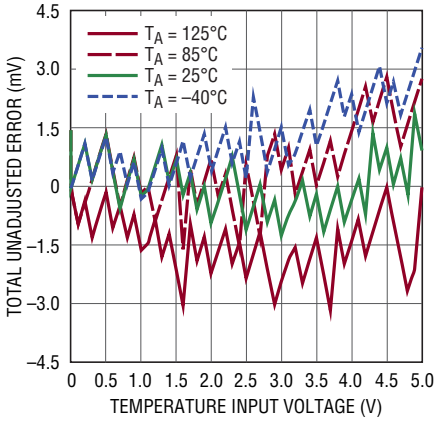
680324 G18

Internal Die Temperature Measurement Error Using an 8mV/°K Scale Factor



680324 G19

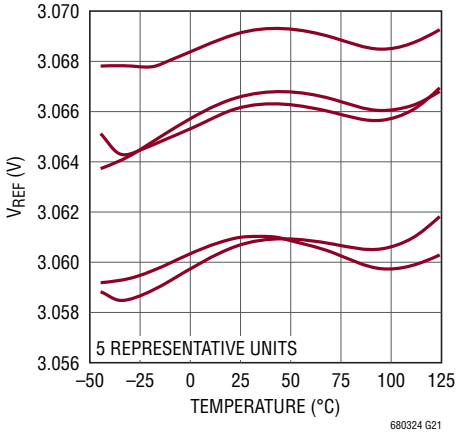
External Temperature Measurement Total Unadjusted Error vs Input



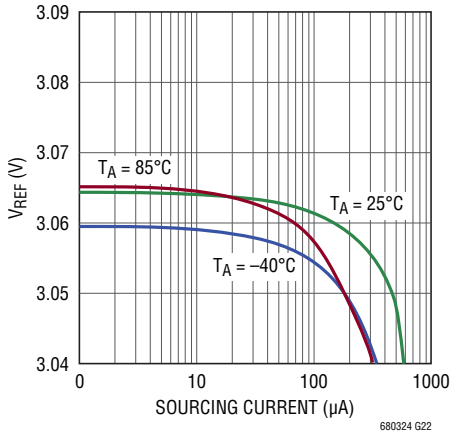
680324 G20

TYPICAL PERFORMANCE CHARACTERISTICS

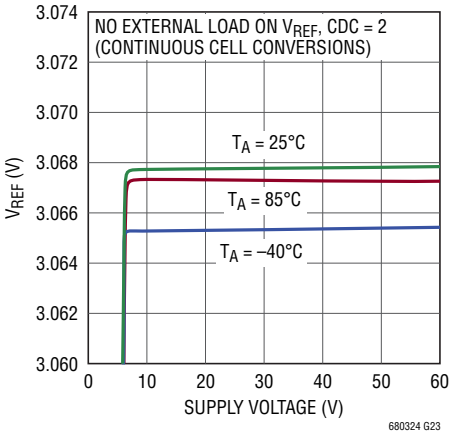
V_{REF} Output Voltage vs Temperature



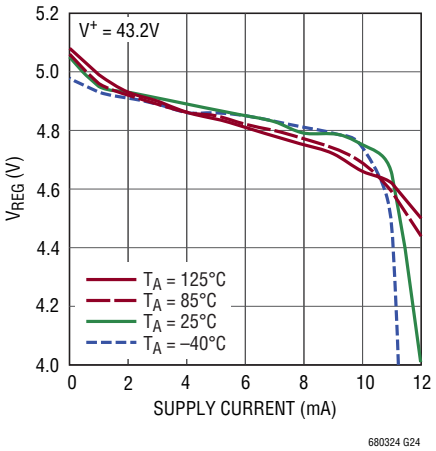
V_{REF} Load Regulation



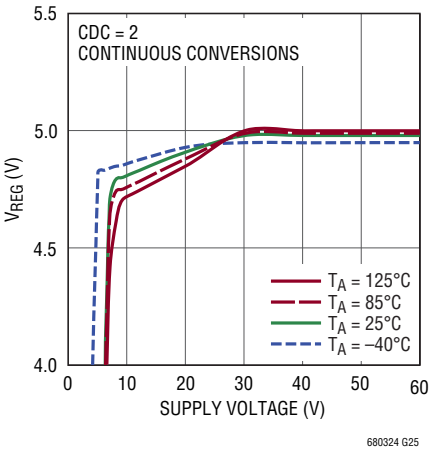
V_{REF} Line Regulation



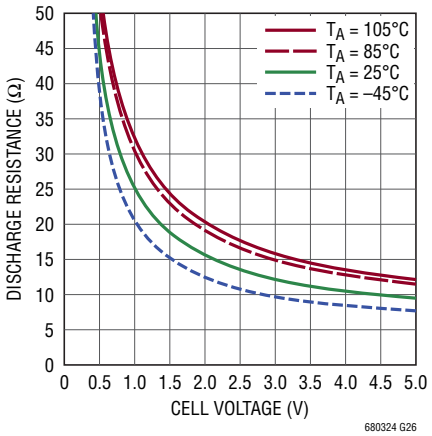
V_{REG} Load Regulation



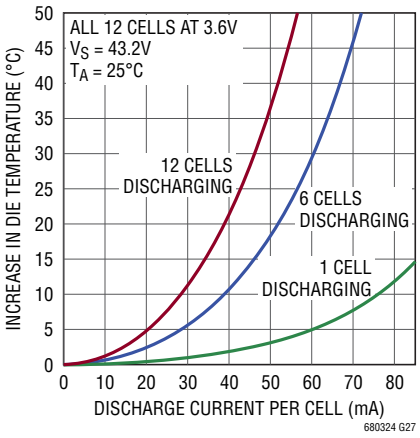
V_{REG} Line Regulation



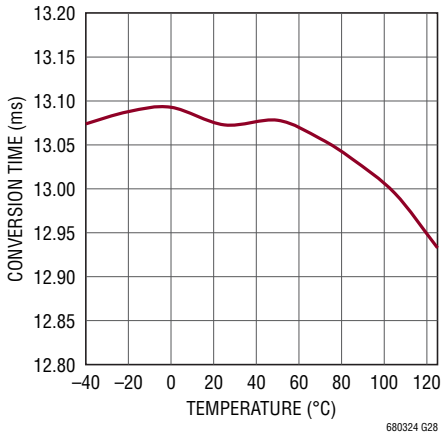
Internal Discharge Resistance vs Cell Voltage



Die Temperature Increase vs Discharge Current in Internal FET



Cell Conversion Time



PIN FUNCTIONS

To ensure pin compatibility with LTC6802-2, the LTC6803-2 is configured such that the bottom cell input (C0) is connected internally to the negative supply voltage (V^-). The LTC6803-4 offers a unique pinout with an input for the bottom cell (C0). This simple functional difference offers the possibility for enhanced cell 1 measurement accuracy, enhanced SPI noise tolerance and simplified wiring. More information is provided in the Applications Information section entitled Advantages of Kelvin Connection for C0.

V^+ (Pin 1): Positive Power Supply. Pin 1 can be tied to the most positive potential in the battery stack or an isolated power supply. V^+ must be greater than the most positive potential in the battery stack under normal operation. With an isolated power supply, LTC6803 can be turned off by simply shutting down V^+.

C12, C11, C10, C9, C8, C7, C6, C5, C4, C3, C2, C1 (Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24): C1 through C12 are the inputs for monitoring battery cell voltages. The negative terminal of the bottom cell should be tied to the V^- pin for the LTC6803-2, and the C0 pin for the LTC6803-4. The next lowest potential is tied to C1 and so forth. See the figures in the Applications Information section for more details on connecting batteries to the LTC6803-2 and LTC6803-4. The LTC6803 can monitor a series connection of up to 12 cells. Each cell in a series connection must have a common mode voltage that is greater than or equal to the cells below it. 100mV negative voltages are permitted.

C0 (Pin 26 on LTC6803-4): Negative Terminal of the Bottom Battery Cell. C0 and V^- form a Kelvin connection to eliminate effect of voltage drop at the V^- trace.

S12, S11, S10, S9, S8, S7, S6, S5, S4, S3, S2, S1 (Pins 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25): S1 though S12 pins are used to balance battery cells. If one cell in a series becomes overcharged, an S output can be used to discharge the cell. Each S output has an internal N-channel MOSFET for discharging. See the Block Diagram. The NMOS has a maximum on-resistance of 20Ω. An external resistor should be connected in series with the NMOS to dissipate heat outside of the LTC6803 package. When using the internal MOSFETs to discharge cells, the die temperature should be monitored. See Power Dissipation and Thermal Shutdown in the Applications Information section. The S pins also feature an internal pull-up PMOS. This allows the S pins to be used to drive the gates of external MOSFETs for higher discharge capability.

V^- (Pin 26 on LTC6803-2/Pin 27 on LTC6803-4): Connect V^- to the most negative potential in the series of cells.

NC (Pin 27 on LTC6803-2/Pin 28 on LTC6803-4): This pin is not used and is internally connected to V^- through 10Ω. It can be left unconnected or connected to V^- on the PCB.

V_{TEMP1}, V_{TEMP2} (Pins 28, 29 on LTC6803-2/Pins 29, 30, on LTC6803-4): Temperature Sensor Inputs. The ADC will measure the voltage on V_{TEMPn} with respect to V^- and store the result in the TMP register. The ADC measurements are relative to the V_{REF} pin voltage. Therefore a simple thermistor and resistor combination connected to the V_{REF} pin can be used to monitor temperature. The V_{TEMP} inputs can also be general purpose ADC inputs.

V_{REF} (Pin 30 on LTC6803-2/Pin 31 on LTC6803-4): 3.065V Voltage Reference Output. This pin should be bypassed with a 1µF capacitor. The V_{REF} pin can drive a 100k resistive load connected to V^-. Larger loads should be buffered with an LT6003 op amp, or a similar device.

V_{REG} (Pin 31 on LTC6803-2/Pin 32 on LTC6803-4): Linear Voltage Regulator Output. This pin should be bypassed with a 1µF capacitor. The V_{REG} is capable of sourcing up to 4mA to an external load. The V_{REG} pin does not sink current.

TOS (Pin 32 on LTC6803-2/Pin 33 on LTC6803-4): Top of Stack Input. The TOS pin can be tied to V_{REG} or V^- for the LTC6803. The state of the TOS pin alters the operation of the SDO pin in the toggle polling mode. See the Serial Port description.

NC (Pin 33 on LTC6803-2): No Connection.

PIN FUNCTIONS

WDTB (Pin 34): Watchdog Timer Output (Active Low). If there is no valid command received in 1 to 2.5 seconds, the WDTB output is asserted. The WDTB pin is an open-drain NMOS output. When asserted it pulls the output down to V^- and resets the configuration register to its default state.

GPIO1, GPIO2 (Pins 35, 36): General Purpose Input/Output. By writing a "0" to a GPIO configuration register bit, the open-drain output is activated and the pin is pulled to V^-. By writing a logic "1" to the configuration register bit, the corresponding GPIO pin is high impedance. An external resistor is required to pull the pin up to V_{REG}. By reading the configuration register locations GPIO1 and GPIO2, the state of the pins can be determined. For example, if a "0" is written to register bit GPIO1, a "0" is always read back because the output N-channel MOSFET pulls Pin 35 to V^-. If a "1" is written to register bit GPIO1, the pin becomes high impedance. Either a "1" or a "0" is read back, depending on the voltage present at Pin 35. The GPIOs makes it possible to turn-on/off circuitry around the LTC6803-4, or read logic values from a circuit around the LTC6803-4. The GPIO pins should be connected to V^- if not used.

A0, A1, A2, A3 (Pins 37, 38, 39, 40): Address Inputs. These pins are tied to V_{REG} or V^-. The state of the address pins (V_{REG} = 1, V^- = 0) determines the LTC6803 address. See Address Commands in the Serial Port subsection of the Applications Information section.

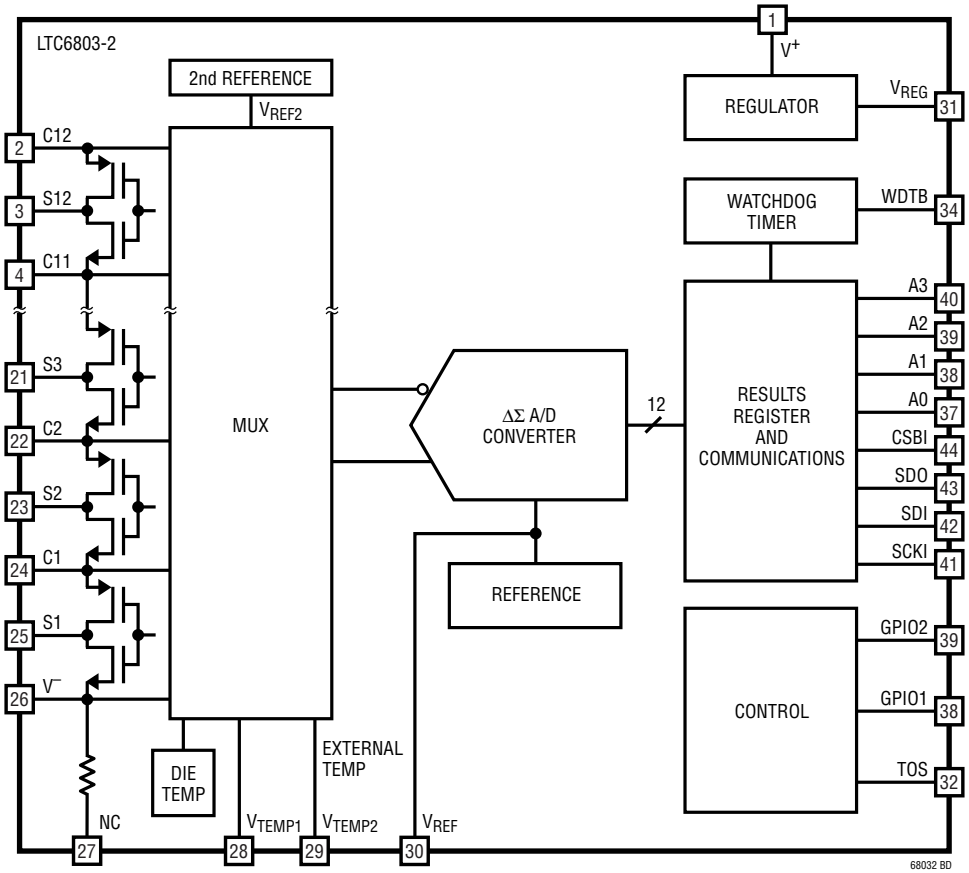
SCKI (Pin 41): Serial Clock Input. The SCKI pin interfaces to any logic gate (TTL levels). See Serial Port in the Applications Information section.

SDI (Pin 42): Serial Data Input. The SDI pin interfaces to any logic gate (TTL levels). See Serial Port in the Applications Information section.

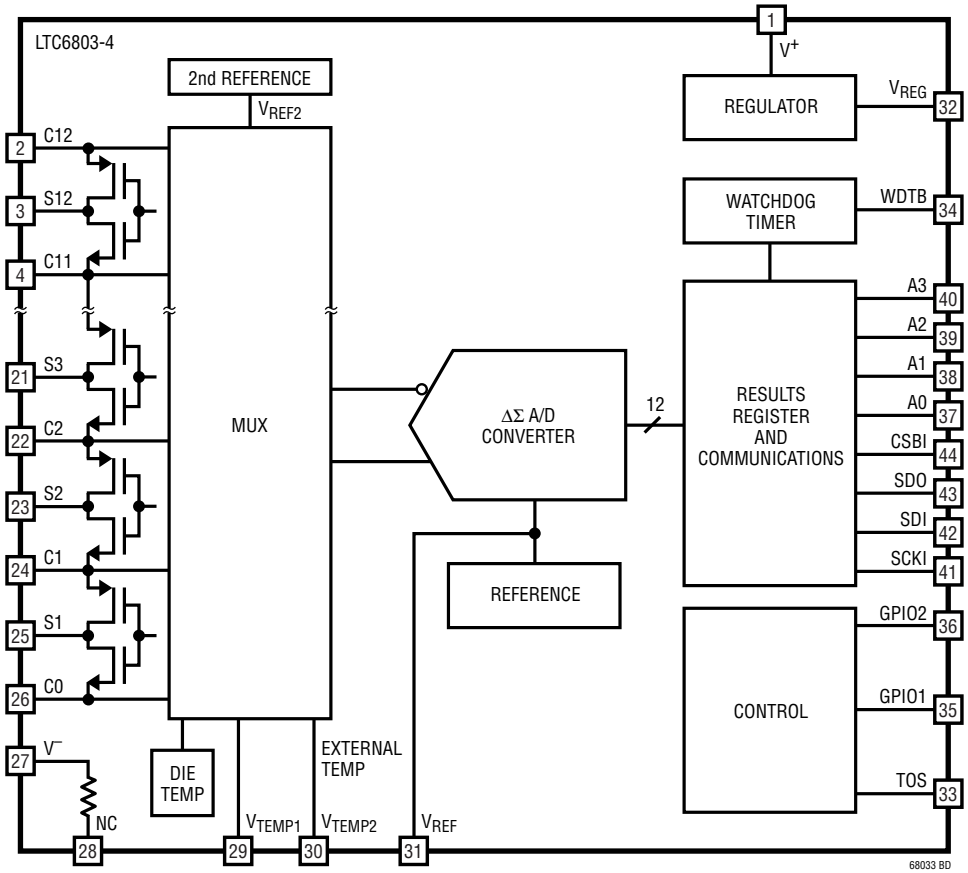
SDO (Pin 43): Serial Data Output. The SDO pin is an NMOS open-drain output. A pull-up resistor is needed on SDO. See Serial Port in the Applications Information section.

CSBI (Pin 44): Chip Select (Active Low) Input. The CSBI pin interfaces to any logic gate (TTL levels). See Serial Port in the Applications Information section.

BLOCK DIAGRAMS

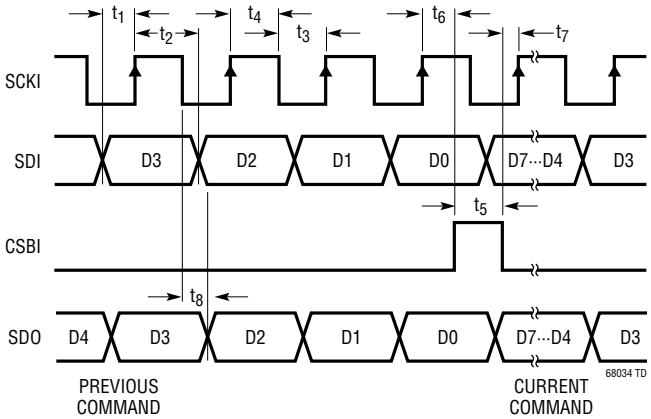


BLOCK DIAGRAMS



TIMING DIAGRAM

Timing Diagram of the Serial Interface



OPERATION

THEORY OF OPERATION

The LTC6803 is a data acquisition IC capable of measuring the voltage of 12 series connected battery cells. An input multiplexer connects the batteries to a 12-bit delta-sigma analog-to-digital converter (ADC). An internal 8ppm/°C voltage reference combined with the ADC give the LTC6803 its outstanding measurement accuracy. The inherent benefits of the delta-sigma ADC versus other types of ADCs (e.g., successive approximation) are explained in Advantages of Delta-Sigma ADCs in the Applications Information section.

Communication between the LTC6803 and a host processor is handled by a SPI compatible serial interface. Multiple LTC6803s can be connected to a single serial interface. As shown in Figure 1, the LTC6803-2s or LTC6803-4s are isolated from one another using digital isolators. A unique addressing scheme allows all the LTC6803-2s or LTC6803-4s to connect to the same serial port of the host processor. Further explanation of the LTC6803-2/LTC6803-4 can be found in the Serial Port section of the data sheet.

The LTC6803 also contains circuitry to balance cell voltages. Internal MOSFETs can be used to discharge cells. These internal MOSFETs can also be used to control external balancing circuits. Figure 1 illustrates cell balancing by internal discharge. Figure 3 shows the S pin controlling an external balancing circuit. It is important to note that the LTC6803 makes no decisions about turning on/off the internal MOSFETs. This is completely controlled by the host processor. The host processor writes values to a configuration register inside the LTC6803 to control the switches. The watchdog timer on the LTC6803 can be used to turn off the discharge switches if communication with the host processor is interrupted.

Since the LTC6803-4 separates C0 and V^-, C0 can have higher potential than V^-. This feature is very useful for super capacitors and fuel cells whose voltages can go to zero or slightly negative. In such a case, the stacked cells can't power the LTC6803-4. In Figure 1, an isolated 36V and –3.6V provides power to each LTC6803-4. This allows the C1 to C12 pins to go up to 3.6V below C0.

The LTC6803 has three modes of operation: hardware shutdown, standby and measure. Hardware shutdown is a true zero power mode. Standby mode is a power saving state where all circuits except the serial interface are turned off. In measure mode, the LTC6803 is used to measure cell voltages and store the results in memory. Measure mode will also monitor each cell voltage for overvoltage (OV) and undervoltage (UV) conditions.

HARDWARE SHUTDOWN MODE

The V^+ pin can be disconnected from the C pins and the battery pack. If the V^+ supply pin is 0V, the LTC6803 will typically draw less than 1nA from the battery cells. All circuits inside the IC are off. It is not possible to communicate with the IC when V^+ = 0V. See the Applications Information section for hardware shutdown circuits.

STANDBY MODE

The LTC6803 defaults (powers up) to standby mode. Standby mode is the lowest supply current state with a supply connected. Standby current is typically 12µA when V^+ = 44V. All circuits are turned off except the serial interface and the voltage regulator. For the lowest possible standby current consumption, all SPI logic inputs should be set to logic 1 level. The LTC6803 can be programmed for standby mode by setting the comparator duty cycle configuration bits, CDC[2:0], to 0. If the part is put into standby mode while ADC measurements are in progress, the measurements will be interrupted and the cell voltage registers will be in an indeterminate state. To exit standby mode, the CDC bits must be written to a value other than 0.

MEASURE MODE

The LTC6803 is in measure mode when the CDC bits are programmed with a value from 1 to 7. When CDC = 1 the LTC6803 is on and waiting for a start ADC conversion command. When CDC is 2 through 7 the IC monitors each cell voltage and produces an interrupt signal on the SDO pin indicating all cell voltages are within the UV and OV limits. The value of the CDC bits determines how often the cells are monitored, and, how much average supply current is consumed.

OPERATION

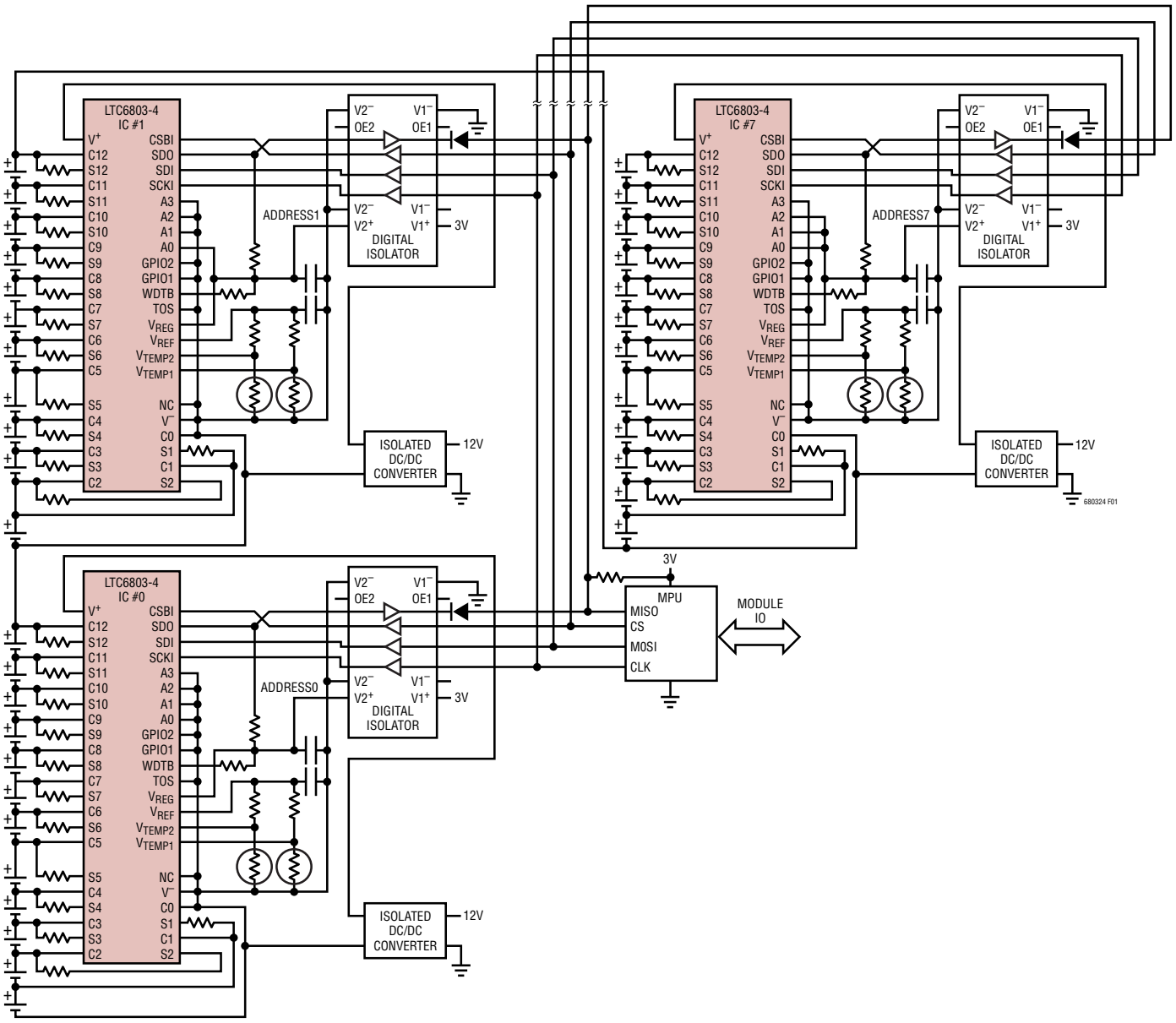


Figure 1. Simplified 96-Cell Battery or Supercapacitor, Isolated Interface. In this Diagram the Battery Negative is Isolated from the Module Ground. Isolated Power Supplies Each LTC6803-4. Opto-Couplers or Digital Isolators Allow Each IC to Be Addressed Individually

OPERATION

There are two methods for indicating the UV/OV interrupt status: toggle polling (using a 1kHz output signal) and level polling (using a high or low output signal). The polling methods are described in the Serial Port section. The UV/OV limits are set by the V_{UV} and V_{OV} values in the configuration registers. When a cell voltage exceeds the UV/OV limits a bit is set in the flag register. The UV and OV flag status for each cell can be determined using the *Read Flag Register Group*.

An ADC measurement can be requested at any time when the IC is in measure mode. To initiate cell voltage measurements while in measure mode, a Start A/D Conversion command is sent. After the command has been sent, the LTC6803 will indicate the A/D converter status via toggle polling or level polling (as described in the Serial Port section). During cell voltage measurement commands, the UV and OV flags (within the flag register group) are also updated. When the measurements are complete, the part will continue monitoring UV and OV conditions at the rate designated by the CDC bits. Note that there is a 5µs window during each UV/OV comparison cycle where an ADC measurement request may be missed. This is an unlikely event. For example, the comparison cycle is 2 seconds when CDC = 7. Use the CLEAR command to detect missing ADC commands.

Operating with Less than 12 Cells

If fewer than 12 cells are connected to the LTC6803, the unused input channels must be masked. The MCxI bits in the configuration registers are used to mask channels. In addition, the LTC6803 can be configured to automatically bypass the measurements of the top 2 cells, reducing power consumption and measurement time. If the CELL10 bit is high, the inputs for cell 11 and cell 12 are masked and only the bottom 10-cell voltages will be measured. By default, the CELL10 bit is low, enabling measurement of all 12-cell voltages. Additional information regarding operation with less than 12 cells is provided in the applications section.

ADC RANGE AND OUTPUT FORMAT

The ADC outputs a 12-bit code with an offset of 0x200 (512 decimal). The input voltage can be calculated as:

$$V_{IN} = (DOUT - 512) \bullet V_{LSB};\ V_{LSB} = 1.5mV$$

where DOUT is a decimal integer.

For example, a 0V input will have an output reading of 0x200. An ADC reading of 0x000 means the input was –0.768V. The absolute ADC measurement range is –0.768V to 5.376V. The resolution is $V_{LSB} = 1.5mV = (5.376 + 0.768)/2^{12}$. The useful range is –0.3V to 5V. This range allows monitoring supercapacitors which could have small negative voltage. Inputs below –0.3V exceed the absolute maximum rating of the C pins. If all inputs are negative, the ADC range is reduced to –0.1V. Inputs above 5V will have noisy ADC readings (see Typical Performance Characteristics).

ADC MEASUREMENTS DURING CELL BALANCING

The primary cell voltage ADC measurement commands (STCVAD and STOWAD) automatically turn off a cell's discharge switch while its voltage is being measured. The discharge switches for the cell above and the cell below will also be turned off during the measurement. For example, discharge switches S4, S5 and S6 will be off while cell 5 is being measured. The UV/OV comparison conversions in CDC modes 2 through 7 also cause a momentary turn-off of the discharge switch. For example, switches S4, S5 and S6 will be off while cell 5 is checked for a UV/OV condition.

In some systems it may be desirable to allow discharging to continue during cell voltage measurements. The cell voltage ADC conversion commands STCVDC and STOWDC allow the discharge switches to remain on during cell voltage measurements. This feature allows the system to perform a self test to verify the discharge functionality.

OPERATION

ADC REGISTER CLEAR COMMAND

The clear command can be used to clear the cell voltage registers and temperature registers. The clear command will set all registers to 0xFFF. This command is used to make sure conversions are being made. When cell voltages are stable, ADC results could stay the same. If a start ADC conversion command is sent to the LTC6803 but the PEC fails to match then the command is ignored and the voltage register contents also will not change. Sending a *clear* command then reading back register contents is a way to make sure LTC6803 is accepting commands and performing new measurements. The clear command takes 1ms to execute.

ADC CONVERTER SELF TEST

Two self-test commands can be used to verify the functionality of the digital portions of the ADC. The self tests also verify the cell voltage registers and temperature monitoring registers. During these self tests a test signal is applied to the ADC. If the circuitry is working properly all cell voltage and temperature registers will contain 0x555 or 0xAAA. The time required for the self-test function is the same as required to measure all cell voltages or all temperature sensors.

MULTIPLEXER AND REFERENCE SELF TEST

The LTC6803 uses a multiplexer to measure the 12 battery cell inputs as well as the temperature signals. A diagnostic command is used to validate the function of the multiplexer, the temperature sensor, and the precision reference circuit. Diagnostic registers will be updated after each diagnostic test. The *muxfail* bit of the registers will be 1 if the multiplexer self test fails.

A constant voltage generated by the 2nd reference circuit will be measured by the ADC and the results written to the diagnostic register. The voltage reading should be 2.5V ±16%. Readings outside this range indicate a failure of the temperature sensor circuit, the precision reference circuit, or the analog portion of the ADC. The DAGN command executes in 16.4ms, which is the sum of the 12-cell t_{CYCLE} and the 3 temperature t_{CYCLE}. The diagnostic read command can be used to read the registers.

USING THE GENERAL PURPOSE INPUTS/OUTPUTS (GPIO1, GPIO2)

The LTC6803 has two general purpose digital input/output pins. By writing a GPIO configuration register bit to a logic low, the open-drain output can be activated. The GPIOs give the user the ability to turn on/off circuitry around the LTC6803. One example might be a circuit to verify the operation of the system.

When a GPIO configuration bit is written to a logic high, the corresponding GPIO pin may be used as an input. The read back value of that bit will be the logic level that appears at the GPIO pins.

WATCHDOG TIMER CIRCUIT

The LTC6803 includes a watchdog timer circuit. The watchdog timer is on for all modes except CDC = 0. The watchdog timer times out if no valid command is received for 1 to 2.5 seconds. When the watchdog timer circuit times out, the WDTB open-drain output is asserted low and the configuration register bits are reset to their default (power-up) state. In the power-up state, CDC is 0, the S outputs are off and the IC is in the low power standby mode. The WDTB pin remains low until a valid command is received. The watchdog timer provides a means to turn off cell discharging should communications to the MPU be interrupted. There is no need for the watchdog timer at CDC = 0 since discharging is off. The open-drain WDTB output can be wire ORd with other external open-drain signals. Pulling the WDTB signal low will not initiate a watchdog event, but the CNFGO bit 7 will reflect the state of this signal. Therefore, the WDTB pin can be used to monitor external digital events if desired.

SERIAL PORT

Overview

The LTC6803-2/LTC6803-4 has an SPI bus compatible serial port. Devices can be connected in parallel, using digital isolators. Multiple devices are uniquely identified by a part address determined by the A0 to A3 pins. Physical Layer on the LTC6803-2/LTC6803-4, four pins comprise the serial interface: CSBI, SCKI, SDI and SDO. The SDO

OPERATION

and SDI may be tied together, if desired, to form a single, bi-directional port. Four address pins (A0 to A3) set the part address for address commands. The TOS pin designates the top device (logic high) for polling commands. All interface pins are voltage mode, with voltage levels sensed with respect to the V^- supply. See Figure 1.

Data Link Layer

Clock Phase And Polarity: The LTC6803 SPI compatible interface is configured to operate in a system using CPHA = 1 and CPOL = 1. Consequently, data on SDI must be stable during the rising edge of SCKI.

Data Transfers: Every byte consists of 8 bits. Bytes are transferred with the most significant bit (MSB) first. On a write, the data value on SDI is latched into the device on the rising edge of SCKI (Figure 2). Similarly, on a read, the data value output on SDO is valid during the rising edge of SCKI and transitions on the falling edge of SCKI (Figure 3).

CSBI must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. On a write command, data is latched in on the rising edge of CSBI.

Network Layer

PEC Byte: The packet error code (PEC) byte is a cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC value of 01000001 and the following characteristic polynomial:

$$x^8 + x^2 + x + 1$$

To calculate the 8-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 0100 0001.
2. For each bit DIN coming into the register group, set IN0 = DIN XOR PEC[7], then IN1 = PEC[0] XOR IN0, IN2 = PEC[1] XOR IN0.
3. Update the 8-bit PEC as PEC[7] = PEC[6], PEC[6] = PEC[5],.....PEC[3] = PEC[2], PEC[2] = IN2, PEC[1] = IN1, PEC[0] = IN0.
4. Go back to step 2 until all data are shifted. The 8-bit result is the final PEC byte.

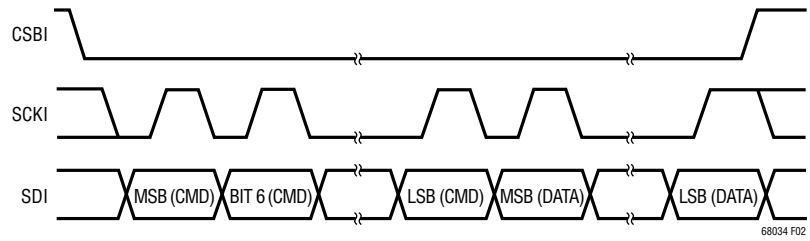


Figure 2. Transmission Format (Write)

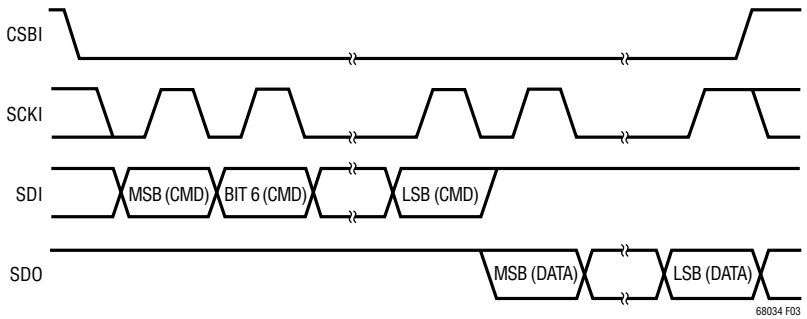


Figure 3. Transmission Format (Read)

OPERATION

An example to calculate the PEC is listed in Table 1 and Figure 4. The PEC of the 1 byte data 0x01 is computed as 0xC7 after the last bit of the byte streamed in. For multiple byte data, PEC is valid at the end (LSB) of the last byte.

LTC6803 calculates PEC byte for any command or data received and compares it with the PEC byte following the command or data. The command or data is regarded as valid only if the PEC bytes match. LTC6803 also attaches the calculated PEC byte at the end of the data it shifts out.

Broadcast Commands: A broadcast command is one to which all devices on the bus will respond, regardless of device address. See the Bus Protocols and Commands sections. With broadcast commands all devices can be sent commands simultaneously. This is useful for ADC conversion and polling commands. It can also be used with write commands when all parts are being written with the same data. Broadcast read commands should not be used in the parallel configuration.

Address Commands: An address command is one in which only the addressed device on the bus responds. The first byte of an address command consists of 4 bits with a value of 1000 and 4 address bits. Following the address command is its PEC byte. The third and fourth bytes are the command byte and its PEC byte respectively. See the Bus Protocols and Commands section.

Polling Methods: For ADC conversions, three methods can be used to determine ADC completion. First, a controller can start an ADC conversion and wait for the specified conversion time to pass before reading the results. The second method is to hold CSBI low after an ADC start command has been sent. The ADC conversion status will be output on SDO (Figure 5). A problem with the second method is that the controller is not free to do other serial communication while waiting for ADC conversions to complete. The third method overcomes this limitation. The controller can send an ADC start command, perform other tasks, and then send a poll ADC converter status (PLADC) command to determine the status of the ADC conversions (Figure 6). For OV/UV interrupt status, the poll interrupt status (PLINT) command can be used to quickly determine whether any cell in a stack is in an overvoltage or undervoltage condition (Figure 6).

Table 1. Procedure to Calculate PEC Byte

CLOCK CYCLE	DIN	IN0	IN1	IN2	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]
0	0	0	1	0	0	1	0	0	0	0	0	1
1	0	1	1	0	1	0	0	0	0	0	1	0
2	0	0	1	1	0	0	0	0	0	0	1	1
3	0	0	0	1	0	0	0	0	0	1	1	0
4	0	0	0	0	0	0	0	0	1	1	0	0
5	0	0	0	0	0	0	0	1	1	0	0	0
6	0	0	0	0	0	0	1	1	0	0	0	0
7	1	1	1	1	0	1	1	0	0	0	0	0
8					1	1	0	0	0	1	1	1

OPERATION

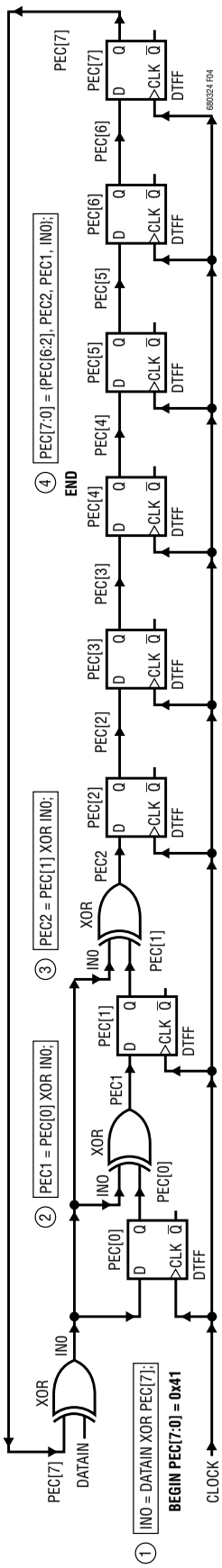


Figure 4

OPERATION

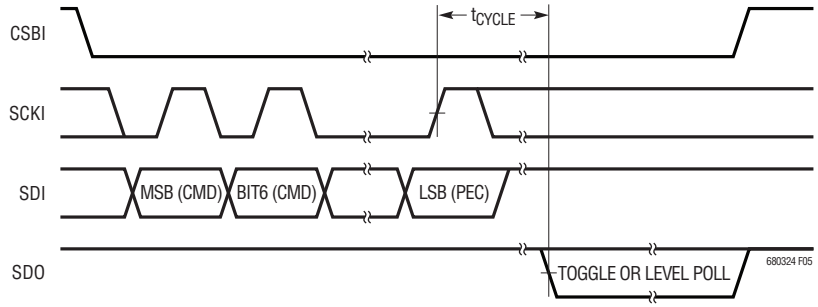


Figure 5. Transmission Format (ADC Conversion and Poll)

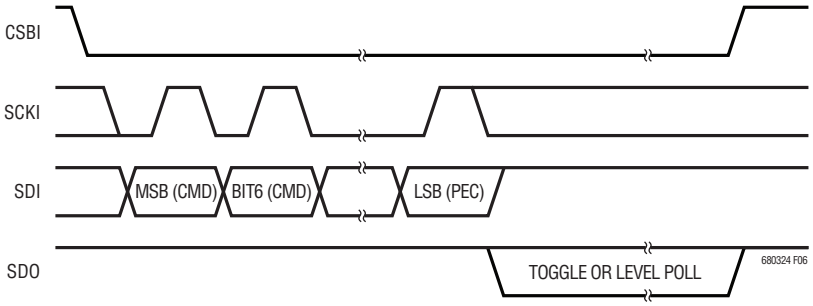


Figure 6. Transmission Format (PLADC Conversion or PLINT)

Toggle Polling: Toggle polling allows a robust determination both of device states and of the integrity of the connections between the devices in a stack. Toggle polling is enabled when the LVLPL bit is low. After entering a polling command, the data out line will be driven by the slave devices based on their status. When polling for the ADC converter status, data out will be low when any device is busy performing an ADC conversion and will toggle at 1kHz when no device is busy. Similarly, when polling for interrupt status, the output will be low when any device has an interrupt condition and will toggle at 1kHz when none has an interrupt condition.

Toggle Polling—Address Polling: The addressed device drives the SDO line based on its state alone—low for busy/in interrupt, toggling at 1kHz for not busy/not in interrupt.

Toggle Polling—Parallel Broadcast Polling: No part address is sent, so all devices respond simultaneously. If a device is busy/in interrupt, it will pull SDO low. If a device is not busy/not in interrupt, then it will release the SDO line (TOS = 0) or attempt to toggle the SDO line at 1kHz (TOS = 1).The master controller pulls CSBI high to exit polling.

Level Polling: Level polling is enabled when the LVLPL bit is high. After entering a polling command, the data out line will be driven by the slave devices based on their status. When polling for the ADC converter status, data out will be low when any device is busy performing an ADC conversion and will be high when no device is busy. Similarly, when polling for interrupt status, the output will be low when any device has an interrupt condition and will be high when none has an interrupt condition.

Level Polling—Address Polling: The addressed device drives the SDO line based on its state alone—pulled low for busy/in interrupt, released for not busy/not in interrupt.

Level polling—Parallel Broadcast Polling: No part address is sent, so all devices respond simultaneously. If a device is busy/in interrupt, it will pull SDO low. If a device is not busy/not in interrupt, then it will release the SDO line. If any device is busy or in interrupt the SDO signal will be low. If all devices are not busy/not in interrupt, the SDO signal will be high. The master controller pulls CSBI high to exit polling.

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Revision Code

The diagnostic register group contains a 2-bit revision code. If software detection of device revision is necessary, then contact the factory for details. Otherwise, the code can be ignored. In all cases, however, the values of all bits must be used when calculating the packet error code (PEC) byte on data reads.

Bus Protocols

There are 6 different protocol formats, depicted in Table 3 through Table 8. Table 2 is the key for reading the protocol diagrams.

Table 2. Protocol Key

PEC		Packet Error Code			Master-to-Slave
N		Number of Bits			Slave-to-Master
...		Continuation of Protocol			Complete Byte of Data

Table 3. Broadcast Poll Command

8	8	
Command	PEC	Poll Data

Table 4. Broadcast Read

8	8	8	…	8	8
Command	PEC	Data Byte Low	…	Data Byte High	PEC

A bus collision will occur if multiple devices are on the same serial bus.

Table 5. Broadcast Write

8	8	8	…	8	8
Command	PEC	Data Byte Low	…	Data Byte High	PEC

Table 6. Address Poll Command

4	4	8	8	8	
1000	Address	PEC	Command	PEC	Poll Data

Table 7. Address Read

4	4	8	8	8	8	…	8	8
1000	Address	PEC	Command	PEC	Data Byte Low	…	Data Byte High	PEC

See Serial Command examples

Table 8. Address Write

4	4	8	8	8	8	…	8	8
1000	Address	PEC	Command	PEC	Data Byte Low	…	Data Byte High	PEC

OPERATION

Commands

Table 9. Command Codes and PEC Bytes

COMMAND DESCRIPTION	NAME		CODE	PEC
Write Configuration Register Group	WRCFG		01	C7
Read Configuration Register Group	RDCFG		02	CE
Read All Cell Voltage Group	RDCV		04	DC
Read Cell Voltages 1-4	RDCVA		06	D2
Read Cell Voltages 5-8	RDCVB		08	F8
Read Cell Voltages 9-12	RDCVC		0A	F6
Read Flag Register Group	RDFLG		0C	E4
Read Temperature Register Group	RDTMP		0E	EA
Start Cell Voltage ADC Conversions and Poll Status	STCVAD	All Cell 1 Cell 2 Cell 3 Cell 4 Cell 5 Cell 6 Cell 7 Cell 8 Cell 9 Cell 10 Cell 11 Cell 12 Clear (FF) Self Test1 Self Test2	10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F	B0 B7 BE B9 AC AB A2 A5 88 8F 86 81 94 93 9A 9D
Start Open-Wire ADC Conversions and Poll Status	STOWAD	All Cell 1 Cell 2 Cell 3 Cell 4 Cell 5 Cell 6 Cell 7 Cell 8 Cell 9 Cell 10 Cell 11 Cell 12	20 21 22 23 24 25 26 27 28 29 2A 2B 2C	20 27 2E 29 3C 3B 32 35 18 1F 16 11 4
Start Temperature ADC Conversions and Poll Status	STTMPAD	All External1 External2 Internal Self Test 1 Self Test 2	30 31 32 33 3E 3F	50 57 5E 59 7A 7D
Poll ADC Converter Status	PLADC		40	07
Poll Interrupt Status	PLINT		50	77
Start Diagnose and Poll Status	DAGN		52	79
Read Diagnostic Register	RDDGNR		54	6B

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Table 9. Command Codes and PEC Bytes (continued)

COMMAND DESCRIPTION	NAME		CODE	PEC
Start Cell Voltage ADC Conversions and Poll Status, with Discharge Permitted	STCVDC	All	60	E7
		Cell 1	61	E0
		Cell 2	62	E9
		Cell 3	63	EE
		Cell 4	64	FB
		Cell 5	65	FC
		Cell 6	66	F5
		Cell 7	67	F2
		Cell 8	68	DF
		Cell 9	69	D8
		Cell 10	6A	D1
		Cell 11	6B	D6
		Cell 12	6C	C3
Start Open-Wire ADC Conversions and Poll Status, with Discharge Permitted	STOWDC	All	70	97
		Cell 1	71	90
		Cell 2	72	99
		Cell 3	73	9E
		Cell 4	74	8B
		Cell 5	75	8C
		Cell 6	76	85
		Cell 7	77	82
		Cell 8	78	AF
		Cell 9	79	A8
		Cell 10	7A	A1
		Cell 11	7B	A6
		Cell 12	7C	B3

Table 10. Configuration (CFG) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGR0	RD/WR	WDT	GPIO2	GPIO1	LVLPL	CELL10	CDC[2]	CDC[1]	CDC[0]
CFGR1	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGR2	RD/WR	MC4I	MC3I	MC2I	MC1I	DCC12	DCC11	DCC10	DCC9
CFGR3	RD/WR	MC12I	MC11I	MC10I	MC9I	MC8I	MC7I	MC6I	MC5I
CFGR4	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGR5	RD/WR	VOV[7]	VOV[6]	VOV[5]	VOV[4]	VOV[3]	VOV[2]	VOV[1]	VOV[0]

OPERATION

Table 11. Cell Voltage (CV) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVR00	RD	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVR01	RD	C2V[3]	C2V[2]	C2V[1]	C2V[0]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVR02	RD	C2V[11]	C2V[10]	C2V[9]	C2V[8]	C2V[7]	C2V[6]	C2V[5]	C2V[4]
CVR03	RD	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVR04	RD	C4V[3]	C4V[2]	C4V[1]	C4V[0]	C3V[11]	C3V[10]	C3V[9]	C3V[8]
CVR05	RD	C4V[11]	C4V[10]	C4V[9]	C4V[8]	C4V[7]	C4V[6]	C4V[5]	C4V[4]
CVR06	RD	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVR07	RD	C6V[3]	C6V[2]	C6V[1]	C6V[0]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVR08	RD	C6V[11]	C6V[10]	C6V[9]	C6V[8]	C6V[7]	C6V[6]	C6V[5]	C6V[4]
CVR09	RD	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVR10	RD	C8V[3]	C8V[2]	C8V[1]	C8V[0]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVR11	RD	C8V[11]	C8V[10]	C8V[9]	C8V[8]	C8V[7]	C8V[6]	C8V[5]	C8V[4]
CVR12	RD	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVR13	RD	C10V[3]	C10V[2]	C10V[1]	C10V[0]	C9V[11]	C9V[10]	C9V[9]	C9V[8]
CVR14	RD	C10V[11]	C10V[10]	C10V[9]	C10V[8]	C10V[7]	C10V[6]	C10V[5]	C10V[4]
CVR15*	RD	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVR16*	RD	C12V[3]	C12V[2]	C12V[1]	C12V[0]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVR17*	RD	C12V[11]	C12V[10]	C12V[9]	C12V[8]	C12V[7]	C12V[6]	C12V[5]	C12V[4]

*Registers CVR15, CVR16, and CVR17 can only be read if the CELL10 bit in register CFGR0 is low

Table 12. Flag (FLG) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLGR0	RD	C4OV	C4UV	C3OV	C3UV	C2OV	C2UV	C1OV	C1UV
FLGR1	RD	C8OV	C8UV	C7OV	C7UV	C6OV	C6UV	C5OV	C5UV
FLGR2	RD	C12OV*	C12UV*	C11OV*	C11UV*	C10OV	C10UV	C9OV	C9UV

* Bits C11UV, C12UV, C11OV and C12OV are always low if the CELL10 bit in register CFGR0 is high

Table 13. Temperature (TMP) Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMPR0	RD	ETMP1[7]	ETMP1[6]	ETMP1[5]	ETMP1[4]	ETMP1[3]	ETMP1[2]	ETMP1[1]	ETMP1[0]
TMPR1	RD	ETMP2[3]	ETMP2[2]	ETMP2[1]	ETMP2[0]	ETMP1[11]	ETMP1[10]	ETMP1[9]	ETMP1[8]
TMPR2	RD	ETMP2[11]	ETMP2[10]	ETMP2[9]	ETMP2[8]	ETMP2[7]	ETMP2[6]	ETMP2[5]	ETMP2[4]
TMPR3	RD	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
TMPR4	RD	NA	NA	NA	THSD	ITMP[11]	ITMP[10]	ITMP[9]	ITMP[8]

Table 14. Packet Error Code (PEC)

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PEC	RD	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]

Table 15. Diagnostic Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DGNR0	RD	REF[7]	REF[6]	REF[5]	REF[4]	REF[3]	REF[2]	REF[1]	REF[0]
DGNR1	RD	REV[1]	REV[0]	MUXFAIL	NA	REF[11]	REF[10]	REF[9]	REF[8]

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Table 16. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES			
CDC	Comparator Duty Cycle	**CDC**	**UV/OV COMPARATOR PERIOD**	**V_{REF} POWERED DOWN BETWEEN MEASUREMENTS**	**CELL VOLTAGE MEASUREMENT TIME**
		0 (Default)	N/A (Comparator Off) Standby Mode	Yes	N/A
		1	N/A (Comparator Off)	No	13ms
		2	13ms	No	13ms
		3	130ms	No	13ms
		4	500ms	No	13ms
		5	130ms	Yes	21ms
		6	500ms	Yes	21ms
		7	2000ms	Yes	21ms
CELL10	10-Cell Mode	0 = 12-cell mode (default); 1 = 10-cell mode			
LVLPL	Level Polling Mode	0 = toggle polling (default); 1 = level polling			
GPIO1	GPIO1 Pin Control	Write: 0 = GPIO1 pin pull-down on; 1 = GPIO1 pin pull-down off (default) Read: 0 = GPIO1 pin at logic '0'; 1 = GPIO1 pin at logic '1'			
GPIO2	GPIO2 Pin Control	Write: 0 = GPIO2 pin pull-down on; 1 = GPIO2 pin pull-down off (default) Read: 0 = GPIO2 pin at logic '0'; 1 = GPIO2 pin at logic '1'			
WDT	Watchdog Timer	Read: 0 = WDTB pin at logic '0'; 1 = WDTB pin at logic '1'			
DCCx	Discharge Cell x	x = 1..12 0 = turn off shorting switch for cell 'x' (default); 1 = turn on shorting switch			
V_{UV}	Undervoltage Comparison Voltage*	Comparison voltage = (V_{UV} –31) • 16 • 1.5mV (Default V_{UV} = 0)			
V_{OV}	Overvoltage Comparison Voltage*	Comparison voltage = (V_{OV} –32) • 16 • 1.5mV (Default V_{OV} = 0)			
MCxI	Mask Cell x Interrupts	x = 1..12 0 = enable interrupts for cell 'x' (default) 1 = turn off interrupts and clear flags for cell 'x'			
CxV	Cell x Voltage*	x = 1..12 12-bit ADC measurement value for cell 'x' cell voltage for cell 'x' = (CxV –512) • 1.5mV reads as 0xFFF while A/D conversion in progress			
CxUV	Cell x Undervoltage Flag	x = 1..12 cell voltage compared to V_{UV} comparison voltage 0 = cell 'x' not flagged for undervoltage condition; 1 = cell 'x' flagged			
CxOV	Cell x Overvoltage Flag	x = 1..12 cell voltage compared to V_{OV} comparison voltage 0 = cell 'x' not flagged for overvoltage condition; 1 = cell 'x' flagged			
ETMPx	External Temperature Measurement*	Temperature measurement voltage = (ETMPx –512) • 1.5mV			
THSD	Thermal Shutdown Status	0 = thermal shutdown has not occurred; 1 = thermal shutdown has occurred Status cleared to '0' on read of Thermal Register Group			
REV	Revision Code	Device revision code			
ITMP	Internal Temperature Measurement*	Temperature measurement voltage = (ITMP –512) • 1.5mV = 8mV • T(°K)			
PEC	Packet Error Code	Cyclic redundancy check (CRC) value			
REF	Reference Voltage for Diagnostics	This reference voltage = (REF –512) • 1.5mV. Normal range is within 2.1V to 2.9V			

*Voltage equations use the decimal value of the registers, 0 to 4095 for 12-bit and 0 to 255 for 8-bit registers