Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Multicell Battery Monitors

FEATURES

- **Pin-Compatible Upgrade from the LTC6804**
- **Measures Up to 12 Battery Cells in Series**
- **1.2mV Maximum Total Measurement Error**
- **Stackable Architecture Supports 100s of Cells**
- **Built-in isoSPI™ Interface**
  - 1Mb Isolated Serial Communications
  - Uses a Single Twisted Pair, up to 100 Meters
  - Low EMI Susceptibility and Emissions
- 290µs to Measure All Cells in a System
- Synchronized Voltage and Current Measurement
- 16-Bit Delta-Sigma ADC with Programmable 3rd Order Noise Filter
- Engineered for ISO26262 Compliant Systems
- Passive Cell Balancing with Programmable Timer
- 5 General Purpose Digital I/O or Analog Inputs
  - Temperature or other Sensor Inputs
  - Configurable as an I^2C or SPI master
- 4µA Sleep Mode Supply Current
- 48-Lead SSOP Package

APPLICATIONS

- Electric and Hybrid Electric Vehicles
- Backup Battery Systems
- Grid Energy Storage
- High Power Portable Equipment

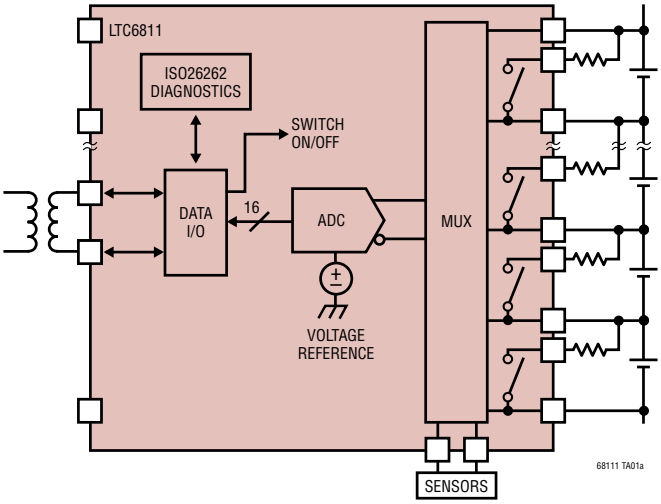
DESCRIPTION

The LTC®6811 is a multicell battery stack monitor that measures up to 12 series connected battery cells with a total measurement error of less than 1.2mV. The cell measurement range of 0V to 5V makes the LTC6811 suitable for most battery chemistries. All 12 cells can be measured in 290µs, and lower data acquisition rates can be selected for high noise reduction.

Multiple LTC6811 devices can be connected in series, permitting simultaneous cell monitoring of long, high voltage battery strings. Each LTC6811 has an isoSPI interface for high speed, RF-immune, long distance communications. Using the LTC6811-1, multiple devices are connected in a daisy chain with one host processor connection for all devices. Using the LTC6811-2, multiple devices are connected in parallel to the host processor, with each device individually addressed.

The LTC6811 can be powered directly from the battery stack or from an isolated supply. The LTC6811 includes passive balancing for each cell, with individual PWM duty cycle control for each cell. Other features include an onboard 5V regulator, five general purpose I/O lines and a sleep mode, where current consumption is reduced to 6µA.

TYPICAL APPLICATION



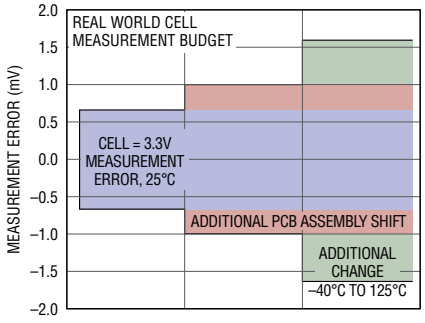


TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage, V^+ to V^- 75V
Supply Voltage (Relative to C6), V^+ to C6 ..... 50V
Input Voltage (Relative to V^-),
- C0 ..... –0.3V to 0.3V
- C12 ..... –0.3V to MIN(V+ + 5.5V, 75V)
- C(n) ..... –0.3V to MIN(8 • n, 75V)
- S(n) ..... –0.3V to MIN(8 • n, 75V)
- IPA, IMA, IPB, IMB ..... –0.3V to V_{REG} + 0.3V, ≤6V
- DRIVE ..... –0.3V to 7V
- All Other Pins ..... –0.3V to 6V

Voltage Between Inputs
- C(n) to C(n – 1) ..... –0.3V to 8V
- S(n) to S(n – 1) ..... –0.3V to 8V
- C12 to C9 ..... –0.3V to 21V
- C9 to C6 ..... –0.3V to 21V
- C6 to C3 ..... –0.3V to 21V
- C3 to C0 ..... –0.3V to 21V

Current In/Out of Pins
- All Pins Except V_{REG}, IPA, IMA, IPB, IMB, S(n) ..10mA
- IPA, IMA, IPB, IMB 30mA

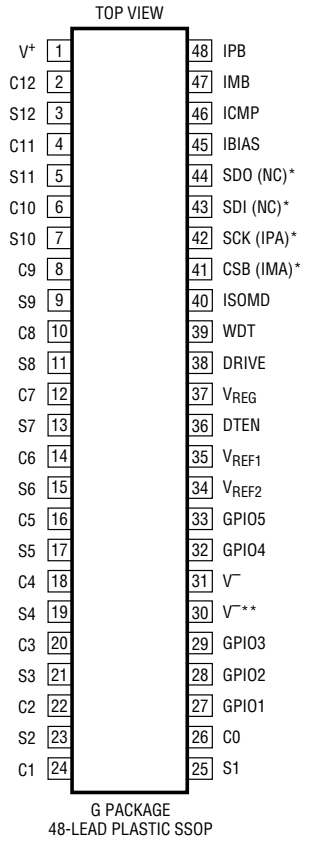
Operating Temperature Range
- LTC6811I ..... –40°C to 85°C
- LTC6811H ..... –40°C to 125°C

Specified Temperature Range
- LTC6811I ..... –40°C to 85°C
- LTC6811H ..... –40°C to 125°C

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec) ..... 300°C

PIN CONFIGURATION

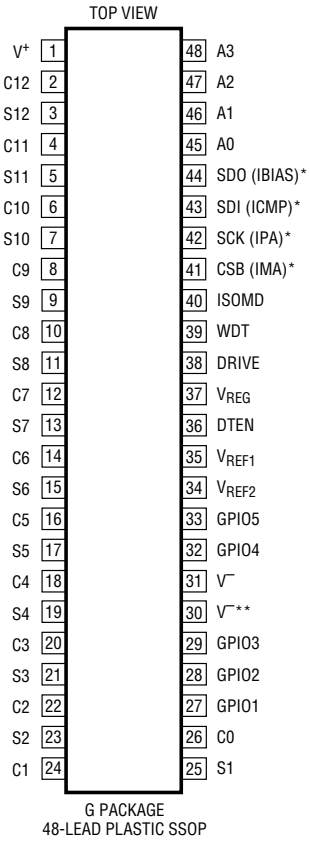
LTC6811-1



G PACKAGE
48-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 55°C/W
*THE FUNCTION OF THESE PINS DEPENDS ON THE CONNECTION OF ISOMD
ISOMD TIED TO V^-: CSB, SCK, SDI, SDO
ISOMD TIED TO V_{REG}: IMA, IPA, NC, NC
**THIS PIN MUST BE CONNECTED TO V^-

LTC6811-2



G PACKAGE
48-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 55°C/W
*THE FUNCTION OF THESE PINS DEPENDS ON THE CONNECTION OF ISOMD
ISOMD TIED TO V^-: CSB, SCK, SDI, SDO
ISOMD TIED TO V_{REG}: IMA, IPA, NC, NC
**THIS PIN MUST BE CONNECTED TO V^-

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6811IG-1#PBF	LTC6811IG-1#TRPBF	LTC6811G-1	48-Lead Plastic SSOP	–40°C to 85°C
LTC6811HG-1#PBF	LTC6811HG-1#TRPBF	LTC6811G-1	48-Lead Plastic SSOP	–40°C to 125°C
LTC6811IG-2#PBF	LTC6811IG-2#TRPBF	LTC6811G-2	48-Lead Plastic SSOP	–40°C to 85°C
LTC6811HG-2#PBF	LTC6811HG-2#TRPBF	LTC6811G-2	48-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Parts ending with PBF are RoHS and WEEE compliant.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/ Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted. The ISOMD pin is tied to the V– pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC DC Specifications							
	Measurement Resolution		●		0.1		mV/bit
	ADC Offset Voltage	(Note 2)	●		0.1		mV
	ADC Gain Error	(Note 2)	 ●		0.01 0.02		% %
	Total Measurement Error (TME) in Normal Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±0.2		mV
		C(n) to C(n – 1) = 2.0			±0.1	±0.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±1.4	mV
		C(n) to C(n – 1) = 3.3			±0.2	±1.2	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±2.2	mV
		C(n) to C(n – 1) = 4.2			±0.3	±1.6	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±2.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±1		mV
		Sum of Cells	●		±0.05	±0.25	%
		Internal Temperature T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.1	±0.25	%
		V_{REF2} Pin	●		±0.02	±0.1	%
		Digital Supply Voltage V_{REGD}	●		±0.1	±1	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Total Measurement Error (TME) in Filtered Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±0.1		mV
		C(n) to C(n – 1) = 2.0			±0.1	±0.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±1.4	mV
		C(n) to C(n – 1) = 3.3			±0.2	±1.2	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±2.2	mV
		C(n) to C(n – 1) = 4.2			±0.3	±1.6	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±2.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±1		mV
		Sum of Cells	●		±0.05	±0.25	%
		Internal Temperature T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.1	±0.25	%
		V_{REF2} Pin	●		±0.02	±0.1	%
		Digital Supply Voltage V_{REGD}	●		±0.1	±1	%
	Total Measurement Error (TME) in Fast Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±2		mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±4	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±4.7	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±8.3	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±10		mV
		Sum of Cells	●		±0.15	±0.5	%
		Internal Temperature T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.3	±1	%
		V_{REF2} Pin	●		±0.1	±0.25	%
		Digital Supply Voltage V_{REGD}	●		±0.2	±2	%
	Input Range	C(n), n = 1 to 12	●	C(n – 1)		C(n – 1) + 5	V
		C0	●		0		
		GPIO(n), n = 1 to 5	●	0		5	V
I_L	Input Leakage Current When Inputs Are Not Being Measured (State: Core = STANDBY)	C(n), n = 0 to 12	●		10	±250	nA
		GPIO(n), n = 1 to 5	●		10	±250	nA
	Input Current When Inputs Are Being Measured (State: Core = MEASURE)	C(n), n = 0 to 12			±1		µA
		GPIO(n), n = 1 to 5			±1		µA
	Input Current During Open Wire Detection		●	70	100	130	µA
Voltage Reference Specifications							
V_{REF1}	1st Reference Voltage	V_{REF1} Pin, No Load	●	3.1	3.2	3.3	V
	1st Reference Voltage TC	V_{REF1} Pin, No Load			3		ppm/°C
	1st Reference Voltage Hysteresis	V_{REF1} Pin, No Load			20		ppm
	1st Reference V. Long Term Drift	V_{REF1} Pin, No Load			20		ppm/$\sqrt{khr}$

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{REF2}	2nd Reference Voltage	V_{REF2} Pin, No Load		●	2.995	3	3.005	V
		V_{REF2} Pin, 5k Load to V^-		●	2.995	3	3.005	V
	2nd Reference Voltage TC	V_{REF2} Pin, No Load				10		ppm/°C
	2nd Reference Voltage Hysteresis	V_{REF2} Pin, No Load				100		ppm
	2nd Reference V. Long Term Drift	V_{REF2} Pin, No Load				60		ppm/$\sqrt{khr}$
General DC Specifications								
I_{VP}	V^+ Supply Current (See Figure 1: LTC6811 Operation State Diagram)	State: Core = SLEEP isoSPI = IDLE	V_{REG} = 0V			4.1	7	µA
			V_{REG} = 0V	●		4.1	10	µA
			V_{REG} = 5V			1.9	3	µA
			V_{REG} = 5V	●		1.9	5	µA
		State: Core = STANDBY		 ●	8 6	13 13	19 24	µA µA
		State: Core = REFUP or MEASURE		 ●	0.4 0.375	0.55 0.55	0.75 0.775	mA mA
$I_{REG(CORE)}$	V_{REG} Supply Current (See Figure 1: LTC6811 Operation State Diagram)	State: Core = SLEEP isoSPI = IDLE	V_{REG} = 5V			2.2	4	µA
			V_{REG} = 5V	●		2.2	6	µA
		State: Core = STANDBY		 ●	17 14	40 40	67 70	µA µA
		State: Core = REFUP		 ●	0.2 0.15	0.45 0.45	0.7 0.75	mA mA
		State: Core = MEASURE		 ●	10.8 10.7	11.5 11.5	12.2 12.3	mA mA
$I_{REG(isoSPI)}$	Additional V_{REG} Supply Current if isoSPI in READY/ACTIVE States Note: ACTIVE State Current Assumes t_{CLK} = 1µs. (Note 3)	LTC6811-2, ISOMD = 1 $R_{B1} + R_{B2}$ = 2K	READY	●	3.6	4.5	5.4	mA
			ACTIVE	●	4.6	5.8	7.0	mA
		LTC6811-1, ISOMD = 0 $R_{B1} + R_{B2}$ = 2K	READY	●	3.6	4.5	5.2	mA
			ACTIVE	●	5.6	6.8	8.1	mA
		LTC6811-1, ISOMD = 1 $R_{B1} + R_{B2}$ = 2K	READY	●	4.0	5.2	6.5	mA
			ACTIVE	●	7.0	8.5	10.5	mA
		LTC6811-2, ISOMD = 1 $R_{B1} + R_{B2}$ = 20K	READY	●	1.0	1.8	2.6	mA
			ACTIVE	●	1.2	2.2	3.2	mA
		LTC6811-1, ISOMD = 0 $R_{B1} + R_{B2}$ = 20K	READY	●	1.0	1.8	2.4	mA
			ACTIVE	●	1.3	2.3	3.3	mA
		LTC6811-1, ISOMD = 1 $R_{B1} + R_{B2}$ = 20K	READY	●	1.6	2.5	3.5	mA
			ACTIVE	●	1.8	3.1	4.8	mA
	V^+ Supply Voltage	TME Specifications Met		●	11	40	55	V
	V^+ to C12 Voltage	TME Specifications Met		●	–0.3			V
	V^+ to C6 Voltage	TME Specifications Met		●			40	V
V_{REG}	V_{REG} Supply Voltage	TME Supply Rejection < 1mV/V		●	4.5	5	5.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	DRIVE Output Voltage	Sourcing 1µA	 ●	5.4 5.2	5.6 5.6	5.8 6.0	V V
		Sourcing 500µA	●	5.1	5.6	6.1	V
V_{REGD}	Digital Supply Voltage		●	2.7	3	3.6	V
	Discharge Switch ON Resistance	V_{CELL} = 3.6V	●		10	25	Ω
	Thermal Shutdown Temperature				150		°C
$V_{OL(WDT)}$	Watch Dog Timer Pin Low	WDT Pin Sinking 4mA	●			0.4	V
$V_{OL(GPIO)}$	General Purpose I/O Pin Low	GPIO Pin Sinking 4mA (Used as Digital Output)	●			0.4	V
ADC Timing Specifications							
t_{CYCLE} (Figure 3, Figure 4, Figure 6)	Measurement + Calibration Cycle Time When Starting from the REFUP State in Normal Mode	Measure 12 Cells	●	2120	2335	2480	µs
		Measure 2 Cells	●	365	405	430	µs
		Measure 12 Cells and 2 GPIO Inputs	●	2845	3133	3325	µs
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Filtered Mode	Measure 12 Cells	●	183	201.3	213.5	ms
		Measure 2 Cells	●	30.54	33.6	35.64	ms
		Measure 12 Cells and 2 GPIO Inputs	●	244	268.4	284.7	ms
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Fast Mode	Measure 12 Cells	●	1010	1113	1185	µs
		Measure 2 Cells	●	180	201	215	µs
		Measure 12 Cells and 2 GPIO Inputs	●	1420	1564	1660	µs
t_{SKEW1} (Figure 6)	Skew Time. The Time Difference between Cell 12 and GPIO1 Measurements, Command = ADCVAX	Fast Mode	●	176	194	206	µs
		Normal Mode	●	493	543	576	µs
t_{SKEW2} (Figure 3)	Skew Time. The Time Difference between Cell 12 and Cell 1 Measurements, Command = ADCV	Fast Mode	●	221	233	248	µs
		Normal Mode	●	609	670	711	µs
t_{WAKE}	Regulator Startup Time	V_{REG} Generated from DRIVE Pin (Figure 32)	●		200	400	µs
t_{SLEEP} (Figure 1)	Watchdog or Discharge Timer	DTEN Pin = 0 or DCTO[3:0] = 0000	●	1.8	2	2.2	sec
		DTEN Pin = 1 and DCTO[3:0] ≠ 0000		0.5		120	min
t_{REFUP} (Figure 3 for example)	Reference Wake-Up Time. Added to t_{CYCLE} Time when Starting from the STANDBY State. t_{REFUP} = 0 When Starting from Other States.	t_{REFUP} Is Independent of the Number of Channels Measured and the ADC Mode.	●	2.7	3.5	4.4	ms
f_S	ADC Clock Frequency				3.3		MHz
SPI interface DC Specifications							
$V_{IH(SPI)}$	SPI Pin Digital Input Voltage High	Pins CSB, SCK, SDI	●	2.3			V
$V_{IL(SPI)}$	SPI Pin Digital Input Voltage Low	Pins CSB, SCK, SDI	●			0.8	V
$V_{IH(CFG)}$	Configuration Pin Digital Input Voltage High	Pins ISOMD, DTEN, GPIO1 to GPIO5, A0 to A3	●	2.7			V
$V_{IL(CFG)}$	Configuration Pin Digital Input Voltage Low	Pins ISOMD, DTEN, GPIO1 to GPIO5, A0 to A3	●			1.2	V
$I_{LEAK(DIG)}$	Digital Input Current	Pins CSB, SCK, SDI, ISOMD, DTEN, A0 to A3	●			±1	µA
$V_{OL(SDO)}$	Digital Output Low	Pin SDO Sinking 1mA	●			0.3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
isoSPI DC Specifications (see Figure 17)							
V_{BIAS}	Voltage on IBIAS Pin	READY/ACTIVE State IDLE State	● ●	1.9	2.0 0	2.1	V V
I_B	Isolated Interface Bias Current	R_{BIAS} = 2k to 20k	●	0.1		1.0	mA
A_{IB}	Isolated Interface Current Gain	$V_A \le 1.6V$ I_B = 1mA I_B = 0.1mA	● ●	18 18	20 20	22 24.5	mA/mA mA/mA
V_A	Transmitter Pulse Amplitude	$V_A = \lvert V_{IP} - V_{IM} \rvert$	●			1.6	V
V_{ICMP}	Threshold-Setting Voltage on ICMP Pin	$V_{TCMP} = A_{TCMP} \bullet V_{ICMP}$	●	0.2		1.5	V
$I_{LEAK(ICMP)}$	Input Leakage Current on ICMP Pin	V_{ICMP} = 0V to V_{REG}	●			±1	µA
$I_{LEAK(IP/IM)}$	Leakage Current on IP and IM Pins	IDLE State, V_{IP} or V_{IM}, 0V to V_{REG}	●			±1	µA
A_{TCMP}	Receiver Comparator Threshold Voltage Gain	$V_{CM} = V_{REG}$ /2 to V_{REG} – 0.2V, V_{ICMP} = 0.2V to 1.5V	●	0.4	0.5	0.6	V/V
V_{CM}	Receiver Common Mode Bias	IP/IM Not Driving		(V_{REG} – V_{ICMP}/3 – 167mV)			V
R_{IN}	Receiver Input Resistance	Single-Ended to IPA, IMA, IPB, IMB	●	26	35	45	kΩ
isoSPI Idle/Wake-Up Specifications (see Figure 26)							
V_{WAKE}	Differential Wake-Up Voltage	t_{DWELL} = 240ns	●	200			mV
t_{DWELL}	Dwell Time at V_{WAKE} Before Wake Detection	V_{WAKE} = 200mV	●	240			ns
t_{READY}	Startup Time After Wake Detection		●			10	µs
t_{IDLE}	Idle Timeout Duration		●	4.3	5.5	6.7	ms
isoSPI Pulse Timing Specifications (see Figure 24)							
$t_{½PW(CS)}$	Chip-Select Half-Pulse Width	Transmitter	●	120	150	180	ns
$t_{FILT(CS)}$	Chip-Select Signal Filter	Receiver	●	70	90	110	ns
$t_{INV(CS)}$	Chip-Select Pulse Inversion Delay	Transmitter	●	120	155	190	ns
$t_{WNDW(CS)}$	Chip-Select Valid Pulse Window	Receiver	●	220	270	330	ns
$t_{½PW(D)}$	Data Half-Pulse Width	Transmitter	●	40	50	60	ns
$t_{FILT(D)}$	Data Signal Filter	Receiver	●	10	25	35	ns
$t_{INV(D)}$	Data Pulse Inversion Delay	Transmitter	●	40	55	65	ns
$t_{WNDW(D)}$	Data Valid Pulse Window	Receiver	●	70	90	110	ns
SPI Timing Requirements (see Figure 16 and Figure 25)							
t_{CLK}	SCK Period	(Note 4)	●	1			µs
t_1	SDI Setup Time before SCK Rising Edge		●	25			ns
t_2	SDI Hold Time after SCK Rising Edge		●	25			ns
t_3	SCK Low	$t_{CLK} = t_3 + t_4 \ge 1µs$	●	200			ns
t_4	SCK High	$t_{CLK} = t_3 + t_4 \ge 1µs$	●	200			ns
t_5	CSB Rising Edge to CSB Falling Edge		●	0.65			µs
t_6	SCK Rising Edge to CSB Rising Edge	(Note 4)	●	0.8			µs
t_7	CSB Falling Edge to SCK Rising Edge	(Note 4)	●	1			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
isoSPI Timing Specifications (See Figure 25)							
t_8	SCK Falling Edge to SDO Valid	(Note 5)	●			60	ns
t_9	SCK Rising Edge to Short ±1 Transmit		●			50	ns
t_{10}	CSB Transition to Long ±1 Transmit		●			60	ns
t_{11}	CSB Rising Edge to SDO Rising	(Note 5)	●			200	ns
t_{RTN}	Data Return Delay		●	325	375	425	ns
$t_{DSY(CS)}$	Chip-Select Daisy-Chain Delay		●		120	180	ns
$t_{DSY(D)}$	Data Daisy-Chain Delay		●	200	250	300	ns
t_{LAG}	Data Daisy-Chain Lag (vs. Chip-Select)	= $[t_{DSY(D)} + t_{½PW(D)}] - [t_{DSY(CS)} + t_{½PW(CS)}]$	●	0	35	70	ns
$t_{5(GOV)}$	Chip-Select High-to-Low Pulse Governor		●	0.8		1.05	µs
$t_{6(GOV)}$	Data to Chip-Select Pulse Governor		●	0.6		0.82	µs

Note 1: Stresses beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error specification.

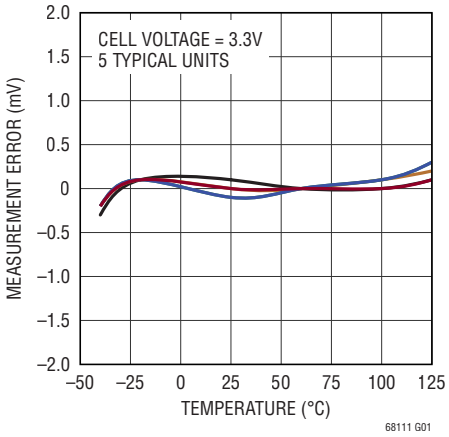
Note 3: The ACTIVE state current is calculated from DC measurements. The ACTIVE state current is the additional average supply current into VREG when there is continuous 1MHz communications on the isoSPI ports with 50% data 1's and 50% data 0's. Slower clock rates reduce the supply current. See Applications Information section for additional details.

Note 4: These timing specifications are dependent on the delay through the cable, and include allowances for 50ns of delay each direction. 50ns corresponds to 10m of CAT5 cable (which has a velocity of propagation of 66% the speed of light). Use of longer cables would require derating these specs by the amount of additional delay.

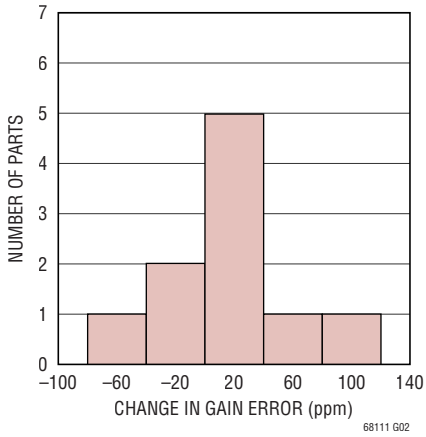
Note 5: These specifications do not include rise or fall time of SDO. While fall time (typically 5ns due to the internal pull-down transistor) is not a concern, rising-edge transition time t_{RISE} is dependent on the pull-up resistance and load capacitance on the SDO pin. The time constant must be chosen such that SDO meets the setup time requirements of the MCU.

TYPICAL PERFORMANCE CHARACTERISTICS

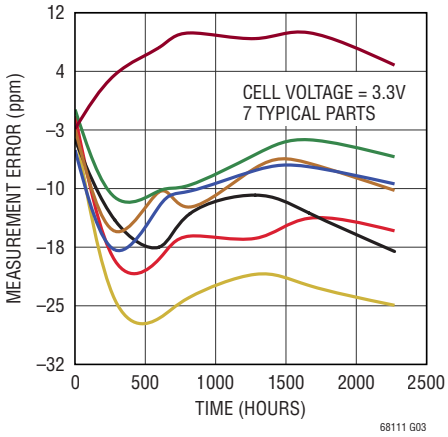
Measurement Error vs Temperature



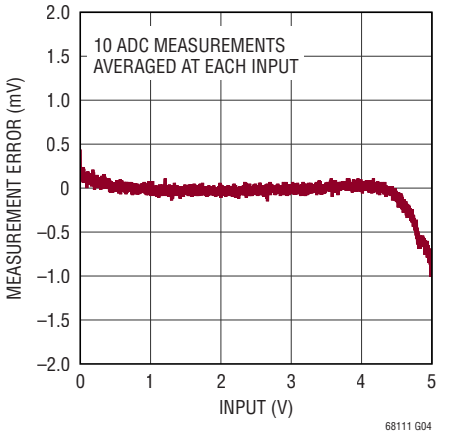
Measurement Error Due to IR Reflow



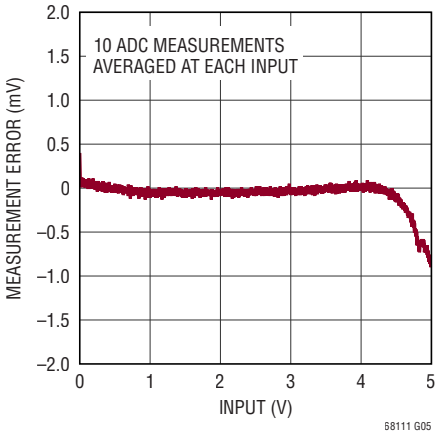
Measurement Error Long-Term Drift



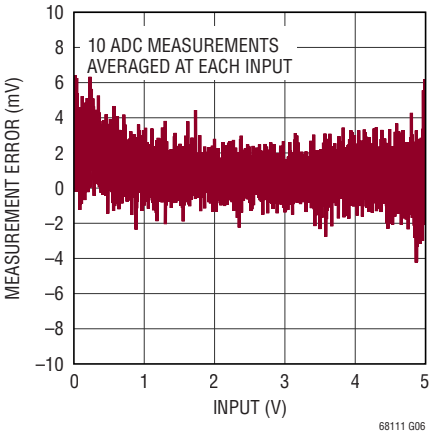
Measurement Error vs Input, Normal Mode



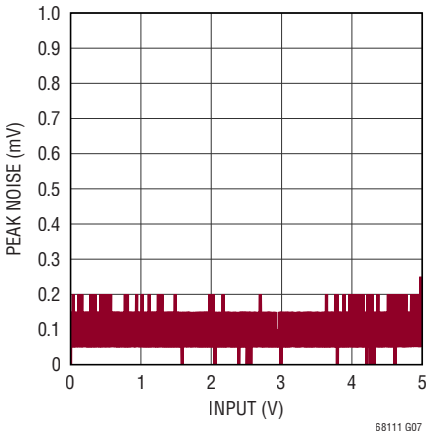
Measurement Error vs Input, Filtered Mode



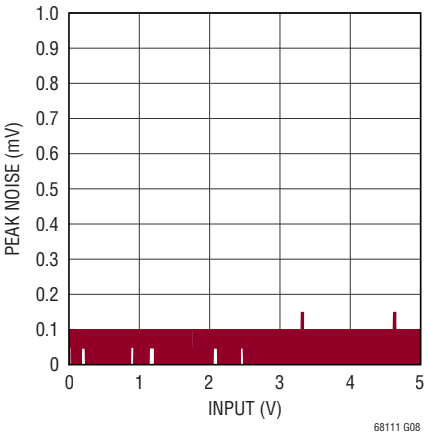
Measurement Error vs Input, Fast Mode



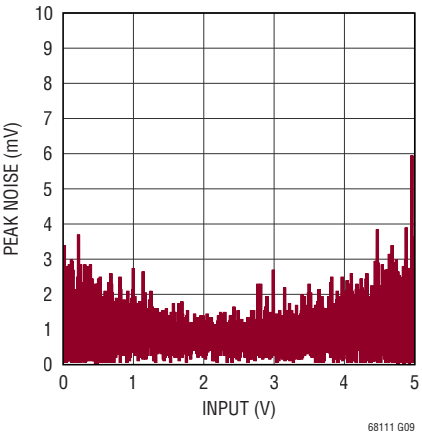
Measurement Noise vs Input, Normal Mode



Measurement Noise vs Input, Filtered Mode

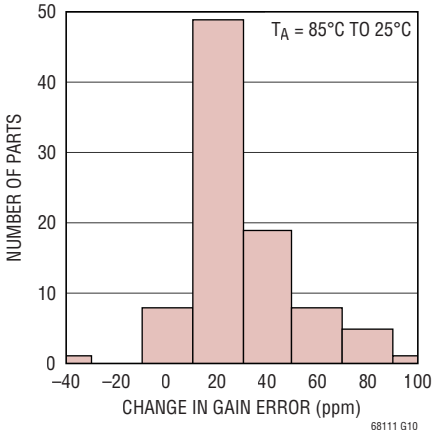


Measurement Noise vs Input, Fast Mode

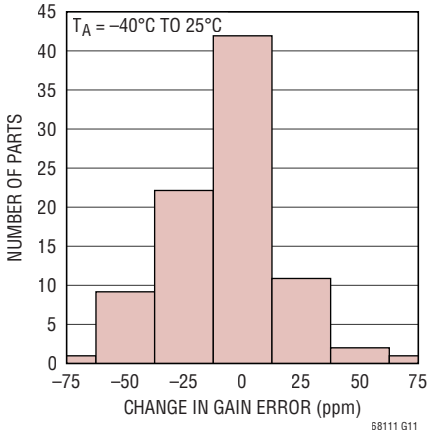


TYPICAL PERFORMANCE CHARACTERISTICS

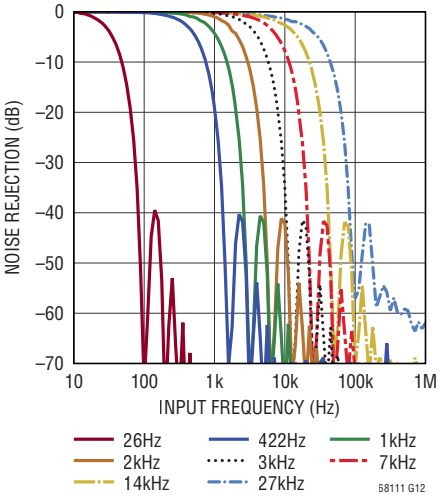
Measurement Gain Error Hysteresis, Hot



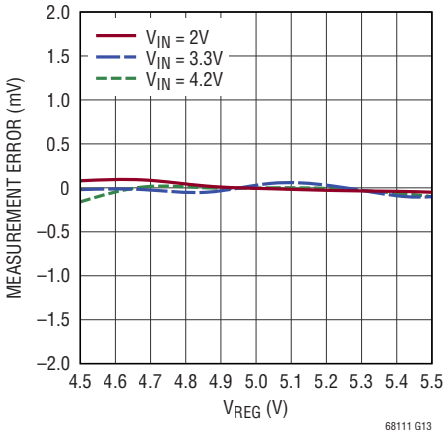
Measurement Gain Error Hysteresis, Cold



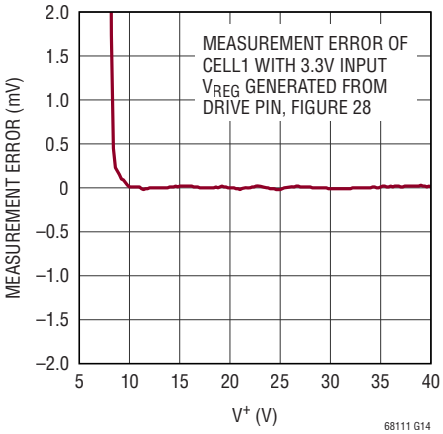
Noise Filter Response



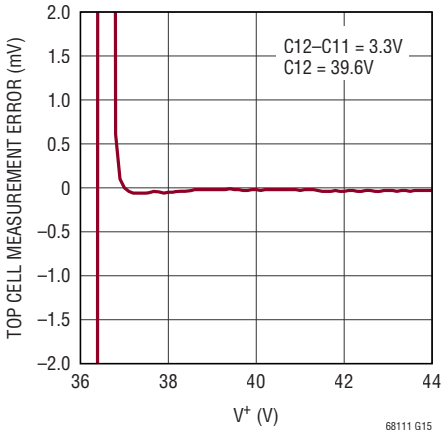
Measurement Error vs VREG



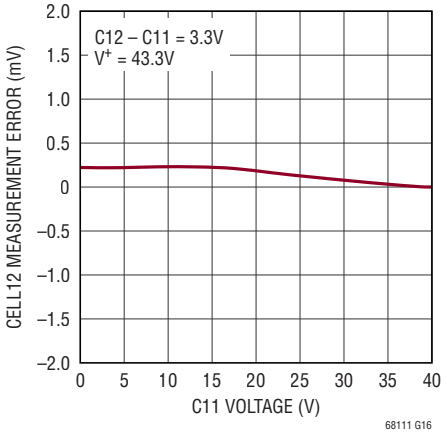
Measurement Error vs V+



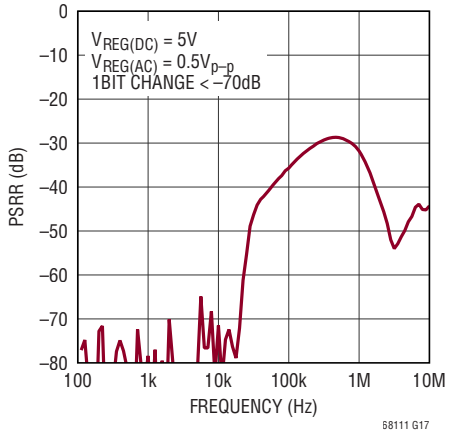
Top Cell Measurement Error vs V+



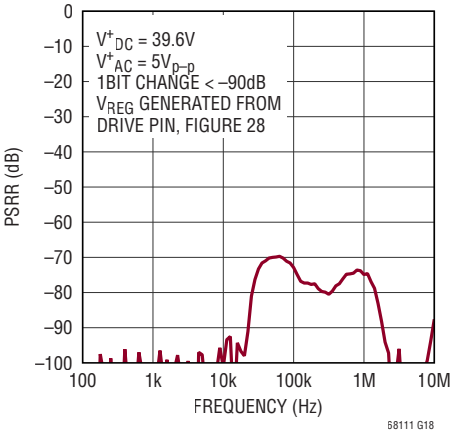
Measurement Error vs Common Mode Voltage



Measurement Error Due to a V_{REG} AC Disturbance

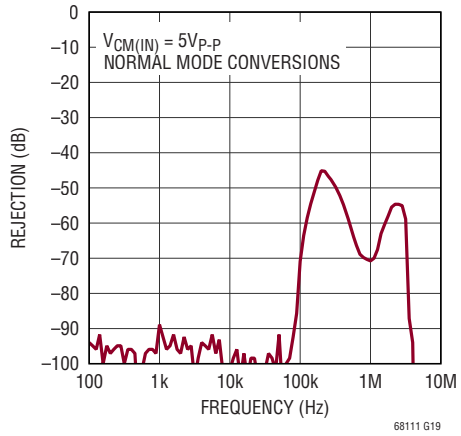


Measurement Error Due to a V+ AC Disturbance

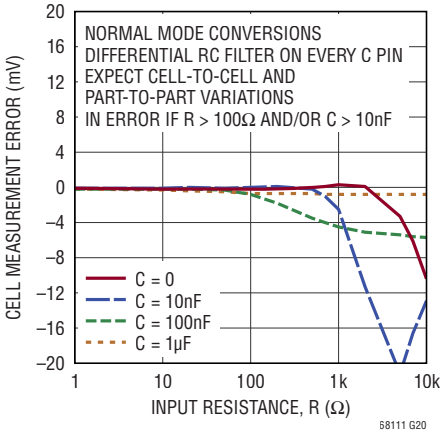


TYPICAL PERFORMANCE CHARACTERISTICS

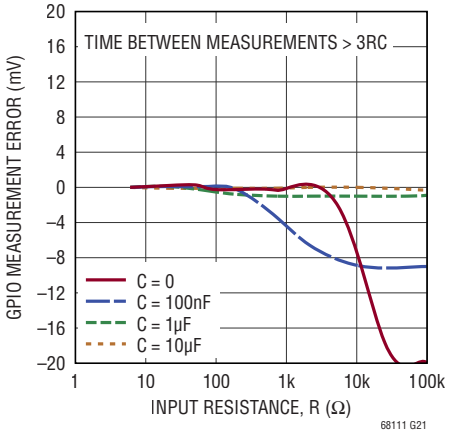
Measurement Error CMRR vs Frequency



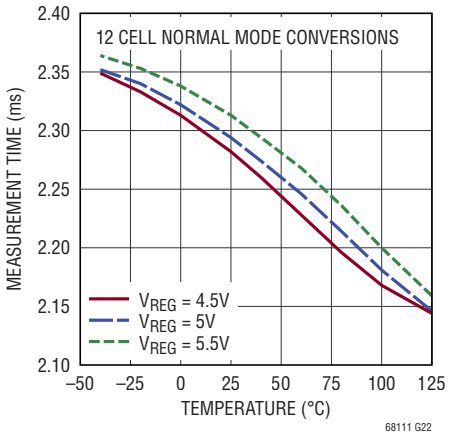
Cell Measurement Error vs Input RC Values



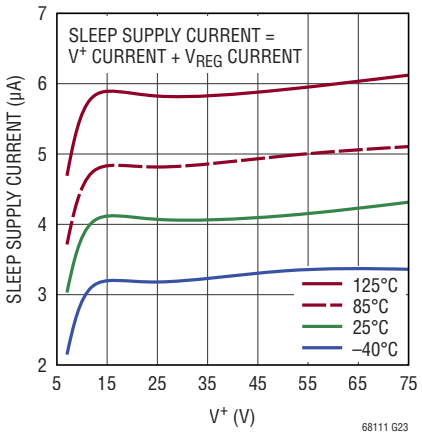
GPIO Measurement Error vs Input RC Values



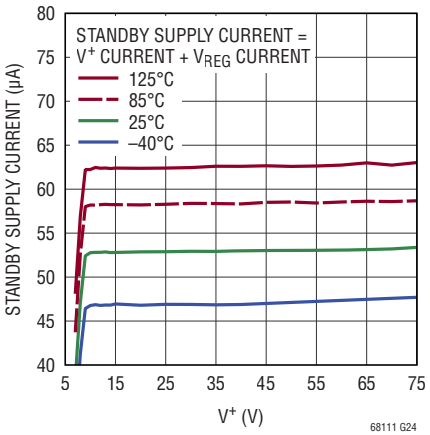
Measurement Time vs Temperature



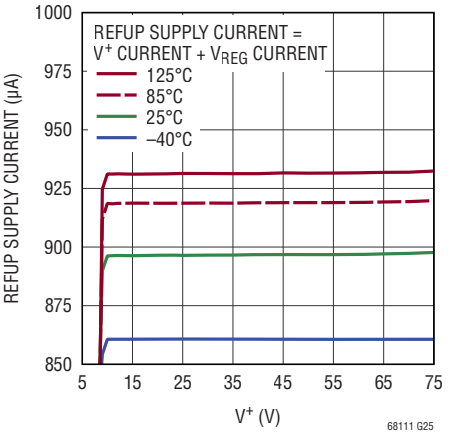
Sleep Supply Current vs V⁺



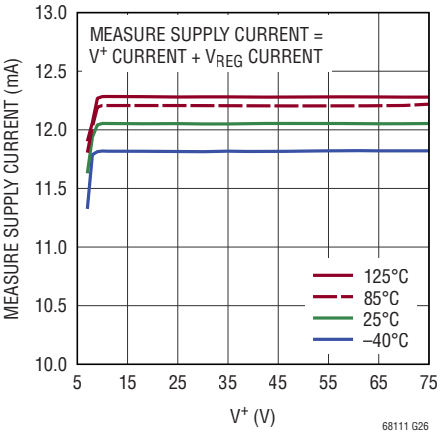
Standby Supply Current vs V⁺



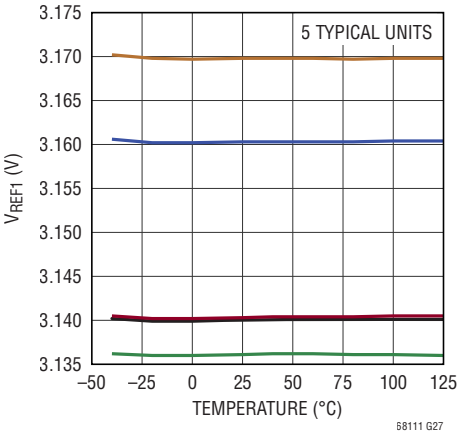
REFUP Supply Current vs V⁺



Measure Supply Current vs V⁺

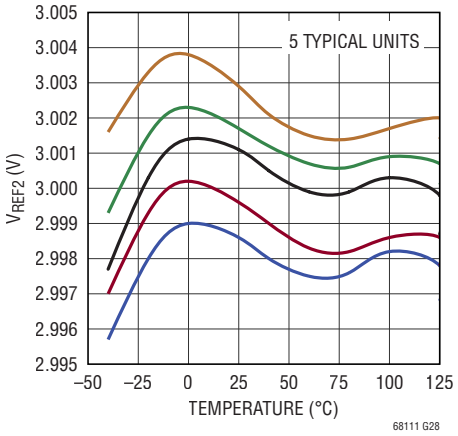


V_{REF1} vs Temperature

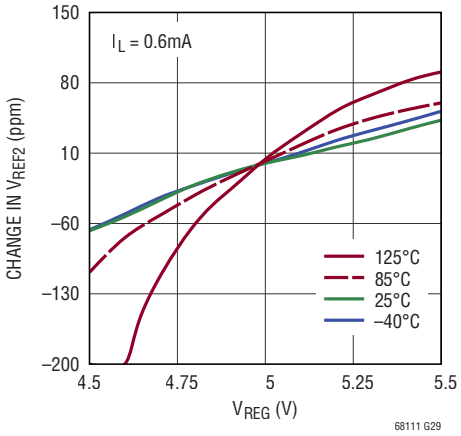


TYPICAL PERFORMANCE CHARACTERISTICS

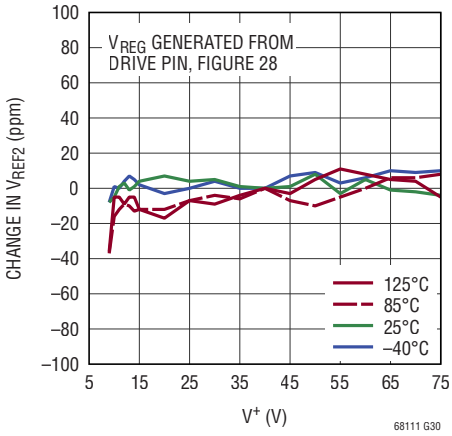
V_{REF2} vs Temperature



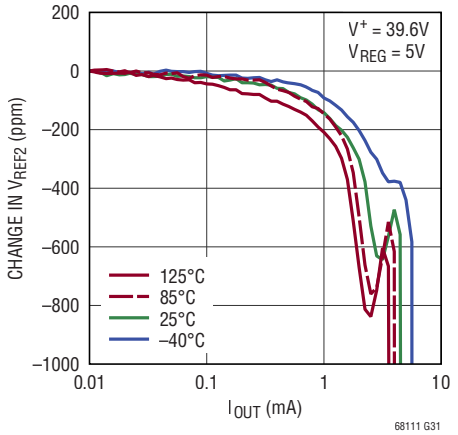
V_{REF2} V_{REG} Line Regulation



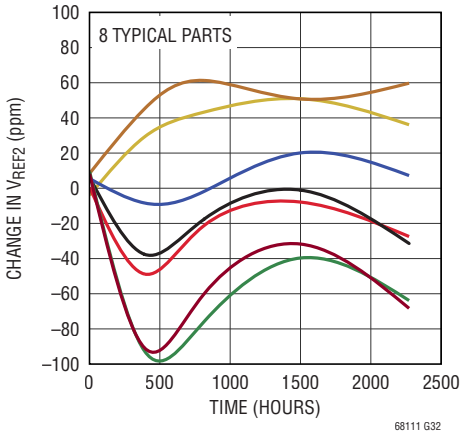
V_{REF2} V^+ Line Regulation



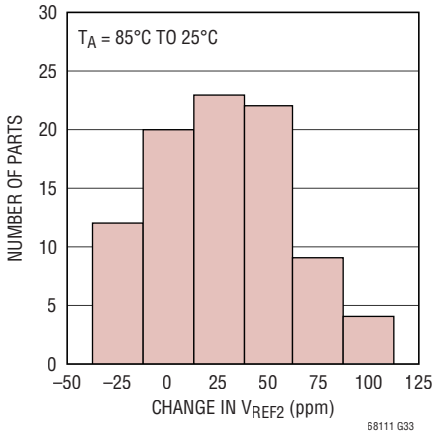
V_{REF2} Load Regulation



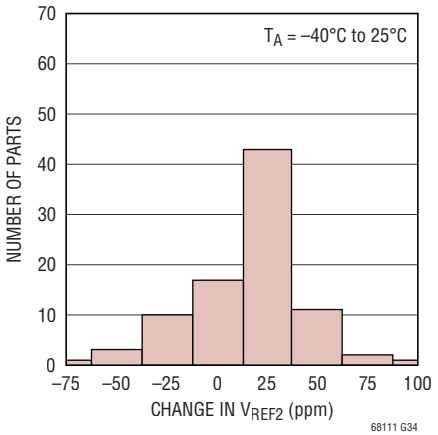
V_{REF2} Long-Term Drift



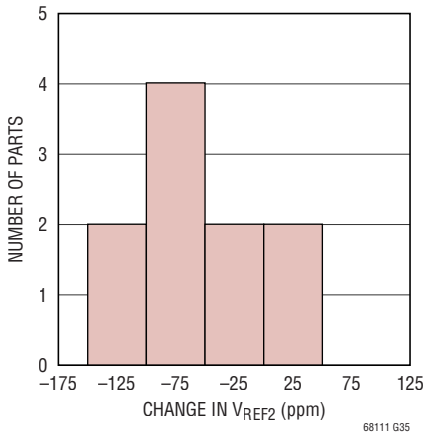
V_{REF2} Hysteresis, Hot



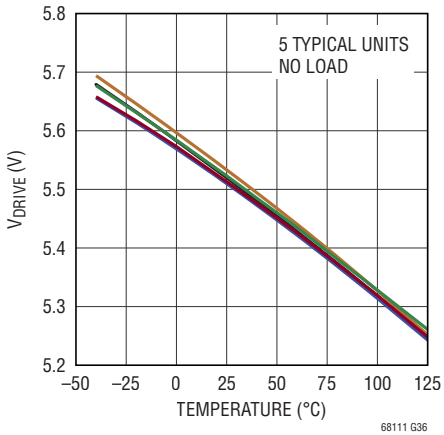
V_{REF2} Hysteresis, Cold



V_{REF2} Change Due to IR Reflow

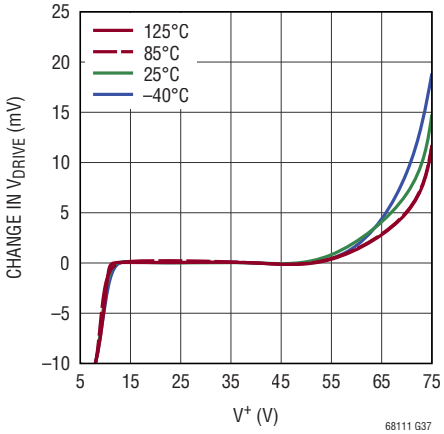


V_{DRIVE} vs Temperature

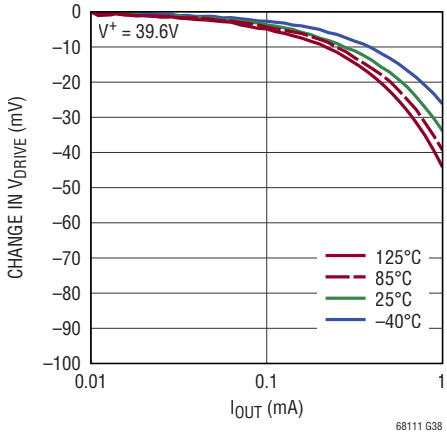


TYPICAL PERFORMANCE CHARACTERISTICS

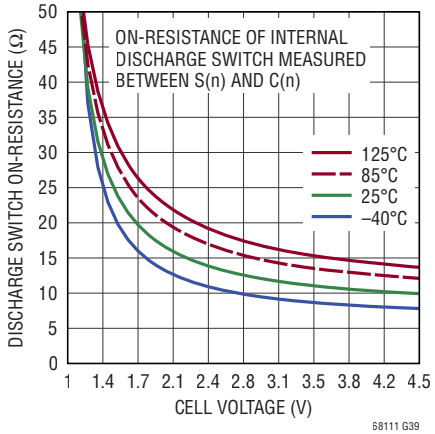
V_{DRIVE} V^+ Line Regulation



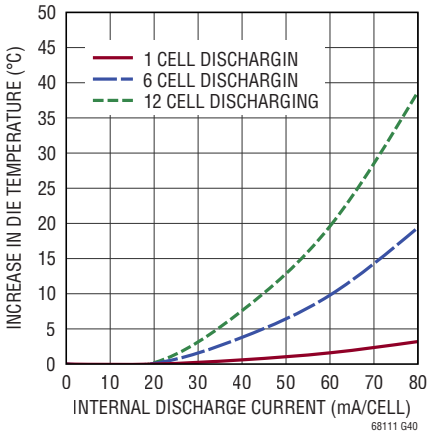
V_{DRIVE} Load Regulation



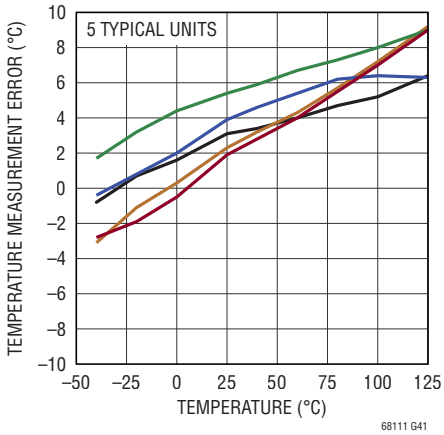
Discharge Switch On-Resistance vs Cell Voltage



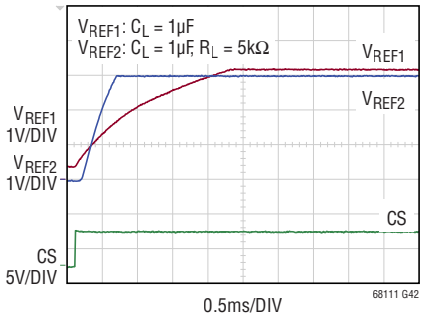
Internal Die Temperature Increase vs Discharge Current



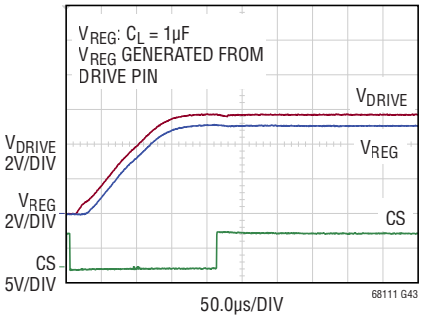
Internal Die Temperature Measurement Error vs Temperature



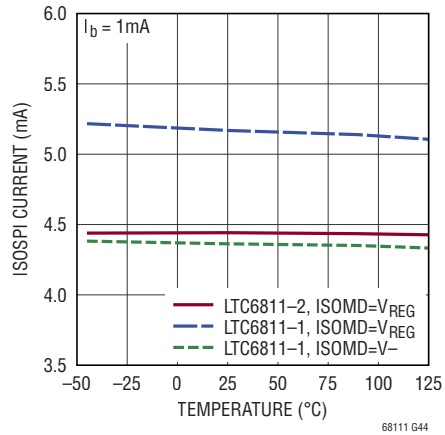
V_{REF1} and V_{REF2} Power-Up



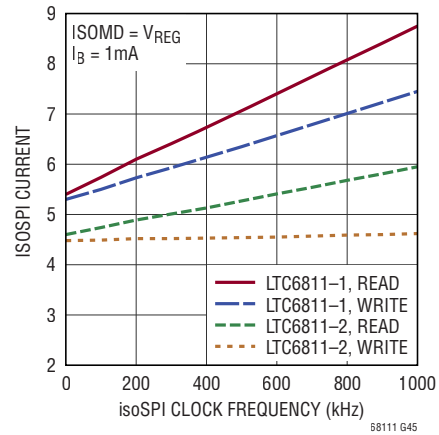
V_{REG} and V_{DRIVE} Power-Up



isoSPI Current (READY) vs Temperature

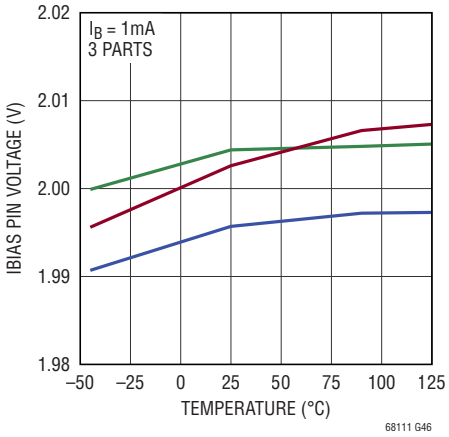


isoSPI Current (ACTIVE) vs isoSPI Clock Frequency

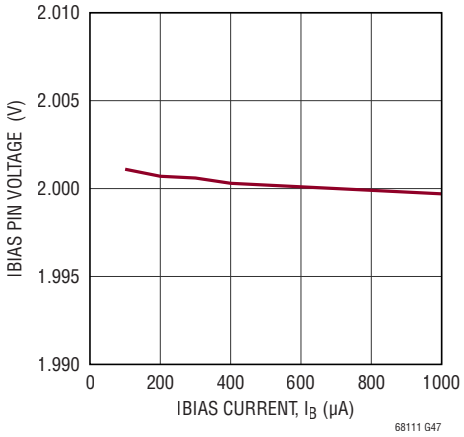


TYPICAL PERFORMANCE CHARACTERISTICS

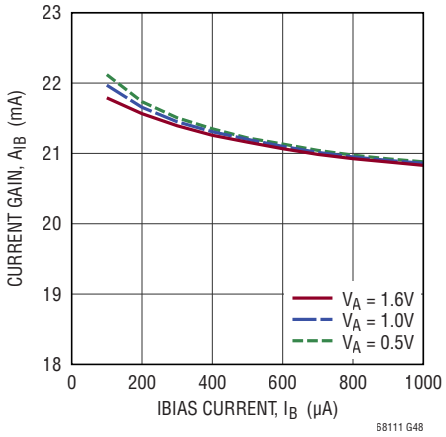
IBIAS Voltage vs Temperature



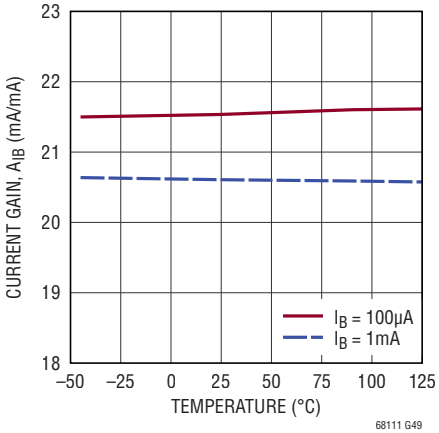
IBIAS Voltage Load Regulation



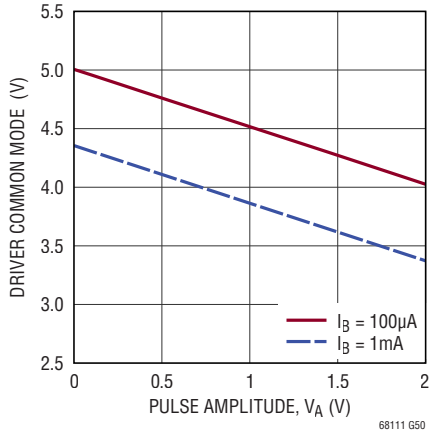
isoSPI Driver Current Gain (Port A/Port B) vs IBIAS Current



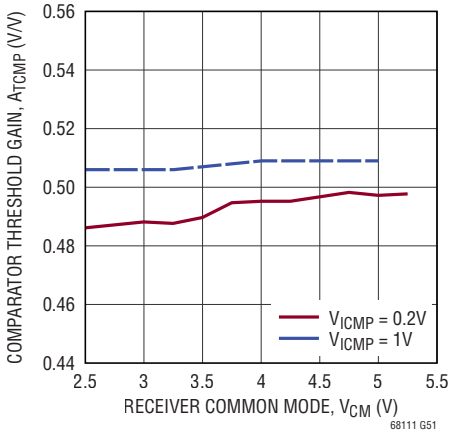
isoSPI Driver Current Gain (Port A/Port B) vs Temperature



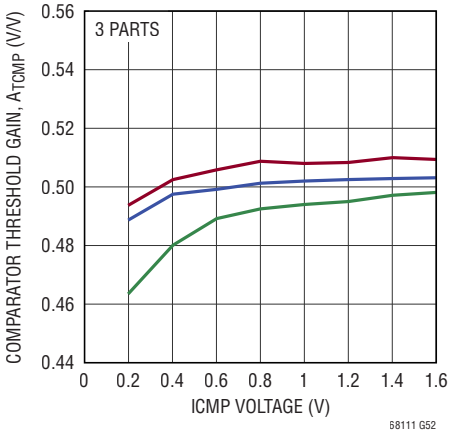
isoSPI Driver Common Mode Voltage (Port A/Port B) vs Pulse Amplitude



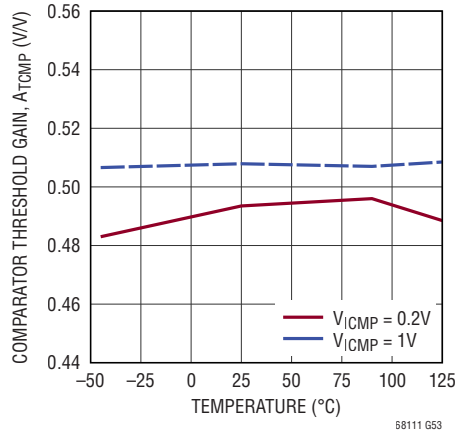
isoSPI Comparator Threshold Gain (Port A/Port B) vs IBIAS Current



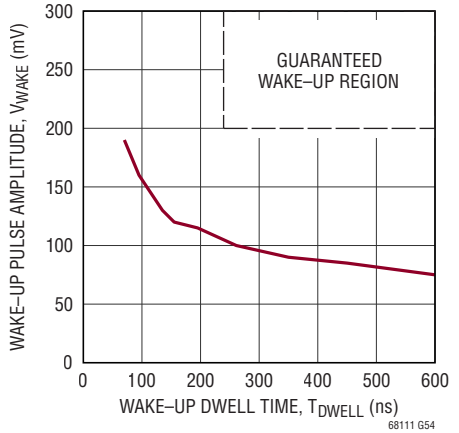
isoSPI Comparator Threshold Gain (Port A/Port B) vs ICMP Voltage



isoSPI Comparator Threshold Gain (Port A/Port B) vs Temperature



Typical Wake-Up Pulse Amplitude (Port A) vs Dwell Time



PIN FUNCTIONS

C0 to C12: Cell Inputs.

S1 to S12: Balance Inputs/Outputs. 12 internal N-MOSFETs are connected between S(n) and C(n – 1) for discharging cells.

V^+: Positive Supply Pin.

V^-: Negative Supply Pins. The V^- pins must be shorted together, external to the IC.

V_{REF2}: Buffered 2nd Reference Voltage for Driving Multiple 10k Thermistors. Bypass with an external 1µF capacitor.

V_{REF1}: ADC Reference Voltage. Bypass with an external 1µF capacitor. No DC loads allowed.

GPIO[1:5]: General Purpose I/O. Can be used as digital inputs or digital outputs, or as analog inputs with a measurement range from V^- to 5V. GPIO[3:5] can be used as an I^2C or SPI port.

DTEN: Discharge Timer Enable. Connect this pin to V_{REG} to enable the discharge timer.

DRIVE: Connect the base of an NPN to this pin. Connect the collector to V^+ and the emitter to V_{REG}.

V_{REG}: 5V Regulator Input. Bypass with an external 1µF capacitor.

ISOMD: Serial Interface Mode. Connecting ISOMD to V_{REG} configures pins 41 to 44 of the LTC6811 for 2-wire isolated interface (isoSPI) mode. Connecting ISOMD to V^- configures the LTC6811 for 4-wire SPI mode.

WDT: Watchdog Timer Output Pin. This is an open drain NMOS digital output. It can be left unconnected or connected with a 1M resistor to V_{REG}. If the LTC6811 does not receive a valid command within 2 seconds, the watchdog timer circuit will reset the LTC6811 and the WDT pin will go high impedance.

Serial Port Pins

	LTC6811-1 (DAISY-CHAINABLE)		LTC6811-2 (ADDRESSABLE)	
	ISOMD = V_{REG}	**ISOMD = V^-**	**ISOMD = V_{REG}**	**ISOMD = V^-**
PORT B (Pins 45 to 48)	IPB	IPB	A3	A3
	IMB	IMB	A2	A2
	ICMP	ICMP	A1	A1
	IBIAS	IBIAS	A0	A0
PORT A (Pins 41 to 44)	(NC)	SDO	IBIAS	SDO
	(NC)	SDI	ICMP	SDI
	IPA	SCK	IPA	SCK
	IMA	CSB	IMA	CSB

CSB, SCK, SDI, SDO: 4-Wire Serial Peripheral Interface (SPI). Active low chip select (CSB), serial clock (SCK) and serial data in (SDI) are digital inputs. Serial data out (SDO) is an open drain NMOS output pin. SDO requires a 5K pull-up resistor.

A0 to A3: Address Pins. These digital inputs are connected to V_{REG} or V^- to set the chip address for addressable serial commands.

IPA, IMA: Isolated 2-Wire Serial Interface Port A. IPA (plus) and IMA (minus) are a differential input/output pair.

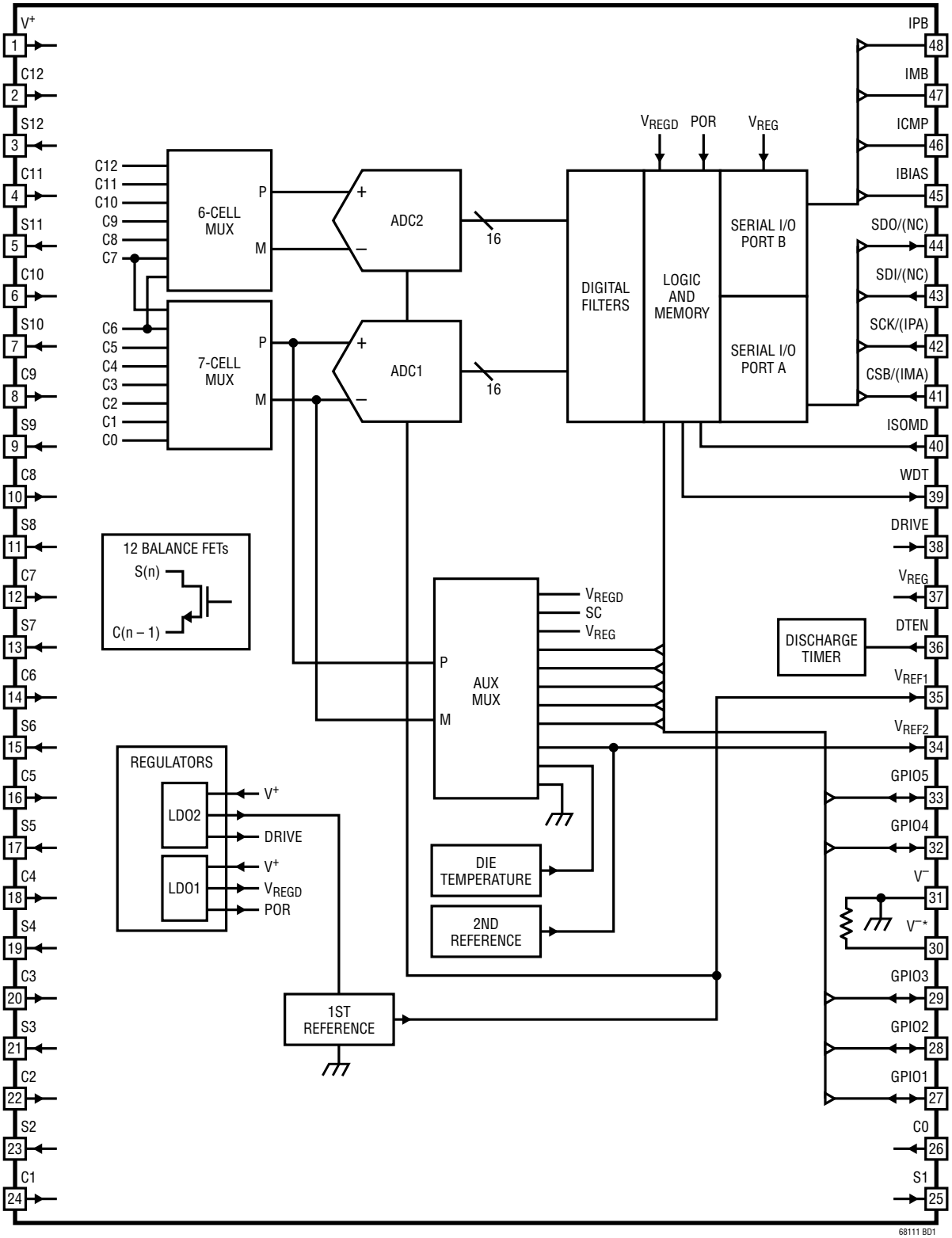
IPB, IMB: Isolated 2-Wire Serial Interface Port B. IPB (plus) and IMB (minus) are a differential input/output pair.

IBIAS: Isolated Interface Current Bias. Tie IBIAS to V^- through a resistor divider to set the interface output current level. When the isoSPI interface is enabled, the IBIAS pin voltage is 2V. The IPA/IMA or IPB/IMB output current drive is set to 20 times the current, I_B, sourced from the IBIAS pin.

ICMP: Isolated Interface Comparator Voltage Threshold Set. Tie this pin to the resistor divider between IBIAS and V^- to set the voltage threshold of the isoSPI receiver comparators. The comparator thresholds are set to half the voltage on the ICMP pin.

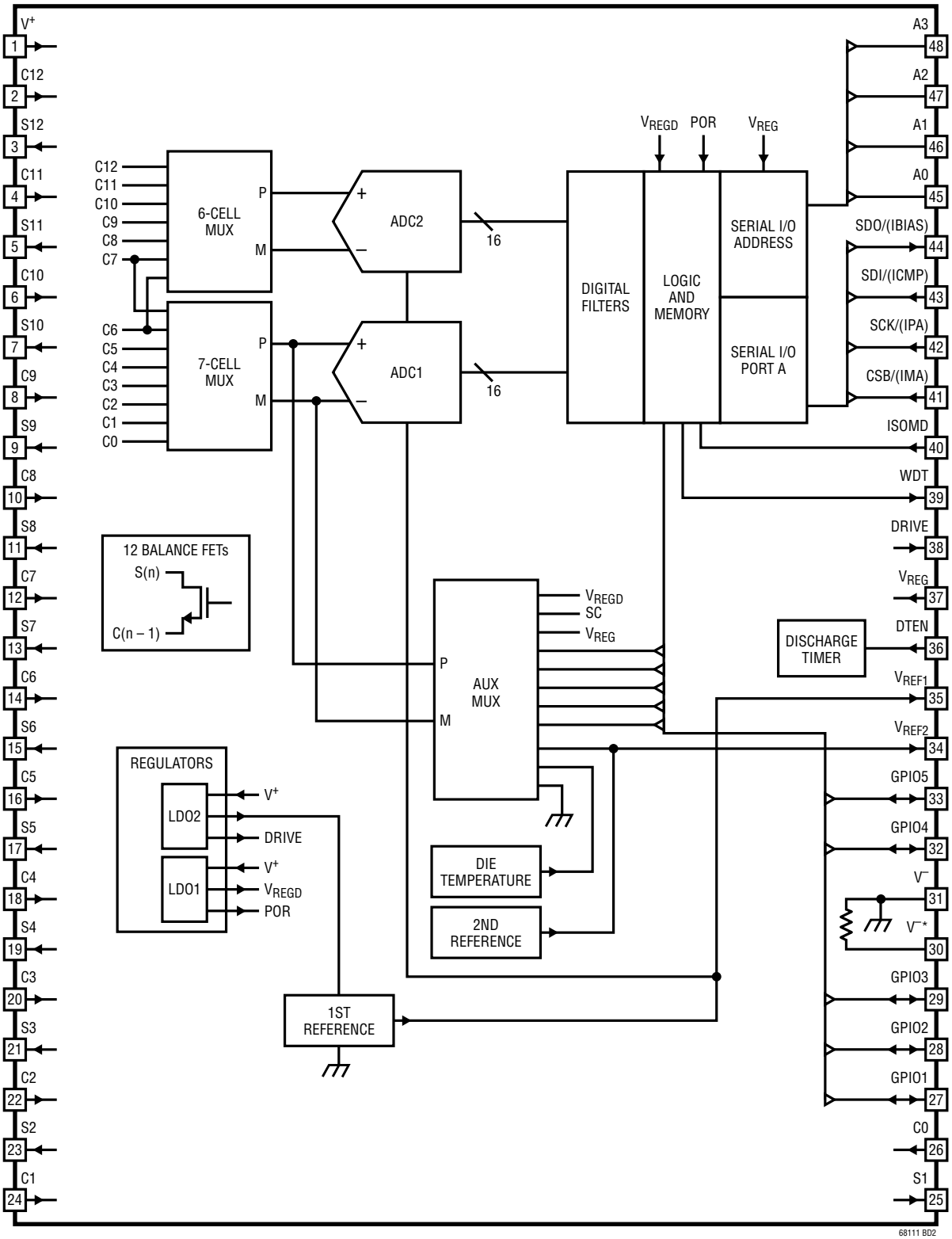
BLOCK DIAGRAM

LTC6811-1



BLOCK DIAGRAM

LTC6811-2



DIFFERENCES BETWEEN THE LTC6804 AND THE LTC6811

The newer LTC6811 is pin compatible and backwards software compatible with the older LTC6804. Users of the LTC6804 should review the following tables of product differences before upgrading existing designs.

Additional LTC6811 Feature	Benefit	Relevant Data Sheet Section(s)
Eight choices of ADC speed vs resolution. The LTC6804 has six choices.	Flexibility for noise filtering.	"ADC Modes" for a description and MD[1,0] Bits in Table 39.
Each discharge control pin (S pin) can have a unique duty cycle.	Improved cell balancing.	"S Pin Pulse Width Modulation for Cell Balancing" for a description and PWMx[x] bits in Table 51.
Measure Cell 7 with both ADCs simultaneously using the ADOL command.	Improved way to check that ADC2 is as accurate as ADC1.	"Overlap Cell Measurement (ADOL Command)"
Sum of Cells measurement has higher accuracy.	Improved way to check that the individual cell measurements are correct.	"Measuring Internal Device Parameters (ADSTAT Command)"
The new ADCVSC command measures the Sum of Cells and the individual cells at the same time.	Reduces the influence of noise on the accuracy of the Sum of Cells measurement.	"Measuring Cell Voltages and Sum of Cells (ADCVSC Command)"
Auxiliary measurements are processed with 2 digital filters simultaneously.	Checks that the digital filters are free of faults.	"Auxiliary (GPIO) Measurements with Digital Redundancy (ADAXD Command)" and "Measuring Internal Device Parameters with Digital Redundancy (ADSTATD Command)"
The S pin has a stronger PMOS pull-up transistor.	Reduces the possibility that board leakage can turn on discharge circuits.	"Cell Balancing with External Transistors"
The 2nd voltage reference has improved specifications.	Improved V_{REF2} specifications mean improved diagnostics for safety.	"Accuracy Check"
The LTC6811 supports daisy-chain polling.	Easier ADC communications.	"Polling Methods"
Commands to control the LT8584 active balance IC.	Easier to program the LT8584.	"S Pin Pulsing Using the S Control Register Group" for a description and SCTLx[x] bits in Table 50.

LTC6811 Restriction vs. LTC6804	Impact	Relevant Data Sheet Section(s)
The ABS MAX specifications for the C pins have changed.	The ABS MAX voltage between input pins, C(n) to C(n – 1), is 8V for both the LTC6804 and LTC6811. In addition, for the LTC6804, the AVERAGE voltage between the input pins from C12 to C8, C8 to C4, and C4 to C0 must be less than 6.25V. For the LTC6811, the AVERAGE voltage between the input pins from C12 to C9, C9 to C6, C6 to C3, and C3 to C0, must be less than 7.0V.	C12 to C9, C9 to C6, C6 to C3 and C3 to C0 in "Absolute Maximum Ratings"
The ABS MAX specifications for the C pins have changed.	If V^+ is powered from a separate supply (not directly powered from the battery stack), the V^+ supply voltage must be less than (50V + C6). If V^+ is powered from the battery stack (ie. V^+ = C12), this restriction has no impact since the maximum voltage between C6–C12 is already restricted to 42V as noted above.	C12 to C9, C9 to C6, C6 to C3 and C3 to C0 in "Absolute Maximum Ratings"
There is now an Operating Max voltage specification for V^+ to C6.	If V^+ is powered from a separate supply (not directly powered from the battery stack), the V^+ supply voltage must be less than (40V + C6) to achieve the TME specifications listed in the "Electrical Characteristics" table.	V^+ to C6 Voltage in "Electrical Characteristics"

OPERATION

STATE DIAGRAM

The operation of the LTC6811 is divided into two separate sections: the Core circuit and the isoSPI circuit. Both sections have an independent set of operating states, as well as a shutdown timeout.

CORE LTC6811 STATE DESCRIPTIONS

SLEEP State

The reference and ADCs are powered down. The watchdog timer (see Watchdog and Discharge Timer) has timed out. The discharge timer is either disabled or timed out. The supply currents are reduced to minimum levels. The isoSPI ports will be in the IDLE state. The Drive pin is 0V.

If a WAKEUP signal is received (see Waking Up the Serial Interface), the LTC6811 will enter the STANDBY state.

STANDBY State

The reference and the ADCs are off. The watchdog timer and/or the discharge timer is running. The DRIVE pin powers the V_{REG} pin to 5V through an external transistor. (Alternatively, V_{REG} can be powered by an external supply).

When a valid ADC command is received or the REFON bit is set to 1 in the Configuration Register Group, the IC pauses for t_{REFUP} to allow for the reference to power up and then enters either the REFUP or MEASURE state. Otherwise, if no valid commands are received for t_{SLEEP} (when both the watchdog and discharge timer have expired), the LTC6811 returns to the SLEEP state. If the discharge timer is disabled, only the watchdog timer is relevant.

REFUP State

To reach this state the REFON bit in the Configuration Register Group must be set to 1 (using the WRCFGA command, see Table 38). The ADCs are off. The reference is powered up so that the LTC6811 can initiate ADC conversions more quickly than from the STANDBY state.

When a valid ADC command is received, the IC goes to the MEASURE state to begin the conversion. Otherwise, the LTC6811 will return to the STANDBY state when the REFON bit is set to 0, either manually (using WRCFGA command) or automatically when the watchdog timer expires (the LTC6811 will then move straight into the SLEEP state if both timers are expired).

MEASURE State

The LTC6811 performs ADC conversions in this state. The reference and ADCs are powered up.

After ADC conversions are complete, the LTC6811 will transition to either the REFUP or STANDBY state, depending on the REFON bit. Additional ADC conversions can be initiated more quickly by setting REFON = 1 to take advantage of the REFUP state.

Note: Non-ADC commands do not cause a Core state transition. Only an ADC conversion or diagnostic commands will place the Core in the MEASURE state.

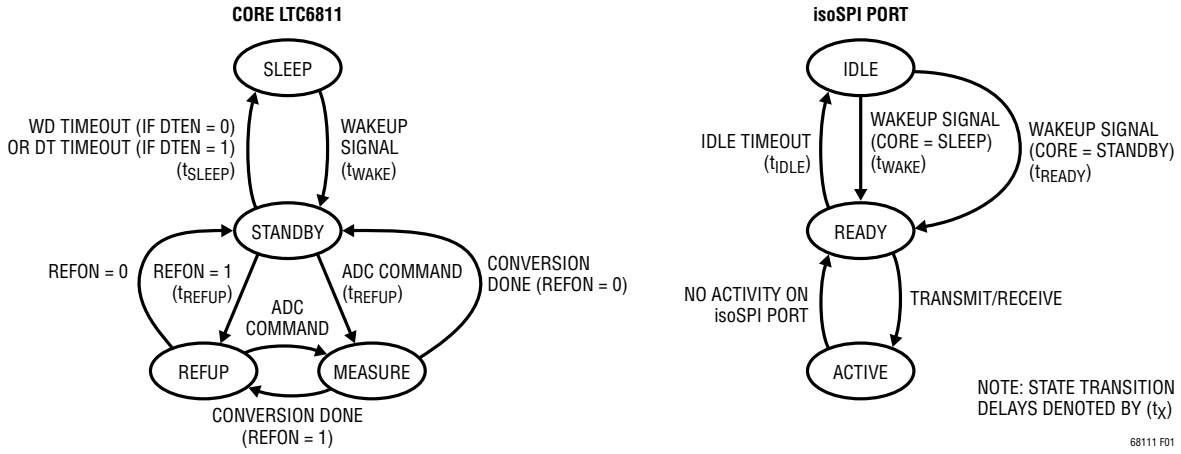


Figure 1. LTC6811 Operation State Diagram

OPERATION

isoSPI STATE DESCRIPTIONS

Note: The LTC6811-1 has two isoSPI ports (A and B), for daisy-chain communication. The LTC6811-2 has only one isoSPI port (A), for parallel-addressable communication.

IDLE State

The isoSPI ports are powered down.

When isoSPI Port A receives a WAKEUP signal (see Waking Up the Serial Interface), the isoSPI enters the READY state. This transition happens quickly (within t_{READY}) if the Core is in the STANDBY state because the DRIVE and V_{REG} pins are already biased up. If the Core is in the SLEEP state when the isoSPI receives a WAKEUP signal, the part transitions to the READY state within t_{WAKE}.

READY State

The isoSPI port(s) are ready for communication. Port B is enabled only for LTC6811-1, and is not present on the LTC6811-2. The serial interface current in this state depends on if the part is LTC6811-1 or LTC6811-2, the status of the ISOMD pin and $R_{BIAS} = R_{B1} + R_{B2}$ (the external resistors tied to the IBIAS pin).

If there is no activity (i.e. no WAKEUP signal) on Port A for greater than t_{IDLE} = 5.5ms, the LTC6811 goes to the IDLE state. When the serial interface is transmitting or receiving data the LTC6811 goes to the ACTIVE state.

ACTIVE State

The LTC6811 is transmitting/receiving data using one or both of the isoSPI ports. The serial interface consumes maximum power in this state. The supply current increases with clock frequency as the density of isoSPI pulses increases.

POWER CONSUMPTION

The LTC6811 is powered via two pins: V^+ and V_{REG}. The V^+ input requires voltage greater than or equal to the top cell voltage minus 0.3V, and it provides power to the high voltage elements of the core circuitry. The V_{REG} input requires 5V and provides power to the remaining core circuitry and the isoSPI circuitry. The V_{REG} input can be powered through an external transistor, driven by the regulated DRIVE output pin. Alternatively, V_{REG} can be powered by an external supply.

The power consumption varies according to the operational states. Table 1 and Table 2 provide equations to approximate the supply pin currents in each state. The V^+ pin current depends only on the Core state. However, the V_{REG} pin current depends on both the Core state and isoSPI state, and can therefore be divided into two components. The isoSPI interface draws current only from the V_{REG} pin.

$$I_{REG} = I_{REG(Core)} + I_{REG(isoSPI)}$$

Table 1. Core Supply Current

STATE		I_{V+}	$I_{REG(CORE)}$
SLEEP	V_{REG} = 0V	4.1µA	0µA
	V_{REG} = 5V	1.9µA	2.2µA
STANDBY		13µA	39µA
REFUP		490µA	430µA
MEASURE		490µA	11.5mA

In the SLEEP state the V_{REG} pin will draw approximately 2.2µA if powered by an external supply. Otherwise, the V^+ pin will supply the necessary current.

ADC OPERATION

There are two ADCs inside the LTC6811. The two ADCs operate simultaneously when measuring twelve cells. Only one ADC is used to measure the general purpose inputs. The following discussion uses the term ADC to refer to one or both ADCs, depending on the operation being performed. The following discussion will refer to ADC1 and ADC2 when it is necessary to distinguish between the two circuits, in timing diagrams, for example.

ADC Modes

The ADCOPT bit (CFGR0[0]) in the Configuration Register Group and the mode selection bits MD[1:0] in the conversion command together provide eight modes of operation for the ADC, which correspond to different oversampling ratios (OSR). The accuracy and timing of these modes are summarized in Table 3. In each mode, the ADC first measures the inputs, and then performs a calibration of each channel. The names of the modes are based on the –3dB bandwidth of the ADC measurement.

OPERATION

Table 2. isoSPI Supply Current Equations

isoSPI STATE	DEVICE	ISOMD CONNECTION	$I_{REG(isoSPI)}$
IDLE	LTC6811-1/LTC6811-2	N/A	0mA
READY	LTC6811-1	V_{REG}	$2.2mA + 3 \bullet I_B$
		V^-	$1.5mA + 3 \bullet I_B$
	LTC6811-2	V_{REG}	$1.5mA + 3 \bullet I_B$
		V^-	0mA
ACTIVE	LTC6811-1	V_{REG}	Write: $2.5mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$ Read: $2.5mA + \left(3 + 20 \bullet \frac{100ns \bullet 1.5}{t_{CLK}}\right) \bullet I_B$
		V^-	$1.8mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$
	LTC6811-2	V_{REG}	Write: $1.8mA + 3 \bullet I_B$ Read: $1.8mA + \left(3 + 20 \bullet \frac{100ns \bullet 0.5}{t_{CLK}}\right) \bullet I_B$
		V^-	0mA

Note: $I_B = V_{BIAS}/(R_{B1} + R_{B2})$

Table 3. ADC Filter Bandwidth and Accuracy

MODE	–3dB FILTER BW	–40dB FILTER BW	TME SPEC AT 3.3V, 25°C	TME SPEC AT 3.3V,–40°C, 125°C
27kHz (Fast Mode)	27kHz	84kHz	±4.7mV	±4.7mV
14kHz	13.5kHz	42kHz	±4.7mV	±4.7mV
7kHz (Normal Mode)	6.8kHz	21kHz	±1.2mV	±2.2mV
3kHz	3.4kHz	10.5kHz	±1.2mV	±2.2mV
2kHz	1.7kHz	5.3kHz	±1.2mV	±2.2mV
1kHz	845Hz	2.6kHz	±1.2mV	±2.2mV
422Hz	422Hz	1.3kHz	±1.2mV	±2.2mV
26Hz (Filtered Mode)	26Hz	82Hz	±1.2mV	±2.2mV

Note: TME is the total measurement error.

Mode 7kHz (Normal):

In this mode, the ADC has high resolution and low TME (total measurement error). This is considered the normal operating mode because of the optimum combination of speed and accuracy.

Mode 27kHz (Fast):

In this mode, the ADC has maximum throughput but has some increase in TME (total measurement error). So this mode is also referred to as the fast mode. The increase in speed comes from a reduction in the oversampling ratio. This results in an increase in noise and average measurement error.

Mode 26Hz (Filtered):

In this mode, the ADC digital filter –3dB frequency is lowered to 26Hz by increasing the OSR. This mode is also referred to as the filtered mode due to its low –3dB frequency. The accuracy is similar to the 7kHz (Normal) mode with lower noise.

OPERATION

Modes 14kHz, 3kHz, 2kHz, 1kHz and 422Hz:

Modes 14kHz, 3kHz, 2kHz, 1kHz and 422Hz provide additional options to set the ADC digital filter –3dB frequency at 13.5kHz, 3.4kHz, 1.7kHz, 845Hz and 422Hz respectively. The accuracy of the 14kHz mode is similar to the 27kHz (fast) mode. The accuracy of 3kHz, 2kHz, 1kHz and 422Hz modes is similar to the 7kHz (normal) mode.

The filter bandwidths and the conversion times for these modes are provided in Table 3 and Table 5. If the Core is in STANDBY state, an additional t_{REFUP} time is required to power up the reference before beginning the ADC conversions. The reference can remain powered up between ADC conversions if the REFON bit in the Configuration Register Group is set to 1 so the Core is in REFUP state after a delay t_{REFUP}. Then, the subsequent ADC commands will not have the t_{REFUP} delay before beginning ADC conversions.

ADC Range and Resolution

The C inputs and GPIO inputs have the same range and resolution. The ADC inside the LTC6811 has an approximate range from –0.82V to +5.73V. Negative readings are rounded to 0V. The format of the data is a 16-bit unsigned integer where the LSB represents 100µV. Therefore, a reading of 0x80E8 (33,000 decimal) indicates a measurement of 3.3V.

Delta-Sigma ADCs have quantization noise which depends on the input voltage, especially at low oversampling ratios (OSR), such as in FAST mode. In some of the ADC modes, the quantization noise increases as the input voltage approaches the upper and lower limits of the ADC range. For example, the total measurement noise versus input voltage in normal and filtered modes is shown in Figure 2

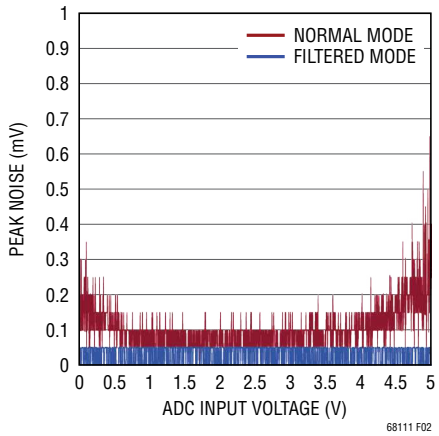


Figure 2. Measurement Noise vs Input Voltage

The specified range of the ADC is 0V to 5V. In Table 4, the precision range of the ADC is arbitrarily defined as 0.5V to 4.5V. This is the range where the quantization noise is relatively constant even in the lower OSR modes (see Figure 2). Table 4 summarizes the total noise in this range for all eight ADC operating modes. Also shown is the noise free resolution. For example, 14-bit noise free resolution in normal mode implies that the top 14 bits will be noise free with a DC input, but that the 15th and 16th least significant bits (LSB) will flicker.

Table 4. ADC Range and Resolution

MODE	FULL RANGE[1]	SPECIFIED RANGE	PRECISION RANGE[2]	LSB	FORMAT	MAX NOISE	NOISE FREE RESOLUTION[3]
27kHz (fast)	–0.8192V to 5.7344V	0V to 5V	0.5V to 4.5V	100µV	Unsigned 16 Bits	±4mV$_{P-P}$	10 Bits
14kHz						±1mV$_{P-P}$	12 Bits
7kHz (normal)						±250µV$_{P-P}$	14 Bits
3kHz						±150µV$_{P-P}$	14 Bits
2kHz						±100µV$_{P-P}$	15 Bits
1kHz						±100µV$_{P-P}$	15 Bits
422Hz						±100µV$_{P-P}$	15 Bits
26Hz (filtered)						±50µV$_{P-P}$	16 Bits

1. Negative readings are rounded to 0V.
2. PRECISION RANGE is the range over which the noise is less than MAX NOISE.
3. NOISE FREE RESOLUTION is a measure of the noise level within the PRECISION RANGE.

OPERATION

ADC Range vs Voltage Reference Value

Typical ADCs have a range which is exactly twice the value of the voltage reference, and the ADC measurement error is directly proportional to the error in the voltage reference. The LTC6811 ADC is not typical. The absolute value of V_{REF1} is trimmed up or down to compensate for gain errors in the ADC. Therefore, the ADC total measurement error (TME) specifications are superior to the V_{REF1} specifications. For example, the 25°C specification of the total measurement error when measuring 3.300V in 7kHz (normal) mode is ±1.2mV and the 25°C specification for V_{REF1} is 3.200V±100mV.

Measuring Cell Voltages (ADCV Command)

The ADCV command initiates the measurement of the battery cell inputs, pins C0 through C12. This command has options to select the number of channels to measure and the ADC mode. See the section on Commands for the ADCV command format.

Figure 3 illustrates the timing of the ADCV command which measures all twelve cells. After the receipt of the ADCV command to measure all 12 cells, ADC1 sequentially measures the bottom 6 cells. ADC2 sequentially measures the top 6 cells. After the cell measurements are complete, each channel is calibrated to remove any offset errors.

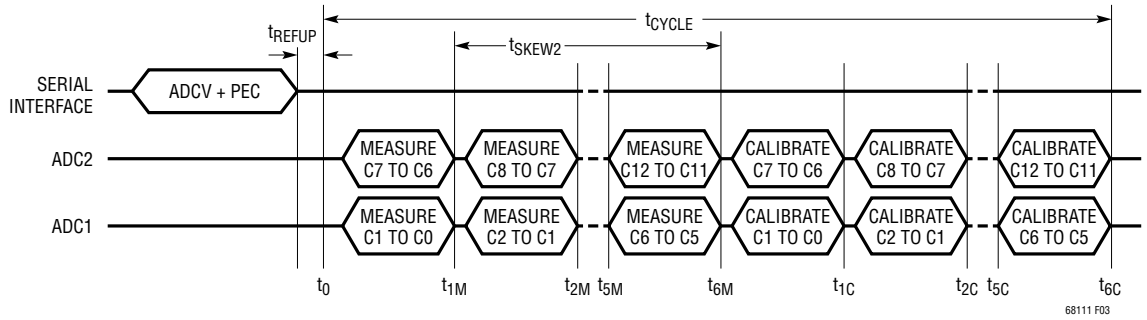


Figure 3. Timing for ADCV Command Measuring All 12 Cells

Table 5. Conversion Times for ADCV Command Measuring All 12 Cells in Different Modes

	CONVERSION TIMES (in µs)								
MODE	t_0	t_{1M}	t_{2M}	t_{5M}	t_{6M}	t_{1C}	t_{2C}	t_{5C}	t_{6C}
27kHz	0	57	103	243	290	432	568	975	1,113
14kHz	0	86	162	389	465	606	742	1,149	1,288
7kHz	0	144	278	680	814	1,072	1,324	2,080	2,335
3kHz	0	260	511	1,262	1,512	1,770	2,022	2,778	3,033
2kHz	0	493	976	2,425	2,908	3,166	3,418	4,175	4,430
1kHz	0	959	1,907	4,753	5,701	5,961	6,213	6,970	7,222
422Hz	0	1,890	3,769	9,407	11,287	11,547	11,799	12,555	12,807
26Hz	0	29,817	59,623	149,043	178,850	182,599	186,342	197,571	201,317

OPERATION

Table 5 shows the conversion times for the ADCV command measuring all 12 cells. The total conversion time is given by t_{6C} which indicates the end of the calibration step.

Figure 4 illustrates the timing of the ADCV command that measures only two cells.

Table 6 shows the conversion time for ADCV command measuring only 2 cells. t_{1C} indicates the total conversion time for this command.

Table 6. Conversion Times for ADCV Command Measuring Only 2 Cells in Different Modes

	CONVERSION TIMES (in µs)		
MODE	**t_0**	**t_{1M}**	**t_{1C}**
27kHz	0	57	201
14kHz	0	86	230
7kHz	0	144	405
3kHz	0	240	501
2kHz	0	493	754
1kHz	0	959	1,219
422Hz	0	1,890	2,150
26Hz	0	29,817	33,568

Under/Over Voltage Monitoring

Whenever the C inputs are measured, the results are compared to undervoltage and overvoltage thresholds stored in memory. If the reading of a cell is above the overvoltage limit, a bit in memory is set as a flag. Similarly, measurement results below the undervoltage limit cause a flag to be set. The overvoltage and undervoltage thresholds are stored in the Configuration Register Group. The flags are stored in the Status Register Group B.

Auxiliary (GPIO) Measurements (ADAX Command)

The ADAX command initiates the measurement of the GPIO inputs. This command has options to select which GPIO input to measure (GPIO1-5) and which ADC mode. The ADAX command also measures the 2nd reference. There are options in the ADAX command to measure each GPIO and the 2nd reference separately or to measure all five GPIOs and the 2nd reference in a single command. See the section on Commands for the ADAX command format. All auxiliary measurements are relative to the V^- pin voltage. This command can be used to read external

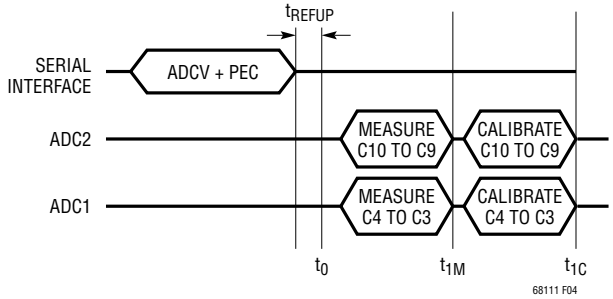


Figure 4. Timing for ADCV Command Measuring 2 Cells