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Ultralow Noise 0.35GHz to 6GHz Fractional-N Synthesizer

FEATURES

- **Low Noise Fractional-N PLL**
- **No ΔΣ Modulator Spurs**
- **18-Bit Fractional Denominator**
- **350MHz to 6GHz VCO Input Range**
- **–226dBc/Hz Normalized In-Band Phase Noise Floor**
- **–274dBc/Hz Normalized In-Band 1/f Noise**
- **–157dBc/Hz Wideband Output Phase Noise Floor**
- **Excellent Integer Boundary Spurious Performance**
- **Output Divider (1 to 6, 50% Duty Cycle)**
- **Output Buffer Muting**
- Charge Pump Supply from 3.15V to 5.25V
- Charge Pump Current from 1mA to 11.2mA
- Reference Input Frequency Up to 425MHz
- Fast Frequency Switching
- FracNWizard™ Software Design Tool Support

APPLICATIONS

- Wireless Basestations (LTE, WiMAX, W-CDMA, PCS)
- Broadband Wireless Access
- Microwave Data Links
- Military and Secure Radio
- Test and Measurement

DESCRIPTION

The LTC®6947 is a high performance, low noise, 6GHz phase-locked loop (PLL), including a reference divider, phase-frequency detector (PFD), ultralow noise charge pump, fractional feedback divider, and VCO output divider.

The fractional divider uses an advanced, 4th order ΔΣ modulator which provides exceptionally low spurious levels. This allows wide loop bandwidths, producing extremely low integrated phase noise values.

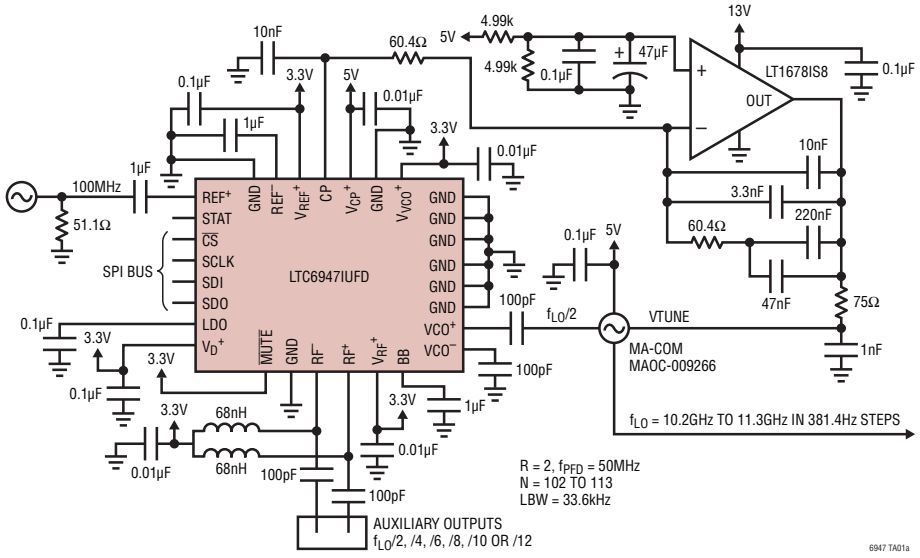
The programmable VCO output divider, with a range of 1 through 6, extends the output frequency range. The differential, low-noise output buffer has user-programmable output power ranging from –4.3dBm to +4.5dBm, and may be muted through either a digital input pin or software.

The ultralow noise charge pump contains selectable high and low voltage clamps useful for VCO monitoring, and also may be set to provide a $V^+/2$ bias.

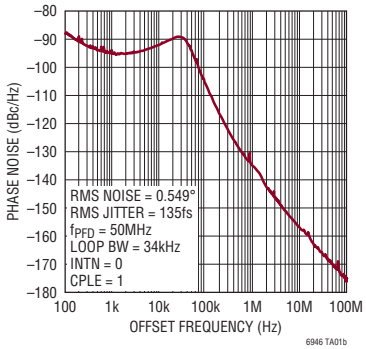
All device settings are controlled through a SPI-compatible serial port.

TYPICAL APPLICATION

11GHz Source for Satellite Communications



System Phase Noise, f_{RF} = 11.260GHz



ABSOLUTE MAXIMUM RATINGS

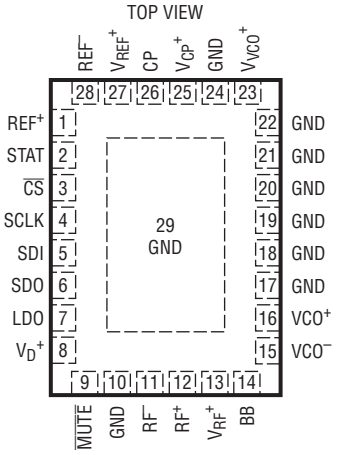
(Note 1)

Supply Voltages
- V^+ (V_{REF}^+, V_{RF}^+, V_{VCO}^+, V_D^+) to GND 3.6V
- V_{CP}^+ to GND 5.5V

Voltage on CP Pin ..... GND – 0.3V to V_{CP}^+ + 0.3V
Voltage on all other Pins ..... GND – 0.3V to V^+ + 0.3V
Operating Junction Temperature Range, T_J
- LTC6947I (Note 2) ..... –40°C to 105°C

Junction Temperature, T_{JMAX} ..... 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, $\theta_{JCbottom}$ = 7°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC6947IUFD#PBF	LTC6947IUFD#TRPBF	6947	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{VCO}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Inputs (REF^+, $REF^–$)							
f_{REF}	Input Frequency		●	10		425	MHz
V_{REF}	Input Signal Level	Single-Ended, 1µF AC-Coupling Capacitors	●	0.5	2	2.7	V_{P-P}
	Input Slew Rate		●	20			V/µs
	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.65	1.85	2.25	V
	Input Resistance	Differential	●	5.8	8.4	11.6	kΩ
	Input Capacitance	Differential			14		pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{VCO}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VCO Input (VCO^+, VCO^-)							
f_{VCO}	Input Frequency		●	350		6000	MHz
P_{VCOI}	Input Power Level	R_Z = 50Ω, Single-Ended	●	–8	0	6	dBm
	Input Resistance	Single-Ended, Each Input	●	94	132	161	Ω
RF Output (RF^+, RF^-)							
f_{RF}	Output Frequency		●	350		6000	MHz
O	Output Divider Range	All Integers Included	●	1		6	
	Output Duty Cycle				50		%
	Output Resistance	Single-Ended, Each Output to V_{RF}^+	●	100	136	175	Ω
P_{RF-SE}	Output Power, Single-Ended, f_{RF} = 900MHz	RFO[1:0] = 0, R_Z = 50Ω, LC Match	●	–9	–7.3	–5.5	dBm
		RFO[1:0] = 1, R_Z = 50Ω, LC Match	●	–6.1	–4.5	–2.8	dBm
		RFO[1:0] = 2, R_Z = 50Ω, LC Match	●	–2.9	–1.4	0.2	dBm
		RFO[1:0] = 3, R_Z = 50Ω, LC Match	●	0.1	1.5	3.0	dBm
	Output Power, Muted, f_{RF} = 900MHz	R_Z = 50Ω, Single-Ended, O = 2 to 6	●			–80	dBm
	Mute Enable Time		●			110	ns
	Mute Disable Time		●			170	ns
Phase/Frequency Detector							
f_{PFD}	Input Frequency	Integer mode	●			100	MHz
		Fractional mode					
		LDOEN = 0	●			76.1	MHz
		LDOV = 3, LDOEN = 1	●			66.3	MHz
		LDOV = 2, LDOEN = 1	●			56.1	MHz
		LDOV = 1, LDOEN = 1	●			45.9	MHz
		LDOV = 0, LDOEN = 1	●			34.3	MHz
Charge Pump							
I_{CP}	Output Current Range	8 Settings (See Table 6)		1		11.2	mA
	Output Current Source/Sink Accuracy	All Settings, V(CP) = V_{CP}^+/2				±6	%
	Output Current Source/Sink Matching	I_{CP} = 1.0mA to 2.8mA, V(CP) = V_{CP}^+/2				±3.5	%
		I_{CP} = 4.0mA to 11.2mA, V(CP) = V_{CP}^+/2				±2	%
	Output Current vs Output Voltage Sensitivity	(Note 3)	●		0.2	1.0	%/V
	Output Current vs Temperature	V(CP) = V_{CP}^+/2	●		170		ppm/°C
	Output Hi-Z Leakage Current	I_{CP} = 11.2mA, CPCLO = CPCHI = 0 (Note 3)			0.03		nA
$V_{CLMP-LO}$	Low Clamp Voltage	CPCLO = 1			0.84		V
$V_{CLMP-HI}$	High Clamp Voltage	CPCHI = 1, Referred to V_{CP}^+			–0.96		V
V_{MID}	Mid-Supply Output Bias Ratio	Referred to (V_{CP}^+ – GND)			0.48		V/V
Reference (R) Divider							
R	Divide Range	All Integers Included	●	1		31	Counts
VCO (N) Divider							
N	Divide Range	All Integers Included, Integer Mode	●	32		1023	Counts
		All Integers Included, Fractional Mode	●	35		1019	Counts
Fractional ΔΣ Modulator							
	Numerator Range	All Integers Included	●	1		262143	Counts

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{VCO}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Modulator LDO							
	Output Voltage	LDO Enabled, Four Values LDO Disabled			1.7 to 2.6 V_D^+		V V
	External Pin Capacitance	Required for LDO Stability	●	0.047	0.1	1	µF
Digital Pin Specifications							
V_{IH}	High Level Input Voltage	$\overline{MUTE}$, $\overline{CS}$, SDI, SCLK	●	1.55			V
V_{IL}	Low Level Input Voltage	$\overline{MUTE}$, $\overline{CS}$, SDI, SCLK	●			0.8	V
V_{IHYS}	Input Voltage Hysteresis	$\overline{MUTE}$, $\overline{CS}$, SDI, SCLK			250		mV
	Input Current	$\overline{MUTE}$, $\overline{CS}$, SDI, SCLK	●			±1	µA
I_{OH}	High Level Output Current	SDO and STAT, $V_{OH} = V_D^+ – 400mV$	●		–3.3	–1.9	mA
I_{OL}	Low Level Output Current	SDO and STAT, V_{OL} = 400mV	●	2.0	3.4		mA
	SDO Hi-Z Current		●			±1	µA
Digital Timing Specifications (See Figure 7 and Figure 8)							
t_{CKH}	SCLK High Time		●	25			ns
t_{CKL}	SCLK Low Time		●	25			ns
t_{CSS}	$\overline{CS}$ Setup Time		●	10			ns
t_{CSH}	$\overline{CS}$ High Time		●	10			ns
t_{CS}	SDI to SCLK Setup Time		●	6			ns
t_{CH}	SDI to SCLK Hold Time		●	6			ns
t_{DO}	SCLK to SDO Time	To V_{IH}/V_{IL}/Hi-Z with 30pF Load	●			16	ns
Power Supply Voltages							
	V_{REF}^+ Supply Range		●	3.15	3.3	3.45	V
	V_D^+ Supply Range		●	3.15	3.3	3.45	V
	V_{RF}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{VCO}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{CP}^+ Supply Range		●	3.15		5.25	V
Power Supply Currents							
I_{DD}	V_D^+ Supply Current	Digital Inputs at Supply Levels, PDFN = 1 Digital Inputs at Supply Levels, Fractional Mode, f_{PFD} = 66.3MHz MHz, LDOV[1:0] = 3	● ●		18.2	1500 22	µA mA
$I_{CC(5V)}$	Sum V_{CP}^+ Supply Currents	I_{CP} = 11.2mA I_{CP} = 1.0mA PDALL = 1	● ● ●		34 12 230	40 14 650	mA mA µA
$I_{CC(3.3V)}$	Sum V_{REF}^+, V_{RF}^+, V_{VCO}^+ Supply Currents	RF Muted, OD[2:0] = 1 RF Enabled, RFO[1:0] = 0, OD[2:0] = 1 RF Enabled, RFO[1:0] = 3, OD[2:0] = 1 RF Enabled, RFO[1:0] = 3, OD[2:0] = 2 RF Enabled, RFO[1:0] = 3, OD[2:0] = 3 RF Enabled, RFO[1:0] = 3, OD[2:0] = 4 to 6 PDALL = 1	● ● ● ● ● ● ●		70.4 81.1 91.3 109.2 114.8 119.6 53	80 95 105 125 135 140 250	mA mA mA mA mA mA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{VCO}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified (Note 2). All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Phase Noise and Spurious							
L_{MIN}	Output Phase Noise Floor (Note 5)	RFO[1:0] = 3, OD[2:0] = 1, f_{RF} = 6GHz			–155		dBc/Hz
		RFO[1:0] = 3, OD[2:0] = 2, f_{RF} = 3GHz			–155		dBc/Hz
		RFO[1:0] = 3, OD[2:0] = 3, f_{RF} = 2GHz			–156		dBc/Hz
		RFO[1:0] = 3, OD[2:0] = 4, f_{RF} = 1.5GHz			–156		dBc/Hz
		RFO[1:0] = 3, OD[2:0] = 5, f_{RF} = 1.2GHz			–157		dBc/Hz
		RFO[1:0] = 3, OD[2:0] = 6, f_{RF} = 1.0GHz			–158		dBc/Hz
$L_{NORM(INT)}$	Integer Normalized In-Band Phase Noise Floor	INTN = 1, I_{CP} = 5.6mA (Notes 6, 7, 9)			–226		dBc/Hz
$L_{NORM(FRAC)}$	Fractional Normalized In-Band Phase Noise Floor	INTN = 0, CPLE = 1, I_{CP} = 5.6mA (Notes 6, 7, 9)			–225		dBc/Hz
$L_{1/f}$	Normalized In-Band 1/f Phase Noise	I_{CP} = 11.2mA (Notes 6, 10)			–274		dBc/Hz
	In-Band Phase Noise Floor	Fractional Mode, CPLE = 1 (Notes 4, 6, 7, 10, 11)			–109		dBc/Hz
	Integrated Phase Noise from 100Hz to 40MHz	Fractional Mode, CPLE = 1 (Notes 4, 7, 11)			0.076		°RMS
	Spurious	Fractional Mode, $f_{OFFSET} = f_{PFD}$, PLL Locked (Notes 4, 7, 11, 12)			–97		dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6947I is guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 105°C.

Note 3: For 0.9V < V(CP) < (V_{CP}^+ – 0.9V).

Note 4: VCO is Crystek CVCO55C-2328-2536.

Note 5: f_{VCO} = 6GHz, f_{OFFSET} = 40MHz.

Note 6: Measured inside the loop bandwidth with the loop locked.

Note 7: Reference frequency supplied by Wenzel 501-04516, f_{REF} = 100MHz, P_{REF} = 10dBm.

Note 8: Reference frequency supplied by Wenzel 500-23571, f_{REF} = 61.44MHz, P_{REF} = 10dBm.

Note 9: Output phase noise floor is calculated from normalized phase noise floor by $L_{OUT} = L_{NORM} + 10\log_{10}(f_{PFD}) + 20\log_{10}(f_{RF}/f_{PFD})$.

Note 10: Output 1/f noise is calculated from normalized 1/f phase noise by $L_{OUT(1/f)} = L_{1/f} + 20\log_{10}(f_{RF}) – 10\log_{10}(f_{OFFSET})$.

Note 11: I_{CP} = 5.6mA, f_{PFD} = 50MHz, FILT[1:0] = 0, Loop BW = 31kHz; f_{RF} = 2415MHz, f_{VCO} = 2415MHz.

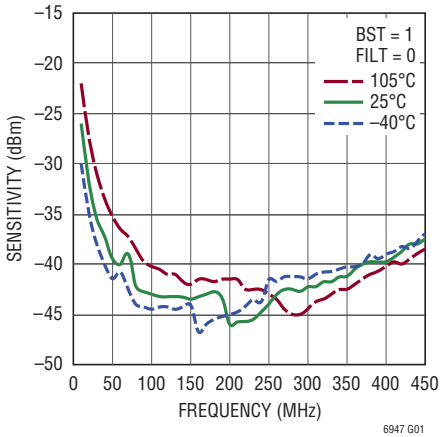
Note 12: Measured using DC1846.

Note 13: VCO is RFMD UMX-918-D16-G.

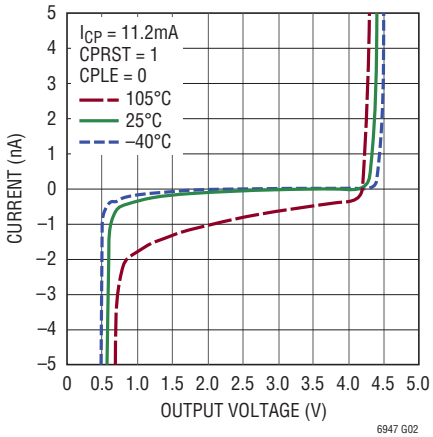
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{VCO}^+ = 3.3V$, $V_{CP}^+ = 5V$, INTN = 0, DITHEN = 1, CPLE = 1, RFO[1:0] = 3, unless otherwise noted.

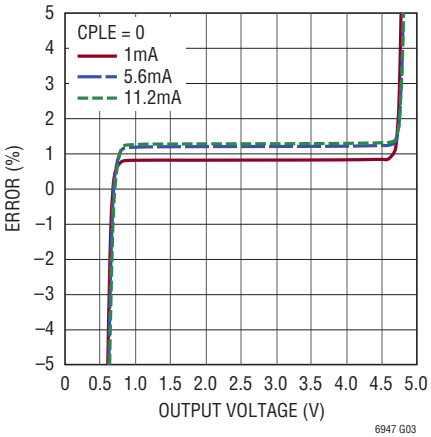
REF Input Sensitivity vs Frequency



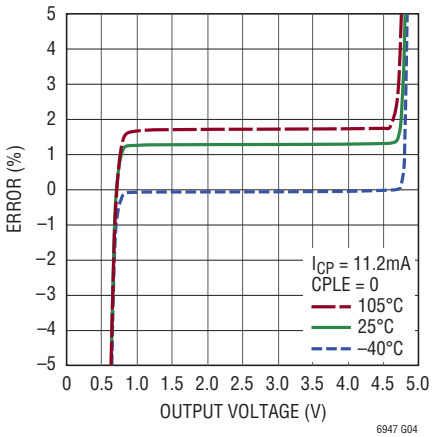
CP Hi-Z Current vs Voltage, Temperature



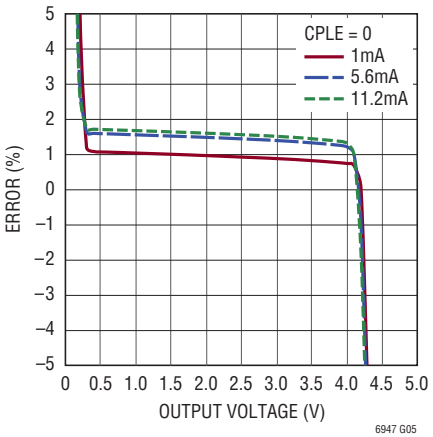
Charge Pump Sink Current Error vs Voltage, Output Current



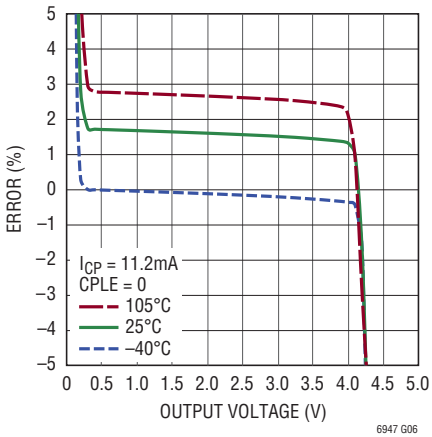
Charge Pump Sink Current Error vs Voltage, Temperature



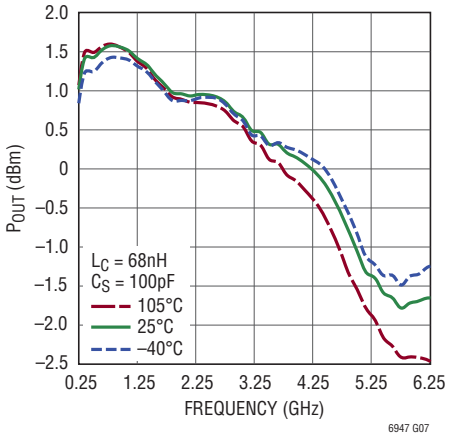
Charge Pump Source Current Error vs Voltage, Output Current



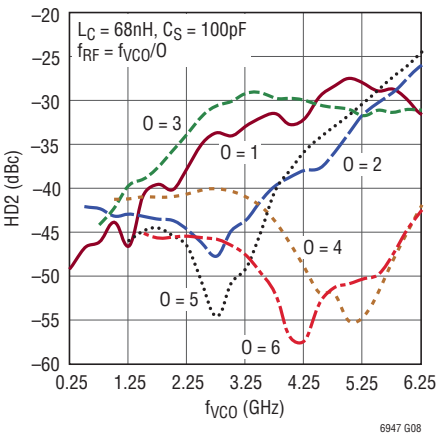
Charge Pump Source Current Error vs Voltage, Temperature



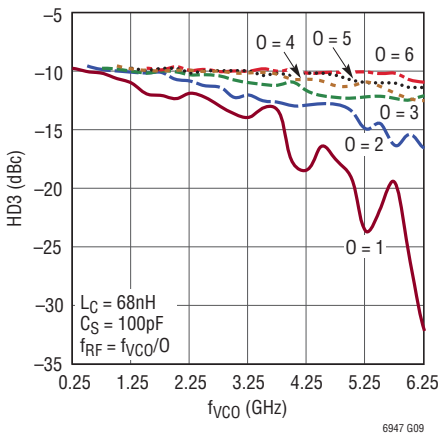
RF Output Power vs Frequency (Single-Ended on RF⁻)



RF Output HD2 vs Output Divide (Single-Ended on RF⁻)



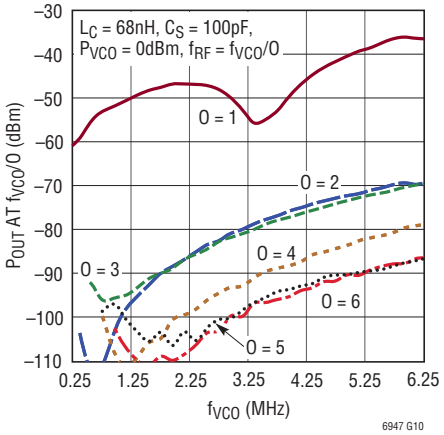
RF Output HD3 vs Output Divide (Single-Ended on RF⁻)



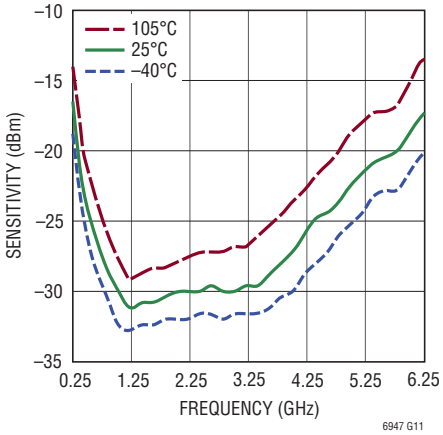
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{VCO}^+ = 3.3V$, $V_{CP}^+ = 5V$, INTN = 0, DITHEN = 1, CPLE = 1, RFO[1:0] = 3, unless otherwise noted.

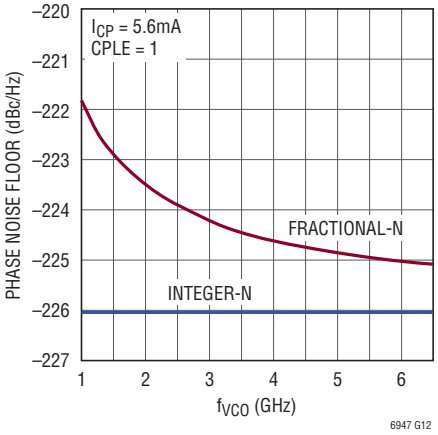
MUTE Output Power vs f_{VCO} and Output Divide (Single-Ended on RF⁻)



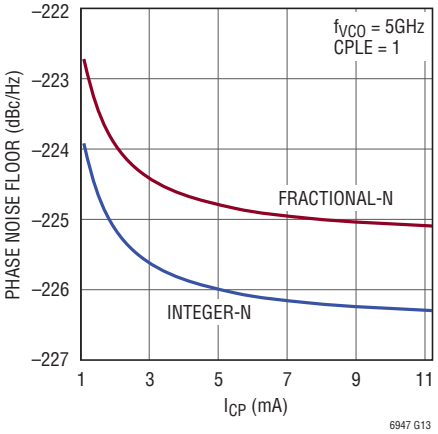
VCO Input Sensitivity vs Frequency



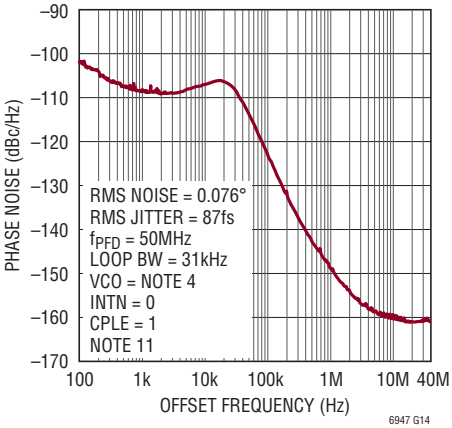
Normalized In-Band Phase Noise Floor vs f_{VCO}



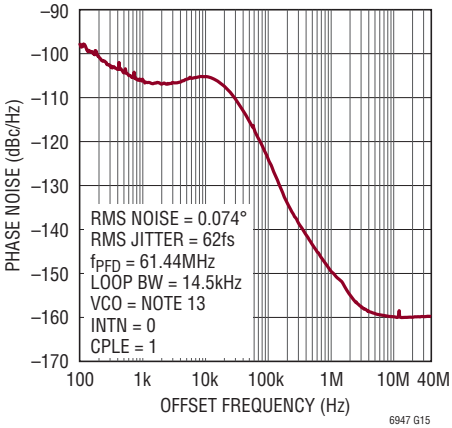
Normalized In-Band Phase Noise Floor vs CP Current



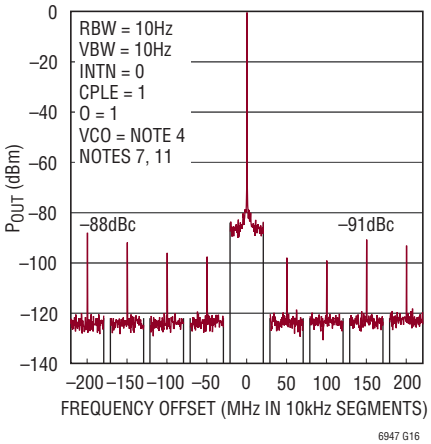
Closed-Loop Phase Noise f_{RF} = 2415MHz



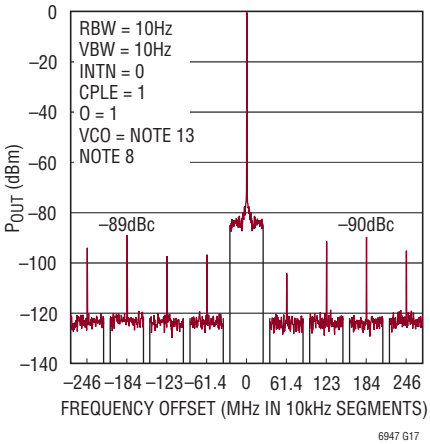
Closed-Loop Phase Noise f_{RF} = 3330MHz



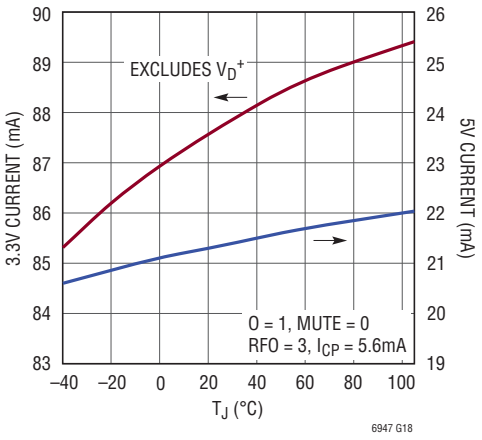
Spurious Response f_{RF} = 2415MHz, f_{REF} = 100MHz, f_{PFD} = 50MHz, Loop BW = 31kHz



Spurious Response f_{RF} = 3330MHz, f_{REF} = 61.44MHz, f_{PFD} = 61.44MHz, Loop BW = 14.5kHz



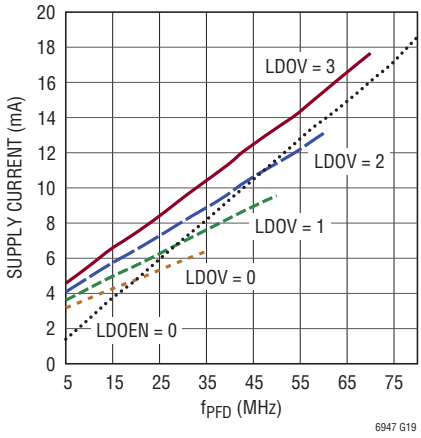
Supply Current vs Temperature



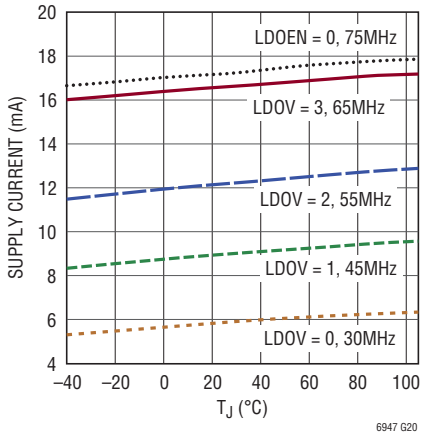
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{VCO}^+ = 3.3V$, $V_{CP}^+ = 5V$, INTN = 0, DITHEN = 1, CPLE = 1, RFO[1:0] = 3, unless otherwise noted.

V_D^+ Supply Current vs LDOV, f_{PFD} (INTN = 0, PDFN = 0)



V_D^+ Supply Current vs LDOV, Temperature (INTN = 0, PDFN = 0, f_{PFD} Noted)



PIN FUNCTIONS

REF⁺, REF⁻ (Pins 1, 28): Reference Input Signals. This differential input is buffered with a low noise amplifier, which feeds the reference divider. They are self-biased and must be AC-coupled with 1µF capacitors. If used single-ended with $V_{REF}^+ \leq 2.7V_{P-P}$, bypass REF⁻ to GND with a 1µF capacitor. If used single-ended with $V_{REF}^+ > 2.7V_{P-P}$, bypass REF⁻ to GND with a 47pF capacitor.

STAT (Pin 2): Status Output. This signal is a configurable logical OR combination of the UNLOK, LOK, THI, and TLO status bits, programmable via the STATUS register. See the Operation section for more details.

$\overline{CS}$ (Pin 3): Serial Port Chip Select. This CMOS input initiates a serial port communication burst when driven low, ending the burst when driven back high. See the Operation section for more details.

SCLK (Pin 4): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. See the Operation section for more details.

SDI (Pin 5): Serial Port Data Input. The serial port uses this CMOS input for data. See the Operation section for more details.

SDO (Pin 6): Serial Port Data Output. This CMOS three-state output presents data from the serial port during a read communication burst. Optionally attach a resistor of >200k to GND to prevent a floating output. See the Applications Information section for more details.

LDO (Pin 7): ΔΣ Modulator LDO Bypass Pin. This pin should be bypassed directly to the ground plane using a low ESR (<0.8Ω) 0.1µF ceramic capacitor as close to the pin as possible.

V_D^+ (Pin 8): 3.15V to 3.45V Positive Supply Pin for Serial Port and ΔΣ Modulator Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

$\overline{MUTE}$ (Pin 9): RF Mute. The CMOS active-low input mutes the RF± differential outputs while maintaining internal bias levels for quick response to de-assertion.

PIN FUNCTIONS

GND (Pins 10, 17, 18, 19, 20, 21, 22, Exposed Pad Pin 29): Negative Power Supply (Ground). These pins should be tied directly to the ground plane with multiple vias for each pin. The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance.

RF^-, RF^+ (Pins 11, 12): RF Output Signals. The VCO output divider is buffered and presented differentially on these pins. The outputs are open-collector, with 136Ω (typical) pull-up resistors tied to V_{RF}^+ to aid impedance matching. If used single-ended, the unused output should be terminated to 50Ω. See the Applications Information section for more details on impedance matching.

V_{RF}^+ (Pin 13): 3.15V to 3.45V Positive Supply Pin for RF Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

BB (Pin 14): RF Reference Bypass. This output has a 2.5k resistance and must be bypassed with a 1µF ceramic capacitor to GND. Do not couple this pin to any other signal.

VCO^-, VCO^+ (Pins 15, 16): VCO Input Signals. The differential signal placed on these pins is buffered with a low noise amplifier and fed to the internal output and feedback dividers. These self-biased inputs must be AC-coupled and present a single-ended 121Ω (typical) resistance to aid impedance matching. They may be used single-ended by bypassing VCO^- to GND with a capacitor. See the Applications Information section for more details on impedance matching.

V_{VCO}^+ (Pin 23): 3.15V to 3.45V Positive Supply Pin for VCO Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

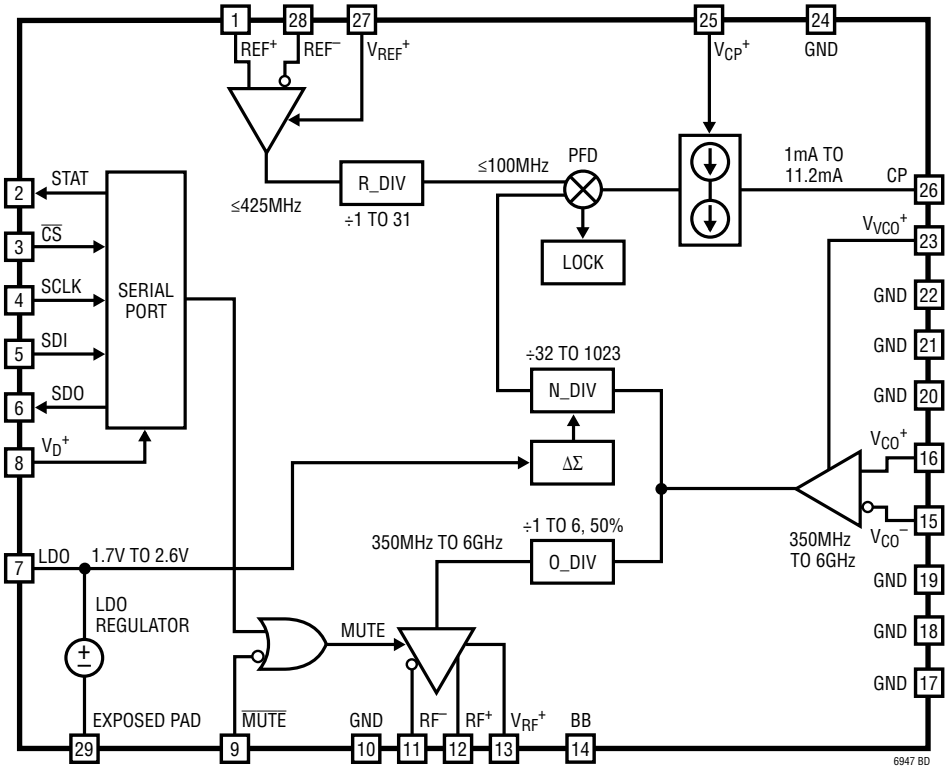
GND (24): Negative Power Supply (Ground). This pin is attached directly to the die attach paddle (DAP) and should be tied directly to the ground plane.

V_{CP}^+ (Pin 25): 3.15V to 5.25V Positive Supply Pin for Charge Pump Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

CP (Pin 26): Charge Pump Output. This bidirectional current output is normally connected to the external loop filter. See the Applications Information section for more details.

V_{REF}^+ (Pin 27): 3.15V to 3.45V Positive Supply Pin for Reference Input Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible.

BLOCK DIAGRAM



OPERATION

The LTC6947 is a high performance fractional-N PLL, and, combined with an external high performance VCO, can produce low noise LO signals up to 6GHz. The output frequency range may be further extended by utilizing the output divider. The device is able to achieve superior integrated phase noise by the combination of its extremely low in-band phase noise performance and the wide bandwidth allowed by its low spurious products.

The fractional-N feedback divider uses an advanced ΔΣ modulator, resulting in virtually no discrete modulator spurious tones. The modulator may be disabled if integer-N feedback is required.

REFERENCE INPUT BUFFER

The PLL's reference frequency is applied differentially on pins REF^+ and REF^-. These high impedance inputs are self-biased and must be AC-coupled with 1µF capacitors (see Figure 1 for a simplified schematic). Alternatively, the inputs may be used single-ended by applying the reference frequency at REF^+ and bypassing REF^- to GND with a 1µF capacitor. If the single-ended signal is greater than $2.7V_{P-P}$, then use a 47pF capacitor for the GND bypass.

A high quality signal must be applied to the $REF^±$ inputs

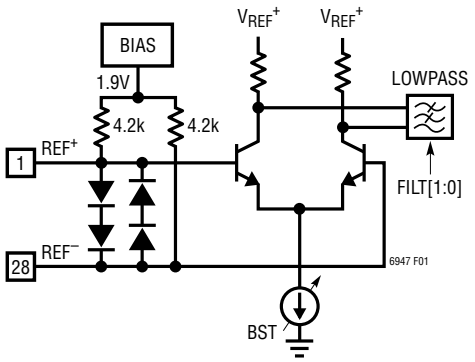


Figure 1. Simplified REF Interface Schematic

as they provide the frequency reference to the entire PLL. To achieve the part's in-band phase noise performance, apply a CW signal of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 40V/µs.

Additional options are available through serial port register h0B to further refine the application. Bits FILT[1:0] control the reference input buffer's lowpass filter, and should be set based upon f_{REF} to limit the reference's wideband noise. The FILT[1:0] bits must be set correctly to reach the L_{NORM} normalized in-band phase noise floor. See Table 1 for recommended settings.

Table 1. FILT[1:0] Programming

FILT[1:0]	f_{REF}
3	<20MHz
2	NA
1	20MHz to 50MHz
0	>50MHz

The BST bit should be set based upon the input signal level to prevent the reference input buffer from saturating. See Table 2 for recommended settings and the Applications Information section for programming examples.

Table 2. BST Programming

BST	V_{REF}
1	$<2V_{P-P}$
0	$≥2V_{P-P}$

REFERENCE (R) DIVIDER

A 5-bit divider, R_DIV, is used to reduce the frequency seen at the PFD. Its divide ratio R may be set to any integer from 1 to 31, inclusive. Use the RD[4:0] bits found in registers h06 to directly program the R divide ratio. See the Applications Information section for the relationship between R and the f_{REF}, f_{PFD}, f_{VCO}, and f_{RF} frequencies.

PHASE/FREQUENCY DETECTOR (PFD)

The phase/frequency detector (PFD), in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the R and N dividers. This action provides the necessary feedback to phase-lock the loop, forcing a phase alignment at the PFD's inputs. The PFD may be disabled with the CPRST bit which prevents UP and DOWN pulses from being produced. See Figure 2 for a simplified schematic of the PFD.

OPERATION

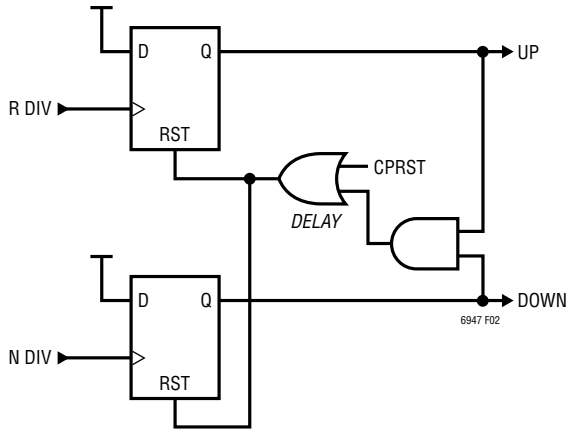


Figure 2. Simplified PFD Schematic

LOCK INDICATOR

The lock indicator uses internal signals from the PFD to measure phase coincidence between the R and N divider output signals. It is enabled by programming LKCT[1:0] in the serial port register h0C (see Table 5), and produces both LOCK and UNLOCK status flags, available through both the STAT output and serial port register h00.

The user sets the phase difference lock window time t_{LWW} for a valid LOCK condition with the LKWIN[2:0] bits. When using the device as a fractional-N synthesizer (fractional mode), the ΔΣ modulator changes the instantaneous phase seen at the PFD on every R_DIV and N_DIV cycle. The maximum allowable time difference in this case depends upon both the VCO frequency f_{VCO} and also the charge pump linearization enable bit CPLE (see the Charge Pump Linearizer section for an explanation of this function). Table 3 contains recommended settings for LKWIN[2:0] when using the device in fractional mode. See the Applications Information section for examples.

Table 3. LKWIN[2:0] Fractional Mode Programming

LKWIN[2:0]	t_{LWW}	f_{VCO} (CPLE = 1)	f_{VCO} (CPLE = 0)
0	5.0ns	≥2.97GHz	≥1.35GHz
1	7.35ns	≥2.00GHz	≥919MHz
2	10.7ns	≥1.39GHz	≥632MHz
3	15.8ns	≥941MHz	≥428MHz
4	23.0ns	≥646MHz	≥294MHz
5	34.5ns	≥431MHz	≥196MHz
6	50.5ns	≥294MHz	≥134MHz
7	76.0ns	≥196MHz	≥89MHz

When using the device as an integer-N synthesizer (integer mode), the phase difference seen at the PFD is minimized by the feedback of the PLL and no longer depends upon f_{VCO}. Table 4 contains recommended settings for different f_{PFD} frequencies when used in integer mode.

Table 4. LKWIN[2:0] Integer Mode Programming

LKWIN[2:0]	t_{LWW}	f_{PFD}
0	5.0ns	>6.8MHz
1	7.35ns	≤6.8MHz
2	10.7ns	≤4.7MHz
3	15.8ns	≤3.2MHz
4	23.0ns	≤2.2MHz
5	34.5ns	≤1.5MHz
6	50.5ns	≤1.0MHz
7	76.0ns	≤660kHz

The PFD phase difference must be less than t_{LWW} for the COUNTS number of successive counts before the lock indicator asserts the LOCK flag. The LKCT[1:0] bits found in register h0C are used to set COUNTS depending upon the application. Set LKCT[1:0] = 0 to disable the lock indicator. See Table 5 for LKCT[1:0] programming and the Applications Information section for examples.

Table 5. LKCT[1:0] Programming

LKCT[1:0]	COUNTS
0	Lock Indicator Disabled
1	32
2	256
3	2048

When the PFD phase difference is greater than t_{LWW}, the lock indicator immediately asserts the UNLOCK status flag and clears the LOCK flag, indicating an out-of-lock condition. The UNLOCK flag is immediately de-asserted when the phase difference is less than t_{LWW}. See Figure 3 below for more details.

Note that f_{REF} must be present for the LOCK and UNLOCK flags to properly assert and clear.

CHARGE PUMP

The charge pump, controlled by the PFD, forces sink (DOWN) or source (UP) current pulses onto the CP pin,

OPERATION

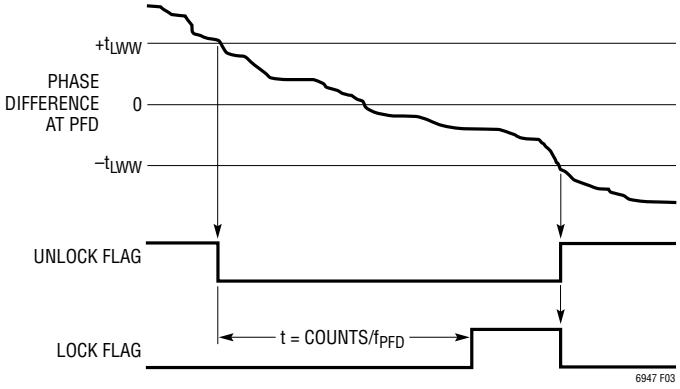


Figure 3. UNLOCK and LOCK Timing

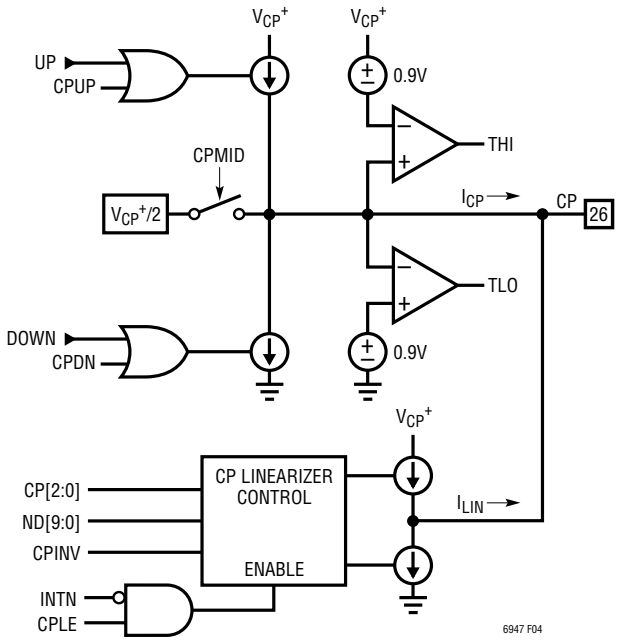


Figure 4. Simplified Charge Pump Schematic

which should be connected to an appropriate loop filter. See Figure 4 for a simplified schematic of the charge pump.

The output current magnitude I_{CP} may be set from 1mA to 11.2mA using the CP[2:0] bits found in serial port register h0C. A larger I_{CP} can result in lower in-band noise due to the lower impedance of the loop filter components, although currents larger than 5.6mA typically cause worse spurious performance. See Table 6 for programming specifics and the Applications Information section for loop filter examples.

Table 6. CP[2:0] Programming

CP[2:0]	I_{CP}
0	1.0mA
1	1.4mA
2	2.0mA
3	2.8mA
4	4.0mA
5	5.6mA
6	8.0mA
7	11.2mA

The CPINV bit found in register h0D should be set for applications requiring signal inversion from the PFD, such as for external loops using an op amp. A passive loop filter as shown in Figure 14 requires CPINV = 0. An active loop filter as shown in Figure 15 requires CPINV = 1 for a positive K_{VCO}.

Charge Pump Functions

The charge pump contains additional features to aid in system startup. See Table 7 for a summary.

Table 7. Charge Pump Function Bit Descriptions

BIT	DESCRIPTION
CPCHI	Enable High Voltage Output Clamp
CPCLO	Enable Low Voltage Output Clamp
CPDN	Force Sink Current
CPINV	Invert PFD Phase
CPLE	Linearizer Enable
CPMID	Enable Mid-Voltage Bias
CPRST	Reset PFD
CPUP	Force Source Current
CPWIDE	Extend Current Pulse Width
THI	High Voltage Clamp Flag
TLO	Low Voltage Clamp Flag

The CPCHI and CPCLO bits found in register h0D enable the high and low voltage clamps, respectively. When CPCHI is enabled and the CP pin voltage exceeds approximately $V_{CP}^+ – 0.9V$, the THI status flag is set, and the charge pump sourcing current is disabled. Alternately, when CPCLO is enabled and the CP pin voltage is less than approximately 0.9V, the TLO status flag is set, and the charge pump sinking current is disabled. See Figure 4 for a simplified schematic.

OPERATION

The CPMID bit also found in register h0D enables a resistive $V_{CP}^{+}/2$ output bias which may be used to pre-bias troublesome loop filters into a valid voltage range. When using CPMID, it is recommended to also assert the CPRST bit, forcing a PFD reset. Both CPMID and CPRST must be set to 0 for normal operation.

The CPUP and CPDN bits force a constant I_{CP} source or sink current, respectively, on the CP pin. The CPRST bit may also be used in conjunction with the CPUP and CPDN bits, allowing a pre-charge of the loop to a known state, if required. CPUP, CPDN, and CPRST must be set to 0 to allow the loop to lock.

The CPWIDE bit extends the charge pump output current pulse width by increasing the PFD reset path's delay value (see Figure 2). CPWIDE is normally set to 0.

Charge Pump Linearizer

When the LTC6947 is operated in fractional mode, the charge pump's current output versus its phase stimulus (its gain linearity) must be extremely accurate. The CP gain linearizer automatically adds a correction current I_{LIN} to minimize the charge pump's impact on in-band phase noise and spurious products during fractional operation.

The CP gain linearizer is enabled by setting CPLE = 1. It is automatically disabled when in integer mode. CPLE should be set to 0 if CPRST or CPMID are asserted to prevent the linearizer from producing unintended currents.

VCO INPUT BUFFER

The VCO frequency is applied differentially on pins VCO^{+} and VCO^{-}. The inputs are self-biased and must be AC-coupled. Alternatively, the inputs may be used single-ended by applying the VCO frequency at VCO^{+} and bypassing VCO^{-} to GND with a capacitor. Each input provides a single-ended 121Ω resistance to aid in impedance matching at high frequencies. See the Applications Information section for matching guidelines.

The BB pin is used to bias internal VCO buffer circuitry. The BB pin has a 2k output resistance and should be bypassed with a 1µF ceramic capacitor to GND, giving a time constant of 2ms. Stable bias voltages are achieved after approximately 3 time constants following power-up.

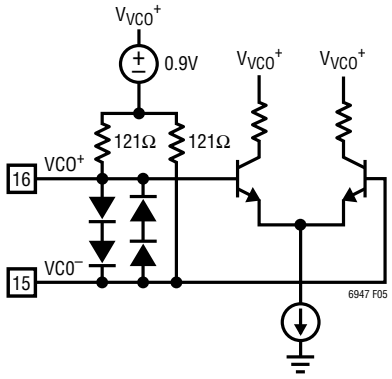


Figure 5. Simplified VCO Interface Schematic

VCO (N) DIVIDER

The 10-bit N divider provides the feedback from the VCO to the PFD. Its divide ratio N is restricted to any integer from 35 to 1019, inclusive, when in fractional mode. The divide ratio may be programmed from 32 to 1023, inclusive, when in integer mode. Use the ND[9:0] bits found in registers h06 and h07 to directly program the N divide ratio. See the Applications Information section for the relationship between N and the f_{REF}, f_{PFD}, f_{VCO}, and f_{RF} frequencies.

ΔΣ MODULATOR

The ΔΣ modulator changes the N divider's ratio each PFD cycle to achieve an average fractional divide ratio. The fractional numerator NUM[17:0] is programmable from 1 to 262143, or $2^{18} - 1$. The fractional denominator is fixed at 262144 (or 2^{18}), with the resulting fractional ratio F given by Equation 3. See the Applications Information section for the relationship between NUM, F, and the f_{REF}, f_{PFD}, f_{VCO}, and f_{RF} frequencies.

The ΔΣ modulator uses digital signal processing (DSP) techniques to achieve an average fractional divide ratio. The modulator is clocked at the f_{PFD} rate. This process produces output modulation noise known as quantization noise with a highpass frequency response. The external lowpass loop filter is used to filter this quantization noise to a level beneath the phase noise of the VCO. This prevents the noise from contributing to the overall phase noise of the system. The loop filter must be designed to adequately filter the quantization noise.

The oversampling ratio OSR is defined as the ratio of the ΔΣ modulator clock frequency f_{PFD} to the loop bandwidth

OPERATION

BW of the PLL (see Equation 10). See the Applications Information section for guidelines concerning the OSR and the loop filter.

When the desired output frequency is such that the needed NUM value is 0, the LTC6947 should be operated in integer mode (INTN = 1). In integer mode, the modulator is placed in standby, with all blocks still powered up, thus allowing it to resume fractional operation immediately.

Enable numerator dither mode (DITHEN = 1) to further reduce spurious produced by the modulator. Dither has no measurable impact on in-band phase noise, and is enabled by default. See Table 8 for a complete list of modulator bit descriptions.

Modulator Reset

To achieve consistent spurious performance, the modulator DSP circuitry should be re-initialized by setting RSTFN = 1 whenever NUM[17:0] is changed. Setting AUTORST = 1 causes the RSTFN bit to be set automatically whenever any of serial port registers h05 through h0A are written. When AUTORST is enabled, there is no need for a separate register write to set the RSTFN bit. See Table 8 for a summary of the modulator bits.

Table 8. Fractional Modulator Bit Descriptions

BIT	DESCRIPTION
AUTORST	Automatically Reset Modulator when Registers h05 to h0A Are Written
DITHEN	Enable Fractional Numerator Dither
INTN	Integer Mode; Fractional Modulator Placed in Standby
RSTFN	Reset Modulator (Auto Clears)
SEED	Seed Value for Pseudorandom Dither Algorithm

LDO REGULATOR

The adjustable low dropout (LDO) regulator supplies power to the ΔΣ modulator. The regulator requires a low ESR ceramic capacitor (ESR < 0.8Ω) connected to the LDO pin (pin 7) for stability. The capacitor value may range from 0.047µF to 1µF.

The LDO voltage is set using the LDOV[1:0] bits, and should be chosen based upon the f_{PFD} frequency to minimize power and spurious. The regulator is disabled by setting the LDOEN bit to 0. When disabled by using either the LDOEN or PDFN bits, the LDO pin is connected directly to V_D^+ using a low impedance switch, and the regulator is powered down. See Table 9 for programming details.

Table 9. LDOV[1:0] and LDOEN Programming

LDOV[1:0]	LDOEN	V(LDO)	f_{PFD}
0	1	1.7V	≤34.3MHz
1	1	2.0V	≤45.9MHz
2	1	2.3V	≤56.1MHz
3	1	2.6V	≤66.3MHz
X	0	V_D^+	≤76.1MHz

OUTPUT (O) DIVIDER

The 3-bit O divider can reduce the frequency from the VCO to extend the output frequency range. Its divide ratio O may be set to any integer from 1 to 6, inclusive, outputting a 50% duty cycle even with odd divide values. Use the OD[2:0] bits found in register h0B to directly program the O divide ratio. See the Applications Information section for the relationship between O and the f_{REF}, f_{PFD}, f_{VCO}, and f_{RF} frequencies.

RF OUTPUT BUFFER

The low noise, differential output buffer produces a differential output power of –4.3dBm to +4.5dBm, settable with bits RFO[1:0] according to Table 10. The outputs may be combined externally, or used individually. Terminate any unused output with a 50Ω resistor to V_{RF}^+.

Table 10. RFO[1:0] Programming

RFO[1:0}	P_{RF} (DIFFERENTIAL)	P_{RF} (SINGLE-ENDED)
0	–4.3dBm	–7.3dBm
1	–1.5dBm	–4.5dBm
2	1.6dBm	–1.4dBm
3	4.5dBm	1.5dBm

Each output is open-collector with 136Ω pull-up resistors to V_{RF}^+, easing impedance matching at high frequencies. See Figure 6 for circuit details and the Applications Information section for matching guidelines. The buffer may be muted with either the OMUTE bit, found in register h02, or by forcing the $\overline{MUTE}$ input low.

OPERATION

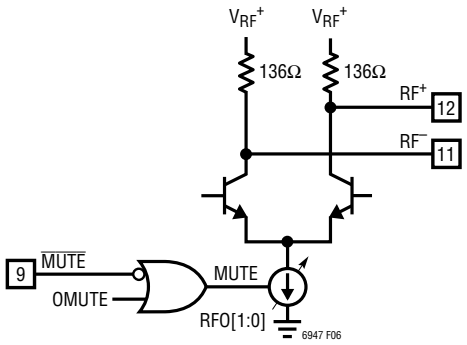


Figure 6. Simplified RF Interface Schematic

SERIAL PORT

The SPI-compatible serial port provides control and monitoring functionality. A configurable status output STAT gives additional instant monitoring.

Communication Sequence

The serial bus is comprised of $\overline{CS}$, SCLK, SDI, and SDO. Data transfers to the part are accomplished by the serial bus master device first taking $\overline{CS}$ low to enable the LTC6947's port. Input data applied on SDI is clocked on the rising edge of SCLK, with all transfers *MSB first*. The communication burst is terminated by the serial bus master returning $\overline{CS}$ high. See Figure 7 for details.

Data is read from the part during a communication burst using SDO. Readback may be multidrop (more than one LTC6947 connected in parallel on the serial bus), as SDO is three-stated (Hi-Z) when $\overline{CS}$ = 1, or when data is not being read from the part. *If the LTC6947 is not used in a multidrop configuration, or if the serial port master is not capable of setting the SDO line level between read sequences, it is recommended to attach a high value resistor of greater than 200k between SDO and GND to ensure the line returns to a known level during Hi-Z states.* See Figure 8 for details.

Single Byte Transfers

The serial port is arranged as a simple memory map, with status and control available in 15 byte-wide registers. All data bursts are comprised of at least two bytes. The seven most significant bits of the first byte are the register address, with an LSB of 1 indicating a read from the part, and LSB of 0 indicating a write to the part. The subsequent byte, or bytes, is data from/to the specified register address. See Figure 9 for an example of a detailed write sequence, and Figure 10 for a read sequence.

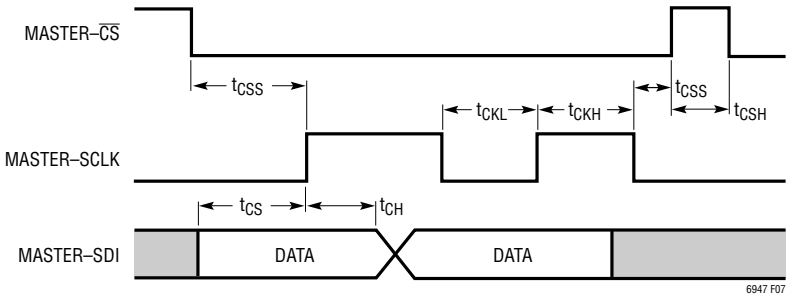


Figure 7. Serial Port Write Timing Diagram

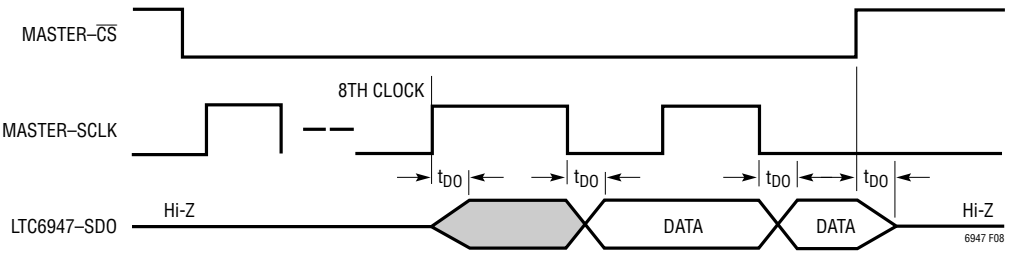


Figure 8. Serial Port Read Timing Diagram

OPERATION

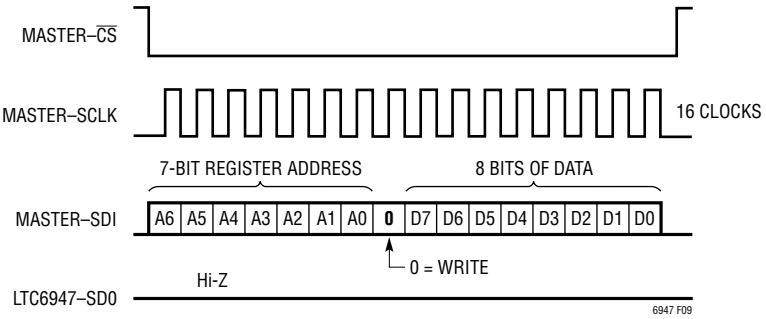


Figure 9. Serial Port Write Sequence

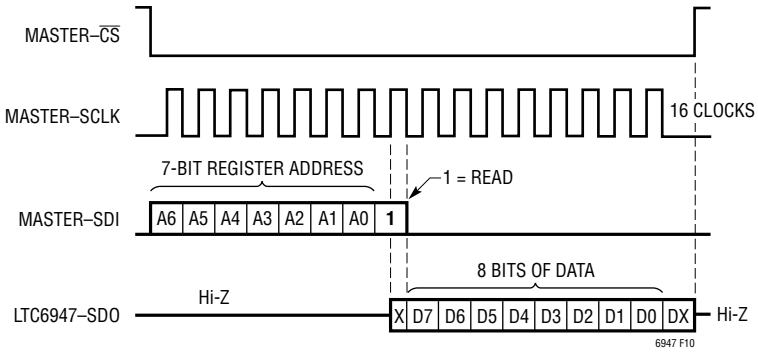


Figure 10. Serial Port Read Sequence

Figure 11 shows an example of two write communication bursts. The first byte of the first burst sent from the serial bus master on SDI contains the destination register address (Addr0) and an LSB of 0 indicating a write. The next byte is the data intended for the register at address Addr0. $\overline{CS}$ is then taken high to terminate the transfer. The first byte of the second burst contains the destination register address (Addr1) and an LSB indicating a write. The next byte on SDI is the data intended for the register at address Addr1. $\overline{CS}$ is then taken high to terminate the transfer.

Multiple Byte Transfers

More efficient data transfer of multiple bytes is accomplished by using the LTC6947's register address auto-increment feature as shown in Figure 12. The serial port master sends the destination register address in the first byte and its data in the second byte as before, but continues sending bytes destined for subsequent registers. Byte 1's address is Addr0+1, Byte 2's address is Addr0+2, and so on. If the register address pointer attempts to increment past 14 (h0E), it is automatically reset to 0.

An example of an auto-increment read from the part is shown in Figure 13. The first byte of the burst sent from the serial bus master on SDI contains the destination register address (Addr0) and an LSB of 1 indicating a read. Once the LTC6947 detects a read burst, it takes SDO out of the Hi-Z condition and sends data bytes sequentially, beginning with data from register Addr0. The part ignores all other data on SDI until the end of the burst.

Multidrop Configuration

Several LTC6947s may share the serial bus. In this multidrop configuration, SCLK, SDI, and SDO are common between all parts. The serial bus master must use a separate $\overline{CS}$ for each LTC6947 and ensure that only one device has $\overline{CS}$ asserted at any time. It is recommended to attach a high value resistor to SDO to ensure the line returns to a known level during Hi-Z states.

Serial Port Registers

The memory map of the LTC6947 may be found in Table 11, with detailed bit descriptions found in Table 12. The

OPERATION

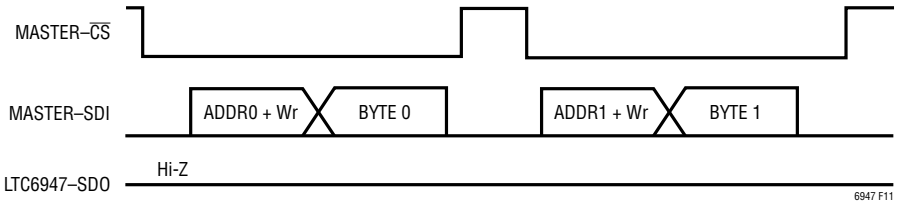


Figure 11. Serial Port Single Byte Write

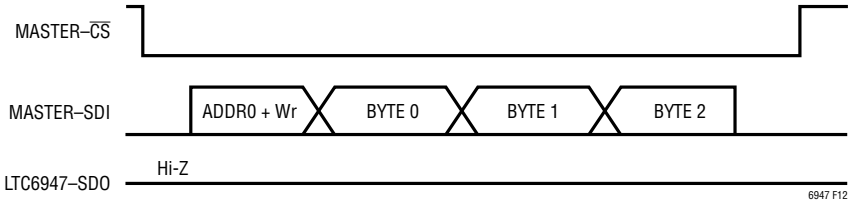


Figure 12. Serial Port Auto-Increment Write

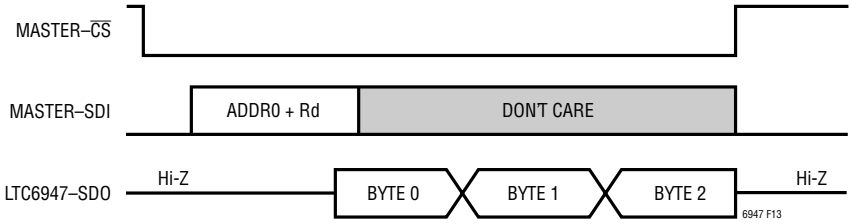


Figure 13. Serial Port Auto-increment Read

Table 11. Serial Port Register Contents

ADDR	MSB	[6]	[5]	[4]	[3]	[2]	[1]	LSB	R/W	DEFAULT
h00	*	*	UNLOCK	*	*	LOCK	THI	TLO	R	
h01	*	*	x[5]	*	*	x[2]	x[1]	x[0]	R/W	h04
h02	PDALL	PDPLL	*	PDOUT	PDFN	*	OMUTE	POR	R/W	h06
h03	*	*	*	*	*	AUTORST	DITHEN	INTN	R/W	h06
h04	*	*	*	*	CPLE	LDOEN	LDOV[1]	LDOV[0]	R/W	h07
h05	SEED[7]	SEED[6]	SEED[5]	SEED[4]	SEED[3]	SEED[2]	SEED[1]	SEED[0]	R/W	h11
h06	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	*	ND[9]	ND[8]	R/W	h08
h07	ND[7]	ND[6]	ND[5]	ND[4]	ND[3]	ND[2]	ND[1]	ND[0]	R/W	hFA
h08	*	*	NUM[17]	NUM[16]	NUM[15]	NUM[14]	NUM[13]	NUM[12]	R/W	h3F
h09	NUM[11]	NUM[10]	NUM[9]	NUM[8]	NUM[7]	NUM[6]	NUM[5]	NUM[4]	R/W	hFF
h0A	NUM[3]	NUM[2]	NUM[1]	NUM[0]	*	*	RSTFN	*	R/W	hF0
h0B	BST	FILT[1]	FILT[0]	RFO[1]	RFO[0]	OD[2]	OD[1]	OD[0]	R/W	hF9
h0C	LKWIN[2]	LKWIN[1]	LKWIN[0]	LKCT[1]	LKCT[0]	CP[2]	CP[1]	CP[0]	R/W	h4F
h0D	CPCHI	CPCLO	CPMID	CPINV	CPWIDE	CPRST	CPUP	CPDN	R/W	hE4
h0E	REV[3]	REV[2]	REV[1]	REV[0]	PART[3]	PART[2]	PART[1]	PART[0]	R	hxx†

*unused †varies depending on version

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Table 12. Serial Port Register Bit Field Summary

BITS	DESCRIPTION	DEFAULT
AUTORST	Reset Modulator Whenever Registers H05 to h0A Are Written	1
BST	REF Buffer Boost Current	1
CP[2:0]	CP Output Current	h7
CPCHI	Enable Hi-Voltage CP Output Clamp	1
CPCLO	Enable Low-Voltage CP Output Clamp	1
CPDN	Force CP Pump Down	0
CPINV	Invert CP Phase	0
CPLE	CP Linearizer Enable	0
CPMID	CP Bias to Mid-Rail	1
CPRST	CP Tri-State	1
CPUP	Force CP Pump Up	0
CPWIDE	Extend CP Pulse Width	0
DITHEN	Enable Fractional Numerator Dither	1
FILT[1:0]	REF Input Buffer Filter	h3
INTN	Integer Mode; Fractional Modulator Placed in Standby	0
LDOEN	LDO Enable	1
LDOV[1:0]	LDO Voltage	h3
LKCT[1:0]	PLL Lock Cycle Count	h1
LKWIN[2:0]	PLL Lock Indicator Window	h2
LOCK	PLL Lock Indicator Flag	
ND[9:0]	N Divider Value (ND[9:0] ≥ 32)	h0FA
NUM[17:0]	Fractional Numerator Value	h3FFF
OD[2:0]	Output Divider Value (0 < OD[2:0] < 7)	h1
OMUTE	Mutes RF Output	1
PART[3:0]	Part Code	h0
PDALL	Full Chip Powerdown	0
PDFN	Powers Down LDO and Modulator Clock	0
PDOUT	Powers Down N_DIV, RF Output Buffer	0
PDPLL	Powers Down REF, R_DIV, PFD, CPUMP	0
POR	Force Power-On-Reset	0
RD[4:0]	R Divider Value (RD[4:0] > 0)	h001
REV[3:0]	Rev Code	h1
RFO[1:0]	RF Output Power	h3
RSTFN	Force Modulator Reset (Auto Clears)	0
SEED[7:0]	Modulator Dither Seed Value	h11
THI	CP Clamp High Flag	
TLO	CP Clamp Low Flag	
UNLOK	PLL Unlock Flag	
x[5,2:0]	STAT Output OR Mask	h04

register address shown in hexadecimal format under the ADDR column is used to specify each register. Each register is denoted as either read-only (R) or read-write (R/W). The register's default value on device power-up or after a reset is shown at the right.

The read-only register at address h00 is used to determine different status flags. These flags may be instantly output on the STAT pin by configuring register h01. See the STAT Output section for more information.

The read-only register at address h0E is a ROM byte for device identification.

STAT Output

The STAT output pin is configured with the x[5,2:0] bits of register h01. These bits are used to bit-wise mask, or enable, the corresponding status flags of status register h00, according to Equation 1. The result of this bit-wise Boolean operation is then output on the STAT pin.

$$STAT = OR\ (Reg00[5,2:0]\ AND\ Reg01[5,2:0]) \quad (1)$$

or, expanded,

$$STAT = (UNLOCK\ AND\ x[5])\ OR\ (LOCK\ AND\ x[2])\ OR\ (THI\ AND\ x[1])\ OR\ (TLO\ AND\ x[0])$$

For example, if the application requires STAT to go high whenever the LOCK or THI flags are set, then x[2] and x[1] should be set to 1, giving a register value of h06.

Block Power-Down Control

The LTC6947's power-down control bits are located in register h02, described in Table 12. Different portions of the device may be powered down independently. *Care must be taken with the LSB of the register, the POR (power-on-reset) bit. When written to a 1, this bit forces a full reset of the part's digital circuitry to its power-up default state.*

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INTRODUCTION

A PLL is a complex feedback system that may conceptually be considered a frequency multiplier. The system multiplies the frequency input at REF± and outputs a higher frequency at RF±. The PFD, charge pump, N divider, external VCO, and loop filter form a feedback loop to accurately control the output frequency (see Figure 14).

The external loop filter is used to set the PLL's loop bandwidth BW. Lower bandwidths generally have better spurious performance and lower ΔΣ modulator quantization noise. Higher bandwidths can have better total integrated phase noise.

The R and O divider and input frequency f_{REF} are used to set the output frequency resolution. When in fractional mode, the ΔΣ modulator changes the N divider's ratio each PFD cycle to produce an average fractional divide ratio. This achieves a much smaller frequency resolution for a given f_{PFD} as compared to integer mode.

OUTPUT FREQUENCY

When the loop is locked, the frequency f_{VCO} (in Hz) produced at the output of the VCO is determined by the reference frequency f_{REF}, the R and N divider values, and the fractional value F, given by Equation 2:

$$f_{VCO} = \frac{f_{REF} \bullet (N+F)}{R} \quad (2)$$

where the fractional value F is given by Equation 3:

$$F = \frac{NUM}{2^{18}} \quad (3)$$

NUM is programmable from 1 to 262143, or $2^{18}-1$. When using the LTC6947 in integer mode, F = 0.

The PFD frequency f_{PFD} is given by the following equation:

$$f_{PFD} = \frac{f_{REF}}{R} \quad (4)$$

and f_{VCO} may be alternatively expressed as:

$$f_{VCO} = f_{PFD} \bullet (N + F) \quad (5)$$

The output frequency f_{RF} produced at the output of the O divider is given by Equation 6:

$$f_{RF} = \frac{f_{VCO}}{O} \quad (6)$$

Using the above equations, the minimum output frequency resolution $f_{STEP(MIN)}$ produced by a unit change in the fractional numerator NUM while in fractional mode is given by Equation 7:

$$f_{STEP(MIN)} = \frac{f_{REF}}{R \bullet O \bullet 2^{18}} \quad (7)$$

Alternatively, to calculate the numerator step size NUM_{STEP} needed to produce a given frequency step $f_{STEP(FRAC)}$, use Equation 8:

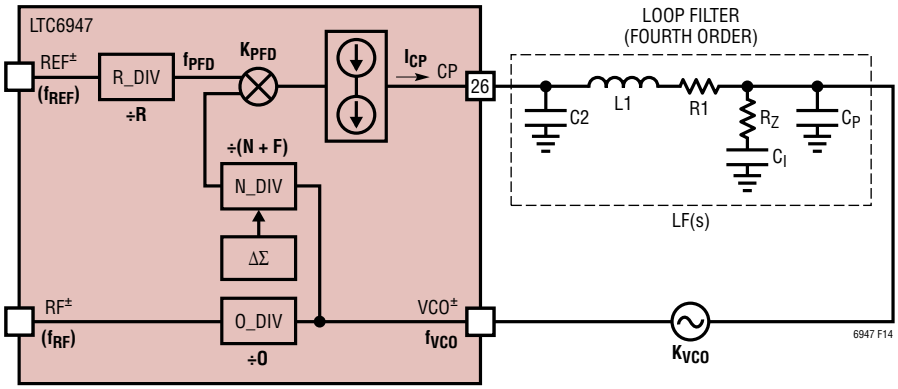

Figure 14. PLL Loop Diagram

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$$NUM_{STEP} = \frac{f_{STEP(FRAC)} \bullet R \bullet O \bullet 2^{18}}{f_{REF}} \quad (8)$$

The output frequency resolution $f_{STEP(INT)}$ produced by a unit change in N while in integer mode is given by Equation 9:

$$f_{STEP(INT)} = \frac{f_{REF}}{R \bullet O} \quad (9)$$

LOOP FILTER DESIGN

A stable PLL system requires care in designing the external loop filter. The Linear Technology FracNWizard application, available from www.linear.com, aids in design and simulation of the complete system.

The loop design should use the following algorithm:

1) *Determine the output frequency f_{RF} and frequency step size f_{STEP} based on application requirements.* Using Equations 2, 4, 6, and 7, change f_{REF}, N, R, and O until the application frequency constraints are met. Use the minimum R value that still satisfies the constraints.

2) *Select the open loop bandwidth BW constrained by f_{PFD} and oversampling ratio OSR.* The OSR is the ratio of f_{PFD} to BW (see Equation 10):

$$OSR = \frac{f_{PFD}}{BW} \quad (10)$$

or

$$BW = \frac{f_{PFD}}{OSR}$$

where BW and f_{PFD} are in Hz.

A stable loop, both in integer and fractional mode, requires that the OSR is greater than or equal to 10. Further, in fractional mode, OSR must be high enough to allow the loop filter to reduce modulator quantization noise to an acceptable level.

Choosing a higher-order loop filter when using the ΔΣ modulator allows for a smaller OSR, and thus a larger loop bandwidth. Linear Technology's FracNWizard helps choose the appropriate OSR and BW values.

3) *Select loop filter component R_Z and charge pump current I_{CP} based on BW and the VCO gain factor, K_{VCO}.* BW (in Hz) is approximated by the following equation:

$$BW \cong \frac{I_{CP} \bullet R_Z \bullet K_{VCO}}{2 \bullet \pi \bullet N} \quad (11)$$

or

$$R_Z = \frac{2 \bullet \pi \bullet BW \bullet N}{I_{CP} \bullet K_{VCO}}$$

where K_{VCO} is in Hz/V, I_{CP} is in Amps, and R_Z is in Ohms. K_{VCO} is the VCO's frequency tuning sensitivity, and may be determined from the VCO specifications. Use I_{CP} = 5.6mA to lower in-band noise unless component values force a lower setting.

4) *Select loop filter components C_I and C_P based on BW and R_Z.* A reliable second-order loop filter design can be achieved by using the following equations for the loop capacitors (in Farads).

$$C_I = \frac{3.5}{2 \bullet \pi \bullet BW \bullet R_Z} \quad (12)$$

$$C_P = \frac{1}{7 \bullet \pi \bullet BW \bullet R_Z} \quad (13)$$

Use FracNWizard to aid in the design of higher order loop filters.

LOOP FILTERS USING AN OP AMP

Some VCO tune voltage ranges are greater than the LTC6947's charge pump voltage range. An active loop filter using an op amp can increase the tuning voltage range. To maintain the LTC6947's high performance, care must be given to picking an appropriate op amp.

The op amp input common mode voltage should be biased within the LTC6947 charge pump's voltage range, while its output voltage should achieve the VCO tuning range. See Figure 15 for an example op amp loop filter.

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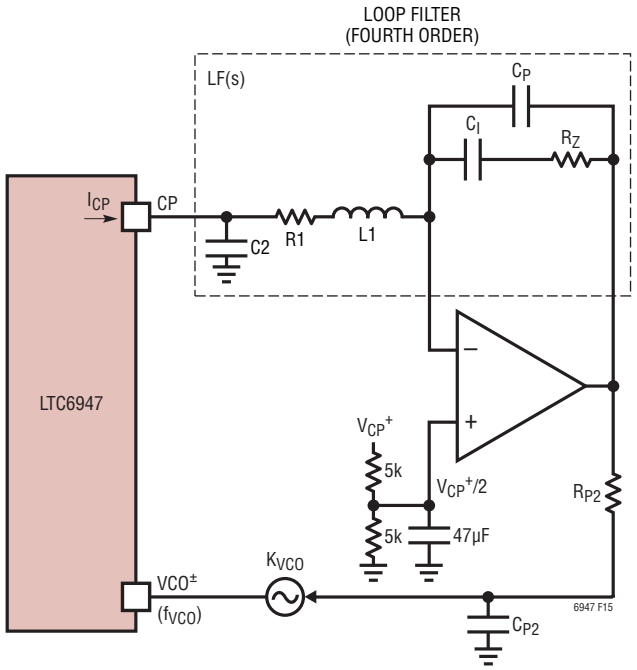

Figure 15. Op Amp Loop Filter

The op amp's input bias current is supplied by the charge pump; minimizing this current keeps spurs related to f_{PFD} low. The input bias current should be less than the charge pump leakage (found in the Electrical Characteristics section) to avoid increasing spurious products.

Op amp noise sources are highpass filtered by the PLL loop filter and should be kept at a minimum, as their effect raises the total system phase noise beginning near the loop bandwidth. Choose a low noise op amp whose input-referred voltage noise is less than the thermal noise of R_Z. Additionally, the gain-bandwidth of the op amp should be at least 20 times the loop bandwidth to limit phase margin degradation. The LT®1678 is an op amp that works very well in most applications.

An additional R-C lowpass filter (formed by R_{P2} and C_{P2} in Figure 15) connected at the input of the VCO will limit the op amp output noise sources. The bandwidth of this filter should be approximately 15 to 20 times the PLL loop bandwidth to limit loop phase margin degradation. R_{P2} should be small (preferably less than R_Z) to minimize its noise impact on the loop. However, picking too small of a value can make the op amp unstable as it has to drive the capacitor in this filter.

DESIGN AND PROGRAMMING EXAMPLE

This programming example uses the DC1846 with the LTC6947. Assume the following parameters of interest:

f_{REF} = 100MHz at 7dBm into 50Ω

f_{STEP} = 50kHz

f_{RF} = 2415.15MHz

f_{VCO} = 2328MHz to 2536MHz

K_{VCO} = 78MHz/V

$L_{M(VCO)}$ = –127dBc/Hz at 100kHz offset

Determining Divider Values

Following the Loop Filter Design algorithm, first determine all the divider values. The maximum f_{PFD} while in fractional mode is less than 100MHz, so R must be greater than 1. Further, the minimum N value in fractional mode is 35, setting the lower limit on R:

R = 2

Then, using Equations 4 and 6, calculate the following values:

O =1

f_{PFD} = 50MHz

Then using Equation 5:

$$N+F=\frac{2415.15MHz}{50MHz}=48.303$$

Therefore:

N = 48

F = 0.303

Then, from Equation 3,

NUM = 0.303 • 2^{18} = 79430

Selecting Filter Type and Loop Bandwidth

The next step in the algorithm is choosing the open loop bandwidth. Select the minimum bandwidth resulting from the below constraints.

1) The OSR must be at least 10 (sets absolute maximum BW).

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2) The integrated phase noise due to thermal noise should be minimized, neglecting any modulator noise.

3) However, the loop bandwidth must also be narrow enough to adequately filter the modulator's quantization noise.

FracNWizard reports loop bandwidths resulting from each of the above constraints. The quantization noise constrained results vary according to the shape of the external loop filter. FracNWizard reports an optimal bandwidth for several filter types.

FracNWizard reports the thermal noise optimized loop bandwidth is 31.6kHz. Filter 2 (third order response) has a quantization noise constrained BW of 56.2kHz, making it a good choice. Select Filter 2 and use the smaller of the two bandwidths (31.6kHz) for optimal integrated phase noise. Use Equation 10 to calculate OSR:

$$OSR = \frac{50MHz}{31.6kHz} = 1582$$

Loop Filter Component Selection

Now set loop filter resistor R_Z and charge pump current I_{CP}. Using an I_{CP} of 5.6mA and the specified K_{VCO} of 78MHz/V, FracNWizard uses Equation 11 to determine R_Z:

$$R_Z = \frac{2 \bullet \pi \bullet 31.6k \bullet 48}{5.6m \bullet 78M}$$

$$R_Z = 21.8\Omega$$

For the 3rd order Filter 2, FracNWizard uses modified Equations 7 and 8 to calculate C_I, C_P:

$$C_I = \frac{4}{2 \bullet \pi \bullet 31.6k \bullet 21.8} = 924nF$$

$$C_P = \frac{1}{10.5 \bullet \pi \bullet 31.6k \bullet 21.8} = 44nF$$

FracNWizard calculates R1 and C2 to be:

R1 = 21.8Ω

C2 = 29.3nF

These values are used with the schematic of Figure 15 (with L1 unused).

Status Output Programming

This example will use the STAT pin to indicate the LTC6947 is locked. Program x[2] = 1 to force the STAT pin high whenever the LOCK flag asserts:

Reg01 = h04

Power Register Programming

For correct PLL operation all internal blocks should be enabled. OMUTE may remain asserted (or the $\overline{MUTE}$ pin held low) until programming is complete. For OMUTE = 1:

Reg02 = h02

AUTORST Programming

Set the modulator auto reset option (AUTORST = 1) and the ΔΣ modulator modes (DITHEN = 1, INTN = 0) at the same time:

Reg03 = h06

The ΔΣ modulator will be reset at the end of the SPI write communication burst (assuming an auto-increment write is used to write all registers).

LDO Programming

Use Table 9 and f_{PFD} = 50MHz to determine V(LDO) and LDOV[1:0]:

V(LDO) = 2.3V and LDOV[1:0] = 1

Use LDOV[1:0] and LDOEN = 1 (to enable the LDO) to set Reg04. CPLE should be set to 1 to reduce in-band noise and spurious due to the ΔΣ modulator:

Reg04 = h0E

SEED Programming

The SEED[7:0] value is used to initialize the ΔΣ modulator dither circuitry. Use the default value:

Reg05 = h11

R and N Divider and Numerator Programming

Program registers Reg06 to Reg0A with the previously determined R and N divider and numerator values. Because

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the AUTORST bit was previously set to 1, RSTFN does not need to be set:

Reg06 = h10

Reg07 = h30

Reg08 = h13

Reg09 = h64

Reg0A = h60

Reference Input Settings and Output Divider Programming

From Table 1, FILT = 0 for a 100MHz reference frequency. Next, convert 7dBm into V_{P-P}. For a CW tone, use the following equation with R = 50:

$$V_{P-P} \cong \sqrt{R} \bullet 10^{(dBm-21)/20} \quad (14)$$

This gives V_{P-P} = 1.41V, and, according to Table 2, set BST = 1.

Now program Reg0B, assuming maximum RF± output power (RFO[1:0] = 3 according to Table 10) and OD[2:0] = 1:

Reg0B = h99

Lock Detect and Charge Pump Current Programming

Next, determine the lock indicator window from f_{PFD}. From Table 3 we see that LKWIN[1:0] = 1 with a t_{LWW} of 7.35ns for CPLE = 1 and f_{VCO} = 2415MHz. The LTC6947 will consider the loop locked as long as the phase coincidence at the PFD is within 132°, as calculated below.

$$\text{phase} = 360° \bullet t_{LWW} \bullet f_{PFD} = 360 \bullet 7.35n \bullet 50M$$

$$\approx 132°$$

Choosing the correct COUNTS value depends upon the OSR. Smaller ratios dictate larger COUNTS values, although application requirements will vary. A COUNTS value of 32 will work for the OSR ratio of 1582. From Table 5, LKCT[1:0] = 1 for 32 counts.

Using Table 6 with the previously selected I_{CP} of 5.6mA gives CP[3:0] = 5. This gives enough information to program Reg0C:

Reg0C = h2D

Charge Pump Function Programming

The DC1846 includes an LT1678I op amp in the loop filter. This allows the circuit to reach the voltage range specified for the VCO's tuning input. However, it also adds an inversion in the loop transfer function. Compensate for this inversion by setting CPINV = 1.

This example does not use the additional voltage clamp features to allow fault condition monitoring. The loop feedback provided by the op amp will force the charge pump output to be equal to the op amp positive input pin's voltage. Disable the charge pump voltage clamps by setting CPCHI = 0 and CPCLO = 0. Disable all the other charge pump functions (CPMID, CPRST, CPUP, and CPDN) to allow the loop to lock:

Reg0D = h10

The loop should now lock. Now un-mute the output by setting OMUTE = 0 (assumes the $\overline{\text{MUTE}}$ pin is high).

Reg02 = h00

REFERENCE SOURCE CONSIDERATIONS

A high quality signal must be applied to the REF± inputs as they provide the frequency reference to the entire PLL. As mentioned previously, to achieve the part's in-band phase noise performance, apply a CW signal of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 40V/µs.

The LTC6947 may be driven single-ended to CMOS levels (greater than $2.7V_{P-P}$). Apply the reference signal at REF^+, and bypass REF^- to GND with a 47pF capacitor. The BST bit must also be set to 0, according to guidelines given in Table 2.

The LTC6947 achieves an integer mode in-band normalized phase noise floor $L_{NORM(INT)}$ = –226dBc/Hz typical, and a fractional mode phase noise floor $L_{NORM(FRAC)}$ = –225 dBc/Hz typical. To calculate its equivalent input phase noise floor L_{IN}, use the following Equation 15.

$$L_{IN} = L_{NORM} + 10 \bullet \log_{10}(f_{REF}) \quad (15)$$

For example, using a 10MHz reference frequency in integer mode gives an input phase noise floor of –156dBc/Hz. The reference frequency source's phase noise must be at

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least 3dB better than this to prevent limiting the overall system performance.

IN-BAND OUTPUT PHASE NOISE

The in-band phase noise floor L_{OUT} produced at f_{RF} may be calculated by using Equation 16.

$$L_{OUT} = L_{NORM} + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}(f_{RF}/f_{PFD}) \quad (16)$$

or

$$L_{OUT} \approx L_{NORM} + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}(N/O)$$

where L_{NORM} is –226dBc/Hz for integer mode and –225dBc/Hz for fractional mode.

As can be seen, for a given PFD frequency f_{PFD}, the output in-band phase noise increases at a 20dB-per-decade rate with the N divider count. So, for a given output frequency f_{RF}, f_{PFD} should be as large as possible (or N should be as small as possible) while still satisfying the application's frequency step size requirements.

OUTPUT PHASE NOISE DUE TO 1/f NOISE

In-band phase noise at very low offset frequencies may be influenced by the LTC6947's 1/f noise, depending upon f_{PFD}. Use the normalized in-band 1/f noise $L_{1/f}$ of –274dBc/Hz with Equation 17 to approximate the output 1/f phase noise at a given frequency offset f_{OFFSET}.

$$L_{OUT(1/f)}(f_{OFFSET}) = L_{1/f} + 20 \bullet \log_{10}(f_{RF}) - 10 \bullet \log_{10}(f_{OFFSET}) \quad (17)$$

Unlike the in-band noise floor L_{OUT}, the 1/f noise $L_{OUT(1/f)}$ does not change with f_{PFD}, and is not constant over offset frequency. See Figure 16 for an example of integer mode in-band phase noise for f_{PFD} equal to 3MHz and 100MHz. The total phase noise will be the summation of L_{OUT} and $L_{OUT(1/f)}$.

VCO INPUT MATCHING

The VCO± inputs may be used differentially or single-ended. Each input provides a single-ended 121Ω resistance to aid in impedance matching at high frequencies. The inputs are self-biased and must be AC-coupled using 100pF capacitors (or 270pF for VCO frequencies less than 500MHz).

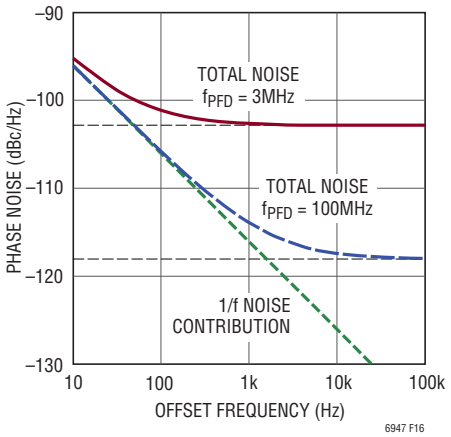

Figure 16. Theoretical Integer Mode In-Band Phase Noise, f_{RF} = 2500MHz

The inputs may be used single-ended by applying the AC-coupled VCO frequency at VCO+ and bypassing VCO– to GND with a 100pF capacitor (270pF for frequencies less than 500MHz). Measured VCO+ s-parameters (with VCO– bypassed with 100pF to GND) are shown in Table 13 to aid in the design of external impedance matching networks.

Table 13. Single-Ended VCO+ Input Impedance

FREQUENCY (MHz)	IMPEDANCE (Ω)	S11 (dB)
250	118 – j78	–5.06
500	83.6 – j68.3	–5.90
1000	52.8 – j56.1	–6.38
1500	35.2 – j41.7	–6.63
2000	25.7 – j30.2	–6.35
2500	19.7 – j20.6	–5.94
3000	17.6 – j11.2	–6.00
3500	17.8 – j3.92	–6.41
4000	19.8 + j4.74	–7.20
4500	21.5 + j15.0	–7.12
5000	21.1 + j19.4	–6.52
5500	27.1 + j22.9	–7.91
6000	38.3 + j33.7	–8.47
6500	36.7 + j42.2	–6.76
7000	46.2 + j40.9	–8.11
7500	76.5 + j36.8	–9.25
8000	84.1+ j52.2	–7.27