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1.4GHz Low Phase Noise, Low Jitter PLL with Clock Distribution

FEATURES

- **Low Phase Noise and Jitter**
- **Additive Jitter: 18fs$_{RMS}$ (12kHz to 20MHz)**
- **Additive Jitter: 85fs$_{RMS}$ (10Hz to Nyquist)**
- **EZSync™ Multichip Clock Edge Synchronization**
- Full PLL Core with Lock Indicator
- –226dBc/Hz Normalized In-Band Phase Noise Floor
- –274dBc/Hz Normalized 1/f Phase Noise
- 1.4GHz Maximum VCO Input Frequency
- Four Independent, Low Noise 1.4GHz LVPECL Outputs
- One LVDS/CMOS Configurable Output
- Five Independently Programmable Dividers Covering All Integers from 1 to 63
- Five Independently Programmable VCO Clock Cycle Delays Covering All Integers from 0 to 63
- –40°C to 105°C Junction Temperature Range

APPLICATIONS

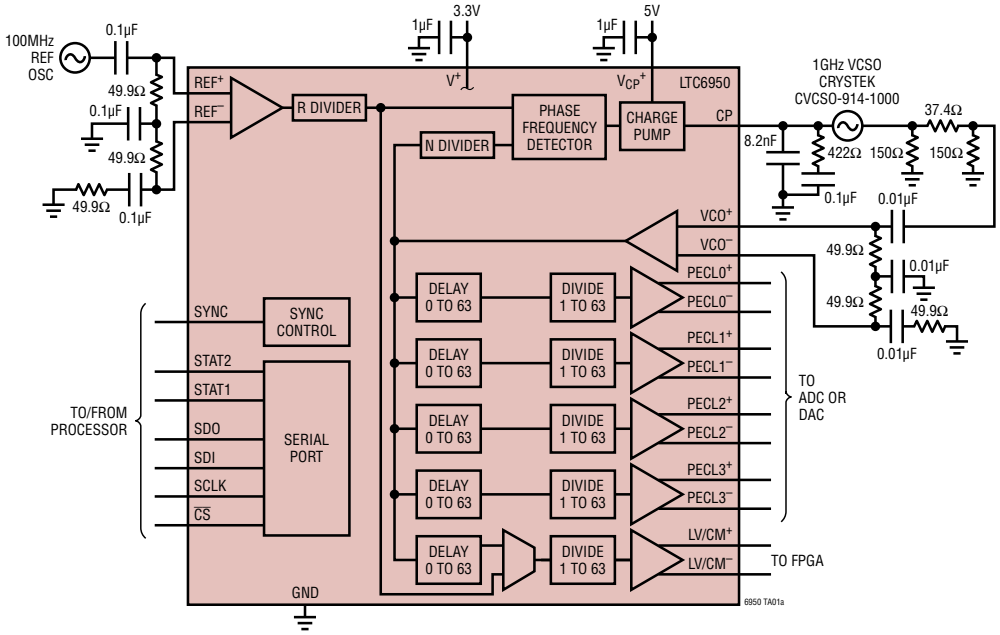
- Clocking High Speed, High Resolution ADCs, DACs and Data Acquisition Systems
- Low Jitter Clock Generation and Distribution

DESCRIPTION

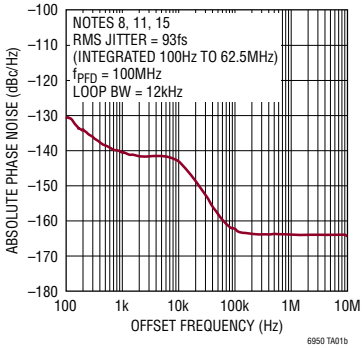
The LTC®6950 is a low phase noise integer-N frequency synthesizer core with clock distribution. The LTC6950 delivers the low phase noise clock signals demanded in high frequency, high resolution data acquisition systems.

The frequency synthesizer contains a full low noise PLL core with a programmable reference divider (R), a programmable feedback divider (N), a phase/frequency detector (PFD) and a low noise charge pump (CP). The clock distribution section of the LTC6950 delivers up to five outputs based on the VCO input. Each output is individually programmed to divide the VCO input frequency by any integer from 1 to 63 and to delay the output by 0 to 63 VCO clock cycles. Four of the outputs feature very low noise, low skew LVPECL logic signals capable of operation up to 1.4GHz. The fifth output is selectable as either an LVDS (800MHz) or CMOS (250MHz) logic type. This output is also programmed to produce an output signal based on either the VCO input or the reference divider output.

TYPICAL APPLICATION



PECLx Closed-Loop Phase Noise, f_{VCSO} = 1GHz, Mx[5:0] = 8, f_{PECLx} = 125MHz

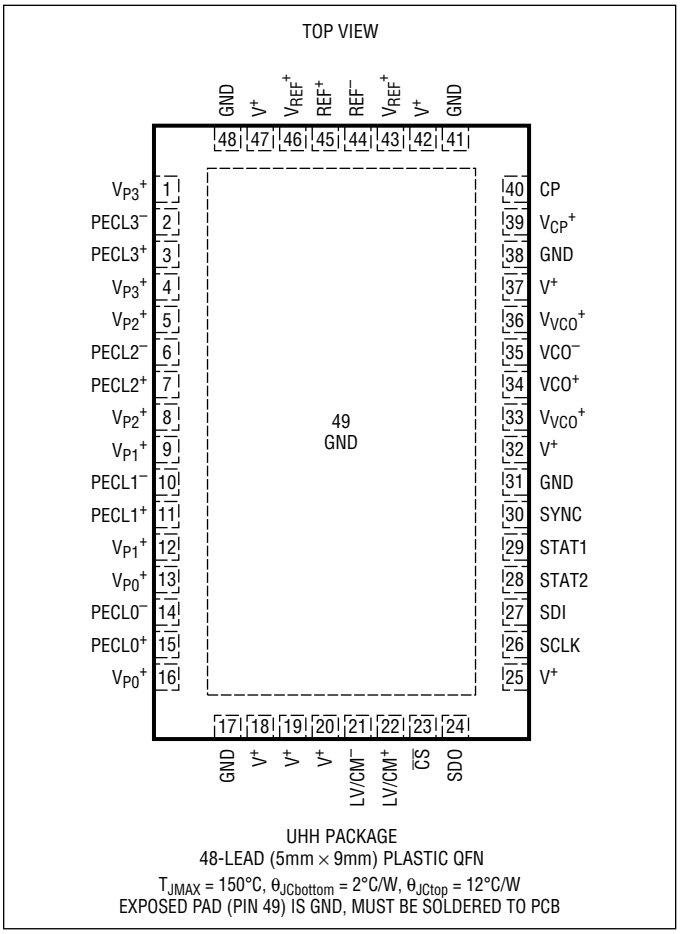


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
V^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+,
V_{VCO}^+, and V_{REF}^+ to GND 3.6V
V_{CP}^+ to GND 5.5V
CP Voltage ..... –0.3V to (V_{CP}^+ + 0.3V)
$\overline{CS}$, SCLK, SDI, SDO, SYNC, VCO^+, VCO^-,
REF^+, REF^-, Voltage ..... –0.3V to (V^+ + 0.3V)
$PECL3^-$, $PECL3^+$, $PECL2^-$, $PECL2^+$, $PECL1^-$,
$PECL1^+$, $PECL0^-$, $PECL0^+$, LV/CM^-, LV/CM^+,
STAT2, STAT1 ..... (Note 28)
Operating Junction Temperature Range, T_J (Note 2)
LTC6950I ..... –40°C to 105°C
Junction Temperature, T_{JMAX} ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHH PACKAGE
48-LEAD (5mm × 9mm) PLASTIC QFN
T_{JMAX} = 150°C, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 12°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC6950IUHH#PBF	LTC6950IUHH#TRPBF	6950	48-Lead (5mm × 9mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Inputs (REF⁺, REF⁻)							
f_{REF}	Input Frequency		●	2		250	MHz
V_{REF}	Input Signal Level	Single-Ended	●		0.8	1.5	V_{P-P}
	Minimum Input Slew Rate				10		V/µs
DC_{REF}	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.9	2.05	2.2	V
	Minimum Common Mode Level	400mV_{P-P} Differential Input			1.5		V
	Maximum Common Mode Level	400mV_{P-P} Differential Input			2.3		V
	Minimum Input Signal Detected	NO_REF = 0, 2MHz ≤ f_{REF} ≤ 250MHz, Sine Wave			350		mV_{P-P}
	Maximum Input Signal Not Detected	NO_REF = 1, 2MHz ≤ f_{REF} ≤ 250MHz, Sine Wave			100		mV_{P-P}
	Input Resistance	Differential	●	1.45	2.2	3.0	kΩ
	Input Capacitance	Differential			1		pF
VCO Inputs (VCO⁺, VCO⁻)							
f_{VCO}	Input Frequency		●			1400	MHz
V_{VCO}	Input Signal Level	Single-Ended	●	0.2	0.8	1.5	V_{P-P}
	Input Slew Rate		●	100			V/µs
DC_{VCO}	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.9	2.05	2.2	V
	Minimum Common Mode Level	400mV_{P-P} Differential Input			1.5		V
	Maximum Common Mode Level	400mV_{P-P} Differential Input			2.3		V
	Minimum Input Signal Detected	NO_VCO = 0, 30MHz ≤ f_{VCO} ≤ 1400MHz, Sine Wave			350		mV_{P-P}
	Maximum Input Signal Not Detected	NO_VCO = 1, 30MHz ≤ f_{VCO} ≤ 1400MHz, Sine Wave			100		mV_{P-P}
	Input Resistance	Differential	●	1.45	2.2	3.0	kΩ
	Input Capacitance	Differential			1		pF
Phase/Frequency Detector (PFD)							
f_{PFD}	Input Frequency		●			100	MHz
	Up/Down Pulse Width, Standard	CPWIDE = 0			1		ns
	Up/Down Pulse Width, Wide	CPWIDE = 1			2		ns
Lock Indicator (LOCK)							
t_{LWW}	Lock Window Width	LKWIN[1:0] = 0 LKWIN[1:0] = 1 LKWIN[1:0] = 2 LKWIN[1:0] = 3			3 10 30 90		ns ns ns ns
t_{LWHYS}	Lock Window Hysteresis	Increase in t_{LWW} Moving from Locked State to Unlocked State			22		%
	Lock Entry PFD Counts	LKCT[1:0] = 0 LKCT[1:0] = 1 LKCT[1:0] = 2 LKCT[1:0] = 3			32 128 512 2048		Counts Counts Counts Counts

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Pump (CP)							
I_{CP}	Output Source/Sink Current Range	12 Settings (See Table 3)		0.25		11.2	mA
	Output Source/Sink Current Accuracy	I_{CP} = 250µA to 1.4mA, $V_{CP} = V_{CP}^+/2$ I_{CP} = 2mA to 11.2mA, $V_{CP} = V_{CP}^+/2$		–7.5 –6		7.5 6	% %
	Output Source/Sink Current Matching	I_{CP} = 250µA to 1.4mA, $V_{CP} = V_{CP}^+/2$ I_{CP} = 2mA to 11.2mA, $V_{CP} = V_{CP}^+/2$		–7 –3.5		7 3.5	% %
	Output Source/Sink Current vs Output Voltage Sensitivity	$0.85V \le V_{CP} \le (V_{CP}^+ - 0.85V)$ $0.95V \le V_{CP} \le (V_{CP}^+ - 0.95V)$		–7 –2	0.1 0.1	1.5 1	% %
	Output Current vs Temperature	$V_{CP} = V_{CP}^+/2$	●		170		ppm/°C
	Output Hi-Z Leakage Current	I_{CP} = 350µA, CPCLO = CPCHI = 0 (Note 3) I_{CP} = 700µA, CPCLO = CPCHI = 0 (Note 3) I_{CP} = 11.2mA, CPCLO = CPCHI = 0 (Note 3)	● ● ●		0.5 0.5 1	10 10 10	nA nA nA
$V_{CLMP(LO)}$	Low Clamp Voltage	CPCLO = 1			0.9		V
$V_{CLMP(HI)}$	High Clamp Voltage	CPCHI = 1			$V_{CP}^+ - 0.9$		V
V_{MID}	Mid Supply Output Bias Ratio	Referenced to (V_{CP}^+ – GND)	●	0.47	0.49	0.53	V/V
R_{MID}	Mid Supply Mode Impedance				8.8		kΩ
Reference Divider (R)							
R	Divide Range	All Integers Included	●	1		1023	Cycles
VCO Divider (N)							
N	Divide Range	All Integers Included	●	1		2047	Cycles
Digital Inputs ($\overline{CS}$, SDI, SCLK, SYNC)							
V_{IH}	Input High Voltage	$\overline{CS}$, SDI, SCLK, SYNC	●	1.55			V
V_{IL}	Input Low Voltage	$\overline{CS}$, SDI, SCLK, SYNC	●			0.8	V
V_{IHYS}	Input Voltage Hysteresis	$\overline{CS}$, SDI, SCLK, SYNC			250		mV
	Input Current	$\overline{CS}$, SDI, SCLK, SYNC	●	–1		1	µA
Digital Outputs (SDO, STAT1, STAT2)							
I_{OH}	High Level Output Current	SDO, STAT1, STAT2, $V_{OH} = V^+ - 400mV$	●		–2.4	–1.4	mA
I_{OL}	Low Level Output Current	SDO, STAT1, STAT2, V_{OH} = 400mV	●	2.0	3.4		mA
	SDO Hi-Z Current		●	–1		1	µA
Digital Timing Specifications (See Figures 21 and 22)							
t_{CKH}	SCLK High Pulse Width		●	25			ns
t_{CKL}	SCLK Low Pulse Width		●	25			ns
t_{CSST}	$\overline{CS}$ Setup Time		●	10			ns
t_{CSHT}	$\overline{CS}$ Hold Time		●	10			ns
t_{CSH}	$\overline{CS}$ High Pulse Width		●	10			ns
t_{CS}	SDI to SCLK Setup Time		●	6			ns
t_{CH}	SDI to SCLK Hold Time		●	6			ns
t_{DO}	SDO Propagation Delay	C_{LOAD} = 30pF			16		ns
t_{SYNCH}	SYNC High Pulse Width		●	1			ms
t_{SYNCL}	Minimum SYNC Low Pulse Width	Before Next SYNC High Pulse			1		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+$ = 3.3V, V_{CP}^+ = 5V unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Divider (M)							
Mx[5:0]	Divider Range M0[5:0], M1[5:0], M2[5:0], M3[5:0], M4[5:0]	All Integers Included	●	1		63	Cycles
DELx[5:0]	Divider Delay in VCO Clock Cycles DEL0[5:0], DEL1[5:0], DEL2[5:0], DEL3[5:0], DEL4[5:0]	All Integers Included	●	0		63	Cycles
PECLx Clock Outputs ($PECL0^+$, $PECL0^-$, $PECL1^+$, $PECL1^-$, $PECL2^+$, $PECL2^-$, $PECL3^+$, $PECL3^-$)							
f_{PECLx}	Frequency	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V)	●			1400	MHz
V_{CM}	Common Mode Voltage (Outputs Static)	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V)	●	V_{Px}^+ – 1.68	V_{Px}^+ – 1.48	V_{Px}^+ – 1.25	V
$\|V_{OD}\|$	Differential Voltage (Outputs Static)	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V) Differential Termination = 100Ω, Internal Bias On	●	610	800 800	1050	mV_{PK} mV_{PK}
t_{RISE}	Rise Time, 20% to 80%	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V) Differential Termination = 100Ω, Internal Bias On			135 135		ps ps
t_{FALL}	Fall Time, 80% to 20%	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V) Differential Termination = 100Ω, Internal Bias On			135 135		ps ps
DC_{PECL}	Duty Cycle	Mx[5:0] = 1 Mx[5:0] > 1 (Even or Odd)	 ●	 45	DC_{VCO} 50	 55	% %
t_{PDP3}	Propagation Delay from VCO to PECL3	M3[5:0] = 1, FILTV = 0 M3[5:0] = 1, FILTV = 1 M3[5:0] > 1, FILTV = 0	● ●	285 335	495 700 560	660 745	ps ps ps
	Propagation Delay from VCO to PECL3, Temperature Variation	M3[5:0] = 1, FILTV = 0 M3[5:0] = 1, FILTV = 1 M3[5:0] > 1, FILTV = 0	● ● ●		0.35 0.50 0.45		ps/°C ps/°C ps/°C
t_{SKEWPx}	Skew, from PECL3 to PECL0	M0[5:0] = M3[5:0] = 1 M0[5:0] = M3[5:0] > 1	● ●	–50 –50	–1.0 –1.5	50 50	ps ps
	Skew, from PECL3 to PECL1	M1[5:0] = M3[5:0] = 1 M1[5:0] = 1, M3[5:0] > 1 M1[5:0] > 1, M3[5:0] = 1 M1[5:0] = M3[5:0] > 1	● ● ● ●	–50 –125 5 –50	4.5 –60 69 5	50 0 135 50	ps ps ps ps
	Skew, from PECL3 to PECL2	M2[5:0] = M3[5:0] = 1 M2[5:0] = M3[5:0] > 1	● ●	–50 –50	5 5.5	50 50	ps ps
	Skew, All PECLx Outputs	FILTV = 0, Same Part	●			55	ps
	Skew, Same PECLx Output	FILTV = 0, Across Multiple Parts (Note 4)	●			320	ps
	Skew, All PECLx Outputs	FILTV = 0, Across Multiple Parts (Note 5)	●			330	ps

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+$ = 3.3V, V_{CP}^+ = 5V unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Clock Outputs (LV/CM⁺ and LV/CM⁻)							
f_{LVDS}	Frequency	Differential Termination = 100Ω	●			800	MHz
$\|V_{OD}\|$	Differential Voltage (Outputs Static)	Differential Termination = 100Ω	●	280	400	525	mV_{PK}
$\|\Delta V_{OD}\|$	Delta V_{OD}	Differential Termination = 100Ω	●		5	60	mV
V_{OS}	Offset Voltage (Outputs Static)	Differential Termination = 100Ω	●	1.125	1.23	1.375	V
$\|\Delta V_{OS}\|$	Delta V_{OS}	Differential Termination = 100Ω	●		5	50	mV
t_{RISE}	Rise Time, 20% to 80%	Differential Termination = 100Ω	●		140		ps
t_{FALL}	Fall Time, 80% to 20%	Differential Termination = 100Ω	●		130		ps
$\|I_{SA}\|$, $\|I_{SB}\|$	Short Circuit Current to Common	Shorted to GND			4.2		mA
$\|I_{SAB}\|$	Short Circuit Current to Complementary				4.2		mA
DC_{LVDS}	Duty Cycle	RDIVOUT = 0, M4[5:0] = 1			DC_{VCO}		%
		RDIVOUT = 1, R[9:0] = 1, M4[5:0] = 1			DC_{REF}		%
		RDIVOUT = 0, M4[5:0] > 1 (Even or Odd)	●	45	50	55	%
		RDIVOUT = 1, M4[5:0] > 1 (Even)			50		%
		RDIVOUT = 1, R[9:0] = 3, M4[5:0] = 3			56		%
		RDIVOUT = 1, R[9:0] = 1023, M4[5:0] = 3			33		%
t_{PD}	Propagation Delay from VCO to LVDS with RDIVOUT Disabled	M4[5:0] = 1, FILTV = 0			1.85		ns
		M4[5:0] = 1, FILTV = 1			2.05		ns
		M4[5:0] > 1, FILTV = 0			1.91		ns
	Propagation Delay from REF to LVDS with RDIVOUT Enabled	M4[5:0] = 1, R = 1, FILTR = 0			2.26		ns
		M4[5:0] = 1, R = 1, FILTR = 1			3.12		ns
		M4[5:0] > 1, R = 1, FILTR = 0			2.32		ns
		M4[5:0] = 1, R > 1, FILTR = 0			2.40		ns
		M4[5:0] > 1, R > 1, FILTR = 0			2.47		ns
	Propagation Delay from VCO to LVDS with RDIVOUT Disabled, Temperature Variation	M4[5:0] = 1, FILTV = 0	●		4.05		ps/°C
		M4[5:0] = 1, FILTV = 1	●		4.20		ps/°C
		M4[5:0] > 1, FILTV = 0	●		4.00		ps/°C
	Propagation Delay from REF to LVDS with RDIVOUT Enabled, Temperature Variation	M4[5:0] = 1, R = 1, FILTR = 0	●		4.55		ps/°C
		M4[5:0] = 1, R = 1, FILTR = 1	●		4.50		ps/°C
		M4[5:0] > 1, R = 1, FILTR = 0	●		4.53		ps/°C
		M4[5:0] = 1, R > 1, FILTR = 0	●		4.55		ps/°C
		M4[5:0] > 1, R > 1, FILTR = 0	●		4.70		ps/°C
t_{SKEWL}	Skew, from PECL3 to LVDS with RDIVOUT Disabled	M3[5:0] = M4[5:0] = 1			1.32		ns
		M3[5:0] = M4[5:0] > 1			1.32		ns
	Skew, from PECL3 to LVDS with RDIVOUT Disabled, Temperature Variation	M3[5:0] = M4[5:0] = 1	●		3.70		ps/°C
		M3[5:0] = M4[5:0] > 1	●		3.55		ps/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Clock Outputs (LV/CM⁺ and LV/CM⁻)							
f_{CMOS}	Frequency		●			250	MHz
V_{OH}	High Voltage (Outputs Static)	2.5mA Load	●	$V^+ – 0.4$			V
V_{OL}	Low Voltage (Outputs Static)	2.5mA Load	●			0.4	V
t_{RISE}	Rise Time, 20% to 80%	C_{LOAD} = 2pF, CMSINV = 1			1010		ps
t_{FALL}	Fall Time, 80% to 20%	C_{LOAD} = 2pF, CMSINV = 1			840		ps
DC_{CMOS}	Duty Cycle	RDIVOUT = 0, M4[5:0] = 1 RDIVOUT = 1, R[9:0] = 1, M4[5:0] = 1 RDIVOUT = 0, M4[5:0] > 1 (Even or Odd) RDIVOUT = 1, M4[5:0] > 1 (Even) RDIVOUT = 1, R[9:0] = 3, M4[5:0] = 3 RDIVOUT = 1, R[9:0] = 1023, M4[5:0] = 3			DC_{VCO} DC_{REF} 50 50 56 33		% % % % % %
t_{PD}	Propagation Delay from VCO to CMOS with RDIVOUT Disabled	M4[5:0] = 1, FILTV = 0, CMSINV = 1 M4[5:0] = 1, FILTV = 1, CMSINV = 1 M4[5:0] > 1, FILTV = 0, CMSINV = 1			2.12 2.32 2.20		ns ns ns
	Propagation Delay from REF to CMOS with RDIVOUT Enabled	M4[5:0] = 1, R = 1, FILTR = 0, CMSINV = 1 M4[5:0] = 1, R = 1, FILTR = 1, CMSINV = 1 M4[5:0] > 1, R = 1, FILTR = 0, CMSINV = 1 M4[5:0] = 1, R > 1, FILTR = 0, CMSINV = 1 M4[5:0] > 1, R > 1, FILTR = 0, CMSINV = 1			2.55 3.40 2.60 2.69 2.76		ns ns ns ns ns
	Propagation Delay from VCO to CMOS with RDIVOUT Disabled, Temperature Variation	M4[5:0] = 1, FILTV = 0, CMSINV = 1 M4[5:0] = 1, FILTV = 1, CMSINV = 1 M4[5:0] > 1, FILTV = 0, CMSINV = 1	● ● ●		4.90 5.10 5.05		ps/°C ps/°C ps/°C
	Propagation Delay from REF to CMOS with RDIVOUT Enabled, Temperature Variation	M4[5:0] = 1, R = 1, FILTR = 0, CMSINV = 1 M4[5:0] = 1, R = 1, FILTR = 1, CMSINV = 1 M4[5:0] > 1, R = 1, FILTR = 0, CMSINV = 1 M4[5:0] = 1, R > 1, FILTR = 0, CMSINV = 1 M4[5:0] > 1, R > 1, FILTR = 0, CMSINV = 1	● ● ● ● ●		5.90 5.80 5.85 5.90 6.00		ps/°C ps/°C ps/°C ps/°C ps/°C
t_{SKEWC}	Skew, from PECL3 to CMOS with RDIVOUT Disabled	M3[5:0] = M4[5:0] = 1, CMSINV = 1 M3[5:0] = M4[5:0] > 1, CMSINV = 1 M3[5:0] = M4[5:0] = 1, CMSINV = 0			1.60 1.60 1.83		ns ns ns
	Skew, from PECL3 to CMOS with RDIVOUT Disabled, Temperature Variation	M3[5:0] = M4[5:0] = 1, CMSINV = 1 M3[5:0] = M4[5:0] > 1, CMSINV = 1 M3[5:0] = M4[5:0] = 1, CMSINV = 0	● ● ●		4.55 4.60 4.15		ps/°C ps/°C ps/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
	V^+, V_{REF}^+, V_{VCO}^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+ Supply Voltage Range		●	3.15	3.3	3.45	V
	V_{CP}^+ Supply Voltage Range		●	V^+		5.25	V
Supply Current							
	V_{CP}^+ Supply Current	I_{CP} = 11.2mA	●		35	43	mA
		I_{CP} = 4mA	●		21	25	mA
		I_{CP} = 1mA	●		13	16	mA
		I_{CP} = 0.5mA	●		11.5	15	mA
		I_{CP} = 250µA	●		11	14	mA
		PDALL = 1	●		0.235	0.6	mA
	Sum of V^+, V_{REF}^+, V_{VCO}^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+ Supply Currents (Changes to Default Power-Up Configuration Noted)	f_{VCO} = 800MHz, f_{REF} = 106.25MHz + Internal Bias Enabled, All PECLx	●		485	550	mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + Termination = 50Ω to (V_{Px}^+ – 2V), All PECLx	●		495	565	mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + External 150Ω Bias, All PECLx			510		mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + No Internal/External Bias, All PECLx	●		405	460	mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + IBIAS0 = 1, IBIAS3 = 1 + PD_DIV1 = 1, PD_DIV2 = 1, PD_DIV4 = 1			260		mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + IBIAS0 = 1, IBIAS3 = 1 + PD_DIV1 = 1, PD_DIV2 = 1, PD_DIV4 = 1 + M0[5:0] = M3[5:0] = 1			220		mA
		PDALL = 1	●		1.6	2.2	mA
Supply Current Delta (Note 6)							
	REF Input Signal Present Circuit On	PDREFAC = 0	●		2.3	3.5	mA
	VCO Input Signal Present Circuit On	PDVCOAC = 0	●		0.6	1.0	mA
	VCO Input On	PDALL = 0, PDREFAC = 1, PDVCOAC = 1, PDPLL = 1, All PD_DIVx = 1, All PD_OUTx = 1,	●		32	40	mA
	REF Input, RDIV, NDIV, PFD, CP On	I_{CP}^+ Current, PDPLL = 0, I_{CP} = 11.2mA setting	●		35	43	mA
		All Other Current, PDPLL = 0	●		73	90	mA
	PECLx Output Divider On PECLx = PECL0, PECL1, PECL2, PECL3	PD_DIVx = 0, Mx[5:0] = 1	●		28	35	mA
		PD_DIVx = 0, Mx[5:0] > 1	●		46	56	mA
	LV/CM Output Divider On	PD_DIV4 = 0, M4[5:0] = 1	●		34	41	mA
		PD_DIV4 = 0, M4[5:0] > 1	●		52	63	mA
	PECLx Output Driver On PECLx = PECL0, PECL1, PECL2, PECL3	PD_OUTx = 0, Termination = 50Ω to (V_{Px}^+ – 2V)	●		32	45	mA
		PD_OUTx = 0, IBIASx = 1 (Internal Bias On)	●		30	38	mA
		PD_OUTx = 0, No Internal/External Bias	●		10	15	mA
	LV/CM Output Driver On	PD_OUT4 = 0, LVDS at 800MHz	●		22	28	mA
		PD_OUT4 = 0, CMOS at 50MHz	●		12	16	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VCO to PECLx (PECL0$^+$, PECL0$^-$, PECL1$^+$, PECL1$^-$, PECL2$^+$, PECL2$^-$, PECL3$^+$, PECL3$^-$) Additive Phase Noise/Time Jitter (Note 7)							
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, Mx[5:0] = 1, f_{PECLx} = 245.76MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–135 –144 –153 –158 –159.5 –159.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, Mx[5:0] = 1, f_{PECLx} = 245.76MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 122.88MHz Integration Bandwidth			44 108		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, Mx[5:0] = 4, f_{PECLx} = 61.44MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–146 –156 –164 –168 –168 –168		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, Mx[5:0] = 4, f_{PECLx} = 61.44MHz	12kHz to 20MHz Integration Bandwidth 10kHz to 30.72MHz Integration Bandwidth			69 85		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 1, f_{PECLx} = 622.08MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–128 –136 –146 –153.5 –155.5 –155.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 1, f_{PECLx} = 622.08MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 311.04MHz Integration Bandwidth			28 108		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 4, f_{PECLx} = 155.52MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–139 –148 –157 –163 –163.5 –163.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 4, f_{PECLx} = 155.52MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 77.76MHz Integration Bandwidth			45 85		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 16, f_{PECLx} = 38.88MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–150 –160 –166 –169 –169.5 –169.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Phase Noise: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 1, f_{PECLx} = 1400MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–123 –131 –140 –147 –151 –152.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 1, f_{PECLx} = 1400MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 700MHz Integration Bandwidth			18 98		fs_{RMS} fs_{RMS}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Phase Noise: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 4, f_{PECLx} = 350MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–132 –143 –151 –157 –160 –160		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 4, f_{PECLx} = 350MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 175MHz Integration Bandwidth			29 85		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 16, f_{PECLx} = 87.5MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–144 –155 –163 –166.5 –166.5 –166.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 16, f_{PECLx} = 87.5MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 43.75MHz Integration Bandwidth			56 85		fs_{RMS} fs_{RMS}
VCO to LVDS Additive Phase Noise/Time Jitter (Note 7)							
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 1, f_{LVDS} = 245.76MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–122 –132 –144 –151.5 –155 –156		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 1, f_{LVDS} = 245.76MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 122.88MHz Integration Bandwidth			65 155		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 4, f_{LVDS} = 61.44MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–133 –140 –153 –161 –163 –163.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 4, f_{LVDS} = 61.44MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 30.72MHz Integration Bandwidth			110 138		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 1, f_{LVDS} = 622.08MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–113 –124 –135 –143 –147 –151		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 1, f_{LVDS} = 622.08MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 311.04MHz Integration Bandwidth			47 170		fs_{RMS} fs_{RMS}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+$ = 3.3V, V_{CP}^+ = 5V unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 4, f_{LVDS} = 155.52MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–125 –134 –147 –154 –158 –159		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 4, f_{LVDS} = 155.52MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 77.76MHz Integration Bandwidth			73 138		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 16, f_{LVDS} = 38.88MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–137 –145 –156 –164 –165 –165		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
VCO to CMOS Additive Phase Noise/Time Jitter (Note 7)							
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 1, f_{CMOS} = 245.76MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–120 –130 –143 –150.5 –155 –157		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 1, f_{CMOS} = 245.76MHz	12kHz to 20MHz integration bandwidth 10Hz to 122.88MHz integration bandwidth			57 135		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 4, f_{CMOS} = 61.44MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–132 –140 –153 –161 –164 –164		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 4, f_{CMOS} = 61.44MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 30.72MHz integration bandwidth			104 125		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 4, f_{CMOS} = 155.52MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–125 –135 –146 –155 –159 –160		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 4, f_{CMOS} = 155.52MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 77.76MHz Integration Bandwidth			65 125		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 16, f_{CMOS} = 38.88MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–136 –146 –157 –163 –165 –165		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Absolute Phase Noise and Spurious Energy							
$L_{M(MIN)}$	Output Phase Noise Floor (Notes 8, 9)	Mx[5:0] = 1, f_{PECLx} = 1GHz Mx[5:0] = 4, f_{PECLx} = 250MHz Mx[5:0] = 16, f_{PECLx} = 62.5MHz Mx[5:0] = 40, f_{PECLx} = 25MHz			–155 –161 –167 –171		dBc/Hz dBc/Hz dBc/Hz dBc/Hz
$L_{M(NORM)}$	Normalized In-Band Phase Noise Floor	I_{CP} = 11.2mA (Notes 10, 11, 12)			–226		dBc/Hz
$L_{M(NORM-1/f)}$	Normalized In-Band 1/f Phase Noise	I_{CP} = 11.2mA (Notes 10, 13)			–274		dBc/Hz
$L_{M(IB)}$	In-Band Phase Noise Floor	f_{OUT} = 1GHz (Notes 10, 11, 12, 14)			–112.5		dBc/Hz
	Integrated Phase Noise from 100Hz to 62.5MHz	Mx[5:0] = 8, f_{PECLx} = 125MHz (Notes 8, 11, 15)			93		fs_{RMS}
	Spurious Signals, PLL Locked	f_{PFD} = 5MHz (Notes 16, 17, 18) f_{PFD} = 10MHz (Notes 8, 11, 16, 19)			–105 –88		dBc dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6950IUHH is guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 105°C. Under maximum operating conditions, air flow or heat sinking may be required to maintain a junction temperature of 105°C or lower. It is strongly recommended that the Exposed Pad (pin 49) be soldered directly to the ground plane with an array of thermal vias as described in the Applications information section.

Note 3: For $0.9V \le V_{CP} \le (V_{CP}^+ – 0.9V)$.

Note 4: This parameter is the difference in the propagation delay over multiple parts for the same PECLx output at the same supply voltages, at the same temperature and in the same configuration.

Note 5: This parameter is the difference in the propagation delay over multiple parts for any two PECLx outputs at the same supply voltages, at the same temperature and in the same configuration.

Note 6: An LTC6950 configured with an individual block powered down will add the specified supply current delta when powered up. Similarly, the specified supply current delta will subtract from the total chip supply current when the block is powered down. Except when noted, the supply current comes from the 3.3V supplies (V^+, V_{REF}^+, V_{VCO}^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+)

Note 7: Additive phase noise and jitter are the phase noise added by the LTC6950. It does not include noise from the external signal source.

Note 8: VCO is a Crystek CVCSO-914-1000 voltage controlled SAW oscillator

Note 9: f_{VCO} = 1GHz, f_{OFFSET} = 5MHz

Note 10: Measured inside the loop bandwidth with the loop locked.

Note 11: Reference frequency supplied by a Wenzel 501-04517D, f_{REF} = 100MHz.

Note 12: Output phase noise floor is calculated from normalized phase noise floor by $L_{M(OUT)} = –226 + 10\log_{10}(f_{PFD}) + 20\log_{10}(f_{OUT}/f_{PFD})$.

Note 13: Output 1/f phase noise is calculated from normalized 1/f phase noise by $L_{M(OUT-1/f)} = –274 + 20\log_{10}(f_{OUT}) – 10\log_{10}(f_{OFFSET})$.

Note 14: I_{CP} = 11.2mA, f_{PFD} = 5MHz, Loop BW = 13.6kHz, IBIASx = 1.

Note 15: I_{CP} = 11.2mA, f_{PFD} = 100MHz, Loop BW = 12kHz, IBIASx = 1.

Note 16: Measured using DC1795.

Note 17: Reference frequency is supplied by a Wenzel 501-04609A, f_{REF} = 10MHz.

Note 18: VCO is a Crystek CVSS-945-125.000 voltage controlled crystal oscillator. I_{CP} = 11.2mA, f_{PFD} = 5MHz, Loop BW = 250Hz, IBIASx = 1.

Note 19: I_{CP} = 11.2mA, f_{PFD} = 10MHz, Loop BW = 4kHz, IBIASx = 1.

Note 20: VCO is a Crystek CVCO55CC-1220-1340 voltage controlled oscillator. Reference frequency is supplied by a Crystek CCHD-957-25-49.152, f_{REF} = 49.152MHz. I_{CP} = 11.2mA, f_{PFD} = 49.152MHz, Loop BW = 26kHz, IBIASx = 1.

Note 21: Reference frequency is supplied by a Wenzel 501-04605D, f_{REF} = 5MHz.

Note 22: The outputs are differentially terminated with a 100Ω resistor across PECLx$^+$ and PECLx$^–$ at the far-end. The internal DC bias is enabled by programming IBIASx = 1.

Note 23: PECLx$^+$ and PECLx$^–$ are each AC-coupled to a 50Ω termination resistor at the far end. DC bias for PECLx$^+$ and PECLx$^–$ is provided by a 150Ω resistor to ground on each output. Internal bias is disabled by programming IBIASx = 0.

Note 24: Default LTC6950 configuration, with the following changes: PDPLL = 1, PDREFAC = 1, PDVCOAC = 1, PD_DIV1 = 1, PD_DIV2 = 1, PD_OUT1 = 1, PD_OUT2 = 1, IBIAS0 = 1, IBIAS3 = 1

Note 25: PD_DIV4 = 1, PD_OUT4 = 1

Note 26: RDIVOUT = 0, LVCMS = 1

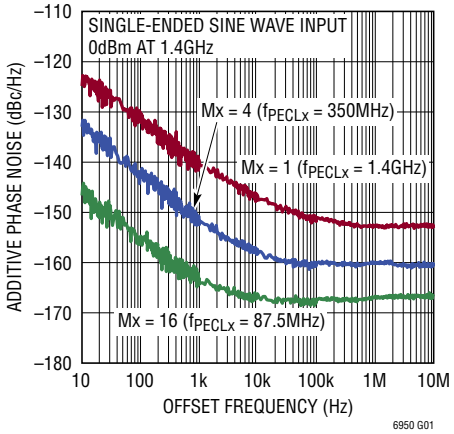
Note 27: RDIVOUT = 0, CMSINV = 1

Note 28: Do not apply a voltage or current source to these output pins. They must only be connected to input buffers and any associated level-shift or termination circuitry as described in the Applications Information section.

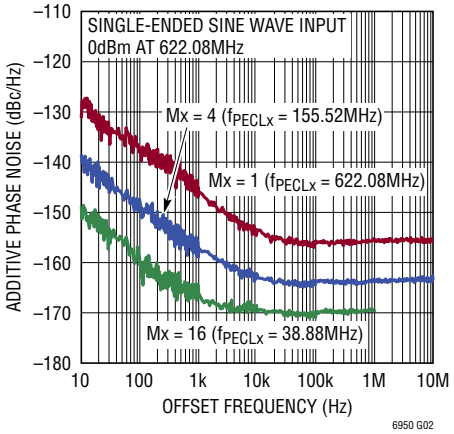
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

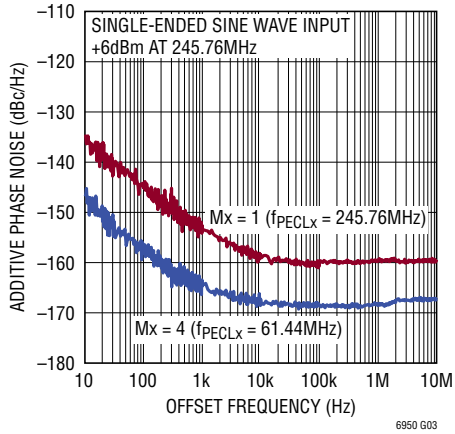
PECLx Additive Phase Noise with 1.4GHz Input (IBIASx = 1)



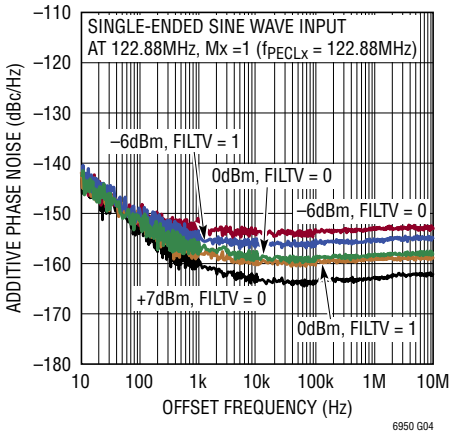
PECLx Additive Phase Noise with 622.08MHz Input (IBIASx = 1)



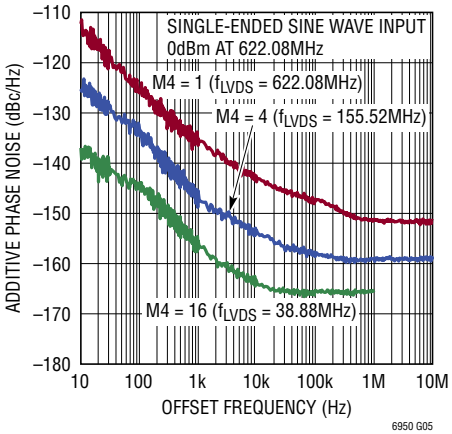
PECLx Additive Phase Noise with 245.76MHz Input (IBIASx = 1)



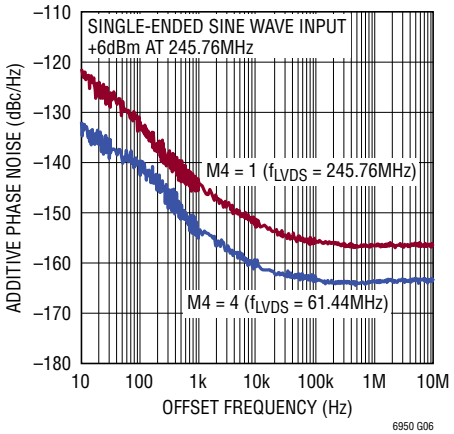
PECLx Additive Phase Noise vs Amplitude (IBIASx = 1)



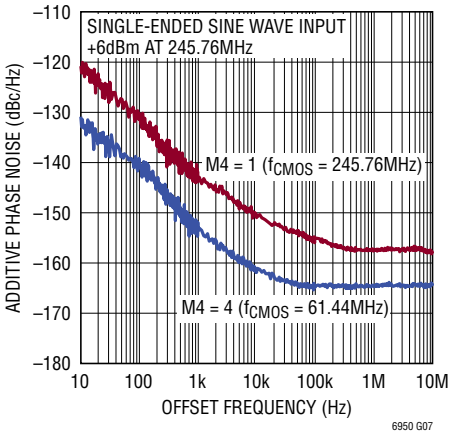
LVDS Additive Phase Noise with 622.08MHz Input



LVDS Additive Phase Noise with 245.76MHz Input



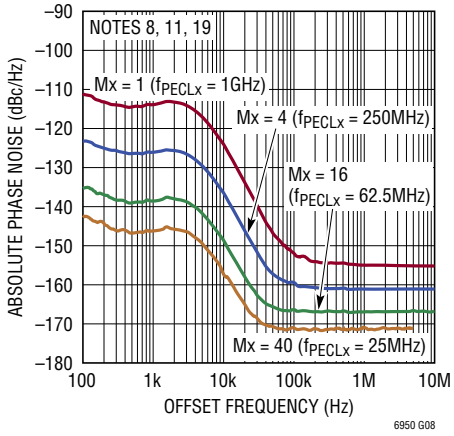
CMOS Additive Phase Noise with 245.76MHz Input (CMSINV = 1)



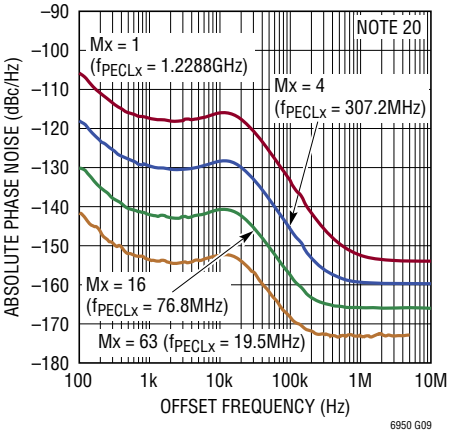
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

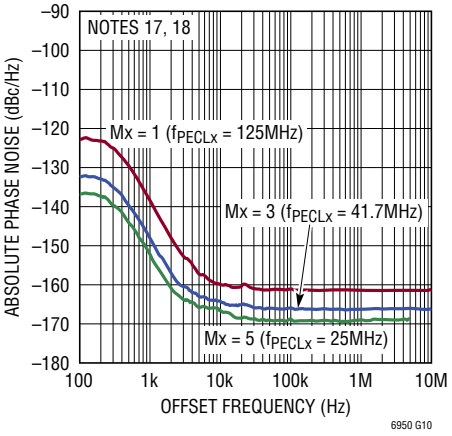
PECLx Closed-Loop Phase Noise VCSO Input at 1GHz



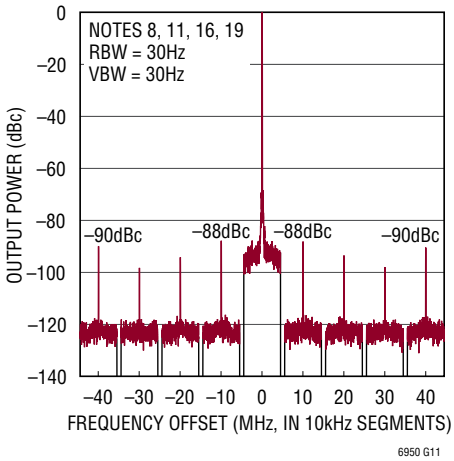
PECLx Closed-Loop Phase Noise VCO Input at 1.2288GHz



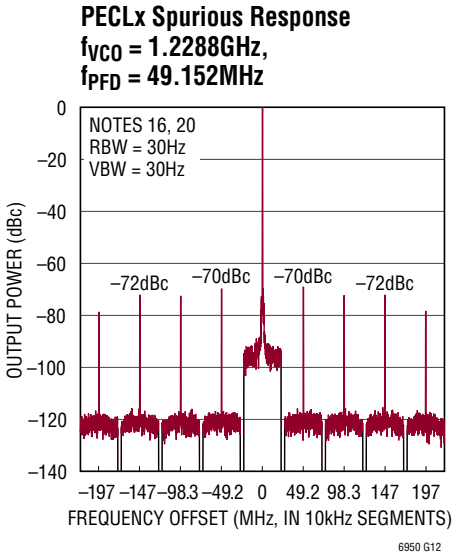
PECLx Closed-Loop Phase Noise VCXO Input at 125MHz



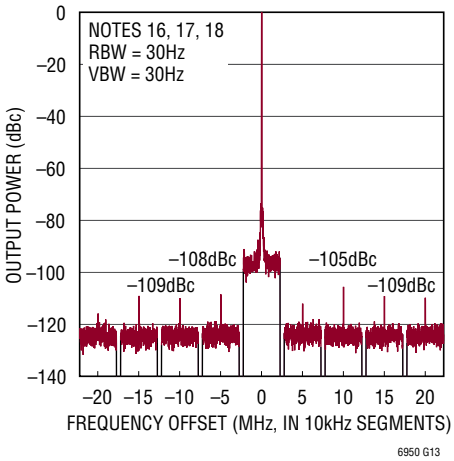
PECLx Spurious Response f_{VCSO} = 1GHz, f_{PFD} = 10MHz



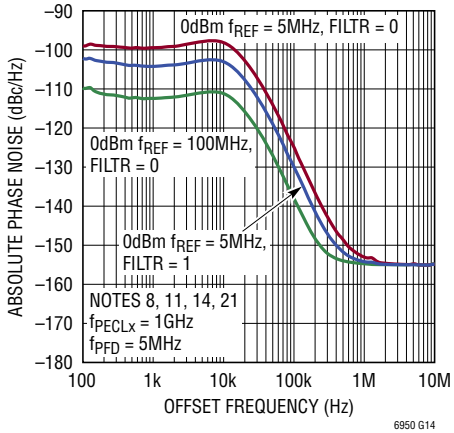
PECLx Spurious Response f_{VCO} = 1.2288GHz, f_{PFD} = 49.152MHz



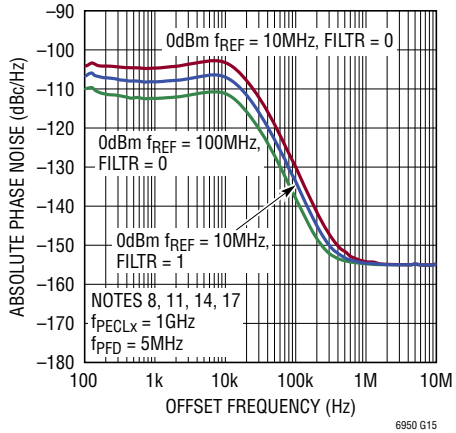
PECLx Spurious Response f_{VCXO} = 125MHz, f_{PFD} = 5MHz



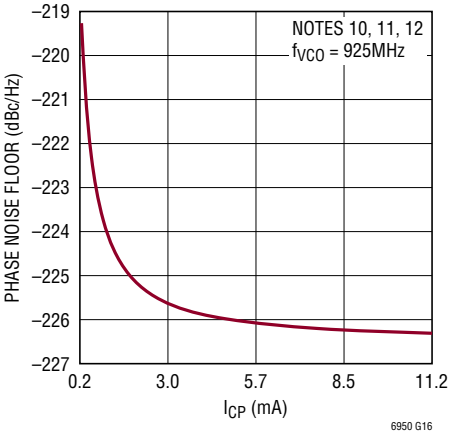
PECLx Closed-Loop Phase Noise 5MHz vs 100MHz Sine Wave Reference Input



PECLx Closed-Loop Phase Noise 10MHz vs 100MHz Sine Wave Reference Input



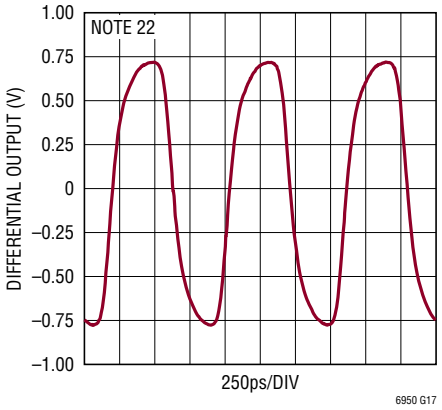
Normalized In-Band Phase Noise Floor vs Charge Pump Current



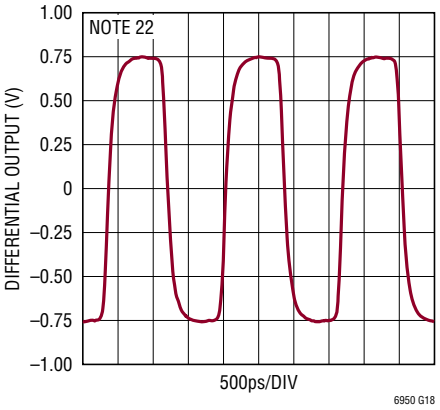
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

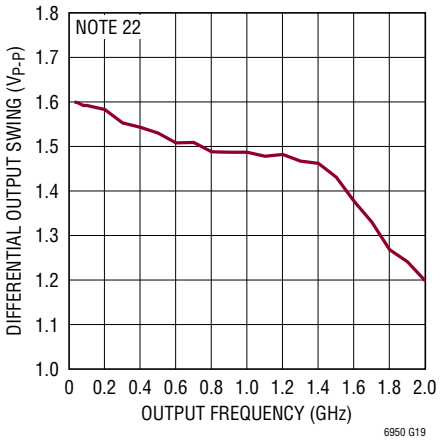
PECLx Differential Output at 1.2GHz (IBIASx = 1)



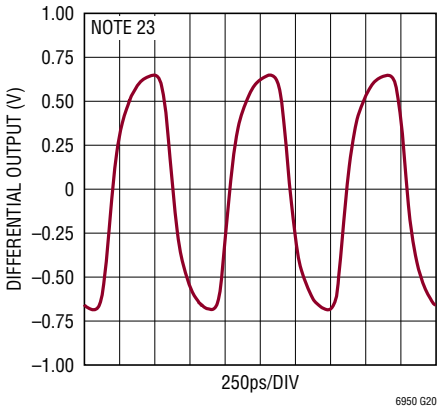
PECLx Differential Output at 600MHz (IBIASx = 1)



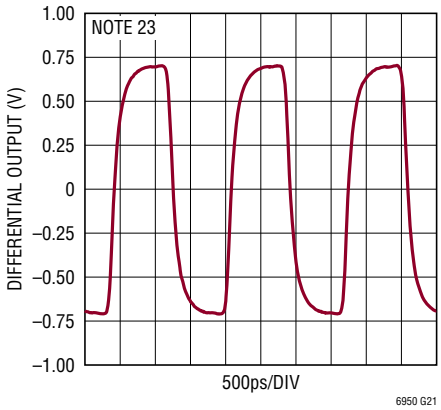
PECLx Differential Output Swing vs Frequency (IBIASx = 1)



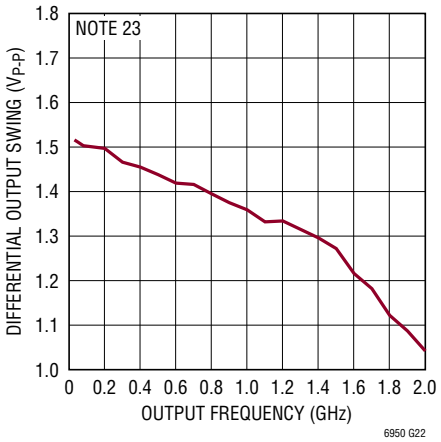
PECLx Differential Output at 1.2GHz (IBIASx = 0)



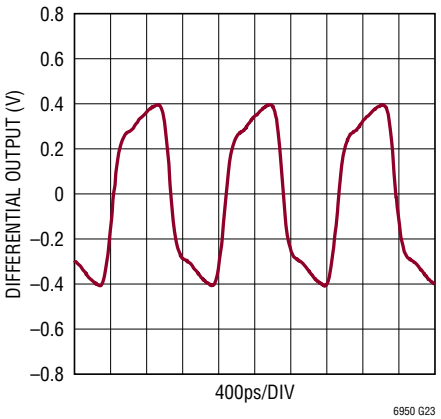
PECLx Differential Output at 600MHz (IBIASx = 0)



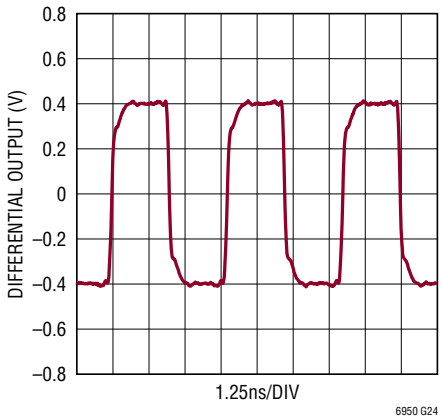
PECLx Differential Output Swing vs Frequency (IBIASx = 0)



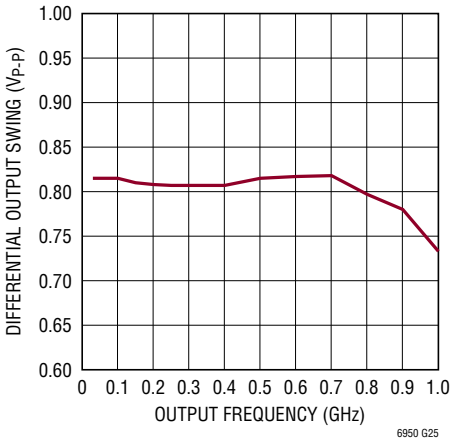
LVDS Output at 800MHz



LVDS Output at 250MHz



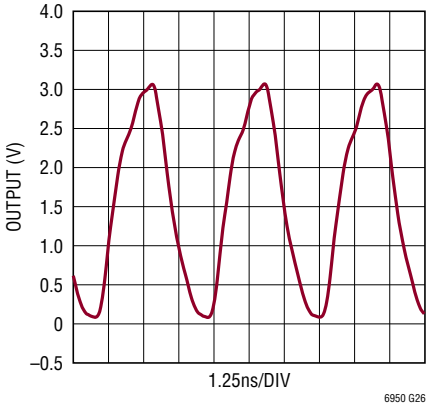
LVDS Output Swing vs Frequency



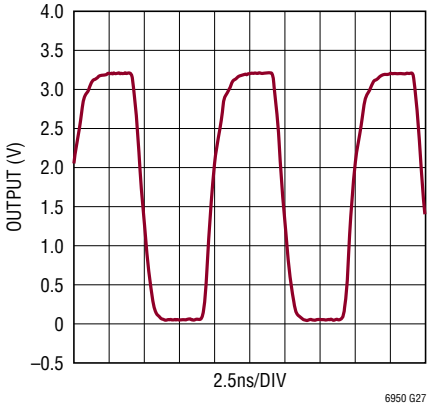
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

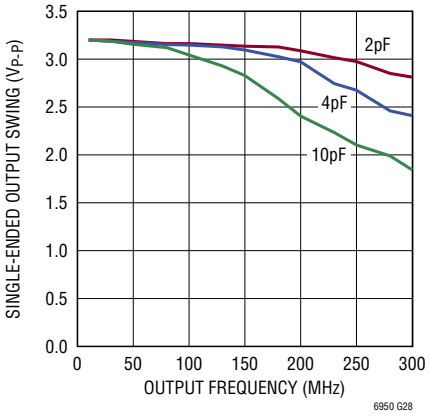
CMOS Single-Ended Output at 250MHz (2pF Load, CMSINV = 1)



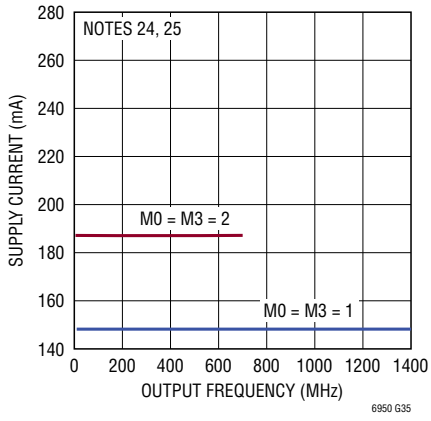
CMOS Single-Ended Output at 100MHz (2pF Load, CMSINV = 1)



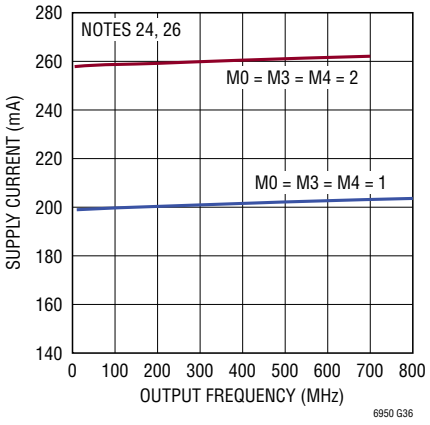
CMOS Single-Ended Output Swing vs Frequency (CMSINV = 1)



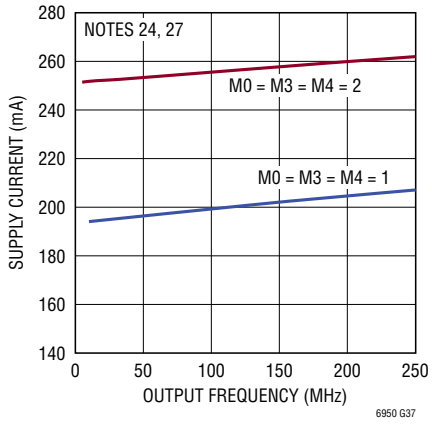
Supply Current vs Frequency PECL0 and PECL3 On



Supply Current vs Frequency PECL0, PECL3 and LVDS On



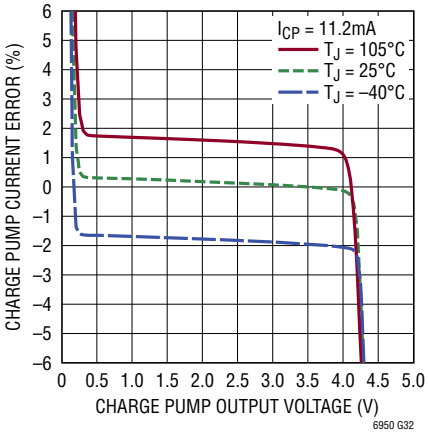
Supply Current vs Frequency PECL0, PECL3 and CMOS On



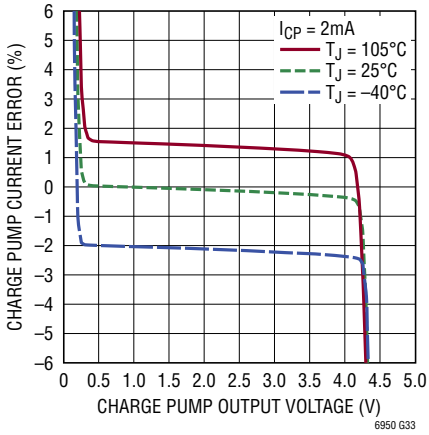
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

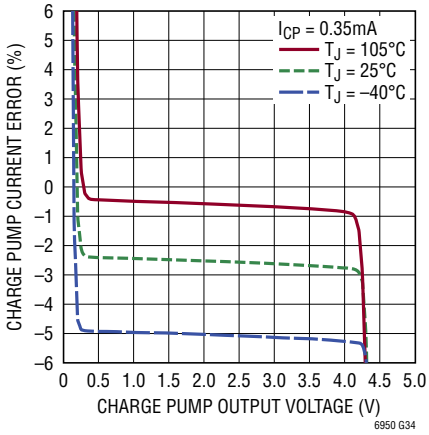
Charge Pump Source Current Error vs Voltage, Temperature (I_{CP} = 11.2mA)



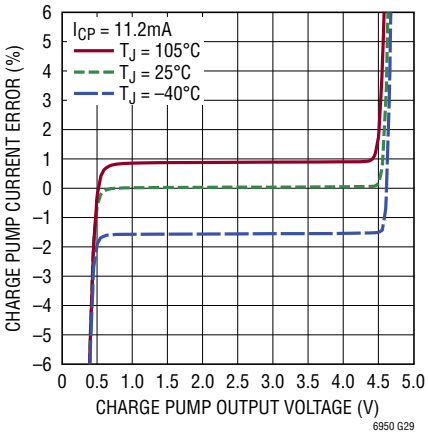
Charge Pump Source Current Error vs Voltage, Temperature (I_{CP} = 2mA)



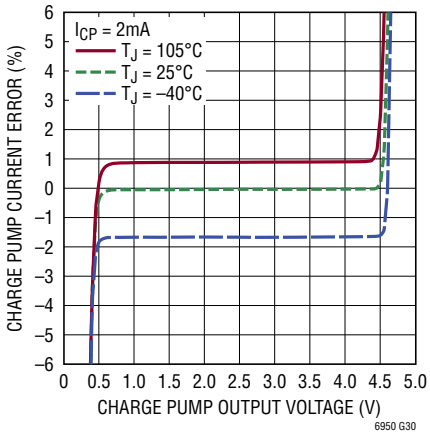
Charge Pump Source Current Error vs Voltage, Temperature (I_{CP} = 0.35mA)



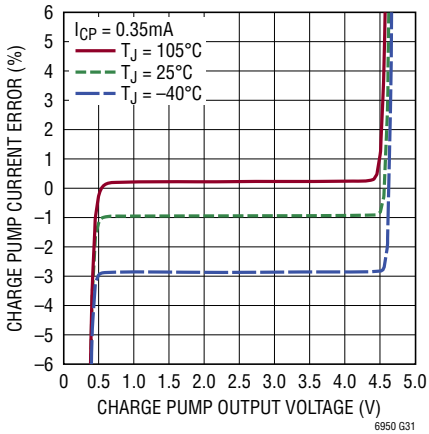
Charge Pump Sink Current Error vs Voltage, Temperature (I_{CP} = 11.2mA)



Charge Pump Sink Current Error vs Voltage, Temperature (I_{CP} = 2mA)



Charge Pump Sink Current Error vs Voltage, Temperature (I_{CP} = 0.35mA)



PIN FUNCTIONS

V_{P3}^+, V_{P2}^+, V_{P1}^+, V_{P0}^+ (Pins 1, 4, 5, 8, 9, 12, 13, 16): PECLx Output Supply Voltages. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. All V_{PX}^+ pins must be connected to the same supply voltage as the V^+ pins. Each pin, or in some cases pin pairs, must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

PECL3⁻, PECL3⁺ (Pins 2, 3): LVPECL Logic Compatible Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{P3}^+ supply. Refer to the Operation and the Applications Information sections for more details.

PECL2⁻, PECL2⁺ (Pins 6, 7): LVPECL Logic Compatible Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{P2}^+ supply. Refer to the Operation and the Applications Information sections for more details.

PECL1⁻, PECL1⁺ (Pins 10, 11): LVPECL Logic Compatible Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{P1}^+ supply. Refer to the Operation and the Applications Information sections for more details.

PECL0⁻, PECL0⁺ (Pins 14, 15): LVPECL Logic Compatible Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{P0}^+ supply. Refer to the Operation and the Applications Information sections for more details.

GND (Pins 17, 31, 38, 41, 48): Ground Connections. Should be tied directly to the die attach paddle (DAP) and to a low impedance ground plane for best performance. Refer to the Applications Information section for more details on grounding for signal integrity and thermal considerations.

V^+ (Pins 18, 19, 20, 25, 32, 37, 42, 47): Positive Supply Voltage. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. All V^+ pins must be connected to the same supply voltage. Each pin, or in some cases pin pairs, must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

LV/CM⁻, LV/CM⁺ (Pins 21, 22): LVDS/CMOS Logic Output Pins. These outputs may be programmed as either LVDS or CMOS logic outputs using the serial port. Refer to the Operation and the Applications Information sections for more details.

$\overline{CS}$ (Pin 23): Serial Port Chip Select Input. This active low CMOS logic input initiates a serial port transaction when brought to a logic low. It finalizes the serial port transaction when brought to a logic high after 16 serial port clock cycles. Refer to the Operation section for more details.

SDO (Pin 24): Serial Port Data Output. Data read from the serial port is presented on this CMOS three-state logic pin. Optionally attach a resistor of >200k to GND to prevent a floating output. Refer to the Operation section for more details.

SCLK (Pin 26): Serial Port Clock Input. This positive edge triggered CMOS logic input signal clocks serial port data in on rising edges. Refer to the Operation section for more details.

SDI (Pin 27): Serial Port Data Input. Data written into the serial port is presented on this CMOS logic pin. Refer to the Operation section for more details.

STAT2, STAT1 (Pins 28, 29): Status Output Pins. These CMOS outputs are configured through the serial port to provide direct status of critical signals that are monitored on-chip. Examples include the lock indicator and REF signal present. Refer to the Operation section for more details.

PIN FUNCTIONS

SYNC (Pin 30): Synchronization Input Pin. A rising edge on this CMOS logic input initiates an output clock synchronization sequence. Precision output synchronization of one or more parts is handled on chip, so the timing of this signal is not critical. Refer to the Operation and the Applications Information sections for more details.

V_{VCO}^+ (Pins 33, 36): VCO Input Supply Voltage. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. Both V_{VCO}^+ pins must be connected to the same supply voltage as the V^+ pins. Each pin must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

VCO^+, VCO^- (Pins 34, 35): VCO Input Pins. The VCO signal can be either differential or single-ended. It can be a sine wave, LVPECL logic or LVDS logic. Refer to the Operation and the Applications Information sections for more details on the correct use of the VCO inputs.

V_{CP}^+ (Pin 39): Charge Pump Supply Voltage. This supply should be kept free of noise and ripple. This pin can go above the V^+ supply up to 5.25V maximum supply. It must be bypassed directly to GND with a 0.1µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on the charge pump supply bypassing.

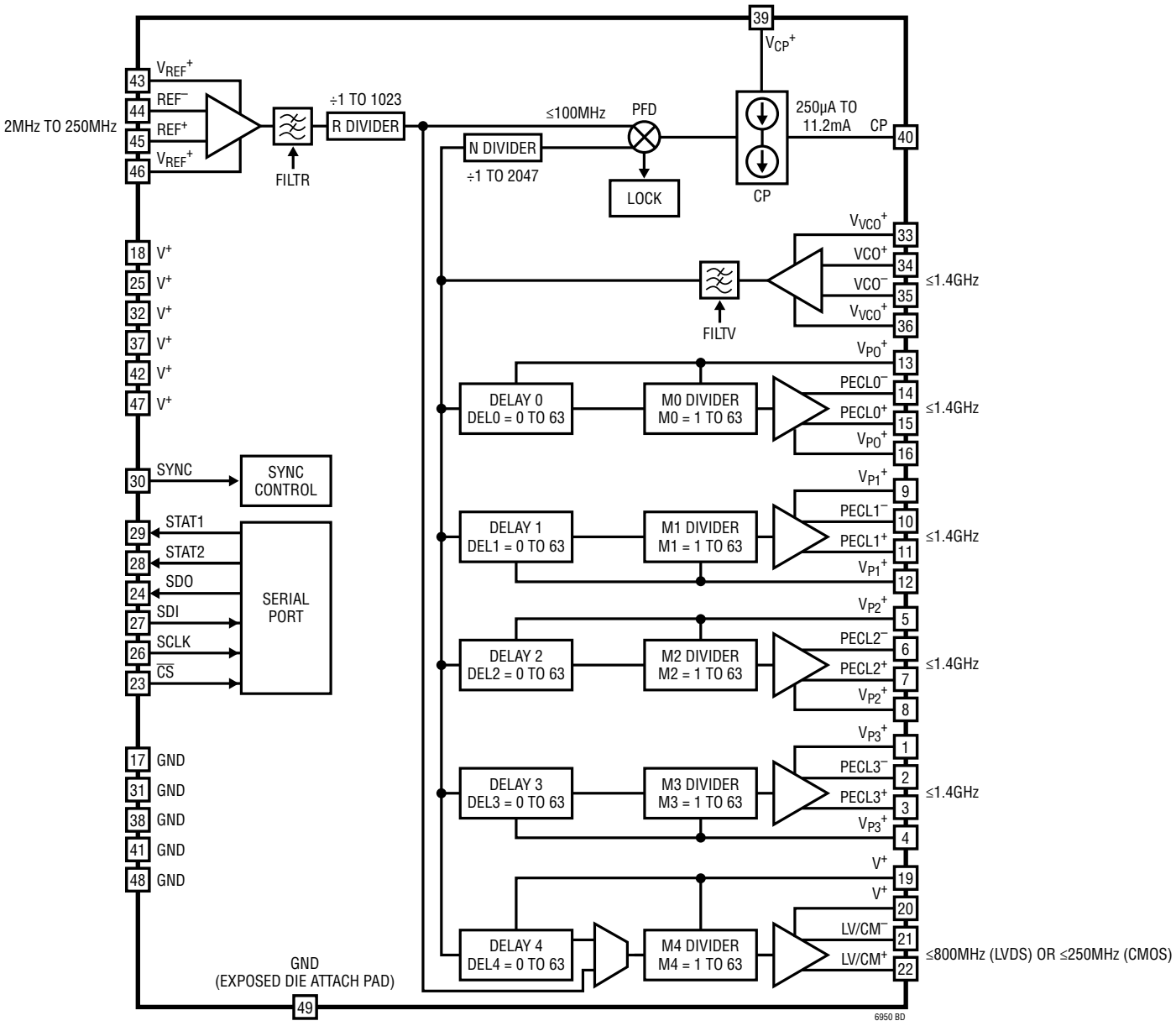
CP (Pin 40): Charge Pump Output Pin. This pin typically connects directly to the VCO tune input to close the PLL loop. Shunt capacitive and resistive elements are necessary to set the loop bandwidth and compensation. Refer to the Operation and the Applications Information sections for more details.

V_{REF}^+ (Pins 43, 46): REF Input Supply Voltage. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. Both V_{REF}^+ pins must be connected to the same supply voltage as the V^+ pins. Each pin must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

REF^-, REF^+ (Pins 44, 45): Reference Input Pins. The reference input signal can be either differential or single-ended. It can be a sine wave, LVPECL logic, LVDS logic or CMOS logic. Refer to the Operation and the Applications Information sections for more details on the correct use of the reference inputs.

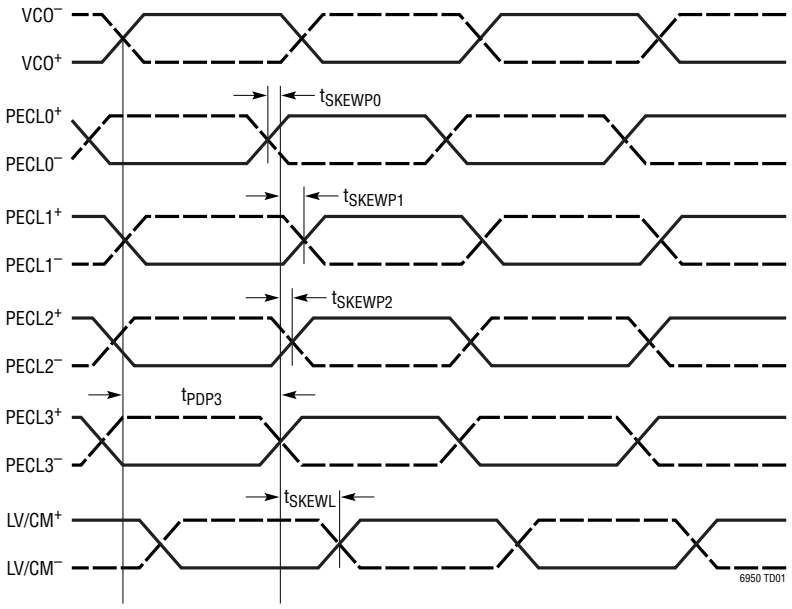
GND (Exposed Pad Pin 49): Ground Connection. The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance. Refer to the Applications Information section for more details on grounding for signal integrity and thermal considerations.

BLOCK DIAGRAM

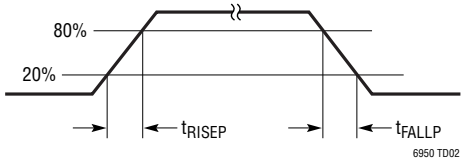


TIMING DIAGRAMS

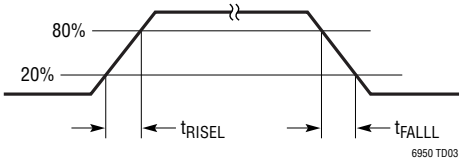
Output Propagation Delays and Skews, Mx[5:0] = 1



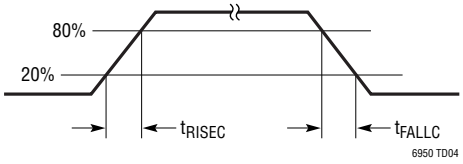
Single-Ended PECLx Rise/Fall Times



Differential LVDS Rise/Fall Times



Single-Ended CMOS Rise/Fall Times



OPERATION

LTC6950 INTRODUCTION

The LTC6950 is a low phase noise integer-N frequency synthesizer core with clock distribution. The LTC6950 delivers the low phase noise and low jitter clock signals demanded in high frequency, high resolution data acquisition systems. As shown in Figure 1, the LTC6950 consists of three distinct circuit sections: phase-locked loop (PLL) core, clock distribution and digital control.

The PLL section of the LTC6950 contains a low noise integer-N PLL core with a programmable reference divider (R), a programmable feedback divider (N), a phase/frequency detector (PFD) and a low noise charge pump (CP). The charge pump's low noise and well balanced design delivers the LTC6950's –226dBc/Hz normalized PLL in-band phase noise floor. To form a complete frequency synthesizer, both an external reference oscillator and a voltage controlled oscillator (VCO) are required.

OPERATION

The clock distribution section of the LTC6950 receives a VCO input signal with a maximum frequency of 1.4GHz and delivers five output signals based on the VCO input. Each output is individually programmed to divide the VCO input frequency by any integer from 1 to 63 and to delay the output by 0 to 63 VCO clock cycles. For a VCO input with a 50% duty cycle, the output duty cycle will always be 50% regardless of the divide number. Four outputs feature very low noise, low skew LVPECL logic signals capable of operation up to 1.4GHz. The fifth output is selectable as either an LVDS (800MHz) or a CMOS (250MHz) logic type. This fifth output is also programmed to produce an output signal based on either the VCO input or the reference divider output.

The digital control section contains a full SPI-compatible serial control bus along with two device status bits and the clock synchronization (SYNC) function. All device settings and operating modes are controlled through the SPI bus. The status output pins (STAT1 and STAT2) indicate the status of the part's input signals, the PLL lock state, the charge pump clamp condition or a logical combination of any of these signals. This is useful as an alert flag or to drive an LED for a visible PLL lock indicator.

To minimize power consumption, most sections of the LTC6950 can be powered down when not in use. As shown in Figure 2, the LTC6950 can be used as a full PLL synthesizer with clock distribution. Any unused outputs from the clock distribution section may be powered down. Alternatively, Figure 3 shows that the LTC6950 can also be used in a clock distribution application with the PLL section powered down.

Figure 4 highlights two LTC6950 parts cascaded as CONTROLLER and FOLLOWER devices. This example shows a single FOLLOWER device, but each output from the CONTROLLER device can control separate FOLLOWER devices for support of up to five FOLLOWER devices. The LTC6950's EZSync multichip synchronization feature assures consistent edge alignment of all outputs from all devices. See the EZSync Clock Output Synchronization section for more details on EZSync operation.

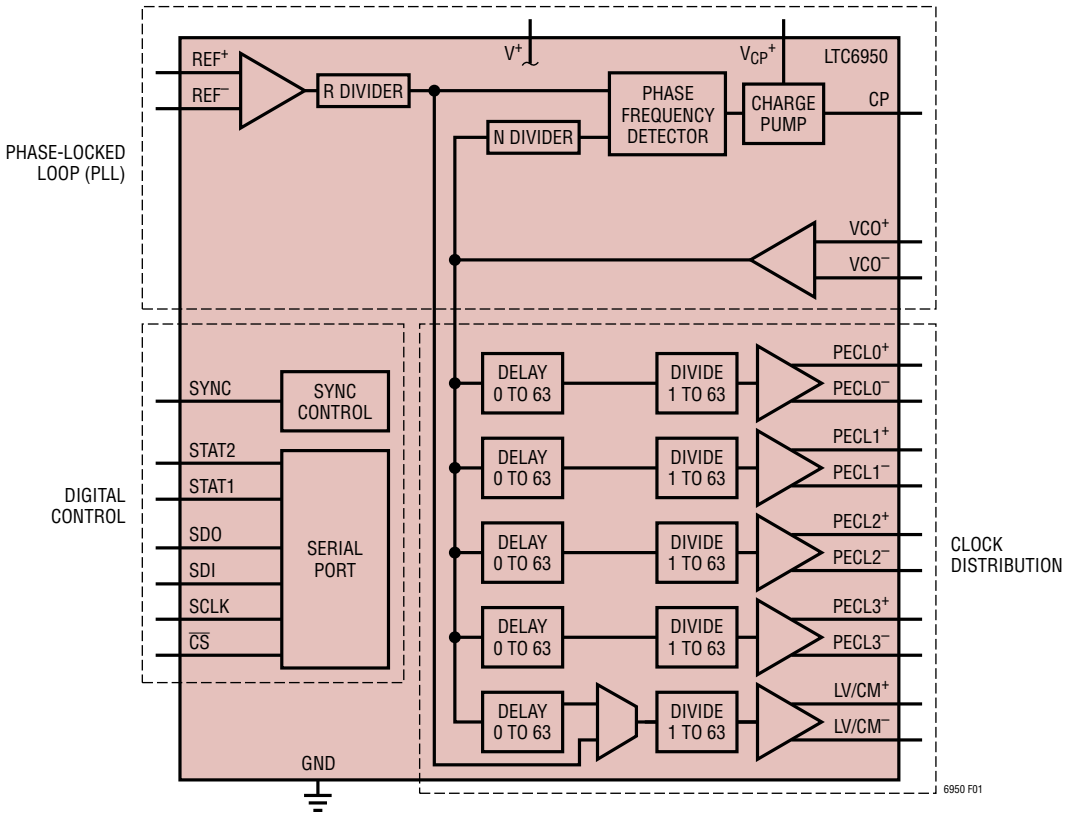


Figure 1. The LTC6950 Highlighting the Three Main Circuit Blocks

OPERATION

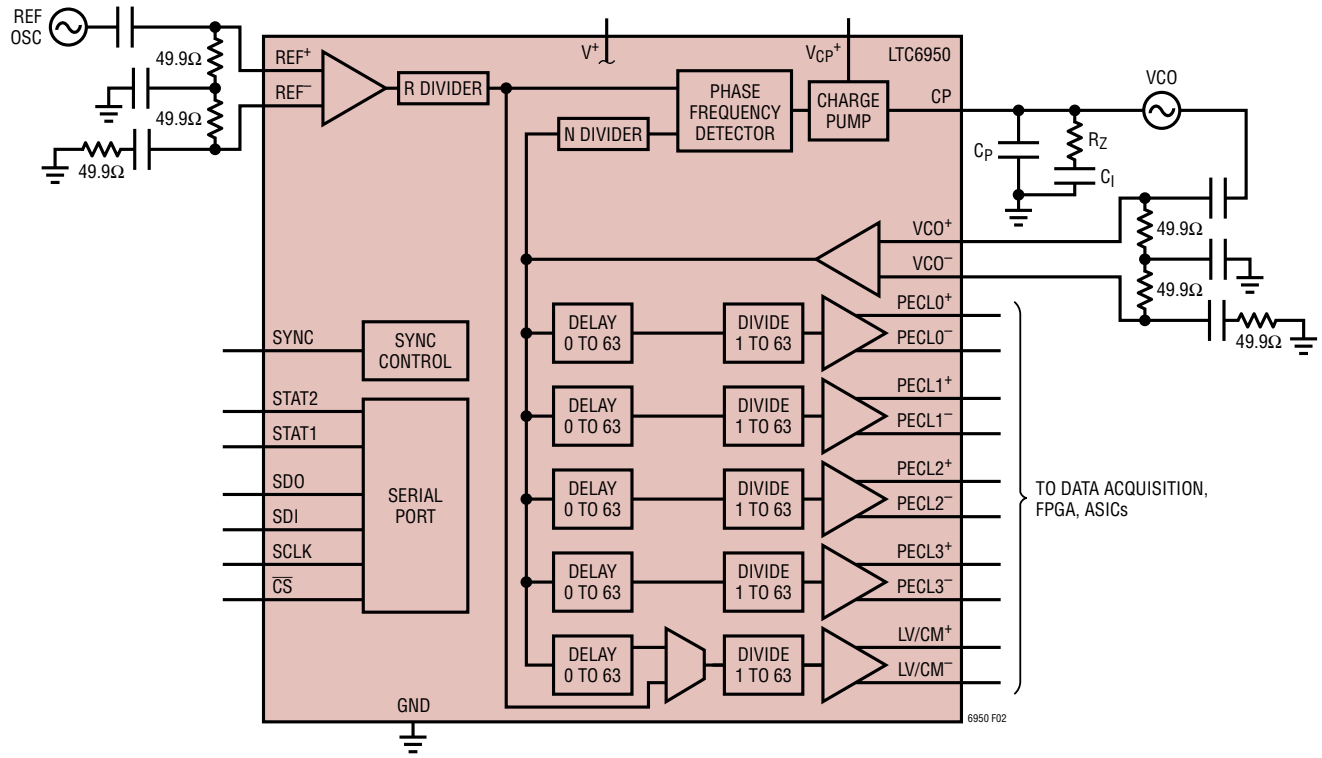


Figure 2. The LTC6950 Connected in PLL plus Clock Distribution Mode (Single-Ended, 50Ω Output Reference Oscillator and VCO Shown as an Example)

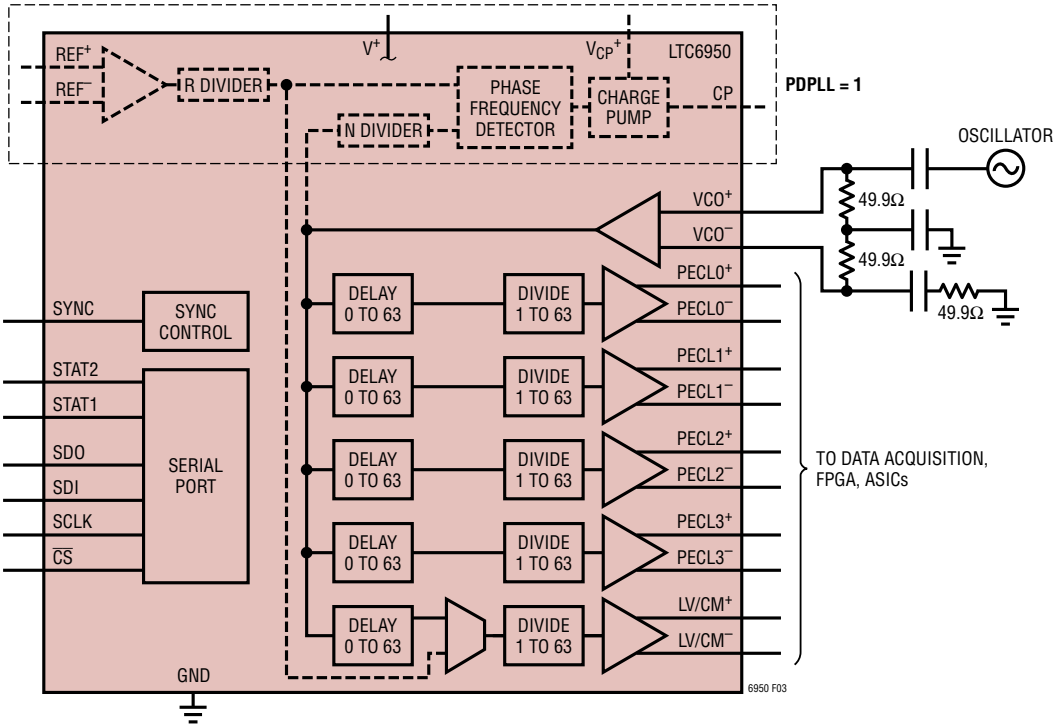


Figure 3. The LTC6950 Connected in Clock Distribution Only Mode with the PLL Section Powered Down (Single-Ended, 50Ω Output Oscillator Shown as an Example)

OPERATION

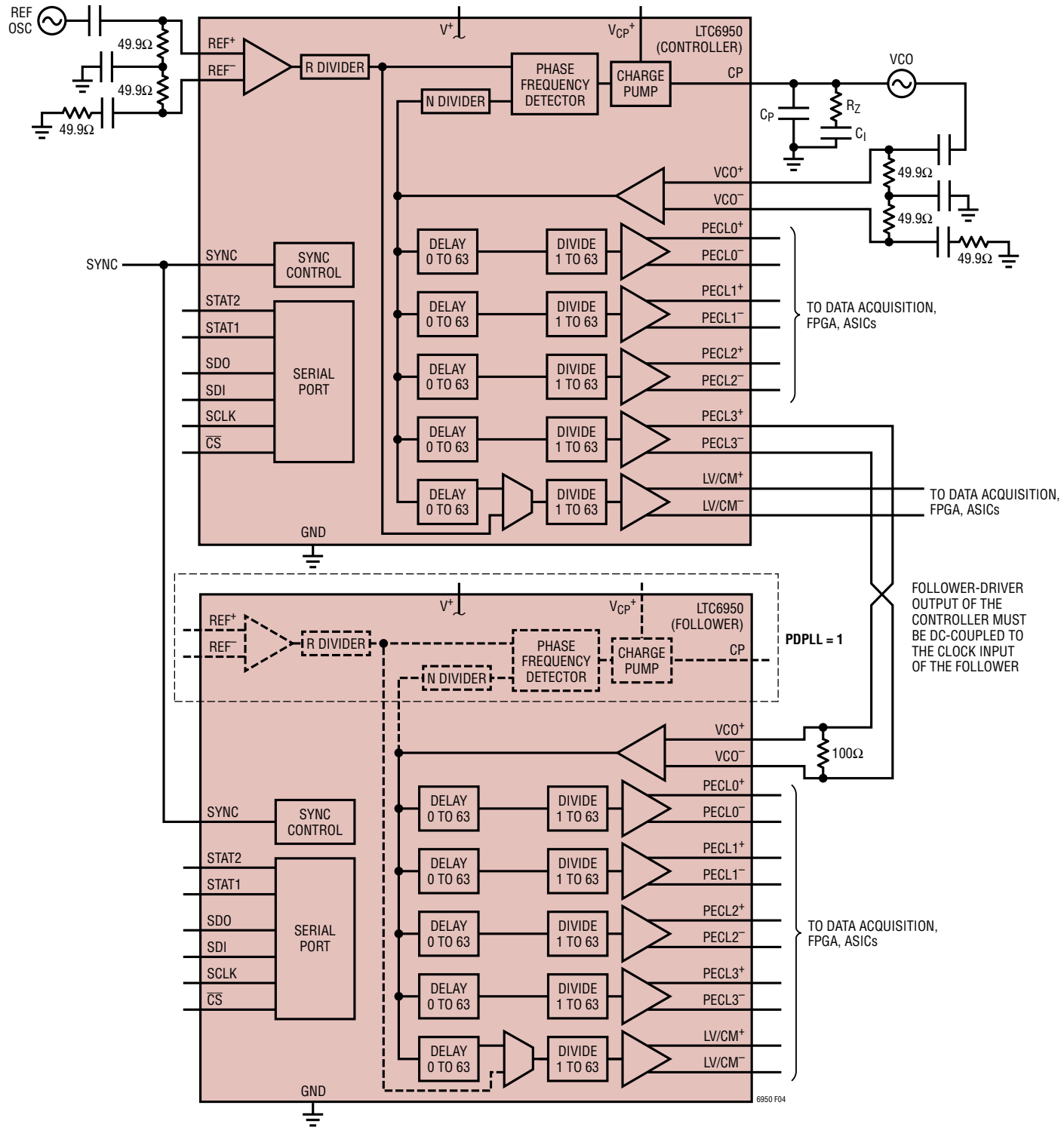


Figure 4. The LTC6950 in PLL plus Clock Distribution Mode (CONTROLLER) Clocking Another LTC6950 in Clock Distribution Only Mode (FOLLOWER). For Best Performance Use One of the PECLx Outputs from the CONTROLLER LTC6950 (with its IBIASx Enabled) to Clock the FOLLOWER LTC6950 with its PLL Section Powered Down. (Single-Ended, 50Ω Output Reference Oscillator and VCO Shown as an Example)

OPERATION

PHASE-LOCKED LOOP

The LTC6950 contains a high performance phase-locked loop (PLL), including low noise reference and VCO input buffers and dividers, phase/frequency detector (PFD), charge pump and lock indicator. The following section describes the function of these different blocks.

REFERENCE INPUT BUFFER

The LTC6950's reference input buffer provides a flexible interface to either differential or single-ended frequency sources. The frequency range for the reference input is from 2MHz to 250MHz. A differential LVPECL reference source may be applied directly to the REF± pins with a 100Ω differential far-end termination. A single-ended reference frequency source may also be used, as long as its peak-to-peak output swing is less than 1.5V to avoid turning on the input protection diodes (see Figure 5).

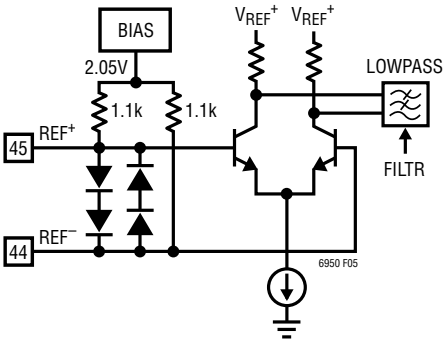


Figure 5. Simplified Reference Input Schematic

Because the signal applied to the REF± inputs provides the frequency reference for the PLL, it is important that this frequency source have low phase noise and a slew rate of at least 100V/µs. For applications where using a reference source with an output slew rate at least 100V/µs is not possible, better phase noise performance will be achieved by enabling the internal broadband noise filtering circuit within the reference input buffer. This is accomplished by asserting the configuration bit FILTR in serial port register h0B. Note that setting FILTR = 1 when the slew rate of the reference frequency source is greater than 100V/µs will degrade the overall PLL phase noise performance. See the Applications Information section for more information on REF input signal requirements and interfacing.

REFERENCE INPUT SIGNAL PRESENT

A reference input signal present circuit is also connected to the REF± pins of the LTC6950. The signal present circuit detects when either a single-ended or differential AC-frequency is applied to the REF± pins, and asserts the status flag NO_REF, found in register h00, when no signal is found. For a reference frequency between 2MHz and 250MHz, NO_REF will go high when the differential input applied at REF± is less than $100mV_{P-P}$. For an applied differential signal greater than $350mV_{P-P}$, the NO_REF flag will remain low.

REFERENCE (R) DIVIDER

A 10-bit reference divider (R) is used to reduce the frequency seen at the PFD. Its divide ratio may be set to any integer from 1 to 1023, inclusive, by directly programming the R[9:0] bits found in registers h07 and h08. The programmed value of R[9:0] will automatically be read when the R divider reaches its terminal count, but this could theoretically take 1023 cycles of the reference input.

For applications where this delay is too long, it may be useful to force a load of the programmed divide ratio by asserting the configuration bit RESET_R in serial port register h07. Because the R divider does not transition while RESET_R = 1, it must then be programmed back to 0 before the R divider will resume dividing. See the Applications Information section for the relationship between R and the f_{REF}, f_{PFD} and f_{VCO} frequencies.

VCO INPUT BUFFER

The LTC6950's VCO input buffer provides a flexible interface to either differential or single-ended frequency sources. The maximum VCO input frequency is 1.4GHz. A differential VCO/VCXO/VCSO may be applied directly to the VCO± pins with a 100Ω differential far-end termination. Alternatively, a single-ended input may also be used, as long as its signal swing is less than $1.5V_{P-P}$ to avoid turning on the input protection diodes (see Figure 6).

It is also important that the VCO± inputs be low noise and have a slew rate of at least 100V/µs, although better performance will be achieved with a higher slew rate. For applications where using a VCO/VCXO/VCSO with an