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Ultralow Jitter Multioutput Clock Synthesizer with Integrated VCO

FEATURES

- **Low Noise Integer-N PLL with Integrated VCO**
- **Output Jitter:**
  - **90fs RMS (12kHz to 20MHz)**
  - **115fs RMS (ADC SNR Method)**
  - **Noise Floor = –165dBc/Hz at 250MHz**
- **EZSync™, ParallelSync™ Multichip Synchronization**
- **SYSREF Generation for JESD204B, Subclass 1**
- **Output Frequency Range:**
  - **1.95MHz to 2.5GHz (LTC6951)**
  - **2.1MHz to 2.7GHz (LTC6951-1)**
- –229dBc/Hz Normalized In-Band Phase Noise Floor
- –277dBc/Hz Normalized In-Band 1/f Noise
- Five Independent, Low Noise Outputs
- Reference Input Frequency up to 425MHz
- LTC6951Wizard™ Software Design Tool Support
- –40°C to 105°C Operating Junction Temperature Range

APPLICATIONS

- High Performance Data Converter Clocking
- Wireless Infrastructure
- Test and Measurement

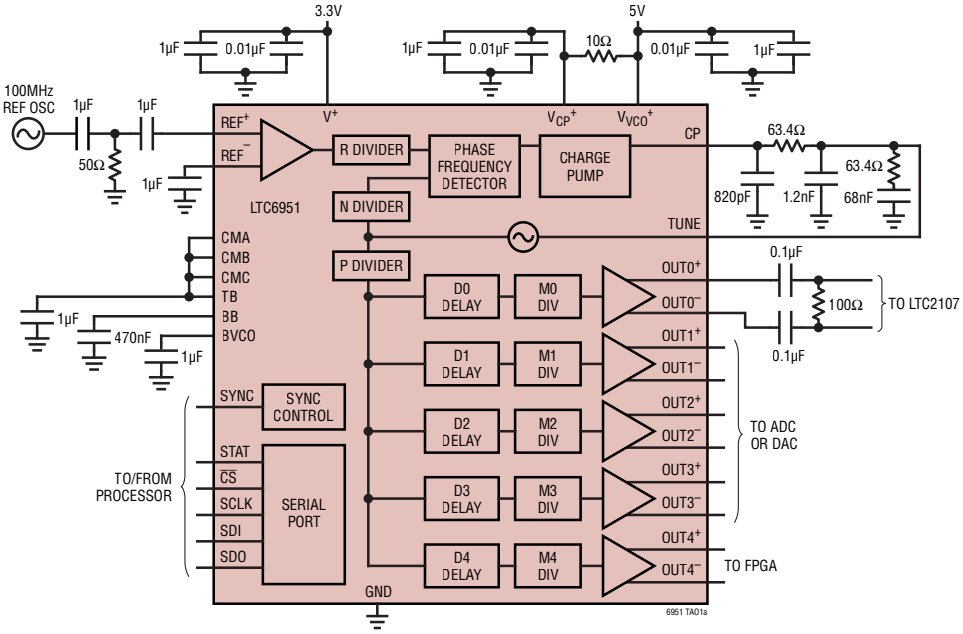
DESCRIPTION

The LTC®6951 is a high performance, low noise, Phase Locked Loop (PLL) with a fully integrated VCO. The low noise VCO uses no external components and is internally calibrated to the correct output frequency with no external system support.

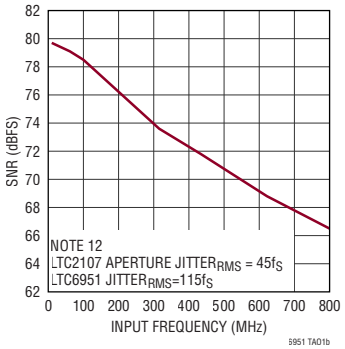
The clock generation section provides five outputs based on the VCO prescaler signal with individual dividers for each output. Four outputs feature very low noise, low skew CML logic. The fifth output is low noise LVDS. All outputs can be synchronized and set to precise phase alignment using the programmable delays.

Choose the LTC6951-1 if any desired output frequency falls in the ranges 2.5GHz to 2.7GHz, 1.66GHz to 1.8GHz, or 1.25GHz to 1.35GHz. Choose the LTC6951 for all other frequencies.

TYPICAL APPLICATION



SNR vs Input Frequency of LTC6951 Clocking an LTC2107, f_S = 210Msps, A_{IN} = –3dBFS



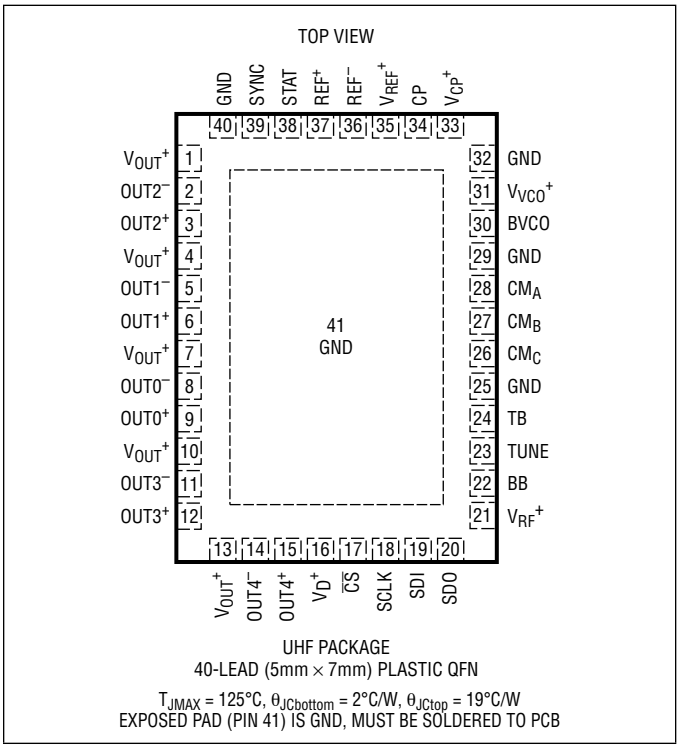
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

V^+ (V_{REF}^+, V_{RF}^+, V_D^+, V_{OUT}^+) to GND 3.6V
V_{CP}^+, V_{VCO}^+ to GND 5.5V
Voltage on CP Pin ..... GND – 0.3V to V_{CP}^+ + 0.3V
Voltage on all other Pins ..... GND – 0.3V to V^+ + 0.3V
Current into $OUTx^+$, $OUTx^-$, (x = 0, 1, 2, 3, 4) ..... ±25mA
Operating Junction Temperature Range, T_J (Note 2)
LTC6951I and LTC6951I-1 ..... –40 to 105°C
Junction Temperature, T_{JMAX} ..... 125°C
Storage Temperature Range ..... –65 to 150°C

PIN CONFIGURATION



UHF PACKAGE
40-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 19°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC6951#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6951IUHF#PBF	LTC6951IUHF#TRPBF	6951	40-Lead (5mm × 7mm) Plastic QFN	–40°C to 105°C
LTC6951IUHF-1#PBF	LTC6951IUHF-1#TRPBF	69511	40-Lead (5mm × 7mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{OUT}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Inputs (REF⁺, REF⁻)							
f_{REF}	Input Frequency		●	1		425	MHz
V_{REF}	Input Signal Level	Single-Ended	●	0.5	2	2.7	V_{P-P}
	Minimum Input Slew Rate				20		V/µs
	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.65	1.85	2.25	V
	Input Signal Detected	REFOK = 1, PDREFPK = 0 10MHz ≤ f_{REF} ≤ 425MHz, Sine Wave	●	350			mV_{P-P}
	Input Signal Not Detected	REFOK = 0, PDREFPK = 0 10MHz ≤ f_{REF} ≤ 425MHz, Sine Wave	●			100	mV_{P-P}
	Input Resistance	Differential	●	2.6	4.2	6.1	kΩ
	Input Capacitance	Differential			7		pF
VCO							
f_{VCO}	Frequency Range	LTC6951 (Note 3) LTC6951-1 (Note 3)	● ●	4.0 4.3		5.0 5.4	GHz GHz
K_{VCO}	Tuning Sensitivity	(Notes 3, 4)			2.5 to 3.7		%Hz/V
Phase/Frequency Detector (PFD)							
f_{PFD}	Input Frequency		●			100	MHz
Charge Pump (CP)							
I_{CP}	Output Current Range	8 Settings (see Table 8)		1.0		11.2	mA
	Output Current Source/Sink Accuracy	All Settings, V(CP) = 2.3V				±6	%
	Output Current Source/Sink Matching	I_{CP} = 1.0mA to 1.4mA, V(CP) = 2.3V				±3.5	%
		I_{CP} = 2.0mA to 11.2mA, V(CP) = 2.3V				±2	%
	Output Current vs Output Voltage Sensitivity	(Note 5)	●		0.1	0.5	%/V
	Output Current vs Temperature	V(CP) = 2.3V	●		140		ppm/°C
	Output Hi-Z Leakage Current	I_{CP} = 1mA (Note 5)			0.5		nA
		I_{CP} = 11.2mA (Note 5)			5		nA
V_{MID}	Mid-Supply Output Bias Ratio	Referred to (V_{CP}^+ – GND)			0.48		V/V
Reference Divider (R)							
R	Divide Range	All Integers Included	●	1		63	Counts
VCO Divider (N)							
N	Divide Range	All Integers Included, RAO = 0	●	32		1023	Counts
		All Integers Included, RAO = 1	●	2		511	Counts
VCO Prescaler Divider (P)							
P	Divide Range	2, 2.5, 3, 3.5, 4 (see Table 14)	●	2		4	Counts
Digital Pin Specifications							
V_{IH}	High Level Input Voltage	$\overline{CS}$, SDI, SCLK, SYNC	●	1.55			V
V_{IL}	Low Level Input Voltage	$\overline{CS}$, SDI, SCLK, SYNC	●			0.8	V
V_{IHYS}	Input Voltage Hysteresis	$\overline{CS}$, SDI, SCLK, SYNC			250		mV
	Input Current	$\overline{CS}$, SDI, SCLK, SYNC	●			±1	µA
I_{OH}	High Level Output Current	SDO and STAT, $V_{OH} = V_D^+ – 400mV$	●		–3.3	–1.9	mA
I_{OL}	Low Level Output Current	SDO and STAT, V_{OL} = 400mV	●	2.0	3.4		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{OUT}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	SDO Hi-Z Current		●			±1	µA
Digital Timing Specifications (See Figure 13 and Figure 14)							
t_{CKH}	SCLK High Time		●	25			ns
t_{CKL}	SCLK Low Time		●	25			ns
t_{CSS}	$\overline{CS}$ Setup Time		●	10			ns
t_{CSH}	$\overline{CS}$ High Time		●	10			ns
t_{CS}	SDI to SCLK Setup Time		●	6			ns
t_{CH}	SDI to SCLK Hold Time		●	6			ns
t_{DO}	SCLK to SDO Time	to V_{IH}/V_{IL}/Hi-Z with 30pF Load	●			16	ns
SYNC Timing Specifications (See Figure 31 and Figure 32)							
t_{SYNCH}	SYNC High Time		●	1			ms
t_{SYNCL}	SYNC Low Time		●	1			ms
	SYNC Skew	EZSync, Part to Part				10	µs
t_{SS}	SYNC to REF Setup Time	(See Note 6)	●	1			ns
t_{SH}	SYNC to REF Hold Time	(See Note 6)	●	1			ns
Output Dividers (M0, M1, M2, M3 and M4)							
Mx	Output Divider Range (x = 0 to 4)	16 Settings (See Table 15)	●	1		512	Counts
Dx	Output Divider Delay (x = 0 to 4)	P Cycles, All Integers Included	●	0		255	Cycles
CML Clock Outputs (OUT0⁺, OUT0⁻, OUT1⁺, OUT1⁻, OUT2⁺, OUT2⁻, OUT3⁺, OUT3⁻), Differential Termination = 100Ω Unless Otherwise Noted							
f_{OUT}	LTC6951 Output Frequency		●	1.95		2500	MHz
		f_{OUT}/2 Subharmonic Generated, P = 2.5, Mx = 1 (Note 16)	●	1667		2000	MHz
		f_{OUT}/2 Subharmonic Generated, P = 3.5, Mx = 1 (Note 16)	●	1250		1333	MHz
	LTC6951-1 Output Frequency		●	2.1		2700	MHz
		f_{OUT}/2 Subharmonic Generated, P = 2.5, Mx = 1 (Note 16)	●	1800		2150	MHz
		f_{OUT}/2 Subharmonic Generated, P = 3.5, Mx = 1 (Note 16)	●	1350		1433	MHz
	Output High Voltage				$V_{OUT}^+ - 0.9$		V
	Output Low Voltage				$V_{OUT}^+ - 1.3$		V
	Output Differential Voltage		●	350	440	520	mV_{PK}
	Output Resistance	Differential, No Termination			100		Ω
t_R	Output Rise Time, 20% to 80%				50		ps
t_F	Output Fall Time, 80% to 20%				50		ps
	Output Duty Cycle	P = 2, 3, 4 all Mx, P = 2.5, 3.5 Mx ≥ 2 P = 2.5, Mx = 1 P = 3.5, Mx = 1	●	45	50 40 57	55	% % %
LVDS Clock Outputs (OUT4⁺, OUT4⁻), Differential Termination = 100Ω							
$f_{OUTLVDS}$	LTC6951 Output Frequency LTC6951-1 Output Frequency		● ●	1.95 2.1		800 800	MHz MHz
V_{OD}	Differential Output Voltage		●	300	380	450	mV_{PK}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{OUT}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\lvert\Delta V_{OD}\rvert$	Delta V_{OD}		●		5	50	mV
V_{OS}	Output Offset Voltage				1.23		V
$\lvert\Delta V_{OS}\rvert$	Delta V_{OS}		●		5	50	mV
t_{RLVDS}	Output Rise Time, 20% to 80%				200		ps
t_{FLVDS}	Output Fall Time, 80% to 20%				200		ps
	Short Circuit Current to Common	Shorted to GND	●		7.4	24	mA
	Short Circuit to Complementary				3.7		mA
	Output Duty Cycle	M4 ≥ 2	●	45	50	55	%
Clock Output Skews (OUT0⁺, OUT0⁻, OUT1⁺, OUT1⁻, OUT2⁺, OUT2⁻, OUT3⁺, OUT3⁻, OUT4⁺, OUT4⁻)							
t_{SKEW1}	Maximum Skew, from OUT0 to OUT1				±10	±35	ps
t_{SKEW2}	Maximum Skew, from OUT0 to OUT2				±10	±35	ps
t_{SKEW3}	Maximum Skew, from OUT0 to OUT3				±10	±35	ps
t_{SKEW4}	Maximum Skew, from OUT0 to OUT4				±20		ps
	Maximum Skew, All CML Outputs	One Part			±20	±40	ps
	Maximum Skew, All CML Outputs	Multiple Parts, RAO = SN = SR = 1			±50	±100	ps
Power Supply Voltages							
	V_{REF}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{OUT}^+ Supply Range		●	3.15	3.3	3.45	V
	V_D^+ Supply Range		●	3.15	3.3	3.45	V
	V_{RF}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{VCO}^+ Supply Range		●	4.75	5.0	5.25	V
	V_{CP}^+ Supply Range		●	4.2		5.25	V
Power Supply Currents							
I_{DDOUT}	V_D^+, V_{OUT}^+ Supply Current	Digital Inputs at Supply Levels, PDOUT=1			32		µA
		Digital Inputs at Supply Levels, SYNC = 3.3V	●		210	254	mA
I_{CC-5V}	Sum V_{CP}^+, V_{VCO}^+ Supply Currents	I_{CP} = 11.2mA	●		56	70	mA
		I_{CP} = 1.0mA	●		33	43	mA
		PDALL = 1			510		µA
$I_{CC-3.3V}$	Sum V_{REF}^+, V_{RF}^+ Supply Currents		●		115	130	mA
		PDALL = 1			140		µA
	V_D^+, V_{OUT}^+ Supply Current Deltas	MCx[1:0] = 2 (x = 0, 1, 2, or 3)			–31		mA
		MCx[1:0] = 3 (x = 0, 1, 2, or 3)			–43		mA
		MC4[1:0] = 2			–21		mA
		MC4[1:0] = 3			–34		mA
		SYNC = V_{OUT}^+ or SSYNC = 1			11		mA
Phase Noise and Spurious							
L_{VCO}	LTC6951 VCO Phase Noise (f_{VCO} = 4.0GHz, f_{OUT0} = 2.0GHz, P = 2, M0 = 1, Note 7)	10kHz Offset			–87		dBc/Hz
		100kHz Offset			–113		dBc/Hz
		1MHz Offset			–135		dBc/Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V_{REF}^+ = V_D^+ = V_{RF}^+ = V_{OUT}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$ unless otherwise specified. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	LTC6951 VCO Phase Noise (f_{VCO} = 5.0GHz, f_{OUT0} = 2.5GHz, P = 2, M0 = 1, Note 7)	10kHz Offset			–83		dBc/Hz
		100kHz Offset			–110		dBc/Hz
		1MHz Offset			–133		dBc/Hz
	LTC6951-1 VCO Phase Noise (f_{VCO} = 5.4GHz, f_{OUT0} = 2.7GHz, P = 2, M0 = 1, Note 7)	10kHz Offset			–83		dBc/Hz
		100kHz Offset			–110		dBc/Hz
		1MHz Offset			–133		dBc/Hz
	LTC6951-1 CML Output Noise/Jitter (f_{VCO} = 5.4GHz, f_{OUT0} = f_{OUT1} = f_{OUT2} = f_{OUT3} = 2.7GHz, P = 2, M0 = M1 = M2 = M3 = 1, Notes 9, 12)	Phase Noise 10kHz Offset			–119		dBc/Hz
		Phase Noise 1MHz Offset			–129		dBc/Hz
		Phase Noise 40MHz Offset			–153		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			90		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			115		fs_{RMS}
	LTC6951 CML Output Noise/Jitter (f_{VCO} = 5.0GHz, f_{OUT0} = f_{OUT1} = f_{OUT2} = f_{OUT3} = 2.5GHz, P = 2, M0 = M1 = M2 = M3 = 1, Notes 9, 12)	Phase Noise 10kHz Offset			–119		dBc/Hz
		Phase Noise 1MHz Offset			–129		dBc/Hz
		Phase Noise 40MHz Offset			–153		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			90		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			115		fs_{RMS}
	LTC6951 CML Output Noise/Jitter (f_{VCO} = 5.0GHz, f_{OUT0} = f_{OUT1} = f_{OUT2} = f_{OUT3} = 1.25GHz, P = 2, M0 = M1 = M2 = M3 = 2, Notes 9, 12)	10kHz Offset			–125		dBc/Hz
		1MHz Offset			–135		dBc/Hz
		40MHz Offset			–156		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			88		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			115		fs_{RMS}
	LTC6951 CML Output Noise/Jitter (f_{VCO} = 4.0GHz, f_{OUT0} = f_{OUT1} = f_{OUT2} = f_{OUT3} = 250MHz, P = 4, M0 = M1 = M2 = M3 = 4, Notes 9, 12)	10kHz Offset			–140		dBc/Hz
		1MHz Offset			–150		dBc/Hz
		40MHz Offset			–165		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			83		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			115		fs_{RMS}
	LTC6951 LVDS Output Noise/Jitter (f_{VCO} = 4.0GHz, f_{OUT4} = 250MHz, P = 4, M4 = 4, Notes 9, 12)	10kHz Offset			–140		dBc/Hz
		1MHz Offset			–150		dBc/Hz
		40MHz Offset			–162		dBc/Hz
		Jitter, 12kHz to 20MHz Integration BW			88		fs_{RMS}
		Jitter, 100Hz to f_{OUTx} Integration BW			140		fs_{RMS}
L_{NORM}	Normalized In-Band Phase Noise Floor	I_{CP} = 11.2mA (Notes 8, 9, 10)			–229		dBc/Hz
$L_{1/f}$	Normalized In-Band 1/f Phase Noise	I_{CP} = 11.2mA (Notes 8, 11)			–277		dBc/Hz
	In-Band Phase Noise Floor	(Notes 8, 9, 10, 13)			–134		dBc/Hz
	Integrated Phase Noise from 100Hz to 40MHz	(Notes 9, 13)			0.015		°RMS
	Spurious	f_{OFFSET} = f_{PFD}, PLL Locked (Notes 9, 13, 14, 15)			–95		dBc

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6951IUHF and LTC6951IUHF-1 are guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 105°C. Under maximum operating conditions, air flow or heat sinking may be required to maintain a junction temperature of 105°C or lower. It is strongly recommended that the Exposed Pad (Pin 41) be soldered directly to the ground plane with an array of thermal vias as described in the Applications Information section.

Note 3: Valid for 1.50V ≤ V(TUNE) ≤ 2.85V with part calibrated after a power cycle or software power-on-reset (POR).

Note 4: Based on characterization.

Note 5: For 1.4V < V(CP) < 3.0V.

Note 6: Measurement requires RAO = 1 with SR = 1 at SYNC rising edge and SN = 1 at SYNC falling edge. REF^+ is a CMOS level signal with a 1ns rise time and the measurement point at the 50% crossing. SYNC is a CMOS level signal with a 1ns rise and fall time. For SYNC rising and SR = 1, the measurement point is 1.55V. For SYNC falling and SN = 1, the measurement point is 0.8V.

Note 7: Measured outside the loop bandwidth, using a narrowband loop.

Note 8: Measured inside the loop bandwidth with the loop locked.

Note 9: Reference frequency supplied by Wenzel 501-04516, f_{REF} = 100MHz, P_{REF} = 10dBm.

Note 10: Output Phase Noise Floor is calculated from Normalized Phase Noise Floor by $L_{OUT} = L_{NORM} + 10\log_{10}(f_{PFD}) + 20\log_{10}(f_{OUTx}/f_{PFD})$.

Note 11: Output 1/f Noise is calculated from Normalized 1/f Phase Noise by $L_{OUT(1/f)} = L_{1/f} + 20\log_{10}(f_{OUTx}) – 10\log_{10}(f_{OFFSET})$.

Note 12: I_{CP} = 11.2mA, f_{PFD} = 100MHz, FILT = 0, Loop BW = 340kHz

Note 13: I_{CP} = 11.2mA, f_{PFD} = 100MHz, FILT = 0, Loop BW = 340kHz; f_{OUT0} = 500MHz, f_{VCO} = 4.0GHz.

Note 14: Measured using DC2248A.

Note 15: Measured using differential LTC6951 outputs driving LTC6954. LTC6954 provides differential to single-ended conversion for rejection of common mode spurious signals. See the Applications Information section for details.

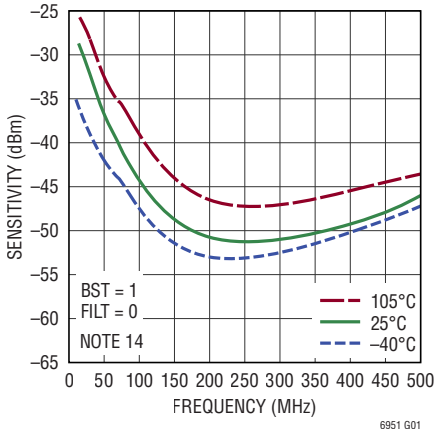
Note 16: When P = 2.5 or 3.5 and Mx = 1, a subharmonic of approximately –45dBc to –25dBc is generated at the output at $f_{OUT}/2$. While most applications are not affected by this spur, some, such as ADC and DAC sampling, are degraded. For applications sensitive to subharmonic spurs, these settings are not recommended unless the output frequency is further divided by at least 2 (i.e. ADC clock divider).

Note 17: Each output can be individually powered down by setting the output's MCx[1:0] bits to 3. See Tables 16 and 17.

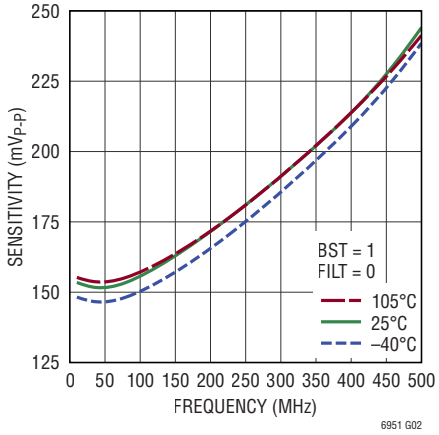
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_{OUT}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, Unless otherwise noted.

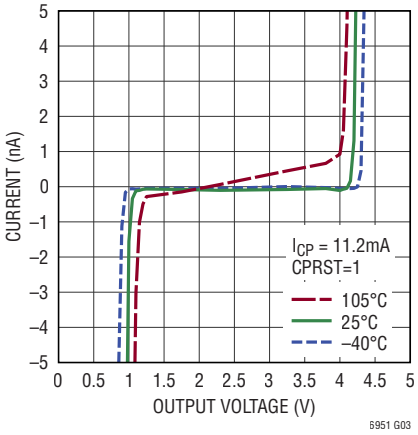
REF Input Sensitivity vs Frequency



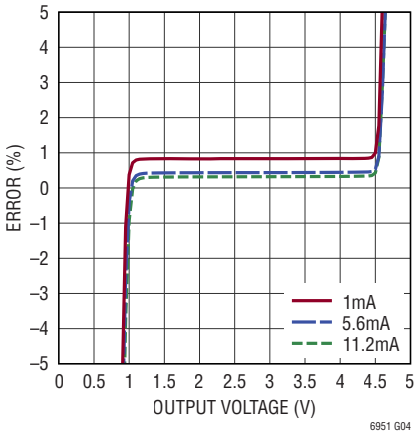
REF Input Signal Detected vs Frequency, Temperature



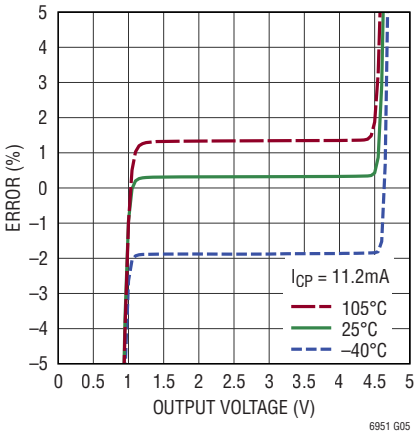
Charge Pump Hi-Z Current vs Voltage, Temperature



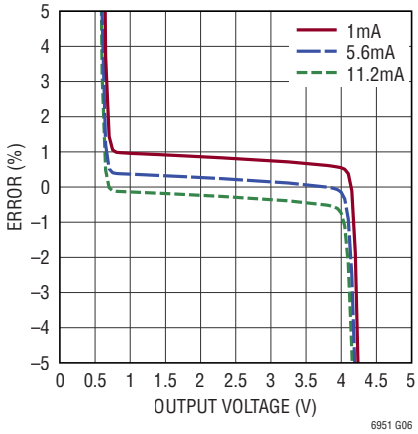
Charge Pump Sink Current Error vs Voltage, Output Current



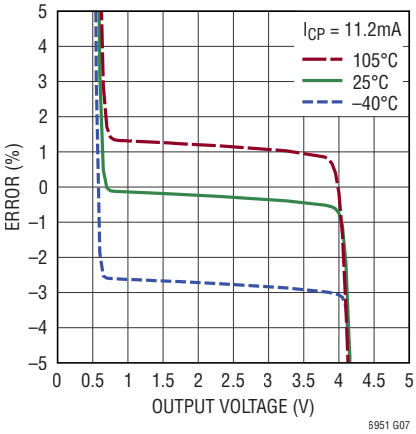
Charge Pump Sink Current Error vs Temperature



Charge Pump Source Current Error vs Voltage, Output Current



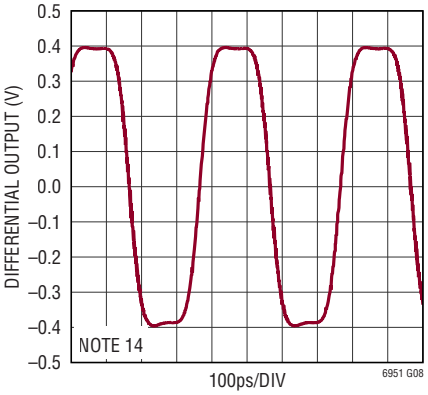
Charge Pump Source Current Error vs Voltage, Temperature



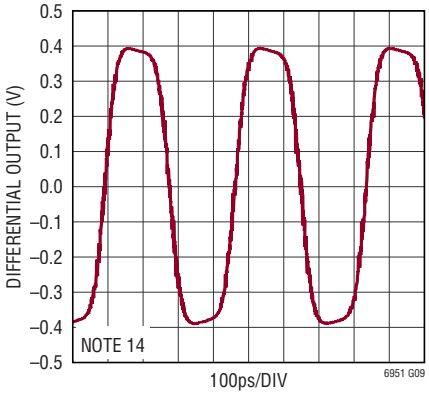
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_{OUT}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, Unless otherwise noted.

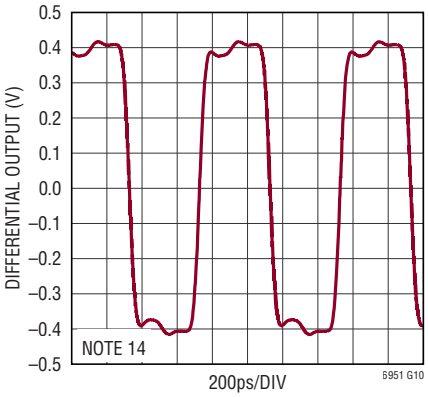
LTC6951 CML Differential Output at 2.5GHz



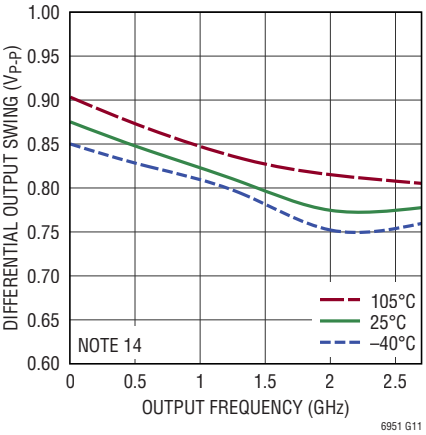
LTC6951-1 CML Differential Output at 2.7GHz



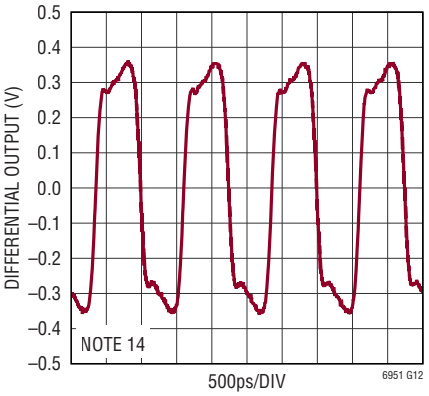
LTC6951 CML Differential Output at 1.25GHz



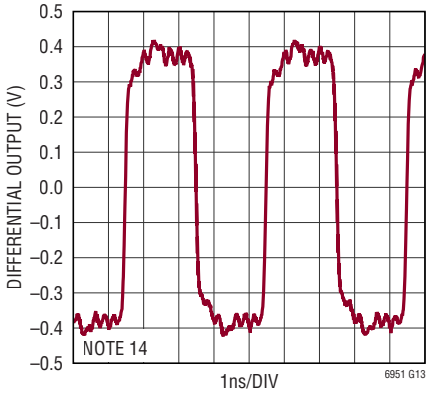
CML Differential Output Swing vs Frequency, Temperature



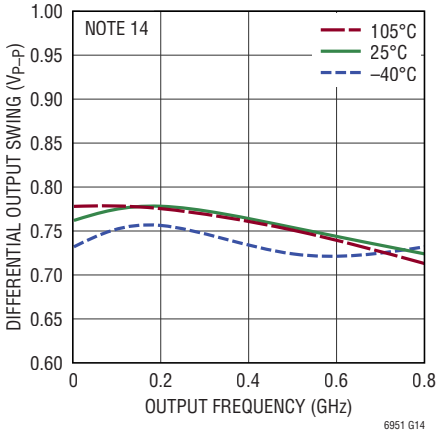
LVDS Differential Output at 800MHz



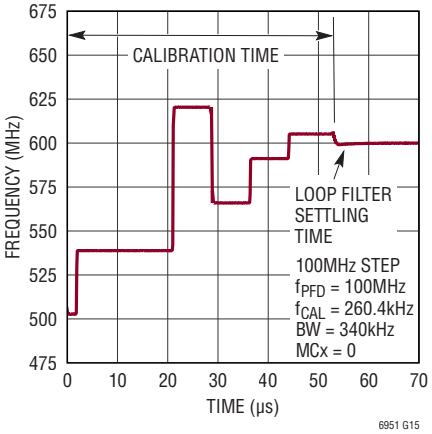
LVDS Differential Output at 250MHz



LVDS Differential Output Swing vs Frequency, Temperature



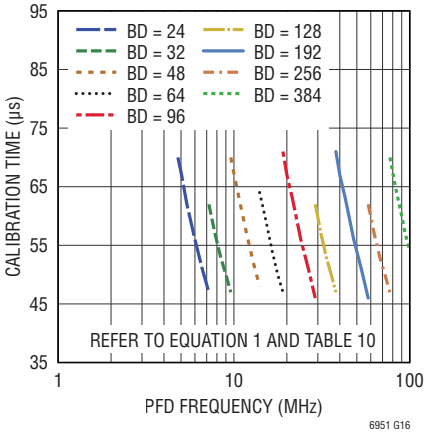
Frequency Step Transient, RAO = 0



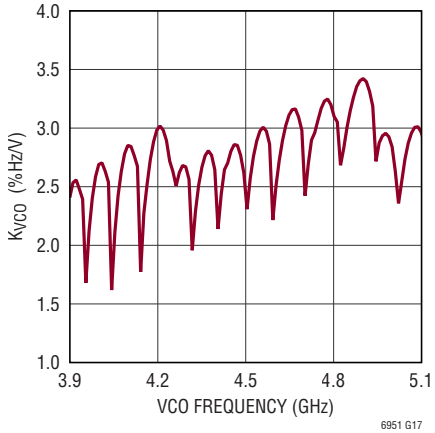
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_{OUT}^+ = V_D^+ = V_{RF}^+$ = 3.3V, $V_{CP}^+ = V_{VCO}^+$ = 5V, Unless otherwise noted.

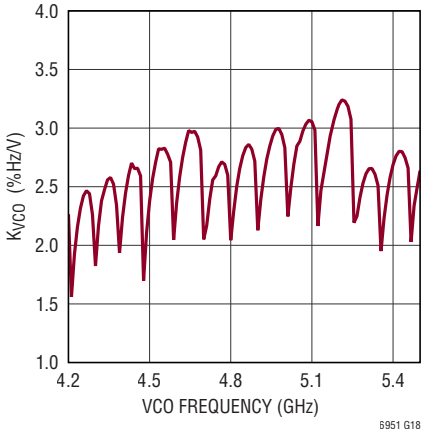
Max Calibration Time (RAO = 0) vs f_{PD}, B Divide Value



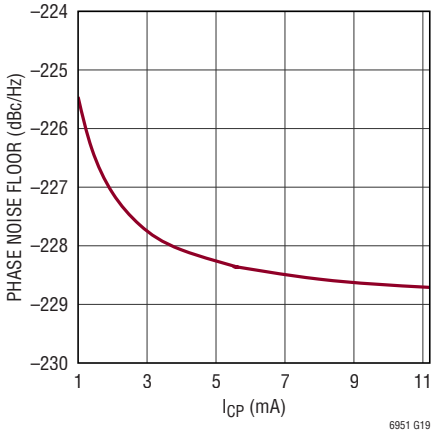
LTC6951 VCO Tuning Sensitivity



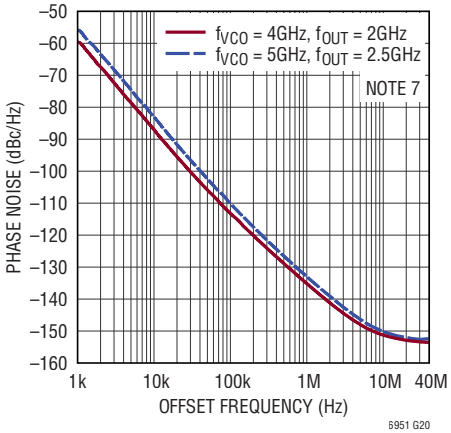
LTC6951–1 VCO Tuning Sensitivity



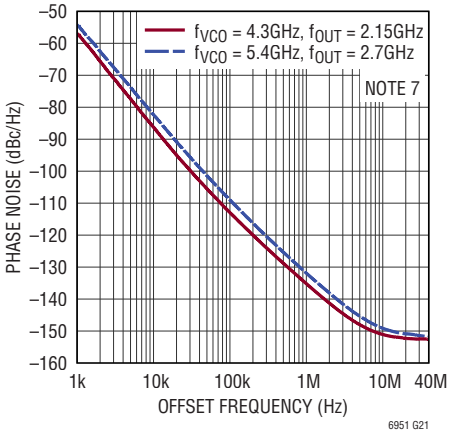
Normalized In-Band Phase Noise Floor vs CP Current



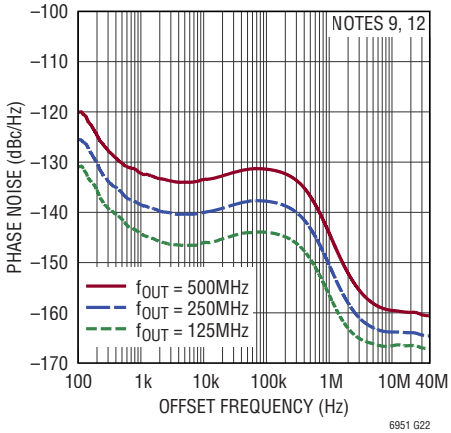
LTC6951 VCO Phase Noise at CML Outputs, P = 2, Mx = 1



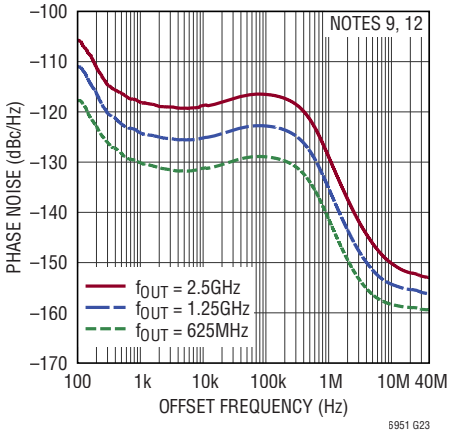
LTC6951-1 VCO Phase Noise at CML Outputs, P = 2, Mx = 1



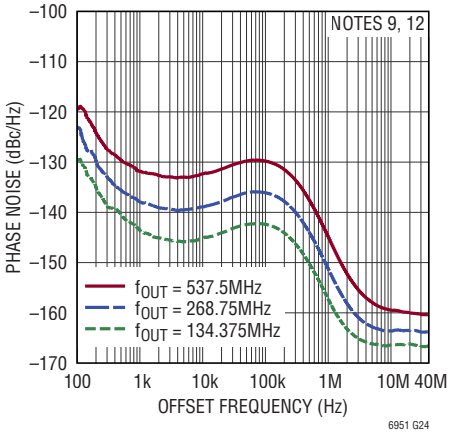
LTC6951 Phase Noise at CML Outputs, f_{VCO} = 4GHz, P = 2, Mx = 4, 8 and 16



LTC6951 Phase Noise at CML Outputs, f_{VCO} = 5GHz, P = 2, Mx = 1, 2 and 4



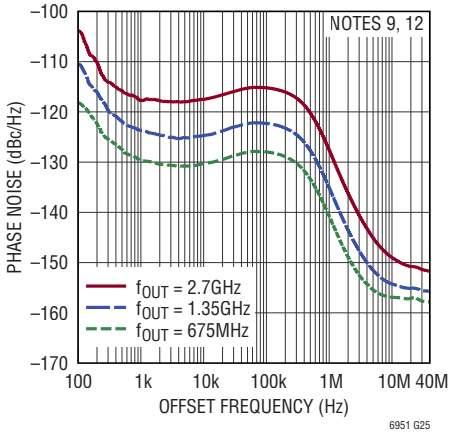
LTC6951-1 Phase Noise at CML Outputs, f_{VCO} = 4.3GHz, P = 2, Mx = 4, 8 and 16



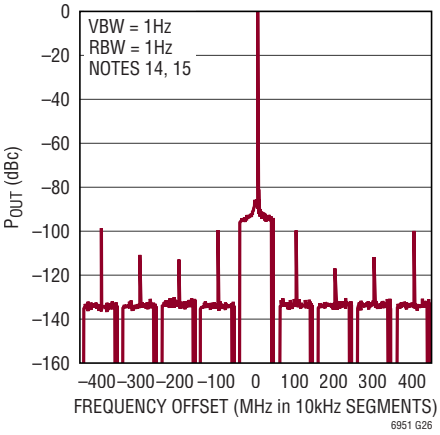
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. $V_{REF}^+ = V_{OUT}^+ = V_D^+ = V_{RF}^+ = 3.3V$, $V_{CP}^+ = V_{VCO}^+ = 5V$, Unless otherwise noted.

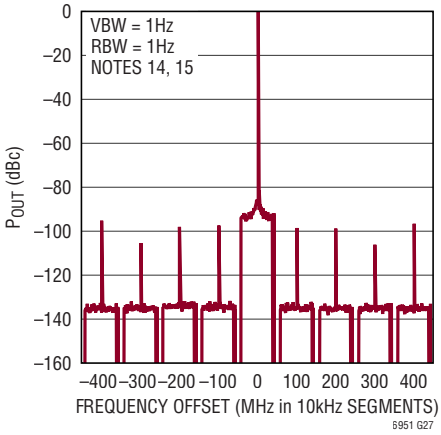
LTC6951-1 Phase Noise at CML Outputs, f_{VCO} = 5.4GHz, P = 2, Mx = 1, 2 and 4



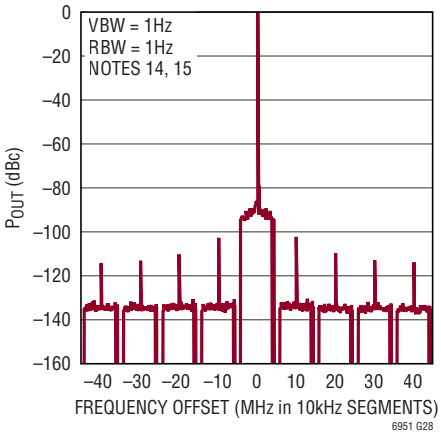
Spurious Response f_{RF} = 1250MHz, f_{REF} = 100MHz, f_{PFD} = 100MHz, Loop BW = 340kHz



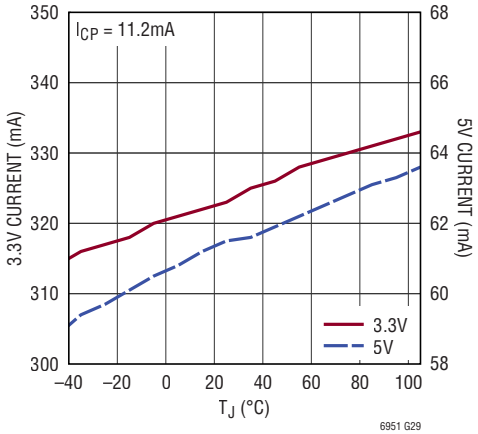
Spurious Response f_{RF} = 500MHz, f_{REF} = 100MHz, f_{PFD} = 100MHz, Loop BW = 340kHz



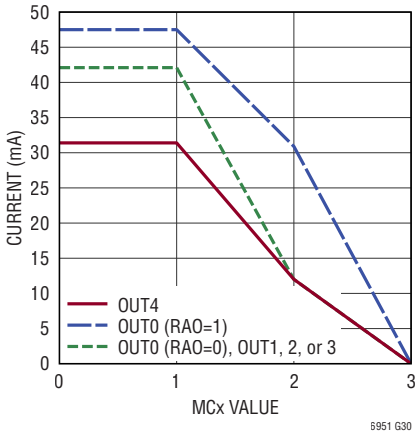
Spurious Response f_{RF} = 500MHz, f_{REF} = 100MHz, f_{PFD} = 10MHz, Loop BW = 290kHz



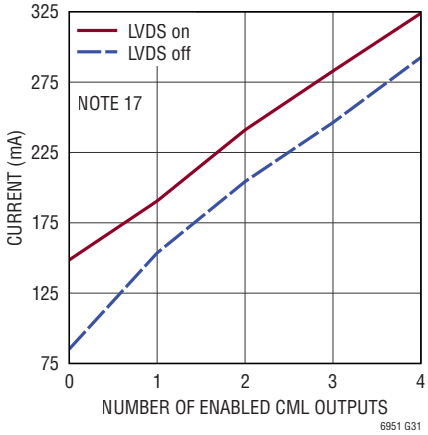
Supply Current vs Temperature RAO = 0, All Outputs Enabled



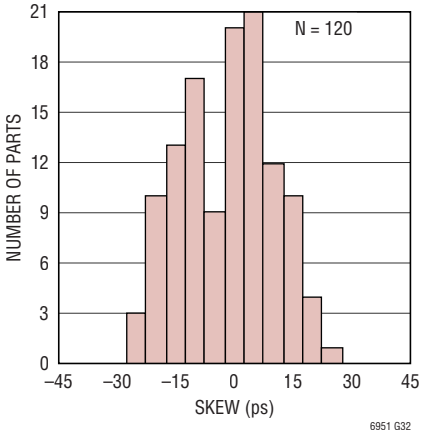
V_{OUT}^+ Supply Current per Output vs MCx Value



3.3V Supply Current vs Number of Enabled CML Outputs



Part to Part Skew,CML Outputs, f_{OUT} = 1GHz



PIN FUNCTIONS

V_{OUT}^+, V_D^+ (Pins 1, 4, 7, 10, 13, 16): 3.15V to 3.45V Positive Supply Pins for Output Dividers, SYNC Function and Serial Port. Each pin should be separately bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible. V_{OUT}^+, V_D^+, V_{RF}^+, and V_{REF}^+ must all be at the same voltage.

OUT2⁻, OUT2⁺ (Pins 2, 3): 2.5V CML Output Signals. The M2 output divider is buffered and presented differentially on these pins. The outputs are connected with 50Ω (typical) pull-up resistors tied to an internal resistive common mode point. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

OUT1⁻, OUT1⁺ (Pins 5, 6): 2.5V CML Output Signals. The M1 output divider is buffered and presented differentially on these pins. The outputs are connected with 50Ω (typical) pull-up resistors tied to an internal resistive common mode point. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

OUT0⁻, OUT0⁺ (Pins 8, 9): 2.5V CML Output Signals. The M0 output divider is buffered and presented differentially on these pins. The outputs are connected with 50Ω (typical) pull-up resistors tied to an internal resistive common mode point. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

OUT3⁻, OUT3⁺ (Pins 11, 12): 2.5V CML Output Signals. The M3 output divider is buffered and presented differentially on these pins. The outputs are connected with 50Ω (typical) pull-up resistors tied to an internal resistive common mode point. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

OUT4⁻, OUT4⁺ (Pins 14, 15): LVDS Output Signals. The M4 output divider is buffered and presented differentially on these pins. The far end of the transmission line is typically terminated with 100Ω connected across the outputs. See the Operation and Applications Information section for more details.

$\overline{CS}$ (Pin 17): Serial Port Chip Select. This CMOS input initiates a serial port communication burst when driven low, ending the burst when driven back high. See the Operation section for more details.

SCLK (Pin 18): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. See the Operation section for more details.

SDI (Pin 19): Serial Port Data Input. The serial port uses this CMOS input for data. See the Operation section for more details.

SDO (Pin 20): Serial Port Data Output. This CMOS three-state output presents data from the serial port during a read communication burst. Optionally attach a resistor of > 200kΩ to GND to prevent a floating output. See the Applications Information section for more details.

V_{RF}^+ (Pin 21): 3.15V to 3.45V Positive Supply Pin for RF Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible. V_{OUT}^+, V_D^+, V_{RF}^+, and V_{REF}^+ must all be at the same voltage.

BB (Pin 22): RF Reference Bypass. This output has a 6.5k resistance and must be bypassed with a 0.47µF ceramic capacitor to GND. Do not couple this pin to any other signal.

TUNE (Pin 23): VCO Tuning Input. This frequency control pin is normally connected to the external loop filter. See the Applications Information section for more details.

TB (Pin 24): VCO Bypass. This output has a 7k resistance and must be bypassed with a 1.0µF ceramic capacitor to GND. It is normally connected to CM_A, CM_B, and CM_C with a short trace. Do not couple this pin to any other signal.

PIN FUNCTIONS

GND (Pins 25, 29, Exposed Pad Pin 41): Negative Power Supply (Ground). These pins should be tied directly to the ground plane with multiple vias for each pin. The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance.

CM_C, CM_B, CM_A (Pins 26, 27, 28): VCO Bias Inputs. These inputs are normally connected to TB with a short trace and bypassed with a 1µF ceramic capacitor to GND. Do not couple these pins to any other signal. *For best phase noise performance, DO NOT place a trace between these pads underneath the package.*

BVCO (Pin 30): VCO Bypass Pin. This output must be bypassed with a 1.0µF ceramic capacitor to GND. Do not couple this pin to any other signal.

V_{VCO}^+ (Pin 31): 4.75V to 5.25V Positive Supply Pin for VCO Circuitry. This pin should be bypassed directly to the ground plane using a 0.01µF ceramic capacitor as close to the pin as possible.

GND (Pins 32, 40): Negative Power Supply (Ground). These pins are attached directly to the Die Attach Paddle (DAP) and should be tied directly to the ground plane.

V_{CP}^+ (Pin 33): 4.2V to 5.25V Positive Supply Pin for Charge Pump Circuitry. This pin should be bypassed directly to the ground plane using two ceramic capacitors of 1µF and 0.01µF as close to the pin as possible. Additionally, a 10Ω resistor should be added in series with the 5V power supply to reduce switching noise. The resistor should be placed between the 5V supply rail and the two ceramic capacitors.

CP (Pin 34): Charge Pump Output. This bidirectional current output is normally connected to the external loop filter. See the Applications Information section for more details.

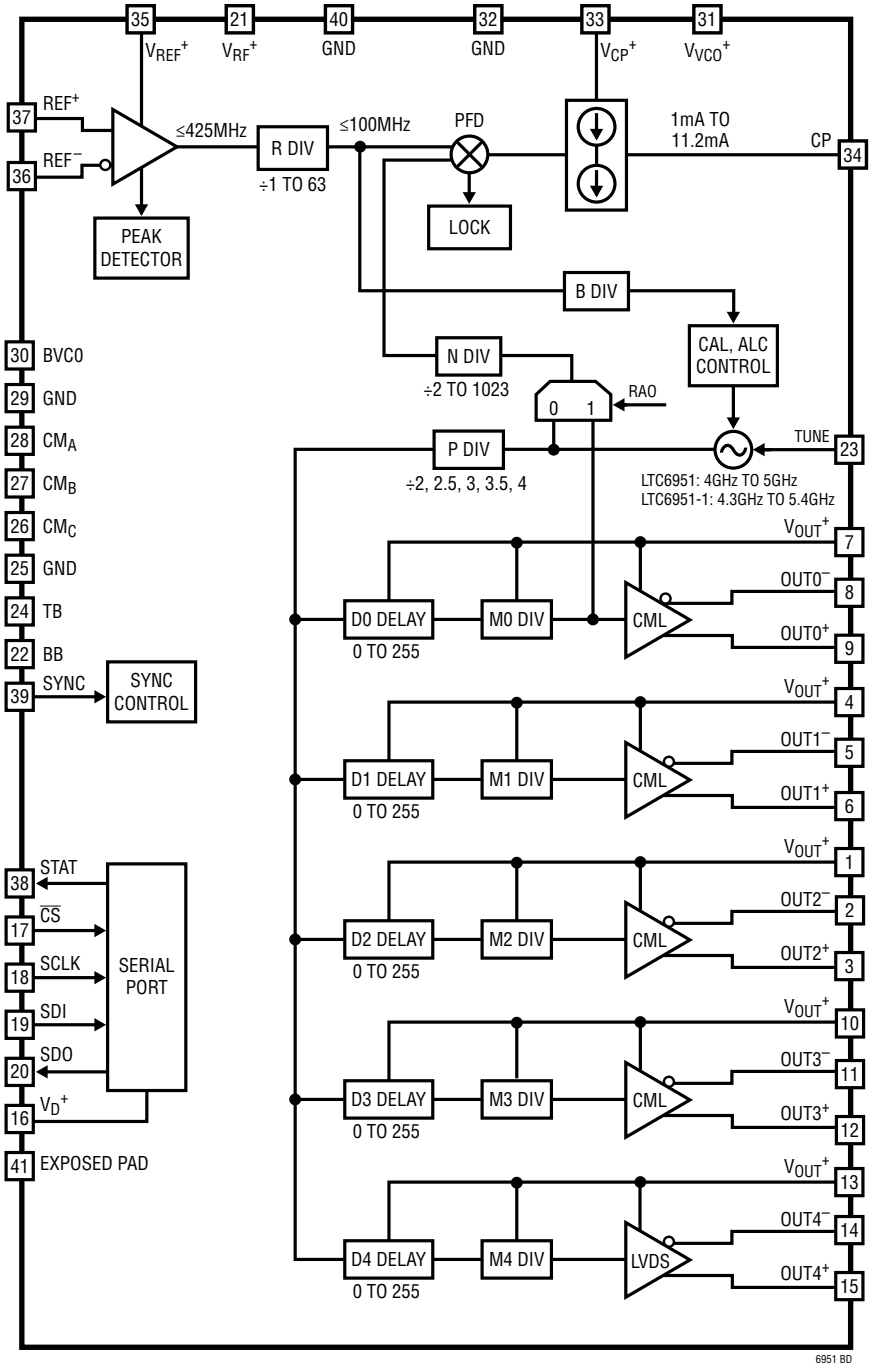
V_{REF}^+ (Pin 35): 3.15V to 3.45V Positive Supply Pin for Reference Input Circuitry. This pin should be bypassed directly to the ground plane using a 0.1µF ceramic capacitor as close to the pin as possible. V_{OUT}^+, V_D^+, V_{RF}^+, and V_{REF}^+ must all be at the same voltage.

REF^-, REF^+ (Pins 36, 37): Reference Input Signals. This differential input is buffered with a low noise amplifier, which feeds the reference divider. They are self-biased and must be AC-coupled with 1µF capacitors. If used single-ended with $V(REF^+) \leq 2.7V_{P-P}$, bypass REF^- to GND with a 1µF capacitor. If used single-ended with $V(REF^+) > 2.7V_{P-P}$, bypass REF^- to GND with a 47pF capacitor.

STAT (Pin 38): Status Output. This signal is a configurable logical OR combination of the UNLOCK, ALCHI, ALCLO, $\overline{LOCK}$, LOCK, $\overline{REFOK}$, and REFOK status bits, programmable via the STATUS register. See the Operation section for more details.

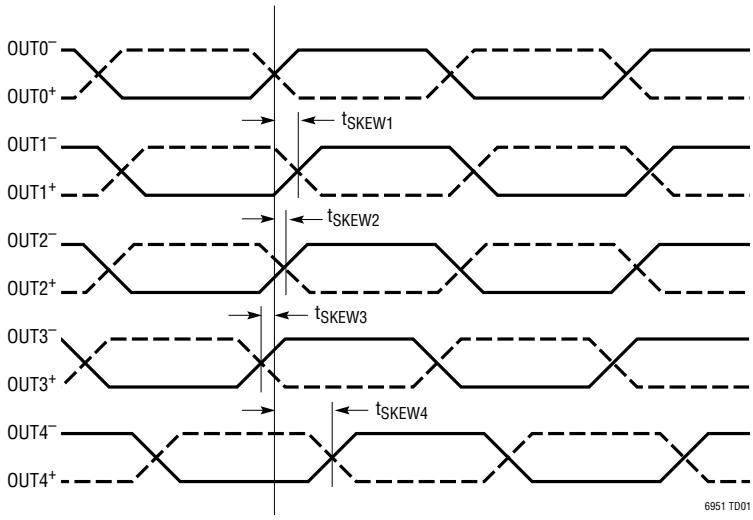
SYNC (Pin 39): Synchronization Input. This CMOS input stops the output dividers when driven high and initiates synchronization when driven back low when enabled for each output. When using the SSYNC software synchronization bit, the SYNC pin must be held at a logic low state. See the Operation and Applications Information section for more details.

BLOCK DIAGRAM

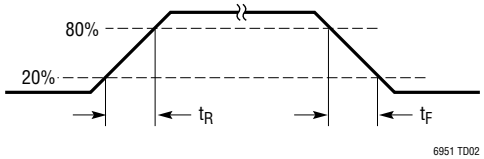


TIMING DIAGRAMS

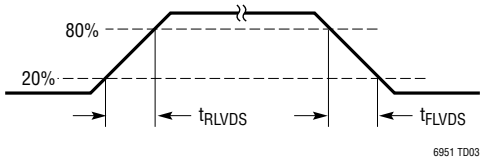
Output Skews



Differential CML Rise/Fall Times



Differential LVDS Rise/Fall Times



OPERATION

The LTC6951 is a high-performance integer-N PLL, complete with a low noise VCO. Its multi-output clock generator incorporates Linear Technology's proprietary EZSync and ParallelSync standards, allowing synchronization across multiple outputs and multiple chips. The device is able to achieve superior integrated jitter performance by the combination of its extremely low in-band phase noise and excellent VCO noise characteristics.

REFERENCE INPUT BUFFER

The PLL's reference frequency is applied differentially on pins REF⁺ and REF⁻. These high-impedance inputs are self-biased and must be AC-coupled with 1µF capacitors (see Figure 1 for a simplified schematic). Alternatively, the inputs may be used single-ended by applying the reference frequency at REF⁺ and bypassing REF⁻ to GND with a 1µF capacitor. If the single-ended signal is greater than $2.7V_{P-P}$, then use a 47pF capacitor for the GND bypass.

A high quality signal must be applied to the REF± inputs as they provide the frequency reference to the entire PLL. To achieve the part's in-band phase noise performance, apply a sine wave signal of at least 6dBm into 50Ω, or a square wave of at least $0.5V_{P-P}$ with slew rate of at least 20V/µs. Figure 2 shows recommended interfaces for different reference types.

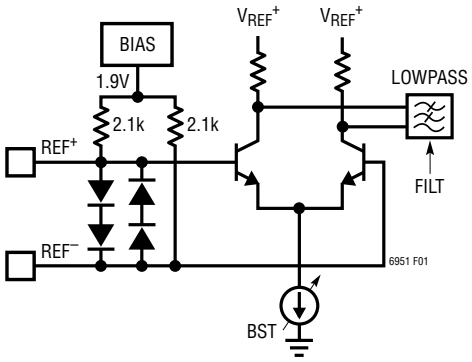


Figure 1. Simplified REF Interface Schematic

Additional options are available through serial port register h03 to further refine the application. Bit FILT controls the reference input buffer's low-pass filter, and should be set for sine wave signals based upon f_{REF} to limit the reference's wideband noise. The FILT bit must be set correctly to reach the L_{NORM} normalized in-band phase noise floor. See Table 1 for recommended settings. Square wave inputs will have FILT set to "0".

OPERATION

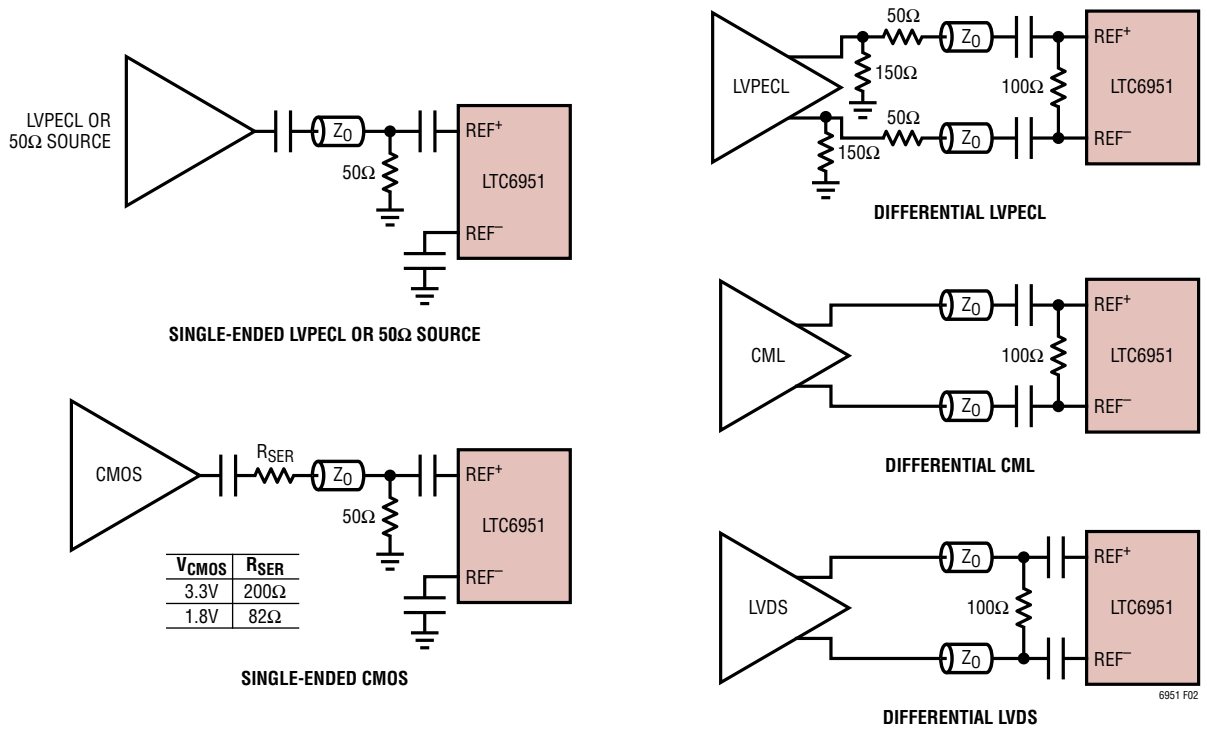


Figure 2. Common Reference Input Interface Configurations. All Z_0 Signal Traces Are 50Ω Transmission Lines and All Caps Are 1µF

Table 1. FILT Programming

FILT	Sine Wave f_{REF}	Square Wave f_{REF}
1	<20MHz	N/A
0	≥20MHz	All f_{REF}

The BST bit should be set based upon the input signal level to prevent the reference input buffer from saturating. The BST programming is the same whether the input is a sine wave or a square wave. See Table 2 for recommended settings and the Applications Information section for programming examples.

Table 2. BST Programming

BST	V_{REF}
1	<1.6V_{P-P}
0	≥1.6V_{P-P}

Peak Detector

A reference input peak detection circuit is provided on the REF± inputs to detect the presence of a reference signal and provides the REFOK and $\overline{\text{REFOK}}$ status flags available through both the STAT output and serial port register h00. $\overline{\text{REFOK}}$ is the logical inverse of REFOK. The circuit has hysteresis to prevent the REFOK flag from chattering at the detection threshold. The reference peak detector may be powered-down using the PDREFPK bit found in register h02.

The peak detector approximates an RMS detector, therefore sine and square wave inputs will give different detection thresholds by a factor of 4/π. See Table 3 for REFOK detection values.

Table 3. REFOK, $\overline{\text{REFOK}}$ Status Output vs REF Input

REFOK	$\overline{\text{REFOK}}$	Sine Wave f_{REF}	Square Wave f_{REF}
1	0	≥350mV_{P-P}	≥275mV_{P-P}
0	1	<100mV_{P-P}	<75mV_{P-P}

OPERATION

REFERENCE ALIGNED OUTPUT (RAO)

The RAO bit (register h03) controls the fundamental configuration of the PLL. Figure 3 shows the PLL loop diagram with bit RAO set to "0", which is the power-up default. All five outputs can be synchronized and delayed relative to each other, but will not be aligned to the Reference input. Systems needing alignment to the Reference input either on an individual basis or across multiple LTC6951s can set RAO to "1" to have the PLL loop diagram as shown in Figure 4. The P and M0 dividers are now part of the overall feedback loop. Table 4 describes the differences in the PLL feedback elements versus the RAO bit setting. Only when the P and M0 dividers are in the feedback loop can the output rising edges be coincident with the N divider output and by inference the R divider output.

When RAO is set to a "1", bits SR and SN become active and allow known and repeatable latency to the outputs in addition to known alignment to the Reference input. Figure 5 shows the operation of the SR bit and Figure 11 shows the operation of the SN bit. Table 5 is a brief description of the SR and SN functions. See the ParallelSync Multi-Chip Synchronization Example in the Applications Information section for a programming example and output timing diagrams of the RAO mode.

Table 4. RAO Programming

RAO	PLL FEEDBACK ELEMENTS
0	N Divider
1	N, P, M0 Dividers

Table 5. SN and SR Function Description

RAO	SN	SR	Description
0	NA	NA	Unknown phase relationship from REF input to outputs, EZSync timing.
1	0	0	Outputs phase aligned to REF input, unknown SYNC to output latency, EZSync timing.
1	1	1	Outputs phase aligned to REF input, known SYNC to output latency, critical SYNC to REF timing.

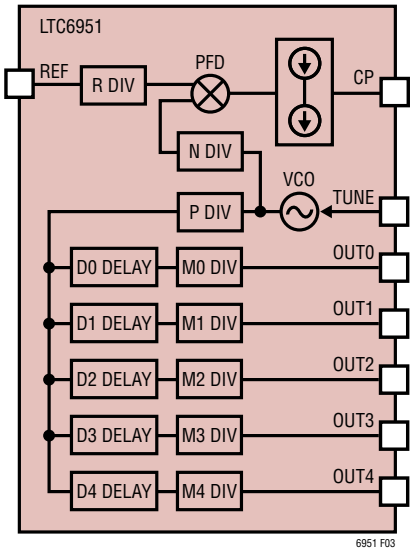


Figure 3. PLL loop diagram, RAO = 0

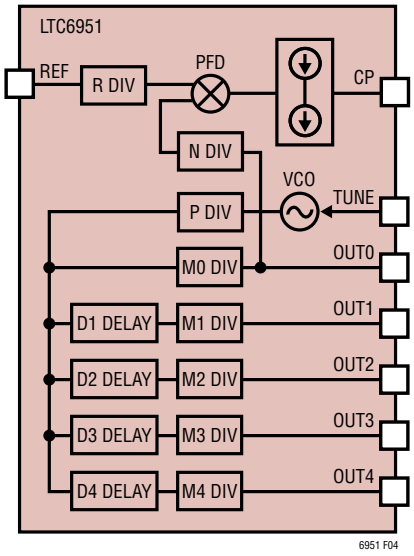


Figure 4. PLL loop diagram, RAO = 1

OPERATION

REFERENCE DIVIDER (R)

A 6-bit divider is used to reduce the frequency seen at the PFD. Its divide ratio R may be set to any integer from 1 to 63. Use the RD[5:0] bits found in register h05 to directly program the R divide ratio. See the Applications Information section for the relationship between R and the f_{REF}, f_{PFD}, f_{VCO} and f_{OUTx} frequencies.

A mode to provide synchronization of the Reference inputs to the R divider output (R ≥ 2) using the SYNC pin input rising edge is enabled when bits RAO in register h03 and SR in register h0A are set to "1". The SYNC pin rising edge must meet setup and hold timing to the rising edge of the Reference input. See Figure 5 for the timing relationships between the Reference input, SYNC and the R divider output. Note that changing the R divider output edge timing will force the PLL to lose phase lock but will return to normal operation after several loop time constants. See Reference Signal and Sync Timing for SR and SN Modes in the Applications Information section for the timing requirements of SYNC to REF in this mode.

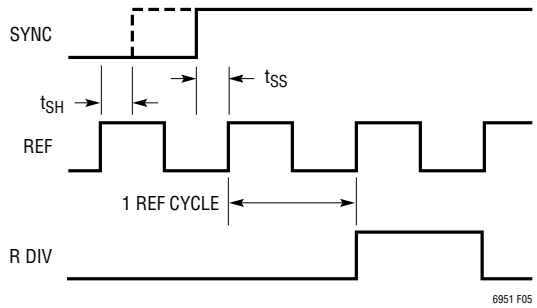


Figure 5. SYNC to REF timing (RAO = SR = 1)

PHASE/FREQUENCY DETECTOR (PFD)

The phase/frequency detector (PFD), in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the R and N dividers. This action provides the necessary feedback to phase-lock the loop, forcing a phase alignment at the PFD's inputs. The PFD may be disabled with the CPRST bit which prevents UP and DOWN pulses from being produced. See Figure 6 for a simplified schematic of the PFD.

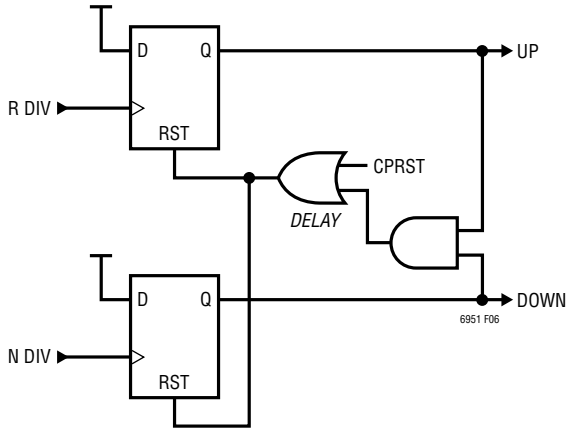


Figure 6. Simplified PFD Schematic

LOCK INDICATOR

The lock indicator uses internal signals from the PFD to measure phase coincidence between the R and N divider output signals. It is enabled by programming LKCT[1:0] in the serial port register h04 (see Table 7), and produces LOCK, $\overline{\text{LOCK}}$ and UNLOCK status flags, available through both the STAT output and serial port register h00. $\overline{\text{LOCK}}$ is the logical inverse of LOCK.

Note that f_{REF} must be present for the LOCK and UNLOCK flags to properly assert and clear.

The user sets the phase difference lock window time t_{LWW} for a valid LOCK condition with the LKWIN bit found in register h04. Table 6 contains recommended settings for different f_{PFD} frequencies. See the Applications Information section for examples.

Table 6. LKWIN Programming

LKWIN	t_{LWW}	f_{PFD}
0	5.0ns	>4.7MHz
1	10.7ns	≤4.7MHz

OPERATION

The PFD phase difference must be less than t_{LWW} for the COUNTS number of successive counts before the lock indicator asserts the LOCK flag. The LKCT[1:0] bits are used to set COUNTS depending upon the application. Set LKCT[1:0] = 0 to disable the lock indicator. See Table 7 for LKCT[1:0] programming and the Applications Information section for examples.

Table 7. LKCT[1:0] Programming

LKCT[1:0]	COUNTS
0	Lock Indicator Disabled
1	32
2	256
3	2048

When the PFD phase difference is greater than t_{LWW}, the lock indicator immediately asserts the UNLOCK status flag and clears the LOCK flag, indicating an out-of-lock condition. The UNLOCK flag is immediately de-asserted when the phase difference is less than t_{LWW}. See Figure 7 below for more details.

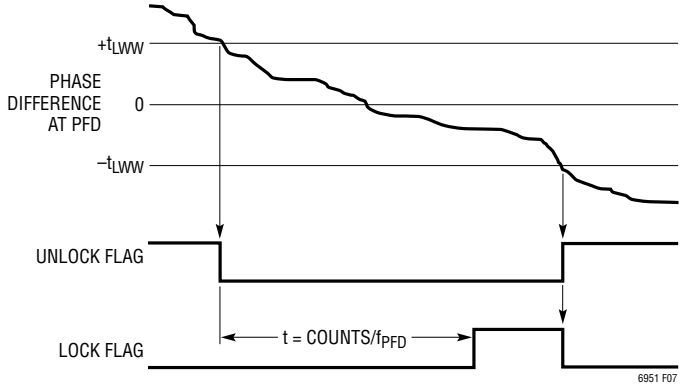


Figure 7. UNLOCK and LOCK Timing

CHARGE PUMP (CP)

The charge pump, controlled by the PFD, forces sink (DOWN) or source (UP) current pulses onto the CP pin, which should be connected to an appropriate loop filter. See Figure 8 for a simplified schematic of the charge pump.

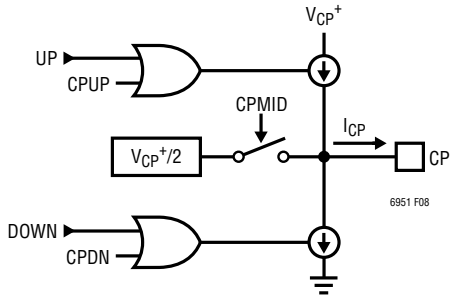


Figure 8. Simplified Charge Pump Schematic

The output current magnitude I_{CP} may be set from 1mA to 11.2mA using the CP[2:0] bits found in serial port register h07. A larger I_{CP} can result in lower in-band noise due to the lower impedance of the loop filter components. See Table 8 for programming specifics and the Applications Information section for loop filter examples.

Table 8. CP[2:0] Programming

CP[2:0]	I_{CP}
0	1.0mA
1	1.4mA
2	2.0mA
3	2.8mA
4	4.0mA
5	5.6mA
6	8.0mA
7	11.2mA

OPERATION

Charge Pump Functions

The charge pump contains additional features to aid in system startup. See Table 9 below for a summary.

Table 9. Charge Pump Function Bit Descriptions

BIT	DESCRIPTION
CPDN	Force sink current.
CPMID	Enable mid-voltage bias.
CPRST	Reset PFD, Hi-Z CP.
CPUP	Force source current.
CPWIDE	Extend current pulse width.

The CPMID bit found in register h07 enables a resistive V_{CP}+/2 output bias which may be used to pre-bias troublesome loop filters into a valid voltage range. When using CPMID, it is recommended to also assert the CPRST bit, forcing a PFD reset which puts the charge pump into a Hi-Z state. Both CPMID and CPRST must be set to "0" for normal operation.

The CPUP and CPDN bits force a constant I_{CP} source or sink current, respectively, on the CP pin. The CPRST bit may also be used in conjunction with the CPUP and CPDN bits, allowing a pre-charge of the loop to a known state, if required. CPUP, CPDN, and CPRST must be set to "0" to allow the loop to lock.

The CPWIDE bit extends the charge pump output current pulse width by increasing the PFD reset path's delay value. CPWIDE is normally set to "0". Setting CPWIDE = 0 provides the best in-band phase noise performance.

VCO

The integrated VCO operates from 4GHz to 5GHz for the LTC6951 and 4.3GHz to 5.4GHz for the LTC6951-1. The frequency range of the VCO, coupled with the output prescaler and output divider capability, allows the LTC6951 to cover an extremely wide range of continuously selectable frequencies.

The BB and TB pins are used to bias internal VCO circuitry. The BB pin has a 6.5kΩ output resistance and should be bypassed with a 0.47µF ceramic capacitor to GND, giving a time constant of 3ms. The TB pin has a 7kΩ output resistance and should be bypassed with a 1µF ceramic capacitor to GND, resulting in a time constant of 7ms. Stable bias voltages are achieved after approximately three time constants following power-up or after deasserting the PDPLL or PDVCO bits.

VCO Calibration

The VCO must be calibrated each time its frequency is modified by any change in f_{REF}, the R divider value, or the N divider value when RAO = 0. Additionally when RAO = 1, any change in f_{REF}, the R divider value, the N divider value, the P divider value, or the M0 divider value requires VCO calibration (see the Applications Information section for the relationship between R, N, P, Mx, and the f_{REF}, f_{PFD}, f_{VCO}, and f_{OUTx} frequencies). *The output frequency is then stable over the LTC6951's entire temperature range, regardless of the temperature at which it was calibrated, until the part is reset due to a power cycle or software power-on-reset (POR).*

The output of the B divider is used to clock digital calibration circuitry as shown in the Block Diagram. The B value, programmed with bits BD[3:0], is dependent on the setting of the RAO bit. The relationship between bits BD[3:0], the B value, and f_{PFD} for RAO = 0 is shown in Table 10.

Table 10. BD[3:0] Programming, RAO = 0

BD[3:0]	B DIVIDE VALUE	f_{PFD} (MHz)
0	8	<2.4
1	12	2.4 to 3.6
2	16	3.6 to 4.8
3	24	4.8 to 7.2
4	32	7.2 to 9.6
5	48	9.6 to 14
6	64	14 to 19
7	96	19 to 29
8	128	29 to 38
9	192	38 to 58
10	256	58 to 77
11	384	>77
12 to 15	Invalid	

OPERATION

The relationship between bits BD[3:0], the B value, and the N value for RAO = 1 is shown in Table 11.

Table 11. BD[3:0] Programming, RAO = 1

BD[3:0]	B DIVIDE VALUE	N DIVIDE VALUE
0	8	NA
1	12	240 to 511
2	16	180 to 239
3	24	120 to 179
4	32	90 to 119
5	48	60 to 89
6	64	45 to 59
7	96	30 to 44
8	128	23 to 29
9	192	12 to 22
10	256	4 to 11
11	384	2 to 3
12 to 15	Invalid	

Once the RD[5:0], ND[9:0], and BD[3:0] bits are written and the reference frequency f_{REF} is present and stable at the REF± inputs, the VCO must be calibrated by setting CAL = 1 (the bit self-clears when calibration is complete). The calibration cycle takes between 12 and 14 clocks of the B divider output with the nominal calibration time shown in Equation 1. Setting bits MCx[1:0] = 1 selectively mutes the outputs during the calibration.

$$t_{CAL} = \frac{14 \bullet B}{f_{PFD}} \quad (1)$$

Note that the f_{REF} frequency and TB and BB voltages must be stable for proper calibration. Stable bias voltages are achieved after approximately three time constants (about 25ms) following power-up.

Setting AUTOCAL = 1 causes the CAL bit to be set automatically whenever serial port registers h05 or h06 are written. When AUTOCAL is enabled and RAO = 0, there is no need for a separate register write to set the CAL bit.

When RAO =1 the loop also uses the P and M0 divide values which are located in registers h08 and h09 which when changed will not trigger the CAL bit with AUTOCAL = 1.

It is recommended to set AUTOCAL = 0 in this mode and to calibrate the VCO by setting CAL = 1 after all the appropriate registers have been written. See Table 12 for a summary of the VCO bits.

Table 12. VCO Bit Descriptions

BIT	DESCRIPTION
AUTOCAL	Calibrate VCOs whenever registers h05 and h06 are written.
CAL	Start VCO calibration (auto clears).
MC0[1:0]	Setting to h1 mutes OUT0 output during calibration.
MC1[1:0]	Setting to h1 mutes OUT1 output during calibration.
MC2[1:0]	Setting to h1 mutes OUT2 output during calibration.
MC3[1:0]	Setting to h1 mutes OUT3 output during calibration.
MC4[1:0]	Setting to h1 mutes OUT4 output during calibration.

VCO Automatic Level Control (ALC)

The VCO uses an internal automatic level control (ALC) algorithm to maintain an optimal amplitude on the VCO resonator, and thus optimal phase noise performance. The user has several ALC configuration and status reporting options as seen in Table 13.

Table 13. ALC Bit Descriptions

BIT	DESCRIPTION
ALCCAL	Auto enable ALC during CAL operation.
ALCEN	Always enable ALC (overrides ALCCAL, ALCMON, and ALCULOK).
ALCHI	ALC too high flag (resonator amplitude too high).
ALCLO	ALC too low flag (resonator amplitude too low).
ALCMON	Enable amplitude monitoring for status flags only; does NOT enable ALC.
ALCULOK	Auto enable ALC when PLL unlocked.

Changes in the internal ALC output can cause extremely small jumps in the VCO frequency. These jumps may be acceptable in some applications but not in others. Use the above table to choose when the ALC is active. The ALCHI and ALCLO flags, valid only when the ALC is active or the ALCMON bit is set, may be used to monitor the resonator amplitude.

The ALC must be allowed to operate during or after a calibration cycle. At least one of the ALCCAL, ALCEN, or ALCULOK bits must be set.

OPERATION

VCO DIVIDER (N)

The 10-bit N divider provides the feedback from the VCO to the PFD. The divide ratio may be programmed from 32 to 1023, when bit RAO = 0. The divide ratio may be programmed from 2 to 511, when bit RAO = 1. Use the ND[9:0] bits found in registers h05 and h06 to directly program the N divide ratio. See the Applications Information section for the relationship between N and the f_{REF}, f_{PFD}, f_{VCO} and f_{OUTx} frequencies.

VCO PRESCALER (P)

The P divider reduces the VCO frequency and distributes it to the five output dividers. The available divide ratios of 2, 2.5, 3, 3.5 and 4, when coupled with the VCO frequency range, allow the P divider output to cover more than an octave of frequency. See Table 14 for programming specifics and the Applications Information section for the relationship between P and the f_{REF}, f_{PFD}, f_{VCO} and f_{OUTx} frequencies.

Table 14. PD[2:0] Programming

PD[2:0]	P
0	2
1	2.5
2	3
3	3.5
4	4
5 to 7	Invalid

OUTPUT DIVIDERS (M0, M1, M2, M3, M4)

The five independent output dividers are driven by the P divider. All settings of Mx ≥ 2 with any P value or Mx = 1 with P = 2, 3, or 4 provide a 50% duty cycle at the output. Setting Mx = 1 with P = 2.5 or 3.5 is allowable, but will produce a signal with a non-50% duty cycle (40% and 57%, respectively) and a large subharmonic spurious output. In systems where the LTC6951 output drives into a frequency divider of at least 2 (as in some ADCs), the subharmonic spur will be removed and the duty cycle will go to 50% at the frequency divider output.

The relationship between the Mx value and the MDx[3:0] bits is shown in Table 15. Unused dividers can be powered down to save current by setting the MCx[1:0] bits to 3. The description of the MCx[1:0] bits is shown in Table 16 and Table 17. Setting the bit RAO = 1 in register h03 causes the PLL to reconfigure with P, M0 and N as part of the overall VCO divide ratio to provide phase alignment between the outputs and the R divider output (f_{PFD}). See the Applications Information section for the relationship between M0, M1, M2, M3 and M4 and the f_{REF}, f_{PFD}, f_{VCO}, f_{OUT0}, f_{OUT1}, f_{OUT2}, f_{OUT3} and f_{OUT4} frequencies.

Table 15. MDx[3:0] Programming

MDx[3:0]	Mx
0	1
1	2
2	4
3	8
4	12
5	16
6	24
7	32
8	48
9	64
10	96
11	128
12	192
13	256
14	384
15	512

Table 16. MCx[1:0] Programming (x = 1 to 4)

MCx[1:0]	DESCRIPTION
0	Do not mute output on VCO CAL.
1	Mute output on VCO CAL.
2	Power down output (divider remains running and synchronized).
3	Power down divider and output.

Table 17. MC0[1:0] Programming

MC0[1:0]	DESCRIPTION
0	Do not mute output on VCO CAL.
1	Mute output on VCO CAL (RAO = 0). Power down output on VCO CAL (RAO = 1).
2	Power down output (divider remains running and synchronized).
3	Power down divider and output.

OPERATION

OUTPUT DELAYS (D0, D1, D2, D3, D4)

Each output divider can have the start time of the output delayed by integer multiples of the P divider output period during a synchronization event. The delay value Dx is programmed into the registers DLY0[7:0], DLY1[7:0], DLY2[7:0], DLY3[7:0] and DLY4[7:0] and can be any value from 0 to 255. Delays are only enabled with synchronization bits SYNCEN0, SYNCEN1, SYNCEN2, SYNCEN3 and SYNCEN4 set to "1". D0 is not available when bit RAO is set to "1". See the Operation section on Synchronization and the Applications Information section for details on the use of the delay settings.

CML OUTPUT BUFFERS (OUT0, OUT1, OUT2, OUT3)

Four of the outputs are very low noise, low skew 2.5V CML buffers. Each output can be AC- or DC-coupled and terminated with 100Ω differential. If a single-ended output is desired, each side of the CML output can be individually AC-coupled and terminated with 50Ω. The bits OINV0, OINV1, OINV2 and OINV3 can selectively invert the sense of each output to facilitate board routing without having to cross matched impedance traces. The bits MUTE0, MUTE1, MUTE2 and MUTE3 set the selected output to a logic "0" state with logic "0" sense set by the OINVx bits as shown in Table 18. (If bit RAO = 1, MUTE0 = 1 has no effect. Set MC0[1:0] = 2 to stop OUT0 from transitioning if RAO = 1.) To save power with the dividers running, each buffer can be turned off by setting the bits MC0[1:0], MC1[1:0], MC2[1:0], and MC3[1:0] to 2. See Figure 9 for circuit details and the Applications Information section for common interface configurations.

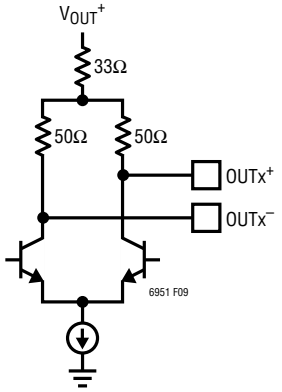


Figure 9. Simplified CML Interface Schematic (OUT0, OUT1, OUT2, OUT3)

LVDS OUTPUT BUFFER (OUT4)

The fifth output is a low noise LVDS buffer capable of operation up to 800MHz. This output is DC-coupled and terminated with 100Ω differential. The bit OINV4 can selectively invert the sense of the output to facilitate board routing without having to cross matched impedance traces. The bit MUTE4 sets the selected output to a logic "0" state with logic "0" sense set by the OINV4 bit as shown in Table 18. To save power with the dividers running, the buffer can be turned off by setting the bits MC4[1:0] to 2. See Figure 10 for circuit details and the Applications Information section for common interface configurations.

Table 18. Output Sense with MUTEx = 1 and OINVx Programming (x = 0 to 4)

OINVx	OUTx+	OUTx–
0	0	1
1	1	0

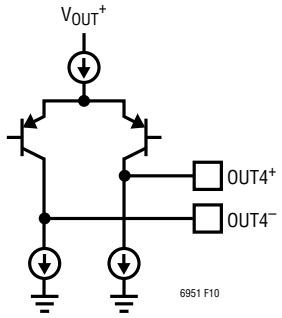


Figure 10. Simplified LVDS Interface Schematic (OUT4)

OUTPUT SYNCHRONIZATION (SYNC)

The LTC6951 has circuitry to allow the outputs to be synchronized into known phase alignment in several different ways to suit different applications using the EZSync and ParallelSync Multichip Clock Edge Synchronization protocols. Synchronization can be between any combination of outputs on the same chip (EZSync Standalone), across multiple cascaded follower chips (EZSync Multi-chip), or even across multiple parallel chips on the same reference domain (ParallelSync). Outputs can also be aligned to the REF input using the Reference Aligned Output mode (RAO = 1). Examples of EZSync standalone, EZSync multichip, and ParallelSync synchronization are shown in the

OPERATION

Applications Information section. The LTC6951Wizard Software Design Tool also provides graphical examples of these synchronization methods. For more information about the EZSync and ParallelSync Protocols, see the LTC6951 Synchronization Guide or contact the factory.

At initial power-up, after a POR, or any time output dividers M0, M1, M2, M3 or M4 are changed, the outputs will not be synchronized. Any changes to the output delays D0, D1, D2, D3 and D4 will not be reflected until after synchronization. Although the part will run properly and the outputs will be at the proper frequency without synchronization, it is highly recommended to use some form of synchronization. See Table 19 for descriptions of the applicable serial port bits and the Applications Information section for specific programming examples.

Table 19. SYNC Bit Descriptions

BIT	DESCRIPTION
DLY0[7:0]	D0 delay setting for the M0 divider (RAO = 0).
DLY1[7:0]	D1 delay setting for the M1 divider.
DLY2[7:0]	D2 delay setting for the M2 divider.
DLY3[7:0]	D3 delay setting for the M3 divider.
DLY4[7:0]	D4 delay setting for the M4 divider.
RAO	Reference alignment mode.
SN	SYNC pin falling edge time alignment to REF (RAO = 1); SSYNC ignored.
SR	SYNC pin rising edge time alignment of R divider to REF (RAO = 1); SSYNC ignored.
SSYNC	Software synchronization.
SYNCEN0	Enable synchronization of the M0 divider (RAO = 0).
SYNCEN1	Enable synchronization of the M1 divider.
SYNCEN2	Enable synchronization of the M2 divider.
SYNCEN3	Enable synchronization of the M3 divider.
SYNCEN4	Enable synchronization of the M4 divider.

Reference Aligned Output Mode (RAO)

The RAO bit (register h03) controls the fundamental configuration of the PLL and the ability to align the outputs back to the Reference input. Figure 3 shows the PLL loop diagram with bit RAO set to “0” which is the default power-up.

Figure 4 shows the PLL loop diagram with bit RAO set to “1”. The P and M0 dividers are now part of the overall feedback loop, and the range on the N divider has changed. SYNCEN0 has no effect on OUT0. DLY0[7:0] in register h0A is now inactive and the contents of h0A[7] and h0A[6] become SN and SR, respectively. See Table 5 for SN and SR function descriptions.

The N divider output is used as a timing event for all synchronization modes. Only when the P and M0 dividers are in the feedback loop can the output rising edges be coincident with the N divider output, and by inference the R divider output, creating a known and repeatable alignment between the outputs and the Reference input.

Synchronization Events

Synchronization begins either with the SYNC pin driven high or by writing “1” to the SSYNC bit (unless RAO = 1 and SR or SN = 1, in which case the SSYNC bit is inactive). Internal to the LTC6951, the SYNC pin’s signal and the SSYNC bit are logically ORed. Choose either the SYNC pin or the SSYNC bit for use during a synchronization event and keep the unused signal held at logic low. Any output with a valid SYNCENx bit set will stop running and return to a logic “0” state after an internal timing delay of greater than 100µs. The SYNC pin or SSYNC bit must remain high for a minimum of 1ms.

When bits RAO and SR are set to “1” and the SYNC pin is driven high, the R divider for R ≥ 2 is retimed as shown in Figure 5 and explained in the Reference Divider (R) section.

When the SYNC pin is driven back low, or “0” is written to the SSYNC bit in cases when it is active, internal retiming begins immediately to allow synchronized outputs to start again. One N divider cycle and then 18 P divider cycles are required to synchronize each output divider. A Dx delay setting of “0” causes that output to start immediately after the 18 P divider cycles. All synchronized outputs with the same Dx delay setting will have the output rising edge occur within the skew times as defined in the Electrical Characteristics table. The range on each delay is 0 to 255 P cycles and is independent of the Mx divide ratio setting of each divider.

OPERATION

The internal synchronization signal is controlled by the settings of RAO and SN. If either bit is "0" the internal synchronization falling edge is delayed by at least 25µs to meet the requirements of EZSync.

RAO = SN = 1, R = 1

When bits RAO and SN are "1", the value of R = 1 and the SYNC pin driven synchronously to the REF inputs, the output timing is as shown in Figure 11.

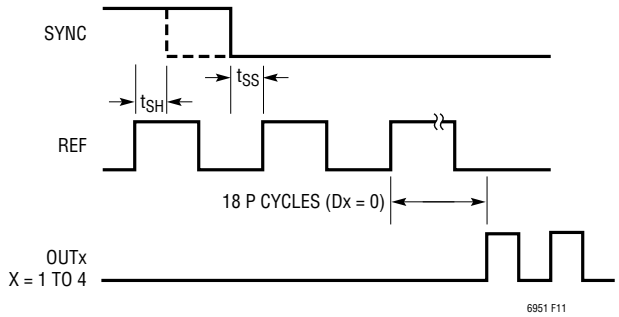


Figure 11. SYNC to REF timing (RAO = SN = 1, R = 1)

RAO = SN = SR = 1, R ≥ 2

When R ≥ 2 bits RAO, SN and SR are "1" and the SYNC pin is driven synchronously to the REF inputs, the output timing is as shown in Figure 12. Note the outputs are now retimed to the R divider output (R DIV) which is an internal node not accessible outside of the part. The SYNC timing must still meet setup (t_{SS}) and hold (t_{SH}) timing to REF. Combining Figure 12 with Figure 5 allows the ability to calculate the width of the SYNC pulse in terms of REF periods (REFCYCLES) to get precise timing back to R DIV with R ≥ 2, noting that the SYNC pulse needs to be high a minimum of 1ms.

$$REFCYCLES = R \bullet CEILING\left(\frac{1ms \bullet f_{REF}}{R}\right) + 1 \qquad (2)$$

where the CEILING(x) function returns the smallest integer greater than or equal to x.

Using Equation 2 to calculate the width of the SYNC pulse in terms of REFCYCLES is not required to get the outputs properly synchronized to each other or across multiple LTC6951s. However, the latency from REF to any output has R different possibilities depending on where SYNC falls relative to R DIV.

If the controlling system can make the SYNC pulse exactly REFCYCLES wide, all outputs will occur with the exact same latency to REF every time synchronization occurs. Note that Equation 2 calculates the minimum number of REFCYCLES for the SYNC pulse. Adding R multiples will give the same result. See ParallelSync Multi-Chip Synchronization in the Applications Information section for an example.

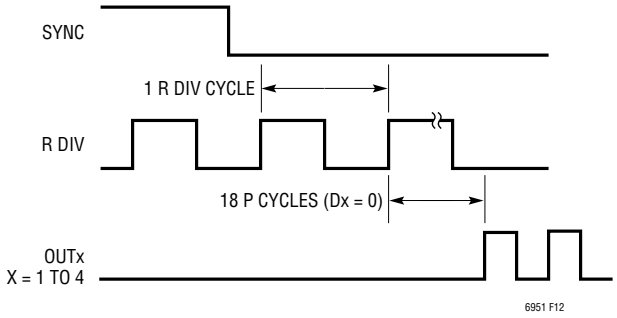


Figure 12. SYNC to R DIV timing (RAO = SN = SR = 1, R ≥ 2)

See Reference Signal and Sync Timing for SR and SN Modes in the Applications Information section for the timing requirements of SYNC to REF in this mode.