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Low Phase Noise, Triple Output Clock Distribution Divider/Driver

FEATURES

- **Low Noise Clock Distribution: Suitable for High Speed/High Resolution ADC Clocking**
- **Additive Jitter < 20fs$_{RMS}$ (12kHz to 20MHz)**
- **Additive Jitter < 85fs$_{RMS}$ (10Hz to Nyquist)**
- **1.8GHz Maximum Input Frequency (LTC6954-1 When DELAY = 0)**
- **1.4GHz Maximum Input Frequency (LTC6954-1 When DELAY > 0, LTC6954-2, -3, -4)**
- **EZSync™ Clock Synchronization Compatible**
- **Three Independent, Low Noise Outputs**
- **Four Output Combinations Available**
- Three Independent Programmable Dividers Covering All Integers From 1 to 63
- Three Independent Programmable Delays Covering All Integers From 0 to 63
- –40°C to 105°C Junction Temperature Range

APPLICATIONS

- Clocking High Speed, High Resolution ADCs, DACs and Data Acquisition Systems
- Low Jitter Clock Distribution

DESCRIPTION

The LTC®6954 is a family of very low phase noise clock distribution parts. Each part has three outputs and each output has an individually programmable frequency divider and delay. There are four members of the family, differing in their output logic signal type:

LTC6954-1: Three LVPECL outputs

LTC6954-2: Two LVPECL and one LVDS/CMOS outputs

LTC6954-3: One LVPECL and two LVDS/CMOS outputs

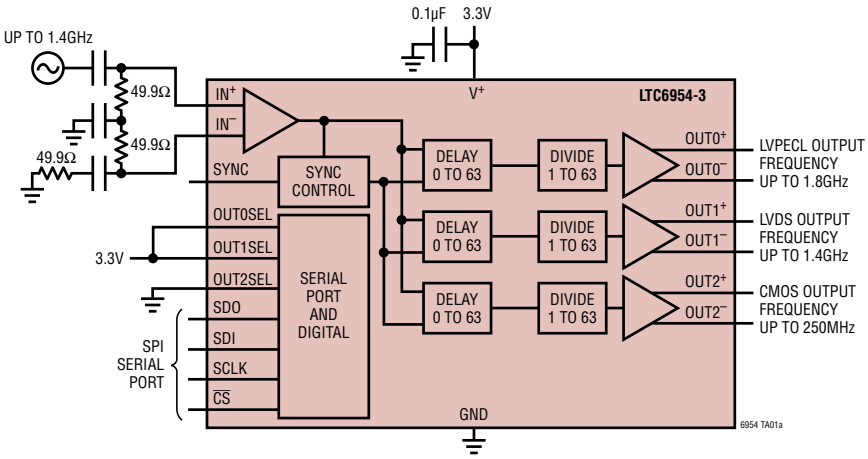
LTC6954-4: Three LVDS/CMOS outputs

Each output is individually programmable to divide the input frequency by any integer from 1 to 63, and to delay each output by 0 to 63 input clock cycles. The output duty cycle is always 50%, regardless of the divide number. The LVDS/CMOS outputs are jumper selectable via the OUTxSEL pins to provide either an LVDS logic output or a CMOS logic output.

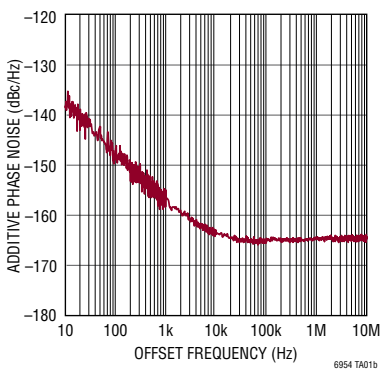
The LTC6954 also features Linear Technology's EZSync system for perfect clock synchronization and alignment every time.

All device settings are controlled through an SPI-compatible serial port.

TYPICAL APPLICATION



Additive Phase Noise vs Offset Frequency, f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUTx} = 155.52MHz

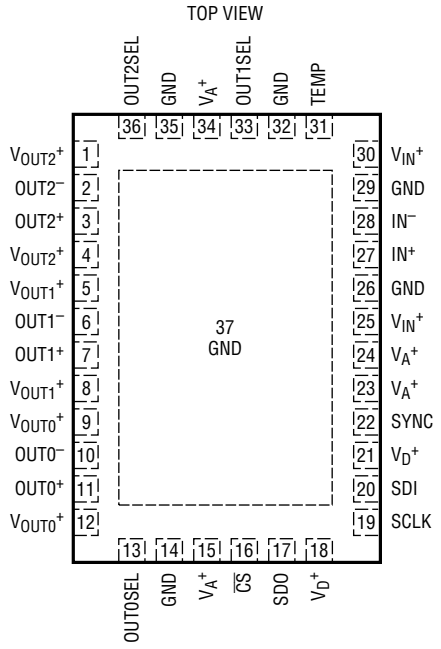


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
(V_A^+, V_D^+, V_{IN}^+, V_{OUT0}^+, V_{OUT1}^+ and
V_{OUT2}^+ to GND) 3.6V
LTC6954-1, -2, -3 LVPECL Outputs
  OUTx Output Voltage High ..... V_{OUT}^+ + 0.3V
  OUTx Output Voltage Low ..... Source 25mA
LTC6954-2, -3, -4 LVDS/CMOS Outputs
  OUTx ..... –0.3V to (V_A^+ +0.3V)
TEMP Input Current 10mA
TEMP Low Voltage ..... –0.3V
Voltage on All Other Pins ..... –0.3V to (V_A^+ + 0.3V)
Operating Junction Temperature Range, T_J (Note 2)
LTC6954I ..... –40°C to 105°C
Junction Temperature, T_{JMAX} ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFF PACKAGE
36-LEAD (4mm × 7mm) PLASTIC QFN
0.5mm LEAD PITCH

T_{JMAX} = 150°C, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 18°C/W
EXPOSED PAD (PIN 37) IS GND, MUST BE SOLDERED TO PCB GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC6954IUFF-1#PBF	LTC6954IUFF-1#TRPBF	69541	36-Lead (4mm × 7mm) Plastic QFN	–40°C to 105°C
LTC6954IUFF-2#PBF	LTC6954IUFF-2#TRPBF	69542	36-Lead (4mm × 7mm) Plastic QFN	–40°C to 105°C
LTC6954IUFF-3#PBF	LTC6954IUFF-3#TRPBF	69543	36-Lead (4mm × 7mm) Plastic QFN	–40°C to 105°C
LTC6954IUFF-4#PBF	LTC6954IUFF-4#TRPBF	69544	36-Lead (4mm × 7mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part markings, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+$ = 3.3V, unless otherwise specified. All voltages are with respect to GND. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input (IN⁺, IN⁻)							
f_{IN}	Input Frequency	LTC6954-1, DELx = 0 LTC6954-1 (DELx > 0), LTC6954-2, -3, -4	● ●			1800 1400	MHz MHz
V_{IN}	Input Signal Level	Single-Ended	●	0.2	0.8	1.5	V_{P-P}
	Input Slew Rate		●	100			V/µs
DC_{IN}	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.9	2.05	2.2	V
	Minimum Common Mode Level	400mV_{P-P} Differential Input			1.8		V
	Maximum Common Mode Level	400mV_{P-P} Differential Input			2.3		V
	Input Resistance	Differential	●	1.8	2.2	2.7	kΩ
	Input Capacitance	Differential			0.5		pF
Output Divider (M)							
Mx[5:0]	Divider Range M0[5:0], M1[5:0], M2[5:0]	All Integers Included	●	1		63	Cycles
DELx[5:0]	Divider Delay in Input Clock Cycles DEL0[5:0], DEL1[5:0], DEL2[5:0]	All Integers Included	●	0		63	Cycles
LVPECL Clock Outputs							
f_{OUT}	Frequency	LTC6954-1, DELx = 0 LTC6954-1 (DELx > 0), LTC6954-2, -3, -4	● ●			1800 1400	MHz MHz
$\|V_{OD}\|$	Differential Voltage (Output Static)	Single-Ended Termination = 50Ω to (V_{OUTx}^+ – 2V)	●	640	775	950	mV_{PK}
		Differential Termination = 100Ω, Internal Bias On	●	640	780	950	mV_{PK}
V_{CM}	Common Mode Voltage (Output Static)	Single-Ended Termination = 50Ω to (V_{OUTx}^+ – 2V)	●	V_{OUTx}^+ – 1.67	V_{OUTx}^+ – 1.42	V_{OUTx}^+ – 1.14	V
		Differential Termination = 100Ω, Internal Bias On	●	V_{OUTx}^+ – 1.67	V_{OUTx}^+ – 1.42	V_{OUTx}^+ – 1.14	V
t_{RISE}	Rise Time, 20% to 80%	Single-Ended Termination = 50Ω to (V_{OUTx}^+ – 2V)			110		ps
		Differential Termination = 100Ω, Internal Bias On			110		ps
t_{FALL}	Fall Time, 80% to 20%	Single-Ended Termination = 50Ω to (V_{OUTx}^+ – 2V)			110		ps
		Differential Termination = 100Ω, Internal Bias On			110		ps
DC_{LVPECL}	Duty Cycle	Mx[5:0] = 1			DC_{IN}		%
		Mx[5:0] > 1 (Even or Odd)	●	45	50	55	%
CMOS Clock Outputs							
f_{OUT}	Frequency		●			250	MHz
V_{OH}	High Voltage (Output Static)	2.5mA Load	●	V^+ – 0.4			V
V_{OL}	Low Voltage (Output Static)	2.5mA Load	●			0.4	V
t_{RISE}	Rise Time, 20% to 80%	C_{LOAD} = 2pF, CMSINV = 1			200		ps
t_{FALL}	Fall Time, 80% to 20%	C_{LOAD} = 2pF, CMSINV = 1			170		ps
DC_{CMOS}	Duty Cycle	Mx[5:0] = 1			DC_{IN}		%
		Mx[5:0] > 1 (Even or Odd)	●	45	50	55	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+$ = 3.3V, unless otherwise specified. All voltages are with respect to GND. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Clock Outputs							
f_{OUT}	Frequency	Differential Termination = 100Ω, 3.5mA Mode	●			800	MHz
		Differential Termination = 50Ω, 7mA Mode	●			1400	MHz
$\|V_{OD}\|$	Differential Voltage (Output Static)	Differential Termination = 100Ω, 3.5mA Mode	●	290	370	450	mV_{PK}
		Differential Termination = 50Ω, 7mA Mode	●	290	370	450	mV_{PK}
$\|\Delta V_{OD}\|$	Delta V_{OD} (Output Static)	Differential Termination = 100Ω, 3.5mA Mode	●	–30		30	mV
		Differential Termination = 50Ω, 7mA Mode	●	–30		30	mV
V_{OS}	Offset Voltage (Output Static)	Differential Termination = 100Ω, 3.5mA Mode	●	1.16	1.23	1.32	V
		Differential Termination = 50Ω, 7mA Mode	●	1.15	1.23	1.32	V
$\|\Delta V_{OS}\|$	Delta V_{OS} (Output Static)	Differential Termination = 100Ω, 3.5mA Mode	●	–15		15	mV
		Differential Termination = 50Ω, 7mA Mode	●	–15		15	mV
t_{RISE}	Rise Time, 20% to 80%	Differential Termination = 100Ω, 3.5mA Mode			240		ps
		Differential Termination = 50Ω, 7mA Mode			120		ps
t_{FALL}	Fall Time, 80% to 20%	Differential Termination = 100Ω, 3.5mA Mode			240		ps
		Differential Termination = 50Ω, 7mA Mode			120		ps
$\|I_{SA}\|$, $\|I_{SB}\|$	Short-Circuit Current to Common	Shorted to GND, 3.5mA Mode			16		mA
		Shorted to GND, 7mA Mode			25		mA
$\|I_{SAB}\|$	Short-Circuit Current to Complementary	3.5mA Mode			4		mA
		7mA Mode			8		mA
DC_{LVDS}	Duty Cycle	Mx[5:0] = 1			DC_{IN}		%
		Mx[5:0] > 1 (Even or Odd)	●	45	50	55	%
Output Propagation Delays							
$t_{PD(LVPECL)}$	Propagation Delay From IN to Any LVPECL Output	Mx[5:0] = 1	●	290	360	480	ps
		Mx[5:0] > 1	●	360	430	550	ps
	Temperature Variation of the Propagation Delay From IN to Any LVPECL Output	Mx[5:0] = 1	●		0.65		ps/°C
		Mx[5:0] > 1	●		0.68		ps/°C
$t_{pd(LVDS)}$	Propagation Delay From IN to Any LVDS Output, LVCSx = 1 (7mA Mode)	Mx[5:0] = 1	●	350	420	545	ps
		Mx[5:0] > 1	●	415	480	625	ps
	Temperature Variation of the Propagation Delay From IN to Any LVDS Output, LVCSx = 1 (7mA Mode)	Mx[5:0] = 1	●		0.8		ps/°C
		Mx[5:0] > 1	●		0.85		ps/°C
	Propagation Delay From IN to Any LVDS Output, LVCSx = 0 (3.5mA Mode)	Mx[5:0] = 1			480		ps
		Mx[5:0] > 1			550		ps
	Temperature Variation of the Propagation Delay From IN to Any LVDS Output, LVCSx = 0 (3.5mA Mode)	Mx[5:0] = 1	●		0.8		ps/°C
		Mx[5:0] > 1	●		0.85		ps/°C
$t_{pd(CMOS)}$	Propagation Delay From IN to Any CMOS Output, Complementary Outputs (CMSINVx = 1)	Mx[5:0] = 1			1.25		ns
		Mx[5:0] > 1			1.32		ns
	Temperature Variation of the Propagation Delay From IN to Any CMOS Output (CMSINVx = 1)	Mx[5:0] = 1	●		1.3		ps/°C
		Mx[5:0] > 1	●		1.4		ps/°C

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Skews							
t_{SKEW}	Skew: Any LVPECL Output to Any LVPECL Output	Mx[5:0], My[5:0] Both = 1 or Both > 1 IBIASx = 0 or 1	●	–50		50	ps
	Skew: Any LVPECL Output to Any LVDS Output	M_{LVPECL}[5:0], M_{LVDS}[5:0] Both = 1 or Both > 1 IBIASx = 0 or 1, LVCSy = 1			65		ps
	Skew: Any LVPECL Output to Any LVDS Output	M_{LVPECL}[5:0] = M_{LVDS}[5:0] = 1 or Both > 1 IBIASx = 0 or 1, LVCSx = 0			120		ps
	Skew: Any LVPECL Output to Any CMOS Output	M_{LVPECL}[5:0], M_{CMOS}[5:0] Both = 1 or Both > 1 IBIASx = 0 or 1, CMSINVy = 1			875		ps
	Skew: Any LVDS Output to Any LVDS Output	Mx[5:0], My[5:0] Both = 1 or Both > 1 LVCSx = 1 for Both Outputs	●	–50		50	ps
	Skew: Any LVDS Output to Any LVDS Output	Mx[5:0], My[5:0] Both = 1 or Both > 1 LVCSx = 0 for Both Outputs			5		ps
	Skew: Any LVDS Output (LVCSx = 1) to Any LVDS Output (LVCSy = 0)	Mx[5:0], My[5:0] Both = 1 or Both > 1 LVCSx = 1, LVCSy = 0			50		ps
	Skew: Any LVDS Output to Any CMOS Output	M_{LVDS}[5:0], M_{CMOS}[5:0] Both = 1 or Both > 1 LVCSx = 1, CMSINV = 1			800		ps
	Skew: Any CMOS Output to Any CMOS Output	Mx[5:0], My[5:0] Both = 1 or Both > 1 CMSINV = 1			5		ps
	Skew: Any CMOS Output to Any CMOS Output, the First Output is Complementary, the Second Output is In-Phase	CMSINVx = 1, CMSINVy = 0			30		ps
	Additional Skew: Any Output to Any Output, Dividers Not the Same	Mx[5:0] = 1, My[5:0] > 1	●	35	70	120	ps

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltages							
	V_A^+ Supply Range		●	3.15	3.3	3.45	V
	V_D^+ Supply Range		●	3.15	3.3	3.45	V
	V_{IN}^+ Supply Range		●	3.15	3.3	3.45	V
	V_{OUT0}^+, V_{OUT1}^+, V_{OUT2}^+ Supply Range		●	3.15	3.3	3.45	V
Supply Current (Sum of V_A^+, V_D^+, V_{IN}^+, V_{OUT0}^+, V_{OUT1}^+, V_{OUT2}^+ Supply Currents)							
	LTC6954-1	f_{IN} = 1400MHz, Power-Up Default Configuration, OUT0SEL = OUT1SEL = OUT2SEL = V_A^+, IBIAS On for All Outputs, Outputs Terminated with 100Ω Differential	●		300	335	mA
		f_{IN} = 1400MHz, Power-Up Default Configuration, OUT0SEL = OUT1SEL = OUT2SEL = GND, IBIAS Off for All Outputs, Outputs Terminated with 50Ω to (V_{OUTx}^+ – 2V)	●		310	350	mA
	LTC6954-2	f_{IN} = 1400MHz, Power-Up Default Configuration, OUT0SEL = OUT1SEL = OUT2SEL = V_A^+, IBIAS On for LVPECL Outputs, LVDS/CMOS = LVDS, Outputs Terminated with 100Ω Differential	●		290	325	mA
		f_{IN} = 1400MHz, Power-Up Default Configuration, OUT0SEL = OUT1SEL = V_A^+, OUT2SEL = GND, IBIAS On for LVPECL Outputs, LVDS/CMOS = CMOS, M2[5:0] = 28, f_{OUT2} = 50MHz, LVPECL Outputs Terminated with 100Ω Differential	●		280	320	mA
	LTC6954-3	f_{IN} = 1400MHz, Power-Up Default Configuration, OUT0SEL = OUT1SEL = OUT2SEL = V_A^+, IBIAS On for LVPECL Output, LVDS/CMOS = LVDS, Outputs Terminated with 100Ω Differential	●		280	320	mA
		f_{IN} = 1400MHz, Power-Up Default Configuration, OUT0SEL = V_A^+, OUT1SEL = OUT2SEL = GND, IBIAS On for LVPECL Output, LVDS/CMOS = CMOS, M1[5:0] = M2[5:0] = 28, f_{OUT1} = f_{OUT2} = 50MHz, LVPECL Output Terminated with 100Ω Differential	●		278	315	mA
	LTC6954-4	f_{IN} = 1400MHz, Power-Up Default Configuration, OUT0SEL = OUT1SEL = OUT2SEL = V_A^+, LVDS/CMOS = LVDS, Outputs Terminated with 100Ω Differential	●		270	315	
		f_{IN} = 1400MHz, Power-Up Default Configuration, OUT0SEL = OUT1SEL = OUT2SEL = GND, LVDS/CMOS = CMOS, M0[5:0], M1[5:0] = M2[5:0] = 28, f_{OUT0} = f_{OUT1} = f_{OUT2} = 50MHz	●		282	310	mA
	ALL LTC6954 Variants	$P_{D(ALL)}$ = 1			0.8		mA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current Delta (Note 3)							
	Output Divider On, LVPECL Output	PD_DIVx = 0, Mx[5:0] = 1, PD_OUTx = 1	●		28	32	mA
		PD_DIVx = 0, Mx[5:0] > 1, PD_OUTx = 1	●		46	54	mA
	Output Driver Only, LVPECL	PD_OUTx = 0, Termination = 50Ω to (V_{OUTx}^+ – 2V)	●		43	50	mA
		PD_OUTx = 0, IBIASx = 1 (Internal Bias On)	●		39	46	mA
		PD_OUTx = 0, No Internal/External Bias	●		19	24	mA
	Output Driver Only, LVDS	PD_OUTx = 0, 3.5mA Mode, LVCSx = 0	●		31	37	mA
		PD_OUTx = 0, 7mA Mode, LVCSx = 1	●		48	58	mA
	Output Driver Only, CMOS	PD_OUTx = 0, CMOS at 50MHz	●		35	43	mA
Digital Inputs ($\overline{CS}$, SDI, SCLK, SYNC, OUT0SEL, OUT1SEL, OUT2SEL)							
V_{IH}	Input High Voltage		●	1.55			V
V_{IL}	Input Low Voltage		●			0.8	V
V_{IHYS}	Input Voltage Hysteresis	CS, SDI and SCLK Only			250		mV
	Input Current		●	–1		1	µA
Digital Outputs (SDO)							
I_{OH}	High Level Output Current	SDO, $V_{OH} = V_D^+$ – 400mV	●		–2.4	–1.5	mA
I_{OL}	Low Level Output Current	SDO, V_{OL} = 400mV	●	2.2	3.4		mA
	SDO Hi-Z Current		●	–1		1	µA
Digital Timing Specifications (See Figure 11 and Figure 12)							
t_{CKH}	SCLK HIGH Pulse Width		●	25			ns
t_{CKL}	SCLK LOW Pulse Width		●	25			ns
t_{CSS}	$\overline{CS}$ Setup Time		●	10			ns
t_{CSH}	$\overline{CS}$ HIGH Pulse Width		●	10			ns
t_{CS}	SDI to SCLK Setup Time		●	6			ns
t_{CH}	SDI to SCLK Hold Time		●	6			ns
t_{DO}	SDO Propagation Delay	C_{LOAD} = 10pF			16		ns
t_{SYNCH}	SYNC HIGH Pulse Width		●	1			ms
t_{SYNCL}	Minimum SYNC LOW Pulse Width	Before Next SYNC HIGH Pulse			1		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+$ = 3.3V, unless otherwise specified. All voltages are with respect to GND. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVPECL Additive Phase Noise/Time Jitter (Note 5)							
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 1, f_{OUT} = 622.08MHz	10Hz Offset			–130		dBc/Hz
		100Hz Offset			–139		dBc/Hz
		1kHz Offset			–148		dBc/Hz
		10kHz Offset			–156		dBc/Hz
		100kHz Offset			–158		dBc/Hz
		>1MHz Offset			–158		dBc/Hz
	Jitter: f_{IN} = 622.08MHz, Mx[5:0] = 1, f_{OUT} = 622.08MHz	12kHz to 20MHz Integration Bandwidth			20		fs_{RMS}
		10Hz to 311.04MHz Integration Bandwidth			80		fs_{RMS}
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUT} = 155.52MHz	10Hz Offset			–138		dBc/Hz
		100Hz Offset			–147		dBc/Hz
		1kHz Offset			–156		dBc/Hz
		10kHz Offset			–163		dBc/Hz
		100kHz Offset			–165		dBc/Hz
		>1MHz Offset			–165		dBc/Hz
	Jitter: f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUT} = 155.52MHz	12kHz to 20MHz Integration Bandwidth			36		fs_{RMS}
		10Hz to 77.75MHz Integration Bandwidth			72		fs_{RMS}
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 16, f_{OUT} = 38.88MHz	10Hz Offset			–147		dBc/Hz
		100Hz Offset			–159		dBc/Hz
		1kHz Offset			–167		dBc/Hz
		10kHz Offset			–170		dBc/Hz
		100kHz Offset			–171		dBc/Hz
		>1MHz Offset			–171		dBc/Hz
	Phase Noise: f_{IN} = 245.76MHz, Mx[5:0] = 1, f_{OUT} = 245.76MHz	10Hz Offset			–137		dBc/Hz
		100Hz Offset			–147		dBc/Hz
		1kHz Offset			–156		dBc/Hz
		10kHz Offset			–161		dBc/Hz
		100kHz Offset			–162		dBc/Hz
		>1MHz Offset			–162		dBc/Hz
	Jitter: f_{IN} = 245.76MHz, Mx[5:0] = 1, f_{OUT} = 245.76MHz	12kHz to 20MHz Integration Bandwidth			33		fs_{RMS}
		10Hz to 122.88MHz Integration Bandwidth			81		fs_{RMS}
	Phase Noise: f_{IN} = 245.76MHz, Mx[5:0] = 4, f_{OUT} = 61.44MHz	10Hz Offset			–140		dBc/Hz
		100Hz Offset			–153		dBc/Hz
		1kHz Offset			–161		dBc/Hz
		10kHz Offset			–166		dBc/Hz
		100kHz Offset			–168		dBc/Hz
		>1MHz Offset			–168		dBc/Hz
	Jitter: f_{IN} = 245.76MHz, Mx[5:0] = 4, f_{OUT} = 61.44MHz	12kHz to 20MHz Integration Bandwidth			65		fs_{RMS}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+$ = 3.3V, unless otherwise specified. All voltages are with respect to GND. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVPECL Additive Phase Noise/Time Jitter (Note 5)							
	Phase Noise: f_{IN} = 1400MHz, Mx[5:0] = 1, f_{OUT} = 1400MHz	10Hz Offset			–126		dBc/Hz
		100Hz Offset			–132		dBc/Hz
		1kHz Offset			–143		dBc/Hz
		10kHz Offset			–149		dBc/Hz
		100kHz Offset			–152.5		dBc/Hz
		>1MHz Offset			–152.5		dBc/Hz
	Jitter: f_{IN} = 1400MHz, Mx[5:0] = 1, f_{OUT} = 1400MHz	12kHz to 20MHz Integration Bandwidth			17		fs_{RMS}
		10Hz to 700MHz Integration Bandwidth			100		fs_{RMS}
	Phase Noise: f_{IN} = 1400MHz, Mx[5:0] = 4, f_{OUT} = 350MHz	10Hz Offset			–132		dBc/Hz
		100Hz Offset			–139		dBc/Hz
		1kHz Offset			–151		dBc/Hz
		10kHz Offset			–157		dBc/Hz
		100kHz Offset			–160		dBc/Hz
		>1MHz Offset			–160		dBc/Hz
	Jitter: f_{IN} = 1400MHz, Mx[5:0] = 4, f_{OUT} = 350MHz	12kHz to 20MHz Integration Bandwidth			29		fs_{RMS}
		10Hz to 175MHz Integration Bandwidth			85		fs_{RMS}
LVDS Additive Phase Noise/Time Jitter LVCS = 1 (Note 5)							
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 1, f_{OUT} = 622.08MHz	10Hz Offset			–130		dBc/Hz
		100Hz Offset			–138		dBc/Hz
		1kHz Offset			–148		dBc/Hz
		10kHz Offset			–156		dBc/Hz
		100kHz Offset			–157.5		dBc/Hz
		>1MHz Offset			–157.5		dBc/Hz
	Jitter: f_{IN} = 622.08MHz, Mx[5:0] = 1, f_{OUT} = 622.08MHz	12kHz to 20MHz Integration Bandwidth			21		fs_{RMS}
		10Hz to 311.04MHz Integration Bandwidth			83		fs_{RMS}
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUT} = 155.52MHz	10Hz Offset			–140		dBc/Hz
		100Hz Offset			–147		dBc/Hz
		1kHz Offset			–157		dBc/Hz
		10kHz Offset			–163		dBc/Hz
		100kHz Offset			–165		dBc/Hz
		>1MHz Offset			–165		dBc/Hz
	Jitter: f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUT} = 155.52MHz	12kHz to 20MHz Integration Bandwidth			36		fs_{RMS}
		10Hz to 77.75MHz Integration Bandwidth			72		fs_{RMS}
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 16, f_{OUT} = 38.88MHz	10Hz Offset			–147		dBc/Hz
		100Hz Offset			–159		dBc/Hz
		1kHz Offset			–166		dBc/Hz
		10kHz Offset			–170		dBc/Hz
		100kHz Offset			–170		dBc/Hz
		>1MHz Offset			–170		dBc/Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+$ = 3.3V, unless otherwise specified. All voltages are with respect to GND. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Additive Phase Noise/Time Jitter LVCS = 1 (Note 5)							
	Phase Noise: f_{IN} = 245.76MHz, Mx[5:0] = 1, f_{OUT} = 245.76MHz	10Hz Offset			–138		dBc/Hz
		100Hz Offset			–146		dBc/Hz
		1kHz Offset			–155		dBc/Hz
		10kHz Offset			–160		dBc/Hz
		100kHz Offset			–162		dBc/Hz
		>1MHz Offset			–162		dBc/Hz
	Jitter: f_{IN} = 245.76MHz, Mx[5:0] = 1, f_{OUT} = 245.76MHz	12kHz to 20MHz Integration Bandwidth			34		fs_{RMS}
		10Hz to 122.88MHz Integration Bandwidth			83		fs_{RMS}
	Phase Noise: f_{IN} = 245.76MHz, Mx[5:0] = 4, f_{OUT} = 61.44MHz	10Hz Offset			–142		dBc/Hz
		100Hz Offset			–153		dBc/Hz
		1kHz Offset			–162		dBc/Hz
		10kHz Offset			–167		dBc/Hz
		100kHz Offset			–168		dBc/Hz
		>1MHz Offset			–168		dBc/Hz
	Jitter: f_{IN} = 245.76MHz, Mx[5:0] = 4, f_{OUT} = 61.4MHz	12kHz to 20MHz Integration Bandwidth			65		fs_{RMS}
	Phase Noise: f_{IN} = 1400MHz, Mx[5:0] = 1, f_{OUT} = 1400MHz	10Hz Offset			–121		dBc/Hz
		100Hz Offset			–133		dBc/Hz
		1kHz Offset			–142		dBc/Hz
		10kHz Offset			–148		dBc/Hz
		100kHz Offset			–152		dBc/Hz
		>1MHz Offset			–152		dBc/Hz
	Jitter: f_{IN} = 1400MHz, Mx[5:0] = 1, f_{OUT} = 1400MHz	12kHz to 20MHz Integration Bandwidth			18		fs_{RMS}
		10Hz to 700MHz Integration Bandwidth			109		fs_{RMS}
	Phase Noise: f_{IN} = 1400MHz, Mx[5:0] = 4, f_{OUT} = 350MHz	10Hz Offset			–129		dBc/Hz
		100Hz Offset			–137		dBc/Hz
		1kHz Offset			–148		dBc/Hz
		10kHz Offset			–156		dBc/Hz
		100kHz Offset			–159		dBc/Hz
		>1MHz Offset			–160		dBc/Hz
	Jitter: f_{IN} = 1400MHz, Mx[5:0] = 4, f_{OUT} = 350MHz	12kHz to 20MHz Integration Bandwidth			30		fs_{RMS}
		10Hz to 175MHz Integration Bandwidth			90		fs_{RMS}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+$ = 3.3V, unless otherwise specified. All voltages are with respect to GND. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Additive Phase Noise/Time Jitter LVCS = 0 (Note 5)							
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 1, f_{OUT} = 622.08MHz	10Hz Offset			–123		dBc/Hz
		100Hz Offset			–135		dBc/Hz
		1kHz Offset			–146		dBc/Hz
		10kHz Offset			–151		dBc/Hz
		100kHz Offset			–153		dBc/Hz
		>1MHz Offset			–153		dBc/Hz
	Jitter: f_{IN} = 622.08MHz, Mx[5:0] = 1, f_{OUT} = 622.08MHz	12kHz to 20MHz Integration Bandwidth			36		fs_{RMS}
		10Hz to 311.04MHz Integration Bandwidth			140		fs_{RMS}
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUT} = 155.52MHz	10Hz Offset			–135		dBc/Hz
		100Hz Offset			–146		dBc/Hz
		1kHz Offset			–154		dBc/Hz
		10kHz Offset			–160		dBc/Hz
		100kHz Offset			–161		dBc/Hz
		>1MHz Offset			–161		dBc/Hz
	Jitter: f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUT} = 155.52MHz	12kHz to 20MHz Integration Bandwidth			29		fs_{RMS}
		10Hz to 77.75MHz Integration Bandwidth			114		fs_{RMS}
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 16, f_{OUT} = 38.88MHz	10Hz Offset			–147		dBc/Hz
		100Hz Offset			–157		dBc/Hz
		1kHz Offset			–165		dBc/Hz
		10kHz Offset			–167		dBc/Hz
		100kHz Offset			–167		dBc/Hz
		>1MHz Offset			–167		dBc/Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. $V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+$ = 3.3V, unless otherwise specified. All voltages are with respect to GND. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Additive Phase Noise/Time Jitter (Note 5)							
	Phase Noise: f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUT} = 155.52MHz	10Hz Offset			–129		dBc/Hz
		100Hz Offset			–143		dBc/Hz
		1kHz Offset			–158		dBc/Hz
		10kHz Offset			–161		dBc/Hz
		100kHz Offset			–162		dBc/Hz
		>1MHz Offset			–162		dBc/Hz
	Jitter: f_{IN} = 622.08MHz, Mx[5:0] = 4, f_{OUT} = 155.52MHz	12kHz to 20MHz Integration Bandwidth			52		fs_{RMS}
		10Hz to 77.75MHz Integration Bandwidth			102		fs_{RMS}
	Phase Noise: f_{IN} = 245.76MHz, Mx[5:0] = 1, f_{OUT} = 245.76MHz	10Hz Offset			–129		dBc/Hz
		100Hz Offset			–139		dBc/Hz
		1kHz Offset			–146		dBc/Hz
		10kHz Offset			–155		dBc/Hz
		100kHz Offset			–159		dBc/Hz
		>1MHz Offset			–160		dBc/Hz
	Jitter: f_{IN} = 245.76MHz, Mx[5:0] = 1, f_{OUT} = 245.76MHz	12kHz to 20MHz Integration Bandwidth			42		fs_{RMS}
		10Hz to 122.88MHz Integration Bandwidth			102		fs_{RMS}
	Phase Noise: f_{IN} = 245.76MHz, Mx[5:0] = 4, f_{OUT} = 61.44MHz	10Hz Offset			–135		dBc/Hz
		100Hz Offset			–147		dBc/Hz
		1kHz Offset			–156		dBc/Hz
		10kHz Offset			–163		dBc/Hz
		100kHz Offset			–166		dBc/Hz
		>1MHz Offset			–166		dBc/Hz
	Jitter: f_{IN} = 245.76MHz, Mx[5:0] = 4, f_{OUT} = 61.44MHz	12kHz to 20MHz Integration Bandwidth			82		fs_{RMS}

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6954I is guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 105°C. Under maximum operating conditions, air flow or heat sinking may be required to maintain a junction temperature of 105°C or lower. It is strongly recommended that the exposed pad (pin 37) be soldered directly to the ground plane with an array of thermal vias as described in the Applications Information section.

Note 3: The supply current delta specifications refer to the amount of supply current that each individual block consumes. Powering on or off this circuit block adds or subtracts this much current from the total supply current consumed in any given configuration.

Note 4: The skews are defined as the second listed output's transition relative to the first listed output's transition. If the second listed output transitions after the first listed output, the skew is positive.

For the same divider setting, LVPECL outputs have nominally the same skew regardless of the IBIAS setting (IBIASx = 0 or 1), for the same divider setting, all LVDS and CMOS outputs transition after the LVPECL outputs, thus these skews are positive. For the same divider setting, all CMOS outputs transition after all LVDS outputs, thus these skews are positive. For the same divider setting, LVDS outputs with the 3.5mA current setting (LVCS = 0) transition after LVDS outputs with the 7mA current setting (LVCS = 1), thus these skews are positive. For the same divider setting, in-phase CMOS outputs (CMSINVx = 0) transition after complementary outputs (CMSINVx = 1), thus this skew is positive.

For the same output type, outputs with the divider setting greater than one (Mx[5:0] > 1) transition after outputs with the divider equal to one (Mx[5:0] = 1), thus this additional skew is positive.

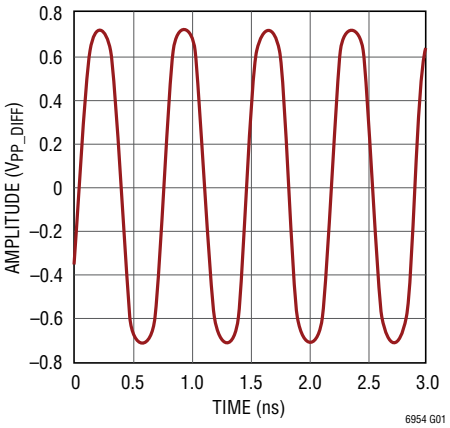
Note 5: Additive phase noise and jitter are the phase noise added by the LTC6954. It does not include noise from the external signal source.

TYPICAL PERFORMANCE CHARACTERISTICS

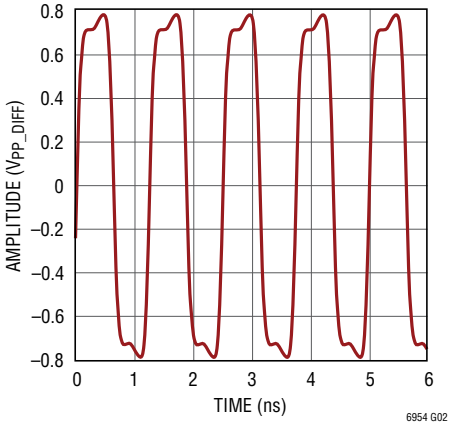
$V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+ = 3.3V$.

T_A = 25°C, unless otherwise specified. All voltages are with respect to GND.

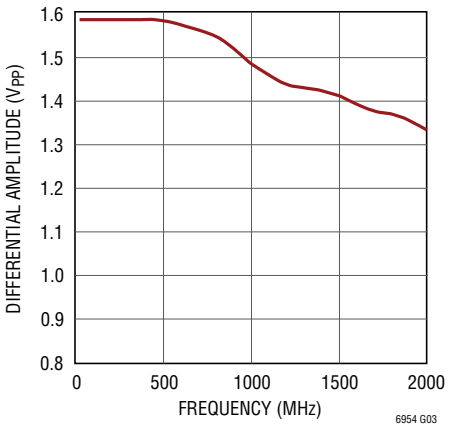
LVPECL Differential Output at 1400MHz, IBIAS Enabled, R_{TERM} = 100Ω Differential



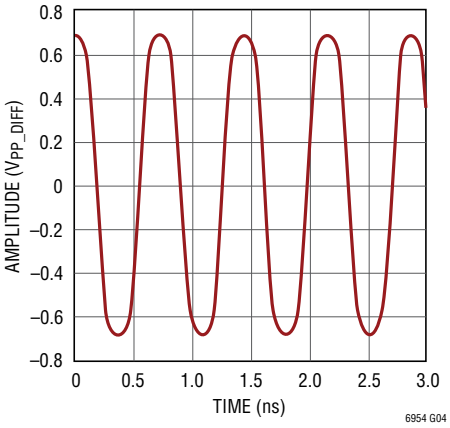
LVPECL Differential Output at 800MHz, IBIAS Enabled, R_{TERM} = 100Ω Differential



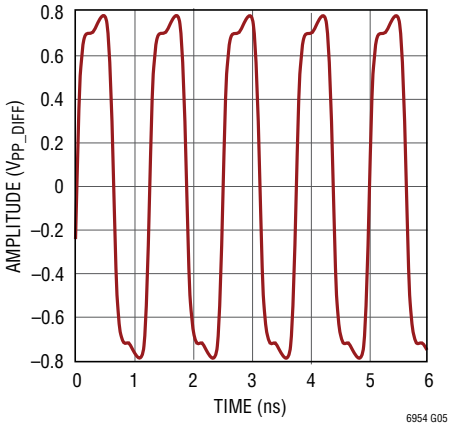
LVPECL Differential Output Swing vs Frequency, IBIAS Enabled, R_{TERM} = 100Ω Differential



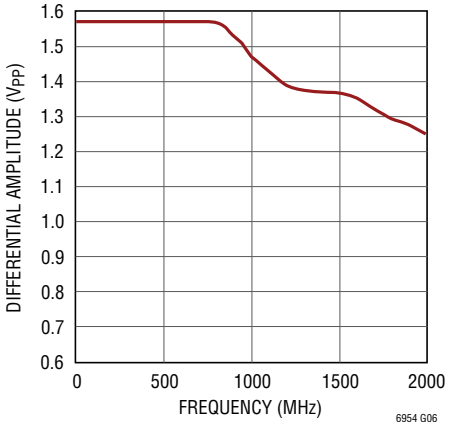
LVPECL Differential Output at 1400MHz, IBIAS Disabled, R_{TERM} = 50Ω to V^+ – 2V



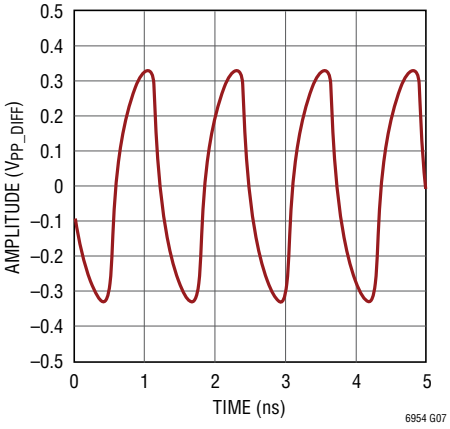
LVPECL Differential Output at 800MHz, IBIAS Disabled, R_{TERM} = 50Ω to V^+ – 2V



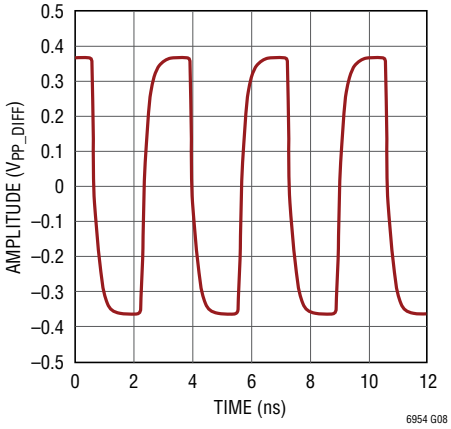
LVPECL Differential Output Swing vs Frequency, IBIAS Disabled, R_{TERM} = 50Ω to V^+ – 2V



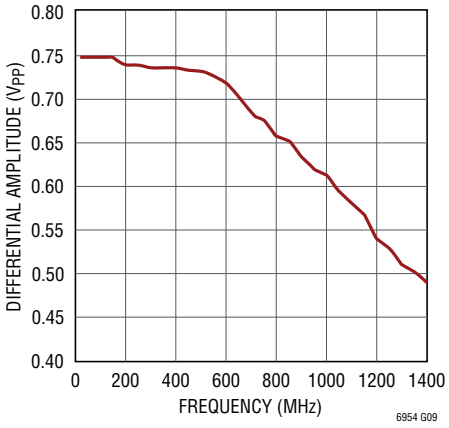
LVDS Differential Output at 800MHz, I_{LVDS} = 3.5mA, R_{TERM} = 100Ω (Differential)



LVDS Differential Output at 300MHz, I_{LVDS} = 3.5mA, R_{TERM} = 100Ω (Differential)



LVDS Differential Output Swing vs Frequency, I_{LVDS} = 3.5mA, R_{TERM} = 100Ω (Differential)

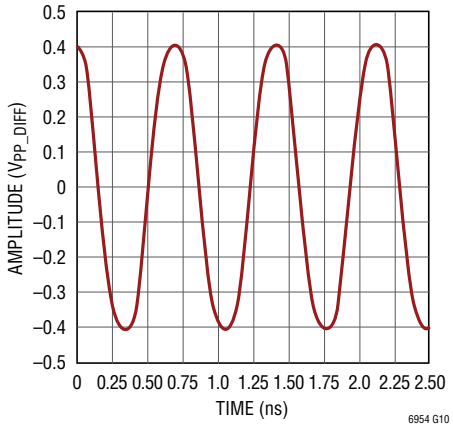


TYPICAL PERFORMANCE CHARACTERISTICS

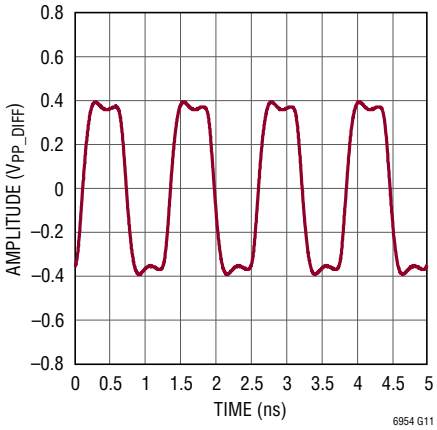
$V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+ = 3.3V$.

T_A = 25°C, unless otherwise specified. All voltages are with respect to GND.

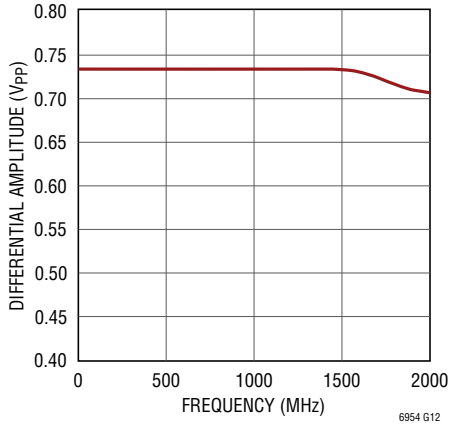
LVDS Differential Output at 1400MHz, I_{LVDS} = 7mA, R_{TERM} = 100Ω||100Ω (Differential)



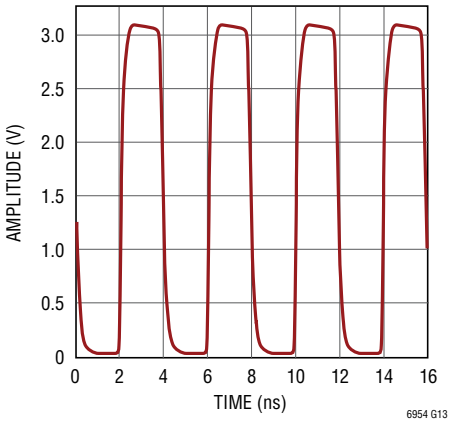
LVDS Differential Output at 800MHz, I_{LVDS} = 7mA, R_{TERM} = 100Ω||100Ω (Differential)



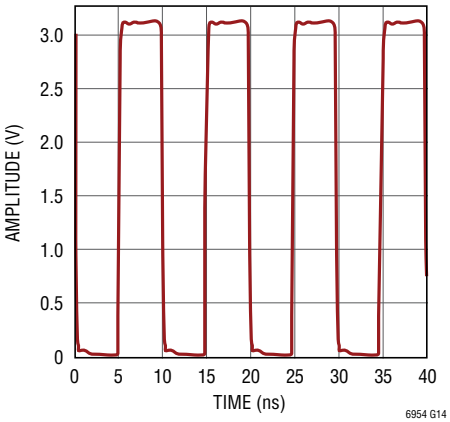
LVDS Differential Output Swing vs Frequency, I_{LVDS} = 7mA, R_{TERM} = 100Ω||100Ω (Differential)



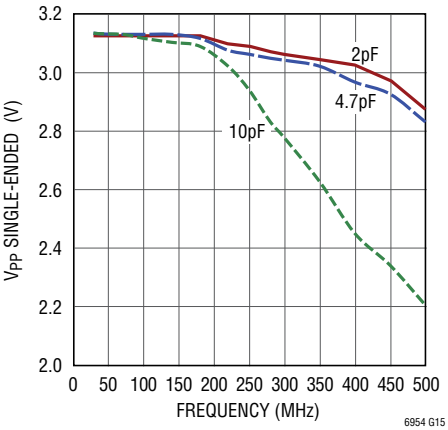
CMOS Output at 250MHz, CMSINV = 1, C_{LOAD} = 2pF



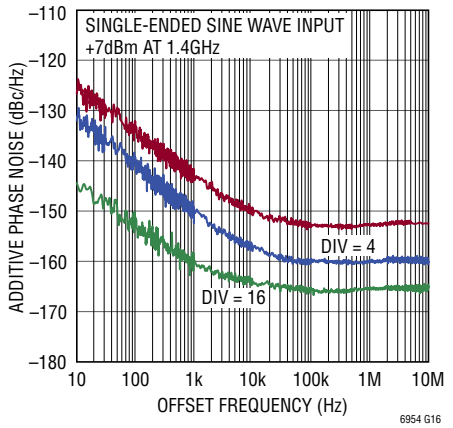
CMOS Output at 100MHz, CMSINV = 1, C_{LOAD} = 2pF



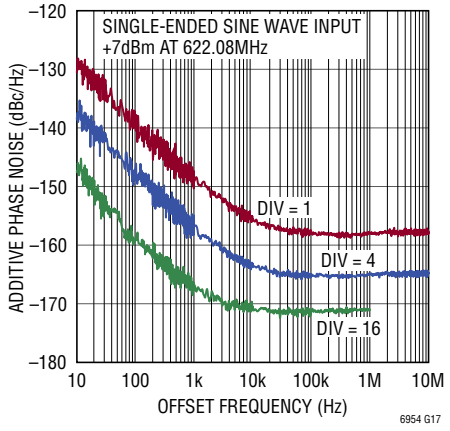
CMOS Output Swing vs Frequency and C_{LOAD}



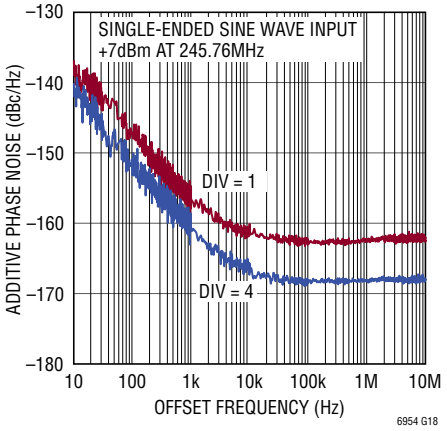
LVPECL Output Additive Phase Noise, f_{IN} = 1400MHz, IBIAS Enabled, R_{TERM} = 100Ω Differential



LVPECL Output Additive Phase Noise, f_{IN} = 622.08MHz, IBIAS Enabled, R_{TERM} = 100Ω Differential



LVPECL Output Additive Phase Noise, f_{IN} = 245.76MHz, IBIAS Enabled, R_{TERM} = 100Ω Differential

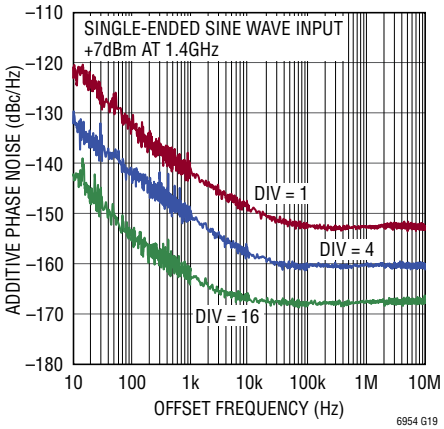


TYPICAL PERFORMANCE CHARACTERISTICS

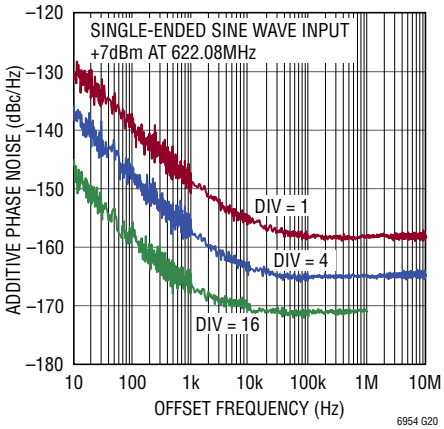
$V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+ = 3.3V$.

T_A = 25°C, unless otherwise specified. All voltages are with respect to GND.

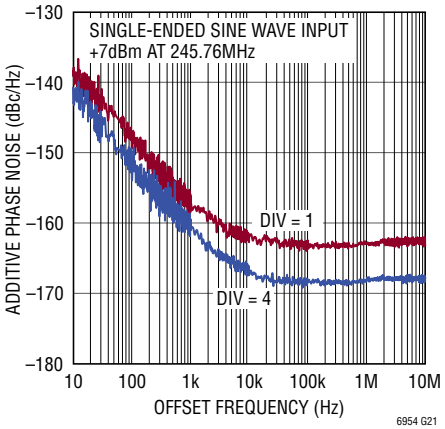
LVPECL Output Additive Phase Noise, f_{IN} = 1400MHz, IBIAS Disabled, R_{TERM} = 50Ω to V⁺ – 2V



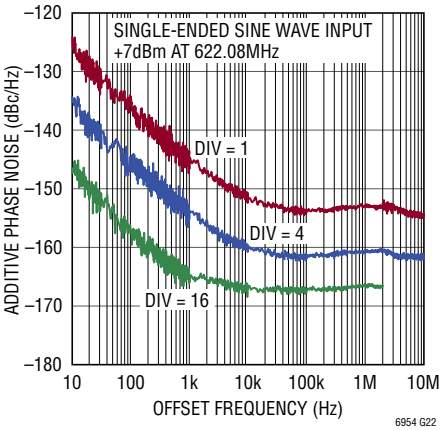
LVPECL Output Additive Phase Noise, f_{IN} = 622.08MHz, IBIAS Disabled, R_{TERM} = 50Ω to V⁺ – 2V



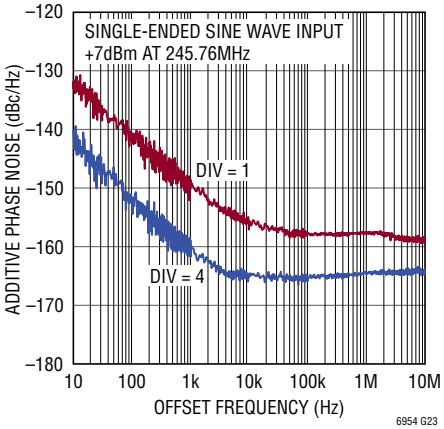
LVPECL Output Additive Phase Noise, f_{IN} = 245.76MHz, IBIAS Disabled, R_{TERM} = 50Ω to V⁺ – 2V



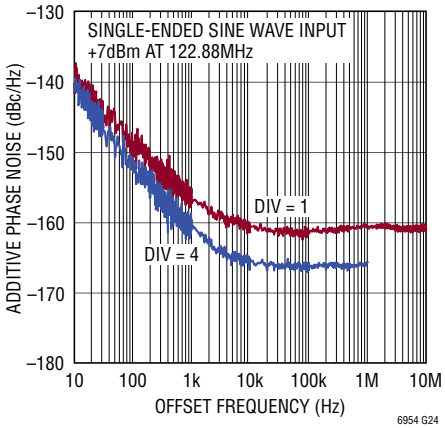
LVDS Output Additive Phase Noise, f_{IN} = 622.08MHz, I_{LVDS} = 3.5mA, R_{TERM} = 100Ω Differential



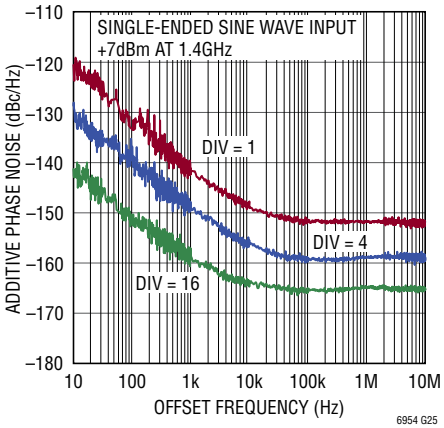
LVDS Output Additive Phase Noise, f_{IN} = 245.76MHz, I_{LVDS} = 3.5mA, R_{TERM} = 100Ω Differential



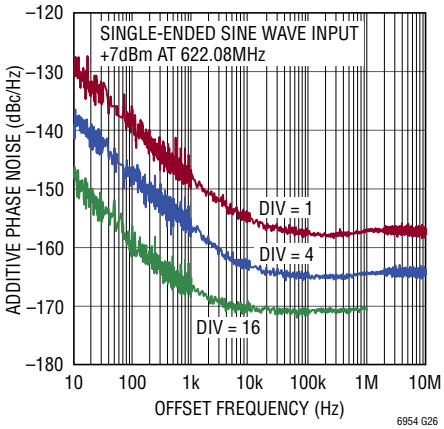
LVDS Output Additive Phase Noise, f_{IN} = 122.88MHz, I_{LVDS} = 3.5mA, R_{TERM} = 100Ω Differential



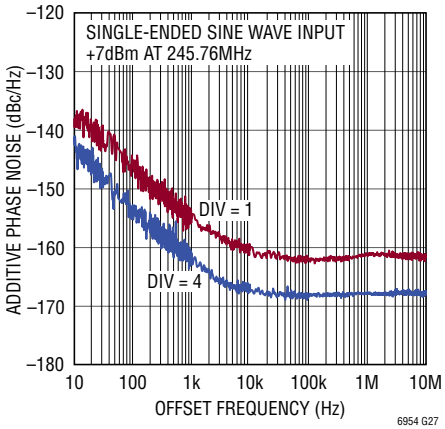
LVDS Output Additive Phase Noise, f_{IN} = 1400MHz, I_{LVDS} = 7mA, R_{TERM} = 100Ω||100Ω (Differential)



LVDS Output Additive Phase Noise, f_{IN} = 622.08MHz, I_{LVDS} = 7mA, R_{TERM} = 100Ω||100Ω (Differential)



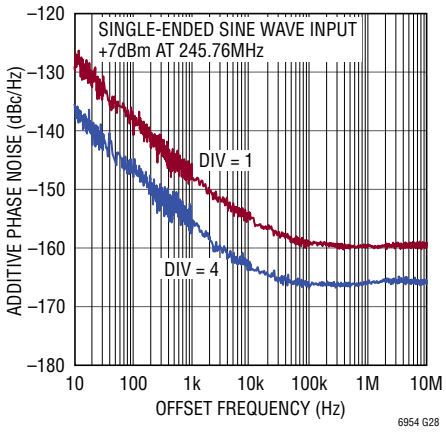
LVDS Output Additive Phase Noise, f_{IN} = 245.76MHz, I_{LVDS} = 7mA, R_{TERM} = 100Ω||100Ω (Differential)



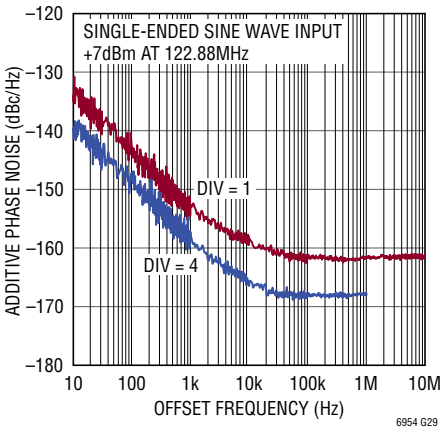
TYPICAL PERFORMANCE CHARACTERISTICS

$V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+ = 3.3V$.
$T_A = 25°C$, unless otherwise specified. All voltages are with respect to GND.

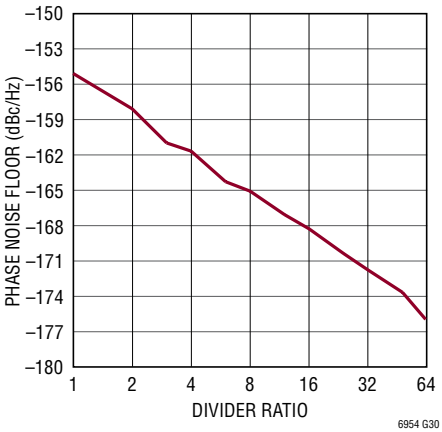
CMOS Output Additive Phase Noise, f_{IN} = 245.76MHz



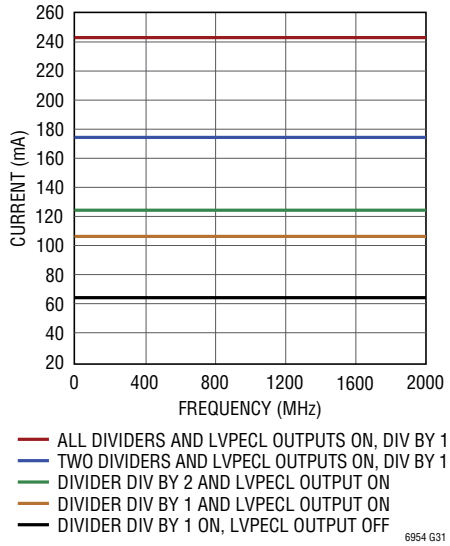
CMOS Output Additive Phase Noise, f_{IN} = 122.88MHz



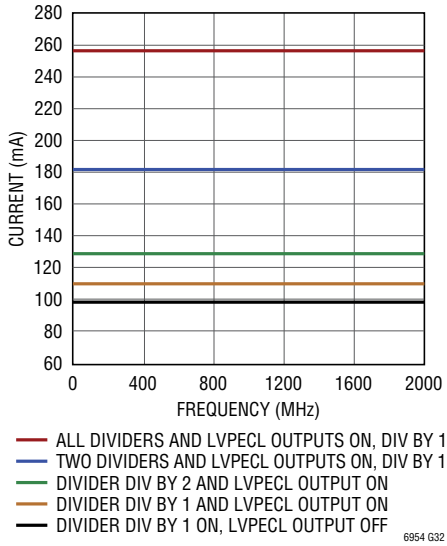
Additive Phase Noise Floor vs Divider Ratio F_{IN} = 1GHz, LVPECL IBIAS Enabled R_{TERM} = 100Ω Differential



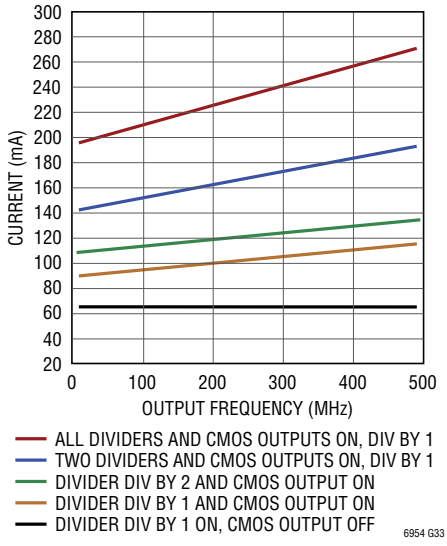
Supply Current vs Frequency, LVPECL Output, IBIAS Enabled, R_{TERM} = 100Ω Differential



Supply Current vs Frequency, LVPECL Output, IBIAS Disabled, R_{TERM} = 50Ω to V^+ – 2V



Supply Current vs Frequency, CMOS Output

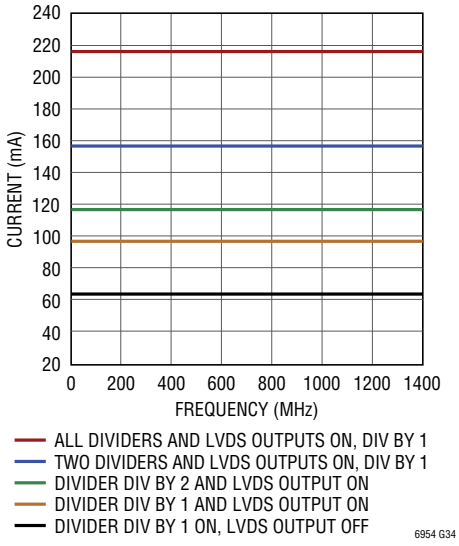


TYPICAL PERFORMANCE CHARACTERISTICS

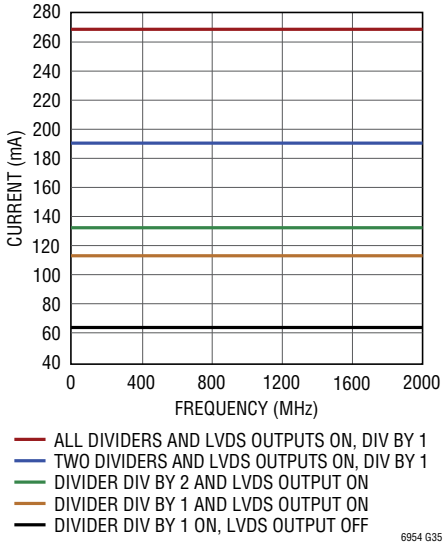
$V_A^+ = V_D^+ = V_{IN}^+ = V_{OUT0}^+ = V_{OUT1}^+ = V_{OUT2}^+ = 3.3V$.

T_A = 25°C, unless otherwise specified. All voltages are with respect to GND.

Supply Current vs Frequency, LVDS Output, I_{LVDS} = 3.5mA, R_{TERM} = 100Ω Differential



Supply Current vs Frequency, LVDS Output, I_{LVDS} = 7mA, R_{TERM} = 100Ω||100Ω (Differential)



PIN FUNCTIONS

LTC6954

V_{OUT0}^+, V_{OUT1}^+, V_{OUT2}^+ (Pins 1, 4, 5, 8, 9, 12): Output Supply Voltages. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. All V_{OUTx}^+ pins must be connected to the same supply voltage as the V_A^+, V_D^+ and V_{IN}^+ pins. Each pin, or in some cases pin pairs, must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

GND (Pins 14, 26, 29, 32, 35): Ground Connections. Should be tied directly to the exposed pad (pin 37) and to a low impedance ground plane for best performance. Refer to the Applications Information section for more details on grounding for signal integrity and thermal considerations.

V_A^+ (Pins 15, 23, 24, 34): Analog Supply Voltages. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. All V_A^+ pins must be connected to the same supply voltage as the V_{OUTx}^+, V_D^+ and V_{IN}^+ pins. Each pin, or in some cases pin pairs, must be separately bypassed directly to GND with a 0.1µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

$\overline{CS}$ (Pin 16): Serial Port Chip Select Input. This active LOW CMOS logic input initiates a serial port transaction when brought LOW. It finalizes the serial port transaction when brought HIGH after 16 serial port clock cycles. Refer to the Operation section for more details.

SDO (Pin 17): Serial Data Output. Data read from the serial port is presented on this CMOS logic pin. Refer to the Operation section for more details.

V_D^+ (Pins 18, 21): Digital Supply Voltages. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. All V_D^+ pins must be connected to the same supply voltage as the V_{OUTx}^+, V_A^+ and V_{IN}^+ pins. Each pin must be separately bypassed directly to GND with a 0.1µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

SCLK (Pin 19): Serial Port Clock Input. This positive edge triggered CMOS logic input signal clocks serial port data in on the rising edge. Refer to the Operation section for more details.

SDI (Pin 20): Serial Port Data Input. Data written into the serial port is presented on this CMOS logic pin. Refer to the Operation section for more details.

SYNC (Pin 22): The Synchronization Input Pin. A rising edge on this CMOS logic input initiates an output clock synchronization sequence. Precision output synchronization of one or more parts is handled on-chip, so the timing of this signal is not critical. Refer to the Operation and the Applications Information sections for more details.

V_{IN}^+ (Pins 25, 30): Analog Supply Voltages. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. All V_{IN}^+ pins must be connected to the same supply voltage as the V_{OUTx}^+, V_A^+ and V_D^+ pins. Each pin must be separately bypassed directly to GND with a 0.1µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

IN^+, IN^- (Pins 27, 28): The Signal Input Pins. The input signal can be either differential or single ended. It can be a sine wave, LVPECL logic, LVDS logic or CMOS logic. Refer to the Operation and Applications Information sections for more details on the correct use of the inputs.

TEMP (Pin 31): Temperature Monitoring Diode. This pin is connected to the anode of a diode that may be used to measure the die temperature, by forcing a current and measuring the voltage. Refer to the Applications Information section for more details on monitoring the die temperature.

GND (Exposed Pad Pin 37): Ground Connection. The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and low thermal resistance. Refer to the Applications Information section for more details on grounding for signal integrity and thermal considerations.

PIN FUNCTIONS

LTC6954-1 OUTPUTS AND MODE SELECT

OUT0SEL (Pin 13): OUT0 Mode Select. Connecting this pin to the V_A^+ supply enables the internal, active biasing of the OUT0 output emitter followers. Connecting this pin to GND disables this internal bias circuit. Refer to the Operation and Applications Information sections for more details on the LVPECL internal bias.

OUT0⁻, OUT0⁺ (Pins 10, 11): LVPECL Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{OUT0}^+ supply. Refer to the Operation and Applications Information sections for more details.

OUT1SEL (Pin 33): OUT1 Mode Select. Connecting this pin to the V_A^+ supply enables the internal, active biasing of the OUT1 output emitter followers. Connecting this pin to GND disables this internal bias circuit. Refer to the Operation and Applications Information sections for more details on the LVPECL internal bias.

OUT1⁻, OUT1⁺ (Pins 6, 7): LVPECL Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{OUT1}^+ supply. Refer to the Operation and Applications Information sections for more details.

OUT2SEL (Pin 36): OUT2 Mode Select. Connecting this pin to the V_A^+ supply enables the internal, active biasing of the OUT2 output emitter followers. Connecting this pin to GND disables this internal bias circuit. Refer to the Operation and Applications Information sections for more details on the LVPECL internal bias.

OUT2⁻, OUT2⁺ (Pins 2, 3): LVPECL Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{OUT2}^+ supply. Refer to the Operation and Applications Information sections for more details.

LTC6954-2 OUTPUTS AND MODE SELECT

OUT0SEL (Pin 13): OUT0 Mode Select. Connecting this pin to the V_A^+ supply enables the internal, active biasing of the OUT0 output emitter followers. Connecting this pin to GND disables this internal bias circuit. Refer to the Operation and Applications Information sections for more details on the LVPECL internal bias.

OUT0⁻, OUT0⁺ (Pins 10, 11): LVPECL Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{OUT0}^+ supply. Refer to the Operation and Applications Information sections for more details.

OUT1SEL (Pin 33): OUT1 Mode Select. Connecting this pin to the V_A^+ supply enables the internal, active biasing of the OUT1 output emitter followers. Connecting this pin to GND disables this internal bias circuit. Refer to the Operation and Applications Information sections for more details on the LVPECL internal bias.

OUT1⁻, OUT1⁺ (Pins 6, 7): LVPECL Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{OUT1}^+ supply. Refer to the Operation and Applications Information sections for more details.

OUT2SEL (Pin 36): OUT2 Mode Select. Connecting this pin to ground configures OUT2 as a CMOS logic type output. Connecting this pin to the V_A^+ supply configures OUT2 as an LVDS logic type output.

OUT2⁻, OUT2⁺ (Pins 2, 3): LVDS/CMOS Output Pins. These outputs may be programmed as LVDS or CMOS outputs using the OUT2SEL pin. Refer to the Operation and the Applications Information sections for more details.

PIN FUNCTIONS

LTC6954-3 OUTPUTS AND MODE SELECT

OUT0SEL (Pin 13): OUT0 Mode Select. Connecting this pin to the V_A^+ supply enables the internal, active biasing of the OUT0 output emitter followers. Connecting this pin to GND disables this internal bias circuit. Refer to the Operation and Applications Information sections for more details on the LVPECL internal bias.

OUT0$^-$, OUT0$^+$ (Pins 10, 11): LVPECL Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{OUT0}^+ supply. Refer to the Operation and Applications Information sections for more details.

OUT1SEL (Pin 33): OUT1 Mode Select. Connecting this pin to GND configures OUT1 as a CMOS logic type output. Connecting this pin to the V_A^+ supply configures OUT1 as an LVDS logic type output.

OUT1$^-$, OUT1$^+$ (Pins 6, 7): LVDS/CMOS Output Pins. These outputs may be programmed as LVDS or CMOS outputs using the OUT1SEL pin. Refer to the Operation and the Applications Information sections for more details.

OUT2SEL (Pin 36): OUT2 Mode Select. Connecting this pin to GND configures OUT2 as a CMOS logic type output. Connecting this pin to the V_A^+ supply configures OUT2 as an LVDS logic type output.

OUT2$^-$, OUT2$^+$ (Pins 2, 3): LVDS/CMOS Output Pins. These outputs may be programmed as LVDS or CMOS outputs using the OUT2SEL pin. Refer to the Operation and the Applications Information sections for more details.

LTC6954-4 OUTPUTS AND MODE SELECT

OUT0SEL (Pin 13): OUT0 Mode Select. Connecting this pin to GND configures OUT0 as a CMOS logic type output. Connecting this pin to the V_A^+ supply configures OUT0 as an LVDS logic type output.

OUT0$^-$, OUT0$^+$ (Pins 10, 11): LVDS/CMOS Output Pins. These outputs may be programmed as LVDS or CMOS outputs using the OUT0SEL pin. Refer to the Operation and the Applications Information sections for more details.

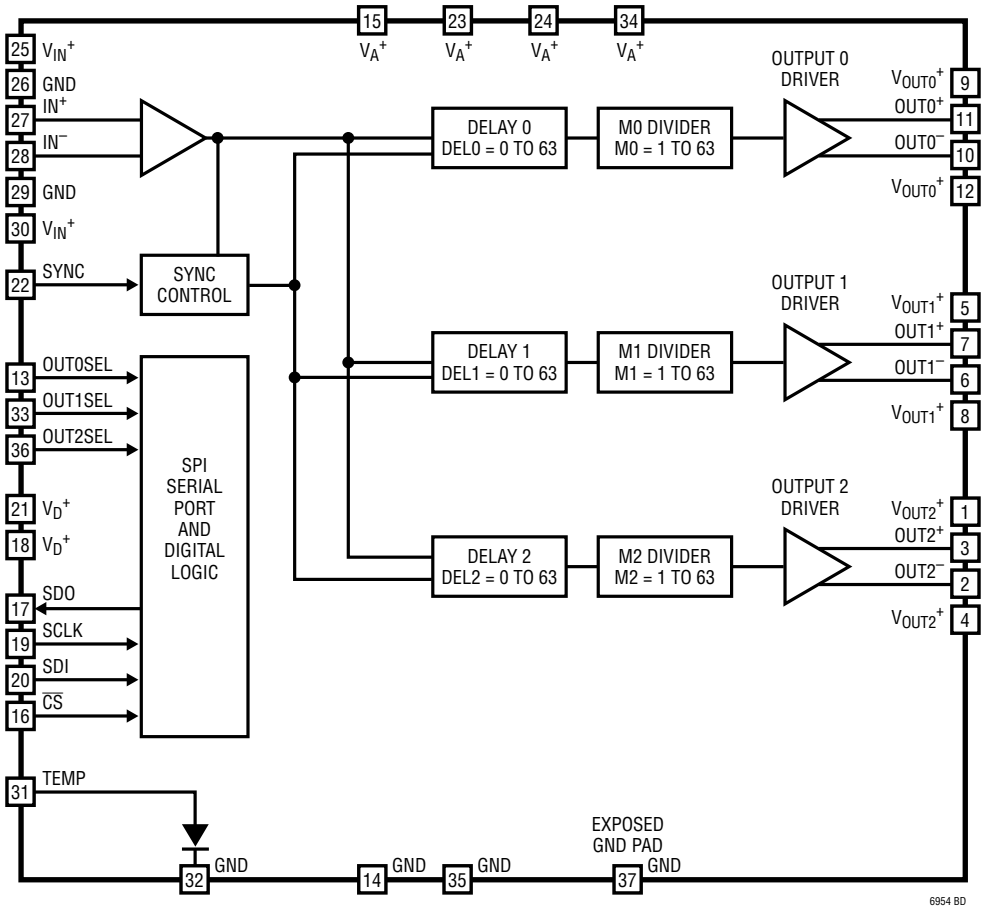
OUT1SEL (Pin 33): OUT1 Mode Select. Connecting this pin to GND configures OUT1 as a CMOS logic type output. Connecting this pin to the V_A^+ supply configures OUT1 as an LVDS logic type output.

OUT1$^-$, OUT1$^+$ (Pins 6, 7): LVDS/CMOS Output Pins. These outputs may be programmed as LVDS or CMOS outputs using the OUT1SEL pin. Refer to the Operation and the Applications Information sections for more details.

OUT2SEL (Pin 36): OUT2 Mode Select. Connecting this pin to GND configures OUT2 as a CMOS logic type output. Connecting this pin to the V_A^+ supply configures OUT2 as an LVDS logic type output.

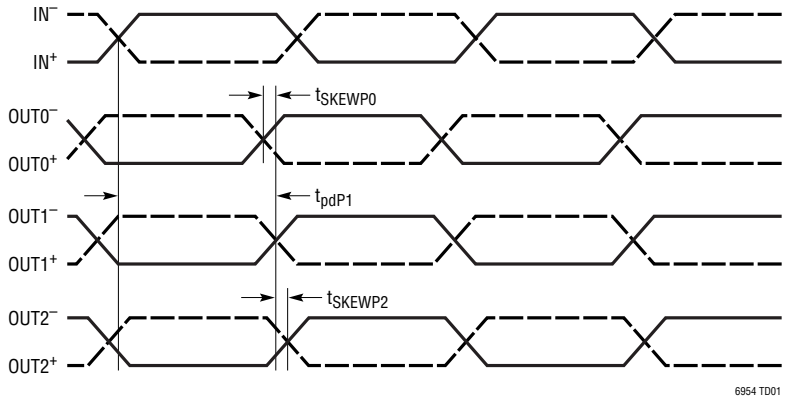
OUT2$^-$, OUT2$^+$ (Pins 2, 3): LVDS/CMOS Output Pins. These outputs may be programmed as LVDS or CMOS outputs using the OUT2SEL pin. Refer to the Operation and the Applications Information sections for more details.

BLOCK DIAGRAM

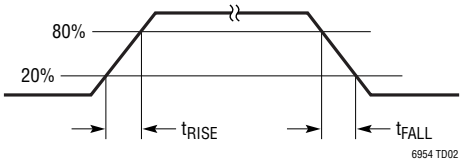


TIMING DIAGRAMS

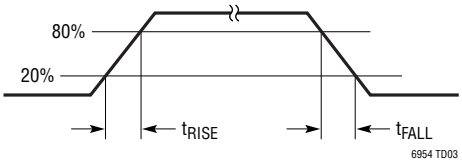
Output Propagation Delays and Skews, Mx[5:0] = 1



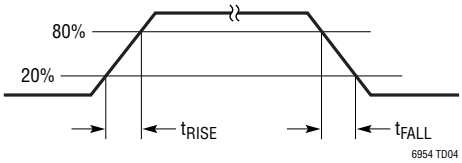
Differential LVPECL Rise/Fall Times



Differential LVDS Rise/Fall Times



Single-Ended CMOS Rise/Fall Times



OPERATION

LTC6954 INTRODUCTION

The LTC6954 is a family of low phase noise clock distribution parts. Each part provides three outputs, each with programmable frequency divider and delay blocks. There are four members of the family differing in their output logic signal type:

LTC6954-1: Three LVPECL outputs

LTC6954-2: Two LVPECL and one LVDS/CMOS outputs

LTC6954-3: One LVPECL and two LVDS/CMOS outputs

LTC6954-4: Three LVDS/CMOS outputs

As shown in Figure 1, the LTC6954 consists of two distinct circuit sections: multioutput clock distribution and digital control.

The clock distribution section of the LTC6954 receives an input signal up to 1.4GHz (1.8GHz for the LTC6954-1 when DELx = 0) and delivers three output signals based on the input. The output signal logic type depends on the LTC6954 part version and the connection of the OUTxSEL output mode selection pins. Table 1 shows all four part versions, each version's available output types and the effect of OUTxSEL pin connection on the output.

The LVPECL logic outputs are capable of operation up to 1.4GHz (1.8GHz for the LTC6954-1 when DELx = 0). Connecting the OUTxSEL pin to the V_A^+ supply enables the internal, active biasing of the output emitter followers. Connecting this pin to GND disables this internal bias circuit.

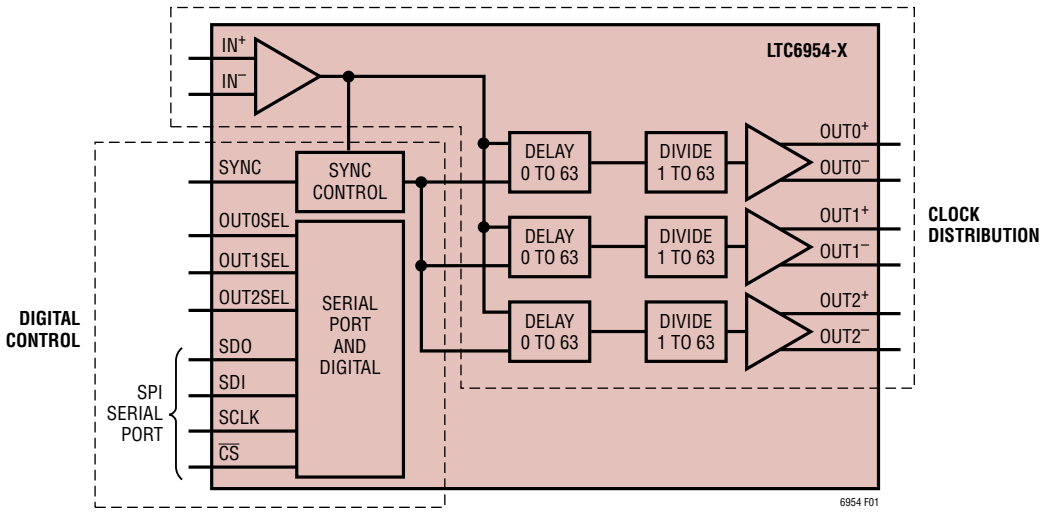


Figure 1.The LTC6954 Highlighting the Circuit Blocks

Table 1. LTC6954 Versions and Output Configurations

LTC6954 VERSION	OUTPUT 0		OUTPUT 1		OUTPUT 2	
	OUT0SEL = GND	OUT0SEL = V_A^+	OUT1SEL = GND	OUT1SEL = V_A^+	OUT2SEL = GND	OUT2SEL = V_A^+
LTC6954-1	LVPECL (IBIAS is Off)	LVPECL (IBIAS is On)	LVPECL (IBIAS is Off)	LVPECL (IBIAS is On)	LVPECL (IBIAS is Off)	LVPECL (IBIAS is On)
LTC6954-2	LVPECL (IBIAS is Off)	LVPECL (IBIAS is On)	LVPECL (IBIAS is Off)	LVPECL (IBIAS is On)	CMOS	LVDS
LTC6954-3	LVPECL (IBIAS is Off)	LVPECL (IBIAS is On)	CMOS	LVDS	CMOS	LVDS
LTC6954-4	CMOS	LVDS	CMOS	LVDS	CMOS	LVDS

OPERATION

The LVDS/CMOS output can be either a CMOS logic type or an LVDS logic type as configured by the OUTxSEL pin connection. Connecting the OUTxSEL pin to ground configures the output as a CMOS logic output capable of operation up to 250MHz. Connecting the OUTxSEL pin to the V_A^+ supply configures the output as an LVDS logic output capable of operation up to 800MHz for LVCSx set to 0 (far end line termination only), and up to 1400MHz for LVCSx set to 1 (doubly terminated). Refer to the Operation and Applications Information sections for more details.

Regardless of the LTC6954 part version and the output logic configuration, all three outputs are individually programmable to divide the input frequency by any integer from 1 to 63 and to delay any output by 0 to 63 input clock cycles. For an input signal with a 50% duty cycle, the output duty cycle will always be 50% regardless of the divide number.

The digital control section contains a full SPI-compatible serial control bus, the three output mode selection pins (OUT0SEL, OUT1SEL and OUT2SEL) and the EZSync clock synchronization (SYNC) function. Most device settings and operating modes are controlled through the SPI bus.

To minimize power consumption, many sections of the LTC6954 can be powered down when not in use. As shown in Figure 2, the LTC6954 can be used as an independent clock distribution part. Any unused outputs from the clock distribution section may be powered down.

Figure 3 highlights an LTC6950 driving the LTC6954. This example shows a single LTC6954 device, but each output from the LTC6950 can drive a separate LTC6954 device for support of up to five LTC6954 devices. The effortless-to-use EZSync multipart synchronization feature assures consistent edge alignment of all outputs from all devices. See the EZSync Clock Output Synchronization section for more details on EZSync operation.

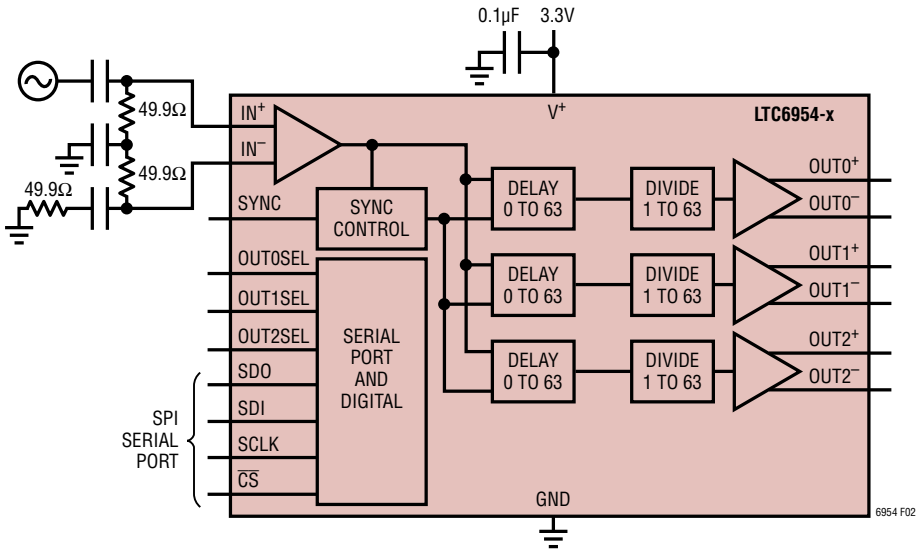


Figure 2. The LTC6954 Connected as an Independent Clock Distribution Part

OPERATION

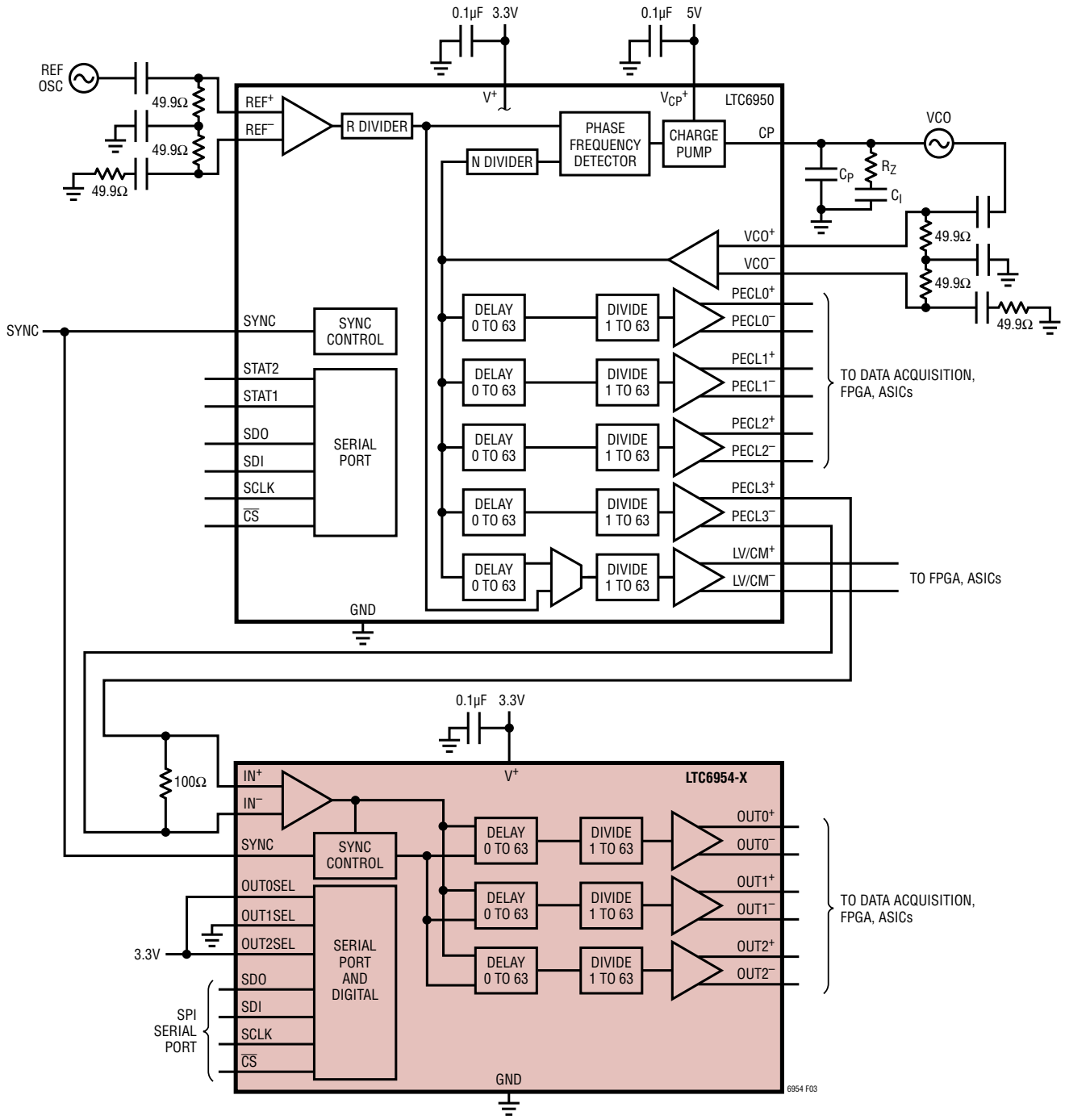


Figure 3. The LTC6950 in Controller Mode Clocking an LTC6954.
For Best Performance Use One of the LVPECL Outputs From the LTC6950 (with the IBIAS Enabled) to Clock the LTC6954. All Outputs From Both Devices Are Easily Synchronized by Applying a 1ms (Min) Wide Pulse on the SYNC Pins.