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## 105V, 2.3A Low EMI Synchronous Step-Down Regulator

### FEATURES

- Wide  $V_{IN}$  Range: 4.4V to 105V (110V Abs Max)
- Ultralow EMI/EMC Emissions: CISPR 25 Compliant
- $2\mu A$   $I_Q$  When Regulating  $48V_{IN}$  to  $3.3V_{OUT}$
- Fast and Accurate Output Current Programming and Monitoring with No External  $R_{SENSE}$
- Brick Wall Current Limit
- Low Minimum On-Time: 40ns
- Wide  $V_{OUT}$  Range: 1V to  $V_{IN}$
- 100% Maximum Duty Cycle Operation
- Programmable Fixed Frequency: 200kHz to 2MHz
- Eight, Pin-Selectable Fixed (1.2V to 15V) or Adjustable Output Voltages
- Selectable Pulse-Skipping or Low Ripple Burst Mode<sup>®</sup> Operation at Light Loads
- PLL Synchronization to External Clock
- $EXTV_{CC}$  LDO Powers Chip from  $V_{OUT} = 3.3V$  to 40V
- OPTI-LOOP<sup>®</sup> or Fixed Internal Compensation
- Input and Output Overvoltage Protection
- Thermally Enhanced (5mm × 6mm) QFN Package

### APPLICATIONS

- Battery Chargers and CC/CV Supplies
- Automotive and Military Systems
- Industrial, Avionics and Heavy Equipment
- Medical Instruments and Telecommunication Systems

### DESCRIPTION

The LTC<sup>®</sup>7103 is a high efficiency, monolithic synchronous step-down DC/DC converter utilizing a constant frequency, average current mode control architecture. It operates from an input voltage range of 4.4V to 105V and provides an adjustable regulated output voltage from 1V to  $V_{IN}$  while delivering up to 2.3A of output current.

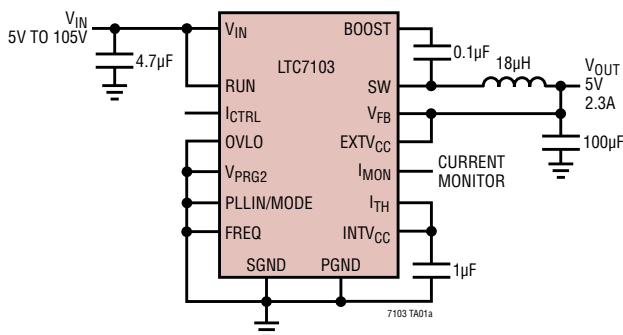
The LTC7103 features high frequency operation and a low minimum on-time that reduce inductor size and enable constant-frequency operation even at very high step-down ratios. In addition, the LTC7103 achieves the lowest possible dropout voltage with 100% maximum duty cycle operation. During light load operation, converter efficiency and output ripple can be optimized by selecting Burst Mode or pulse-skipping operation.

The LTC7103 includes accurate, high speed average current programming and monitoring without the need for an external sense resistor. Additional features include a bypass LDO to maximize efficiency, fixed or adjustable output voltage and loop compensation, and a wide array of protection features to enhance reliability.

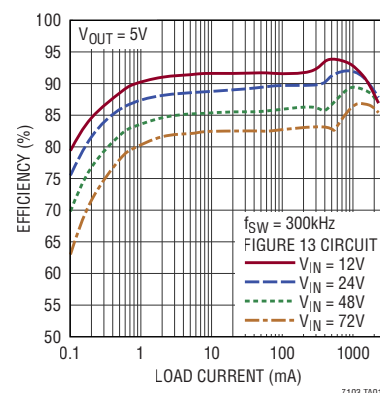
LT, LT, LTC, LTM, Linear Technology, Burst Mode, OPTI-LOOP and the Linear logo are registered trademarks of Analog Devices, Inc. All other trademarks are the property of their respective owners.

### TYPICAL APPLICATION

5V to 105V Input to 5V/2.3A Output Step-Down Regulator



Efficiency vs Load Current



# LTC7103

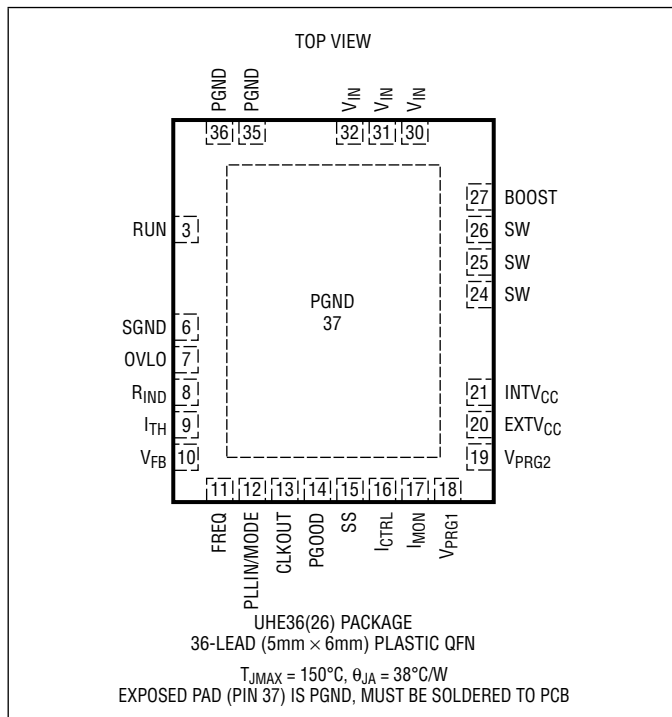
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$  Supply Voltage ..... -0.3V to 110V  
 $INTV_{CC}$ , (BOOST-SW) Voltages ..... -0.3V to 6V  
 BOOST Voltage ..... -0.3V to 110V  
 RUN Voltage ..... -0.3V to 110V  
 $V_{FB}$ , PGOOD Voltages ..... -0.3V to 16V  
 $EXTV_{CC}$  Voltage ..... -0.3V to 41V  
 $R_{IND}$ ,  $V_{PRG1}$ ,  $V_{PRG2}$  Voltages ..... -0.3V to  $INTV_{CC}$

$I_{CTRL}$ , SS Voltages ..... -0.3V to  $INTV_{CC}$   
 FREQ,  $I_{TH}$ , PLLIN/MODE, OVLO Voltages ..... -0.3V to 6V  
 Operating Junction Temperature Range (Notes 2, 3, 4)  
 LTC7103E, LTC7103I ..... -40°C to 125°C  
 LTC7103H ..... -40°C to 150°C  
 LTC7103MP ..... -55°C to 150°C  
 Storage Temperature Range ..... -65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

(<http://www.linear.com/product/LTC7103#orderinfo>)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7103EUHE#PBF	LTC7103EUHE#TRPBF	7103	36-Lead (5mm × 6mm) Plastic QFN	-40°C to 125°C
LTC7103IUHE#PBF	LTC7103IUHE#TRPBF	7103	36-Lead (5mm × 6mm) Plastic QFN	-40°C to 125°C
LTC7103HUHE#PBF	LTC7103HUHE#TRPBF	7103	36-Lead (5mm × 6mm) Plastic QFN	-40°C to 150°C
LTC7103MPUHE#PBF	LTC7103MPUHE#TRPBF	7103	36-Lead (5mm × 6mm) Plastic QFN	-55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.



## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 2)  $V_{IN} = 12\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Main Regulator and Voltage Loop</b>							
$V_{IN}$	Operating Input Voltage Range		4.4		105	V	
$V_{IN(UVLO)}$	$V_{IN}$ Undervoltage Lockout	$V_{IN}$ Rising	● 4.36	4.50	4.64	V	
		$V_{IN}$ Falling	● 4.11	4.25	4.39	V	
$V_{OUT}$	Operating Output Voltage Range		1.0		105	V	
$I_Q$	$V_{IN}$ Input DC Supply Current	(Note 8)					
	Pulse-Skipping Mode	$V_{FB} = 1.04\text{V}$ , $EXTV_{CC} = 3.3\text{V}$ $V_{FB} = 1.04\text{V}$ , $EXTV_{CC} = 0\text{V}$		200 4.4		$\mu\text{A}$ mA	
	Sleep Mode	$V_{FB} = 1.04\text{V}$ , $EXTV_{CC} = 3.3\text{V}$ $V_{FB} = 1.04\text{V}$ , $EXTV_{CC} = 0\text{V}$		1.0 9.0		$\mu\text{A}$ $\mu\text{A}$	
	Shutdown	$RUN = 0\text{V}$		0.7	8.0	$\mu\text{A}$	
	$V_{IN}$ Input Current In Regulation	Figure 13 Circuit, $V_{IN} = 48\text{V}$ , $I_{OUT} = 500\mu\text{A}$ Figure 15 Circuit, $V_{IN} = 48\text{V}$ , $I_{OUT} = 0\mu\text{A}$		64 2	75	$\mu\text{A}$ $\mu\text{A}$	
$V_{FB}$	Regulated Feedback Voltage	(Note 5)					
		$I_{TH}$ Voltage = 0.5V to 1.2V, $V_{IN} = 4.5\text{V}$ to 105V	●	0.990	1.000	1.010	V
		$V_{PRG1} = V_{PRG2} = \text{FLOAT}$	●	1.182	1.200	1.218	V
		$V_{PRG1} = V_{PRG2} = \text{INTV}_{CC}$	●	1.770	1.800	1.827	V
		$V_{PRG1} = \text{FLOAT}$ , $V_{PRG2} = \text{INTV}_{CC}$	●	2.455	2.500	2.537	V
		$V_{PRG1} = V_{PRG2} = \text{SGND}$	●	3.234	3.300	3.350	V
		$V_{PRG1} = \text{SGND}$ , $V_{PRG2} = \text{FLOAT}$	●	3.528	3.600	3.654	V
		$V_{PRG1} = \text{SGND}$ , $V_{PRG2} = \text{INTV}_{CC}$	●	4.900	5.000	5.075	V
		$V_{PRG1} = \text{FLOAT}$ , $V_{PRG2} = \text{SGND}$	●	11.75	12.00	12.24	V
		$V_{PRG1} = \text{INTV}_{CC}$ , $V_{PRG2} = \text{FLOAT}$ $V_{PRG1} = \text{INTV}_{CC}$ , $V_{PRG2} = \text{SGND}$	●	14.70	15.00	15.30	V
	Feedback Input Bias Current	$V_{PRG1} = V_{PRG2} = \text{FLOAT}$ $V_{PRG1}$ or $V_{PRG2}$ Tied to SGND or $\text{INTV}_{CC}$		$\pm 2$ 1.25	$\pm 10$ 1.6	nA $\mu\text{A}$	
$g_m$	Error Amplifier $g_m$	$I_{TH} = 1\text{V}$ , Sink/Source = $5\mu\text{A}$ (Note 5)		1.52		mS	
$t_{ON,MIN}$	Minimum Controllable ON-Time	(Note 7)	●	40	60	ns	
$R_{DS(ON)TOP}$	Top Switch On-Resistance			265		m $\Omega$	
$R_{DS(ON)BOT}$	Bottom Switch On-Resistance			142		m $\Omega$	
<b>Current Control and Monitoring</b>							
$I_{LIM(AVG)}$	Average Output Current Limit	(Note 6)		2.25	2.50	2.75	A
		$I_{CTRL} = 1.3\text{V}$ $I_{CTRL} = 0.58\text{V}$		0.36	0.5	0.64	A
$I_{PK}$	Top Switch Peak Current Limit	$I_{CTRL} = 1.3\text{V}$		3.32	3.70	4.30	A
		$I_{CTRL} = 0.58\text{V}$		1.56	1.70	2.09	A
$V_{IMON}$	Current Monitor Output Voltage	(Note 6)		1.04	1.12	1.19	V
		$I_{SW} = 2\text{A}$ $I_{SW} = 0.5\text{A}$		0.54	0.58	0.63	V
	$I_{CTRL}$ Pin Pull-Up Current	$V_{ICTRL} = 0.5\text{V}$	●	18	20	22	$\mu\text{A}$
<b>Start-Up and Shutdown</b>							
$I_{SS}$	Soft-Start Charge Current	$SS = 0\text{V}$	●	8	11	14	$\mu\text{A}$
$t_{SS(INT)}$	Internal Soft-Start Ramp Time	$SS = \text{FLOAT}$		1.2		ms	
$V_{FB(OV)}$	Feedback Overvoltage Protection	Relative to Regulated $V_{FB}$		7	10	13	%
$V_{RUN(ON)}$	RUN Pin ON Threshold	$V_{RUN}$ Rising	●	1.16	1.21	1.26	V
	RUN Pin Hysteresis			100		mV	
	RUN Pin Leakage Current	$RUN = 1.5\text{V}$		-10	0	10	nA
$V_{OV(R)}$	OVLO Pin Rising Threshold	$V_{OVLO}$ Rising	●	1.16	1.21	1.26	V

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 2)  $V_{IN} = 12\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
	OVLO Pin Hysteresis			65		mV	
	OVLO Pin Leakage Current	OVLO = 1.5V	-10	0	10	nA	
<b>Bias Regulators and Housekeeping</b>							
	INTV <sub>CC</sub> Undervoltage Lockout	INTV <sub>CC</sub> Rising INTV <sub>CC</sub> Falling		3.00 2.80		V V	
V <sub>EXTVCC</sub>	EXTV <sub>CC</sub> Switchover Voltage	EXTV <sub>CC</sub> Rising	●	3.04	3.10	3.17	V
		EXTV <sub>CC</sub> Falling	●	2.95	3.00	3.07	V
	Regulated INTV <sub>CC</sub> Voltage from V <sub>IN</sub>			3.37	3.5	3.6	V
	Regulated INTV <sub>CC</sub> Voltage from EXTV <sub>CC</sub>			3.37	3.5	3.6	V
<b>Oscillator and Phase-Locked Loop</b>							
	Programmable Frequency Accuracy	R <sub>FREQ</sub> = 12.5k (200kHz) to 57.5k (2MHz) PLLIN/MODE = 0V	●	-15		15	%
f <sub>LOW</sub>	Low Preset Frequency	V <sub>FREQ</sub> = 0V; PLLIN/MODE = 0V	●	270	300	330	kHz
f <sub>HIGH</sub>	High Preset Frequency	V <sub>FREQ</sub> = INTV <sub>CC</sub> ; PLLIN/MODE = 0V	●	0.9	1.0	1.1	MHz
	Synchronizable Frequency	PLLIN/MODE = External Clock	●	200		2000	kHz
	PLLIN/MODE Input High Level for Clocking	PLLIN/MODE = External Clock	●	2.0			V
	PLLIN/MODE Input Low Level for Clocking	PLLIN/MODE = External Clock	●			0.8	V
<b>PGOOD Output</b>							
	PGOOD Voltage Low	I <sub>PGOOD</sub> = 1mA		0.3	0.5		V
	PGOOD Leakage Current	V <sub>PGOOD</sub> = 12V		-1		1	μA
	PGOOD Trip Level	V <sub>FB</sub> with Respect to Set Regulated Voltage					
		V <sub>FB</sub> Ramping Positive		7	10	13	%
		Hysteresis			2.5		%
		V <sub>FB</sub> Ramping Negative		-13	-10	-7	%
		Hysteresis			2.5		%
T <sub>PG</sub>	Delay for Reporting a Fault			24			μs

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC7103E is guaranteed to meet specifications from 0°C to 85°C with specifications over the -40°C to 125°C operating junction temperature range assured by design, characterization and correlation with statistical process controls. The LTC7103I is guaranteed over the -40°C to 125°C operating junction temperature range, the LTC7103H is guaranteed over the -40°C to 150°C operating junction temperature range, and the LTC7103MP is tested and guaranteed over the -55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

**Note 3:**  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formula:

$$T_J = T_A + (P_D \cdot \theta_{JA} \text{ } ^\circ\text{C/W})$$

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device. The overtemperature protection level is not production tested.

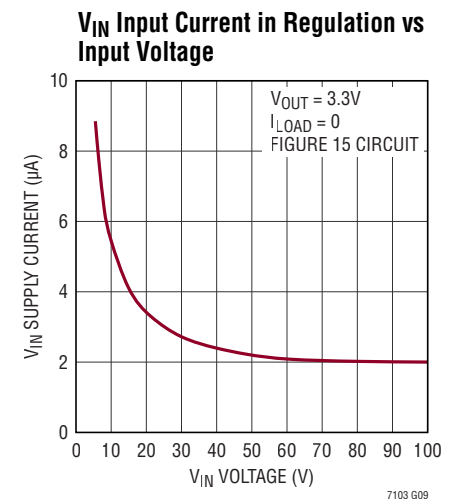
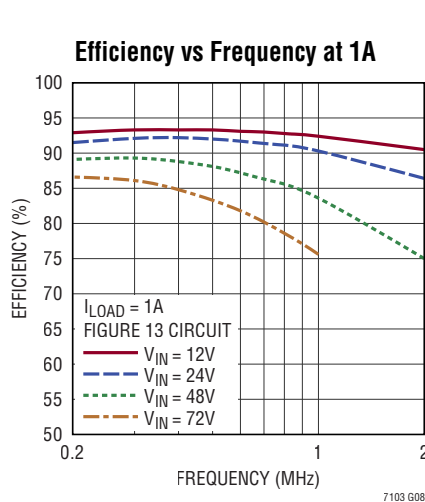
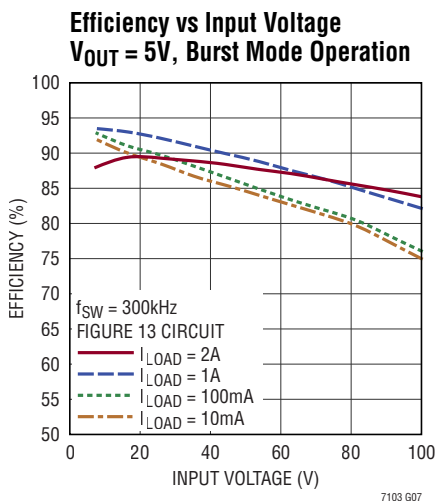
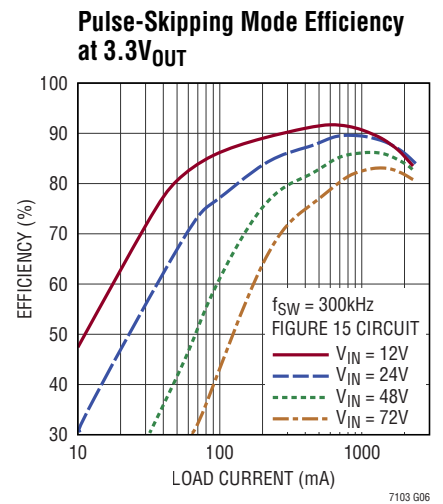
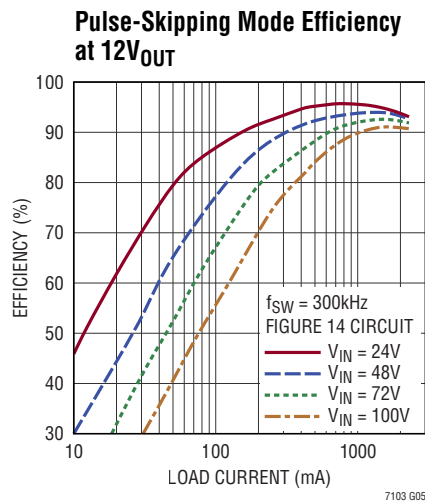
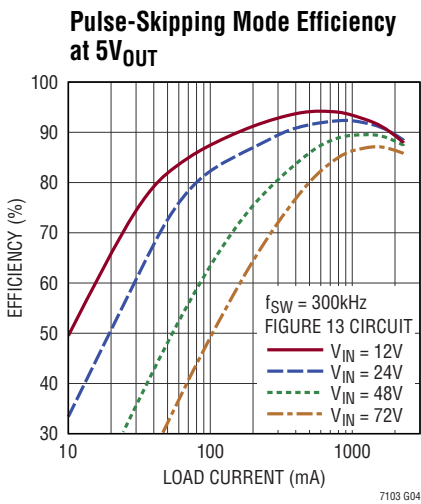
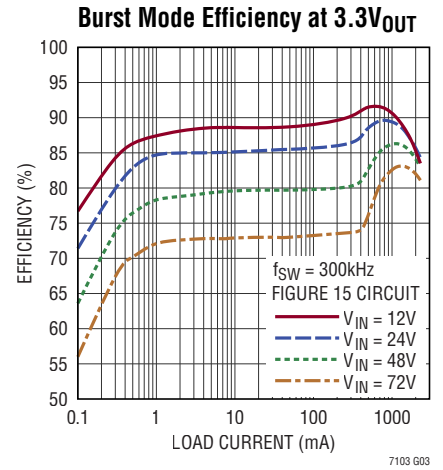
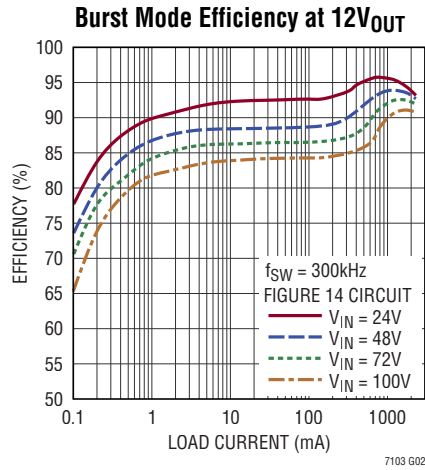
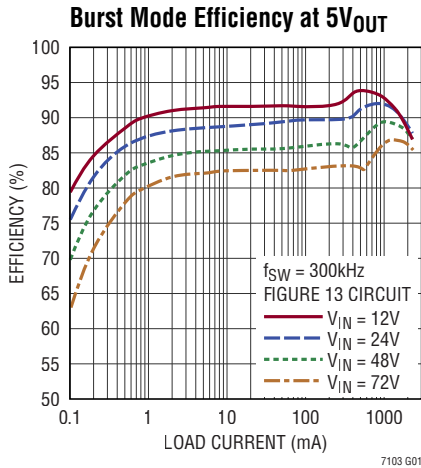
**Note 5:** The LTC7103 is tested in a feedback loop that servos  $V_{FB}$  to a voltage near the internal reference voltage to obtain the specified  $I_{TH}$  voltage.

**Note 6:** The Average Output Current Limit, the Top Switch Peak Current Limit and the Current Monitor Output Voltage are measured in a test circuit that simulates operation in a typical application.

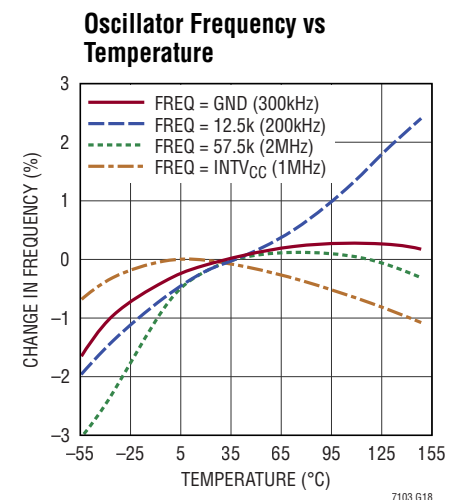
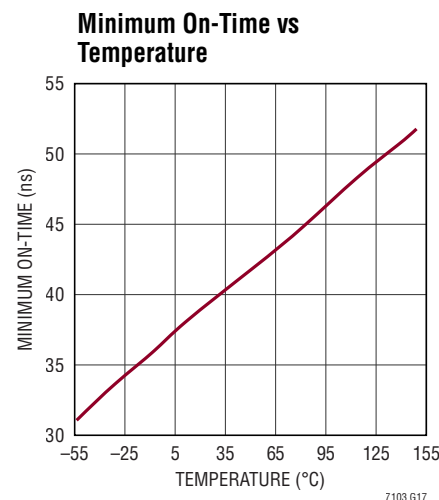
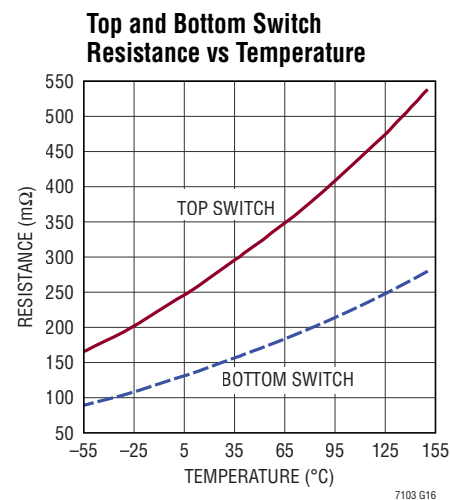
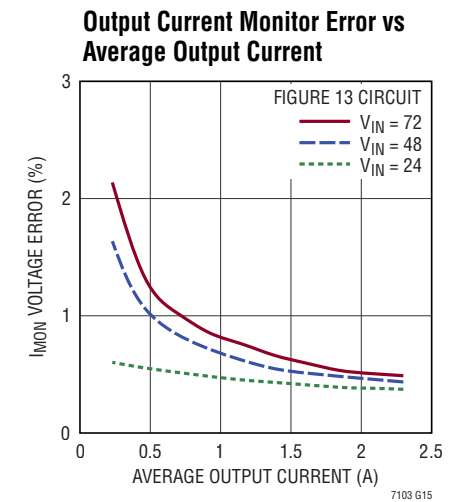
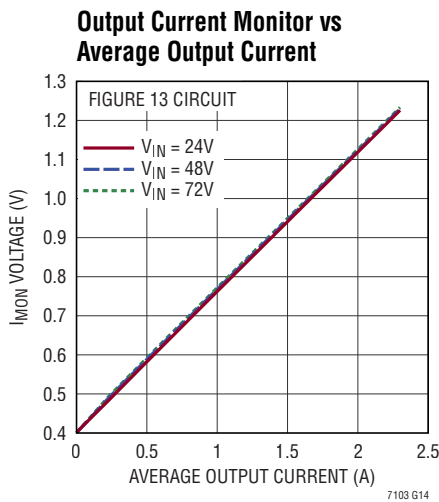
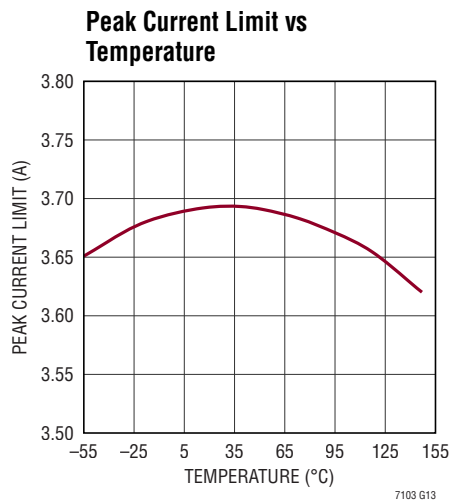
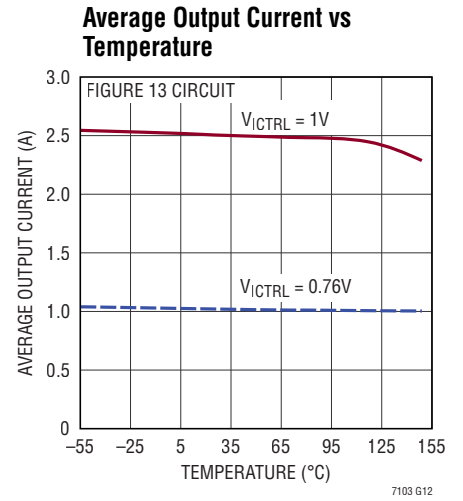
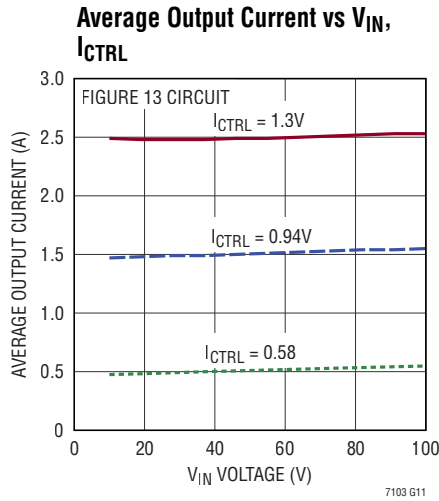
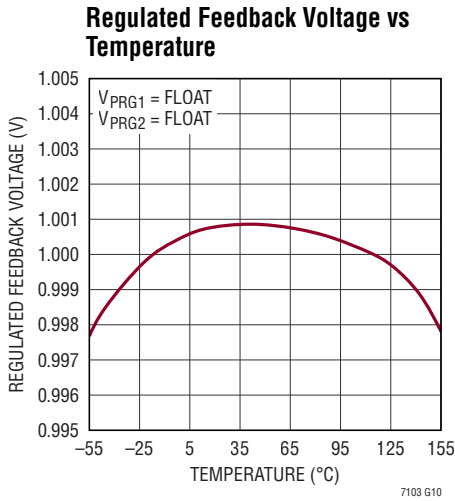
**Note 7:** The minimum controllable on-time is measured in a test mode. (See Minimum ON-Time Considerations in the Applications Information section.)

**Note 8:** Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

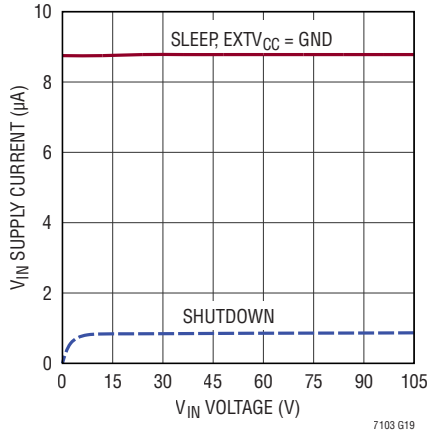


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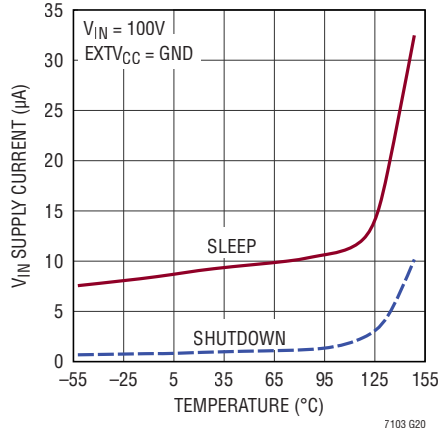


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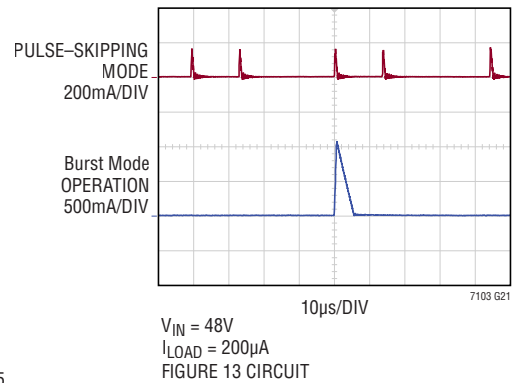
**Quiescent Input Current vs Input Voltage**



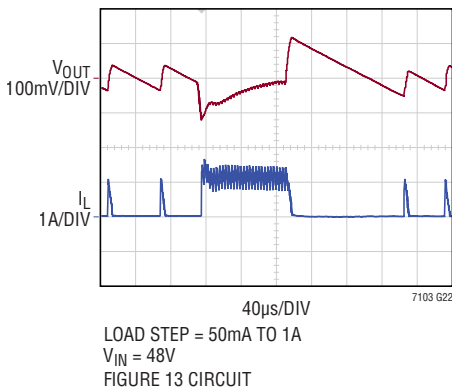
**V<sub>IN</sub> Quiescent Current vs Temperature**



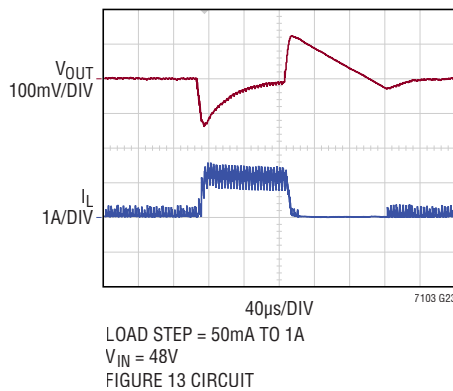
**Inductor Current at Light Load**



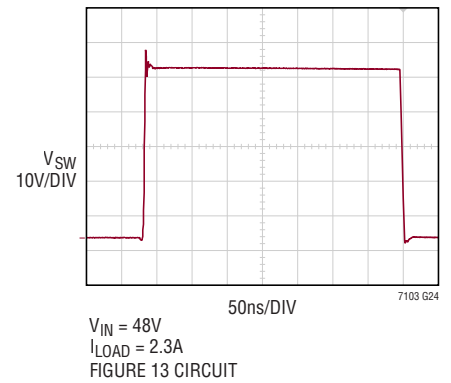
**Load Step Burst Mode Operation**



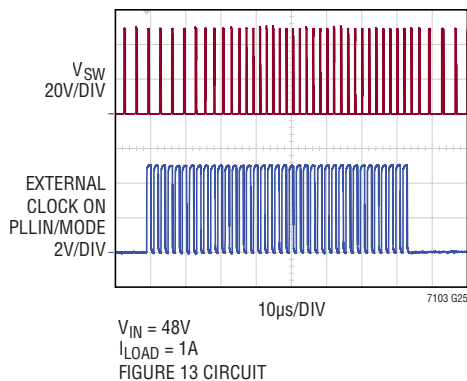
**Load Step Pulse-Skipping Mode**



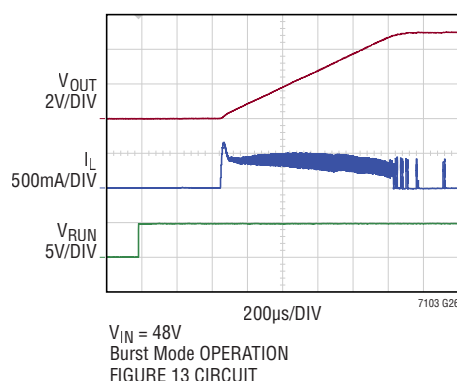
**SW Node Waveform at Full Load**



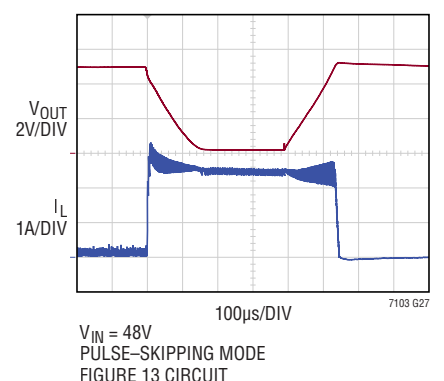
**Synchronization to External Clock**



**Start-Up from Shutdown**



**Short-Circuit and Recovery**

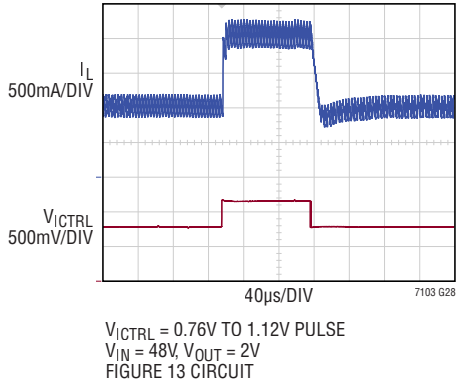




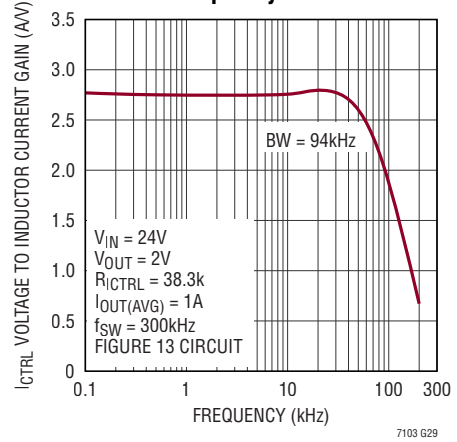
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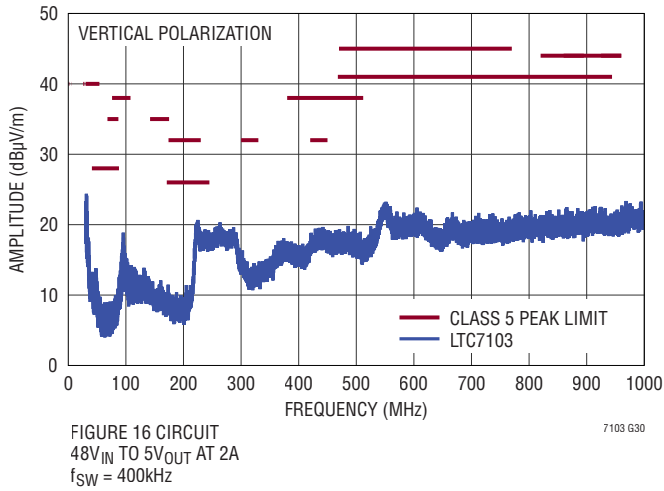
**Output Current Programming  
Current Loop Step Response**



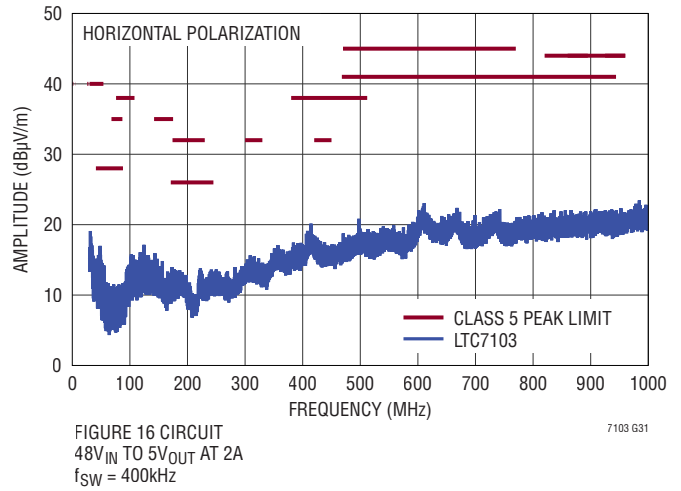
**$I_{CTRL}$  Voltage to Inductor Current  
Gain vs Frequency**



**Radiated EMI Performance (CISPR25 Radiated  
Emission Test with Class 5 Peak Limits)**



**Radiated EMI Performance (CISPR25 Radiated  
Emission Test with Class 5 Peak Limits)**



## PIN FUNCTIONS

**RUN (Pin 3):** Run Control Input. Holding this pin below 1.1V shuts off the switching regulator. Holding this pin below 0.7V reduces the quiescent current to approximately 0.7 $\mu$ A. Place a resistor divider between  $V_{IN}$  and this pin to use as an undervoltage lockout. Tie this pin to  $V_{IN}$  to always enable the LTC7103.

**SGND (Pin 6):** Signal Ground.

**OVLO (Pin 7):** Overvoltage Shutdown Input. If the voltage on this pin exceeds 1.21V, then the switching regulator is shut down and the SS pin is internally grounded. Tie this pin to SGND to allow operation with  $V_{IN}$  up to 105V.

**$R_{IND}$  (Pin 8):** Sets the current used to create an internal ramp that replicates the inductor current up-slope for low duty cycle operation. This pin generates a voltage that varies with the switching frequency. Place a resistor to SGND on this pin equal to  $1/(7.5 \cdot L)$  to set the internal ramp current. This pin can be left floating if fixed output voltage mode is selected using the  $V_{PRG1}$  and  $V_{PRG2}$  pins. If  $V_{PRG1}$  and  $V_{PRG2}$  are both floating, then a resistor from  $R_{IND}$  to SGND must be used.

**$I_{TH}$  (Pin 9):** Error Amplifier Output and Switching Regulator Compensation Point. Place compensation components between the  $I_{TH}$  pin and SGND. Tie this pin to  $INTV_{CC}$  for fixed internal compensation.

**$V_{FB}$  (Pin 10):** Regulator Feedback Input. When set to adjustable mode, use an external resistor divider between the regulator output voltage and the  $V_{FB}$  pin. For fixed output voltage mode, tie  $V_{FB}$  directly to the regulator output.

**FREQ (Pin 11):** The frequency control pin for the internal VCO. Connect this pin to SGND for 300kHz operation or to  $INTV_{CC}$  for 1MHz operation. Place a resistor to SGND on this pin to set the operating frequency between 200kHz and 2MHz. Minimize the capacitance on this pin if Burst Mode operation is used. This pin sources 40 $\mu$ A.

**PLLIN/MODE (Pin 12):** External Synchronization Input to Phase Detector and Burst Mode Control Input. When an external clock is applied to this pin, the phase-locked loop will force the rising edge of the SW signal to be synchronized with the rising edge of the external clock, and

the LTC7103 operates in pulse-skipping mode. When not synchronizing to an external clock, this input determines how the LTC7103 operates at light loads. Tie this pin to SGND or float to select Burst Mode operation or tie this pin to  $INTV_{CC}$  through a 100k resistor to select pulse-skipping operation. This pin sinks 10 $\mu$ A to SGND. Do not tie this pin directly to  $INTV_{CC}$ .

**CLKOUT (Pin 13):** Output clock signal available to synchronize additional regulators for parallel operation. The rising edge of CLKOUT is 180° out of phase with respect to the rising edge of the SW pin. The output level swings from SGND to  $INTV_{CC}$ .

**PGOOD (Pin 14):** Open-Drain Power Good Output. The  $V_{FB}$  pin is monitored to ensure that the output is in regulation. When the output is not in regulation, the PGOOD pin is pulled low.

**SS (Pin 15):** Soft-Start and Regulator Timeout Input. The voltage on the SS pin limits the regulated output voltage when the SS voltage is less than 1V. An internal 10 $\mu$ A pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Leave this pin floating to use the internal 1.2ms soft-start ramp. The SS pin also serves as a timeout to disable switching if the  $EXTV_{CC}$  voltage is too low. To disable the regulator timeout feature, tie a 75k resistor between SS and  $INTV_{CC}$ . See Soft-Start and LDO Regulator Timeout in the Applications Information section.

**$I_{CTRL}$  (Pin 16):** Programs the Average Output Current in Constant Current Mode. The voltage on this pin determines the maximum  $I_{TH}$  voltage, which in turn sets the average output current in constant-current mode. The peak current limit tracks 1.2A above the average current limit set point. Tie this pin to a voltage between 0.4V and 1.3V to program the average output current to a value between 0A and 2.5A. An internal 20 $\mu$ A pull-up on this pin allows a single resistor to SGND to be used to set the voltage.

**$I_{MON}$  (Pin 17):** Average Output Current Monitor. This pin generates a voltage between 0.4V and 1.3V that corresponds to an average output current between 0A and 2.5A.

## PIN FUNCTIONS

**V<sub>PRG1</sub>, V<sub>PRG2</sub> (Pins 18, 19):** Output Voltage Programming Pins. These pins set the regulator to adjustable output mode or to fixed output mode. Floating both pins allows the output to be programmed through the V<sub>FB</sub> pin using external resistors, regulating V<sub>FB</sub> to the 1V reference. Tying one of these pins to SGND or INTV<sub>CC</sub> while the other is tied to SGND, INTV<sub>CC</sub> or floating programs the output to one of eight fixed output voltages. See Output Voltage Programming in the Applications Information section.

**EXTV<sub>CC</sub> (Pin 20):** External Power Input to an Internal LDO that Generates INTV<sub>CC</sub>. This LDO supplies INTV<sub>CC</sub> power from EXTV<sub>CC</sub>, bypassing the internal LDO powered from V<sub>IN</sub> whenever EXTV<sub>CC</sub> is between 3.1V and 40V. If EXTV<sub>CC</sub> is not used, the regulator timeout feature must be disabled by tying a 75k resistor between SS and INTV<sub>CC</sub>. See INTV<sub>CC</sub> Regulations in the Applications Information section.

**INTV<sub>CC</sub> (Pin 21):** Output of the Internal LDO regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to PGND with a 1μF to 4.7μF ceramic capacitor.

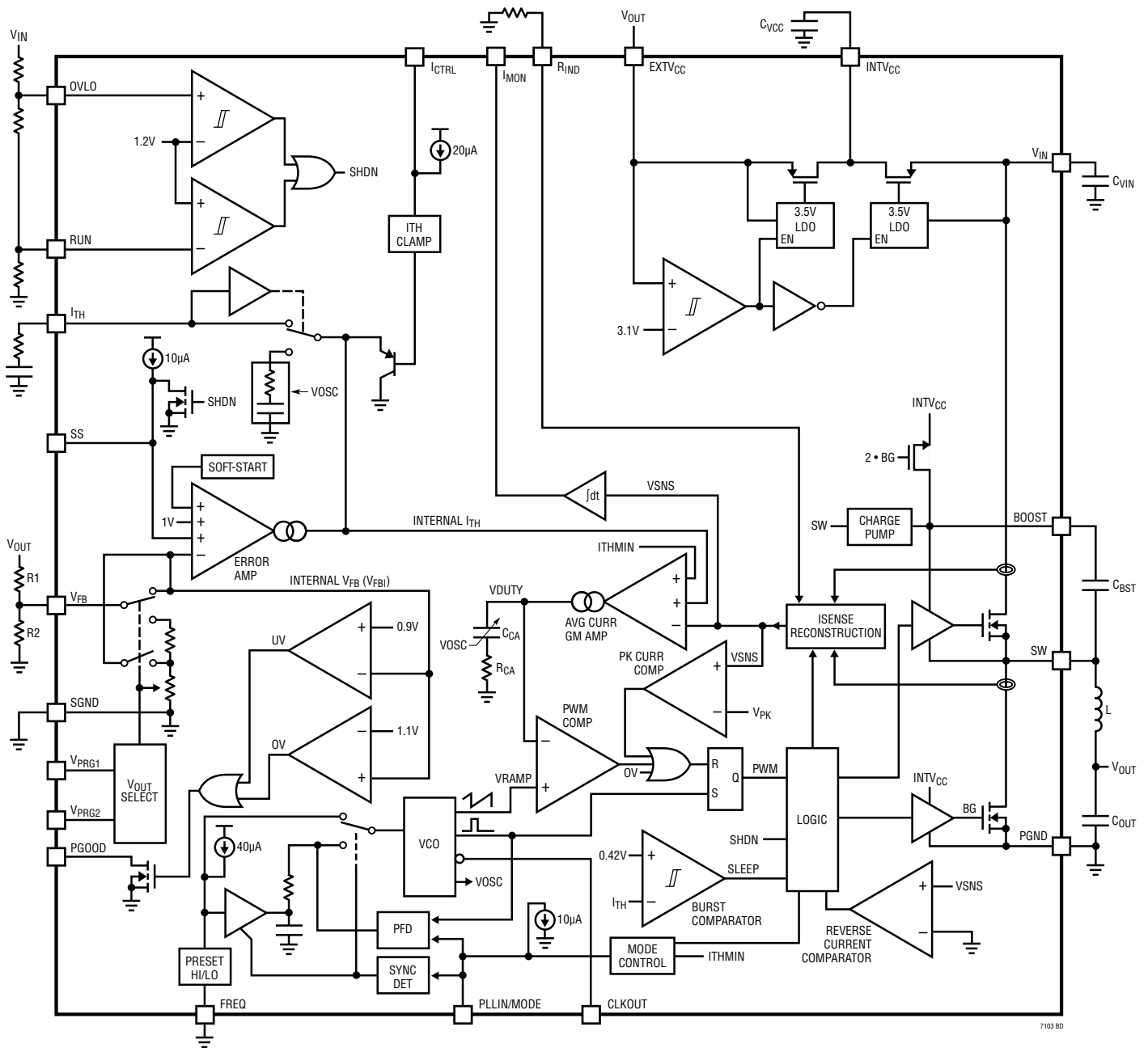
**SW (Pins 24, 25, 26):** SW Node connection from the internal MOSFET power switches to the output inductor.

**BOOST (Pin 27):** Bootstrapped Supply to the High Side Floating Gate Driver. Connect a 0.1μF ceramic capacitor between the BOOST and SW pins.

**V<sub>IN</sub> (Pins 30, 31, 32):** Power Input Supply. This is the power input to the integrated high side MOSFET switch as well as the input to the internal LDO that generates INTV<sub>CC</sub> voltage. Decouple this pin with a capacitor to PGND.

**PGND/Exposed Pad (Pin 35, 36, 37):** Power Ground. Connect to power ground plane. The exposed pad must be connected to PCB ground for rated electrical and thermal performance.

# FUNCTIONAL DIAGRAM



7103 BD

## OPERATION

### Main Control Loop

The LTC7103 is a high efficiency, monolithic, synchronous step-down DC/DC converter utilizing a constant frequency, average current mode control architecture. Average current mode control enables fast and precise control of the output current without the need for an external sense resistor or current sense amplifier. Instead, the inductor current is sensed internally by losslessly monitoring the top and bottom power switch currents. The LTC7103 also contains a unique circuit that replicates the inductor current immediately after the top switch turn-on and combines this with the sensed switch currents to fully reconstruct the inductor current signal internally. This technique allows for direct control and monitoring of the average output current as well as clean operation at very low duty cycles.

During normal operation, the internal top power switch (N-channel MOSFET) is turned on at the beginning of each clock cycle, causing the inductor current to increase. The sensed inductor current is then delivered to the average current amplifier, whose output (VDUTY) is compared with a saw-tooth ramp (VRAMP). When the VRAMP voltage exceeds the VDUTY voltage, the PWM comparator trips and turns off the top power MOSFET.

After the top power MOSFET turns off, the synchronous power switch (N-channel MOSFET) turns on, causing the inductor current to decrease. The bottom switch stays on until the beginning of the next clock cycle, unless the reverse current limit (OA) is reached and the reverse current comparator trips.

In closed-loop operation, the average current amplifier creates an average current loop that forces the average sensed current signal to be equal to the internal  $I_{TH}$  voltage. Note that the DC gain and compensation of this average current loop is automatically adjusted to maintain an optimum current-loop response. The error amplifier adjusts the  $I_{TH}$  voltage by comparing the divided-down output voltage ( $V_{FBI}$ ) with a 1.0V reference voltage. If the load current changes, the error amplifier adjusts the average inductor current as needed to keep the output voltage in regulation.

The LTC7103 has been optimized to provide the fastest possible average current loop. To achieve this, the filter on the average current amplifier output ( $C_{CA}$ ,  $R_{CA}$ ) is set to provide high DC gain (provided by integrator capacitor  $C_{CA}$ ) while allowing the inductor current signal to pass through unfiltered. This is accomplished by resistor  $R_{CA}$ , which introduces a zero that is well below the switching frequency. The resulting typical PWM comparator waveforms are shown in Figure 1. Note that the VDUTY signal is an inverted reflection of the inductor current signal, which is essential for obtaining a high speed average current loop.

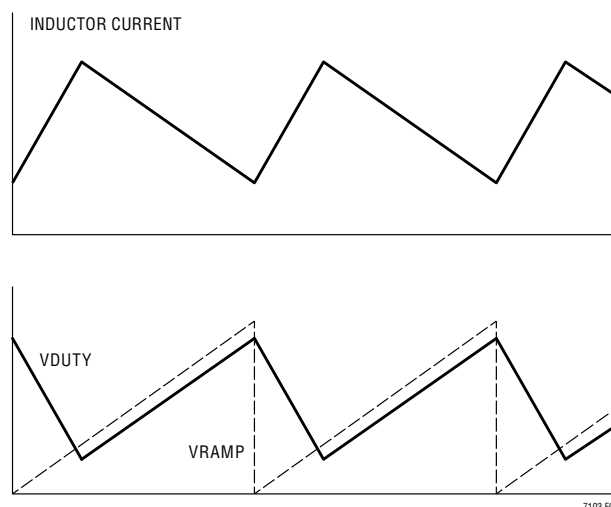


Figure 1. Typical Current Loop Operating Waveforms

Voltage loop compensation can be set externally using the  $I_{TH}$  pin, taking advantage of OPTI-LOOP compensation to optimize the loop response. The compensation of the voltage loop is essentially the same as for peak current mode control. Alternatively, the  $I_{TH}$  pin can be tied to  $INTV_{CC}$  to select internal voltage loop compensation. When internal voltage loop compensation is selected, the LTC7103 automatically adjusts the internal compensation based on switching frequency to maintain a fast and stable voltage loop.

### Power and Bias Supplies ( $V_{IN}$ , SW, BOOST, $INTV_{CC}$ , $EXTV_{CC}$ Pins)

The  $V_{IN}$  pins on the LTC7103 are used to supply voltage to the drain terminal of the internal high side N-channel MOSFET. These pins also supply bias voltage for an internal



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LDO regulator (the  $V_{IN}$  LDO) that generates 3.5V at  $INTV_{CC}$ . The voltage on  $INTV_{CC}$  in turn is used for internal chip bias as well as gate drive for the bottom power MOSFETs. The gate drive for the top power MOSFET is supplied by a floating supply ( $C_{BST}$ ) between the BOOST and SW pins, which is charged by an internal synchronous diode from  $INTV_{CC}$ . In addition, an internal charge pump allows for 100% duty cycle operation by maintaining the BOOST to SW voltage when the top MOSFET is on continuously.

To improve efficiency and limit power dissipation in the  $V_{IN}$  LDO regulator, a second LDO regulator (the  $EXTV_{CC}$  LDO) allows the  $INTV_{CC}$  voltage to be derived from the lower-voltage  $EXTV_{CC}$  pin. In most applications, the  $EXTV_{CC}$  pin is simply tied directly to the regulated output voltage of the DC/DC converter to enable operation in a high efficiency, bootstrapped configuration. In order to ensure that the power dissipation on the internal  $V_{IN}$  LDO is limited to a safe level, the LTC7103 incorporates a special regulator timeout feature into the soft-start pin.

### Start-Up and Shutdown (RUN, SS, OVLO Pins)

When the RUN pin is below 0.7V, the LTC7103 enters a low current shutdown state, reducing the DC supply current to 0.7 $\mu$ A. When the RUN pin is above 0.7V and the  $V_{IN}$  pin is above than the internal undervoltage threshold ( $V_{IN(UVLO)}$ ) of 4.55V, the  $INTV_{CC}$  LDO regulators are enabled. However, switching is inhibited until the RUN pin is greater than  $V_{RUN(ON)} = 1.21V$ . This allows the RUN pin to be used to implement a  $V_{IN}$  undervoltage lockout function so that the power supply will not operate below a user-adjustable level. In addition, switching is also inhibited if the voltage on the OVLO pin exceeds  $V_{OV(R)} = 1.21V$ . This feature can be used to implement an input overvoltage lockout function to prevent power supply operation during an overvoltage condition on the input supply.

When appropriate voltages are present on the  $V_{IN}$ , RUN and OVLO pins, the LTC7103 will begin switching and initiate a soft-start ramp of the output voltage. An internal soft-start ramp of 1.2ms will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, a capacitor can be placed from the SS pin to ground. The 10 $\mu$ A current that is sourced from the SS pin will create a smooth voltage ramp on the capacitor. If this external ramp rate is slower

than the internal 1.2ms soft-start, then the output voltage will be limited by the ramp rate on the SS pin instead. Once both the external and internal soft-start ramps have exceeded 1V, the output voltage will be in regulation. The internal and external soft-start functions are reset during initial start-up and after an undervoltage or overvoltage condition on the input supply.

The soft-start pin is also used to implement a regulator timeout feature. This feature limits die temperature rise due to power dissipation in the internal  $V_{IN}$  LDO regulator by disabling the top and bottom power MOSFETs after a timeout, if  $EXTV_{CC}$  voltage is not present. This is useful, for example, if  $EXTV_{CC}$  is tied to the output of the DC/DC converter, but the converter output gets shorted to ground. During start-up, a regulator timeout begins after both the internal and external soft-start ramps have exceeded 1V, and  $EXTV_{CC} < 3V$ . If this condition persists for a period of time (approximately 1.4 times the normal soft-start time), then a regulator timeout fault occurs and all switching stops. After a long restart delay (approximately 46 times the normal soft-start time), a restart is initiated. If the regulator timeout feature is not needed, the SS pin should be tied to  $INTV_{CC}$  through a 75k resistor. See Soft-Start and LDO Regulator Timeout in the Applications Section for more information.

### Output Voltage Programming ( $V_{PRG1}$ , $V_{PRG2}$ , $V_{FB}$ Pins)

The  $V_{PRG1}$  and  $V_{PRG2}$  pins provide a great deal of flexibility in programming the output voltage of the power supply. Floating both pins selects adjustable  $V_{OUT}$  mode. In this mode, the output is programmed using external resistors on the  $V_{FB}$  pin, and the  $V_{FB}$  voltage is regulated to the 1V reference. If one of the pins is tied either to SGND or  $INTV_{CC}$ , then fixed output voltage mode is selected. In this mode, precision internal resistor dividers are used to program the output voltage to one of eight fixed voltage levels. See Output Voltage Programming in the Applications Information Section.

### Inductor Current Replication ( $R_{IND}$ Pin)

The LTC7103 contains a unique circuit that replicates the inductor current immediately after the top switch turn-on and combines this with the sensed switch currents to fully reconstruct the inductor current signal internally. This

## OPERATION

technique allows for direct control and monitoring of the average output current as well as clean operation at very short top switch on-times. In order to replicate the inductor current, the LTC7103 needs to know the approximate value of the inductor. This is achieved by placing a resistor on the  $R_{IND}$  pin that is equal to  $1/(7.5 \cdot L)$ . The LTC7103 uses the current in the  $R_{IND}$  resistor in conjunction with the voltage on the  $V_{IN}$  and SW pins to generate a replicated inductor current signal. In addition, the  $R_{IND}$  pin current is also used in conjunction with the voltages on  $V_{IN}$  and SW to set the DC gain of the average current amplifier. This is done to maintain optimum current loop performance over all operating conditions.

Note that if fixed output voltage mode is selected using the  $V_{PRG1}$  and  $V_{PRG2}$  pins, then the  $R_{IND}$  pin can be left floating. In this case, the LTC7103 will assume a particular inductor value based on output voltage and switching frequency. See Inductor Value and  $R_{IND}$  Resistor Selection in the Applications Information section.

### Light Load Operation: Burst and Pulse-Skipping Modes (PLLIN/MODE Pin)

The LTC7103 can be set to enter high efficiency Burst Mode operation or constant frequency pulse-skipping mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground. To select pulse-skipping mode, tie the PLLIN/MODE pin to  $INTV_{CC}$  through a 100k resistor.

When the LTC7103 is set for Burst Mode operation, the minimum output current is set to approximately 200mA even though the voltage on the  $I_{TH}$  pin might indicate a lower value. If the average inductor current is higher than the load current, the error amplifier will decrease the voltage on the  $I_{TH}$  pin. When the  $I_{TH}$  voltage drops below 0.4V, the internal sleep signal goes high (enabling sleep mode) and both MOSFETs are turned off. The  $I_{TH}$  pin is then disconnected from the output of the error amplifier and parked at 0.43V.

In sleep mode, much of the internal circuitry is turned off, reducing the total quiescent current that the LTC7103 draws to 9 $\mu$ A. When  $EXTV_{CC}$  is present, the majority of this quiescent current (8 $\mu$ A) is drawn from the  $EXTV_{CC}$  supply and only 1 $\mu$ A is drawn from the  $V_{IN}$  supply. This dramatically reduces the sleep mode  $V_{IN}$  supply current in bootstrapped applications where  $EXTV_{CC}$  is tied to  $V_{OUT}$  and  $V_{IN} \gg V_{OUT}$ . In sleep mode, the load current is supplied by the output capacitor. As the output voltage  $V_{OUT}$  decreases, the error amplifier output begins to rise. When the  $V_{OUT}$  voltage drops enough, the  $I_{TH}$  pin is reconnected to the output of the error amplifier, the sleep signal goes low, and normal operation is resumed by turning on the top MOSFET on the next cycle of the internal oscillator.

When the LTC7103 is set for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the converter operates with discontinuous inductor current (DCM).

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC7103 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation.

When operating with discontinuous inductor current (DCM) in either burst or pulse-skipping mode, the LTC7103 smoothly transitions from average current to peak current control. This feature eases compensation of the voltage loop in light load DCM operation by removing the pole associated with the average current loop.

## OPERATION

To avoid spurious changes in the operating mode, the LTC7103 incorporates a 20 $\mu$ s delay before changing from one mode to another. This is particularly helpful since the PLLIN/MODE pin can be used to select an initial operating mode, and subsequently be used to receive an external clock for synchronization. The 20 $\mu$ s delay avoids changes in mode while the synchronizing signal is recognized. When synchronized, the LTC7103 operates in pulse-skipping mode.

### Frequency Selection and Phase-Locked Loop (FREQ, PLLIN/MODE Pins)

The switching frequency of the LTC7103 can be selected using the FREQ pin, which can be tied to SGND, tied to INTV<sub>CC</sub>, or programmed through an external resistor. Tying FREQ to SGND selects 300kHz while tying FREQ to INTV<sub>CC</sub> selects 1MHz. Placing a resistor between FREQ and SGND sends the FREQ pin voltage into the input of the voltage controlled oscillator (VCO), allowing the frequency to be programmed between 200kHz and 2MHz.

A phase-locked loop (PLL) is available on the LTC7103 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC7103's phase detector (PFD) and low pass filter adjust the voltage of the VCO input to align the turn-on of the top MOSFET to the rising edge of the synchronizing signal.

When an external clock is detected, the PFD low pass filter is quickly prebiased to the operating frequency set by the FREQ pin before the PLL is allowed to take over the VCO. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the top MOSFET turn-on. The ability to prebias the loop filter allows the PLL to lock in rapidly without deviating far from the desired frequency.

The typical capture range of the phase-locked loop is from approximately 160kHz to 2.3MHz, with a guarantee over all manufacturing variations to be between 200kHz and 2MHz. In other words, the LTC7103's PLL is guaranteed to lock to an external clock source whose frequency is between 200kHz and 2MHz.

After the PLL has locked to an external clock, if the external clock is stopped, the LTC7103 will immediately detect this condition and prevent the PFD from adjusting the loop, so that the internal oscillator continues operating at the external clock frequency. After approximately 9 $\mu$ s, the LTC7103 will detect a loss of SYNC, and the oscillator operating frequency returns to the level set by the FREQ pin. This feature prevents the oscillator frequency from dipping momentarily when the external clock is stopped, and enables smooth transitions into and out of synchronization.

The typical input clock thresholds on the PLLIN/MODE pin are 1.5V rising and 1.1V falling, and this input is TTL compatible.

The CLKOUT pin supplies a reference clock that is helpful for synchronizing other switching circuits to the LTC7103 switching frequency. The output high level of this signal is equal to INTV<sub>CC</sub> (3.5V typical), and the rising edge of the CLKOUT signal is 180° out of phase with respect to the top MOSFET turn-on. This makes it easy to synchronize two LTC7103 converters and operate them out of phase to minimize input current, or to use two LTC7103's together for a higher current, 2-Phase converter. See 2-Phase Operation in the Applications Information section.

### Setting and Monitoring Output Current (I<sub>CTRL</sub>, I<sub>MON</sub> Pins)

Because the LTC7103 utilizes average current mode control, in which the I<sub>TH</sub> voltage is proportional to average output current, the setting and monitoring of the average output current is straight-forward.

The average output current limit is set using the I<sub>CTRL</sub> pin, whose voltage directly clamps the I<sub>TH</sub> voltage to a maximum level. Tie this pin to a voltage between 0.4V and 1.3V to program the average output current to a value between 0A and 2.5A. An internal 20 $\mu$ A pull-up on this pin allows a single resistor to SGND to be used to set the voltage.

By maintaining a fast and optimized current loop over all operating conditions, the LTC7103 responds to changes in the I<sub>CTRL</sub> pin voltage with the greatest possible speed. This is orders of magnitude faster than most competing solutions, where a slow, average current loop is placed outside of the voltage regulation loop. By placing the av-

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average current loop inside of the voltage regulation loop, the LTC7103 allows for current programming on a nearly cycle-by-cycle basis.

The average output current can be monitored at the  $I_{MON}$  pin. The reconstructed inductor current signal ( $V_{SNS}$ ) is run through a low pass filter ( $f_c = 10\text{kHz}$ ), buffered, and then delivered to the  $I_{MON}$  pin. The voltage on the  $I_{MON}$  normally varies between 0.4V and 1.3V, corresponding to an average output current between 0A and 2.5A. The  $I_{MON}$  voltage may momentarily be less than 0.4V or greater than 1.3V, but eventually is limited to these levels by the average current loop. During SLEEP, this pin is held at 0.4V.

### Short-Circuit Protection and Minimum On-Time

The architecture of the LTC7103 provides inherent protection against short-circuit conditions, without the need for folding back either the output current or the oscillator frequency. This is made possible because the PWM comparator is continuously receiving inductor current information from the average current amplifier. This results in automatic cycle skipping under short-circuit conditions if the minimum on-time of the top switch is too long to maintain control of the inductor current at the full switching frequency. Because a given switching cycle is skipped only as needed to satisfy the high speed average current loop, this creates a brick-wall style current limit without any foldback or hiccups in the operation down to  $V_{OUT} = 0\text{V}$ . Figure 2 illustrates the typical operation of this brick-wall current limit.

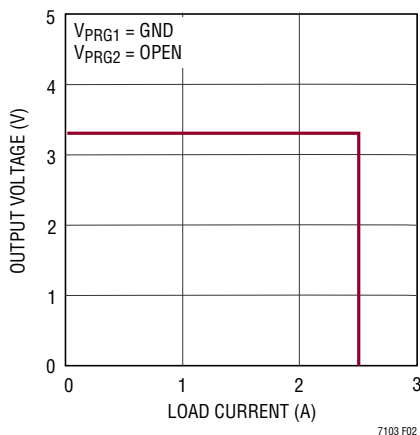


Figure 2. Typical Current Limit Operation

While the average current loop is extremely fast, a failsafe peak current limit ( $I_{PK}$ ) comparator has also been incorporated to ensure that the inductor current cannot exceed a safe level even momentarily. The peak current limit is internally set to 1.2A above the average current limit, and tracks with the average current limit set by the voltage on the  $I_{CTRL}$  pin. In practice, this peak current limit comparator is only needed when there is an abnormal voltage on the average current amplifier output filter and a short-circuit is simultaneously applied. In this case, the peak current limit comparator may be needed for a few cycles while the average current amplifier filter settles.

When operating at a high step-down ratio from  $V_{IN}$  to  $V_{OUT}$ , care should be taken to choose a switching frequency that is low enough to avoid operation at minimum on-time. However, in the event that a high step-down ratio requires the minimum on-time to be exceeded, the LTC7103 architecture offers inherent protection against output overvoltage. Once again, the PWM comparator will automatically cause the skipping of a cycle as needed to maintain regulation of the output voltage. While this avoids output overvoltage, operation in this mode is undesirable as it increases inductor current ripple.

In addition to this inherent protection, a separate output overvoltage comparator monitors the  $V_{FB}$  voltage and prevents top MOSFET turn-on if an overvoltage condition is present ( $V_{FB}$  exceeds  $V_{FB(OV)}$ ).

### Boost Supply and Dropout Operation

By making use of an internal charge pump, the LTC7103 is capable of operating at 100% duty cycle, providing the lowest possible dropout voltage and zero switching noise while in dropout. This charge pump delivers the small current required to maintain the static gate voltage on the top MOSFET switch when operating in dropout. When not operating in dropout, the gate drive voltage required for switching the top MOSFET switch is supplied by the charge pump formed by the BOOST capacitor ( $C_{BST}$ ), the bottom MOSFET switch, and an internal switch from  $INTV_{CC}$  to BOOST. As dropout is approached, the on-time

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of the bottom MOSFET switch is lengthened as needed to maintain an adequate supply to the floating gate driver between BOOST and SW.

### Power Good (PGOOD Pin)

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the internal feedback voltage ( $V_{FB1}$ ) is not within  $\pm 10\%$  of the 1V reference voltage. The PGOOD pin is also pulled low when the RUN pin is low (shutdown). When  $V_{FB1}$  is within the  $\pm 10\%$  requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 16V. There is a  $20\mu\text{s}$  delay ( $T_{PG}$ ) before the PGOOD pin goes low in response to the  $V_{FB1}$  voltage going outside of the  $\pm 10\%$  window.

### Overtemperature and Overvoltage Protection

In addition to the OVLO pin, which provides a user-adjustable protection against  $V_{IN}$  overvoltage, the LTC7103 contains an internal  $V_{IN}$  overvoltage shutdown feature. If the  $V_{IN}$  pin voltage exceeds 118.5V rising (112V falling), then the top and bottom MOSFETs are held off and all switching stops. Likewise, if the internal die temperature exceeds 171°C rising (155°C falling), then the LTC7103 disables switching as well as the LDO regulators until the temperature drops. Note that the internal overvoltage and overtemperature protection features are activated outside of the absolute maximum range of operation, and therefore should not be relied upon operationally. These features are only intended as a secondary failsafe to improve overall system reliability and safety.

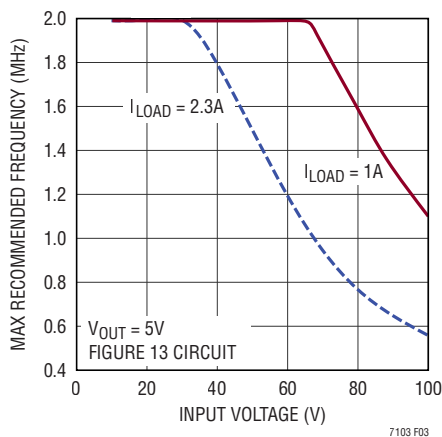


## APPLICATIONS INFORMATION

A general LTC7103 application circuit is shown on the first page of this data sheet. External component selection is largely driven by the load requirement and begins with the selection of the operating frequency and light load operating mode. Next, the inductor L is chosen, which also determines the value of resistor  $R_{IND}$ . After the inductor is chosen, the input capacitor  $C_{IN}$ , the output capacitor  $C_{OUT}$ , the internal regulator capacitor  $C_{VCC}$ , and the boost capacitor  $C_{BST}$ , can be selected. Next, either a fixed output voltage or feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as  $V_{IN}$  undervoltage/overvoltage lock-out, external soft-start, LDO regulator timeout, external loop compensation, average output current monitor and limit, and PGOOD.

### Setting the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage.



**Figure 3. Maximum Recommended Frequency vs Input Voltage**

For most LTC7103 applications, a good balance between size and efficiency is achieved with a switching frequency between 300kHz and 750kHz. Operating at higher switching frequencies up to 2MHz is readily possible, but switching

losses generally limit the input voltage to lower levels. This is illustrated in Figure 3, which shows the maximum recommended switching frequency versus input voltage at 1A and 2.3A loads for the application circuit of Figure 13. These lines correspond to a power loss of 2.5W in the LTC7103, which will result in a junction temperature rise of approximately 85°C without air flow. See Efficiency Considerations and Thermal Considerations sections for more information on calculating the power loss and temperature rise.

An additional constraint on operating frequency is the minimum controllable on-time of the LTC7103. While the architecture of the LTC7103 inherently maintains output voltage regulation even if the minimum on-time is exceeded, cycle-skipping will result in increased inductor current ripple. To avoid this, choose a switching frequency such that:

$$f < \frac{V_{OUT}}{V_{IN(MAX)} \cdot t_{ON(MIN)}}$$

The switching frequency is set using the FREQ and/or PLLIN/MODE pins as shown in Table 1.

**Table 1. Frequency Setting**

FREQ PIN	PLLIN/MODE PIN	FREQUENCY(F)
SGND	DC Voltage	300kHz
INTV <sub>CC</sub>	DC Voltage	1MHz
R = (f/40 + 7.5k) to SGND	DC Voltage	200kHz to 2MHz
Any of the Above	External Clock	Phase-Locked to External Clock (200kHz to 2MHz)

Tying the FREQ pin to SGND selects 300kHz while tying FREQ to INTV<sub>CC</sub> selects 1MHz. Since the FREQ pin sources 40μA, placing a resistor between FREQ and SGND allows the frequency to be programmed anywhere between 200kHz and 2MHz. Choose a FREQ pin resistor such that:

$$R_{FREQ} = \frac{f}{40} + 7.5k$$

A phase-locked loop (PLL) is also available on the LTC7103 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. Once

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synchronized, the turn-on of the top MOSFET is aligned to the rising edge of the synchronizing signal. See Phase-Locked Loop and Frequency Synchronization section for details.

### Setting the Light-Load Operating Mode

The LTC7103 can be set to enter high efficiency Burst Mode operation or constant frequency pulse-skipping mode at light load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground. To select pulse-skipping mode, tie the PLLIN/MODE pin to INTV<sub>CC</sub> through a 100k resistor. When synchronized, the LTC7103 operates in pulse-skipping mode. Table 2 summarizes the use of the PLLIN/MODE pin to select light-load operating mode.

**Table 2. Mode Selection**

PLLIN/MODE PIN	LIGHT-LOAD OPERATING MODE
SGND	Burst Mode Operation
R = 100k to INTV <sub>CC</sub>	Pulse-Skipping Mode
External Clock	Pulse-Skipping Mode

In general, the requirements of each application will dictate the appropriate choice for light-load operating mode.

In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the converter operates in discontinuous operation. In addition, when the average output current falls below approximately 200mA, the inductor current will begin bursting at frequencies lower than the switching frequency, and entering a low current SLEEP mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light loads.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst

Mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple and EMI.

In some applications, it may be desirable to change light-load operating mode based on the conditions present in the system. For example, if a system is inactive, one might select high efficiency Burst Mode operation by keeping the PLLIN/MODE pin set to 0V. When the system wakes, one might send an external clock to PLLIN/MODE, to switch to pulse-skipping mode. Such on-the-fly mode changes can allow an individual application to benefit from the advantages of each light-load operating mode.

### Inductor Value Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left( \frac{V_{OUT}}{f \cdot L} \right) \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of  $\Delta I_L$  allows the use of lower value inductors, but results in greater core loss in the inductor, greater ESR loss in the output capacitor, and larger output ripple. Generally, highest efficiency operation is obtained at low operating frequency with small ripple current.

A reasonable starting point for setting the ripple current is approximately 0.75A<sub>P-P</sub>. Note that the largest ripple current occurs at the highest V<sub>IN</sub>. To guarantee the ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left( \frac{V_{OUT}}{f \cdot \Delta I_{L(MAX)}} \right) \left( 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

The LTC7103 contains a fast, average current limit loop that limits the DC output current to a value determined by the voltage on the I<sub>CTRL</sub> pin. (See Average Output Current Limit and Monitor section for details.) However, some ap-

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Applications may experience inductor current transients that are limited by the peak current limit comparator, which tracks nominally 1.2A above the average current limit set point. To avoid saturation, choose an inductor with a saturation current  $I_{SAT}$  such that:

$$I_{SAT} > \frac{V_{ICTRL} - 0.4}{0.36} + 1.5A$$

This enables the use of an inductor with a current rating that fits the needs of a given application. If the average output current limit is set to the default value of 2.5A, then an inductor with  $I_{SAT} > 4A$  is required. However, if the average current limit is set to 1.5A, then an inductor with  $I_{SAT} > 3A$  may be used. Note that if there is a varying voltage on the  $I_{CTRL}$  pin, always uses the highest value present on  $I_{CTRL}$  when calculating the required inductor saturation current.

If fixed  $V_{OUT}$  operation is selected using the  $V_{PRG1}$  and  $V_{PRG2}$  pins, the  $R_{IND}$  pin can be left floating, but only if the inductance value is chosen according to Table 3. Since the  $R_{IND}$  pin resistor indicates the inductance value being used, the LTC7103 will automatically assume an inductance value as shown in Table 3 when this pin is left floating. These inductance values will provide an inductor ripple current that is approximately 30% to 40% of the full load current. If the nominal value of the inductance used differs by more than 10% from the values specified in Table 3, a resistor must be placed on the  $R_{IND}$  pin to indicate this value.

**Table 3. Required Inductor Values with  $R_{IND}$  Pin Floating**

FIXED $V_{OUT}$	REQUIRED INDUCTANCE VALUE ( $R_{IND} = \text{FLOAT}$ )		
	f = 300kHz	f = 1MHz	f = ADJ
1.2V	3.9 $\mu$ H	1.2 $\mu$ H	L = 1.1/f
1.8V	5.6 $\mu$ H	1.8 $\mu$ H	L = 1.7/f
2.5V	8.2 $\mu$ H	2.5 $\mu$ H	L = 2.5/f
3.3V	12 $\mu$ H	3.3 $\mu$ H	L = 3.6/f
3.6V	12 $\mu$ H	3.3 $\mu$ H	L = 3.6/f
5V	18 $\mu$ H	5.6 $\mu$ H	L = 5.4/f
12V	47 $\mu$ H	15 $\mu$ H	L = 14/f
15V	47 $\mu$ H	15 $\mu$ H	L = 14/f

### Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value but is very dependent on the inductance selected. As the inductance increases, core loss decreases. Unfortunately, increased inductance requires more turns of wire leading to increased copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials saturate hard, meaning the inductance collapses abruptly when the peak design current is exceeded. This collapse will result in an abrupt increase in inductor ripple current, so it is important to ensure the core will not saturate.

### $R_{IND}$ Resistor Selection

The resistor on the  $R_{IND}$  pin is used to indicate to the LTC7103 what inductance value is being used. This is required for the internal reconstruction of the inductor current waveform and to set the DC gain of the current loop. Once the inductor value is selected, the  $R_{IND}$  pin resistor is chosen according to:

$$R_{IND} = \frac{1}{7.5 \cdot L}$$

If fixed  $V_{OUT}$  operation is selected using the  $V_{PRG1}$  and  $V_{PRG2}$  pins, the  $R_{IND}$  pin can be left floating, but only if the inductance value is chosen according to Table 3. Do not leave the  $R_{IND}$  pin floating when adjustable  $V_{OUT}$  mode is selected. If the  $R_{IND}$  pin is left floating and adjustable  $V_{OUT}$  mode selected ( $V_{PRG1}$  and  $V_{PRG2}$  are both floating), the LTC7103 will detect this as a fault condition and will not operate.

The allowable current range on the  $R_{IND}$  pin is between 8 $\mu$ A and 220 $\mu$ A, which means that:

$$1.1 \leq f \cdot L \leq 30$$

In practice, the above constraint does not normally affect the choice of inductor value.

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### $C_{IN}$ Selection

The input capacitance,  $C_{IN}$ , is needed to filter the trapezoidal current at the drain of the top power MOSFET.  $C_{IN}$  should be sized to do this without causing a large variation in input voltage. In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of:

$$I_{RMS} = \frac{I_{OUT(MAX)}}{2}$$

Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7103, ceramic capacitors can also be used for  $C_{IN}$ . In many applications, an X7R capacitor of 4.7 $\mu$ F or greater is a suitable choice. Always consult the manufacturer if there is any question.

The input capacitor,  $C_{IN}$ , should be placed as close as possible to the  $V_{IN}$  pins, with a low inductance connection to the PGND (paddle) of the IC. In addition to a larger bulk capacitor, a smaller case-size (0603 or 0805) ceramic decoupling capacitor can be placed closer to the  $V_{IN}$  pins to reduce EMI.

### Using an LC Input Filter

For high voltage applications, it can be costly to use bulk capacitance that is rated to handle the required RMS input current. Moreover, when using a simple capacitor to filter the AC input current, it is difficult to determine exactly where this AC current is flowing when a power supply is placed into a larger system. To avoid these issues, an LC filter can be used on the power supply input as shown in Figure 4. This keeps the higher AC currents contained in a relatively small and inexpensive capacitor ( $C_F$ ) whose RMS current rating is known to be adequate. Choose an LC filter such that:

$$\frac{1}{2\pi\sqrt{L_F C_F}} < \frac{f}{5}$$

where  $f$  is the switching frequency. This will attenuate the RMS input current by a factor of approximately 5X, greatly alleviating the RMS input requirements of the larger bulk capacitor  $C_{BULK}$ . The filter inductor  $L_F$  should have a saturation current of at least:

$$I_{SAT(LF)} \geq 1.3 \cdot \frac{V_{OUT} I_{OUT(MAX)}}{V_{IN(MIN)}}$$

In order to keep the ripple voltage at the filter output to a reasonable level, choose a value of  $L_F$  and  $C_F$  that also satisfies:

$$\sqrt{\frac{L_F}{C_F}} < 2.9 \cdot \left( \frac{V_{RIPPLE}}{I_{OUT(MAX)}} + \frac{R_{ESR}}{2} \right)$$

where  $V_{RIPPLE}$  is the desired ripple voltage at the output of the input filter and  $R_{ESR}$  is the ESR of capacitor  $C_F$ . A reasonable target for  $V_{RIPPLE}$  is 3% of nominal  $V_{IN}$ .

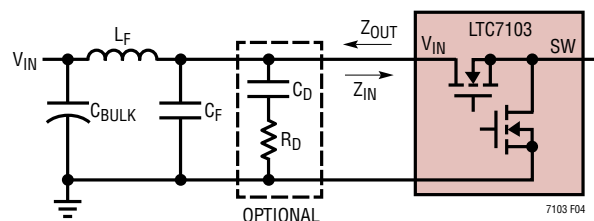


Figure 4. Input Filter with Optional Damping Network

When using an LC input filter, the output impedance of the LC filter ( $Z_{OUT}$ ) must never be greater in magnitude than the input impedance looking into the power stage of the DC/DC converter ( $Z_{IN}$ ). This is necessary to avoid ringing and possible voltage loop instability. In many applications, this condition is naturally satisfied because the ESR of the bulk input capacitance  $C_{BULK}$  is high enough to lower the Q of the LC input filter. In some situations, a series damping network must be added as shown in Figure 4. In order to provide critical damping, choose  $C_D$  and  $R_D$  according to:

$$C_D \approx 4 \cdot C_F$$

$$R_D = \sqrt{\frac{L_F}{C_F}}$$

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### C<sub>OUT</sub> Selection

The selection of C<sub>OUT</sub> is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV<sub>OUT</sub>) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left( ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right)$$

where f is the operating frequency, C<sub>OUT</sub> is the output capacitance and ΔI<sub>L</sub> is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI<sub>L</sub> increases with input voltage.

If internal voltage loop compensation is selected, than a minimum amount of bulk output capacitance is required to ensure stability. Loop stability can be checked by viewing the load transient response. See Internal/External Loop Compensation in the Applications Information section.

### Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now available in small case sizes. Their high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input, and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V<sub>IN</sub> input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V<sub>IN</sub> large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors select the X5R or X7R dielectric formulations. These dielectrics provide the best temperature and voltage characteristics for a given value and size. In addition, be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

### INTV<sub>CC</sub> Regulators

The LTC7103 features two separate internal low dropout linear regulators (LDO) that supply power at the INTV<sub>CC</sub> pin from either the V<sub>IN</sub> pin or the EXTV<sub>CC</sub> pin depending on the EXTV<sub>CC</sub> pin voltage available. INTV<sub>CC</sub> powers the internal MOSFET gates and most of the internal circuitry. The V<sub>IN</sub> LDO and the EXTV<sub>CC</sub> LDO each regulate INTV<sub>CC</sub> to 3.5V.

The INTV<sub>CC</sub> pin must be bypassed to ground with a minimum of 1μF ceramic capacitor, placed as close as possible to the INTV<sub>CC</sub> pin. In order to minimize noise and ripple on the INTV<sub>CC</sub> supply, always use a capacitor C<sub>VCC</sub> on INTV<sub>CC</sub> that is at least 10x greater than the capacitor C<sub>BST</sub> from BOOST to SW:

$$C_{VCC} > 10 \cdot C_{BST}$$

Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

For high V<sub>IN</sub> applications it is advantageous to tie EXTV<sub>CC</sub> to V<sub>OUT</sub> (bootstrapping), as this will improve efficiency and reduce power dissipation in the V<sub>IN</sub> LDO. This can be done with any V<sub>OUT</sub> voltage between 3.3V and 40V. Alternatively, the EXTV<sub>CC</sub> pin can be tied to any DC voltage between 3.3V and 40V that is capable of delivering the required INTV<sub>CC</sub> bias current, which varies with switching frequency and operating mode. At full-load operation, which is the worst case, the INTV<sub>CC</sub> bias current is given approximately by:

$$I_{INTVCC} = 4mA + 1nC \left( 8 + \frac{V_{IN}}{20} \right) \cdot f$$

When EXTV<sub>CC</sub> is not present, the LDO timeout feature limits the junction temperature rise due to the V<sub>IN</sub> LDO power dissipation. See Soft-Start and LDO Regulator Timeout section for more information.

The following list summarizes the four possible connections for EXTV<sub>CC</sub>:

1. EXTV<sub>CC</sub> left open (or grounded). This will cause INTV<sub>CC</sub> to be powered from the V<sub>IN</sub> LDO resulting in an efficiency penalty at high input voltages.



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- EXTV<sub>CC</sub> connected directly to the output voltage V<sub>OUT</sub>. This is the normal connection for a 3.3V to 40V regulator and provides the highest efficiency.
- EXTV<sub>CC</sub> connected to an external supply. If an external supply is available in the 3.3V to 40V range, it may be used to power EXTV<sub>CC</sub> providing it can supply the required INTV<sub>CC</sub> current. Operating with EXTV<sub>CC</sub> > V<sub>IN</sub> is allowed.
- EXTV<sub>CC</sub> connected to an output-derived boost or charge-pump network. For 2.5V and other low voltage buck regulators, efficiency gains can still be realized by connecting EXTV<sub>CC</sub> to an output-derived voltage that has been boosted to greater than 3.05V.

Most applications will simply tie EXTV<sub>CC</sub> to V<sub>OUT</sub> for high efficiency bootstrapping. In this configuration, with Burst Mode operation selected, the no-load V<sub>IN</sub> current in regulation can be calculated using:

$$I_{VIN} = 1\mu\text{A} + \frac{V_{OUT}}{0.8 \cdot V_{IN}} \cdot \left( \frac{V_{OUT}}{R_D} + \frac{V_{OUT}}{6\text{M}\Omega} + 8\mu\text{A} \right)$$

where R<sub>D</sub> is the total resistance of the feedback resistive divider from V<sub>OUT</sub> to GND. In fixed output voltage mode, where V<sub>OUT</sub> is programmed using V<sub>PRG1</sub> and V<sub>PRG2</sub>, use R<sub>D</sub> = V<sub>OUT</sub>/1.25μA. For adjustable V<sub>OUT</sub> mode (Figure 5), use R<sub>D</sub> = R1 + R2.

### Topside MOSFET Driver Supply (C<sub>BST</sub>)

The boost capacitor, C<sub>BST</sub>, on the Functional Diagram is used to create a voltage rail above the applied input voltage, V<sub>IN</sub>. Specifically, the boost capacitor is charged through an internal MOSFET switch to a voltage equal to approximately INTV<sub>CC</sub> each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOST pin voltage will be equal to approximately V<sub>IN</sub> + 3.5V. For most applications a 0.1μF, X7R ceramic capacitor will provide adequate performance.

The LTC7103 also contains an internal charge pump that supplies a small amount of current to the BOOST pin to allow for continuous operation at 100% duty cycle. This charge pump is adequate to support internal biasing needs and to keep the top MOSFET fully enhanced. Note that the total external leakage on the BOOST pin (including the C<sub>BST</sub> capacitor leakage) must be less than 4μA to ensure continuous operation at 100% duty cycle.

### Output Voltage Programming

The V<sub>PRG1</sub> and V<sub>PRG2</sub> pins provide a great deal of flexibility in programming the output voltage of the power supply. Floating both pins selects adjustable V<sub>OUT</sub> mode. In this mode, the output is programmed using external resistors on the V<sub>FB</sub> pin as shown in Figure 5. The regulated output voltage is determined by:

$$V_{OUT} = 1\text{V} \left( 1 + \frac{R1}{R2} \right)$$

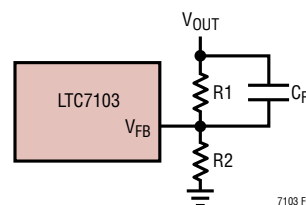


Figure 5. Setting the Output Voltage

Place resistors R1 and R2 very close to the V<sub>FB</sub> pin to minimize PCB trace length and noise. Great care should be taken to route the V<sub>FB</sub> trace away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feedforward capacitor (C<sub>FF</sub>) may be used.

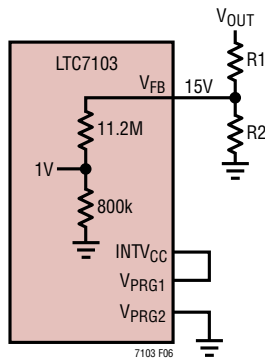
If either V<sub>PRG1</sub> or V<sub>PRG2</sub> is tied to SGND or INTV<sub>CC</sub>, then fixed output voltage mode is selected. In this mode, precision internal resistor dividers are used to program the output voltage to one of eight fixed voltage levels as shown in Table 4.

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**Table 4. Output Voltage Programming**

V <sub>PRG1</sub>	V <sub>PRG2</sub>	V <sub>OUT</sub>
INTV <sub>CC</sub>	INTV <sub>CC</sub>	1.2V
OPEN	INTV <sub>CC</sub>	1.8V
SGND	SGND	2.5V
SGND	OPEN	3.3V
SGND	INTV <sub>CC</sub>	3.6V
OPEN	SGND	5V
INTV <sub>CC</sub>	OPEN	12V
INTV <sub>CC</sub>	SGND	15V
OPEN	OPEN	Adjustable 1V to V <sub>IN</sub>

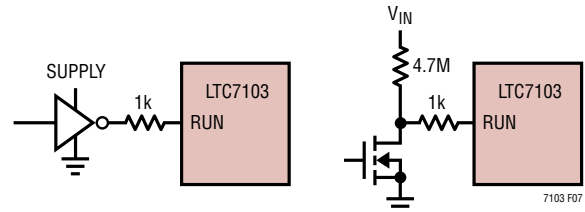
To avoid excessively large values of R1 in high output voltage applications (V<sub>OUT</sub> ≥ 15V), a combination of external and internal resistors can be used to set the output voltage. Figure 6 shows the LTC7103 with the V<sub>FB</sub> pin configured for a 15V fixed output with an external divider to generate a higher output voltage. The internal 12M resistance appears in parallel with R2, and the value of R2 must be adjusted accordingly. R2 should be chosen to be less than 400k to keep the output voltage variation less than 1% due to the tolerance of the LTC7103's internal resistor.



**Figure 6. Setting the Output Voltage with External and Internal Resistors**

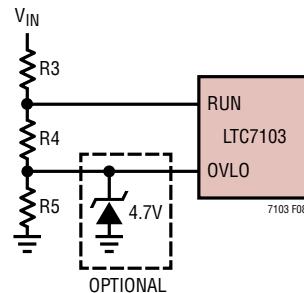
### RUN Pin and Overvoltage/Undervoltage Lockout

The LTC7103 has a low power shutdown mode controlled by the RUN pin. Pulling the RUN pin below 0.7V puts the LTC7103 into a low quiescent current shutdown mode (I<sub>Q</sub> = 0.7μA). When the RUN pin is greater than V<sub>RUN(ON)</sub> = 1.21V, switching is enabled. Figure 7 shows examples of configurations for driving the RUN pin from logic.



**Figure 7. RUN Pin Interface to Logic**

The RUN and OVLO pins can alternatively be configured as precise undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V<sub>IN</sub> supply with a resistor divider from V<sub>IN</sub> to ground. A simple resistor divider can be used as shown in Figure 8 to meet specific V<sub>IN</sub> voltage requirements.



**Figure 8. Adjustable UV and OV Lockout**

The current that flows through the R3-R4-R5 divider will directly add to the shutdown, sleep, and active current of the LTC7103, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R4 + R5 (R<sub>TOTAL</sub>) should be chosen first based on the allowable DC current that can be drawn from V<sub>IN</sub>. The individual values of R3, R4 and R5 can then be calculated from the following equations:

$$R5 = R_{TOTAL} \cdot \frac{1.21V}{\text{RISING } V_{IN} \text{ OVLO THRESHOLD}}$$

$$R4 = R_{TOTAL} \cdot \frac{1.21V}{\text{RISING } V_{IN} \text{ UVLO THRESHOLD}} - R5$$

$$R3 = R_{TOTAL} - R5 - R4$$

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For applications that do not need a precise external OVLO, the OVLO pin should be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the previous equations with  $R5 = 0\Omega$ .

Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to  $V_{IN}$ . In this configuration, the UVLO threshold is limited to the internal  $V_{IN}$  UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the previous equations with  $R3 = 0\Omega$ . Be aware that the OVLO pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the OVLO pin from exceeding 6V, the following relation should be satisfied:

$$V_{IN(MAX)} \cdot \left( \frac{R5}{R3+R4+R5} \right) < 6V$$

If this equation cannot be satisfied in the application, connect a 4.7V Zener diode between the OVLO pin and ground to clamp the OVLO pin voltage as shown in Figure 8.

### Soft-Start and LDO Regulator Timeout

An internal soft-start ramp of 1.2ms will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, a capacitor can be placed from the SS pin to ground. The value of the soft-start capacitor needed to provide a desired soft-start time ( $t_{SS}$ ) can be calculated by:

$$C_{SS} = t_{SS} \cdot 10\mu A$$

Note that the value of  $C_{SS}$  must be greater than 12nF to provide a soft-start time that is greater than the internal default of  $t_{SS(INT)} = 1.2ms$ .

The LTC7103 also includes an LDO regulator timeout feature that is essential for limiting die temperature rise due to power dissipation in the  $V_{IN}$  LDO. This is useful in high  $V_{IN}$  applications, where  $EXTV_{CC}$  is tied to  $V_{OUT}$ , and  $V_{OUT}$  gets shorted to ground. When this occurs, the  $V_{IN}$  LDO will take over the  $INTV_{CC}$  current, resulting in potentially high power dissipation ( $>1W$ ) in the  $V_{IN}$  LDO

pass device. If this condition persists, an LDO timeout occurs, disabling the switching of the top and bottom MOSFETs. Once switching is disabled, the  $INTV_{CC}$  bias current is reduced to approximately 4mA, thereby lowering the power dissipation in the LDO. After a long restart delay, a soft-start is again initiated.

The LDO regulator timeout and restart time are dependent on the length of the soft-start time selected,  $t_{SS}$ , which is either the default of 1.2ms or set externally. After the soft-start is complete, a timeout will occur if  $EXTV_{CC} < 3V$  for a time given by:

$$t_{TIMEOUT} = 1.4 \cdot t_{SS}$$

At this point, switching will stop, and a restart delay timer will be activated. A restart will occur after a delay given by:

$$t_{RESTART} = 46 \cdot t_{SS}$$

As long as this condition persists ( $EXTV_{CC} < 3V$ ), the LTC7103 will continue operating in a hiccup restart mode. This yields an effective duty cycle of power dissipation in the  $V_{IN}$  LDO of approximately 2%, which prevents any significant rise in die temperature. Note, however, that the LDO regulator timeout feature precludes operation in constant output current mode in applications where  $EXTV_{CC}$  is tied to  $V_{OUT}$ , and  $V_{OUT} < 3V$ .

If the LDO regulator timeout feature is not needed, the SS pin can be tied to  $INTV_{CC}$  through a 75k resistor. This will prevent the LDO timeout from occurring, allowing continuous operation even with  $EXTV_{CC} = 0V$ . The addition of this resistor also affects the soft-start time when an external capacitor is used (the internal 1.2ms soft-start is not affected). With SS tied to  $INTV_{CC}$  through 75k, the value of the soft-start capacitor needed to provide a desired soft-start time ( $t_{SS}$ ) can be calculated by:

$$C_{SS(75k)} = t_{SS} \cdot 51\mu A$$

If the LDO regulator timeout feature is defeated, care must be taken to avoid exceeding the maximum junction temperature. See Thermal Considerations for more information.