



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



FEATURES

- Synchronous Boost and Buck Controllers
- When Cascaded, Allows V_{IN} Above, Below, or Equal to Regulated V_{OUT} of Up to 60V
- Wide Bias Input Voltage Range: 4.5V to 60V
- Output Remains in Regulation Through Input Dips (e.g. Cold Crank) Down to 2.2V
- Adjustable Gate Drive Level 5V to 10V (OPTI-DRIVE)
- Low EMI with Low Input and Output Ripple
- Fast Output Transient Response
- No External Bootstrap Diodes Required
- High Light Load Efficiency
- Low Operating I_Q : 29 μ A (One Channel On)
- Low Operating I_Q : 34 μ A (Both Channels On)
- R_{SENSE} or Lossless DCR Current Sensing
- Buck Output Voltage Range: $0.8V \leq V_{OUT} \leq 60V$
- Boost Output Voltage Up to 60V
- Phase-Lockable Frequency (75kHz to 850kHz)
- Small 32-Pin 5mm \times 5mm QFN Package

APPLICATIONS

- Automotive and Industrial Power Systems
- High Power Battery Operated Systems

DESCRIPTION

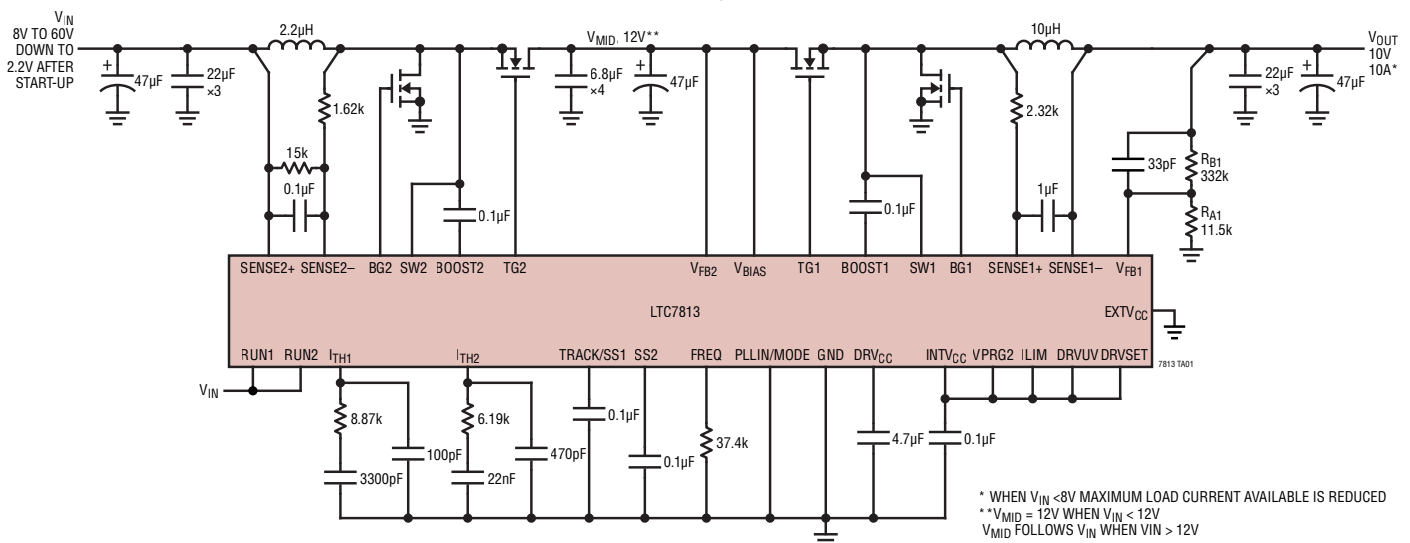
The LTC7813 is a high performance synchronous Boost+Buck DC/DC switching regulator controller that drives all N-channel power MOSFET stages. It contains independent step-up (boost) and step-down (buck) controllers that can regulate two separate outputs or be cascaded to regulate an output voltage from an input voltage that can be above, below, or equal to the output voltage. The LTC7813 operates from a wide 4.5V to 60V input supply range. When biased from the output of the boost regulator, the LTC7813 can operate from an input supply as low as 2.2V after start-up. The 34 μ A no-load quiescent current (both channels on) extends operating runtime in battery-powered systems.

Unlike conventional buck-boost regulators, the LTC7813's cascaded Boost+Buck solution has continuous, non-pulsating, input and output currents, substantially reducing voltage ripple and EMI. The LTC7813 has independent feedback and compensation points for the boost and buck regulation loops, enabling a fast output transient response that can be externally optimized.

LT, LT, LTC, LTM, Linear Technology, the Linear logo and Burst Mode are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

Wide Input Range to 10V/10A Low I_Q Cascaded Boost+Buck Regulator



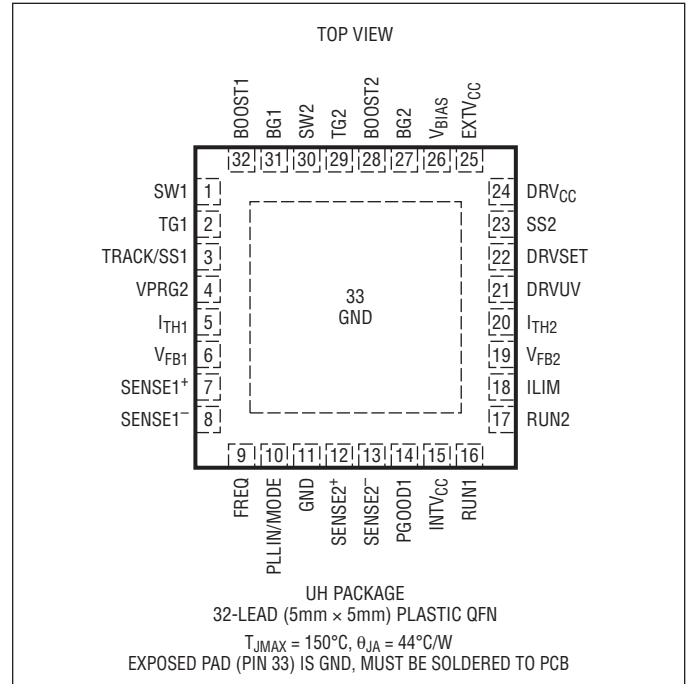
LTC7813

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Bias Input Supply Voltage (V_{BIAS}).....	-0.3V to 65V
Topside Driver Voltages	
BOOST1, BOOST2.....	-0.3V to 76V
Switch Voltage (SW1, SW2).....	-5V to 70V
DRV_{CC} , (BOOST1-SW1), (BOOST2-SW2)....	-0.3V to 11V
BG1, BG2, TG1, TG2.....	(Note 8)
RUN1, RUN2 Voltages.....	-0.3V to 65V
SENSE1 ⁺ , SENSE2 ⁺ , SENSE1 ⁻	
SENSE2 ⁻ Voltages.....	-0.3V to 65V
PLLIN/MODE, FREQ, DRVSET Voltages.....	-0.3V to 6V
EXTV _{CC} Voltage.....	-0.3V to 14V
ITH1, ITH2, V_{FB1} Voltages.....	-0.3V to 6V
V_{FB2} Voltage.....	-0.3V to 65V
VPRG2 Voltage.....	-0.3V to 6V
TRACK/SS1, SS2 Voltages.....	-0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3)	
LTC7813E, LTC7813I.....	-40°C to 125°C
LTC7813H.....	-40°C to 150°C
LTC7813MP.....	-55°C to 150°C
Storage Temperature Range.....	-65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7813EUH#PBF	LTC7813EUH#TRPBF	7813	32-Lead (5mm × 5mm) Plastic QFN	-40°C to 125°C
LTC7813IUH#PBF	LTC7813IUH#TRPBF	7813	32-Lead (5mm × 5mm) Plastic QFN	-40°C to 125°C
LTC7813HUH#PBF	LTC7813HUH#TRPBF	7813	32-Lead (5mm × 5mm) Plastic QFN	-40°C to 150°C
LTC7813MPUH#PBF	LTC7813MPUH#TRPBF	7813	32-Lead (5mm × 5mm) Plastic QFN	-55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 2) $V_{\text{BIAS}} = 12\text{V}$, $V_{\text{RUN1,2}} = 5\text{V}$, $V_{\text{EXTVCC}} = 0\text{V}$, $V_{\text{DRVSET}} = 0\text{V}$, $V_{\text{PRG2}} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{BIAS}	Bias Input Supply Operating Voltage Range		4.5		60	V	
V_{OUT1}	Buck Regulated Output Voltage Set Point		0.8		60	V	
V_{OUT2}	Boost Regulated Output Voltage Set Point				60	V	
$V_{\text{SENSE2(CM)}}$	SENSE2 Pins Common Mode Range (BOOST Converter Input Supply Voltage)		2.2		60	V	
V_{FB1}	Buck Regulated Feedback Voltage	(Note 4) ITH1 Voltage = 1.2V 0°C to 85°C	● 0.792 ● 0.788	0.800 0.800	0.808 0.812	V V	
V_{FB2}	Boost Regulated Feedback Voltage	(Note 4) ITH2 Voltage = 1.2V VPRG2 = 0V VPRG2 = FLOAT VPRG2 = INTV _{CC}	● 1.182 ● 9.78 ● 11.74	1.200 10.00 12.00	1.218 10.22 12.26	V V V	
I_{FB1}	Buck Feedback Current	(Note 4)		-2	±50	nA	
I_{FB2}	Boost Feedback Current	(Note 4) VPRG2 = 0V VPRG2 = FLOAT VPRG2 = INTV _{CC}		±0.01 4 5	±0.05 6 7	μA μA μA	
	Reference Voltage Line Regulation	(Note 4) $V_{\text{BIAS}} = 4.5\text{V}$ to 60V		0.002	0.02	%/V	
	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔITH Voltage = 1.2V to 0.7V	●	0.01	0.1	%	
		(Note 4) Measured in Servo Loop, ΔITH Voltage = 1.2V to 2V	●	-0.01	-0.1	%	
$g_{\text{m1,2}}$	Transconductance Amplifier g_{m}	(Note 4) ITH1,2 = 1.2V, Sink/Source 5μA		2		mmho	
I_{Q}	Input DC Supply Current	(Note 5), $V_{\text{DRVSET}} = 0\text{V}$					
	Pulse-Skipping or Forced Continuous Mode (One Channel On)	RUN1 = 5V and RUN2 = 0V or RUN2 = 5V and RUN1 = 0V $V_{\text{FB1}} = 0.83\text{V}$ (No Load), $V_{\text{FB2}} = 1.25\text{V}$ (No Load)		1.6 0.8		mA mA	
	Pulse-Skipping or Forced Continuous Mode (Both Channels On)	RUN1,2 = 5V, $V_{\text{FB1}} = 0.83\text{V}$ (No Load), $V_{\text{FB2}} = 1.25\text{V}$ (No Load)		2.2		mA	
	Sleep Mode (One Channel On, Buck)	RUN1 = 5V and RUN2 = 0V $V_{\text{FB1}} = 0.83\text{V}$ (No Load)	●	29	55	μA	
	Sleep Mode (One Channel On, Boost)	RUN2 = 5V and RUN1 = 0V, $V_{\text{FB2}} = 1.25\text{V}$ (No Load)		29	50	μA	
	Sleep Mode (Both Channels On)	RUN1 = 5V and RUN2 = 5V, $V_{\text{FB1}} = 0.83\text{V}$ (No Load), $V_{\text{FB2}} = 1.25\text{V}$ (No Load)		34	55	μA	
	Shutdown	RUN1,2 = 0V		3.6	10	μA	
UVLO	Undervoltage Lockout	DRV _{CC} Ramping Up DRVUV = 0V DRVUV = INTV _{CC}	● ●	4.0 7.5	4.2 7.8	V V	
		DRV _{CC} Ramping Down DRVUV = 0V DRVUV = INTV _{CC}	● ●	3.6 6.4	3.8 6.7	4.0 7.0	V V
	Buck Feedback Overvoltage Protection	Measured at V_{FB1} Relative to Regulated V_{FB1}		7	10	13	%
	SENSE1+ Pin Current				±1	μA	
	SENSE2+ Pin Current			170		μA	
	SENSE1- Pin Current	$V_{\text{SENSE1-}} < V_{\text{INTVCC}} - 0.5\text{V}$ $V_{\text{SENSE1-}} > V_{\text{INTVCC}} + 0.5\text{V}$		700		±1	μA μA
	SENSE2- Pin Current	$V_{\text{SENSE2+}}, V_{\text{SENSE2-}} = 12\text{V}$				±1	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 2) $V_{\text{BIAS}} = 12\text{V}$, $V_{\text{RUN1,2}} = 5\text{V}$, $V_{\text{EXTVCC}} = 0\text{V}$, $V_{\text{DRVSET}} = 0\text{V}$, $V_{\text{PRG2}} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Maximum Duty Factor for TG	Buck (Channel 1) in Dropout, $\text{FREQ} = 0\text{V}$ Boost (Channel 2)	97.5	99 100		% %
	Maximum Duty Factor for BG	Buck (Channel 1) in Overvoltage Boost (Channel 2)		100 96		% %
$I_{\text{TRACK/SS1}}$	Soft-Start Charge Current	$V_{\text{TRACK/SS1}} = 0\text{V}$	8	10	12	μA
I_{SS2}	Soft-Start Charge Current	$V_{\text{SS2}} = 0\text{V}$	8	10	12	μA
$V_{\text{RUN1,2 ON}}$	RUN Pin On Threshold	V_{RUN1} , V_{RUN2} Rising	● 1.22	1.275	1.33	V
	RUN Pin Hysteresis			75		mV
$V_{\text{SENSE1,2(MAX)}}$	Maximum Current Sense Threshold	$I_{\text{LIM}} = \text{Float}$ $I_{\text{LIM}} = 0\text{V}$ $I_{\text{LIM}} = \text{INTVCC}$	● 65 ● 43 ● 90	75 50 100	85 58 109	mV mV mV

Gate Driver

TG1,2	Pull-Up On-Resistance Pull-Down On-Resistance	$V_{\text{DRVSET}} = \text{INTVCC}$		2.2 1.0		Ω Ω
BG1,2	Pull-Up On-Resistance Pull-Down On-Resistance	$V_{\text{DRVSET}} = \text{INTVCC}$		2.2 1.0		Ω Ω
	BOOST1,2 to DRVCC Switch On-Resistance	$V_{\text{SW1,2}} = 0\text{V}$, $V_{\text{DRVSET}} = \text{INTVCC}$		3.7		Ω
	TG Transition Time: Rise Time Fall Time	(Note 6) $V_{\text{DRVSET}} = \text{INTVCC}$ $C_{\text{LOAD}} = 3300\text{pF}$ $C_{\text{LOAD}} = 3300\text{pF}$		25 15		ns ns
	BG Transition Time: Rise Time Fall Time	(Note 6) $V_{\text{DRVSET}} = \text{INTVCC}$ $C_{\text{LOAD}} = 3300\text{pF}$ $C_{\text{LOAD}} = 3300\text{pF}$		25 15		ns ns
	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	$C_{\text{LOAD}} = 3300\text{pF}$ Each Driver, $V_{\text{DRVSET}} = \text{INTVCC}$ Buck (Channel 1) Boost (Channel 2)		55 85		ns ns
	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	$C_{\text{LOAD}} = 3300\text{pF}$ Each Driver, $V_{\text{DRVSET}} = \text{INTVCC}$ Buck (Channel 1) Boost (Channel 2)		50 80		ns ns
$t_{\text{ON(MIN)1}}$	Buck Minimum On-Time	(Note 7) $V_{\text{DRVSET}} = \text{INTVCC}$		80		ns
$t_{\text{ON(MIN)2}}$	Boost Minimum On-Time	(Note 7) $V_{\text{DRVSET}} = \text{INTVCC}$		120		ns

DRVCC Linear Regulator

	DRVCC Voltage from Internal V_{BIAS} LDO	$V_{\text{EXTVCC}} = 0\text{V}$ $7\text{V} < V_{\text{BIAS}} < 60\text{V}$, $\text{DRVSET} = 0\text{V}$ $11\text{V} < V_{\text{BIAS}} < 60\text{V}$, $\text{DRVSET} = \text{INTVCC}$	5.8 9.6	6.0 10.0	6.2 10.4	V V
	DRVCC Load Regulation from V_{BIAS} LDO	$I_{\text{CC}} = 0\text{mA}$ to 50mA , $V_{\text{EXTVCC}} = 0\text{V}$		0.9	2.0	%
	DRVCC Voltage from Internal EXTVCC LDO	$7\text{V} < V_{\text{EXTVCC}} < 13\text{V}$, $\text{DRVSET} = 0\text{V}$ $11\text{V} < V_{\text{EXTVCC}} < 13\text{V}$, $\text{DRVSET} = \text{INTVCC}$	5.8 9.6	6.0 10.0	6.2 10.4	V V
	DRVCC Load Regulation from Internal EXTVCC LDO	$I_{\text{CC}} = 0\text{mA}$ to 50mA , $V_{\text{EXTVCC}} = 8.5\text{V}$, $V_{\text{DRVSET}} = 0\text{V}$		0.7	2.0	%
	EXTVCC LDO Switchover Voltage	EXTVCC Ramping Positive $\text{DRVSET} = 0\text{V}$ or $R_{\text{DRVSET}} \leq 100\text{k}\Omega$ $\text{DRVSET} = \text{INTVCC}$	4.5 7.4	4.7 7.7	4.9 8.0	V V
	EXTVCC Hysteresis			250		mV
	Programmable DRVCC	$R_{\text{DRVSET}} = 50\text{k}\Omega$, $V_{\text{EXTVCC}} = 0\text{V}$		5.0		V
	Programmable DRVCC	$R_{\text{DRVSET}} = 70\text{k}\Omega$, $V_{\text{EXTVCC}} = 0\text{V}$	6.4	7.0	7.6	V
	Programmable DRVCC	$R_{\text{DRVSET}} = 90\text{k}\Omega$, $V_{\text{EXTVCC}} = 0\text{V}$		9.0		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 2) $V_{\text{BIAS}} = 12\text{V}$, $V_{\text{RUN1,2}} = 5\text{V}$, $V_{\text{EXTVCC}} = 0\text{V}$, $V_{\text{DRVSET}} = 0\text{V}$, $V_{\text{PRG2}} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop						
	Programmable Frequency	$R_{\text{FREQ}} = 25\text{k}\Omega$, PLLIN/MODE = DC Voltage		105		kHz
	Programmable Frequency	$R_{\text{FREQ}} = 65\text{k}\Omega$, PLLIN/MODE = DC Voltage	375	440	505	kHz
	Programmable Frequency	$R_{\text{FREQ}} = 105\text{k}\Omega$, PLLIN/MODE = DC Voltage		835		kHz
	Low Fixed Frequency	$V_{\text{FREQ}} = 0\text{V}$, PLLIN/MODE = DC Voltage	320	350	380	kHz
	High Fixed Frequency	$V_{\text{FREQ}} = \text{INTV}_{\text{CC}}$, PLLIN/MODE = DC Voltage	485	535	585	kHz
	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75	850	kHz
PLLIN V_{IH}	PLLIN/MODE Input High Level	PLLIN/MODE = External Clock	●	2.5		V
PLLIN V_{IL}	PLLIN/MODE Input Low Level	PLLIN/MODE = External Clock	●		0.5	V
BOOST2 Charge Pump						
	BOOST2 Charge Pump Available Output Current	FREQ = 0V, PLLIN/MODE = INTV_{CC} $V_{\text{BOOST2}} = 16.5\text{V}$, $V_{\text{SW2}} = 12\text{V}$ $V_{\text{BOOST2}} = 19\text{V}$, $V_{\text{SW2}} = 12\text{V}$		75 35		μA μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

Note 2: The LTC7813 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7813E is guaranteed to meet performance specifications from 0°C to 85°C . Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7813I is guaranteed over the -40°C to 125°C operating junction temperature range, the LTC7813H is guaranteed over the -40°C to 150°C operating junction temperature range and the LTC7813MP is tested and guaranteed over the -55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C . Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J , in $^\circ\text{C}$) is calculated from the ambient temperature (T_A , in $^\circ\text{C}$) and power dissipation (P_D , in Watts) according to the formula:

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

where $\theta_{JA} = 44^\circ\text{C}$.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The LTC7813 is tested in a feedback loop that servos $V_{\text{ITH1,2}}$ to a specified voltage and measures the resultant $V_{\text{FB1,2}}$. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC7813E and LTC7813I, 150°C for the LTC7813H and LTC7813MP). For the LTC7813I and LTC7813H, the specification at 0°C is not tested in production and is assured by design, characterization and correlation to production testing at -40°C . For the LTC7813MP, the specification at 0°C is not tested in production and is assured by design, characterization and correlation to production testing at -55°C .

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications information.

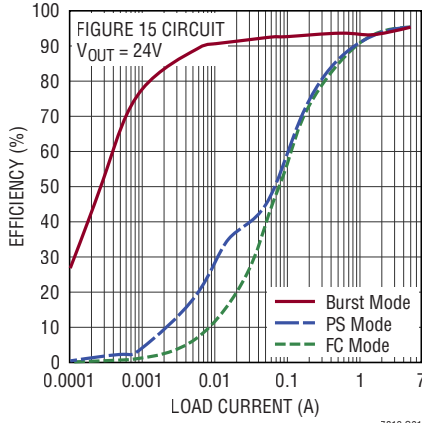
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current $>40\%$ of I_{MAX} (See Minimum On-Time Considerations in the Applications Information section).

Note 8: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

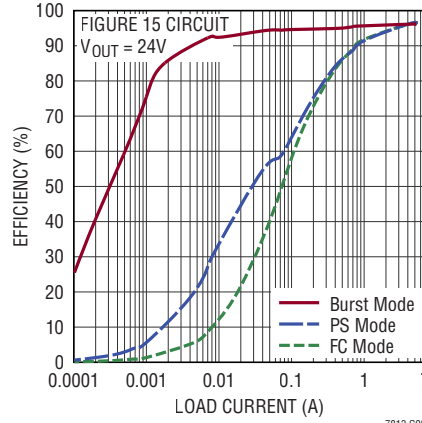
**Efficiency vs Load Current,
 $V_{IN} = 18V$**



PS = PULSE-SKIPPING
FC = FORCED CONTINUOUS

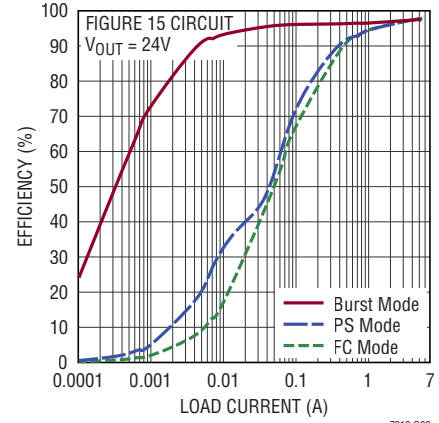
7813 G01

**Efficiency vs Load Current,
 $V_{IN} = 24V$**



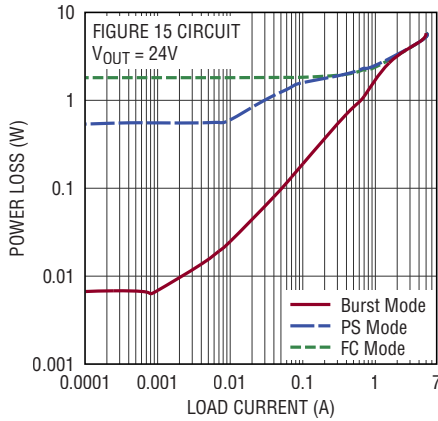
7813 G02

**Efficiency vs Load Current,
 $V_{IN} = 36V$**



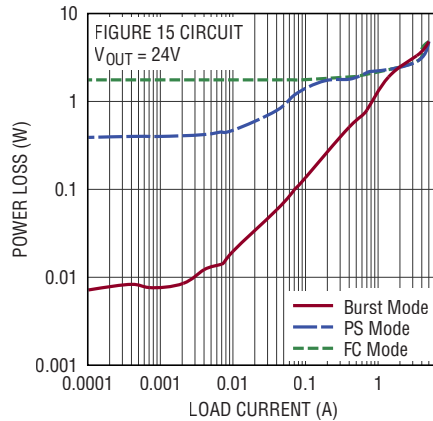
7813 G03

**Power Loss vs Load Current,
 $V_{IN} = 18V$**



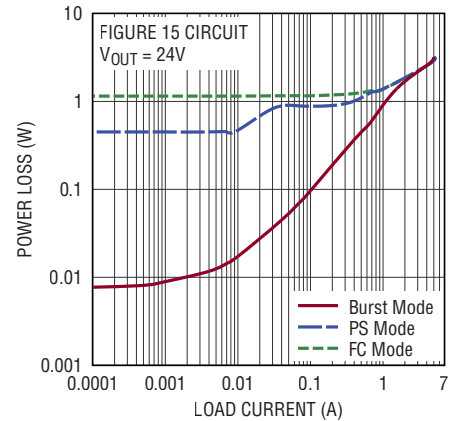
7813 G04

**Power Loss vs Load Current,
 $V_{IN} = 24V$**



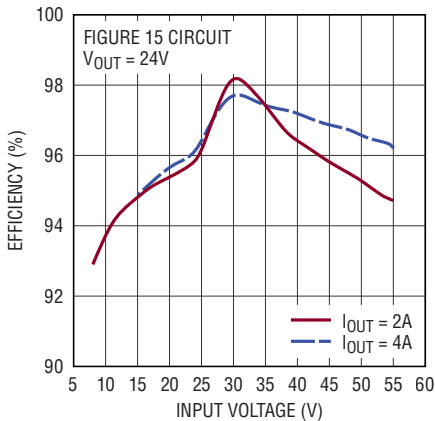
7813 G05

**Power Loss vs Load Current,
 $V_{IN} = 36V$**



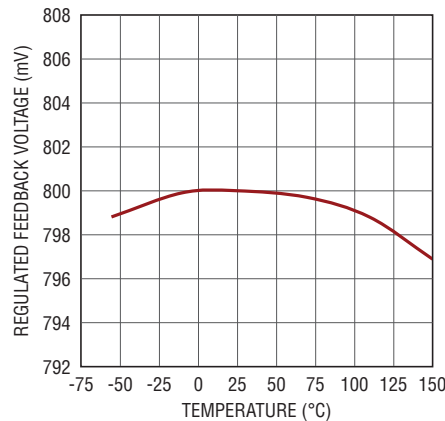
7813 G06

Efficiency vs Input Voltage



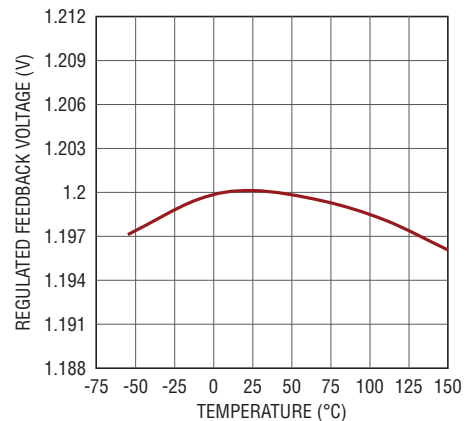
7813 G07

**Buck Regulated Feedback Voltage
vs Temperature**



7813 G08

**Boost Regulated Feedback
Voltage vs Temperature**



7813 G09

TYPICAL PERFORMANCE CHARACTERISTICS

**Load Step at $V_{IN} = 18V$,
Burst Mode Operation**

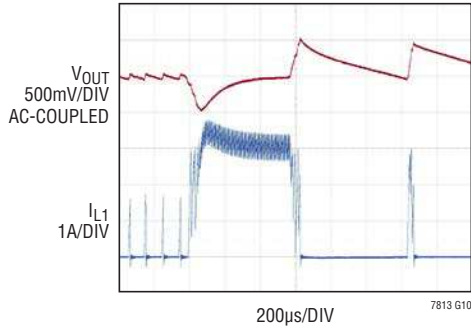


FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

**Load Step at $V_{IN} = 24V$,
Burst Mode Operation**

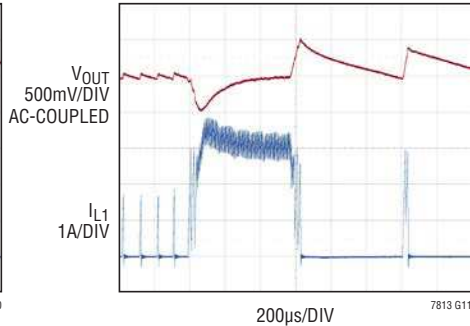


FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

**Load Step at $V_{IN} = 36V$,
Burst Mode Operation**

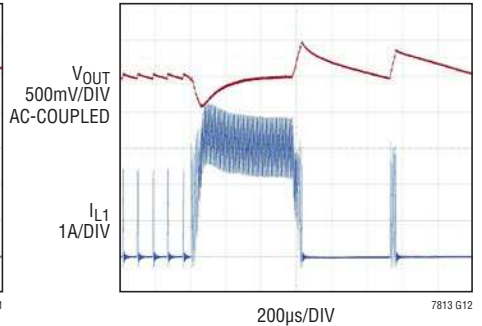


FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

**Load Step at $V_{IN} = 18V$,
Pulse-Skipping Mode**

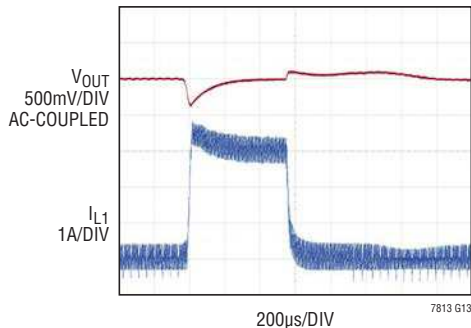


FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

**Load Step at $V_{IN} = 24V$,
Pulse-Skipping Mode**

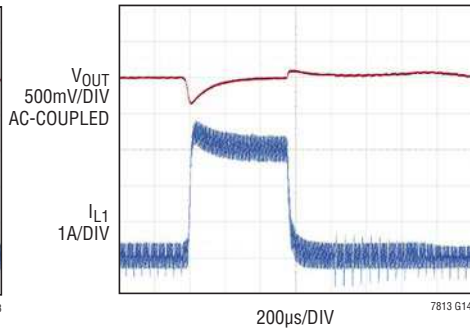


FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

**Load Step at $V_{IN} = 36V$,
Pulse-Skipping Mode**

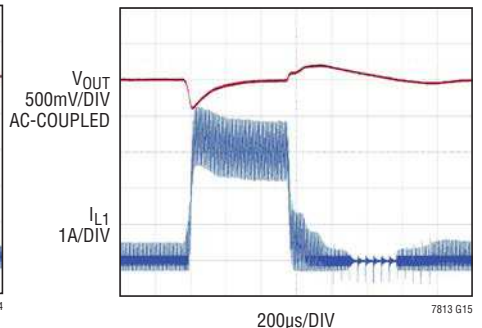


FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

**Load Step at $V_{IN} = 18V$,
Forced Continuous Mode**

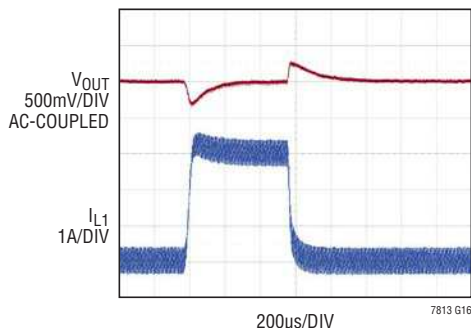


FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

**Load Step at $V_{IN} = 24V$,
Forced Continuous Mode**

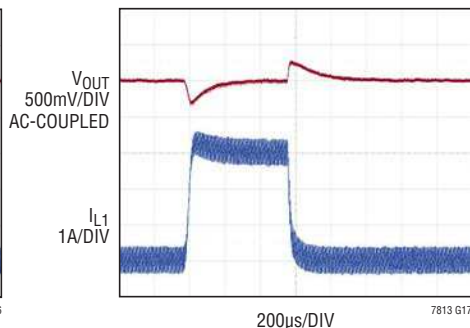


FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

**Load Step at $V_{IN} = 36V$,
Forced Continuous Mode**

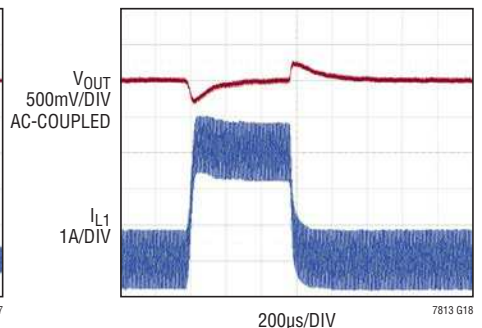
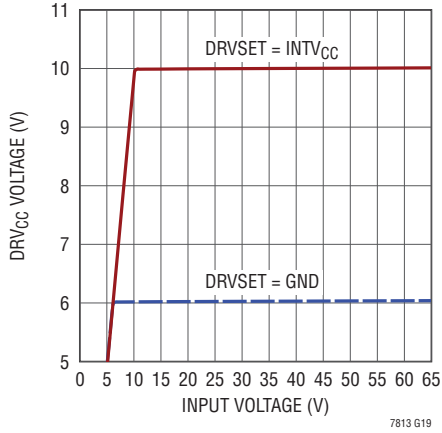


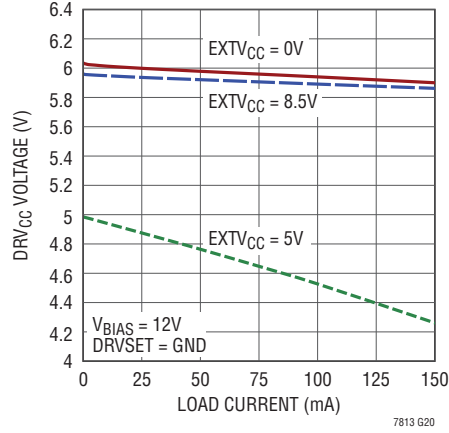
FIGURE 15 CIRCUIT
 $V_{OUT} = 24V$

TYPICAL PERFORMANCE CHARACTERISTICS

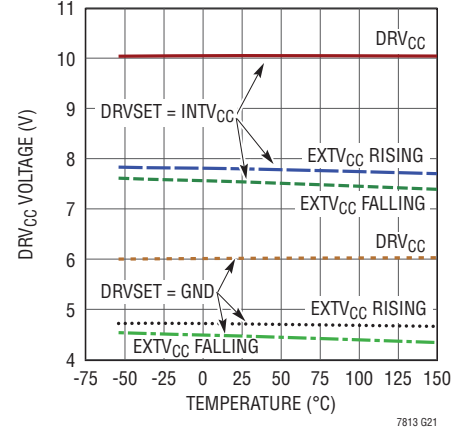
DRV_{CC} Line Regulation



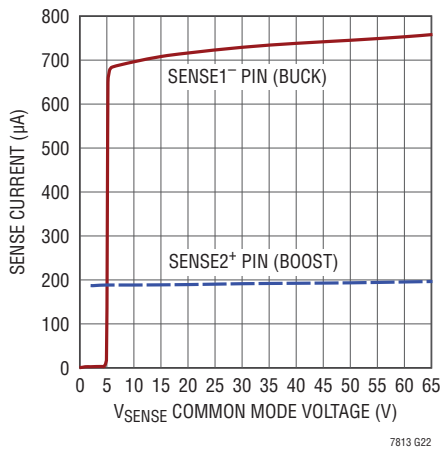
DRV_{CC} and EXTV_{CC} vs Load Current



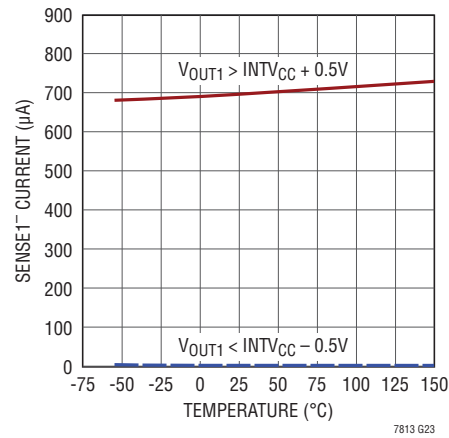
EXTV_{CC} Switchover and DRV_{CC} Voltages vs Temperature



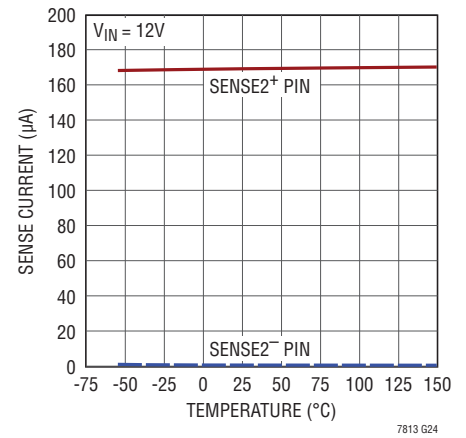
SENSE Pins Input Current vs V_{SENSE} Voltage



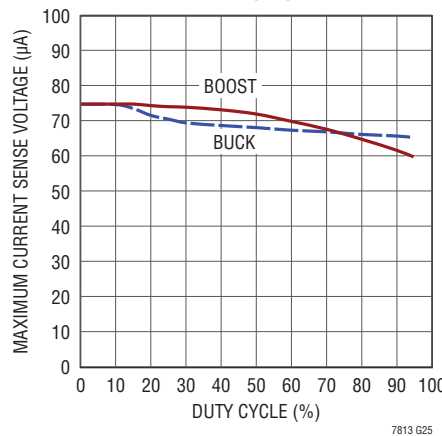
Buck SENSE1⁻ Pin Input Bias Current vs Temperature



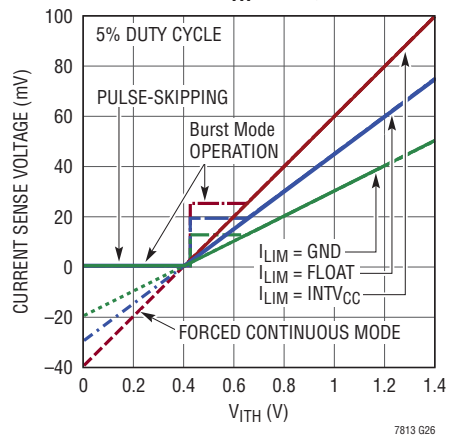
Boost SENSE2⁺ Pins Input Current vs Temperature



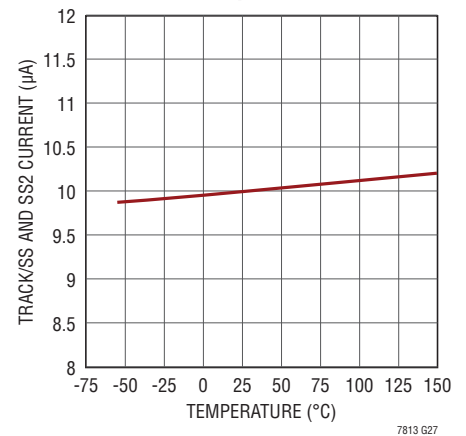
Maximum Current Sense Threshold vs Duty Cycle



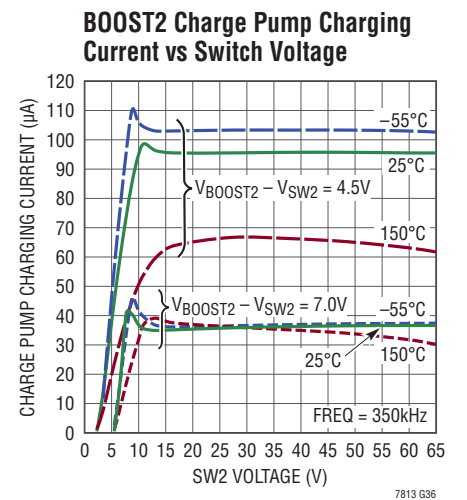
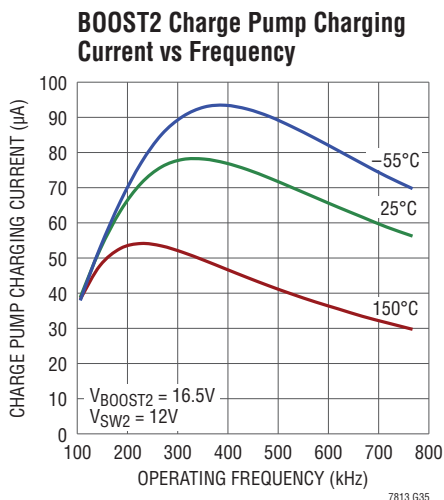
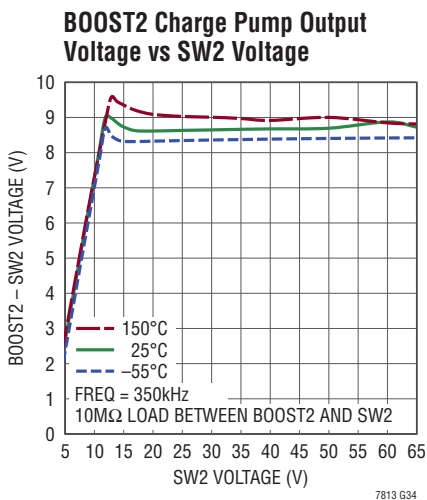
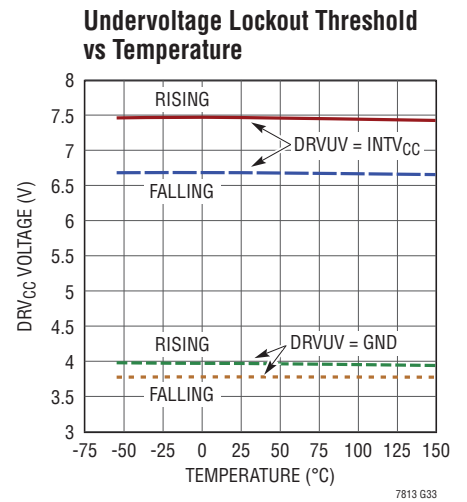
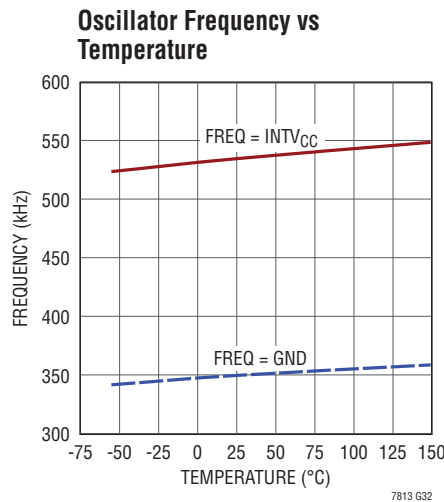
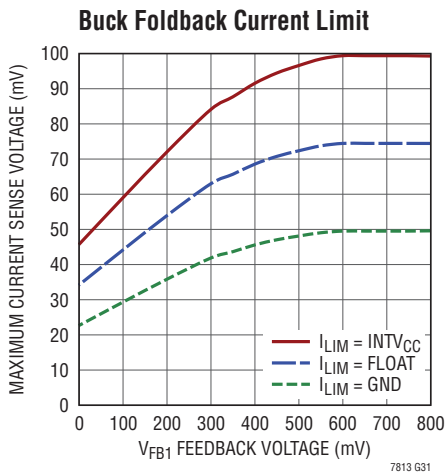
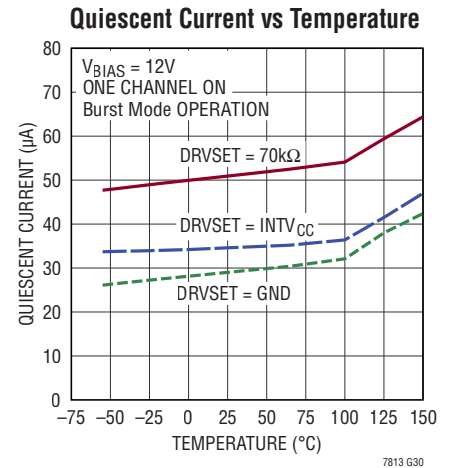
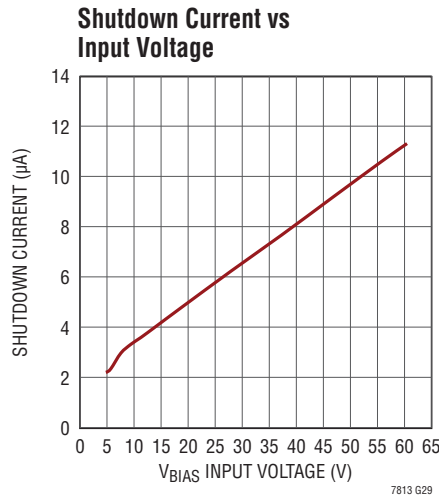
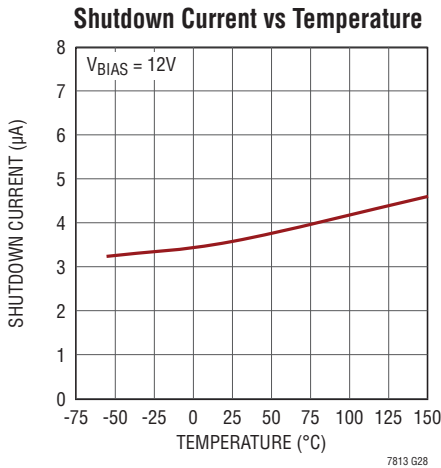
Maximum Current Sense Threshold vs I_{TH} Voltage



TRACK/SS1 and SS2 Pull-Up Current vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up

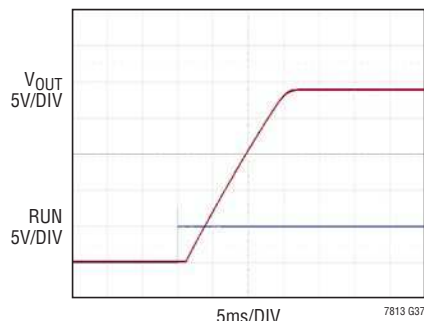


FIGURE 15 CIRCUIT

7813 G37

Buck Inductor Current at Light Load

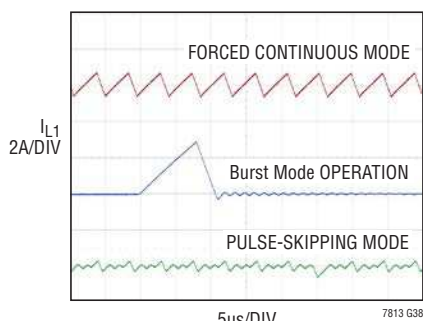


FIGURE 15 CIRCUIT

$V_{IN} = 32V$
 $V_{OUT} = 24V$
 $I_{OUT} = 1mA$

7813 G38

Boost Inductor Current at Light Load

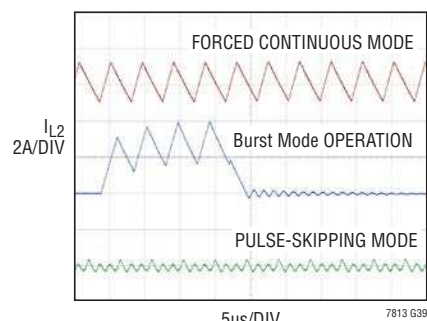


FIGURE 15 CIRCUIT

$V_{IN} = 18V$
 $V_{OUT} = 24V$
 $I_{OUT} = 1mA$

7813 G39

PIN FUNCTIONS

SW1, SW2 (Pins 1, 30): Switch Node Connections to Inductors.

TG1, TG2 (Pins 2, 29): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to DRV_{CC} superimposed on the switch node voltage SW.

TRACK/SS1, SS2 (Pins 3, 23): External Tracking and Soft-Start Input. For the buck channel, the LTC7813 regulates the V_{FB1} voltage to the smaller of 0.8V, or the voltage on the TRACK/SS1 pin. For the boost channel, the LTC7813 regulates the V_{FB2} voltage to the smaller of 1.2V, or the voltage on the SS2 pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to the TRACK/SS1 pin allows the LTC7813 buck output to track the other supply during start-up.

VPRG2 (Pin 4): Channel 2 Output Control Pin. This pin sets the boost channel to adjustable output mode using external feedback resistors or fixed 10V/12V output mode using internal resistive dividers. Grounding this pin allows the output to be programmed through the V_{FB2} pin using external resistors, regulating V_{FB2} to the 1.2V reference. Floating this pin or connecting it to $INTV_{CC}$ programs the output to 10V or 12V (respectively), with V_{FB2} used to sense the output voltage.

ITH1, ITH2 (Pins 5, 20): Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage.

V_{FB1} (Pin 6): This pin receives the remotely sensed feedback voltage for the buck controller from an external resistive divider across the output.

SENSE1+, SENSE2+ (Pins 7, 12): The (+) Input to the Differential Current Comparators. The ITH pin voltage and controlled offsets between the SENSE⁻ and SENSE⁺ pins in conjunction with R_{SENSE} set the current trip threshold. For the boost channel, the SENSE2⁺ pin supplies current to the current comparator.

SENSE1-, SENSE2- (Pins 8, 13): The (-) Input to the Differential Current Comparators. When SENSE1⁻ for the buck channel is greater than $INTV_{CC}$, the SENSE1⁻ pin supplies current to the current comparator.

FREQ (Pin 9): The frequency control pin for the internal VCO. Connecting this pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting this pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed using a resistor between FREQ and GND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency.

7813f

PIN FUNCTIONS

PLLIN/MODE (Pin 10): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, the phase-locked loop will force the rising TG1 and BG2 signals to be synchronized with the rising edge of the external clock, and the regulators will operate in forced continuous mode. When not synchronizing to an external clock, this input, which acts on both controllers, determines how the LTC7813 operates at light loads. Pulling this pin to ground selects Burst Mode® operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to INTV_{CC} forces continuous inductor current operation. Tying this pin to a voltage greater than 1.1V and less than INTV_{CC} – 1.3V selects pulse-skipping operation. This can be done by connecting a 100k resistor from this pin to INTV_{CC}.

GND (Pin 11, Exposed Pad Pin 33): Ground. The exposed pad must be soldered to the PCB for rated electrical and thermal performance.

PGOOD1 (Pin 14): Open-Drain Logic Output. PGOOD1 is pulled to ground when the voltage on the V_{FB1} pin is not within ±10% of its set point.

INTV_{CC} (Pin 15): Output of the Internal 5V Low Dropout Regulator. The low voltage analog and digital circuits are powered from this voltage source. A low ESR 0.1μF ceramic bypass capacitor should be connected between INTV_{CC} and GND, as close as possible to the IC.

RUN1, RUN2 (Pins 16, 17): Run Control Inputs for Each Controller. Forcing either of these pins below 1.2V shuts down that controller. Forcing both of these pins below 0.7V shuts down the entire LTC7813, reducing quiescent current to approximately 3.6μA.

ILIM (Pin 18): Current Comparator Sense Voltage Range Input. Tying this pin to GND or INTV_{CC} or floating it sets the maximum current sense threshold (for both channels) to one of three different levels (50mV, 100mV, or 75mV, respectively).

V_{FB2} (Pin 19): If VPRG2 is grounded, this pin receives the remotely sensed feedback voltage for the boost controller from an external resistive divider across the output. If VPRG2 is floated or tied to INTV_{CC}, this pin receives the remotely sensed output voltage of the boost controller.

DRVUV (Pin 21): Determines the higher or lower DRV_{CC} UVLO and EXTV_{CC} switchover thresholds, as listed on the Electrical Characteristics table. Connecting DRVUV to GND chooses the lower thresholds whereas tying DRVUV to INTV_{CC} chooses the higher thresholds.

DRVSET (Pin 22): Sets the regulated output voltage of the DRV_{CC} LDO regulator. Connecting this pin to GND sets DRV_{CC} to 6V whereas connecting it to INTV_{CC} sets DRV_{CC} to 10V. Voltages between 5V and 10V can be programmed by placing a resistor (50k to 100k) between the DRVSET pin and GND.

DRV_{CC} (Pin 24): Output of the Internal or External Low Dropout (LDO) Regulator. The gate drivers are powered from this voltage source. The DRV_{CC} voltage is set by the DRVSET pin. Must be decoupled to ground with a minimum of 4.7μF ceramic or other low ESR capacitor. Do not use the DRV_{CC} pin for any other purpose.

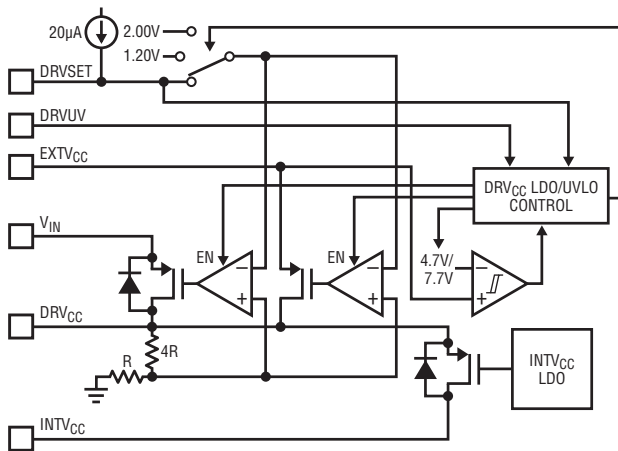
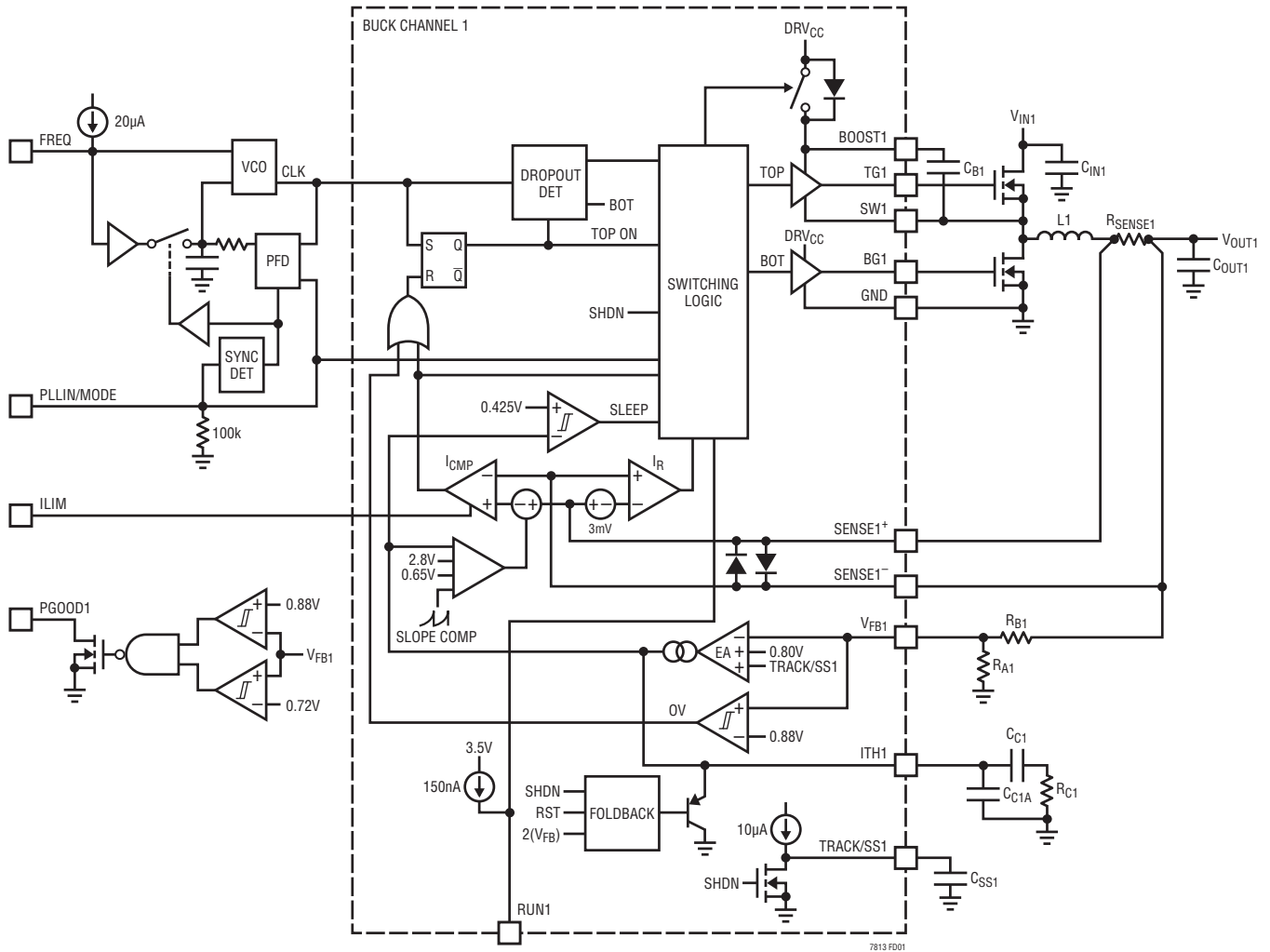
EXTV_{CC} (Pin 25): External Power Input to an Internal LDO Connected to DRV_{CC}. This LDO supplies DRV_{CC} power, bypassing the internal LDO powered from V_{BIAS} whenever EXTV_{CC} is higher than its switchover threshold (4.7V or 7.7V depending on the DRVSET pin). See EXTV_{CC} Connection in the Applications Information section. Do not float or exceed 14V on this pin. Do not connect EXTV_{CC} to a voltage greater than V_{BIAS}. Connect to GND if not used.

V_{BIAS} (Pin 26): Main Supply Pin. A bypass capacitor should be tied between this pin and the GND pin.

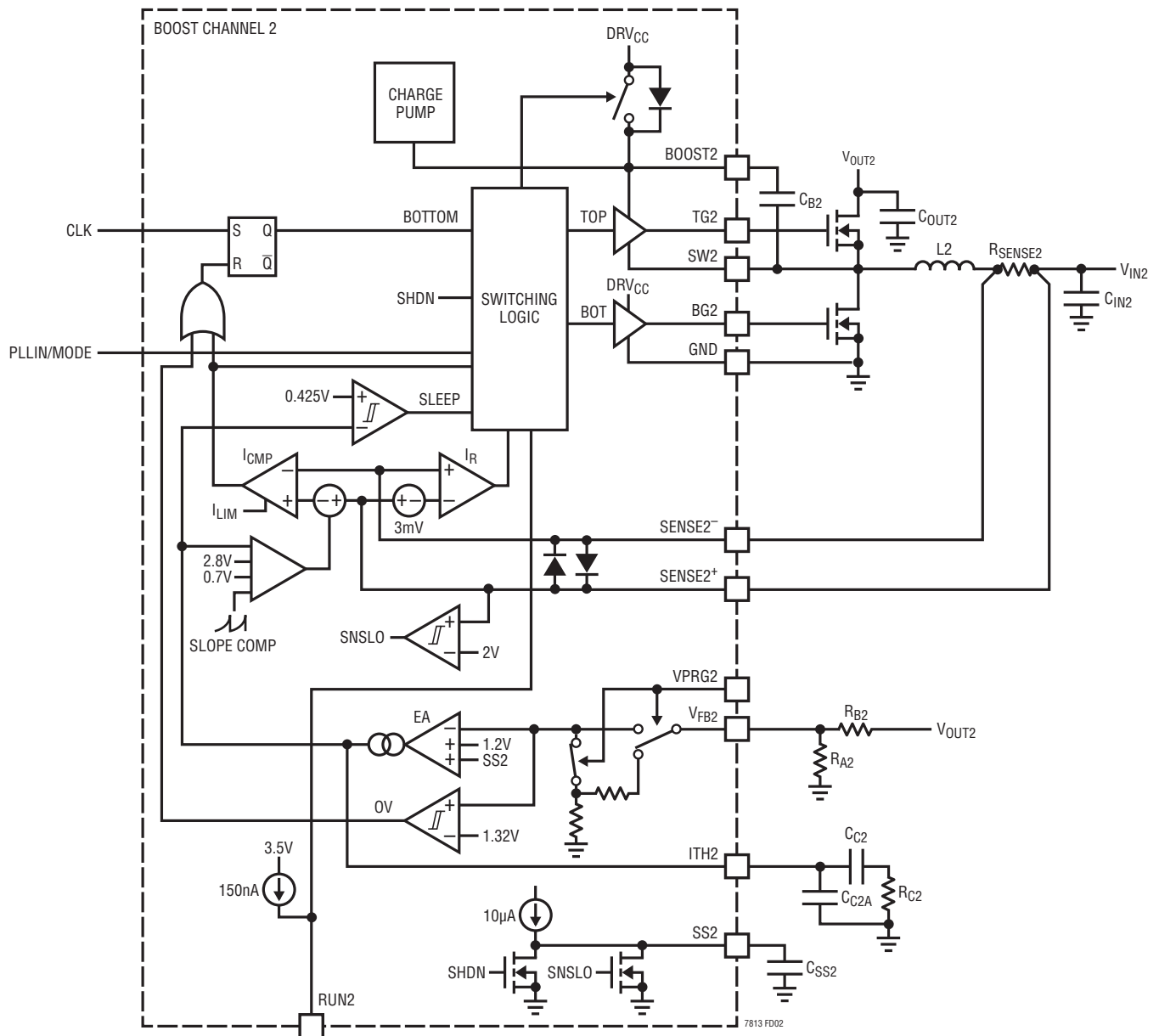
BG1, BG2 (Pins 31, 27): High Current Gate Drives for Bottom N-Channel MOSFETs. Voltage swing at these pins is from ground to DRV_{CC}.

BOOST1, BOOST2 (Pins 32, 28): Bootstrapped Supplies to the Topside Floating Drivers. Capacitors are connected between the BOOST and SW pins. Voltage swing at BOOST1 is from approximately DRV_{CC} to (V_{IN1} + DRV_{CC}). Voltage swing at BOOST2 is from approximately DRV_{CC} to (V_{OUT2} + DRV_{CC}).

FUNCTIONAL DIAGRAMS



FUNCTIONAL DIAGRAMS



OPERATION (Refer to the Functional Diagrams)

Main Control Loop

The LTC7813 uses a constant frequency, current mode control architecture. Channel 1 is a buck (step-down) controller, and channel 2 is a boost (step-up) controller. During normal operation, the external top MOSFET for the buck channel (the external bottom MOSFET for the boost controller) is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, I_{CMP} , resets the RS latch. The peak inductor current at which I_{CMP} trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT} , to ground) to the internal 0.800V reference voltage (1.2V reference voltage for the boost). When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET for the buck (the bottom MOSFET for the boost) is turned off each cycle, the bottom MOSFET is turned on (the top MOSFET for the boost) until either the inductor current starts to reverse, as indicated by the current comparator I_R , or the beginning of the next clock cycle.

DRV_{CC}/EXTV_{CC}/INTV_{CC} Power

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} supply voltage can be programmed from 5V to 10V through control of the DRVSET pin. When the EXTV_{CC} pin is tied to a voltage below its switchover voltage (4.7V or 7.7V depending on the DRVUV voltage), the V_{BIAS} LDO (low dropout linear regulator) supplies power from V_{BIAS} to DRV_{CC}. If EXTV_{CC} is taken above its switchover voltage, the V_{BIAS} LDO is turned off and an EXTV_{CC} LDO is turned on. Once enabled, the EXTV_{CC} LDO supplies power from EXTV_{CC} to DRV_{CC}. Using the EXTV_{CC} pin allows the DRV_{CC} power to be derived from a high efficiency external source such as the LTC7813 buck regulator output.

Each top MOSFET driver is biased from the floating bootstrap capacitor, C_B , which normally recharges during each cycle through an internal switch whenever SW goes low.

For buck channel 1, if the input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period every tenth cycle to allow C_B to recharge, resulting in about 99% duty cycle.

The INTV_{CC} supply powers most of the other internal circuits in the LTC7813. The INTV_{CC} LDO regulates to a fixed value of 5V and its power is derived from the DRV_{CC} supply.

Shutdown and Start-Up (RUN, TRACK/SS Pins)

The two channels of the LTC7813 can be independently shut down using the RUN1 and RUN2 pins. Pulling a RUN pin below 1.22V shuts down the main control loop for that channel. Pulling both pins below 0.7V disables both controllers and most internal circuits, including the DRV_{CC} and INTV_{CC} LDOs. In this state, the LTC7813 draws only 3.6 μ A of quiescent current.

Releasing a RUN pin allows a small 150nA internal current to pull up the pin to enable that controller. Each RUN pin may be externally pulled up or driven directly by logic. Each RUN pin can tolerate up to 65V (absolute maximum), so it can be conveniently tied to V_{BIAS} in always-on applications where one or both controllers are enabled continuously and never shut down.

The start-up of each controller's output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, SS2 for channel 2). When the voltage on the TRACK/SS pin is less than the 0.8V internal reference for the buck and the 1.2V internal reference for the boost, the LTC7813 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the corresponding reference voltage. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to GND. An internal 10 μ A pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V/1.2V (and beyond up to about 4V), the output voltage V_{OUT} rises smoothly from zero (V_{IN} for the boost) to its final value.

OPERATION (Refer to the Functional Diagrams)

Alternatively the TRACK/SS1 pin for the buck channel can be used to cause the start-up of V_{OUT1} to track that of another supply. Typically, this requires connecting to the TRACK/SS1 pin an external resistor divider from the other supply to ground (see the Applications Information section).

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Forced Continuous Mode) (PLLIN/MODE Pin)

The LTC7813 can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to GND. To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.1V and less than $INTV_{CC} - 1.3V$. This can be done by connecting a 100k Ω resistor between PLLIN/MODE and $INTV_{CC}$.

When a controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of the maximum sense voltage (30% for the boost) even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC7813 draws. If one channel is in sleep mode and the other is shut down, the LTC7813 draws only 29 μ A of quiescent current (with $DRVSET = 0V$). If both controllers are enabled in sleep mode, the LTC7813 draws only 34 μ A of quiescent current. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET (the bottom external MOSFET for the boost) on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_R) turns off the bottom external MOSFET (the top external MOSFET for the boost) just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates discontinuously.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current. Clocking the LTC7813 from an external source enables forced continuous mode (see the Frequency Selection and Phase-Locked Loop section).

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC7813 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, I_{CMP} , may remain tripped for several cycles and force the external top MOSFET (bottom for the boost) to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

OPERATION (Refer to the Functional Diagrams)

The switching frequency of the LTC7813's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to GND, tied to INTV_{CC} or programmed through an external resistor. Tying FREQ to GND selects 350kHz while tying FREQ to INTV_{CC} selects 535kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 10.

A phase-locked loop (PLL) is available on the LTC7813 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC7813's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of TG1 and BG2 to the rising edge of the synchronizing signal.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of TG1 and BG2. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the LTC7813's phase-locked loop is from approximately 55kHz to 1MHz, with a guarantee to be between 75kHz and 850kHz. In other words, the LTC7813's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.1V (falling). It is recommended that the external clock source swings from ground (0V) to at least 2.5V.

Boost Controller Operation When $V_{IN2} > V_{OUT2}$

When the input voltage to the boost channel rises above its regulated V_{OUT2} voltage, the controller can behave differently depending on the mode, inductor current and V_{IN2} voltage. In forced continuous mode, the loop works

to keep the top MOSFET on continuously once V_{IN2} rises above V_{OUT2} . An internal charge pump delivers current to the boost capacitor from the BOOST2 pin to maintain a sufficiently high TG2 voltage. Because the LTC7813 uses internal switches and does not require external bootstrap diodes, the charge pump only has to overcome small leakage currents (board leakage, etc.).

In pulse-skipping mode, if V_{IN} is between 0% and 10% above the regulated V_{OUT2} voltage, TG2 turns on if the inductor current rises above approximately 3% of the programmed I_{LIM} current. If the part is programmed in Burst Mode operation under this same V_{IN2} window, then TG2 turns on at the same threshold current as long as the chip is awake (the buck channel is awake and switching). If the buck channel is asleep or shut down in this V_{IN2} window, then TG2 will remain off regardless of the inductor current.

If V_{IN} rises more than 10% above the regulated V_{OUT} voltage in any mode, the controller turns on TG2 regardless of the inductor current. In Burst Mode operation, however, the internal charge pump turns off if the entire chip is asleep (if the buck channel is also asleep or shut down). With the charge pump off, there would be nothing to prevent the boost capacitor from discharging, resulting in an insufficient TG2 voltage needed to keep the top MOSFET completely on. The charge pump turns back on when the chip wakes up, and it remains on as long as the buck channel is actively switching.

Boost Controller at Low SENSE Pin Common Voltage

The current comparator of the boost controller is powered directly from the SENSE2⁺ pin and can operate to voltages as low as 2.2V. Since this is lower than the V_{BIAS} UVLO of the chip, V_{BIAS} can be connected to the output of the boost controller, as illustrated in the typical application circuit in Figure 12. This allows the boost controller to handle input voltage transients down to 2.2V while maintaining output voltage regulation. If SENSE2⁺ falls below 2.0V, then switching stops and SS2 is pulled low. If SENSE2⁺ rises back above 2.2V, the SS2 pin will be released, initiating a new soft-start sequence.

OPERATION (Refer to the Functional Diagrams)

Buck Controller Output Overvoltage Protection

The buck channel has an overvoltage comparator that guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{FB1} pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Buck Foldback Current

When the buck output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB1} voltage is keeping up with the TRACK/SS1 voltage). There is no foldback current limiting for the boost channel.

APPLICATIONS INFORMATION

Cascaded Boost+Buck Regulator

The LTC7813 can be configured to regulate two separate, completely independent outputs, one boost and one buck. Or, it can be configured as a cascaded Boost+Buck single output converter that regulates an output voltage from an input voltage that can be above, below, or equal to the output voltage. When cascaded, the input voltage feeds the boost regulator, which generates an intermediate node supply (V_{MID}) that then serves as the input to the buck regulator, which then regulates the output voltage.

When used as a cascaded Boost+Buck regulator, the LTC7813 has distinct advantages compared to traditional single inductor buck-boost regulators. Even though it requires two inductors, these inductors are individually smaller and provide inherent filtering at the input and output, substantially reducing conducted EMI and voltage ripple, thereby requiring less input and output filtering. Even though they are cascaded, the boost and buck regulators are independently optimized and compensated. The buck regulator provides a very fast transient response compared to a buck-boost regulator, further reducing the amount of output capacitance that is required. The LTC7813 also features a very low quiescent current Burst Mode which dramatically reduces power loss and increases efficiency at light loads. Thus, for those applications that require low EMI, low ripple, fast transient response, low quiescent current, and/or high light load efficiency, the LTC7813 cascaded Boost+Buck regulator provides an excellent solution.

The Typical Application on the first page is a basic LTC7813 application circuit. LTC7813 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing has become popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the

power MOSFETs are selected. Finally, input and output capacitors are selected.

SENSE+ and SENSE- Pins

The SENSE+ and SENSE- pins are the inputs to the current comparators.

Buck Controller (SENSE1+/SENSE1-): The common mode voltage range on these pins is 0V to 65V (absolute maximum), enabling the LTC7813 to regulate buck output voltages up to a nominal 60V set point (allowing margin for tolerances and transients). The SENSE1+ pin is high impedance over the full common mode range, drawing at most $\pm 1\mu\text{A}$. This high impedance allows the current comparators to be used in inductor DCR sensing. The impedance of the SENSE1- pin changes depending on the common mode voltage. When SENSE1- is less than $\text{INTV}_{CC} - 0.5\text{V}$, a small current of less than $1\mu\text{A}$ flows out of the pin. When SENSE1- is above $\text{INTV}_{CC} + 0.5\text{V}$, a higher current ($\approx 700\mu\text{A}$) flows into the pin. Between $\text{INTV}_{CC} - 0.5\text{V}$ and $\text{INTV}_{CC} + 0.5\text{V}$, the current transitions from the smaller current to the higher current.

Boost Controller (SENSE2+/SENSE2-): The common mode input range for these pins is 2.2V to 60V, allowing the boost converter to operate from inputs over this full range. The SENSE2+ pin also provides power to the current comparator and draws about $170\mu\text{A}$ during normal operation (when not shut down or asleep in Burst Mode operation). There is a small bias current of less than $1\mu\text{A}$ that flows into the SENSE2- pin. This high impedance on the SENSE2- pin allows the current comparator to be used in inductor DCR sensing.

Filter components mutual to the sense lines should be placed close to the LTC7813, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

APPLICATIONS INFORMATION

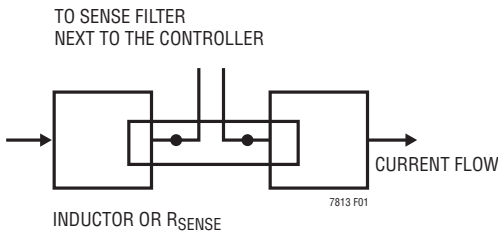


Figure 1. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

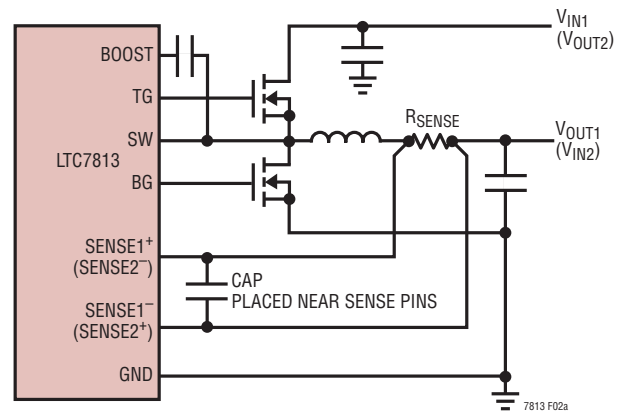
The current comparators have a maximum threshold $V_{SENSE(MAX)}$ of 50mV, 75mV or 100mV. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX} , equal to the peak value less half the peak-to-peak ripple current, ΔI_L . To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

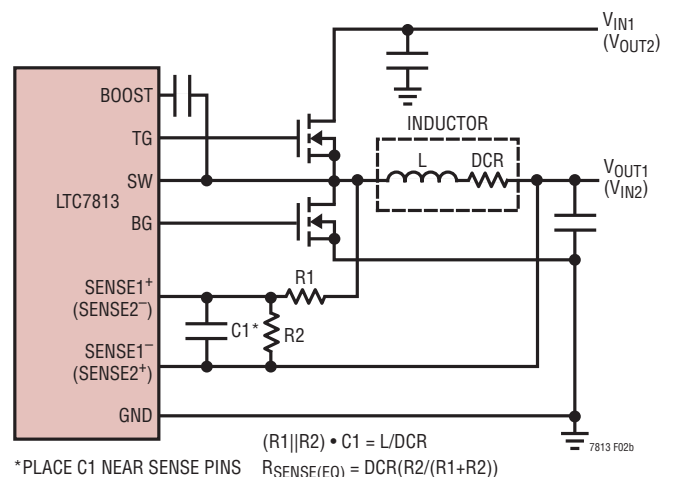
When using the buck controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criteria for buck regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current depending upon the operating duty factor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7813 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Current Sensing Methods

If the external $(R1 || R2) \cdot C1$ time constant is chosen to be exactly equal to the L / DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by $R2 / (R1 + R2)$. $R2$ scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

APPLICATIONS INFORMATION

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{\text{SENSE(EQUIV)}} = \frac{V_{\text{SENSE(MAX)}}}{I_{\text{MAX}} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{\text{SENSE(MAX)}}$ in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(\text{MAX})}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value (R_D), use the divider ratio:

$$R_D = \frac{R_{\text{SENSE(EQUIV)}}}{\text{DCR}_{\text{MAX}} \text{ at } T_{L(\text{MAX})}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces $R1 \parallel R2$ to around 2k, reducing error that might have been caused by the SENSE1+/SENSE2- pin's ±1µA current.

The equivalent resistance $R1 \parallel R2$ is scaled to the temperature inductance and maximum DCR:

$$R1 \parallel R2 = \frac{L}{(\text{DCR at } 20^\circ\text{C}) \cdot C1}$$

The sense resistor values are:

$$R1 = \frac{R1 \parallel R2}{R_D}; \quad R2 = \frac{R1 \cdot R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{\text{LOSS R1}} = \frac{(V_{\text{IN(MAX)}} - V_{\text{OUT}}) \cdot V_{\text{OUT}}}{R1}$$

For the boost controller, the maximum power loss in R1 will occur in continuous mode at $V_{\text{IN}} = 1/2 \cdot V_{\text{OUT}}$:

$$P_{\text{LOSS R1}} = \frac{(V_{\text{OUT(MAX)}} - V_{\text{IN}}) \cdot V_{\text{IN}}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are inter-related in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L , decreases with higher inductance or higher frequency. For the buck controllers, ΔI_L increases with higher V_{IN} :

$$\Delta I_L = \frac{1}{(f)(L)} V_{\text{OUT}} \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right)$$

For the boost controller, ΔI_L increases with higher V_{OUT} :

$$\Delta I_L = \frac{1}{(f)(L)} V_{\text{IN}} \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}} \right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{\text{MAX}})$. The maximum ΔI_L occurs at the maximum input voltage for the bucks and $V_{\text{IN}} = 1/2 \cdot V_{\text{OUT}}$ for the boost.

APPLICATIONS INFORMATION

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit (30% for the boost) determined by R_{SENSE} . Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET Selection

Two external power MOSFETs must be selected for each controller in the LTC7813: one N-channel MOSFET for the top switch (main switch for the buck, synchronous for the boost), and one N-channel MOSFET for the bottom switch (main switch for the boost, synchronous for the buck).

The peak-to-peak drive levels are set by the DRV_{CC} voltage. This voltage can range from 5V to 10V depending on configuration of the DRVSET pin. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed DRV_{CC} voltage. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

The LTC7813's unique ability to adjust the gate drive level between 5V to 10V (OPTI-DRIVE) allows an application circuit to be precisely optimized for efficiency. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER} , input voltage and maximum output current. Miller capacitance, C_{MILLER} , can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS} . This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS} . When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Buck Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Buck Sync Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

$$\text{Boost Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Boost Sync Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

APPLICATIONS INFORMATION

The MOSFET power dissipations at maximum output current are given by:

$$P_{\text{MAIN_BUCK}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} (I_{\text{OUT(MAX)}})^2 (1 + \delta) R_{\text{DS(ON)}} + (V_{\text{IN}})^2 \left(\frac{I_{\text{OUT(MAX)}}}{2} \right) (R_{\text{DR}}) (C_{\text{MILLER}}) \cdot \left[\frac{1}{V_{\text{DRVCC}} - V_{\text{THMIN}}} + \frac{1}{V_{\text{THMIN}}} \right] (f)$$

$$P_{\text{SYNC_BUCK}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{V_{\text{IN}}} (I_{\text{OUT(MAX)}})^2 (1 + \delta) R_{\text{DS(ON)}}$$

$$P_{\text{MAIN_BOOST}} = \frac{(V_{\text{OUT}} - V_{\text{IN}}) V_{\text{OUT}}}{V_{\text{IN}}^2} (I_{\text{OUT(MAX)}})^2 \cdot (1 + \delta) R_{\text{DS(ON)}} + \left(\frac{V_{\text{OUT}}^3}{V_{\text{IN}}} \right) \left(\frac{I_{\text{OUT(MAX)}}}{2} \right) \cdot (R_{\text{DR}}) (C_{\text{MILLER}}) \cdot \left[\frac{1}{V_{\text{DRVCC}} - V_{\text{THMIN}}} + \frac{1}{V_{\text{THMIN}}} \right] (f)$$

$$P_{\text{SYNC_BOOST}} = \frac{V_{\text{IN}}}{V_{\text{OUT}}} (I_{\text{OUT(MAX)}})^2 (1 + \delta) R_{\text{DS(ON)}}$$

where δ is the temperature dependency of $R_{\text{DS(ON)}}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the main N-channel equations for the buck and boost controllers include an additional term for transition losses, which are highest at high input voltages for the buck and low input voltages for the boost. For $V_{\text{IN}} < 20\text{V}$ (higher V_{IN} for the boost) the high current efficiency generally improves with larger MOSFETs, while for $V_{\text{IN}} > 20\text{V}$ (lower V_{IN} for the boost) the transition losses rapidly increase to the point that the use of a higher $R_{\text{DS(ON)}}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses for the buck controller are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{\text{DS(ON)}}$ vs Temperature curve, but $\delta = 0.005/^\circ\text{C}$ can be used as an approximation for low voltage MOSFETs.

Boost C_{IN} , C_{OUT} Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The boost input capacitor C_{IN} voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

In a boost converter, the output has a discontinuous current, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\text{Ripple} = \frac{I_{\text{OUT(MAX)}} \cdot (V_{\text{OUT}} - V_{\text{IN(MIN)}})}{C_{\text{OUT}} \cdot V_{\text{OUT}} \cdot f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{\text{ESR}} = I_{\text{L(MAX)}} \cdot \text{ESR}$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount

APPLICATIONS INFORMATION

packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings such as OS-CON and POSCAP.

Buck C_{IN} , C_{OUT} Selection

The selection of C_{IN} is usually based off the worst-case RMS input current. The highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 1 to determine the maximum RMS capacitor current requirement.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX}}{V_{IN}} [(V_{OUT})(V_{IN} - V_{OUT})]^{1/2} \quad (1)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7813, ceramic capacitors can also be used for C_{IN} . Always consult the manufacturer if there is any question.

A small (0.1 μ F to 1 μ F) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC7813, is also suggested. A small ($\leq 10\Omega$) resistor placed between C_{IN} ($C1$) and the V_{IN} pin provides further isolation.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting Buck Output Voltage

The LTC7813 output voltage for the buck controller is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT(BUCK)} = 0.8V \left(1 + \frac{R_B}{R_A} \right)$$

To improve the frequency response, a feedforward capacitor, C_{FF} , may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

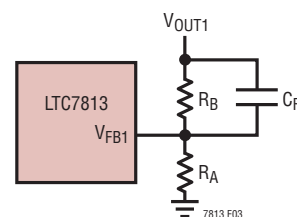


Figure 3. Setting Buck Output Voltage

Setting Boost Output Voltage (VPRG2 Pin)

Through control of the VPRG2 pin, the boost controller output voltage can be set by an external feedback resistor divider or programmed to a fixed 10V or 12V output.

Grounding VPRG2 allows the boost output voltage to be set by an external feedback resistor divider placed across the output, as shown in Figure 4a. The regulated output voltage is determined by:

$$V_{OUT(BOOST)} = 1.2V \left(1 + \frac{R_B}{R_A} \right)$$

Tying the VPRG2 to $INTV_{CC}$ or floating it configures the boost controller in fixed output voltage mode. Figure 4b shows how the V_{FB2} pin is used to sense the output

APPLICATIONS INFORMATION

voltage in this mode. Tying VPRG2 to INTV_{CC} programs the boost output to 12V, whereas floating VPRG2 programs the output to 10V.

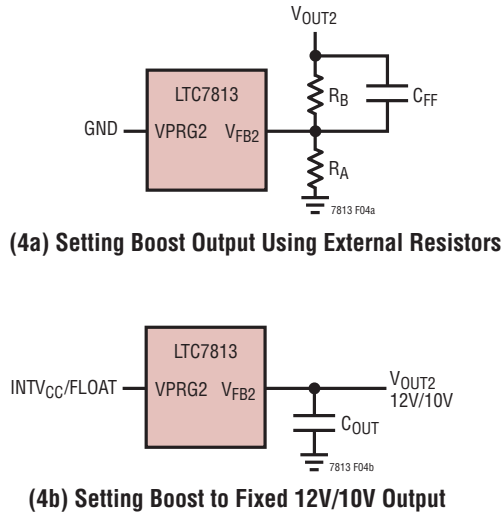


Figure 4. Setting Boost Output Voltage

RUN Pins

The LTC7813 is enabled using the RUN1 and RUN2 pins. The RUN pins have a rising threshold of 1.275V with 75mV of hysteresis. Pulling a RUN pin below 1.2V shuts down the main control loop for that channel. Pulling all three RUN pins below 0.7V disables the controllers and most internal circuits, including the DRV_{CC} and INTV_{CC} LDOs. In this state, the LTC7813 draws only 3.6μA of quiescent current.

Releasing a RUN pin allows a small 150nA internal current to pull up the pin to enable that controller. Because of condensation or other small board leakage pulling the pin down, it is recommended the RUN pins be externally pulled up or driven directly by logic. Each RUN pin can tolerate up to 65V (absolute maximum), so it can be conveniently tied to V_{BIAS} in always-on applications where one or more controllers are enabled continuously and never shut down.

The RUN pins can be implemented as a UVLO by connecting them to the output of an external resistor divider network off V_{BIAS}, as shown in Figure 5.

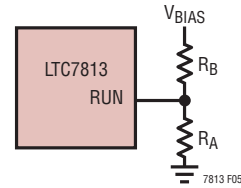


Figure 5. Using the RUN Pins as a UVLO

The rising and falling UVLO thresholds are calculated using the RUN pin thresholds and pull-up current:

$$V_{UVLO(RISING)} = 1.275V \left(1 + \frac{R_B}{R_A} \right) - 150nA \cdot R_B$$

$$V_{UVLO(FALLING)} = 1.20V \left(1 + \frac{R_B}{R_A} \right) - 150nA \cdot R_B$$

Tracking and Soft-Start (TRACK/SS1 and SS2 Pins)

The start-up of each V_{OUT} is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, SS2 for channel 2). When the voltage on the TRACK/SS pin is less than the internal 0.8V reference (1.2V reference for the boost channel), the LTC7813 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin instead of the internal reference. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 6. An internal 10μA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC7813 will regulate its feedback voltage (and hence V_{OUT}) according to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V (V_{IN} for the boost)

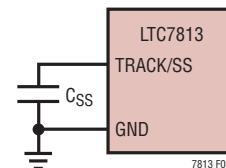


Figure 6. Using the TRACK/SS Pin to Program Soft-Start

APPLICATIONS INFORMATION

to its final regulated value. The total soft-start time will be approximately:

$$t_{SS_BUCK} = C_{SS} \cdot \frac{0.8V}{10\mu A}$$

$$t_{SS_BOOST} = C_{SS} \cdot \frac{1.2V}{10\mu A}$$

Alternatively, the TRACK/SS1 pin for the buck controller can be used to track another supply during start-up, as shown qualitatively in Figures 7a and 7b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply (V_{OUT}), as shown in Figure 8. During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \cdot \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

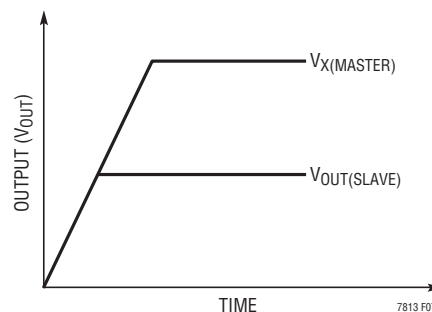
For coincident tracking ($V_{OUT} = V_X$ during start-up),

$$R_A = R_{TRACKA}$$

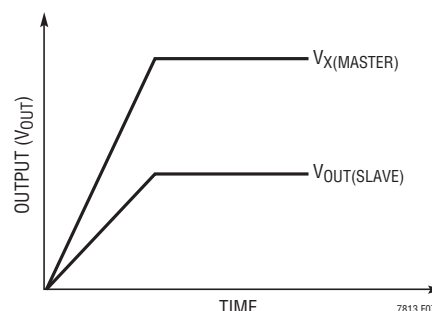
$$R_B = R_{TRACKB}$$

DRV_{CC} and INTV_{CC} Regulators (OPTI-DRIVE)

The LTC7813 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the DRV_{CC} pin from either the V_{BIAS} supply pin or the EXT_{V_{CC}} pin depending on the connections of the EXT_{V_{CC}} and DRVSET pins. A third P-channel LDO supplies power at the INTV_{CC} pin from the DRV_{CC} pin. DRV_{CC} powers the gate drivers whereas INTV_{CC} powers much of the LTC7813's internal circuitry. The V_{BIAS} LDO and the EXT_{V_{CC}} LDO regulate DRV_{CC} between 5V to 10V, depending on how the DRVSET pin is set. Each of these LDOs can supply a peak current of at least 50mA and must be bypassed to ground with a minimum of 4.7μF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels. The INTV_{CC} supply must be bypassed with a 0.1μF ceramic capacitor.



(7a) Coincident Tracking



(7b) Ratiometric Tracking

Figure 7. Two Different Modes of Output Voltage Tracking

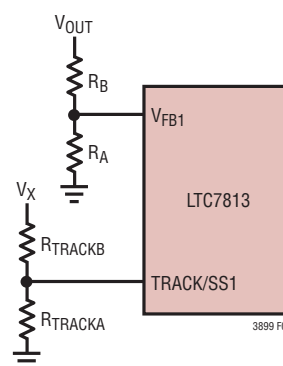


Figure 8. Using the TRACK/SS1 Pin for Tracking