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High Efficiency Switching Surge Stopper

FEATURES

- **High Efficiency V_{OUT} Clamp Stops High Voltage Input Surges**
- **SWITCH-ON Mode 100% Duty Cycle for Normal Operation**
- **PROTECTIVE PWM Mode for Transients and Faults**
- **V_{IN} Pin to SGND Range: 3.5V to 60V**
- **External Input Voltage is Extendable to 200V+**
- **Adjustable Output Voltage Clamp**
- **Adjustable Output Overcurrent Protection**
- Power Inductor Improves Input EMI in Normal Operation
- Programmable Fault Timer
- Adjustable Soft-Start for Input Inrush Current Limiting
- 4.5% Retry Duty Cycle During Faults
- Adjustable Switching Frequency: 50kHz to 850kHz
- Optional Reverse Input Voltage Protection
- Available in Thermally Enhanced 12-lead MSOP Package

APPLICATIONS

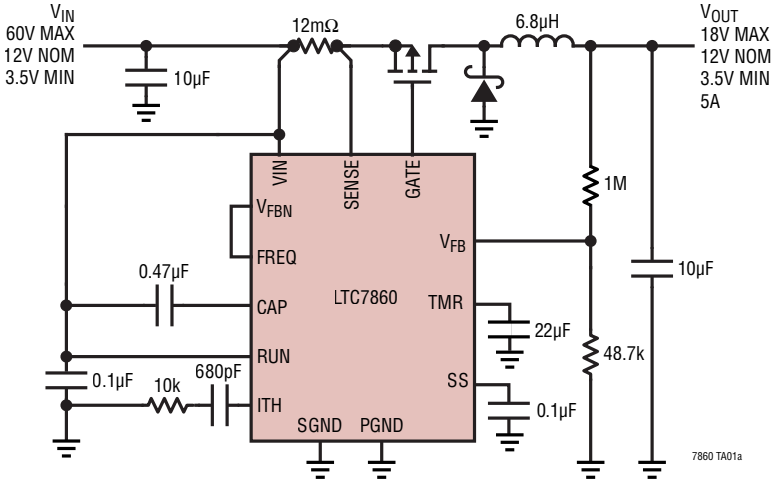
- Industrial and Automotive Power
- Telecom Power
- Vehicle Power Including ISO7637
- Military Power Including MIL1275

DESCRIPTION

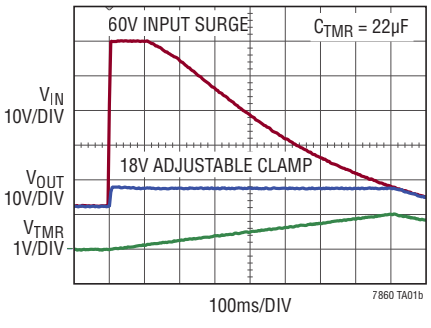
The LTC®7860 high efficiency surge stopper protects loads from high voltage transients. High efficiency permits higher currents and smaller solution sizes. During an input overvoltage event, such as a load dump in vehicles, the LTC7860 controls the gate of an external MOSFET to act as a switching DC/DC regulator (PROTECTIVE PWM mode). This operation regulates the output voltage to a safe level, allowing the loads to operate through the input over-voltage event. During normal operation (SWITCH-ON mode), the LTC7860 turns on the external MOSFET continuously, passing the input voltage through to the output. An internal comparator limits the voltage across the current sense resistor and regulates the maximum output current to protect against overcurrent faults.

An adjustable timer limits the time that the LTC7860 can spend in overvoltage or overcurrent regulation. When the timer expires, the external MOSFET is turned off until the LTC7860 restarts after a cool down period. By strictly limiting the time in PROTECTIVE PWM Mode when the power loss is high, the components and thermal design can be optimized for normal operation and safely operate through high voltage input surges and/or overcurrent faults. An additional PMOS can be added for reverse battery protection.

TYPICAL APPLICATION



PROTECTIVE PWM: V_{OUT} Clamped to 18V During a V_{IN} Surge

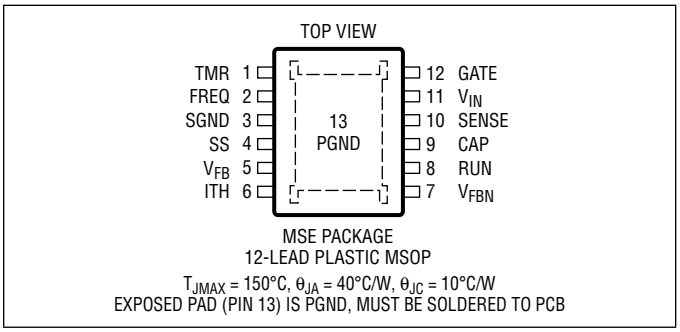


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Input Supply Voltage (V_{IN}) ..... –0.3V to 65V
V_{IN}-V_{SENSE} Voltage ..... –0.3V to 6V
V_{IN}-V_{CAP} Voltage ..... –0.3V to 10V
RUN Voltage ..... –0.3V to 65V
V_{FBN}, TMR Voltages ..... –0.3V to 6V
SS, ITH, FREQ, V_{FB} Voltages ..... –0.3V to 5V
Operating Junction Temperature Range
(Notes 3, 4) ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP Package ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 13) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7860EMSE#PBF	LTC7860EMSE#TRPBF	7860	12-Lead Plastic MSOP	–40°C to 125°C
LTC7860IMSE#PBF	LTC7860IMSE#TRPBF	7860	12-Lead Plastic MSOP	–40°C to 125°C
LTC7860HMSE#PBF	LTC7860HMSE#TRPBF	7860	12-Lead Plastic MSOP	–40°C to 150°C
LTC7860MPMSE#PBF	LTC7860MPMSE#TRPBF	7860	12-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 3) V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{IN}	Input Voltage Operating Range			3.5		60	V
V_{UVLO}	Undervoltage Lockout	(V_{IN}-V_{CAP}) Ramping Up Threshold (V_{IN}-V_{CAP}) Ramping Down Threshold Hysteresis	● ●	3.25 3.00	3.50 3.25 0.25	3.8 3.50	V V V
I_Q	Input DC Supply Current	FREQ = 0V, V_{FB} = 0.83V (No Load)			0.77	1.2	mA
	Shutdown Supply Current	RUN = 0V			7	12	µA
Output Sensing							
V_{REG}	Regulated Feedback Voltage V_{REG} = (V_{FB} – V_{FBN})	V_{ITH} = 1.2V (Note 4)	●	0.791	0.800	0.809	V
	Feedback Voltage Line Regulation	V_{IN} = 3.8V to 60V (Note 4)		–0.005		0.005	%/V
	Feedback Voltage Load Regulation	V_{ITH} = 0.6V to 1.8V (Note 4)		–0.1	–0.015	0.1	%
$g_{m(EA)}$	Error Amplifier Transconductance	V_{ITH} = 1.2V, ΔI_{ITH} = ±5µA (Note 4)			1.8		mS
I_{FB}	Feedback Input Bias Current			–50	–10	50	nA
I_{FBN}	Feedback Negative Input Bias Current			–50	–10	50	nA
Current Sensing							
V_{ILIM}	Current Limit Threshold (V_{IN}-V_{SENSE})	V_{FB} = 0.77V	●	85	95	103	mV
I_{SENSE}	SENSE Pin Input Current	V_{SENSE} = V_{IN}			0.1	2	µA
Start-Up and Shutdown							
V_{RUN}	RUN Pin Enable Threshold	V_{RUN} Rising	●	1.22	1.26	1.32	V
	RUN Pin Hysteresis				150		mV
I_{SS}	Soft-Start Pin Charging Current	V_{SS} = 0V			10		µA
Fault Timer							
I_{TPU}	TMR Pull-Up Current	TMR = 1.1V, V_{FB} = 0.83V	●	–35	–30	–25	µA
I_{TPDR}	TMR Pull-Down Current Restart	TMR = 1.1V, V_{FB} = 0.77V			40		µA
I_{TPDC}	TMR Pull-Down Current Cool Down	TMR = 1.1V, V_{FB} = 0.77V		1.0	1.3	1.6	µA
V_{GTH}	TMR Gate Off Threshold	V_{FB} = 0.77V	●	1.25	1.29	1.35	V
V_{RTH}	TMR Restart Threshold	V_{FB} = 0.77V			240		mV
$T_{SETI(1µF)}$	TMR Set Time Initial for Fault Detection for 1µF (T_{SETI} = V_{GTH}/I_{TPU})		●	37	44	50	ms/µF
$T_{SETR(1µF)}$	TMR Set Time Repeat for Fault Detection for 1µF (T_{SETI} = (V_{GTH} – V_{RTH})/I_{TPU})				32		ms/µF
$T_{RSTC(1µF)}$	TMR Restart Cool Down Time for 1µF (T_{RSTC} = (V_{GTH} – V_{RTH})/I_{TPDC})				732		ms/µF
DTY_{TSTR}	TMR Restart Duty Cycle in a Sustained Fault (DTY_{TSTR} = T_{SETR}/T_{RSTC})		●	3.5	4.5	5.5	%
Switching Frequency							

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 3) V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Programmable Switching Frequency	R_{FREQ} = 24.9kΩ R_{FREQ} = 64.9kΩ R_{FREQ} = 105kΩ		 375	105 440 810	 505	kHz kHz kHz
	Low Switching Frequency	FREQ = 0V		320	350	380	kHz
	High Switching Frequency	FREQ = Open		485	535	585	kHz
f_{FOLD}	Foldback Frequency as Percentage of Programmable Frequency	V_{FB} = 0V, FREQ = 0V			18		%
$t_{ON(MIN)}$	Minimum On-Time				220		ns
Gate Driver							
V_{CAP}	Gate Bias LDO Output Voltage (V_{IN}-V_{CAP})	I_{GATE} = 0mA	●	7.6	8.0	8.5	V
R_{UP}	Gate Pull-Up Resistance	Gate High			2		Ω
R_{DN}	Gate Pull-Down Resistance	Gate Low			0.9		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

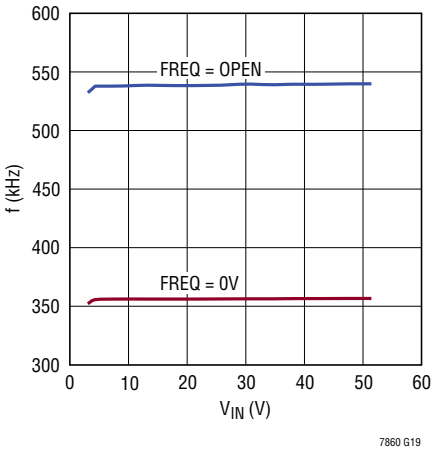
where θ_{JA} (in °C/W) is the package thermal impedance provided in the Pin Configuration section for the corresponding package.

Note 3: The LTC7860 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7860E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature range. The LTC7860E specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7860I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range, the LTC7860H is guaranteed over the –40°C to 150°C operating junction temperature range, and the LTC7860MP is guaranteed and tested over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

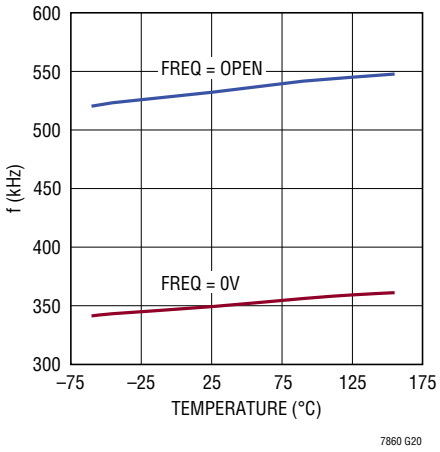
Note 4: The LTC7860 is tested in a feedback loop that adjust V_{REG} or (V_{FB} – V_{FBN}) to achieve a specified error amplifier output voltage (on ITH pin).

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

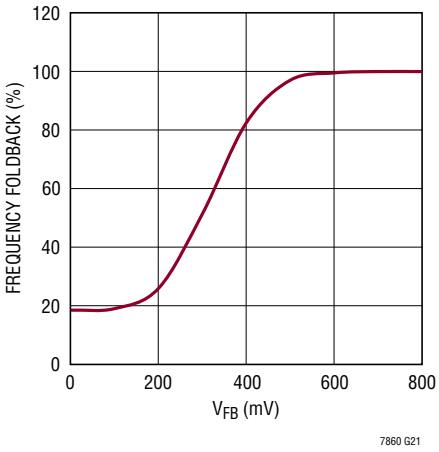
Frequency Over Input Voltage



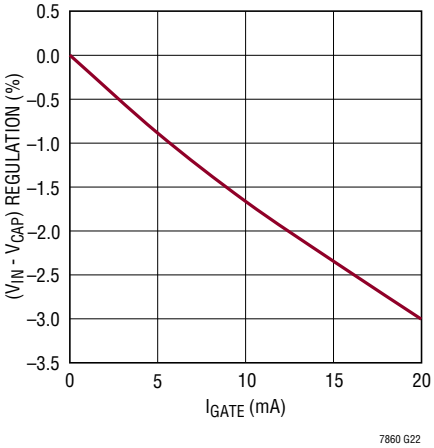
Frequency Over Temperature



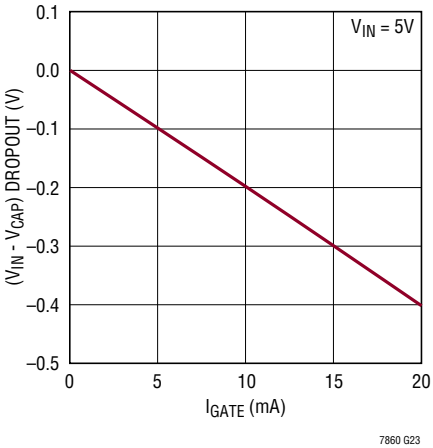
Frequency Foldback % Over Feedback Voltage



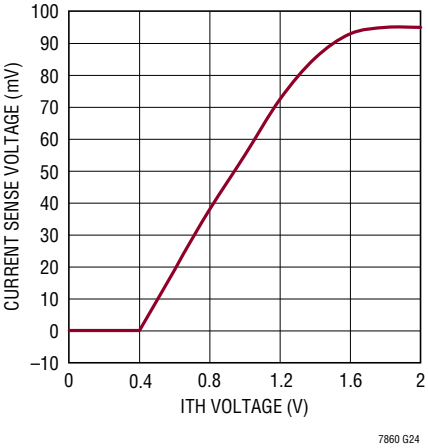
GATE Bias LDO (V_{IN} - V_{CAP}) Load Regulation



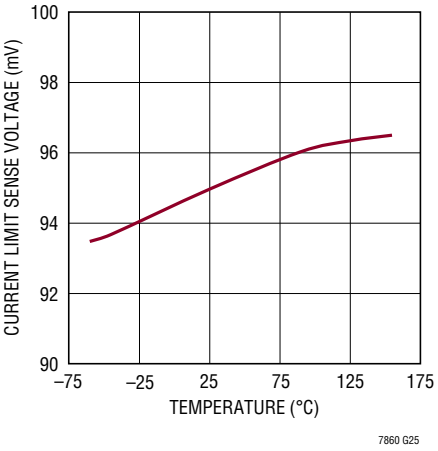
GATE Bias LDO (V_{IN} - V_{CAP}) Dropout Behavior



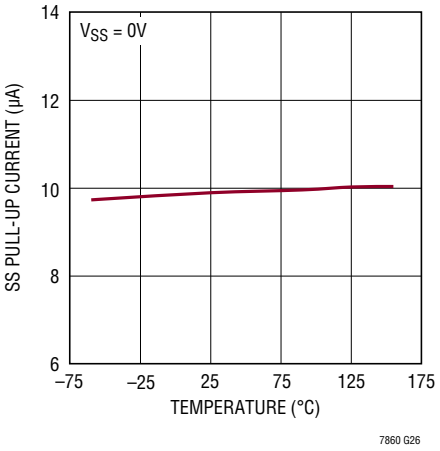
Current Sense Voltage Over ITH Voltage



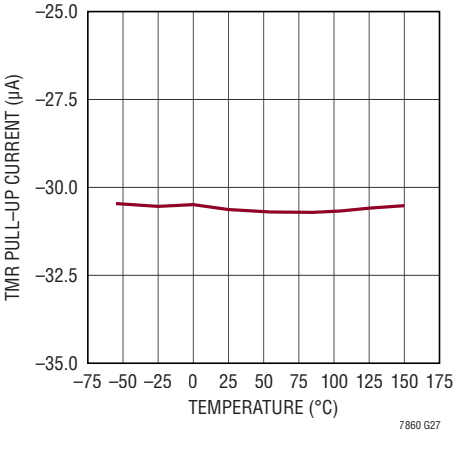
Current Sense Voltage Over Temperature



SS Pin Pull-Up Current Over Temperature



TMR Pull-UP Current Over Temperature



PIN FUNCTIONS

TMR (Pin 1): Programmable Fault Timer. The TMR function monitors the time spent in PROTECTIVE PWM mode and provides fault control. During a fault, a 30µA (I_{TPU}) current pulls up the TMR pin. If the fault clears before the 1.29V TMR Gate Off Threshold (V_{GTH}) is reached, a 40µA current (I_{TPDR}) resets the TMR pin to ground. The gate turns off and shuts down when V_{GTH} is reached. In shutdown, a 1.3µA (I_{TPDC}) current pulls TMR down to a 240mV TMR Restart Threshold (V_{RTH}) allowing a cool down period before restart.

FREQ (Pin 2): Switching Frequency Setpoint Input. The switching frequency is programmed by an external setpoint resistor R_{FREQ} connected between the FREQ pin and signal ground. An internal 20µA current source creates a voltage across the external setpoint resistor to set the internal oscillator frequency. Alternatively, this pin can be driven directly by a DC voltage to set the oscillator frequency. Grounding selects a fixed operating frequency of 350kHz. Floating selects a fixed operating frequency of 535kHz.

SGND (Pin 3): Ground Reference for Small-Signal Analog Component (Signal Ground). Signal ground should be used as the common ground for all small-signal analog inputs and compensation components. Connect the signal ground to the power ground (ground reference for power components) only at one point using a single PCB trace.

SS (Pin 4): Soft-Start and External Tracking Input. The LTC7860 regulates the feedback voltage to the smaller of 0.8V or the voltage on the SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage.

V_{FB} (Pin 5): Output Feedback Sense. A resistor divider from the regulated output point to this pin sets the output voltage. The LTC7860 will nominally regulate V_{FB} to the internal reference value of 0.8V. If V_{FB} is less than 0.4V, the switching frequency will linearly decrease and fold back to about one-fifth of the internal oscillator frequency to reduce the minimum duty cycle.

ITH (Pin 6): Current Control Threshold and Controller Compensation Point. This pin is the output of the error amplifier and the switching regulator's compensation point. The voltage ranges from 0V to 2.9V, with 0.8V corresponding to zero sense voltage (zero current).

V_{FBN} (Pin 7): Feedback Input for an Inverting Feedback Option. Connect V_{FBN} to the center of a resistor divider between the output and V_{FB}. The V_{FBN} threshold is 0V. To defeat the inverting amplifier and use Non-Inverting feedback option, tie V_{FBN} > 2V. V_{FBN} can be tied to FREQ if FREQ is floated and a 535kHz fixed operating frequency is selected. The minimum suggested value of the feedback resistor between V_{FB} and V_{FBN} for Inverting Feedback Option is 10K.

RUN (Pin 8): Run Control Input. A RUN voltage above the 1.26V threshold enables normal operation, while a voltage below the threshold shuts down the controller. An internal 0.4µA current source pulls the RUN pin up to about 3.3V. The RUN pin can be connected to an external power supply up to 60V.

CAP (Pin 9): Gate Driver (–) Supply. A low ESR ceramic bypass capacitor of at least 0.47µF or 10X the effective C_{MILLER} of the P-channel power MOSFET, is required from V_{IN} to this pin to serve as a bypass capacitor for the internal regulator. To ensure stable low noise operation, the bypass capacitor should be placed adjacent to the V_{IN} and CAP pins and connected using the same PCB metal layer.

SENSE (Pin 10): Current Sense Input. A sense resistor, R_{SENSE}, from the V_{IN} pin to the SENSE pin sets the maximum current limit. The peak inductor current limit is equal to 95mV/R_{SENSE}. For accuracy, it is important that the V_{IN} pin and the SENSE pin route directly to the current sense resistor and make a Kelvin (4-wire) connection.

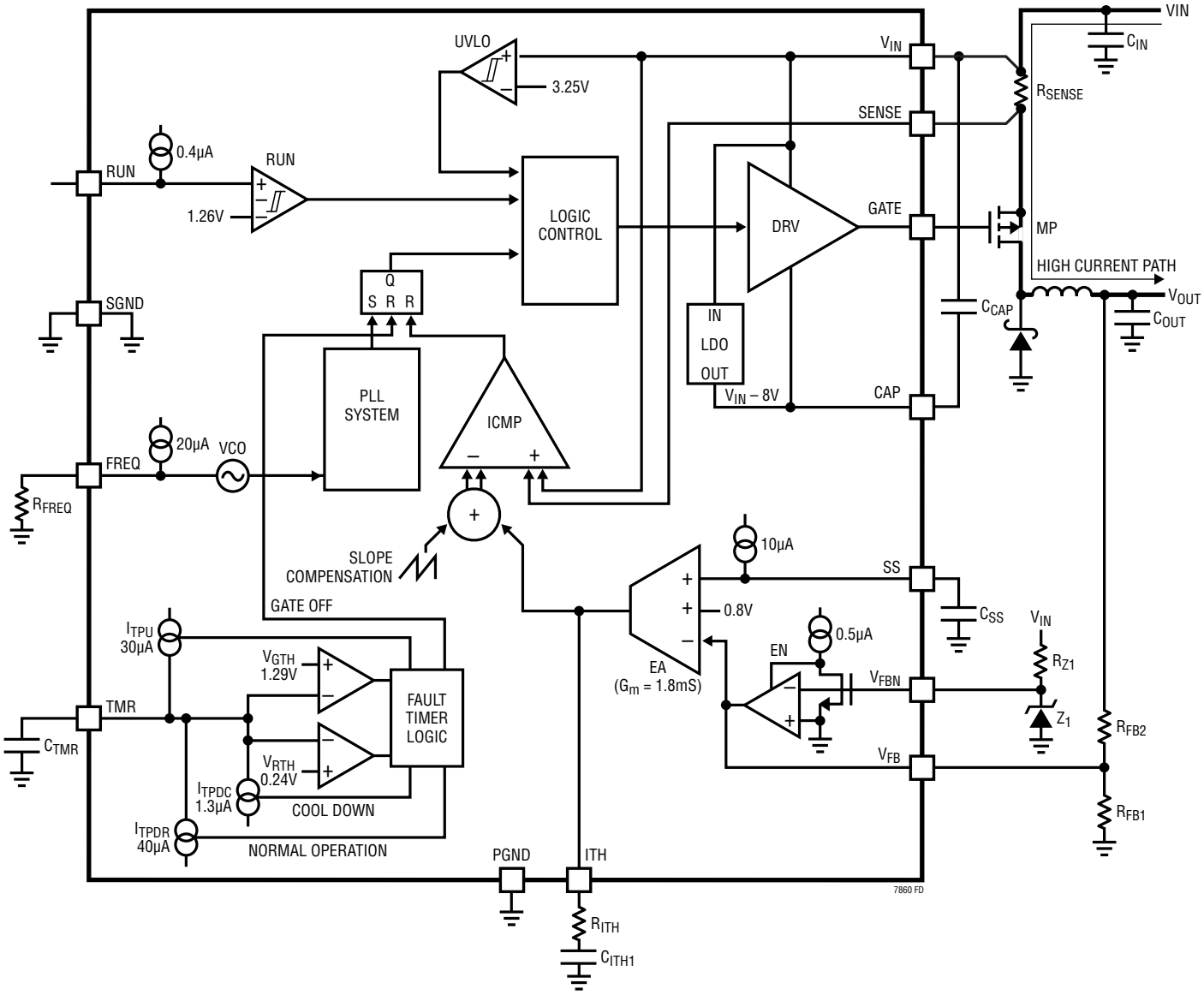
V_{IN} (Pin 11): Chip Power Supply. A minimum bypass capacitor of 0.1µF is required from the V_{IN} pin to power ground. For best performance use a low ESR ceramic capacitor placed near the V_{IN} pin.

PIN FUNCTIONS

GATE (Pin 12): Gate Drive Output for External P-Channel MOSFET. The gate driver bias supply voltage (V_{IN}-V_{CAP}) is regulated to 8V when V_{IN} is greater than 8V. The gate driver is disabled when (V_{IN}-V_{CAP}) is less than 3.5V (typical), 3.8V maximum in start-up and 3.25V (typical) 3.5V maximum in normal operation.

PGND (Exposed Pad Pin 13): Ground Reference for Power Components (Power Ground). The PGND exposed pad must be soldered to the circuit board for electrical contact and for rated thermal performance of the package. Connect signal ground to power ground only at one point using a single PCB trace.

FUNCTIONAL DIAGRAM



OPERATION

High Efficiency Switching Surge Stopper Overview

The LTC7860 is designed for use as a high efficiency switching surge stopper and/or input inrush current limiter. Normal operation for the LTC7860 is in "dropout" or SWITCH-ON mode. The LTC7860 switches during start-up or in response to either an input over-voltage or output short-circuit event (PROTECTIVE PWM mode). If the time spent switching exceeds the time programmed by the timer the LTC7860 will shut down.

A high efficiency surge stopper or input inrush current limiter can be thought of as a pre-regulator. As an example of a MIL1275 application, the input voltage connects to a 28V vehicle power bus. The 28V power bus can go as high as 100V with a surge profile lasting up to 500mS. The output must be pre-regulated or limited to 34V maximum and can go as low as 12V during engine cranking. The LTC7860 limits the voltage seen at the output and protects any load connected to the 28V bus from potentially destructive voltage levels. The LTC7860 timer limits the time spent switching where excessive and thermally destructive power loss can occur.

For both a linear surge stopper such as the LTC4363 and the LTC7860 switching surge stopper, the power loss increases significantly once regulation begins. In a linear surge stopper, the power loss is the power loss of the regulating MOSFET. In a high efficiency surge stopper or switching surge stopper, internal power loss is determined by conversion efficiency. A switching surge stopper will allow higher output current and power levels than a comparable linear solution by virtue of reduced power loss. In a switching surge stopper the internal surge power loss can increase by as much as 10 times the normal power loss. If the time spent in PWM mode regulation is limited, the operating power can be pushed beyond what can be achieved in steady state operation. This is precisely the same concept as utilized in linear surge stoppers but extended to a switching supply. The use of the timer improves reliability and reduces component size when compared to a continuous solution. By limiting the time in regulation when the power loss is high, the components and thermal design can be optimized for normal operation and safely operate through high voltage input surges and/or overcurrent faults.

In a switching surge stopper the insertion loss in normal operation or SWITCH-ON mode is the primary consideration and not efficiency in switching. The LTC7860 circuit must operate without damage during a surge or fault event. The Switching Surge Stopper is effectively a wire in normal operation where the insertion loss is determined by multiplying the input current by the effective resistance.

LTC7860 Main Control Loop

The LTC7860 uses a peak current-mode control architecture to regulate the output in a step-down DC/DC switching regulator. The V_{FB} input is compared to an internal reference by a transconductance error amplifier (EA). The internal reference can be either a fixed 0.8V reference V_{REF} or the voltage input on the SS pin. In normal operation V_{FB} regulates to the internal 0.8V reference voltage. In soft-start, when the SS pin voltage is less than the internal 0.8V reference voltage, V_{FB} will regulate to the SS pin voltage. The error amplifier output connects to the ITH (current [I] threshold [TH]) pin. The voltage level on the ITH pin is then summed with a slope compensation ramp to create the peak inductor current set point.

The peak inductor current is measured through a sense resistor, R_{SENSE}, placed across the V_{IN} and SENSE pins. The resultant differential voltage from V_{IN} to SENSE is proportional to the inductor current and is compared to the peak inductor current setpoint. During normal operation the P-channel power MOSFET is turned on when the clock leading edge sets the SR latch through the S input. The P-channel MOSFET is turned off through the SR latch R input when the differential voltage from V_{IN} to SENSE is greater than the peak inductor current setpoint and the current comparator, ICMP, trips high.

OPERATION

Power CAP and V_{IN} Undervoltage Lockout (UVLO)

Power for the P-channel MOSFET gate driver is derived from the CAP pin. The CAP pin is regulated to 8V below V_{IN} in order to provide efficient P-channel operation. The power for the V_{CAP} supply comes from an internal LDO, which regulates the V_{IN}-CAP differential voltage. A minimum capacitance of 0.47µF (low ESR ceramic) is required between V_{IN} and CAP to assure stability.

For $V_{IN} \leq 8V$, the LDO will be in dropout and the CAP voltage will be at ground, i.e., the V_{IN}-CAP differential voltage will equal V_{IN}. If V_{IN}-CAP is less than 3.25V (typical), the LTC7860 enters a UVLO state where the GATE is prevented from switching and most internal circuitry is shut down. In order to exit UVLO, the V_{IN}-CAP voltage would have to exceed 3.5V (typical).

Shutdown and Soft-Start

When the RUN pin is below 0.7V, the controller and most internal circuits are disabled. In this micropower shutdown state, the LTC7860 draws only 7µA. Releasing the RUN pin allows a small internal pull-up current to pull the RUN pin above 1.26V and enable the controller. The RUN pin can be pulled up to an external supply of up to 60V or driven directly by logic levels.

The start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 0.8V internal reference, the V_{FB} pin is regulated to the voltage on the SS pin. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to signal ground. An internal 10µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises from 0V to 0.8V, the output voltage V_{OUT} rises smoothly from zero to its final value. The SS time must be sufficiently less than the TMR set time to avert a timer shutdown in startup or fault recovery.

If the slew rate of the SS pin is greater than 1.2V/ms, the output will track an internal soft-start ramp instead of the SS pin. The internal soft-start will guarantee a smooth start-up of the output under all conditions, including in the case of a short-circuit recovery where the output voltage will recover from near ground.

Frequency Selection

The switching frequency of the LTC7860 can be selected using the FREQ pin. The FREQ pin can be tied to signal ground, floated, or programmed through an external resistor. Tying FREQ pin to signal ground selects 350kHz, while floating selects 535kHz. Placing a resistor between FREQ pin and signal ground allows the frequency to be programmed between 50kHz and 850kHz. Refer to the chart in the Application section for switching frequency versus resistor values.

Fault Protection

In the event of an output short-circuit or overcurrent condition that causes the output voltage to drop significantly while in current limit, the LTC7860 operating frequency will fold back. Anytime the output feedback V_{FB} voltage is less than 50% of the 0.8V internal reference (i.e., 0.4V), frequency foldback is active. The frequency will continue to drop as V_{FB} drops until reaching a minimum foldback frequency of about 18% of the setpoint frequency. Frequency foldback is designed, in combination with peak current limit, to limit current in start-up and short-circuit conditions. Setting the foldback frequency as a percentage of operating frequency assures that start-up characteristics scale appropriately with operating frequency.

APPLICATIONS INFORMATION

The LTC7860 is a high efficiency switching surge stopper which provides input voltage surge protection, input inrush current limiting and output short protection. High Efficiency Switching permits high output current capability and small solution size. During an input overvoltage event, such as a load dump in vehicles, the LTC7860 controls the gate of an external MOSFET to act as a switching DC/DC regulator (PROTECTIVE PWM mode). This operation regulates the output voltage to a safe level, allowing the loads to operate through the input over-voltage event.

During normal operation (SWITCH-ON mode), the LTC7860 turns on the external MOSFET continuously, passing the input voltage through to the output. An internal comparator limits the voltage across the current sense resistor and regulates the maximum output current to protect against over current faults.

OUTPUT VOLTAGE PROGRAMMING

The LTC7860 is highly flexible and offers application options to address a variety of input and output voltage ranges. These options are best divided into two categories. The first category is operation at or below V_{IN} = 60V. The second category is operation above 60V. The LTC7860 input and output voltage operation in the second category depends only on external components and can be reliably extended up to 200V.

Operation for V_{IN} of 60V and BELOW

For operation at V_{IN} of 60V and BELOW, the output voltage is programmed by connecting a feedback resistor divider from the output to the V_{FB} pin as shown in Figure 1a. The front page application is an example of this configuration. The output voltage in steady state operation is set by the feedback resistors R_{FB2} and R_{FB1} according to the equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the GATE signal that drives the external P MOSFET. The best practice is to locate resistors R_{FB2} and R_{FB1} and capacitor C_{FF} local to the LTC7860 to keep the V_{FB} trace short and without VIAS. The planes for V_{OUT} and GND are then routed to the desired regulation point. Detailed layout suggestions are discussed in the Layout sections later in the data sheet. The feed-forward capacitor C_{FF} is added to improve transient response.

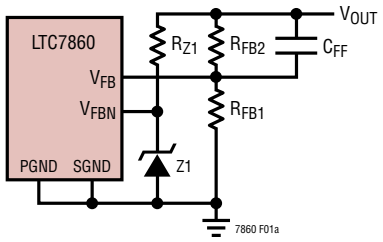


Figure 1a. Switching Surge Stopper for V_{IN} Operation of 60V and BELOW (V_{FBN} > 2V)

Operation for V_{IN} ABOVE 60V

For operation at V_{IN} = 60V, a floating ground must be created by a bootstrapped shunt regulator such as a Zener or similar element. To establish shunt DC bias to the LTC7860, connect the floating ground to the LTC7860 PGND and SGND pins. The Zener voltage or Shunt DC bias limit is typically 12V to minimize internal power dissipation but can be extended up to 60V. The V_{IN} Operational Input voltage ranges for these applications are limited only by external components and can reliably extend to 200V and beyond. There are two feedback options for operation above 60V which are Inverting and Non-Inverting Feedback.

The Inverting Feedback Option uses fewer components with slightly reduced accuracy (Figure 1b). The Non- Inverting Feedback Option uses additional components but with better accuracy (Figure 1c). It has the additional advantage of reducing VIN quiescent current in normal operation.

Inverting Feedback Option

In the Inverting Feedback Option for V_{IN} ABOVE 60V, the voltage is programmed by connecting a feedback resistor divider from the output to ground as shown in Figure 1b. V_{OUT} is divided down and the voltage presented to the gate of Q_{FB}. The gate voltage is then translated into a signal current by Q_{FB} and R_{FB3} and sent to the LTC7860 Floating Ground Inverting Feedback Pin V_{FBN}. The resistor R_{FB4}

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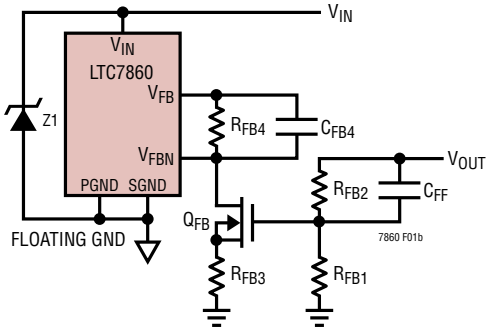

Figure 1b. Switching Surge Stopper for V_{IN} Operation ABOVE 60V with Inverting Feedback

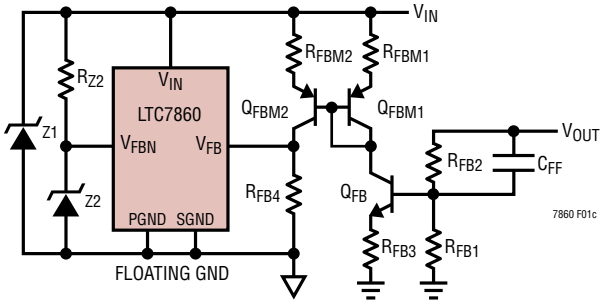

Figure 1c. Switching Surge Stopper with V_{IN} Operation ABOVE 60V with Non-Inverting Feedback

translates the signal current proportional to V_{OUT} into a feedback voltage between V_{FB} and V_{FBN}. The voltage at V_{FBN} is the input of an inverting amplifier and is nominally equal to the Floating Ground. The output voltage in steady state operation is set by the feedback resistors according to the equation:

$$V_{OUT} = \left(0.8V \bullet \frac{R_{FB3}}{R_{FB4}} + VGS_{QFB}\right) \bullet \left(1 + \frac{R_{FB2}}{R_{FB1}}\right)$$

The shunt DC bias or Zener and floating ground permits the drain current of Q_{FB} to be translated to a differential feedback voltage $V_{FB} – V_{FBN}$ independent of the value of V_{IN}. R_{FB4} should be greater than 10k to avoid V_{FB} pin output current limitations.

The integrator capacitor, C_{FB4}, should be sized to ensure the negative sense amplifier gain rolls off and limits high frequency gain peaking in the DC/DC control loop. The integrator capacitor pole can be safely set to be two times the switching frequency without affecting the DC/DC phase margin according to the following equation. It is highly recommended that C_{FB4} be used in most applications.

$$C_{FB4} = \frac{1}{(2 \bullet \pi \bullet 2 \bullet R_{FB4} \bullet FREQSW)}$$

Great care should be taken to route the V_{FB} and V_{FB} lines away from noise sources, such as the inductor or the GATE signal that drives the external P MOSFET.

Non-Inverting Feedback Option

In the Non-Inverting Feedback Option for V_{IN} ABOVE 60V, the voltage is programmed by connecting a feedback resistor divider from the output to ground as shown in Figure 1c. V_{OUT} is divided down and the voltage presented to the base of Q_{FB}. The base voltage is then translated into a signal current by Q_{FB} and R_{FB3} and sent to PNP mirror Q_{FBM1}, R_{FBM1}, Q_{FBM2} and R_{FBM2}.

In the Non-Inverting Option, the internal inverting amplifier must be defeated by tying V_{FBN} greater than 2V. In Figure 1c, R_{Z2} and Z2 are used to tie V_{FBN} high where Z2 is chosen greater than 2V but less than 6V. V_{FBN} may also be tied to the FREQ pin when the pin is floated and a fixed 535kHz switching frequency is selected. Choosing a fixed 535kHz in the Non-Inverting option can simplify the PCB design and reduce component count.

For the Non-Inverting Option, an NPN is used for Q_{FB}, which results in greater accuracy. The resistor R_{FB4} translates the signal current proportional to V_{OUT} into a feedback voltage applied directly to the V_{FB} pin. The V_{FBN} pin is tied high and the inverting amplifier is defeated. The output voltage in steady state operation is set by the feedback resistors according to the equation:

$$V_{OUT} = \left(0.8V \bullet \frac{R_{FB3}}{R_{FB4}} + VBE_{QFB}\right) \bullet \left(1 + \frac{R_{FB2}}{R_{FB1}}\right)$$

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SWITCHING FREQUENCY

The choice of operating frequency is a trade-off between efficiency and component size. Lowering the operating frequency improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. Conversely, raising the operating frequency degrades efficiency but reduces component size.The switching frequency and resulting switching power loss are of secondary concern. It is generally recommended to go with as high a switching frequency as practical so as to limit the overall solution size.

The free-running switching frequency can be programmed from 50kHz to 850kHz by connecting a resistor from FREQ pin to signal ground. The resulting switching frequency as a function of resistance on the FREQ pin is shown in Figure 2.

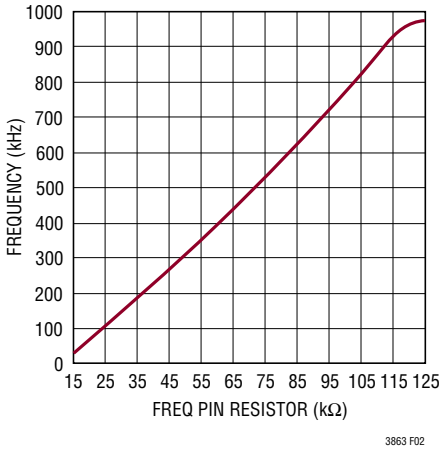

Figure 2. Switching Frequency vs Resistor on FREQ pin

INDUCTOR SELECTION

A reasonable starting point for ripple current is 70% of $I_{OUT(MAX)}$ at maximum V_{IN}. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Select an inductor with a saturation current rating sufficient to cover peak current during a full load input transient or output over load. Powder core inductors are typically a good choice as they tend to be small and have good saturation characteristics.

CURRENT SENSING AND CURRENT LIMIT PROGRAMMING

The LTC7860 senses the inductor current through a current sense resistor, R_{SENSE}, placed across the V_{IN} and SENSE pins. The voltage across the resistor, V_{SENSE}, is proportional to inductor current and in normal operation is compared to the peak inductor current setpoint. An inductor current limit condition is detected when V_{SENSE} exceeds 95mV. When the current limit threshold is exceeded, the P-channel MOSFET is immediately turned off by pulling the GATE voltage to V_{IN} regardless of the controller input.

The peak inductor current limit is equal to:

$$I_{L(PEAK)} \cong \left(\frac{95mV}{R_{SENSE}}\right)$$

This inductor current limit would translate to an output current limit based on the inductor ripple and duty factor:

$$I_{OUT(LIMIT)} = \left(\frac{95mV}{R_{SENSE}} - \frac{\Delta I_L}{2}\right)$$

The SENSE pin is a high impedance input with a maximum leakage of ±2µA. Since the LTC7860 is a peak current mode controller, noise on the SENSE pin can create pulse width jitter. Careful attention must be paid to the layout of R_{SENSE}. To ensure the integrity of the current sense signal, V_{SENSE}, the traces from V_{IN} and SENSE pins should be short and run together as a differential pair and Kelvin (4-wire) connected across R_{SENSE} (Figure 3).

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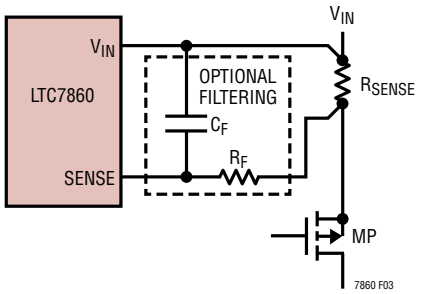

Figure 3. Inductor Current Sensing

The LTC7860 has internal filtering of the current sense voltage which should be adequate in most applications. However, adding a provision for an external filter offers added flexibility and noise immunity, should it be necessary. The filter can be created by placing a resistor from the R_{SENSE} resistor to the SENSE pin and a capacitor across the V_{IN} and SENSE pins. It is important that the V_{IN} plane be a clean low inductance connection with minimal PCB via's.

The maximum output current in SWITCH-ON mode is greater than the maximum current in PROTECTIVE PWM mode by one half the ripple current. The SWITCH-ON mode power path components must be designed to support the maximum power seen at the non-switching current limit setting.

POWER MOSFET SELECTION

The LTC7860 drives a P-channel power MOSFET that serves as the main switch for the nonsynchronous inverting converter. Important P-channel power MOSFET parameters include drain-to-source breakdown voltage, on-resistance $R_{DS(ON)}$, threshold voltage $V_{GS(TH)}$, and the MOSFET's thermal resistance $\theta_{JC(MOSFET)}$ and $\theta_{JA(MOSFET)}$.

The drain-to-source breakdown voltage must meet the following condition:

$$BV_{DSS} > V_{IN(MAX)}$$

The most important parameter for selection of the PMOS switch (after voltage rating) is $R_{DS(ON)}$. This will determine PMOS loss during SWITCH-ON operation.

The gate driver bias voltage V_{IN}-V_{CAP} is set by an internal LDO regulator. In normal operation, the CAP pin will be regulated to 8V below V_{IN}. A minimum 0.47µF capacitor is required across the V_{IN} and CAP pins to ensure LDO stability. If required, additional capacitance can be added to accommodate higher gate currents without voltage droop. In shutdown and Burst Mode operation, the CAP LDO is turned off. In the event of CAP leakage to ground, the CAP voltage is limited to 9V by a weak internal clamp from V_{IN} to CAP. As a result, a minimum 10V V_{GS} rated MOSFET is required.

DIODE SELECTION

When the P-channel MOSFET is turned off, a commutating diode carries the inductor current. This diode is *only* used during switching and does not conduct in SWITCH-ON mode. The average forward diode current is described as:

$$I_{F(AVG)} = I_{OUT} \bullet (1 - D)$$

The worst-case condition for diode conduction is a short circuit condition where the diode must handle the maximum current as the P-channel MOSFET's duty factor approaches 0%. The diode therefore must be chosen carefully to meet worstcase voltage and current requirements. A good practice is to choose a diode that has a forward current rating higher than $I_{OUT(MAX)}$.

The diode reverse breakdown voltage must meet the following condition:

$$V_R > V_{IN(MAX)}$$

C_{IN} AND C_{OUT} SELECTION (BUCK MODE)

The input capacitance, C_{IN}, is required to filter the square wave current through the P-channel MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current:

$$I_{CIN(RMS)} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

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The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{CIN(RMS)} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. Ripple currents will only be applied during PROTECTIVE PWM operation, so de-rating requirements are minimal.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, specialty polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Specialty polymer capacitors offer very low ESR but have lower specific capacitance than other types. Tantalum capacitors have the highest specific capacitance, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects.

EXTERNAL SOFT-START

Start-up characteristics are controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 0.8V reference, the LTC7860 regulates the V_{FB} pin voltage to the voltage on the SS pin. When the SS pin is greater than the internal 0.8V reference, the V_{FB} pin voltage regulates to the 0.8V internal reference. The SS pin is used to program an external soft-start function. The primary function of the external SOFT START feature for a Switching Surge Stopper is as an inrush current limiter in startup and fault recovery.

Soft-start is enabled by connecting a capacitor from the SS pin to ground. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin that causes V_{OUT} to rise smoothly from 0V to its final value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

SHORT-CIRCUIT FAULTS: CURRENT LIMIT AND FOLDBACK

The inductor current limit is inherently set in a current mode controller by the maximum sense voltage and R_{SENSE}. In the LTC7860, the maximum sense voltage is 95mV, measured across the inductor sense resistor, R_{SENSE}, placed across the V_{IN} and SENSE pins. The output current limit is approximately:

$$I_{LIMIT(MIN)} = \left(\frac{95mV}{R_{SENSE}} - \frac{\Delta I_L}{2} \right)$$

The current limit must be chosen to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$ under all operating conditions. Short-circuit fault protection is assured by the combination of current limit and frequency foldback. When the output feedback voltage, V_{FB}, drops below 0.4V, the operating frequency, f, will fold back to a minimum value of 0.18 • f when V_{FB} reaches 0V. Both current limit and frequency foldback are active in all modes of operation. In a short-circuit fault condition, the output current is first limited by current limit and then further reduced by folding back the operating frequency as the short becomes more severe. The worst-case fault condition occurs when V_{OUT} is shorted to ground.

SHORT-CIRCUIT RECOVERY AND INTERNAL SOFT-START

An internal soft-start feature guarantees a maximum positive output voltage slew rate in all operational cases. In a short-circuit recovery condition for example, the output recovery rate is limited by the internal soft-start so that

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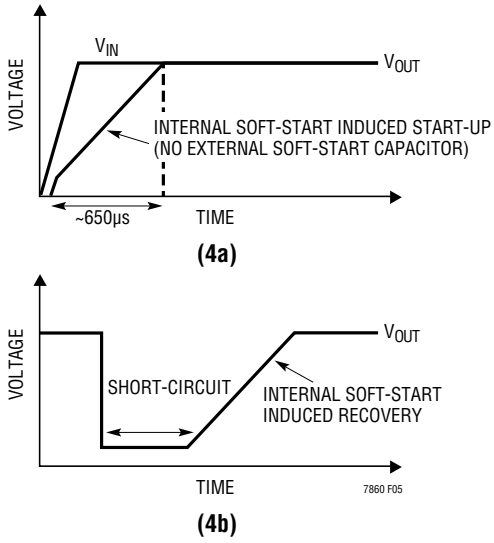

Figure 4. Internal Soft-Start (4a) Allows Soft-Start without an External Soft-Start Capacitor and Allows Soft Recovery from (4b) a Short-Circuit

output voltage overshoot and excessive inductor current buildup is prevented.

The internal soft-start voltage and the external SS pin operate independently. The output will track the lower of the two voltages. The slew rate of the internal soft-start voltage is roughly 1.2V/ms, which translates to a total soft-start time of 650µs. If the slew rate of the SS pin is greater than 1.2V/ms the output will track the internal soft-start ramp. To assure robust fault recovery, the internal soft-start feature is active in all operational cases. If a short-circuit condition occurs which causes the output to drop significantly, the internal soft-start will assure a soft recovery when the fault condition is removed.

The internal soft-start assures a clean soft ramp-up from any fault condition that causes the output to droop, guaranteeing a maximum ramp rate in soft-start, short-circuit fault release. Figure 4 illustrates how internal soft-start controls the output ramp-up rate under varying scenarios.

V_{IN} UNDERVOLTAGE LOCKOUT (UVLO)

The LTC7860 is designed to accommodate applications requiring widely varying power input voltages from 3.5V to 60V. To accommodate the cases where V_{IN} drops significantly, the LTC7860 is guaranteed to operate down to a V_{IN} of 3.5V over the full temperature range.

The implications of both the UVLO rising and UVLO falling specifications must be carefully considered for low V_{IN} operation. The UVLO threshold with V_{IN} rising is typically 3.5V (with a maximum of 3.8V) and UVLO falling is typically 3.25V (with a maximum of 3.5V). The operating input voltage range of the LTC7860 is guaranteed to be 3.5V to 60V over temperature, but the initial V_{IN} ramp must exceed 3.8V to guarantee start-up.

For example, Figure 5 illustrates LTC7860 operation when an automotive battery droops during a cold crank condition. The typical automotive battery voltage is 12V to 14.4V, which is more than enough headroom above 3.8V for the LTC7860 to start up. Onboard electronics which are powered by a DC/DC regulator require a minimum supply voltage for seamless operation during the cold crank condition, and the battery may droop close to these minimum supply requirements during a cold crank. The DC/DC regulator should not exacerbate the situation by having excessive voltage drop between the already suppressed battery voltage input and the output of the regulator which powers these electronics. As seen in Figure 5, the LTC7860's 100% duty cycle capability allows low dropout from the battery to the output. The drop from V_{IN} to V_{OUT} is determined by the output Load current multiplied by the total series resistance of the switching surge stopper. The 3.5V guaranteed UVLO assures sufficient margin for continuous, uninterrupted operation in extreme cold crank battery drooping conditions. However, additional input capacitance or slower soft start-up time may be required at low V_{IN} (e.g. 3.5V to 4.5V) in order to limit V_{IN} droop caused by inrush currents, especially if the input source has a sufficiently large output impedance.

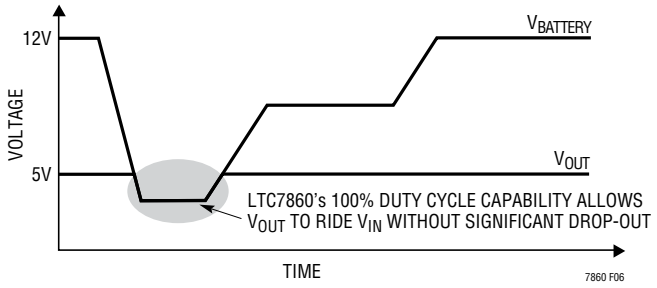

Figure 5. Typical Automotive Cold Crank

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MINIMUM ON-TIME CONSIDERATIONS

The minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC7860 is capable of turning on the power MOSFET, and is typically 220ns. It is determined by internal timing delays and the gate charge required to turn on the MOSFET. Low duty cycle applications may approach this minimum on-time limit, so care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN(MAX)} \bullet f}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will skip cycles. However, the output voltage will continue to regulate.

THERMAL CONSIDERATIONS

The sustained or static power loss in SWITCH-ON operation must be limited so as to ensure suitable maximum component temperatures during all normal operating conditions. The temperature rise of a Switching Surge Stopper is best measured empirically. Power Loss for the SWITCH-ON power paths is I^2R_{SW-ON} and may be calculated according to the equation below.

$$I^2R_{SW-ON} = I^2 \bullet (R_{SENSE} + R_{DS(ON)} + R_{INDUCTOR})$$

The dynamic or transient power loss in PROTECTIVE PWM operation is of concern with respect to component temperature rise and is principally managed by the timer function which sets a maximum time in this mode. Thermal mass and thermal resistance play key roles in determining the peak temperatures of components at the point in time when the timer cycles off and shuts down.

Worst-case operation for a single fault shorted output is typically with the input voltage in the high normal operating range and the output shorted. For this condition, the catch diode is typically the hottest component, as it conducts nearly all the peak current at a high duty cycle. Worst-case operation for a single fault input voltage surge is with the input at the maximum expected input voltage or profile at the maximum operational load current. An input voltage surge and output short is a double fault and may not be required. Specific fault testing and design margin is determined by system requirements.

Thermal evaluation and timer setting can be most easily done empirically by observing key component temperatures dynamically in various fault conditions. Observe peak temperatures with an instrument with sufficient bandwidth to track temperatures, such as an infrared (IR) camera. One with video capability is ideal.

Set a maximum temperature rise goal based on component maximum junction temperature ratings, maximum expected ambient temperature, and allowed junction to case temperature rise. Start at lower input voltages and/or shorter TMR timer settings and increase after empirical system verification and measurement.

OPTI-LOOP® COMPENSATION

OPTI-LOOP compensation, through the availability of the ITH pin, allows the transient response to be optimized for a wide range of loads and output capacitors. The ITH pin not only allows optimization of the control loop behavior but also provides a test point for the regulator's DC-coupled and AC-filtered closed-loop response. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at this pin.

The ITH series R_{ITH}-C_{ITH1} filter sets the dominant pole-zero loop compensation. Additionally, a small capacitor placed from the ITH pin to signal ground, C_{ITH2}, may be required to attenuate high frequency noise. The values can be modified to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback gain and phase. An output

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current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The general goal of OPTI-LOOP compensation is to realize a fast but stable ITH response with minimal output droop due to the load step. For a detailed explanation of OPTI-LOOP compensation, refer to Application Note 76.

FAULT TIMER

The LTC7860 is a Switching Surge Stopper. The LTC7860 switches only during startup, during an overcurrent fault and during an input overvoltage surge (PROTECTIVE PWM operation). The primary function of a surge stopper is to limit the output to a programmed maximum voltage during an input voltage surge. Limiting the output voltage "Surge Stops" the input voltage surge and prevents it from propagating to the system and potentially causing damage.

The Switching Surge Stopper external components are optimized to minimize total line resistance in normal operation or SWITCH-ON mode rather than overload operation. The fault timer limits the switching time during an overload.

The fault timer is programmed to allow the Switching Surge Stopper to operate below a safe peak temperature with the PWM power losses in startup, in a current limit fault or in an input voltage surge. Since the device shuts down before reaching thermal equilibrium, the power rating can be significantly increased over continuous operation. The fault timer saves system cost and size by allowing component selections to be determined by normal or SWITCH-ON mode rather than Protective PWM operating mode. The timer indirectly limits the peak Switching Surge Stopper temperatures by limiting the total time spent in higher power loss PROTECTIVE PWM operating mode.

Fault Timer Functionality

In normal operation the TMR pin voltage is held at ground by the current source TMR Pull-Down Reset I_{TPDR}. When switching is detected, the TMR Pull-Up current or I_{TPU} pulls up the TMR pin. If the fault is removed and the TMR reverses before reaching the fault set Gate Off threshold or V_{GTH} the TMR pin reverses and pulls to ground by I_{TPDR}. Please reference Figure 6, Timer (TMR) Functional Diagram.

When the TMR pin exceeds V_{GTH}, a fault is detected and the PMOS Gate is turned off and is held off for a cool down time. Once V_{GTH} threshold is reached, the pull down current source I_{TPDC} pulls down the TMR until reaching the TMR Reset Threshold or V_{RTH}. The time the PMOS gate is shutdown after V_{GTH} is reached until the fault is reset is called the cool down time. Once the fault is reset, the TMR pin will either pull-down to ground if the fault condition has been cleared or pulled up to V_{GTH} if the fault is present. In the case of a persistent fault caused by a short circuit, TMR will continuously retry and shutdown.

Programming the Fault Timer

The TMR Initial Set Time for Fault Detection (T_{SETI}) is the total time allowed in PWM Regulation before the PMOS Gate is turned off and shutdown. The constant $T_{SETI(1µF)}$ is measured and can be used to calculate T_{SETI}. The constant includes extension (1µF) to indicate that the time is for a 1µF capacitor and needs to be scaled by C_{TMR} in µF's. T_{SETI} can be calculated using the equations below:

$$T_{SET1} = C_{TMR} \bullet \frac{V_{GTH}}{I_{TPU}}$$

$$T_{SET1} = C_{TMR} \bullet T_{SET(1µF)}$$

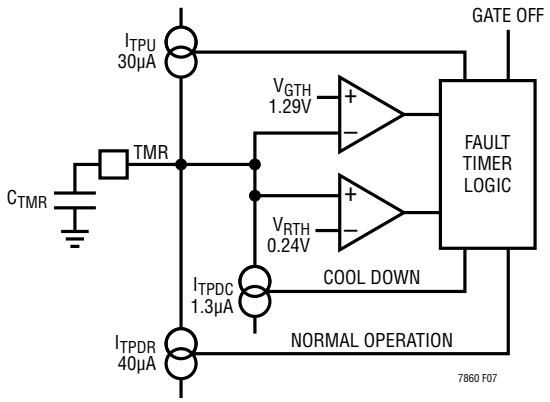

Figure 6. Timer (TMR) Functional Diagram

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The TMR Reset Cool Down Time is T_{RSTC} and is the total time allowed for the system to cool down before the PMOS Gate is turned on again after a fault. The constant $T_{RSTC(1\mu F)}$ is measured and can be used to calculate T_{RSTC}. The constant includes extension (1µF) to indicate that the time is for a 1µF capacitor and needs to be scaled by C_{TMR} in µF's. T_{RSTC} can be calculated using the equations below:

$$T_{RSTC} = C_{TMR} \bullet \frac{V_{GTH} - V_{RTH}}{I_{TPDC}}$$

$$T_{RSTC} = C_{TMR} \bullet T_{RSTC(1\mu F)}$$

T_{SETI} determines how long the switcher is allowed to switch before shutting down. T_{RSTC} determines how long the switcher cools down before the PMOS Gate can be turned on again. For a single fault exceeding T_{SET1}, that shuts down the Switching Surge Stopper, it will restart after the TMR Reset Cooldown period (T_{RSTC}).

In the case of a sustained fault the TMR pin rises after the cool down period expires. In a sustained fault, the TMR pin will pull up from the V_{RTH} threshold. The TMR Set Time Repeat after cool down is T_{SETR}. The constant $T_{SETR(1\mu F)}$ is measured and can be used to calculate T_{SETR}. The constant includes extension (1µF) to indicate that the value is for a 1µF capacitor and needs to be scaled by C_{TMR} in µF's. T_{SETR} can be calculated using the equations below:

$$T_{SETR} = C_{TMR} \bullet \frac{V_{GTH} - V_{RTH}}{I_{TPU}}$$

$$T_{SETR} = C_{TMR} \bullet T_{SET(1\mu F)}$$

In a sustained fault, the Switching Surge Stopper will continuously start, shutdown, cool down and restart at a fixed duty factor. The TMR Reset duty cycle in a sustained fault is DTY_{TSTR}. DTY_{TSTR} is measured and is calculated according to the equation below.

$$DTY_{TSTR} = \frac{T_{SETR}}{T_{RSTC}}$$

Design Example

A Switching Surge Stopper can be designed for performance in normal operation or SWITCH-ON mode. Its components and thermal design are optimized for normal operation and safely operate through high voltage input surges and/or overcurrent faults. Transient operation due to surges and other faults can be survived because the time in regulation is strictly limited when power loss is high. The principle design criterion in normal operation is the total resistance from V_{IN} to V_{OUT} with the resulting power loss and thermal considerations.

As a design example, take an application with the following specifications: V_{IN} = 8V to 14V DC with an input voltage transient of 60V and a decay constant of 500ms, V_{OUT} < 18V, with a continuous output load current rating of 5A.

We choose a P-channel MOSFET with the appropriate BV_{DSS} and I_D rating. In this example a good choice is the Vishay Si7461DP (BV_{DSS} = 60V, $R_{DS(ON)}$ = 11.5mΩ (typ), ρ120 = 1.6). The expected power dissipation from the P-channel in normal operation or SWITCH-ON mode can be calculated at T_J = 120°C for V_{IN} at 12V and I_{OUT} equal to 5A.

$$P_{PMOS} = I_{OUT}^2 \bullet R_{DS(ON)} = 5A^2 \bullet 14.5m\Omega\,(1.6) = 580mW$$

Next, set the inductor value to give 70% ripple current at maximum V_{IN} = 60V.

$$L = \left(\frac{17.2V}{540kHz \bullet (0.7 \bullet 5A)}\right)\left(1 - \frac{17.2V}{60V}\right) = 6.5\mu H$$

Select 6.8µH as the nearest standard value. A good choice for this application is the Coilcraft XAL6060-682ME, with a DCR value of 19mΩ. The resulting ripple current is:

$$I_{RIPPLE} = \left(\frac{17.2V}{540kHz \bullet 6.8\mu H}\right)\left(1 - \frac{17.2V}{60V}\right) = 3.33A$$

APPLICATIONS INFORMATION

The output voltage is programmed according to:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_{FB2}}{R_{FB1}}\right)$$

If R_{FB2} is chosen at 1M, then R_{FB1} is 48.7k.

The FREQ pin is floated in order to program the switching frequency to 540kHz. The on-time required at 60V to generate 17.2V output can be calculated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \bullet f} = \frac{17.2V}{60V \bullet 540kHz} = 531ns$$

This on-time is larger than the LTC7860's minimum on-time with sufficient margin to prevent cycle skipping.

Set the R_{SENSE} resistor value to ensure the converter can deliver a maximum output current of 5.0A during an input surge with sufficient margin to account for component variations and worst-case R_{SENSE} data sheet tolerance.

$$R_{SENSE} = \frac{85mV}{1.05 \bullet \left(5A + \frac{3.33A}{2}\right)} = 12.1m\Omega$$

The nearest standard value for R_{SENSE} is 12mΩ.

The current limit in Normal Operation or SWITCH-ON mode is not reduced by the ripple current and is:

$$I_{LIMIT(SURGE)} = \frac{95mV}{12m\Omega} = 7.9A$$

R_{SENSE} power loss for normal operation and at current limit can be calculated according to the equations below.

$$P_{RSENSE} = I_{OUT}^2 \bullet R_{SENSE} = 5A^2 \bullet 12m\Omega = 300mW$$

$$P_{RSENSE} = I_{OUT}^2 \bullet R_{SENSE} = 7.9A^2 \bullet 12m\Omega = 750mW$$

Select a 12mΩ resistor capable of dissipating at least one watt.

The average output current limit during a surge is the Normal Operation current limit minus half the ripple current. The maximum current delivered during a surge will always be less than in Normal Operation or SWITCH-ON mode.

$$I_{LIMIT(SURGE)} = \frac{95mV}{12m\Omega} - \frac{3.33}{2} = 6.25A$$

The total SWITCH-ON resistance R_{SW-ON} from V_{IN} to V_{OUT} is:

$$R_{SW-ON} = R_{SENSE} + R_{DS(ON)} + R_{INDUCTOR}$$

$$R_{SW-ON} = 12m\Omega + 11.5m\Omega \bullet (1.6) + 19m\Omega = 49.4m\Omega$$

The total insertion loss in Normal Operation or SWITCH-ON mode can be calculated below.

$$V_{DROP} = I_{OUT} \bullet R_{SW-ON} = 5A \bullet 49.4m\Omega = 247mW$$

The system will need to be designed to operate in this mode continuously. Temperature rise during a surge or fault operation will be limited by the timer.

Choose an appropriate diode that will handle the power requirements during the surge or fault condition. The diode will never engage during normal operation or SWITCH-ON mode but only during a surge or fault. The PDS5100-13 Schottky diode is selected ($V_{F(5A,\ 125°C)}$ = 0.60V) for this application. The continuous current rating of 5A is sufficient during the TMR limited PROTECTIVE PWM operation. The power dissipated during a surge or fault is.

$$P_{DIODE(SURGE)} = 5A \bullet \left(1 - \frac{17.2V}{60V}\right) \bullet 0.60V = 2.14W$$

A soft-start time of 8ms can be programmed through a 0.1µF capacitor on the SS pin:

$$C_{SS} = \frac{8ms \bullet 10\mu A}{0.8V} = 0.1\mu F$$

APPLICATIONS INFORMATION

A 700ms minimum time limit was chosen based on input surge specifications. We will calculate C_{TMR} for the worst case using $T_{SET(1\mu F)}$ minimum and allow for a 10% tolerance and a 10% variation in capacitance over temperature. We can calculate the required C_{TMR} by using $T_{SET(1\mu F)MIN}$ according to the equation below.

$$C_{TMR} = \frac{T_{SETIMIN}}{T_{SET(1\mu F)MIN}} \bullet \frac{1}{0.9} \bullet \frac{700}{37} \bullet \frac{1}{0.9} = 21\mu F$$

The nearest standard value for C_{TMR} is 22µF which results in the TMR Set Time Initial or T_{SETI} values given by the equations below. We assume 10% tolerance for capacitors over temperature.

$T_{SETITYP} = T_{SET(1\mu F)} \bullet 22\mu F = 44 \bullet 22\mu F = 968ms$

$T_{SETIMIN} = T_{SET(1\mu F)} \bullet 22\mu F = 37 \bullet 22\mu F \bullet 0.90 = 732ms$

$T_{SETIMAX} = T_{SET(1\mu F)} \bullet 22\mu F = 50 \bullet 22\mu F \bullet 1.1 = 1210ms$

Once T_{SET} is tripped there will be a defined TMR Reset Cool Down Time $T_{RSTCTYP}$.

$T_{RSTCTYP} = T_{RSTC(1\mu F)}) \bullet 22\mu F = 732 \bullet 22\mu F = 16.1s$

Loop compensation components on the ITH pin are chosen based on load step transient behavior (as described under OPTI-LOOP Compensation) and optimized for stability. Compensation is chosen to be 680pF and 10K.

GATE DRIVER COMPONENT PLACEMENT, LAYOUT AND ROUTING

It is important to follow recommended power supply PC board layout practices such as placing external power elements to minimize loop area and inductance in switching paths. Be careful to pay particular attention to gate driver component placement, layout and routing.

We recommend a ceramic 0.47µF 16V capacitor with a high quality dielectric such as X5R or X7R. Some high current applications with large Qg PMOS switches may benefit from an even larger C_{CAP} capacitance. The effective C_{CAP} capacitance should be greater than 0.1µF minimum in all operating conditions. Operating voltage and temperature both decrease the rated capacitance to varying degrees depending on dielectric type. The LTC7860 is a PMOS controller with an internal gate driver and boot-strapped LDO that regulates the differential CAP voltage ($V_{IN} - V_{CAP}$) to 8V nominal. The C_{CAP} capacitance needs to be large enough to assure stability and provide cycle-to-cycle current to the PMOS switch with minimum series inductance.

Figure 7 shows the LTC7860 Generic Application Schematic which includes an optional current sense filter and series gate resistor. Figure 8 illustrates the recommended gate driver component placement, layout and routing of the GATE, V_{IN}, SENSE and CAP pins and key gate driver components. It is recommended that the gate driver layout follow the example shown in Figure 8 to assure proper operation and long term reliability.

The LTC7860 gate driver should connect to the external power elements in the following manner. First route the V_{IN} pin using a single low impedance isolated trace to the positive R_{SENSE} resistor PAD without connection to the V_{IN} plane. The reason for this precaution is that the V_{IN} pin is internally Kelvin connected to the current sense comparator, internal V_{IN} power and the PMOS gate driver.

Connecting the V_{IN} pin to the V_{IN} power plane adds noise and can result in jitter or instability. Figure 8 shows a single V_{IN} trace from the positive R_{SENSE} pad connected to C_{SF}, C_{CAP}, V_{IN} pad and C_{INB}. The total trace length to R_{SENSE} should be minimized and the capacitors C_{CF}, C_{CAP} and C_{INB} should be placed near the V_{IN} pin of the LTC7860.

C_{CAP} should be placed near the V_{IN} and CAP pins. Figure 8 shows C_{CAP} placed adjacent to the V_{IN} and CAP pins with SENSE routed between the pads. This is the recommended layout and results in the minimum parasitic inductance. The gate driver is capable of providing high peak current. Parasitic inductance in the gate drive and the series inductance between V_{IN} to CAP can cause a voltage spike between V_{IN} and CAP on each switching cycle. The voltage spike can result in electrical over-stress to the gate driver and can result in gate driver failures in extreme cases. It is recommended to follow the example shown in Figure 8 for the placement of C_{CAP} as close as is practical.

R_{GATE} resistor pads can be added with a 1Ω resistor to allow the damping resistor to be added later. The total length of the gate drive trace to the PMOS gate should be minimized and ideally be less than 1cm. In most cases with a good layout the R_{GATE} resistor is not needed. The R_{GATE} resistor should be located near the gate pin to reduce peak current through GATE and minimize reflected noise on the gate pin.

The R_{SF} and C_{SF} pads can be added with a zero ohm resistor for R_{SF} and C_{SF} not populated. In most applications, external filtering is not needed. The current sense filter R_{SF} and C_{SF} can be added later if noise if demonstrated to be a problem.

The bypass capacitor C_{INB} is used to locally filter the V_{IN} supply. C_{INB} should be tied to the V_{IN} pin trace and to the PGND exposed pad. The C_{INB} positive pad should connect to R_{SENSE} positive though the V_{IN} pin trace. The C_{INB} ground trace should connect to the PGND exposed pad connection.

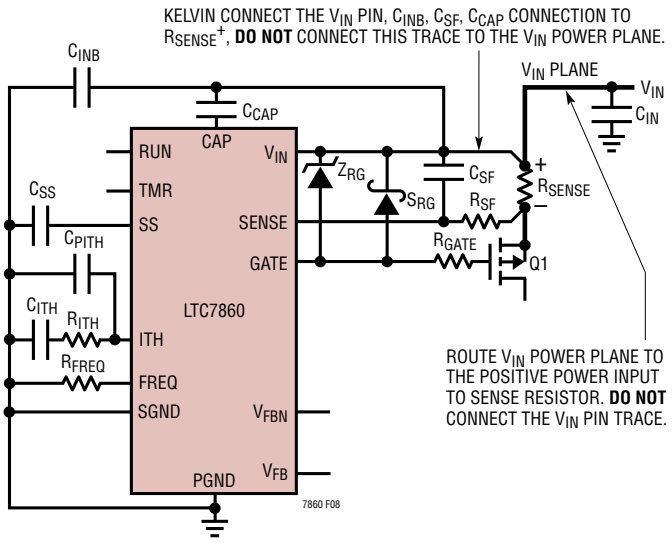


Figure 7. LTC7860 Generic Application Schematic with Optional Current Sense Filter and Series Gate Resistor

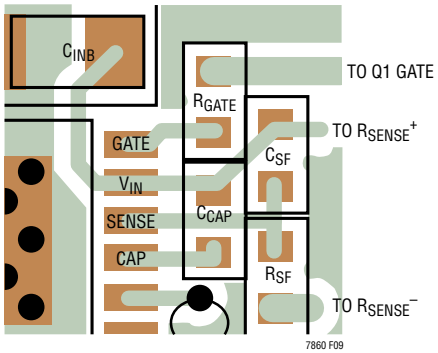


Figure 8. LTC7860 Recommended Gate Driver PC Board Placement, Layout and Routing

The Zener Z_{RG} and Schottky S_{RG} are recommended when driving large Power MOSFET's and should always be used in combination with R_{GATE} equal to 1Ω. We recommend using a 9.1V Zener in parallel with a Schottky diode when either the rise or fall time is measured to be greater than 30ns. The purpose of the diodes is to protect the internal multi-Amp gate driver against possible electrical over stress when switching the high capacitance power MOSFET Gate through an inductive gate trace at high current.

APPLICATIONS INFORMATION

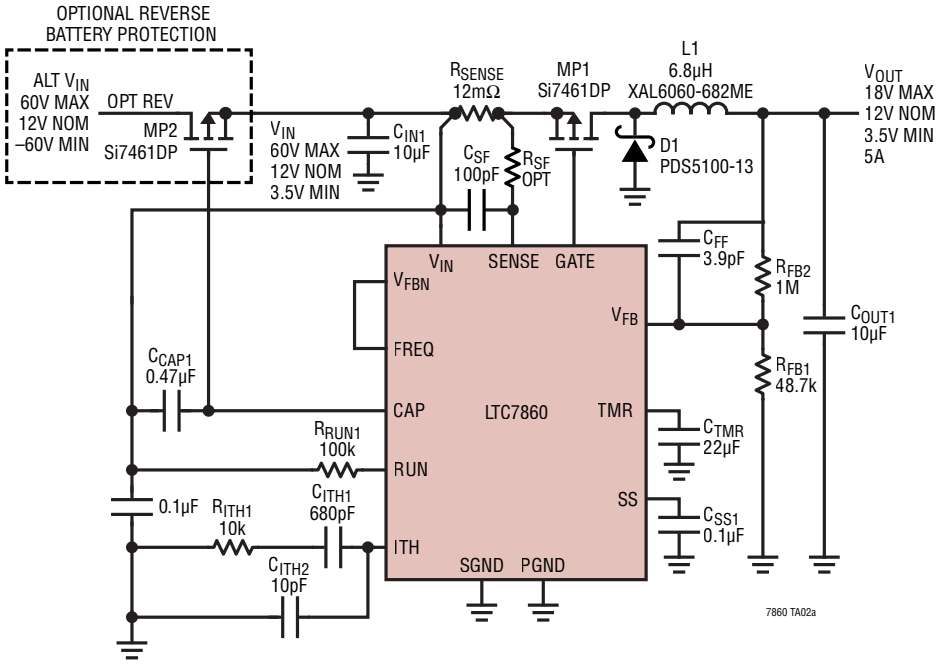
PC BOARD LAYOUT CHECKLIST

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC7860.

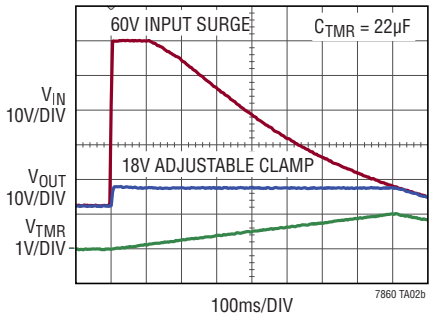
1. Multilayer boards with dedicated ground layers are preferable for reduced noise and for heat sinking purposes. Use wide rails and/or entire planes for V_{IN}, V_{OUT} and GND for good filtering and minimal copper loss. If a ground layer is used, then it should be immediately below (and/or above) the routing layer for the power train components which consist of C_{IN}, sense resistor, P-channel MOSFET, Schottky diode, inductor, and C_{OUT}. Flood unused areas of all layers with copper for better heat sinking.
2. Keep signal and power grounds separate except at the point where they are shorted together. Short the signal and power ground together only at a single point with a narrow PCB trace (or single via in a multilayer board). All power train components should be referenced to power ground and all small-signal components (e.g., C_{ITH1}, R_{FREQ}, C_{SS} etc.) should be referenced to the signal ground.
3. Place C_{IN}, sense resistor, P-channel MOSFET, inductor, and primary C_{OUT} capacitors close together in one compact area. The junction connecting the drain of the P-channel MOSFET, cathode of the Schottky, and (+) terminal of the inductor (this junction is commonly referred to as switch or phase node) should be compact but be large enough to handle the inductor currents without large copper losses. Place the sense resistor and source of P-channel MOSFET as close as possible to the (+) plate of the C_{IN} capacitor(s) that provides the bulk of the AC current (these are normally the ceramic capacitors), and connect the (–) terminal of the inductor as close as possible to the (–) terminal of the same C_{IN} capacitor(s). The high dI/dt loop formed by C_{IN}, the MOSFET, and the Schottky diode should have short leads and PCB trace lengths to minimize high frequency EMI and voltage stress from inductive ringing. The (+) terminal of the primary C_{OUT} capacitor(s) which filter the bulk of the inductor ripple current (these are normally the ceramic capacitors) should also be connected close to the (–) terminal of C_{IN}.
4. Place Pins 7 to 12 facing the power train components. Keep high dV/dt signals on GATE and switch away from sensitive small-signal traces and components.
5. Place the sense resistor close to the (+) terminal of C_{IN} and source of P-channel MOSFET. Use a Kelvin (4-wire) connection across the sense resistor and route the traces together as a differential pair into the V_{IN} and SENSE pins. An optional RC filter could be placed near the V_{IN} and SENSE pins to filter the current sense signal.
6. Place the feedback divider $R_{FB1/2}$ as close as possible to the V_{FB} and V_{FBN} pins. The (–) terminal of the feedback divider should connect to the output regulation point and the (+) terminal of the feedback divider should connect to V_{FB}.
7. Place the ceramic C_{CAP} capacitor as close as possible to the V_{IN} and CAP pins. This capacitor provides the gate discharging current for the power P-channel MOSFET.
8. Place small signal components as close to their respective pins as possible. This minimizes the possibility of PCB noise coupling into these pins. Give priority to V_{FB}, ITH, and FREQ pins.

TYPICAL APPLICATIONS

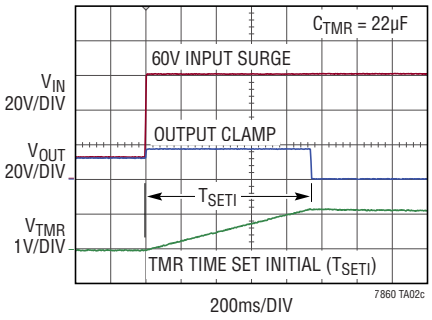
3.5V to 60V Input, 12V/18V Maximum 5A Output at 535kHz



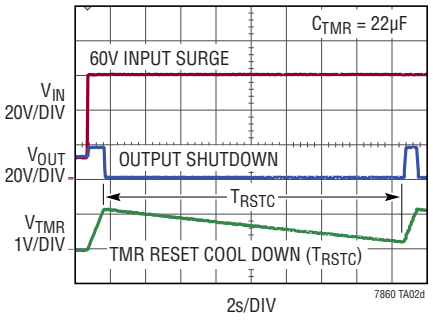
PROTECTIVE PWM: V_{OUT} Clamped to 18V During a V_{IN} Surge



PROTECTIVE PWM: V_{OUT} Clamped for TMR Timer Set Initial (T_{SETI})

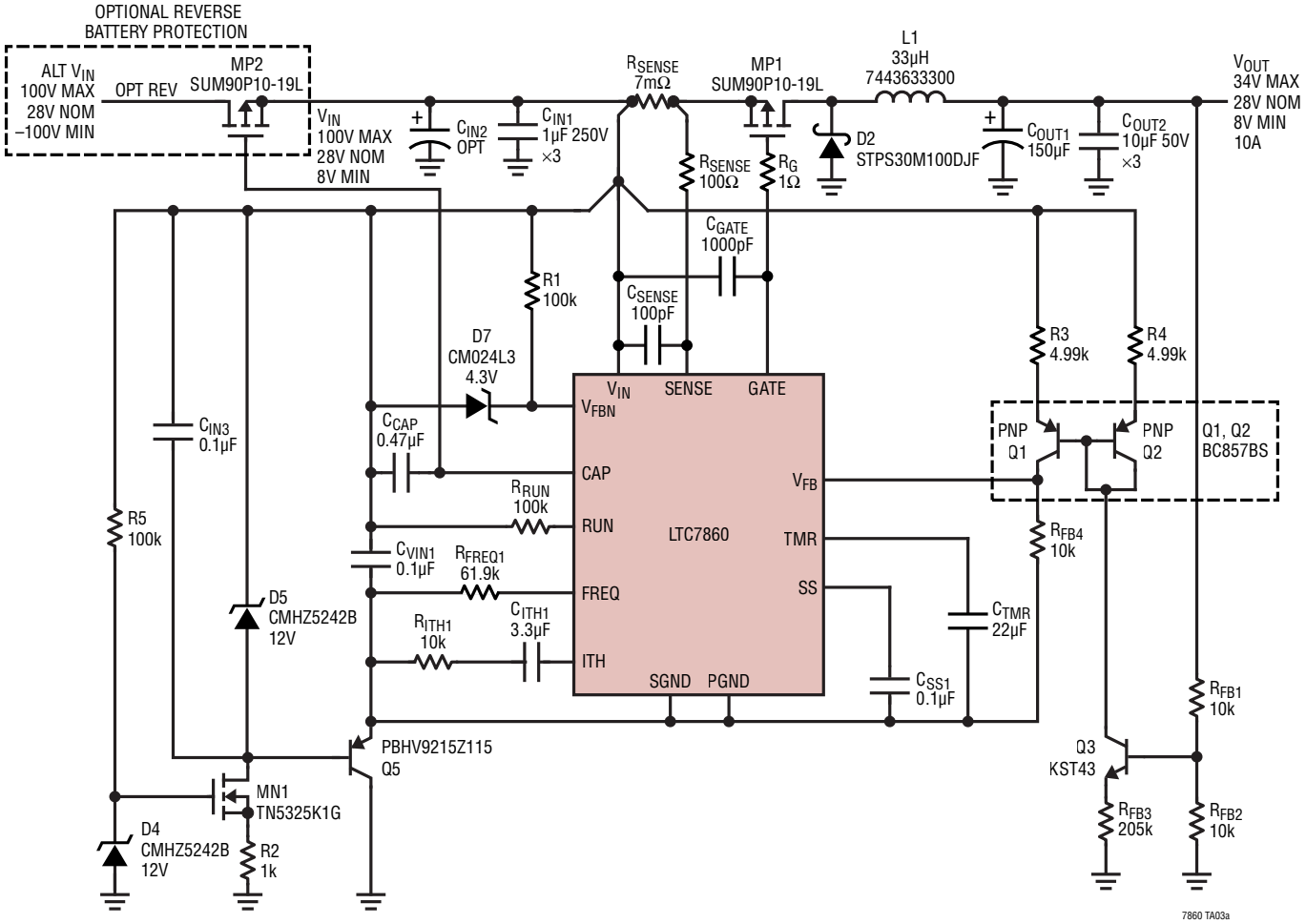


PROTECTIVE PWM: V_{OUT} Shutdown for TMR Reset Cool Down (T_{RSTC})

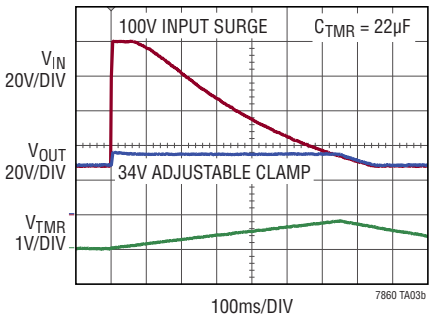


TYPICAL APPLICATIONS

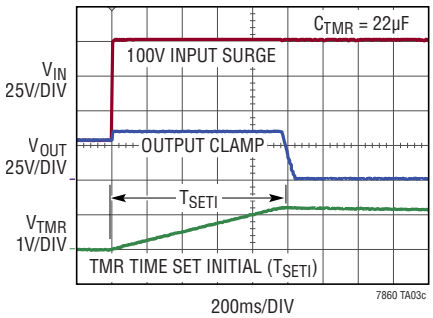
8V to 100V Input, 28V Nominal/34V Maximum, 10A Output at 400kHz with Non-Inverting Feedback Option



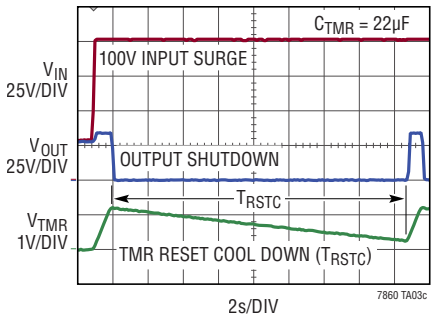
PROTECTIVE PWM: V_{OUT} Clamped to 34V During a V_{IN} Surge



PROTECTIVE PWM: V_{OUT} Clamped for TMR Timer Set Initial (T_{SETI})



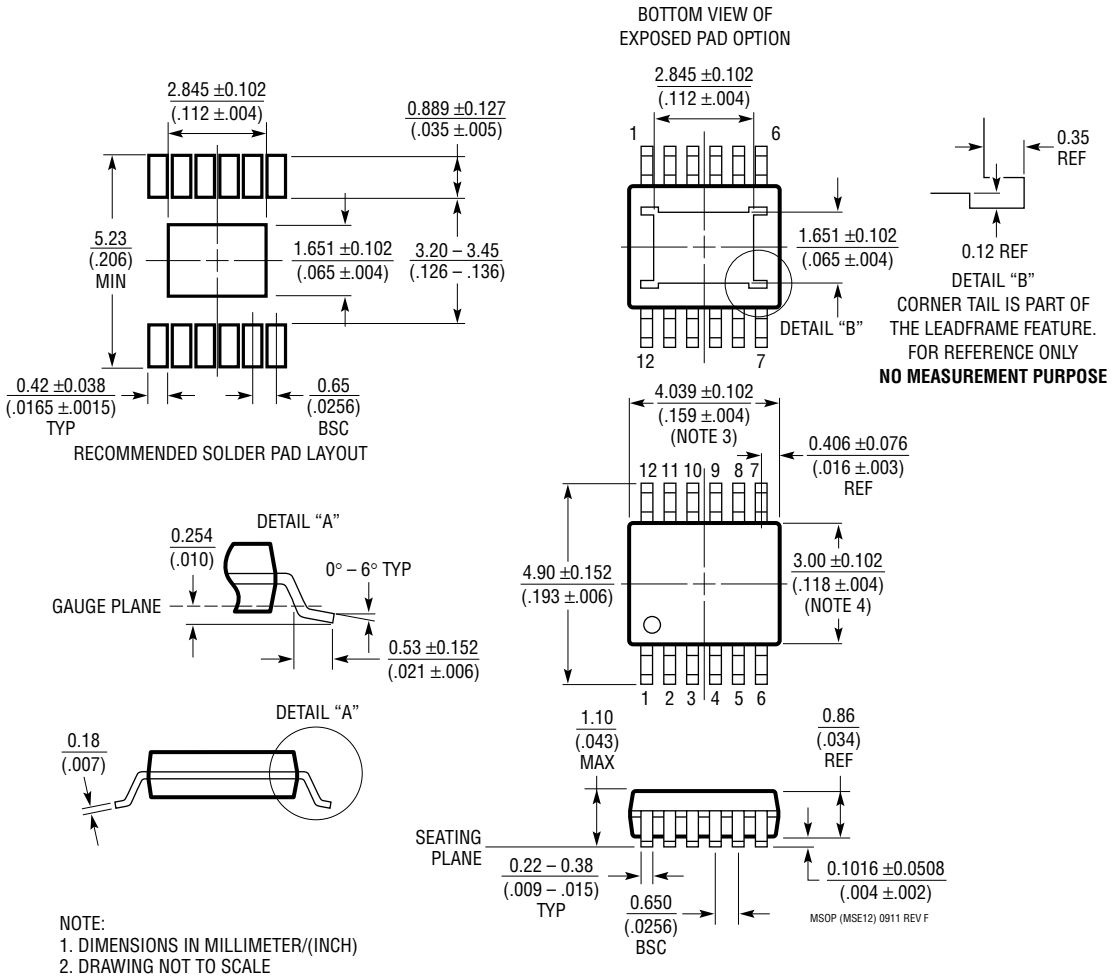
PROTECTIVE PWM: V_{OUT} Shutdown for TMR Reset Cool Down (T_{RSTC})



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.