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SPI/Digital or I²C µModule Isolator

FEATURES

- **6-Channel Logic Isolator: 3500V_{RMS} for 1 Minute**
- **UL-CSA Recognized File #E151738**
- **3V to 5.5V Supply Operation**
- **No External Components Required**
- **SPI/Digital (LTM2892-S) or I²C (LTM2892-I) Options**
- **High Common Mode Transient Immunity: 50kV/µs**
- **High Speed Operation:**
  - **10MHz Digital Isolation**
  - **4MHz/8MHz SPI Isolation**
  - **400kHz I²C Isolation**
- Operation Up to 125°C (H-Grade)
- 1.62V to 5.5V Logic Supplies for Flexible Digital Interfacing
- ±15kV ESD HBM Across the Isolation Barrier
- Maximum Continuous Working Voltage: 850V_{PEAK}
- Low Current Shutdown Mode (<10µA)
- Small (9mm × 6.25mm × 2.91mm) BGA Package

DESCRIPTION

The LTM®2892 is a complete galvanic digital µModule® (micromodule) isolator. No external components are required. Individual 3V to 5.5V supplies power each side of the digital isolator. Separate logic supply pins allow easy interfacing with different logic levels from 1.62V to 5.5V, independent of the main supply.

Module options are available with compatibility to SPI (LTM2892-S) and I²C (LTM2892-I), master mode only, specifications.

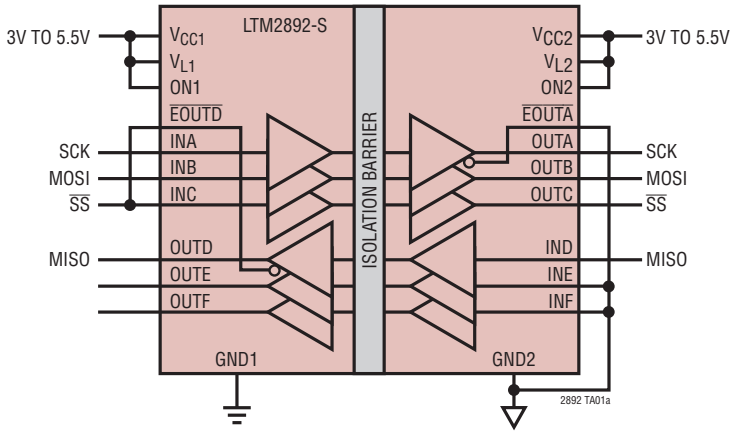
Coupled inductors provide 3500V_{RMS} of isolation between the input and output logic interface. This device is ideal for systems where the ground loop is broken, allowing uninterrupted communication through large common mode transients faster than 50kV/µs.

APPLICATIONS

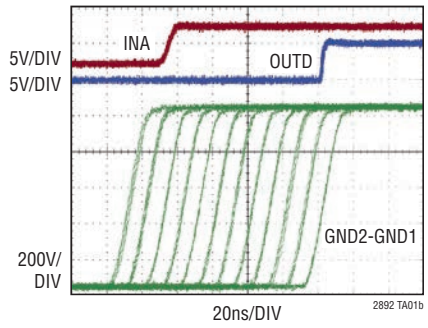
- Isolated SPI or I²C Interfaces
- Industrial Systems
- Test and Measurement Equipment
- Breaking Ground Loops

TYPICAL APPLICATION

Isolated 4MHz SPI Interface



LTM2892 Operating Through 50kV/µs CM Transients



OUTA CONNECTED TO IND

ABSOLUTE MAXIMUM RATINGS

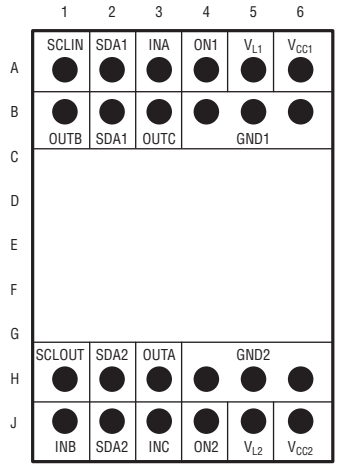
(Note 1)

V_{CC1} to GND1 ..... –0.3V to 6V
V_{L1} to GND1 ..... –0.3V to 6V
V_{CC2} to GND2 ..... –0.3V to 6V
V_{L2} to GND2 ..... –0.3V to 6V
Logic Inputs
INA, INB, INC, SCLIN, SDA1, $\overline{EOUTD}$,
ON1 to GND1 ..... –0.3V to (V_{L1} + 0.3V)
INB, INC, IND, INE, INF, SDA2, $\overline{EOUTA}$,
ON2 to GND2 ..... –0.3V to (V_{L2} + 0.3V)
Logic Outputs
OUTB, OUTC, OUTD, OUTE,
OUTF to GND1 ..... – 0.3V to (V_{L1} + 0.3V)
OUTA, OUTB, OUTC,
SCLOUT to GND2 ..... – 0.3V to (V_{L2} + 0.3V)
Operating Temperature Range (Note 4)
LTM2892C ..... 0°C to 70°C
LTM2892I ..... –40°C to 85°C
LTM2892H ..... –40°C to 125°C
Maximum Internal Operating Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 150°C
Peak Body Reflow Temperature ..... 260°C

PIN CONFIGURATION

LTM2892-I

TOP VIEW

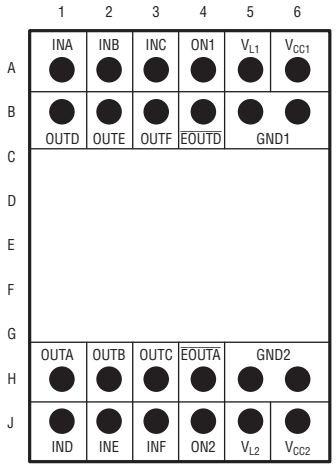


BGA PACKAGE
24-PIN (9mm × 6.25mm × 2.91mm)

T_{JMAX} = 125°C, θ_{JA} = 30°C/W, $\theta_{JC(bottom)}$ = 15.7°C/W,
$\theta_{JC(top)}$ = 25°C/W, θ_{JB} = 14.5°C/W
θ VALUES DETERMINED PER JESD 51-9, WEIGHT = 0.3g

LTM2892-S

TOP VIEW



BGA PACKAGE
24-PIN (9mm × 6.25mm × 2.91mm)

T_{JMAX} = 125°C, θ_{JA} = 30°C/W, $\theta_{JC(bottom)}$ = 15.7°C/W,
$\theta_{JC(top)}$ = 25°C/W, θ_{JB} = 14.5°C/W
θ VALUES DETERMINED PER JESD 51-9, WEIGHT = 0.3g

ORDER INFORMATION

http://www.linear.com/product/LTM2892#orderinfo

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM2892CY-I#PBF	LTM2892CY-I#PBF	LTM2892Y-I	24-Lead (9mm × 6.25mm × 2.91mm) BGA	0°C to 70°C
LTM2892IY-I#PBF	LTM2892IY-I#PBF	LTM2892Y-I	24-Lead (9mm × 6.25mm × 2.91mm) BGA	–40°C to 85°C
LTM2892HY-I#PBF	LTM2892HY-I#PBF	LTM2892Y-I	24-Lead (9mm × 6.25mm × 2.91mm) BGA	–40°C to 125°C
LTM2892CY-S#PBF	LTM2892CY-S#PBF	LTM2892Y-S	24-Lead (9mm × 6.25mm × 2.91mm) BGA	0°C to 70°C
LTM2892IY-S#PBF	LTM2892IY-S#PBF	LTM2892Y-S	24-Lead (9mm × 6.25mm × 2.91mm) BGA	–40°C to 85°C
LTM2892HY-S#PBF	LTM2892HY-S#PBF	LTM2892Y-S	24-Lead (9mm × 6.25mm × 2.91mm) BGA	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/
This product is moisture sensitive. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = 5V, V_{CC2} = 5V, V_{L1} = 3.3V, V_{L2} = 3.3V, GND1 = GND2 = 0V, ON1 = V_{L1}, and ON2 = V_{L2} unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supplies							
V_{CC1}, V_{CC2}	Input Supply Range		●	3		5.5	V
V_{L1}, V_{L2}	Logic Supply Range	LTM2892-S LTM2892-I	● ●	1.62 3		5.5 5.5	V V
I_{CC1}, I_{CC2}	Input Supply Current	ON1 = ON2 = 0V ON1 = V_{L1}, ON2 = V_{L2}	● ●		0 3.2	10 4.5	µA mA
I_{L1}, I_{L2}	Logic Supply Current	ON1 = ON2 = 0V LTM2892-S, ON1 = V_{L1}, ON2 = V_{L2} I_{L1}, LTM2892-I, ON1 = V_{L1}, ON2 = V_{L2} I_{L2}, LTM2892-I, ON1 = V_{L1}, ON2 = V_{L2}	● ●		0 10	10 150 300	µA µA µA µA
Logic/SPI							
V_{ITH}	Input Threshold Voltage	ON1, INx, $\overline{EOUTD}$, 1.62V ≤ V_{L1} < 2.35V ON1, INx, $\overline{EOUTD}$, 2.35V ≤ V_{L1} ON2, INx, $\overline{EOUTA}$, 1.62V ≤ V_{L2} < 2.35V ON2, INx, $\overline{EOUTA}$, 2.35V ≤ V_{L2}	● ● ● ●	0.25•V_{L1} 0.33•V_{L1} 0.25•V_{L2} 0.33•V_{L2}		0.75•V_{L1} 0.67•V_{L1} 0.75•V_{L2} 0.67•V_{L2}	V V V V
I_{INL}	Input Current		●			±1	µA
V_{HYS}	Input Hysteresis	(Note 2)			150		mV
V_{OH}	Output High Voltage	OUTx, I_{LOAD} = –1mA, 1.62V ≤ V_{L1} < 3V OUTx, I_{LOAD} = –4mA, 3V ≤ V_{L1} ≤ 5.5V OUTB (LTM2892-I), I_{LOAD} = –2mA, 3V ≤ V_{L1} ≤ 5.5V	●	V_{L1} – 0.4			V
		OUTx, I_{LOAD} = –1mA, 1.62V ≤ V_{L2} < 3V OUTx, I_{LOAD} = –4mA, 3V ≤ V_{L2} ≤ 5.5V	●	V_{L2} – 0.4			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = 5V, V_{CC2} = 5V, V_{L1} = 3.3V, V_{L2} = 3.3V, GND1 = GND2 = 0V, ON1 = V_{L1}, and ON2 = V_{L2} unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output Low Voltage	OUTx, I_{LOAD} = 1mA, 1.62V ≤ V_{L1} < 3V OUTx, I_{LOAD} = 4mA, 3V ≤ V_{L1} ≤ 5.5V OUTB (LTM2892-I), I_{LOAD} = 2mA, 3V ≤ V_{L1} ≤ 5.5V	●			0.4	V
		OUTx, I_{LOAD} = 1mA, 1.62V ≤ V_{L2} < 3V OUTx, I_{LOAD} = 4mA, 3V ≤ V_{L2} ≤ 5.5V	●			0.4	V
I_{SC}	Short-Circuit Current	0V ≤ OUTx ≤ V_{L1} 0V ≤ OUTB (LTM2892-I) ≤ V_{L1} 0V ≤ OUTx ≤ V_{L2}	● ●		 ±30 	±85 ±85	mA mA mA
I^2C							
V_{IL}	Low Level Input Voltage	SCLIN, SDA1 SDA2	● ●			0.3•V_{L1} 0.3•V_{L2}	V V
V_{IH}	High Level Input Voltage	SCLIN, SDA1 SDA2	● ●	0.7•V_{L1} 0.7•V_{L2}			V V
I_{INL}	Input Current	SCLIN, SDA1 = V_{L1} or 0V SDA2 = V_{L2}, SDA2 = V_{L2} = 0V	● ●			±1 ±1	µA µA
V_{HYS}	Input Hysteresis	SCLIN, SDA1 SDA2			0.05•V_{L1} 0.05•V_{L2}		mV mV
V_{OH}	Output High Voltage	SCLOUT, I_{LOAD} = –2mA	●	V_{L2} – 0.4			V
V_{OL}	Output Low Voltage	SDA1, I_{LOAD} = 3mA, SCLOUT, I_{LOAD} = 2mA SDA2 = No Load, SDA1 = 0V, 4.5V ≤ V_{L2} < 5.5V SDA2 = No Load, SDA1 = 0V, 3V ≤ V_{L2} < 4.5V	● ● ●		 0.3	0.4 0.45 0.55	V V V
C_{IN}	Input Pin Capacitance	SCLIN, SDA1, SDA2 (Note 2)	●			10	pF
C_B	Bus Capacitive Load	SCLOUT, Standard Speed (Note 2) SCLOUT, Fast Speed SDA1, SDA2, SR ≥ 1V/µs, Standard Speed (Note 2) SDA1, SDA2, SR ≥ 1V/µs, Fast Speed	● ● ● ●			400 200 400 200	pF pF pF pF
	SDA, SDA2 Slew Rate		●	1			V/µs
I_{SC}	Short-Circuit Current	SDA2 = 0, SDA1 = V_{L1} 0V ≤ SCLOUT ≤ V_{L2} SDA1 = 0, SDA2 = V_{L2} SDA1 = V_{L1}, SDA2 = 0	●		 ±30 6 –1.8	100	mA mA mA mA
ESD (HBM) (Note 2)							
	Isolation Boundary	GND2 to GND1 (V_{CC2}, V_{L2}, GND2) to (V_{CC1}, V_{L1}, GND1)			±15 ±10		kV kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = 5V, V_{CC2} = 5V, V_{L1} = 3.3V, V_{L2} = 3.3V, GND1 = GND2 = 0V, ON1 = V_{L1}, and ON2 = V_{L2} unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic/SPI							
	Maximum Data Rate	INx → OUTx, C_L = 15pF (Note 3) Bidirectional SPI Communication Unidirectional SPI Communication	● ● ●	10 4 8			MHz MHz MHz
t_{PHL}, t_{PLH}	Propagation Delay	INx → OUTx, C_L = 15pF (Figure 1)	●	35	60	100	ns
t_R, t_F	Rise and Fall Time	OUTx, C_L = 15pF (Figure 1) LTM2892-I, OUTB, C_L = 15pF (Figure 1)	● ●		3 20	12.5 35	ns ns
t_{PWU}	Output Pulse Width Uncertainty	OUTB, OUTC, OUTE, OUTF (Note 2)		–20		50	ns
t_{PZH}, t_{PZL}	Output Enable Time	$\overline{EOUTx}$ = ↓ to OUTx, R_L = 1k, C_L = 15pF (Figure 2)	●			50	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$\overline{EOUTx}$ = ↑ to OUTx, R_L = 1k, C_L = 15pF (Figure 2)	●			50	ns
t_{PZH}, t_{PZL}	ONx Enable Time	ONx = ↑ to OUTx, R_L = 1k, C_L = 15pF (Figure 4)	●			60	µs
t_{PHZ}, t_{PLZ}	ONx Disable Time	ONx = ↓ to OUTx, R_L = 1k, C_L = 15pF (Figure 4)	●			50	ns
I²C							
	Maximum Data Rate	(Note 3)	●	400			kHz
t_{PHL}, t_{PLH}	Propagation Delay	SCLIN → SCLOUT, C_L = 15pF (Figure 1) SDA1 → SDA2, R_L = Open, C_L = 15pF (Figure 3) SDA2 → SDA1, R_L = 1.1k, C_L = 15pF (Figure 3)	● ● ●		150 150 300	225 250 500	ns ns ns
t_R	Rise Time	SDA2, C_L = 200pF (Figure 3) SDA2, C_L = 200pF (Figure 3) SDA1, R_L = 1.1k, C_L = 200pF (Figure 3) SCLOUT, C_L = 200pF (Figure 3)	● ● ●	40 40 40		300 250 250 250	ns ns ns ns
t_F	Fall Time	SDA2, C_L = 200pF (Figure 3) SDA1, R_L = 1.1k, C_L = 200pF (Figure 3) SCLOUT, C_L = 200pF (Figure 3)	● ● ●	40 40		250 250 250	ns ns ns
t_{PWU}	Output Pulse Width Uncertainty	SDA1, SDA2 (Note 2)		–20		50	ns
t_{PZH}, t_{PZL}	ONx Enable Time	ON1 = ↑ to SDA1, R_L = 1k, C_L = 15pF (Figure 4) ON2 = ↑ to (SCLOUT, SDA2), C_L = 15pF (Figure 4)	● ●			60	µs
t_{PHZ}, t_{PLZ}	ONx Disable Time	ON1 = ↓ to SDA1, R_L = 1k, C_L = 15pF (Figure 4) ON2 = ↓ to SCLOUT, R_L = 1k, C_L = 15pF (Figure 4) ON2 = ↓ to SDA2, R_L = Open, C_L = 15pF (Figure 4)	● ● ●			50 50 225	ns ns ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns

ISOLATION CHARACTERISTICS T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage	1 Minute, Derived from 1 Second Test 1 Second (Notes 5, 6)	3500 4200			V_{RMS} V_{RMS}
	Common Mode Transient Immunity	V_{CC1} = V_{L1} = ON1 = 5V, V_{CC2} = V_{L2} = ON2 = 5V V_{CM} = 1kV, Δt = 20ns (Note 2)	50			kV/µs
V_{IORM}	Maximum Continuous Working Voltage	(Notes 2, 5)	850 600			V_{PEAK} V_{RMS}
	Partial Discharge	V_{PD} = 1590V_{PEAK} (Note 5)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 2)			0.1	mm
DTI	Distance Through Insulation	(Note 2)		0.1		mm
	Input to Output Resistance	(Notes 2, 5)	10^{12}			Ω
	Input to Output Capacitance	(Notes 2, 5)		3		pF
	Creepage Distance	(Note 2)		5		mm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not subject to production test.

Note 3: Maximum data rate is guaranteed by other measured parameters and is not tested directly.

Note 4: This µModule isolator includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

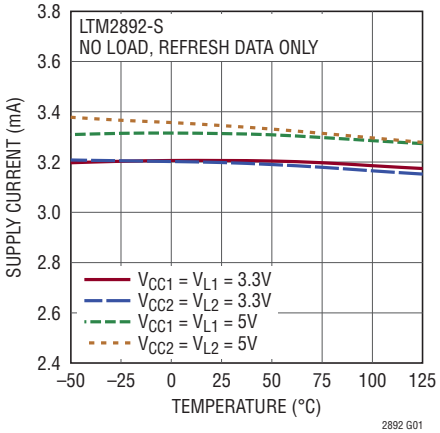
Note 5: Device is considered a 2-terminal device. Pin group A1 through B6 shorted together and pin group H1 through J6 shorted together.

Note 6: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

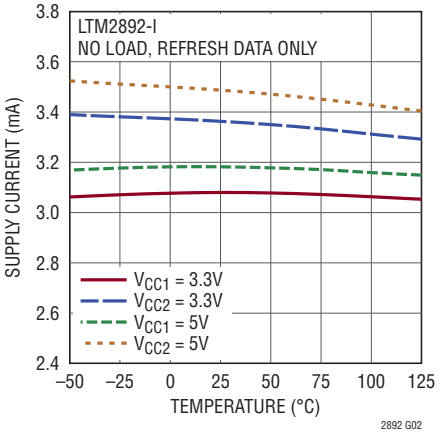
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC1} = 5V, V_{CC2} = 5V, V_{L1} = 3.3V, V_{L2} = 3.3V, GND1 = GND2 = 0V, ON1 = V_{L1}, and ON2 = V_{L2}, unless otherwise noted.

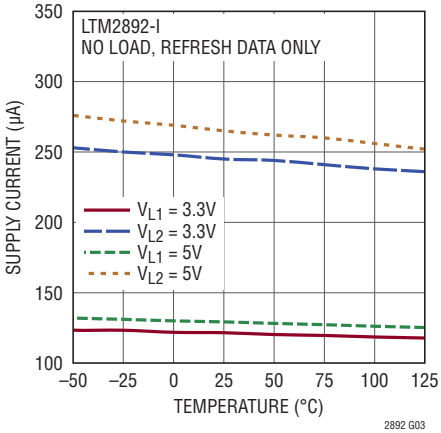
V_{CCx} and V_{Lx} Supply Current vs Temperature



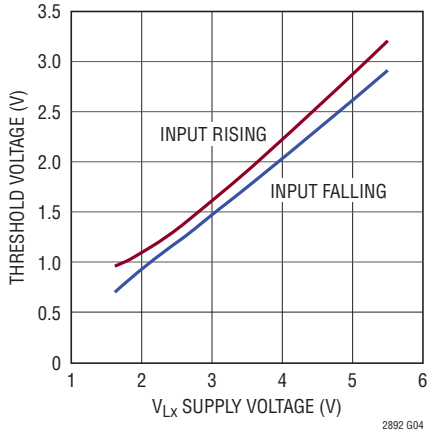
V_{CCx} Supply Current vs Temperature



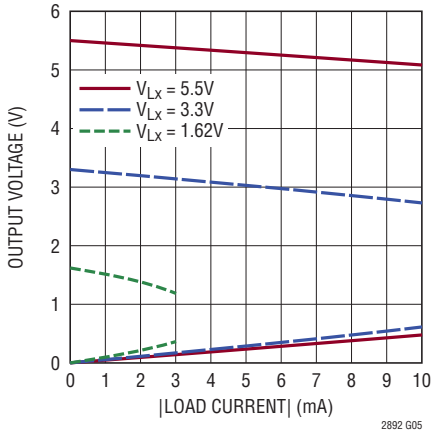
V_{Lx} Supply Current vs Temperature



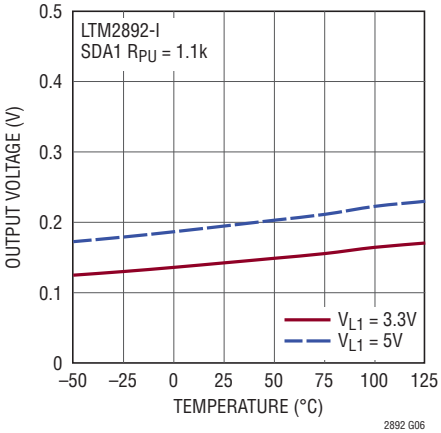
Logic Input Threshold vs V_{Lx} Supply Voltage



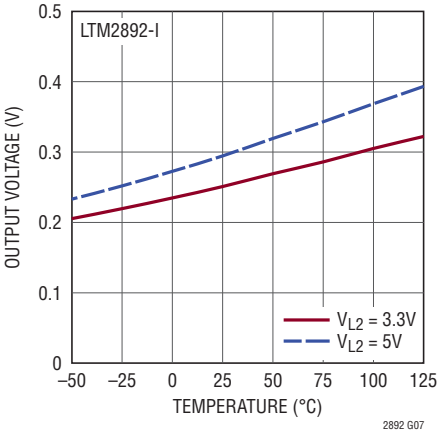
Logic Output Voltage vs Load Current



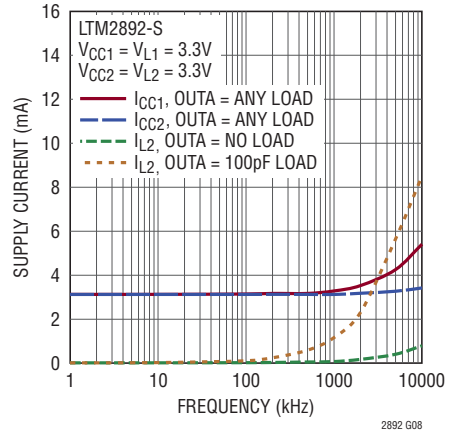
SDA1 Low Level Output Voltage vs Temperature



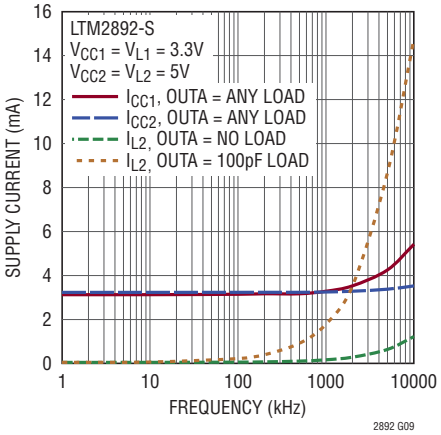
SDA2 Low Level Output Voltage vs Temperature



Supply Current vs INA to OUTA Data Rate



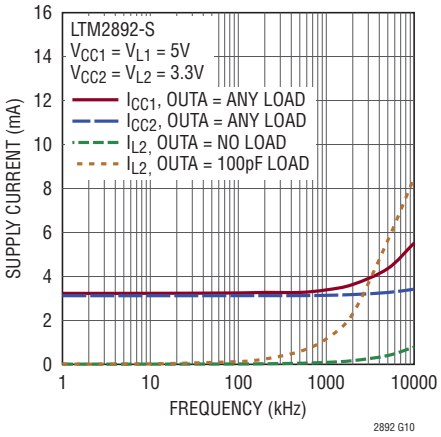
Supply Current vs INA to OUTA Data Rate



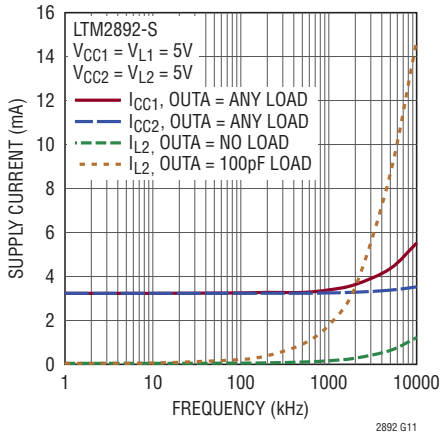
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC1} = 5V, V_{CC2} = 5V, V_{L1} = 3.3V, V_{L2} = 3.3V, GND1 = GND2 = 0V, ON1 = V_{L1}, and ON2 = V_{L2}, unless otherwise noted.

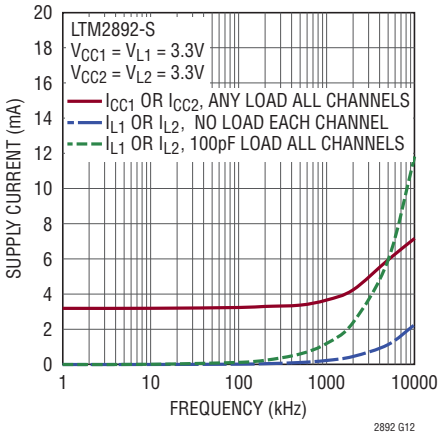
Supply Current vs INA to OUTA Data Rate



Supply Current vs INA to OUTA Data Rate



Supply Current vs Data Rate, All Channels



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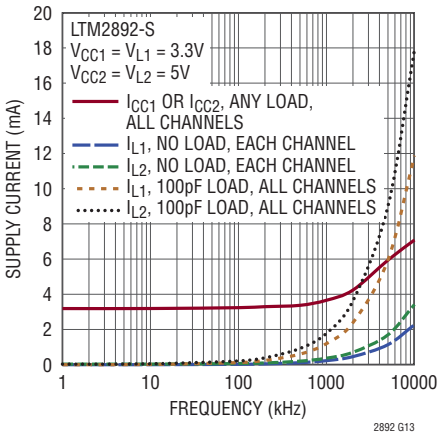
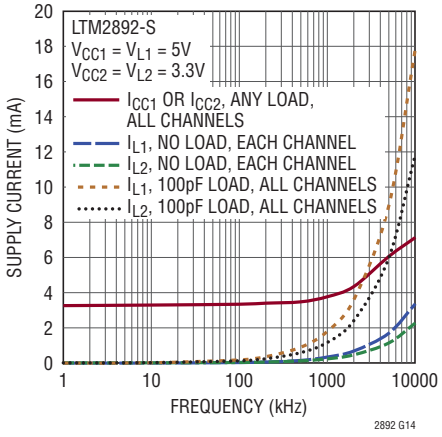
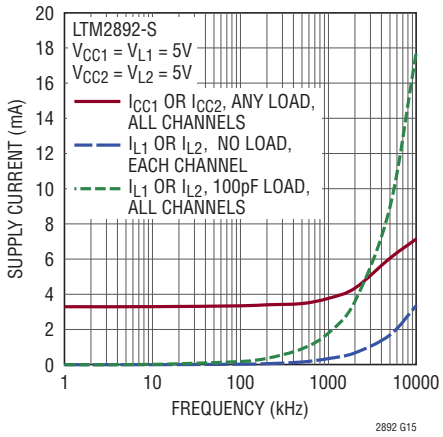


Supply Current vs Data Rate, All Channels



Supply Current vs Data Rate, All Channels



PIN FUNCTIONS (LTM2892-I)

Logic Side

SCLIN (A1): Serial I²C Clock Input, Referenced to V_{L1} and GND1. Logic input connected to isolated side SCLOUT pin through the isolation barrier. Clock is unidirectional from logic to isolated side. Pull up to V_{L1} if not used.

SDA1 (A2, B2): Serial I²C Data Pins, Referenced to V_{L1} and GND1. Bidirectional logic pins connected to isolated side SDA2 pins through the isolation barrier. Under the condition of an isolation communication failure pins are in a high impedance state. Pins connected internally. Pull up to V_{L1} if not used.

INA (A3): Digital Input, Referenced to V_{L1} and GND1. Logic input connected to OUTA through the isolation barrier. The logic state on INA translates to the same logic state on OUTA. Connect to GND1 or V_{L1} if not used.

ON1 (A4): Enable, Referenced to V_{L1} and GND1. Enables data communication through the isolation barrier. If ON1 is high the part is enabled and communications are functional to the isolated side. If ON1 is low the logic side is held in reset, all digital outputs are in a high impedance state. Connect to V_{L1} if not driven.

V_{L1} (A5): Logic Supply. Interface supply voltage for pins SCLIN, INA, OUTB, OUTC, and ON1. Operating voltage is 3V to 5.5V. Internally bypassed with 0.22µF.

V_{CC1} (A6): Supply Voltage. Operating voltage is 3V to 5.5V. Internally bypassed with 1.0µF.

OUTB (B1): Digital Output, Referenced to V_{L1} and GND1. Logic output connected to INB through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

OUTC (B3): Digital Output, Referenced to V_{L1} and GND1. Logic output connected to INC through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

GND1 (B4 to B6): Circuit Ground.

Isolated Side

SCLOUT (H1): Serial I²C Clock Output, Referenced to V_{L2} and GND2. Logic output connected to logic side SCLIN pin through the isolation barrier. Clock is unidirectional from logic to isolated side. SCLOUT has a push-pull output stage; do not connect an external pull-up device. Under the condition of an isolation communication failure this output defaults to a high state.

SDA2 (H2, J2): Serial I²C Data Pins, Referenced to V_{L2} and GND2. Bidirectional logic pins connected to logic side SDA1 pins through the isolation barrier. Output is biased high by a 1.8mA current source. Do not connect an external pull-up device to SDA2. Under the condition of an isolation communication failure outputs default to a high state. Pins connected internally.

OUTA (H3): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to INA through the isolation barrier. Under the condition of an isolation communication failure OUTA defaults to a high state.

GND2 (H3 to H5): Isolated Ground.

INB (J1): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to OUTB through the isolation barrier. The logic state on INB translates to the same logic state on OUTB. Connect to GND2 or V_{L2} if not used.

INC (J3): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to OUTC through the isolation barrier. The logic state on INC translates to the same logic state on OUTC. Connect to GND2 or V_{L2} if not used.

ON2 (J4): Enable, Referenced to V_{L2} and GND2. Enables data communication through the isolation barrier. If ON2 is high the part is enabled and communications are functional to the logic side. If ON2 is low the isolated side is held in reset, all digital outputs are in a high state. Connect to V_{L2} if not driven.

V_{L2} (J5): Logic Supply, Referred to GND2. Interface supply voltage for pins SCLOUT, SDA2, INB, INC, OUTA, and ON2. Operating voltage is 3V to 5.5V. Internally bypassed with 0.22µF.

V_{CC2} (J6): Supply Voltage, Referred to GND2. Operating voltage is 3V to 5.5V. Internally bypassed with 1.0µF.

PIN FUNCTIONS (LTM2892-S)

Logic Side

INA (A1): Digital Input, Referenced to V_{L1} and GND1. Logic input connected to OUTA through the isolation barrier. The logic state on INA translates to the same logic state on OUTA. Connect to GND1 or V_{L1} if not used.

INB (A2): Digital Input, Referenced to V_{L1} and GND1. Logic input connected to OUTB through the isolation barrier. The logic state on INB translates to the same logic state on OUTB. Connect to GND1 or V_{L1} if not used.

INC (A3): Digital Input, Referenced to V_{L1} and GND1. Logic input connected to OUTC through the isolation barrier. The logic state on INC translates to the same logic state on OUTC. Connect to GND1 or V_{L1} if not used.

ON1 (A4): Enable, Referenced to V_{L1} and GND1. Enables data communication through the isolation barrier. If ON1 is high the part is enabled and communications are functional to the isolated side. If ON1 is low the logic side is held in reset, all digital outputs are in a high impedance state. Connect to V_{L1} if not driven.

V_{L1} (A5): Logic Supply. Interface supply voltage for pins INA, INB, INC, OUTD, OUTE, OUTF, $\overline{EOUTD}$, and ON1. Operating voltage is 1.62V to 5.5V. Internally bypassed with 0.22µF.

V_{CC1} (A6): Supply Voltage. Operating voltage is 3V to 5.5V. Internally bypassed with 1.0µF.

OUTD (B1): Digital Output, Referenced to V_{L1} and GND1. Logic output connected to IND through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

OUTE (B2): Digital Output, Referenced to V_{L1} and GND1. Logic output connected to INE through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

OUTF (B3): Digital Output, Referenced to V_{L1} and GND1. Logic output connected to INF through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

$\overline{EOUTD}$ (B4): Digital Output Enable, Referenced to V_{L1} and GND1. A logic high on $\overline{EOUTD}$ places the logic side OUTD pin in a high impedance state, a logic low enables the output. Connect to GND1 or V_{L1} if not used.

GND1 (B5, B6): Circuit Ground.

Isolated Side

OUTA (H1): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to INA through the isolation barrier. Under the condition of an isolation communication failure OUTA defaults to a low state.

OUTB (H2): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to INB through the isolation barrier. Under the condition of an isolation communication failure OUTB defaults to a low state.

OUTC (H3): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to INC through the isolation barrier. Under the condition of an isolation communication failure OUTC defaults to a high state.

$\overline{EOUTA}$ (H4): Digital Output Enable, Referenced to V_{L2} and GND2. A logic high on $\overline{EOUTA}$ places the logic side OUTA pin in a high impedance state, a logic low enables the output. Connect to GND2 or V_{L2} if not used.

GND2 (H5, H6): Isolated Ground.

IND (J1): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to OUTD through the isolation barrier. The logic state on IND translates to the same logic state on OUTD. Connect to GND2 or V_{L2} if not used.

INE (J2): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to OUTE through the isolation barrier. The logic state on INE translates to the same logic state on OUTE. Connect to GND2 or V_{L2} if not used.

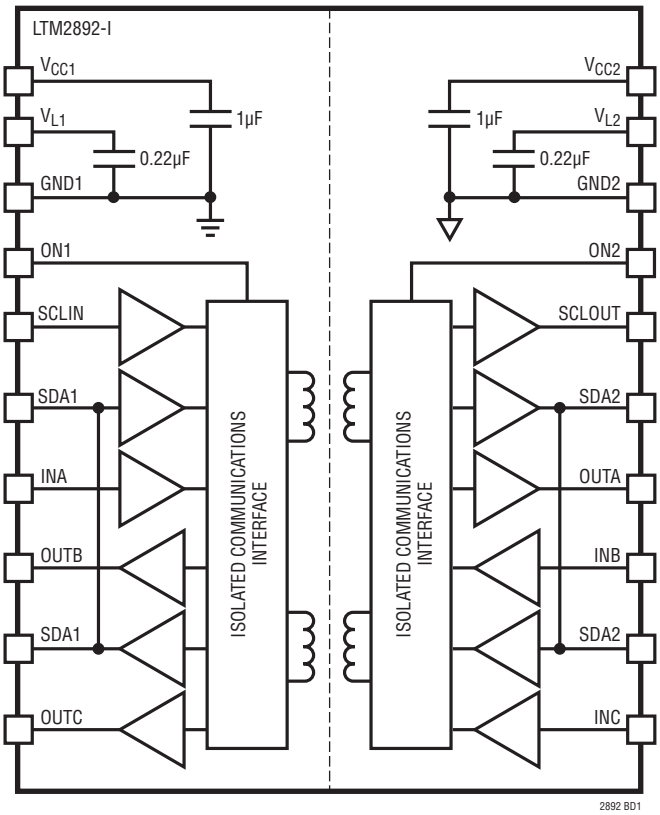
INF (J3): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to OUTF through the isolation barrier. The logic state on INF translates to the same logic state on OUTF. Connect to GND2 or V_{L2} if not used.

ON2 (J4): Enable, Referenced to V_{L2} and GND2. Enables data communication through the isolation barrier. If ON2 is high the part is enabled and communications are functional to the logic side. If ON2 is low the isolated side is held in reset, OUTA and OUTB are in a low state, and OUTC is in a high state. Connect to V_{L2} if not driven.

V_{L2} (J5): Logic Supply, Referred to GND2. Interface supply voltage for pins OUTA, OUTB, OUTC, IND, INE, INF, $\overline{EOUTA}$, and ON2. Operating voltage is 1.62V to 5.5V. Internally bypassed with 0.22µF.

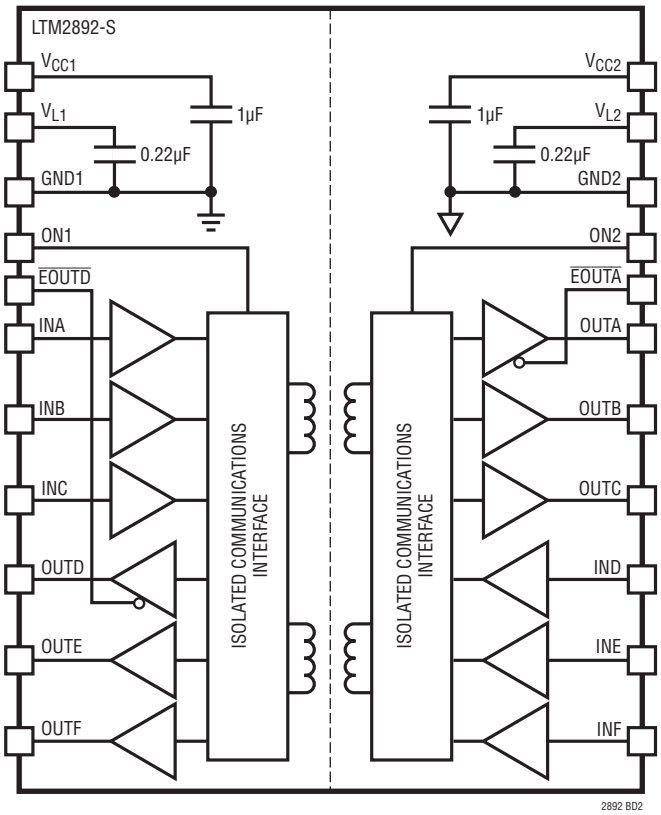
V_{CC2} (J6): Supply Voltage, Referred to GND2. Operating voltage is 3V to 5.5V. Internally bypassed with 1.0µF.

BLOCK DIAGRAMS



LTM2892-I

BLOCK DIAGRAMS



LTM2892-S

TEST CIRCUITS

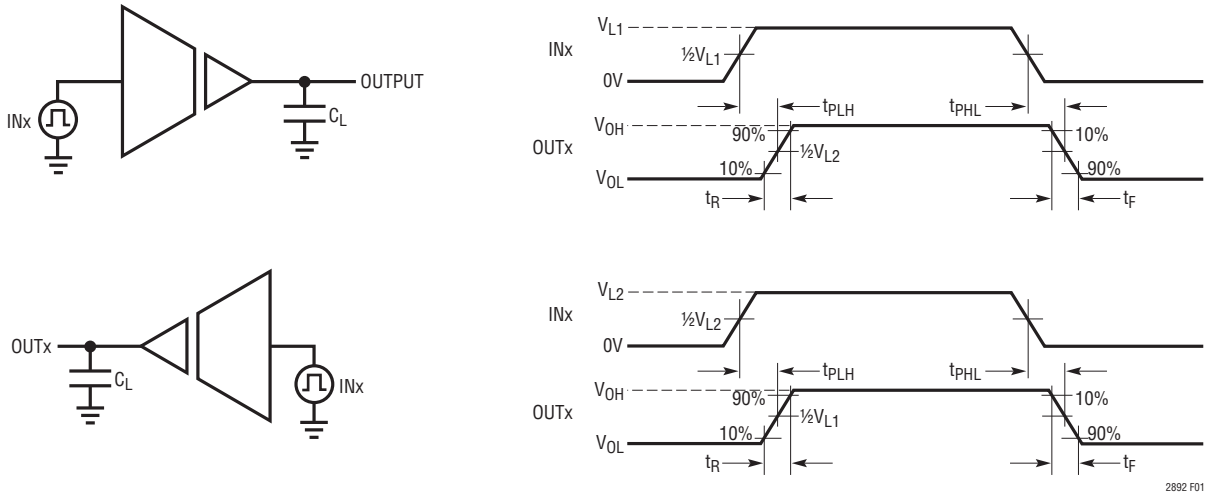


Figure 1. Logic Timing Measurements

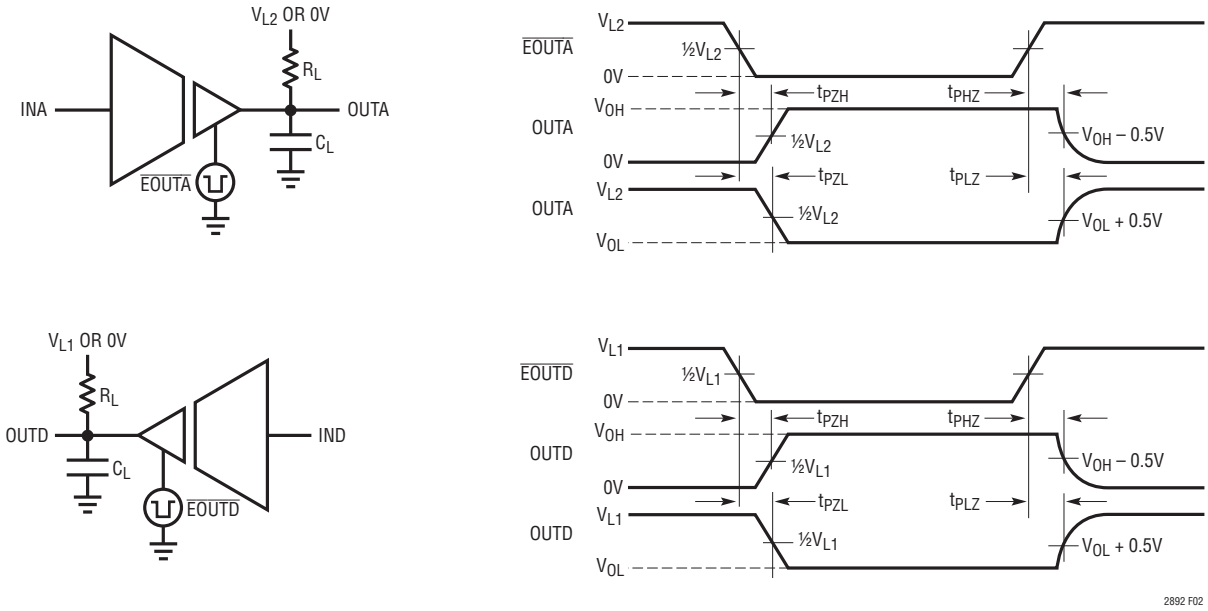


Figure 2. Logic Enable/Disable Time

TEST CIRCUITS

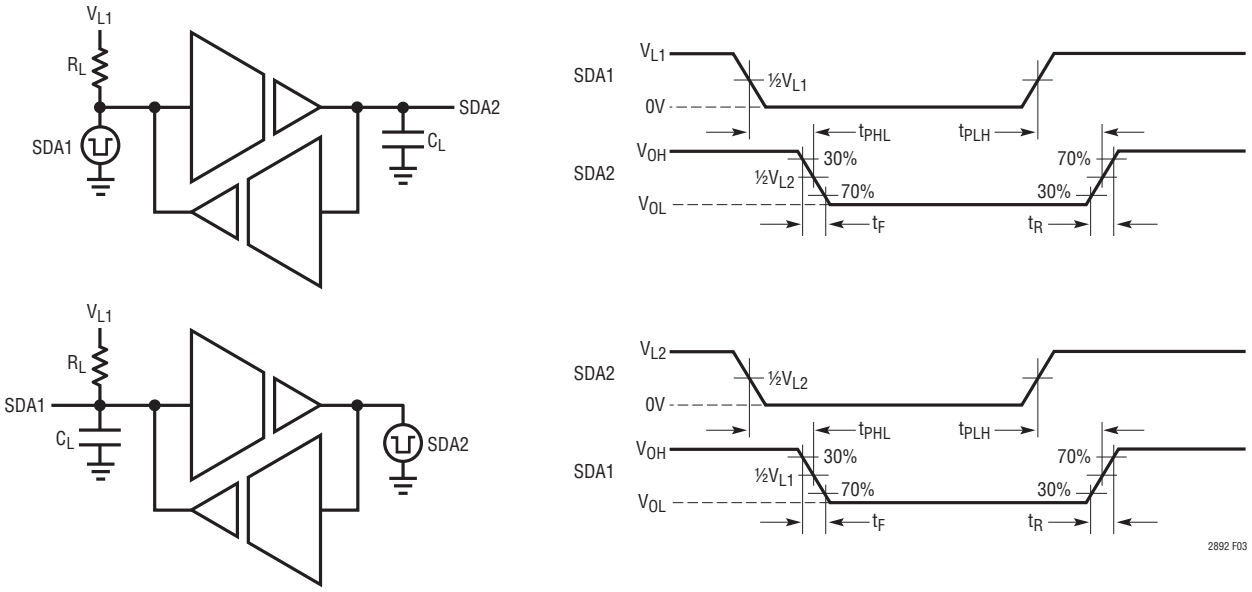


Figure 3. I²C Timing Measurements

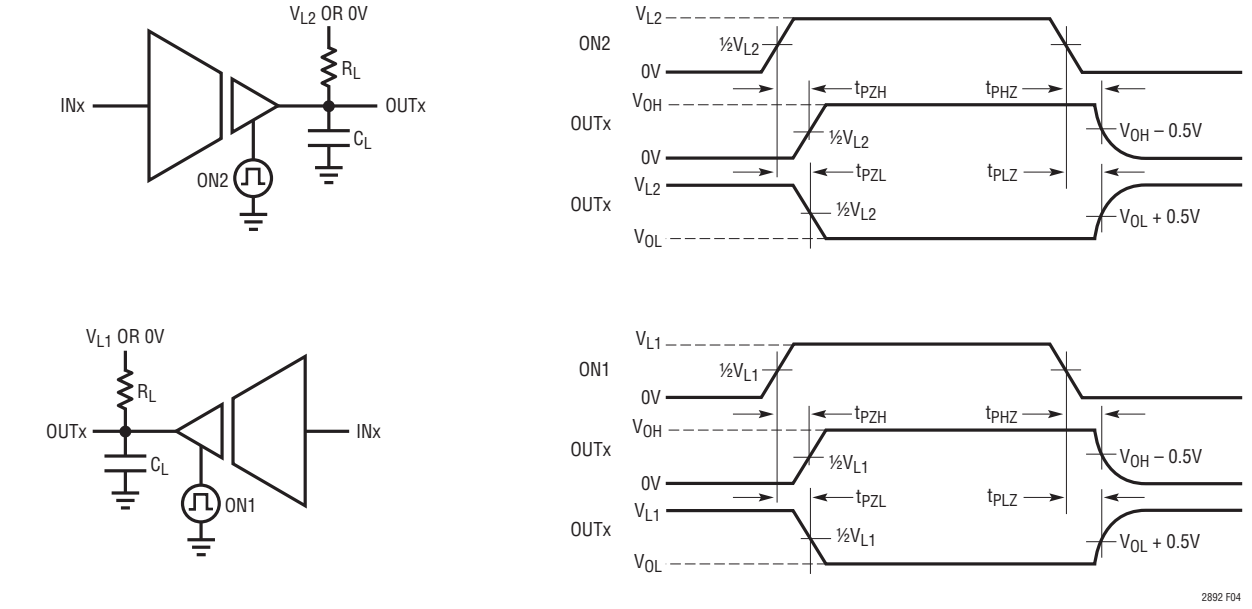


Figure 4. ONx Enable/Disable Time

APPLICATIONS INFORMATION

Overview

The LTM2892 digital µModule isolator provides a galvanically-isolated robust logic interface, complete with decoupling capacitors. The LTM2892 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2892 blocks high voltage differences and eliminates ground loops, and is extremely tolerant of common mode transients between ground planes. Error-free operation is maintained through common mode events as fast as 50kV/µs providing excellent noise isolation.

Input Supplies (V_{CC1}, V_{CC2})

The LTM2892 is powered by 3V to 5.5V supplies on each side of the isolation interface. The input supplies provide power to the internal isolated communications interface and are completely independent of the logic power supplies. V_{CC1} and V_{CC2} are each bypassed with 1.0µF ceramic capacitors.

Logic Supplies (V_{L1}, V_{L2})

Separate logic supply pins, V_{L1} and V_{L2}, allow the LTM2892 to interface with any logic signal from 1.62V to 5.5V for the SPI version and 3V to 5.5V for the I^2C version, as shown in Figure 5. Simply connect the desired logic supplies to V_{L1} and V_{L2}.

There is no interdependency between V_{CC1}, V_{CC2}, V_{L1}, and V_{L2}; they may simultaneously operate at any voltage within their specified operating ranges and sequence in any order. V_{L1} and V_{L2} are bypassed internally by 0.22µF capacitors.

Hot Plugging Safely

Caution must be exercised in applications where power is plugged into the LTM2892's power supplies, V_{CC1}, V_{CC2}, V_{L1}, or V_{L2} due to the integrated ceramic decoupling capacitors. The parasitic cable inductance along with the high Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTM2892. Refer to Application Note 88, entitled "Ceramic Input Capacitors Can Cause Overvoltage Transients" for a detailed discussion and mitigation of this phenomenon.

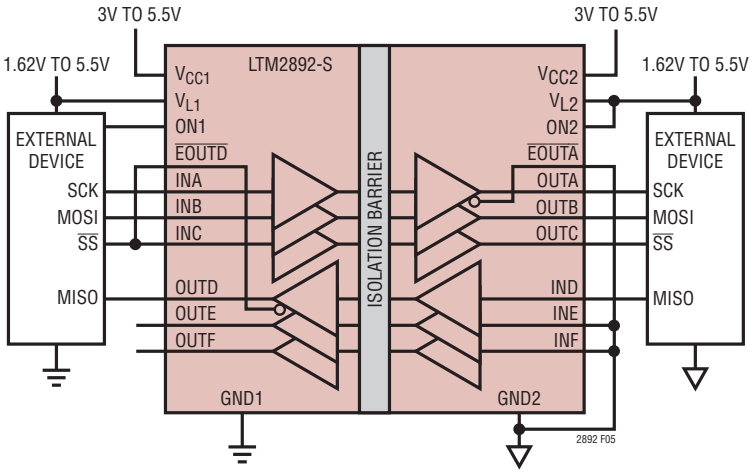


Figure 5. Supplies Are Independent

APPLICATIONS INFORMATION

Channel Timing Uncertainty

Multiple channels are supported across the isolation boundary by encoding and decoding of the inputs and outputs. Up to three signals in each direction are assembled as serial packets and transferred across the isolation barrier. The time required to transfer all three bits is 100ns maximum, and sets the limit for how often a signal can change on the opposite side of the barrier. Encoding and transmission is independent for each data direction. The technique used assigns INA(-S) or SCL(-I) on the logic side, and IND(-S) or INB(-I) on the isolated side, the highest priority such that there is no jitter on the associated output channels, only delay. This preemptive scheme will produce a certain amount of uncertainty on the other isolation channels. The resulting pulse width uncertainty on these low priority channels is typically ±6ns, but may vary up to ±44ns if the low priority channels are not encoded within the same high priority serial packet.

Serial Peripheral Interface (SPI) Bus

The LTM2892-S provides an SPI compatible isolated interface. The maximum data rate is a function of the inherent channel propagation delays, channel to channel pulse width uncertainty, and data direction requirements. Channel timing is detailed in Figures 6 through 9 and Tables 2 and 3. The SPI protocol supports four unique timing configurations defined by the clock polarity (CPOL) and clock phase (CPHA) summarized in Table 1.

Table 1. SPI Mode

CPOL	CPHA	DATA TO (CLOCK) RELATIONSHIP	
0	0	Sample (Rising)	Setup (Falling)
0	1	Setup (Rising)	Sample (Falling)
1	0	Sample (Falling)	Setup (Rising)
1	1	Setup (Falling)	Sample (Rising)

The maximum data rate for bidirectional communication is 4MHz, based on a synchronous system, as detailed in the timing waveforms. Slightly higher data rates may be achieved by skewing the clock duty cycle and minimizing the SDO to SCK setup time, however the clock rate is still dominated by the system propagation delays. A discussion of the critical timing paths relative to Figures 6 and 7 follows. For SPI communication INA = SCK, INB = SDI, INC = $\overline{CS}$, IND = SDO2, OUTA = SCK2, OUTB = SDI2, OUTC = $\overline{CS2}$, and OUTD = SDO.

- $\overline{CS}$ to SCK (master sample SDO, 1st SDO valid)
  - $t_0 \rightarrow t_1$ ≈50ns, $\overline{CS}$ to $\overline{CS2}$ propagation delay
  - $t_1 \rightarrow t_{1+}$ Isolated slave device propagation (response time), asserts SDO2
  - $t_1 \rightarrow t_3$ ≈50ns, SDO2 to SDO propagation delay
  - $t_3 \rightarrow t_5$ Setup time for master SDO to SCK
- SDI to SCK (master data write to slave)
  - $t_2 \rightarrow t_4$ ≈50ns, SDI to SDI2 propagation delay
  - $t_5 \rightarrow t_6$ ≈50ns, SCK to SCK2 propagation delay
  - $t_2 \rightarrow t_5$ ≥50ns, SDI to SCK, separate packet non-zero setup time
  - $t_4 \rightarrow t_6$ ≥50ns, SDI2 to SCK2, separate packet non-zero setup time
- SDO to SCK (master sample SDO, subsequent SDO valid)
  - t_8 Setup data transition SDI and SCK
  - $t_8 \rightarrow t_{10}$ ≈50ns, SDI to SDI2 and SCK to SCK2 propagation delay
  - t_{10} SDO2 data transition in response to SCK2
  - $t_{10} \rightarrow t_{11}$ ≈50ns, SDO2 to SDO propagation delay
  - $t_{11} \rightarrow t_{12}$ Setup time for master SDO to SCK

Maximum data rate for single direction communication, master to slave, is 8MHz, limited by the systems encoding/decoding scheme or propagation delay. Timing details for both variations of clock phase are shown in Figures 8 and 9 and Table 3.

Additional requirements to insure maximum data rate are:

- $\overline{CS}$ is transmitted prior to (asynchronous) or within the same (synchronous) data packet as SDI
- SDI and SCK setup data transition occur within the same data packet. Referencing Figure 6, SDI can precede SCK by up to 13ns ($t_7 \rightarrow t_8$) or lag SCK by 3ns ($t_8 \rightarrow t_9$) and not violate this requirement. Similarly in Figure 8, SDI can precede SCK by up to 13ns ($t_4 \rightarrow t_5$) or lag SCK by 3ns ($t_5 \rightarrow t_6$).

APPLICATIONS INFORMATION

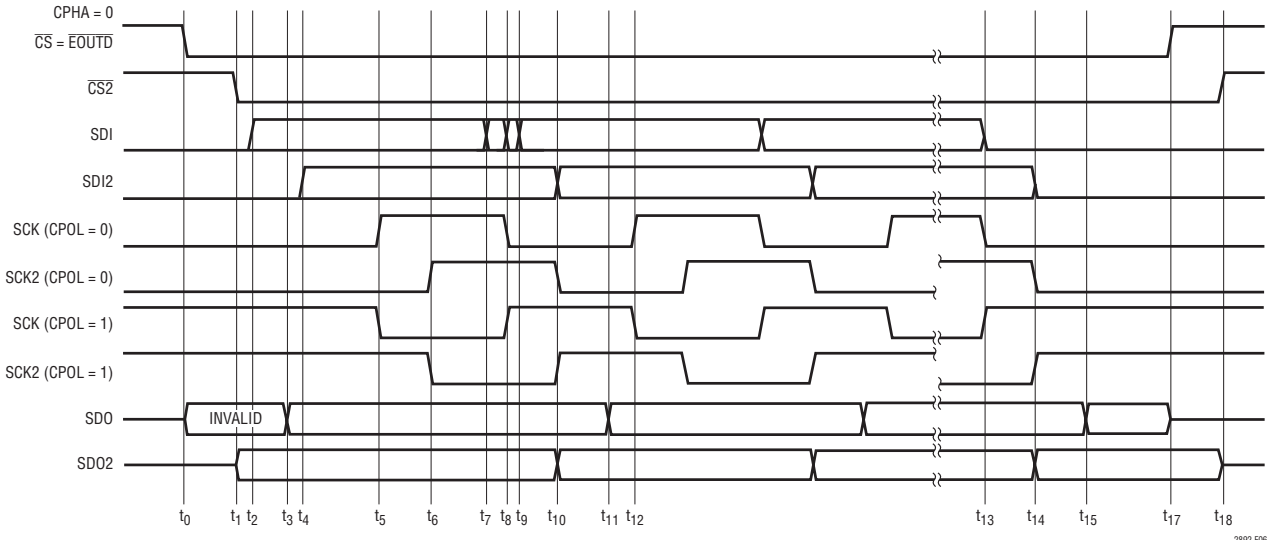


Figure 6. SPI Timing, Bidirectional, CPHA = 0

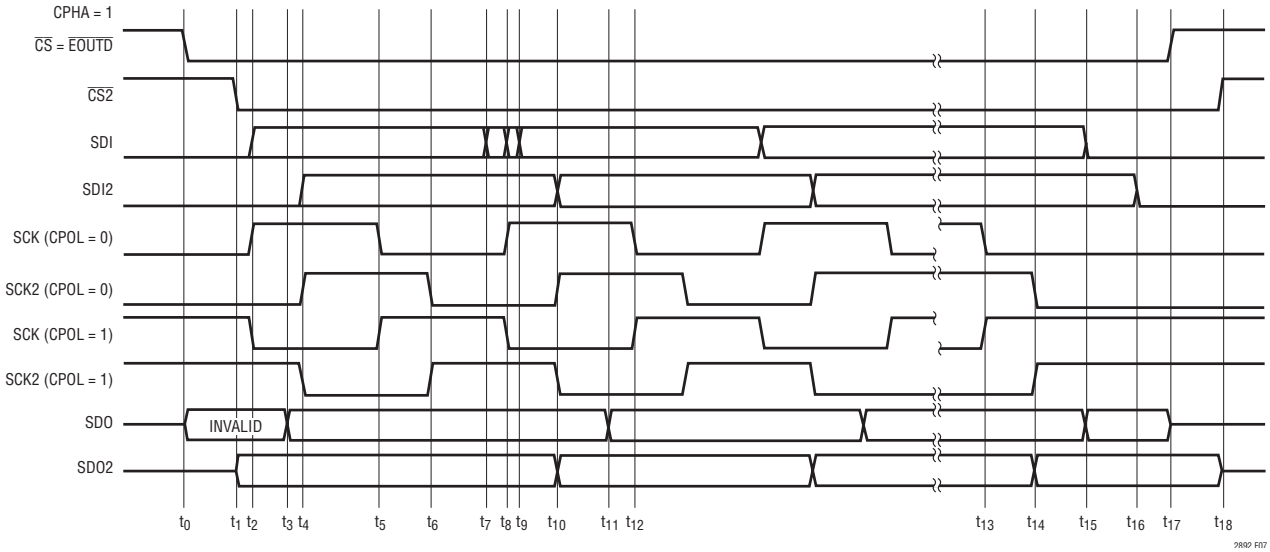


Figure 7. SPI Timing, Bidirectional, CPHA = 1

APPLICATIONS INFORMATION

Table 2. Bidirectional SPI Timing Event Description

TIME	CPHA	EVENT DESCRIPTION
t_0	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns. Logic side slave data output enabled, initial data is not equivalent to slave device data output.
t_0-t_1, t_{17}-t_{18}	0, 1	Propagation delay chip select, logic to isolated side, 50ns typical.
t_1	0, 1	Slave device chip select output data enable.
t_2	0	Start of data transmission, data setup.
	1	Start of transmission, data and clock setup. Data transition must be within –13ns to 3ns of clock edge.
t_1-t_3	0, 1	Propagation delay of slave data, isolated to logic side, 50ns typical.
t_3	0, 1	Slave data output valid, logic side.
t_2-t_4	0	Propagation delay of data, logic side to isolated side.
	1	Propagation delay of data and clock, logic side to isolated side.
t_5	0, 1	Logic side data sample time, half clock period delay from data setup transition.
t_5-t_6	0, 1	Propagation delay of clock, logic to isolated side.
t_6	0, 1	Isolated side data sample time.
t_8	0, 1	Synchronous data and clock transition, logic side.
t_7-t_8	0, 1	Data to clock delay, must be ≤ 13ns.
t_8-t_9	0, 1	Clock to data delay, must be ≤ 3ns.
t_8-t_{10}	0, 1	Propagation delay clock and data, logic to isolated side.
t_{10}, t_{14}	0, 1	Slave device data transition.
t_{10}-t_{11}, t_{14}-t_{15}	0, 1	Propagation delay slave data, isolated to logic side.
t_{11}-t_{12}	0, 1	Slave data output to sample clock setup time.
t_{13}	0	Last data and clock transition logic side.
	1	Last sample clock transition logic side.
t_{13}-t_{14}	0	Propagation delay data and clock, logic to isolated side.
	1	Propagation delay clock, logic to isolated side.
t_{15}	0	Last slave data output transition logic side.
	1	Last slave data output and data transition, logic side.
t_{15}-t_{16}	1	Propagation delay data, logic to isolated side.
t_{17}	0, 1	Asynchronous chip select transition, end of transmission. Disable slave data output logic side.
t_{18}	0, 1	Chip select transition isolated side, slave data output disabled.

APPLICATIONS INFORMATION

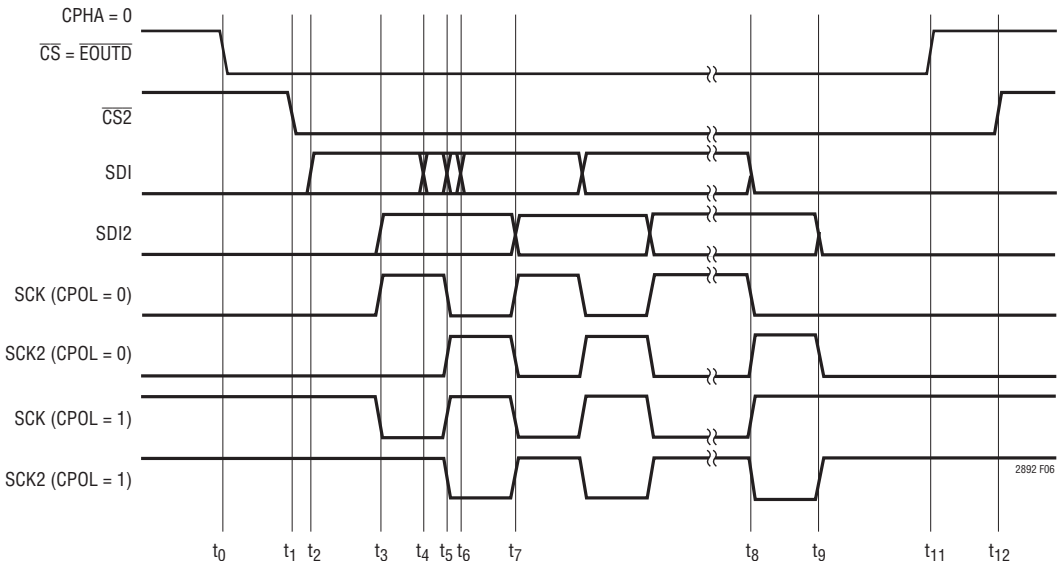


Figure 8. SPI Timing, Unidirectional, CPHA=0

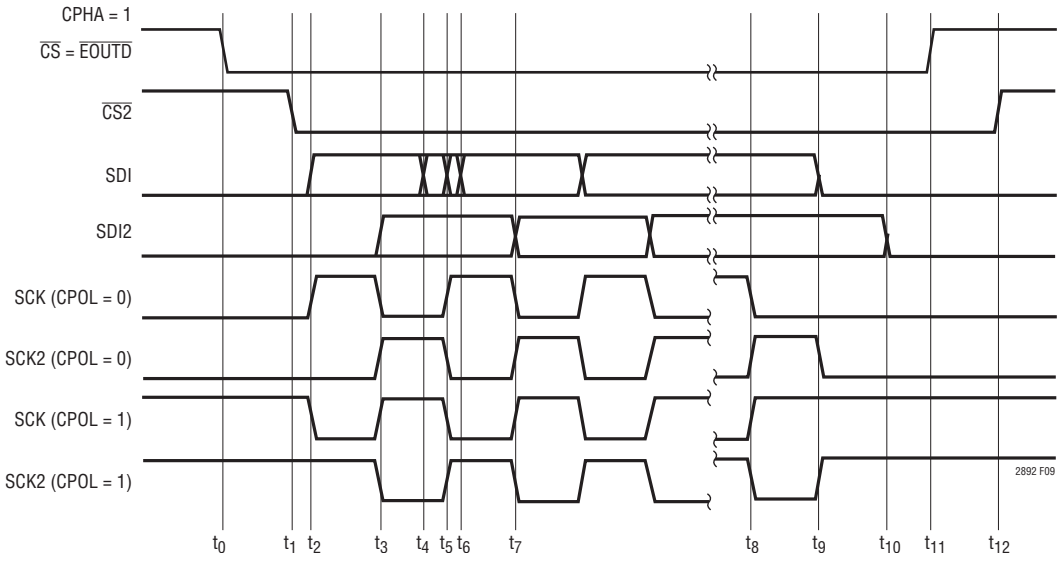


Figure 9. SPI Timing, Unidirectional, CPHA=1

APPLICATIONS INFORMATION

Table 3. Unidirectional SPI Timing Event Description

TIME	CPHA	EVENT DESCRIPTION
t_0	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns.
t_0-t_1	0, 1	Propagation delay chip select, logic to isolated side.
t_2	0	Start of data transmission, data setup.
	1	Start of transmission, data and clock setup. Data transition must be within –13ns to 3ns of clock edge.
t_2-t_3	0	Propagation delay of data, logic side to isolated side.
	1	Propagation delay of data and clock, logic side to isolated side.
t_3	0, 1	Logic side data sample time, half clock period delay from data setup transition.
t_3-t_5	0, 1	Clock propagation delay, clock and data transition.
t_4-t_5	0, 1	Data to clock delay, must be ≤ 13ns.
t_5-t_6	0, 1	Clock to data delay, must be ≤ 3ns.
t_5-t_7	0, 1	Data and clock propagation delay.
t_8	0	Last clock and data transition.
	1	Last clock transition.
t_8-t_9	0	Clock and data propagation delay.
	1	Clock propagation delay.
t_9-t_{10}	1	Data propagation delay.
t_{11}	0, 1	Asynchronous chip select transition, end of transmission.
t_{12}	0, 1	Chip select transition isolated side.

APPLICATIONS INFORMATION

Inter-IC Communication (I^2C) Bus

The LTM2892-I provides an isolated I^2C compatible interface supporting master mode only, with a unidirectional clock (SCLIN), and bidirectional data (SDA1). The maximum data rate is 400kHz which supports fast-mode I^2C. Timing is detailed in Figure 10. The data rate is limited by the slave acknowledge setup time ($t_{SU;ACK}$), consisting of the I^2C standard minimum setup time ($t_{SU;DAT}$) of 100ns, maximum clock propagation delay of 225ns, glitch filter and isolated data delay of 500ns maximum, and the combined isolated and logic data fall time of 300ns at maximum bus loading. The total setup time reduces the I^2C data hold time ($t_{HD;DAT}$) to a maximum of 175ns, guaranteeing sufficient data setup time ($t_{SU;ACK}$).

The isolated side bidirectional serial data pin, SDA2, simplified schematic is shown in Figure 11. An internal 1.8mA current source provides a pull-up for SDA2. Do not connect any other pull-up device to SDA2. This current source is sufficient to satisfy the system requirements for bus capacitances greater than 200pF in fast mode and greater than 400pF in standard mode.

Additional proprietary circuitry monitors the slew rate on the SDA1 and SDA2 signals to manage directional control across the isolation barrier. Slew rates on both pins must be greater than 1V/µs for proper operation.

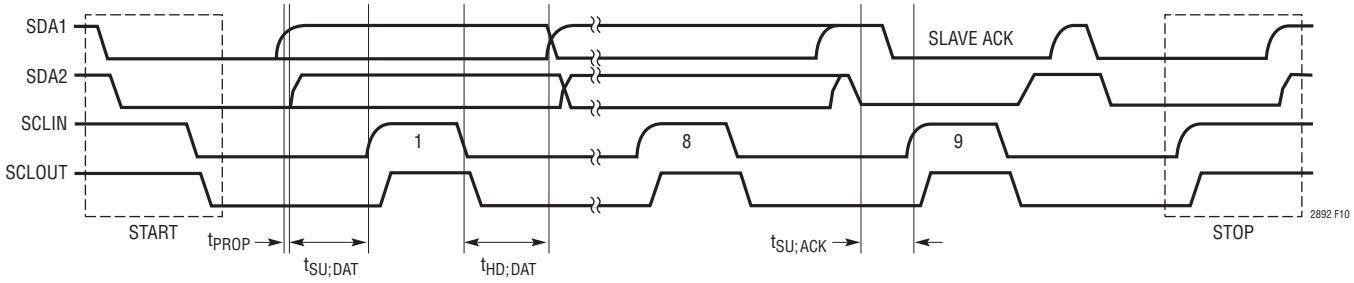


Figure 10. I^2C Timing Diagram

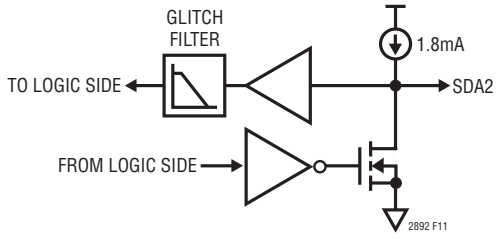


Figure 11. Isolated SDA2 Pin Schematic

APPLICATIONS INFORMATION

The logic side bidirectional serial data pin, SDA1, requires a pull-up resistor or current source connected to V_{L1}. Follow the requirements in Figures 12 and 13 for the appropriate pull-up resistor on SDA1 that satisfies the desired rise time specifications and V_{OL} maximum limits for fast and standard modes. The resistance curves represent the maximum resistance boundary; any value may be used to the left of the appropriate curve.

The isolated side clock pin, SCLOUT, has a weak push-pull output driver; do not connect an external pull-up device. SCLOUT is compatible with I^2C devices without clock stretching. On lightly loaded connections, a 100pF capacitor from SCLOUT to GND2 or RC lowpass filter (R = 500Ω, C = 100pF) can be used to decrease the rise and fall times and minimize noise.

Some consideration must be given to signal coupling between SCLOUT and SDA2. Separate these signals on a printed circuit board or route with ground between. If these signals are wired off board, twist SCLOUT with V_{L2} and/or GND2 and SDA2 with GND2 and/or V_{L2}; do not twist SCLOUT and SDA2 together. If coupling between SCLOUT and SDA2 is unavoidable, place the aforementioned RC filter at the SCLOUT pin to reduce noise injection onto SDA2.

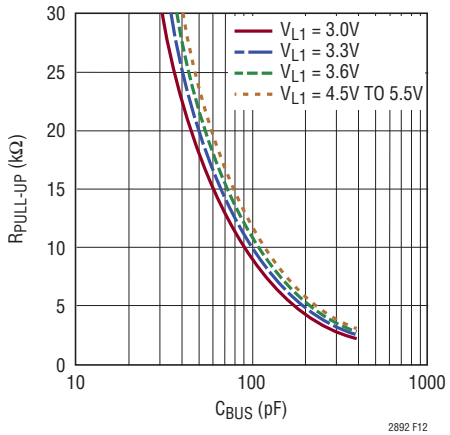


Figure 12. Maximum Standard Speed Pull-Up Resistance on SDA1

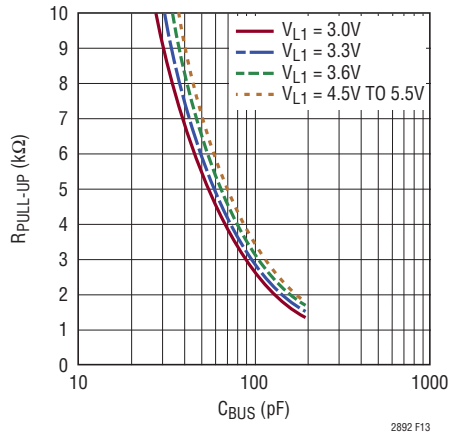


Figure 13. Maximum Fast Speed Pull-Up Resistance on SDA1

APPLICATIONS INFORMATION

Common Mode Transient Immunity (CMTI)

The minimum specified common mode transient immunity for the LTM2892 is 50kV/µs, with typical performance of 70kV/µs. This rating applies to the LTM2892 while actively transmitting data across the isolation barrier as shown in Figures 14 through 16.

The following oscilloscope screen capture characteristics apply to all figures related to the discussion of CMTI. The topmost trace input signal on INA, the trace immediately below is output signal on OUTD, data is looped on the isolated side (OUTA tied to IND), and the bottom trace is the common mode transient applied from GND2 to GND1. All data was captured using infinite persistence unless otherwise noted. The common mode transient repetition rate is 10Hz. Measurements were done using the LTM2892-S with $V_{CC1} = V_{L1} = 5V$, and $V_{CC2} = V_{L2}$ at approximately 4.7V under battery power. Figures 16 and 18 show the actual transient rate of change using data averaging.

This exceptional level of transient immunity is a direct result of the differential receiver and center tapped data coils employed in the isolated data communication system. Figure 17 shows the LTM2892 in a static data state in the presence of 200kV/µs transients with no state change or system latch-up. The system is known to be in a static state since the data changed approximately 600ns prior to the transient; the internal data refresh which guarantees the correct DC state does not occur until 1.2µs after the last transition.

Figure 18 shows 200kV/µs transients occurring in a data communication interval, just prior to data transmission across the isolation barrier.

For transients greater than 70kV/µs it is possible to corrupt the dynamic data communication. In this case the output data may be incorrect for up to one data refresh period. This situation is shown in Figure 19. The output state is automatically corrected after approximately 1.2µs.

The output data states may also be corrupted for transients greater than 70kV/µs, if the common mode transient aligns with the refresh data transmission. Figures 20 and 21 show data corruption for one refresh period with common mode transients of 200kV/µs.

RF, Magnetic Field Immunity

The isolator µModule technology used within the LTM2892 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, radio-frequency, electromagnetic field immunity

EN 61000-4-8 Power frequency magnetic field immunity

EN 61000-4-9 Pulsed magnetic field immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 4.

Table 4. EMC Immunity Tests

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3 Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8 Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8 Level 5	60Hz	100A/m*
EN 61000-4-9 Level 5	Pulse	1000A/m

* Non IEC method.

APPLICATIONS INFORMATION

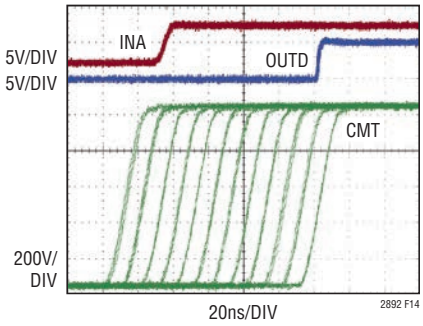


Figure 14. Operation with Repetitive Bursts of Common Mode Transients, 50kV/µs

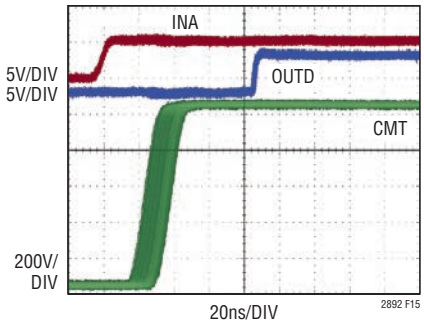


Figure 15. 70kV/µs Transient Operation Coincident with Data Transmission/Reception

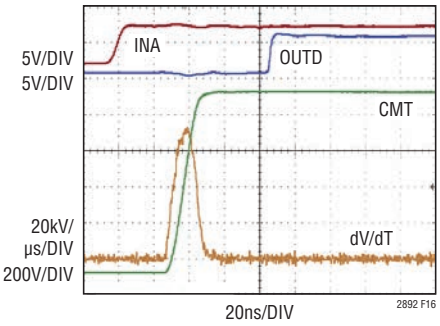


Figure 16. Transient dV/dT, 70kV/µs

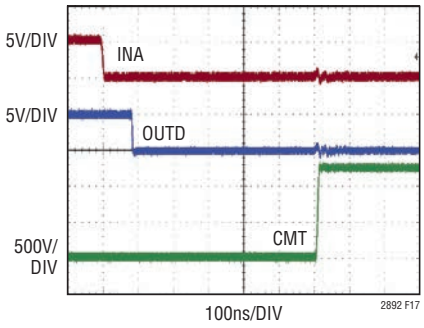


Figure 17. Static Operation with 200kV/µs Transients

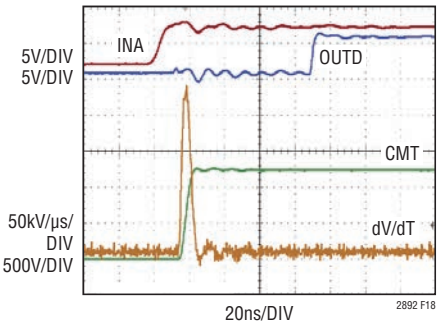


Figure 18. 200kV/µs Transient Prior to Data Transmission

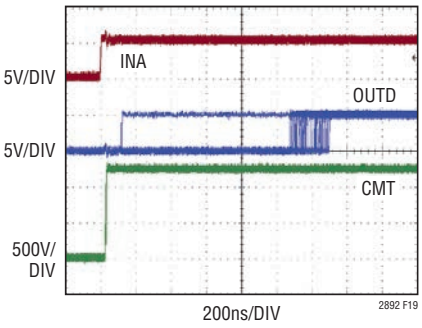


Figure 19. Data Refresh Recovery for 200kV/µs Transient

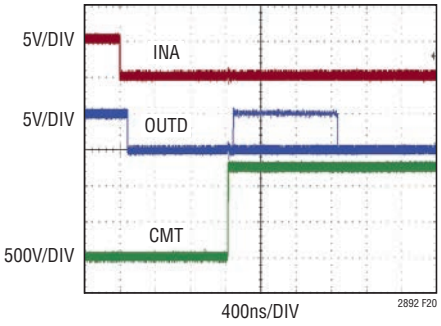


Figure 20. Common Mode Transient (200kV/µs) Coincident with Data Refresh, Data Low

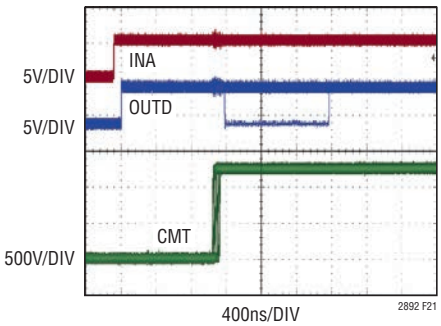


Figure 21. Common Mode Transient (200kV/µs) Coincident with Data Refresh, Data High

APPLICATIONS INFORMATION

PCB Layout

The high integration of the LTM2892 makes PCB layout very simple. However, to optimize its electrical isolation characteristics and EMI performance, some layout considerations are necessary.

- Input and output supply decoupling is not required, since these components are integrated within the package. An additional polarized bulk capacitor with a value of 3.3µF to 10µF is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1µF to 4.7µF, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND1 and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, and minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes, where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND1 and GND2. If ground planes are used it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.
- For large ground planes a small capacitance (≤ 330pF) from GND1 to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be 4 layers. Care must be exercised in applying either technique to ensure the voltage rating of the barrier is not compromised.
- In applications without an embedded PCB substrate capacitance, a slot may be added between the logic side and isolated side device pins. The slot extends the creepage path between terminals on the PCB side, and may reduce leakage caused by PCB contamination. The slot should be placed in the middle of the device and extend beyond the package perimeter.

The PCB layout in Figures 22a and 22b shows the demo boards for the LTM2892.

EMI performance is shown in Figure 23, measured using a gigahertz transverse electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, “Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides.”