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## FEATURES

- Three Independent 10A DC Output Current Regulator Channels
- Input Voltage Range: 4.7V to 16V
  - 2.375V to 16V with External 5V Bias
- $V_{OUT1,2}$  Voltage Range: 0.8V to 1.8V
- $V_{OUT3}$  Voltage Range: 0.8V to 5.5V
- $\pm 1.5\%$  Maximum Total DC Output Error
- Current Mode Control/Fast Transient Response
- Frequency Synchronization
- Output Overvoltage and Overcurrent Protection
- Multiphase Operation with Current Sharing on  $V_{OUT1}$  and  $V_{OUT2}$
- General Purpose Temperature Monitors
- Soft-Start/Voltage Tracking
- Power Good Monitors
- 15mm  $\times$  15mm  $\times$  5.01mm BGA Package

## APPLICATIONS

- Telecom, Networking and Industrial Equipment
- High Density Point of Load Regulation

## DESCRIPTION

The LTM<sup>®</sup>4633  $\mu$ Module<sup>®</sup> (micromodule) regulator combines three complete 10A switching mode DC/DC converters into one small package. Included in the package are the switching controllers, power FETs, inductors, and most support components. The LTM4633's three regulators operate from 4.7V to 16V input rail(s) or 2.375V to 16V with an external 5V bias. The  $V_{OUT1}$  and  $V_{OUT2}$  output range is 0.8V to 1.8V, while the  $V_{OUT3}$  output range is 0.8V to 5.5V. Each output is set by one external resistor.

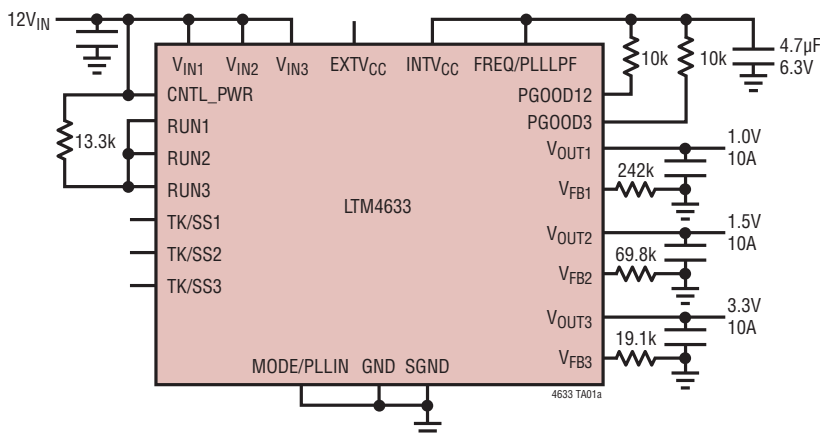
High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The device supports frequency synchronization, multiphase parallel operation of  $V_{OUT1}$  and  $V_{OUT2}$ , soft-start and output voltage tracking for supply rail sequencing.

Fault protection features include overvoltage protection, overcurrent protection and temperature monitoring. The power module is offered in a space saving, thermally enhanced 15mm  $\times$  15mm  $\times$  5.01mm BGA package. The LTM4633 is RoHS compliant with Pb-free finish.

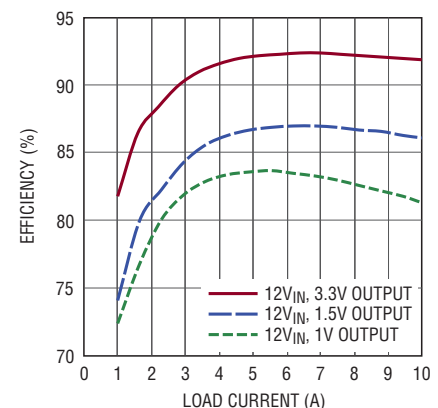
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## TYPICAL APPLICATION

12V Input to 1.0V, 1.5V and 3.3V Output Regulator



Efficiency vs Load Current





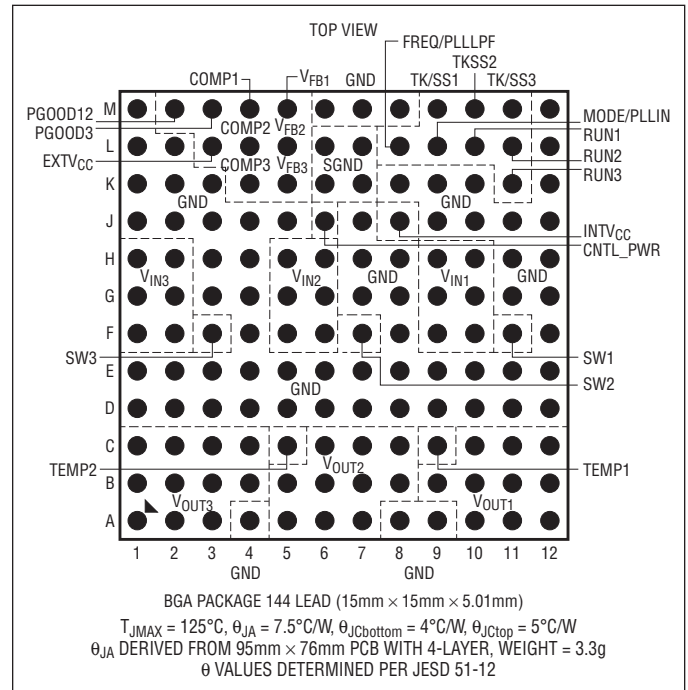
# LTM4633

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

CNTL_PWR .....	-0.3V to 18V
$V_{IN1}$ , $V_{IN2}$ , $V_{IN3}$ .....	-0.3V to 18V
$V_{OUT1}$ , $V_{OUT2}$ .....	-0.3V to 2.2V
$V_{OUT3}$ .....	-0.3V to 5.5V
Switch Voltage (SW1, SW2 and SW3) .....	-1V to 18V
MODE/PLLIN, TK/SS1, TK/SS2, TK/SS3, FREQ/PLLLPF, $V_{FB1}$ , $V_{FB2}$ , $V_{FB3}$ .....	-0.3V to INTV <sub>CC</sub>
COMP1, COMP2, COMP3 (Note 6) .....	-0.3V to INTV <sub>CC</sub>
RUN1, RUN2, RUN3, INTV <sub>CC</sub> , EXTV <sub>CC</sub> , PGOOD12, PGOOD3 .....	-0.3V to 6V
TEMP1, TEMP2 .....	-0.3V to 0.8V
INTV <sub>CC</sub> Peak Output Current .....	75mA
Operating Junction Temperature Range (Note 2) .....	-55°C to 125°C
Storage Temperature Range .....	-55°C to 125°C
Peak Solder Reflow Body Temperature .....	245°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE (NOTE 2)
LTM4633EY#PBF	LTM4633EY#PBF	LTM4633Y	144-Lead (15mm × 15mm × 5.01mm) BGA	-40°C to 125°C
LTM4633IY#PBF	LTM4633IY#PBF	LTM4633Y	144-Lead (15mm × 15mm × 5.01mm) BGA	-40°C to 125°C
LTM4633MPY#PBF	LTM4633MPY#PBF	LTM4633Y	144-Lead (15mm × 15mm × 5.01mm) BGA	-55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

This product is only offered in trays. For more information go to: <http://www.linear.com/packaging/>

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ , per the typical application for each regulator channel.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{IN}$	Input DC Voltage	CNTL_PWR Powered from Separate Supply (5V to 16V Range)	●	2.375	16	V	
		CNTL_PWR Powered Tied to $V_{IN}$ Supply	●	4.7	16	V	
$V_{OUT(\text{RANGE})}$	Output Voltage Range $V_{OUT1}$ , $V_{OUT2}$ Output Voltage Range $V_{OUT3}$		●	0.8	1.8	V	
			●	0.8	5.5	V	
$V_{OUT(\text{DC})}$	Output Voltage, Total Variation with Line and Load, $V_{OUT1}$ , $V_{OUT2}$ , $V_{OUT3}$	$C_{IN} = 22\mu\text{F} \times 3$ , $C_{OUT} = 100\mu\text{F}$ Ceramic $\times 3$ , $R_{FB} = 69\text{k}$ , MODE/PLLIN = 0V, $V_{IN} = 4.7\text{V}$ to 16V, $I_{OUT} = 0\text{A}$ to 10A (Note 4)	●	1.477	1.50	1.523	V

#### Input Specifications

$V_{RUN}$	RUN1, RUN 2, RUN 3 Pin ON Threshold	$V_{RUN}$ Rising		1.15	1.3	1.4	V
$V_{RUN(\text{HYS})}$	RUN Pin Hysteresis			175			mV
$I_{Q(VIN)}$	Input Supply Bias Current Each Channel	$V_{OUT} = 1.5\text{V}$ , Burst Mode Operation $V_{OUT} = 1.5\text{V}$ , Pulse-Skipping Mode $V_{OUT} = 1.5\text{V}$ , Switching Continuous Shutdown, RUN = 0V			0.5		mA
					1		mA
					45		mA
					50		$\mu\text{A}$
$I_{S(VIN)}$	Input Supply Current Each Channel	$V_{OUT} = 1.5\text{V}$ , $I_{OUT} = 10\text{A}$		1.5			A

#### Output Specifications

$I_{OUT(\text{DC})}$	Output Continuous Current Range Each Channel	$V_{OUT} = 1.5\text{V}$ (Note 4)		0	10		A
$\frac{\Delta V_{OUT(\text{LINE})}}{V_{OUT}}$	Line Regulation Accuracy per Channel	$V_{OUT} = 1.5\text{V}$ , $V_{IN}$ from 2.375V to 16V $I_{OUT} = 0\text{A}$ , CNTL_PWR = 12V	●		0.015	0.02	%/V
$\frac{\Delta V_{OUT(\text{LOAD})}}{V_{OUT}}$	Load Regulation Accuracy per Channel	$V_{OUT} = 1.5\text{V}$ , $I_{OUT} = 0\text{A}$ to 10A (Note 4)	●		0.3	0.5	%
$V_{OUT(\text{AC})}$	Output Ripple Voltage per Channel	$I_{OUT} = 0\text{A}$ , $C_{OUT} = 100\mu\text{F}$ Ceramic $\times 3$ , $V_{OUT} = 1.5\text{V}$			15		mV
$\Delta V_{OUT(\text{START})}$	Turn-On Overshoot per Channel	$C_{OUT} = 100\mu\text{F}$ Ceramic $\times 3$ , $V_{OUT} = 1.5\text{V}$ , $I_{OUT} = 0\text{A}$			20		mV
$t_{\text{START}}$	Turn-On Time per Channel	$C_{OUT} = 100\mu\text{F}$ Ceramic $\times 3$ , No Load, TK/SS = 0.01 $\mu\text{F}$			6		ms
$V_{OUT(\text{LS})}$	Peak Deviation for Dynamic Load per Channel	Load: 0% to 50% to 0% of Full Load, $C_{OUT} = 100\mu\text{F}$ Ceramic $\times 3$ , $V_{OUT} = 1.5\text{V}$ Typical Bench Data			100		mV
$t_{\text{SETTLE}}$	Settling Time for Dynamic Load Step per Channel	Load: 0% to 50% to 0% of Full Load, $C_{OUT} = 100\mu\text{F}$ Ceramic $\times 3$ , $V_{OUT} = 1.5\text{V}$ Typical Bench Data			40		$\mu\text{s}$
$I_{OUT(\text{PK})}$	Output Current Limit per Channel	$V_{OUT} = 1.5\text{V}$			13		A

#### Control Specifications

$V_{FB}$	Voltage at $V_{FB}$ Pin per Channel	$I_{OUT} = 0\text{A}$ , $V_{OUT} = 1.5\text{V}$ $I_{OUT} = 0\text{A}$ , $V_{OUT} = 1.5\text{V}$	●	0.792	0.80	0.808	V
				0.794	0.80	0.806	V
$I_{FB}$	Current at $V_{FB}$ Pin per Channel	(Note 3)			-10	-50	nA
$V_{OVL}$	Feedback Overvoltage Lockout per Channel		●	0.84	0.86	0.88	V
$I_{TK/SS}$	Track Pin Soft-Start Pull-Up Current per Channel	TK/SS = 0V		1.1	1.5	1.9	$\mu\text{A}$
$t_{ON(\text{MIN})}$	Minimum On-Time	(Note 3)			90		ns
Max DC	Maximum Duty Cycle	2.375V to 2V at 10A, 5.5V to 5V at 0A (Note 6)			100		%

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ , per the typical application for each regulator channel.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$R_{FBHI}$	Resistor Between $V_{OUT}$ and $V_{FB}$ Pins		60	60.4	60.8	$k\Omega$
$V_{PGOOD}$	PGOOD Trip Level PGOOD12 PGOOD3	$V_{FB}$ With Respect to Set Output $V_{FB}$ Ramping Negative $V_{FB}$ Ramping Positive		-7.5 7.5		% %
$V_{PGL}$	PGOOD Voltage Low	$I_{PGOOD} = 2\text{mA}$		0.1	0.3	V

### INTV<sub>CC</sub> Linear Regulator

$V_{INTVCC}$	Internal $V_{CC}$ Voltage	Float MODE/PLLIN	$6\text{V} < V_{IN} < 16\text{V}$	4.8	5	5.2	V
$V_{INTVCC}$ Load Reg	INTV <sub>CC</sub> Load Regulation		$I_{CC} = 0\text{mA}$ to $50\text{mA}$		0.5		%
$V_{EXTVCC}$	EXTV <sub>CC</sub> Switchover Voltage		EXTV <sub>CC</sub> Ramping Positive ●	4.5	4.7		V
$V_{LDO EXT}$	EXTV <sub>CC</sub> Voltage Drop		$I_{CC} = 20\text{mA}$ , $V_{EXTVCC} = 5\text{V}$		30	75	mV
$V_{LDOHYS}$	EXTV <sub>CC</sub> Hysteresis				200		mV

### Oscillator and Phase-Locked Loop

$f_{SYNC}$	SYNC Capture Range	Clock Input Duty Cycle = 50%		600		750	kHz
$f_S$	Switching Frequency	$V_{FREQ/PLLPF} = INTV_{CC}$		700	750	800	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				250		$k\Omega$
$V_{IH(MODE/PLLIN)}$	Clock Input Level High			2.0			V
$V_{IL(MODE/PLLIN)}$	Clock Input Level Low					0.8	V
Clock Phase	$V_{OUT2}$ to $V_{OUT1}$ Phase $V_{OUT3}$ to $V_{OUT2}$ Phase $V_{OUT1}$ to $V_{OUT3}$ Phase	$V_{FREQ/PLLPF} = 1.2\text{V}$ (Note 3)			120		Deg Deg Deg
$V_{TEMP1,2}$	Temperature Diode Forward Voltage	$I_{TEMP} = 100\mu\text{A}$ at $25^\circ\text{C}$			0.598		V
TC $V_{TEMP}$	Temperature Coefficient				-2.0		$\text{mV}/^\circ\text{C}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM4633 is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTM4633E is guaranteed to meet performance specifications over the  $0^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4633I is guaranteed to meet specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. The LTM4633MP is guaranteed and tested to meet specifications over the  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

**Note 3:** 100% tested at wafer level.

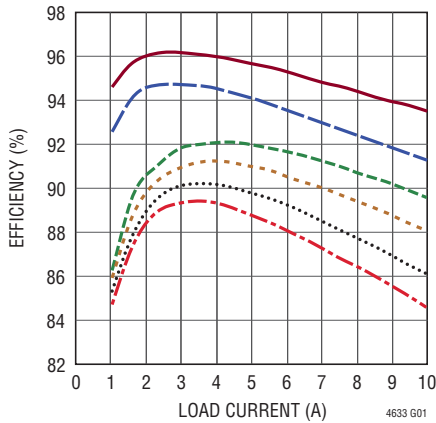
**Note 4:** See output current derating curves for different  $V_{IN}$ ,  $V_{OUT}$  and  $T_A$ .

**Note 5:** Guaranteed by design.

**Note 6:** High duty designs need to be validated based on maximum temperature rise and derating in ambient conditions.

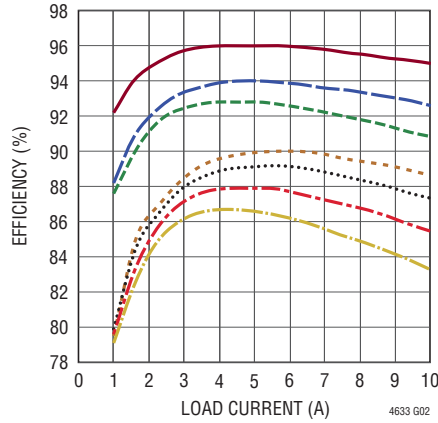
# TYPICAL PERFORMANCE CHARACTERISTICS

**5V Input Efficiency**



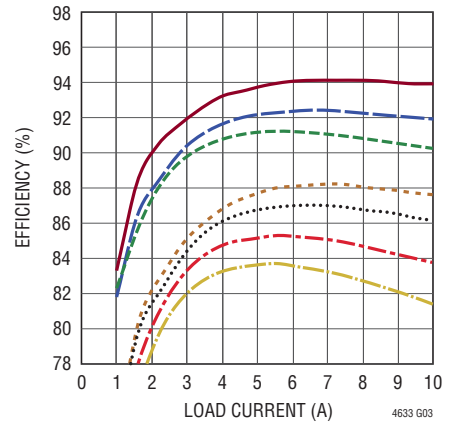
4633 G01  
 — 5V<sub>IN</sub> TO 3.3V (700kHz) — 5V<sub>IN</sub> TO 1.5V (700kHz)  
 — 5V<sub>IN</sub> TO 2.5V (700kHz) — 5V<sub>IN</sub> TO 1.2V (700kHz)  
 — 5V<sub>IN</sub> TO 1.8V (700kHz) — 5V<sub>IN</sub> TO 1V (700kHz)

**8V Input Efficiency**



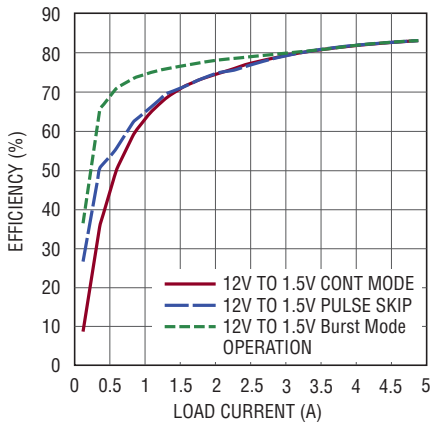
4633 G02  
 — 8V<sub>IN</sub> TO 5V (700kHz) — 8V<sub>IN</sub> TO 1.5V (700kHz)  
 — 8V<sub>IN</sub> TO 3.3V (700kHz) — 8V<sub>IN</sub> TO 1.2V (700kHz)  
 — 8V<sub>IN</sub> TO 2.5V (700kHz) — 8V<sub>IN</sub> TO 1V (700kHz)  
 — 8V<sub>IN</sub> TO 1.8V (700kHz)

**12V Input Efficiency**



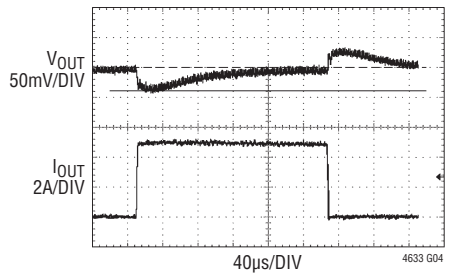
4633 G03  
 — 12V<sub>IN</sub> TO 5V (700kHz) — 12V<sub>IN</sub> TO 1.5V (700kHz)  
 — 12V<sub>IN</sub> TO 3.3V (700kHz) — 12V<sub>IN</sub> TO 1.2V (700kHz)  
 — 12V<sub>IN</sub> TO 2.5V (700kHz) — 12V<sub>IN</sub> TO 1V (700kHz)  
 — 12V<sub>IN</sub> TO 1.8V (700kHz)

**Light Load Efficiency**



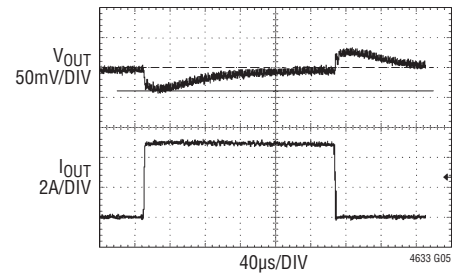
4633 G17

**12V to 1V Load Step Response**



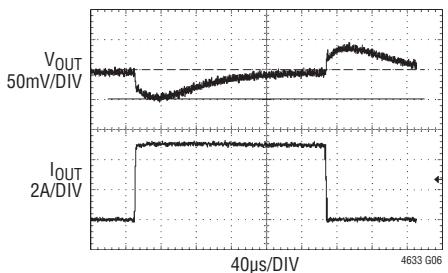
4633 G04  
 $C_{FF} = 220\text{pF}$  0A TO 5A LOAD STEP AT 5A/ $\mu\text{s}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}, 1 \times 470\mu\text{F POSCAP}$

**12V to 1.2V Load Step Response**



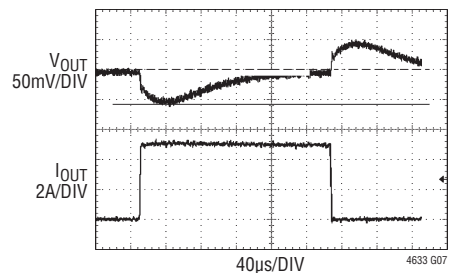
4633 G05  
 $C_{FF} = 220\text{pF}$  0A TO 5A LOAD STEP AT 5A/ $\mu\text{s}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}, 1 \times 470\mu\text{F POSCAP}$

**12V to 1.5V Load Step Response**



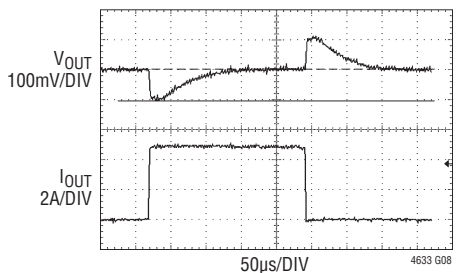
4633 G06  
 $C_{FF} = 220\text{pF}$  0A TO 5A LOAD STEP AT 5A/ $\mu\text{s}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}, 1 \times 470\mu\text{F POSCAP}$

**12V to 1.8V Load Step Response**



4633 G07  
 $C_{FF} = 220\text{pF}$  0A TO 5A LOAD STEP AT 5A/ $\mu\text{s}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}, 1 \times 470\mu\text{F POSCAP}$

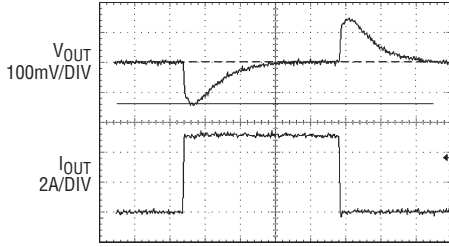
**12V to 2.5V Load Step Response**



4633 G08  
 $C_{FF} = 100\text{pF}$  0A TO 5A LOAD STEP AT 5A/ $\mu\text{s}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}$

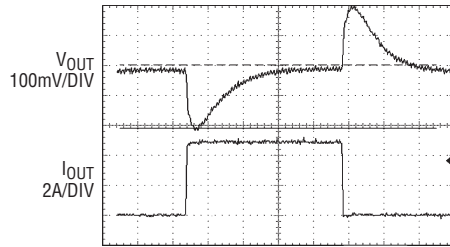
## TYPICAL PERFORMANCE CHARACTERISTICS

### 12V to 3.3V Load Step Response



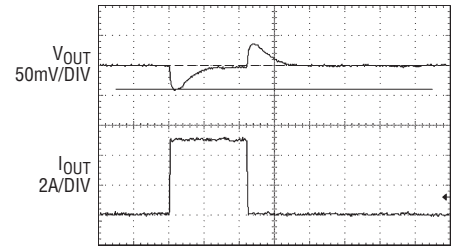
$C_{FF} = 100\text{pF}$ , 0A TO 5A LOAD STEP AT  $5\text{A}/\mu\text{s}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}$

### 12V to 5V Load Step Response



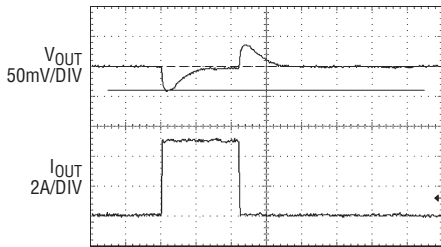
$C_{FF} = 100\text{pF}$ , 0A TO 5A LOAD STEP AT  $5\text{A}/\mu\text{s}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}$

### 3.3V to 1V Load Step Response



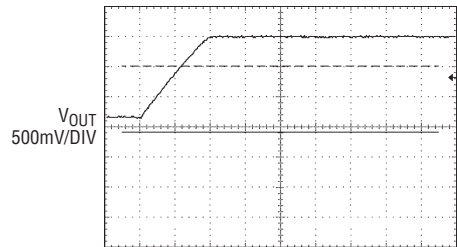
$C_{FF} = \text{NONE}$ , 0A TO 5A LOAD STEP AT  $5\text{A}/\mu\text{s}$   
 $C_{OUT} = 4 \times 100\mu\text{F CERAMIC}$ ,  $1 \times 470\mu\text{F POSCAP}$

### 3.3V to 1.8V Load Step Response



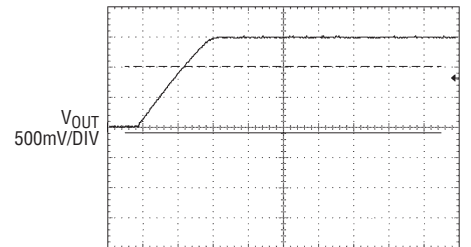
$C_{FF} = \text{NONE}$ , 0A TO 5A LOAD STEP AT  $5\text{A}/\mu\text{s}$   
 $C_{OUT} = 4 \times 100\mu\text{F CERAMIC}$ ,  $1 \times 470\mu\text{F POSCAP}$

### 12V to 1.5V No-Load Start-Up



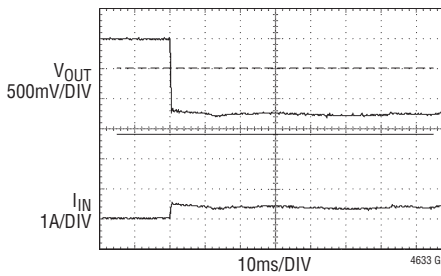
TK/SS CAPACITOR =  $0.1\mu\text{F}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}$ ,  $1 \times 470\mu\text{F POSCAP}$

### 12V to 1.5V Full-Load Start-Up

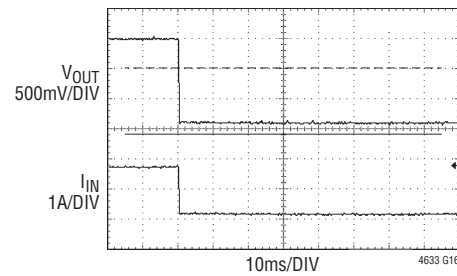


TK/SS CAPACITOR =  $0.1\mu\text{F}$   
 $C_{OUT} = 2 \times 100\mu\text{F CERAMIC}$ ,  $1 \times 470\mu\text{F POSCAP}$

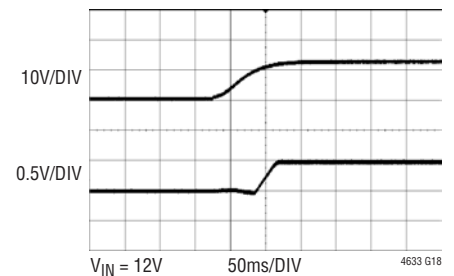
### 12V to 1.5V No-Load Short Circuit



### 12V to 1.5V, 10A Load Short Circuit



### Start Into Pre-Bias Output



$V_{IN} = 12\text{V}$   
 $V_{OUT} = 1\text{V}$   
 PRE-BIASED AT  $500\text{mV}$

## PIN FUNCTIONS



PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

**GND (A4, A8-A9, D1- D12, E1-E12, F4, F8, F12, G3-G4, G7-G8, G11-G12, H3-H4, H7-H8, H11-H12, J1-J5, J7, J9-J12, K1-K3, K8-K10, K12,L1-L2,L12, M1, M6-M8, M12):** Ground Pins for Both Input and Output Returns. All ground pins need to connect with large copper areas underneath the unit.

**V<sub>OUT1</sub>, V<sub>OUT2</sub>, V<sub>OUT3</sub> (A10-A12, B9-B12, and C10-C12); (A5-A7, B5-B8, C6-C8); (A1-A3, B1-B4, C1-C4):** Power Output Pins. Apply output load between these pins and the GND pins. Recommend placing output decoupling capacitance directly between these pins and the GND pins. See Table 5.

**TEMP1 AND TEMP2 (C9, C5):** Two Onboard Temperature Diodes for Monitoring the VBE Junction Voltage Change with Temperature. Each of these two temperature diode connected PNP transistors is placed in the middle of channel 1 and channel 2, and in the middle of channel 2 and channel 3. See the Applications Information section and an example in Figure 19.

**V<sub>IN1</sub>, V<sub>IN2</sub>, V<sub>IN3</sub> (F9-F10, G9-G10, H9-H10); (F5-F6, G5-G6, H5-H6); (F1-F2, G1-G2, H1-H2):** Power Input Pins. Apply input voltage between these pins and the GND pins. Recommend placing input decoupling capacitance directly between the V<sub>IN</sub> pins and the GND pins. The V<sub>IN</sub> paths can be all combined from one power source, or powered from independent power sources. The V<sub>IN</sub> paths can operate down to 2.375V when the CNTL\_PWR is biased separately from a supply in the range of 4.7V to 16V. See the Applications Information section.

**SW1 (F11), SW2 (F7), SW3 (F3):** The internal switch node for each of the regulator channels for monitoring the switching waveform. An R-C snubber circuit can be placed on these pins to ground to eliminate switch node ringing noise.

**CNTL\_PWR (J6):** Input Supply to an Internal Bias LDO to Power the Internal Controller and MOSFET Drivers. This pin is connected to an input supply voltage range of 4.7V to 16V. If the voltage at CNTL\_PWR is  $\leq 5.5V$ , the INTV<sub>CC</sub> pin should be tied to CNTL\_PWR for optimum efficiency. If the voltage at CNTL\_PWR is  $> 5.5V$ , leave INTV<sub>CC</sub> floating with the recommended decoupling capacitor. When using multiple input supplies, choose the lowest input supply between 4.7V to 16V to supply the CNTL\_PWR pin. This will lower the internal power loss and improve efficiency.

**INTV<sub>CC</sub> (J8):** Output of the Internal Bias LDO for Powering Internal Control Circuitry. Connect a 4.7 $\mu$ F ceramic capacitor to ground for decoupling. If the voltage at CNTL\_PWR is  $\leq 5.5V$ , tie the INTV<sub>CC</sub> pin to CNTL\_PWR for optimum efficiency. If the voltage at CNTL\_PWR is  $> 5.5V$ , leave INTV<sub>CC</sub> floating. See the Applications Information section.

**SGND (K6-K7, L6-L7):** Signal Ground Connections. The signal ground connection in the module is separated from normal power ground (GND) by an internal 2.2 $\Omega$  resistor. This allows the designer to connect the signal ground pin close to GND near the external output capacitors on the regulator channel's outputs. The entire internal small-signal feedback circuitry is referenced to SGND, thus allowing for better output regulation. See the recommended layout in the Applications Information section.

**EXTV<sub>CC</sub> (L3):** External Bias Power Input. The internal bias LDO is bypassed whenever the voltage at EXTV<sub>CC</sub> is above 4.7V. Never exceed 6V at this pin and ensure CNTL\_PWR  $>$  EXTV<sub>CC</sub> at all times to avoid reverse polarity on the internal bias LDO. Connect a 1 $\mu$ F capacitor to ground when used otherwise leave floating. When generating a 5V output on channel 3, connect the 5V output to this pin to improve efficiency.



## PIN FUNCTIONS

**FREQ/PLLLPF (L8):** Frequency Set and PLL Lowpass Filter Pin. This pin is driven with a DC voltage to set the operating frequency. Generally the pin is just connected to  $INTV_{CC}$  to set the typical 750kHz operating frequency. Applying a DC voltage of 1.4V to this pin will set the frequency to 600kHz and 1.6V will set it to 700kHz. When an external clock is used, then the FREQ/PLLLPF pin must not be connected to any DC voltage. The pin must be floating and will have the proper internal compensation for the internal loop filter. For  $V_{OUT1,2,3} \leq 1.5V$  use 600kHz, and for  $V_{OUT1,2,3} \geq 1.5V$  use  $\geq 700kHz$ . These frequency settings optimize efficiency and eliminate minimum on-time issues for less than 1V output. See the Applications Information section.

**MODE/PLLIN (L9):** Force Continuous Mode, Burst Mode, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force all channels into the continuous mode of operation. Connect to  $INTV_{CC}$  to enable pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock on the pin will force the controller into continuous mode of operation and synchronize the internal oscillator.

**RUN1, RUN2, RUN3 (L10, L11, K11):** Run Control Inputs. A voltage above 1.3V on any RUN pin turns on that particular channel. However, forcing any of these RUN pins below 1.2V causes that channel to shut down. Each of the RUN pins has an internal 10k resistor to ground. This resistor can be used with an external pull-up resistor to the input voltage to set a UVLO for that channel, or simply to turn on the channel. The RUN pins have a maximum voltage of 6V. See the Applications Information section.

**PGOOD12, PGOOD3 (M2, M3):** Output voltage power good indicator for  $V_{OUT1}$  and  $V_{OUT2}$  are combined, and  $V_{OUT3}$  separate. The open-drain logic output is pulled to ground when the output voltage is not within  $\pm 7.5\%$  of the regulation point.

**COMP1, COMP2, COMP3 (M4, L4, K4):** Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The LTM4633 regulator channels are all internally compensated for proper stability. COMP1 and COMP2 can be tied together for PolyPhase® 20A parallel operation. See the Applications Information section.

**$V_{FB1}$ ,  $V_{FB2}$ ,  $V_{FB3}$  (M5, L5, K5):** The Negative Input of the Error Amplifier for Each of the Three Channels. Internally, each of these pins is connected to their respective output with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between each individual  $V_{FB}$  pin and ground. In PolyPhase operation, tying the  $V_{FB1}$  and  $V_{FB2}$  pins together allows for parallel operation up to 20A. See the Applications Information section for details.

**TK/SS1, TK/SS2, TK/SS3 (M9, M10, M11):** Output Voltage Tracking and Soft-Start Inputs. When one particular channel is configured to be the master, a capacitor to ground at this pin sets the ramp rate for the master channel's output voltage. When the channel is configured to be the slave, the  $V_{FB}$  voltage of the master channel is reproduced by a resistor divider and applied to this pin. Internal soft-start currents of 1.5 $\mu$ A are charging the soft-start capacitors. In dual output (2 + 1) mode, TK/SS1 and TK/SS2 need to be shorted externally.

# BLOCK DIAGRAM

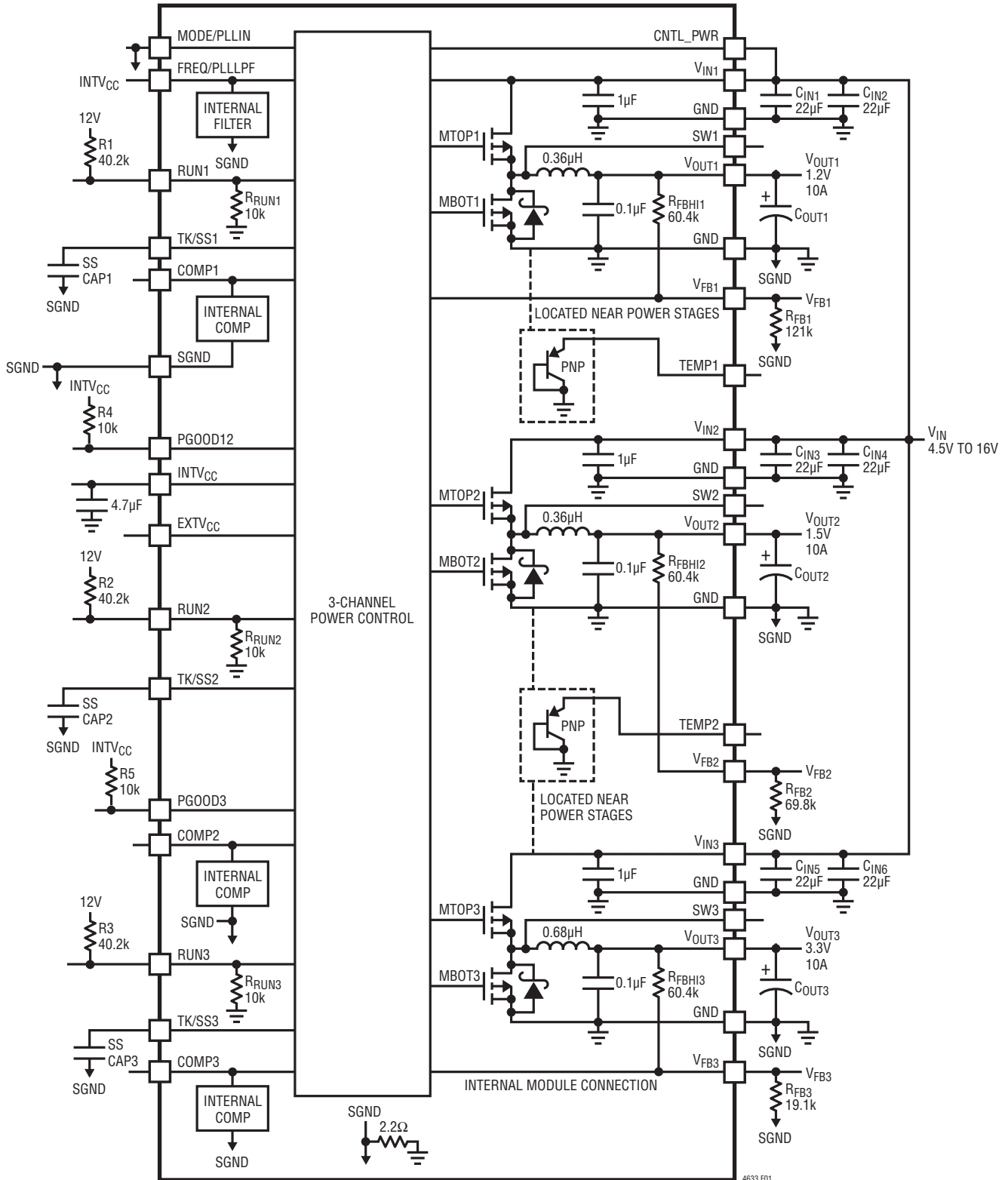


Figure 1. Simplified LTM4633 Block Diagram

## OPERATION

### Power Module Description

The LTM4633  $\mu$ Module regulator is a high performance triple output nonisolated switching mode DC/DC power supply. It can provide 10A per output with a few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from 0.8V DC to 1.8V DC ( $V_{OUT1}$  and  $V_{OUT2}$ ), and 0.8V DC to 5.5V DC ( $V_{OUT3}$ ) over a 2.375V to 16V input range with control bias on the CNTL\_PWR pin, or 4.7V to 16V with control bias tied to  $V_{IN}$ . When applying control bias in the range from 4.7V to 5.5V, then connect the bias to CNTL\_PWR and  $INVT_{CC}$ , otherwise if  $>5.5V$  only bias the CNTL\_PWR pin. The typical application schematic is shown in Figure 16.

The LTM4633 has three integrated constant-frequency current mode regulators, power MOSFETs, power inductors, and other supporting discrete components. The typical switching frequency is 750kHz. For switching noise-sensitive applications, it can be externally synchronized from 600kHz to 750kHz. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4633 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit in an overcurrent condition. An internal overvoltage monitor protects the output voltages in the event of an overvoltage  $>7.5\%$ . The top MOSFET is turned off and the bottom MOSFET is turned on until the output

overvoltage is cleared. There are two temperature monitors in the LTM4633. TEMP1 monitors the close relative temperature of channels 1 and 2, and TEMP2 monitors the close relative temperature of channels 2 and 3. The two diode connected PNP transistors are grounded in the module and can be used as general purpose temperature monitors using a device that is designed to monitor the single-ended connection.

Pulling any of the RUN pins below 1.3V forces the corresponding regulator channel into a shutdown state. The TK/SS pins are used for programming the output voltage ramp and voltage tracking during start-up for each of the channels. See the Applications Information section.

The LTM4633 is internally compensated to be stable over all operating conditions. Table 5 provides a guideline for input and output capacitances for several operating conditions. The LTpowerCAD™ software tool is provided for transient and stability analysis. The  $V_{FB}$  pin is used to program the output voltage with a single external resistor to ground.

Each of the channels, operate with a 120° phase shift for multiphase operation.  $V_{OUT1}$  and  $V_{OUT2}$  can be combined to provide a single 20A output. The two channels will not be operating 180° phase shift, but 120° phase when combined for a 20A design. So the input RMS current will be higher than a 180° phase shifted design. See the Applications Information section.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE/PLLIN pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

## APPLICATIONS INFORMATION

The typical LTM4633 application circuit is shown in Figure 16. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 5 for specific external capacitor requirements for particular applications.

### $V_{IN}$ to $V_{OUT}$ Step-Down Ratios

There are restrictions in the  $V_{IN}$  to  $V_{OUT}$  step-down ratio that can be achieved for a given input voltage. The  $V_{IN}$  to  $V_{OUT}$  minimum dropout is a function of load current and at very low input voltage and high duty cycle applications output power may be limited as the internal top power MOSFET is not rated for 10A operation at higher ambient temperatures. At very low duty cycles the minimum 90ns on-time must be maintained. See the Frequency Adjustment section and temperature derating curves.

### Output Voltage Programming

The PWM controller has an internal  $0.8V \pm 1\%$  reference voltage. As shown in the Block Diagram, a 60.4k precision internal feedback resistor connects the  $V_{OUT}$  and  $V_{FB}$  pins together.

The output voltage will default to 0.8V with no feedback resistor. Adding a resistor  $R_{FB}$  from  $V_{FB}$  to ground programs the output voltage:

$$V_{OUT} = 0.8V \cdot \left( \frac{60.4k + R_{FB}}{R_{FB}} \right), R_{FB} = \frac{48.32k}{V_{OUT} - 0.8V}$$

**Table 1.  $V_{FB}$  Resistor Table vs Various Output Voltages**

$V_{OUT}(V)$	0.8	1.0	1.2	1.5	1.8	2.5	3.3	5.0
$R_{FB}(k\Omega)$	Open	242	121	69.8	48.7	28.7	19.1	11.5

For parallel operation of  $V_{OUT1}$  and  $V_{OUT2}$ , the following equation can be used to solve for  $R_{FB}$ :

$$R_{FB} = \frac{60.4k}{\frac{2}{\frac{V_{OUT}}{0.8V} - 1}}$$

In the parallel operation the following pins should be tied together,  $V_{FB1}$  and  $V_{FB2}$  pins, COMP1 and COMP2 pins, TK/SS1 and TK/SS2, and RUN1 and RUN2.

### Input Capacitors

The LTM4633 module should be connected to a low AC impedance DC source. Additional input capacitors are needed for the RMS input ripple current rating. The  $I_{CIN(RMS)}$  equation which follows can be used to calculate the input capacitor requirement for each channel. Typically 22 $\mu$ F X7R ceramics are a good choice with RMS ripple current ratings of ~2A each. A 47 $\mu$ F to 100 $\mu$ F surface mount aluminum electrolytic capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)} \quad (1)$$

In the previous equation,  $\eta\%$  is the estimated efficiency of the power module in decimal form (0.nn) for a given  $V_{OUT}$ -to- $V_{IN}$  ratio.

The selection of  $C_{IN}$  is simplified by the 3-phase architecture and its impact on the worst-case RMS current draw occurs when only one channel is operating. This is true when the three channels are powered from a common  $V_{IN}$ . The channel with the highest duty cycle  $D$  peaking at 0.5 and maximum load current needs to be used in the



## APPLICATIONS INFORMATION

above formula. This will give the maximum RMS capacitor current requirement. Increasing the output current drawn from the other channels will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 50% when compared to a single phase power supply solution. If the three channels are powered from independent input sources, then each of the input RMS current ratings will need to be calculated specific to that channel.

### Output Capacitors

The LTM4633 is designed for low output voltage ripple noise. The bulk output capacitors defined as  $C_{OUT}$  are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements.  $C_{OUT}$  can be a low ESR tantalum capacitor, low ESR Polymer capacitor or ceramic capacitor. The typical output capacitance range is from 200 $\mu$ F to 470 $\mu$ F. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 5 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 5A/ $\mu$ s transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 5 matrix, and LTpowerCAD is available for free to conduct stability analysis. LTpowerCAD can calculate the output ripple reduction as the number of implemented phases increases by N times.

### Burst Mode Operation

The LTM4633 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply float the MODE/PLLIN pin. During Burst Mode operation, the peak current of the inductor is set to approximately 30% of the maximum peak current value in normal operation

even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise, the internal sleep line goes low, and the LTM4633 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

### Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4633 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE/PLLIN pin to INTV<sub>CC</sub> enables pulse-skipping operation. With pulse-skipping mode at light load, the internal current comparator may remain tripped for several cycles, thus skipping operation cycles. This mode has lower ripple than Burst Mode operation and maintains a higher frequency operation than Burst Mode operation.

### Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE/PLLIN pin to ground. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4633 output voltage is in regulation.

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### PLL, Frequency Synchronization

The LTM4633 device operates up to 750kHz. It can also be synchronized with an input clock that has a high level above 2V and a low level below 0.8V at the MODE/PLLIN pin. The FREQ/PLLLPF pin must be floating when synchronized to an incoming clock. Once the LTM4633 is synchronized to an external clock frequency, it will always be running in forced continuous operation. The synchronizing range is from 600kHz to 750kHz. For  $V_{OUT1,2,3} \leq 1.5V$  use 600kHz, and for  $V_{OUT1,2,3} \geq 1.5V$  use  $\geq 700kHz$ . These frequencies optimize efficiency, eliminate minimum on-time issues for less than 1V output, and control the inductor ripple currents over the input and output voltage ranges.

A DC voltage should be applied to the FREQ/PLLLPF pin to set the operating frequency when clock synchronization is not used. A voltage divider from the INTV<sub>CC</sub> pin (5V) to ground can be used to set the frequency to 600kHz (set to 1.4V), 700kHz (set to 1.6V), or tie the FREQ/PLLLPF pin to the INTV<sub>CC</sub> pin for 750kHz. The top resistor in the voltage divider should be 50k, and the bottom resistor should be 19.6k for 600kHz (set to 1.4V), or 23.7k for 700kHz (set to 1.6V). In most cases the FREQ/PLLLPF pin can be tied to the INTV<sub>CC</sub> pin for 750kHz operation as long as the minimum on-time is not below 100ns. See Figure 18 for an example.

### Parallel Channel Operation

For outputs that demand more than 10A of load current, the LTM4633 device can parallel  $V_{OUT1}$  and  $V_{OUT2}$  to supply 20A of load current. The two channels will operate at 120° of phase shift. The input RMS ripple current can be calculated using Equation 1. For example, 12V to 1.2V at 20A equates to duty cycle  $D = 0.1$ .

$$I_{CIN(RMS)} = \frac{20A}{0.84} \cdot \sqrt{0.1 \cdot (1-0.1)}$$

$I_{CIN(RMS)} = 7.14A_{RMS}$ , use  $4 \times 22\mu F$  16V X5R or X7R ceramic capacitors rated at  $2A_{RMS}$  each.

The LTM4633 regulators are inherently current mode controlled devices, so the paralleling of  $V_{OUT1}$  and  $V_{OUT2}$  channels will have good current sharing. This will balance the thermals in the design. Tie the COMP,  $V_{FB}$ , TK/SS and RUN pins together for these two channels to share the current evenly. Figure 18 shows a schematic of the parallel design.

### Minimum On-Time

Minimum on-time,  $t_{ON}$ , is the smallest time duration that any of the three regulator channels is capable of turning on the top MOSFET. It is determined by internal timing delays, and the gate charge required to turn-on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \cdot FREQ} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple and inductor ripple current will increase. The minimum on-time can be increased by lowering the switching frequency. A good rule of thumb is to use 100ns for the minimum on-time.

### Output Voltage Tracking

Output voltage tracking can be programmed externally using the TK/SS pins. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4633 uses an accurate 60.4k resistor internally for the top feedback resistor for each channel. Figure 2 shows an example of coincident tracking for  $V_{OUT1}$  and  $V_{OUT2}$ .  $V_{OUT1}$  is the master and  $V_{OUT2}$  is the slave:

$$V_{SLAVE} = \left( 1 + \frac{60.4k}{R_{TA}} \right) V_{TRACK}$$

## APPLICATIONS INFORMATION

$V_{TRACK}$  is the track ramp applied to the slave's track pin.  $V_{TRACK}$  has a control range of 0V to 0.8V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when  $V_{TRACK}$  is more than 0.8V.  $R_{TA}$  in Figure 2 will be equal to the  $R_{FB2}$  for coincident tracking.

The TK/SS pin of the master can be controlled by a capacitor placed on the master regulator TK/SS pin to ground. A 1.5 $\mu$ A current source will charge the TK/SS pin up to the reference voltage and then proceed up to  $INTV_{CC}$ . After the 0.8V ramp, the TK/SS pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. Foldback current limit is disabled during this sequence of turn-on during tracking or soft-starting. The TK/SS pins are pulled low when the

RUN pin is below 1.3V or  $INTV_{CC}$  drops below 3.5V. The total soft-start time can be calculated as:

$$t_{SS} = \left( \frac{0.8V \cdot C_{SS}}{1.5\mu A} \right)$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator channels will always start in pulse-skipping mode up to  $TK/SS = 0.64V$ . Between  $TK/SS = 0.64V$  and  $0.74V$ , it will operate in forced continuous mode and revert to the selected mode once  $TK/SS > 0.74V$ . The output ripple is minimized during the 100mV forced continuous mode window ensuring a clean PGOOD signal.

When the channel is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. Note that the small soft-

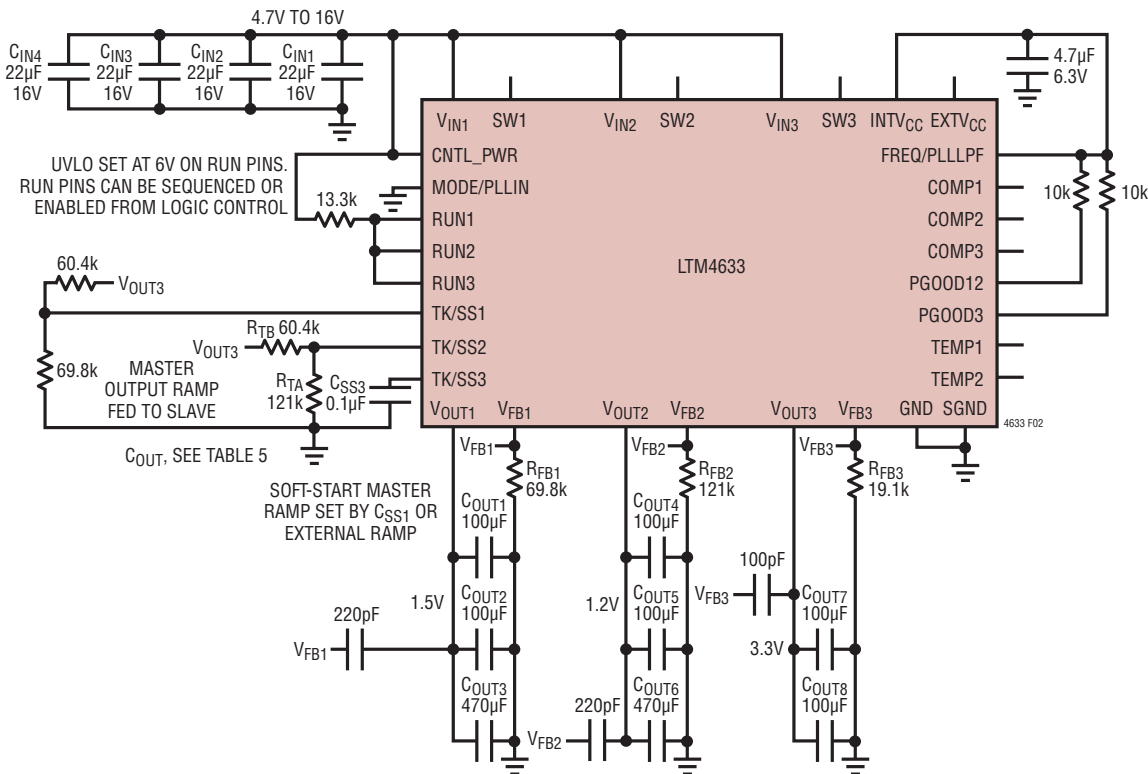


Figure 2. Triple Outputs, 1.5V and 1.2V Tracking to 3.3V

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start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider value to be small enough to make this error negligible. In order to track down another channel or supply after the soft-start phase expires, the LTM4633 is forced into continuous mode of operation as soon as  $V_{FB}$  is below the undervoltage threshold of 0.74V regardless of the setting of the MODE/PLLIN pin. However, the LTM4633 should always be set in force continuous mode tracking down when there is no load. After TK/SS drops below 0.1V, its channel will operate in discontinuous mode.

The master's TK/SS pin slew rate is directly equal to the master's output slew rate in Volts/Time. The equation:

$$R_{TB} = \left( \frac{MR}{SR} \right) \cdot 60.4k$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus  $R_{TB}$  is equal the 60.4k.  $R_{TA}$  is derived from equation:

$$R_{TA} = \frac{0.8V}{\frac{V_{FB}}{60.4k} + \frac{V_{FB} - V_{TRACK}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where  $V_{FB}$  is the feedback voltage reference of the regulator, and  $V_{TRACK}$  is 0.8V. Since  $R_{TB}$  is equal to the 60.4k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then  $R_{TA}$  is equal to  $R_{FB}$  with  $V_{FB} = V_{TRACK}$ . Therefore  $R_{TB} = 60.4k$ , and  $R_{TA} = 60.4k$  in Figure 2.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator.  $R_{TB}$  can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

### Power Good

The PGOOD12 pin is an open-drain pin that can be used to monitor valid output voltage regulation for  $V_{OUT1}$  and  $V_{OUT2}$ , and PGOOD3 for monitoring  $V_{OUT3}$ . These pins monitor a  $\pm 7.5\%$  window around the 0.8V feedback voltage on either  $V_{FB1,2,3}$  from the output regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring. Any of the PGOOD pins are pulled low when the RUN pin of the corresponding channel is pulled low.

### Overcurrent and Overvoltage Protection

Each of the regulator channels senses the peak inductor current on a cycle-by-cycle basis as current mode operation. When current limit is reached the output voltage will begin to fall and the internal current limit threshold will begin fold back as the output voltage falls below 50% of its value. Foldback current limit is disabled during start-up or track-up. Under a short-circuit condition at low duty cycle operation, each of the regulator channels will begin to skip cycles to limit the short-circuit current.

Overvoltage protection is implemented by monitoring each one of the regulator's  $V_{FB}$  pins. When the  $V_{FB}$  voltage exceeds  $\sim 7.5\%$  above the 0.8V reference value, then an internal comparator monitor will turn off the top power switch, and turn on the bottom power switch to protect the load. If the top power switch faults as a short, then a fuse or circuit breaker would be recommended to protect the system. This is due to the top switch being shorted while the bottom switch is turning on to protect the output from over voltage. High currents will flow and could damage the bottom switch.



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### Stability Compensation

The LTM4633 has already been internally compensated for all output voltages. Table 5 is provided for most application requirements with verified stability. LTpowerCAD is available for other control loop optimization.

### Run Enable

The RUN 1, 2, 3 pins have an enable threshold of 1.4V maximum, typically 1.3V with 175mV of hysteresis. They control the turn-on of their respective channel. There is a 10k resistor on each pin to ground. The RUN pins can be pulled up to  $V_{IN}$  for 5V operation, or a resistor can be placed on the pins and connected to  $V_{IN}$  for higher than 5V input. This resistor can be set along with the onboard 10k resistor such that an undervoltage lockout (UVLO) level can be programmed to shut down a particular regulator channel if  $V_{IN}$  falls below a set value. Use the equation:

$$R = \frac{10k(V_{UVLO} - 1.3V)}{1.3V}$$

where R is the resistor from the RUN pin to  $V_{IN}$  to set the UVLO trip point. For example, if the UVLO point is to be 6.25V while operating at 12V input:

$$R = \frac{10k(6.25V - 1.3V)}{1.3V} \approx 38.3k$$

See the Typical Application circuits in Figure 17. The RUN pins must not go above 6V maximum voltage. The RUN pins have to be pulled up to enable the regulators.

### SW Pins

The SW pins are generally used for testing purposes by monitoring the pin of interest. The SW pins can also be used to dampen out switch node ringing caused by LC parasitics in the switched current path. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor.

If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the PowerPath™ board inductance in combination with the MOSFET interconnect inductance.

First, the SW pin can be monitored using a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance, Z, can be calculated:

$$Z_{(L)} = 2\pi \cdot f \cdot L$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is then chosen so that its impedance is equal to the resistor at the ring frequency:

$$Z_{(C)} = \frac{1}{2\pi \cdot f \cdot C}$$

These values are a good place to start with. Modification to these components should be made to attenuate the ringing without lowering the regulator's conversion efficiency.

### INTV<sub>CC</sub> and EXTV<sub>CC</sub>

The LTM4633 has an onboard linear regulator fed by CNTL\_PWR which delivers a roughly 5V output at INTV<sub>CC</sub> to power the internal controller and MOSFET drivers for all three regulator channels. CNTL\_PWR requires a voltage between 4.7V to 16V. Apply a 4.7μF ceramic capacitor between INTV<sub>CC</sub> and ground for decoupling. If the voltage supplied to CNTL\_PWR is ≤ 5.5V, connect INTV<sub>CC</sub> to CNTL\_PWR. Otherwise, INTV<sub>CC</sub> should be left floating. To eliminate power loss in the onboard linear regulator and improve efficiency connect a supply from 4.7V to 6V at EXTV<sub>CC</sub>. Biasing EXTV<sub>CC</sub> will reduce the power loss in the internal LDO by  $(V_{CNTL\_PWR} - 5V) \cdot 70mA$ . If EXTV<sub>CC</sub> is used add a 1μF ceramic capacitor to ground at EXTV<sub>CC</sub> and

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ensure the voltage at CNTL\_PWR is always greater than the voltage at EXTV<sub>CC</sub> at all times including during start-up and shutdown. Connecting V<sub>OUT3</sub> to EXTV<sub>CC</sub> may present a convenient way to meet the sequencing requirement if V<sub>OUT3</sub> is a 5V output. Otherwise float EXTV<sub>CC</sub> if not used.

### Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a  $\mu$ Module package mounted to a hardware test board defined by JESD 51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients is found in JESD 51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers in lieu or to compliment any FEA activities may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the  $\mu$ Module regulator’s thermal performance in their application at various electrical and environmental operating conditions. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of-themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided later in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section provides values based on four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased:

1.  $\theta_{JA}$ : The thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2.  $\theta_{JCbottom}$ : The thermal resistance from the junction to the bottom of the product case, is determined with all of the internal power dissipation flowing through the bottom of the package. In a typical  $\mu$ Module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don’t generally match the user’s application.
3.  $\theta_{JCTop}$ : The thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical  $\mu$ Module regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of  $\theta_{JCbottom}$ , this value may be useful for comparing packages but the test conditions don’t generally match the user’s application.
4.  $\theta_{JB}$ : The thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the  $\mu$ Module package and into the board, and is really the sum of the  $\theta_{JCbottom}$  and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured at a specified distance from the package, using a 2-sided, 2-layer board. This board is described in JESD 51-9.

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A graphical representation of the aforementioned thermal resistances is given in Figure 3; blue resistances are contained within the  $\mu$ Module regulator, whereas green resistances are external to the  $\mu$ Module package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JEDEC 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a  $\mu$ Module regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the  $\mu$ Module package—as the standard defines for  $\theta_{JCtop}$  and  $\theta_{JCbottom}$ , respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4633, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with

laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4633 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSDE 51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4633 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields a set of derating curves provided in other sections of this data sheet.

After these laboratory tests have been performed and correlated to the LTM4633 model, then the  $\theta_{JB}$  and  $\theta_{BA}$  are summed together to correlate quite well with the device model conditions of no airflow or heat sinking in a properly

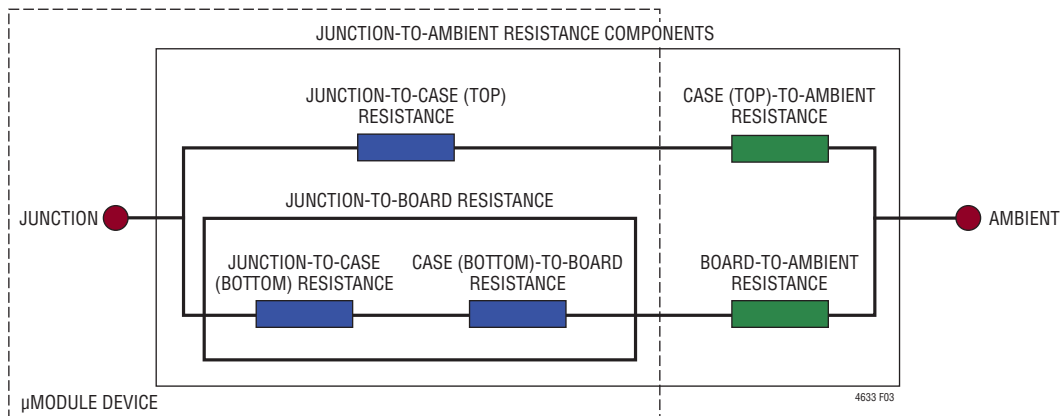


Figure 3. Graphical Representations of JEDEC51-12 Thermal Coefficients

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defined chamber. This  $\theta_{JB} + \theta_{BA}$  value should accurately equal the  $\theta_{JA}$  value because approximately 100% of power loss flows from the junction through the board into ambient with no air-flow or top mounted heat sink.

### LTM4633 Thermal Considerations and Output Current Derating

The power loss curves at 5V input, 8V input, and 12V input are in Figures 7 to 9. These power loss curves can be used in coordination with the load current derating curves in Figures 10 to 15 for calculating an approximate  $\theta_{JA}$  thermal resistance for the LTM4633 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a multiplicative factor of 1.4 at 125°C junction. This factor comes from the fact that the power loss of the regulator increases about 50% from 25°C to 150°C, thus a 50% spread over 125°C delta equates to ~0.4%/°C power loss increase. A 125°C maximum junction minus 25°C room temperature equates to a 100°C increase. This 100°C increase multiplied by 0.4%/°C equals a 40% power loss increase at the 125°C junction, thus the 1.4 multiplier.

The derating curves are plotted with the output current starting at 30A and the ambient temperature at 40°C. The 30A come from each of the three channels operating at 10A each. This simplifies the loading for this thermal testing. The output voltages are 1.0V and 1.8V when all three channels are loaded together in parallel. Channel 1 and Channel 2 are designed to operate with outputs up to 1.8V. Two additional derating curves are shown with Channel 1 and Channel 2 operating at 1.8V at 10A each for a total of 20A while Channel 3 is at 5V with 10A load current derated over ambient temperature. This is done to look at some of the different output power conditions to correlate thermal resistance numbers that can be used for derating the LTM4633 power module with different output power requirements. The power loss curve values

at a particular output voltage and output current for each output are taken and multiplied by 1.4 for increased power loss at 125°C junction. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 125°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 125°C minus the ambient operating temperature specifies how much temperature rise can be allowed. For example, in Figure 11, the 1V load current is derated to ~20A at ~85°C with no air and with heat sink. In Figure 9, the 12V to 1.0V power loss at 6.66A per channel is 1.4W. The total power loss would be 3 times 1.4W or 4.2W. The 4.2W is then multiplied by the 1.4 multiplier for 125°C junction. This 5.88W value is used with the total temperature rise of 125°C minus the 85°C ambient to calculate  $\theta_{JA}$  thermal resistance. If the 85°C ambient temperature is subtracted from the 125°C junction temperature, then the difference of 40°C divided by 5.88W equals a 6.8°C/W  $\theta_{JA}$  thermal resistance. Table 2 specifies a 6°C/W value which is very close. Tables 2 to 4 provide equivalent thermal resistances for 1.0V, 1.8V, and combination 1.8V and 5V outputs with and without air flow and heat sinking. The derived thermal resistances in Tables 2 and 4 for the various conditions can be multiplied by the calculated power loss as a function of the 125°C maximum junction temperature to determine if the temperature rise plus ambient is below the 125°C maximum junction temperature. Thermal or infrared imaging should be performed to validate the calculated results. Room temperature power loss can be derived from the power



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loss curves in Figures 8 to 10 and adjusted with the 1.4 multiplier. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm x 76mm. The BGA heat sinks are listed below Table 4.

### Temperature Monitoring (TEMP1 and TEMP2)

A diode connected PNP transistor is used for the TEMP monitor function by monitoring its voltage over temperature. The temperature dependence of this diode can be understood in the equation:

$$D = nV_T \ln\left(\frac{I_D}{I_S}\right)$$

where  $V_T$  is the thermal voltage ( $kT/q$ ), and  $n$ , the ideality factor is 1 for the two diode connected PNPs being used in the LTM4633. Since  $I_D$  has an exponential temperature dependence that can be understood from the typical empirical equation for  $I_S$ :

$$I_S = I_0 \exp\left(\frac{-V_{G0}}{V_T}\right)$$

where  $I_0$  is some process and geometry-dependent current ( $I_0$  is typically around 20 orders of magnitude larger than  $I_S$  at room temperature, so  $I_0$  is much larger than typical values of  $I_D$ ), and  $V_{G0}$  is the band gap voltage of 1.2V extrapolated to absolute zero of  $-273^\circ\text{C}$  Kelvin. Figure 4 shows a plot of the diode temperature characteristic of the diode connected PNP transistor biased with a 100ua current source. This plot would extend to the left back to 1.2V at  $-273^\circ\text{C}$  Kelvin. This curve is stop at  $-55^\circ\text{C}$  due to the test system limits.

If we take the  $I_S$  equation and substitute into the  $V_D$  equation, then we get:

$$V_D = V_{G0} - \left(\frac{kT}{q}\right) \ln\left(\frac{I_0}{I_D}\right), \quad V_T = \frac{kT}{q}$$

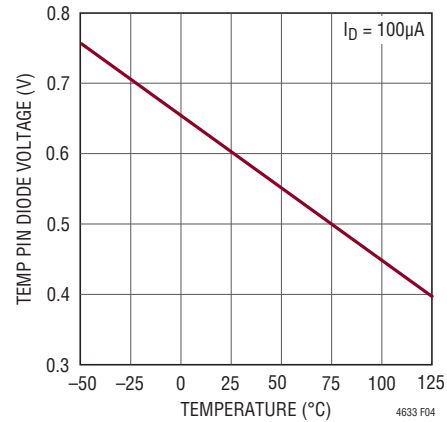


Figure 4. TEMP Pin Diode Voltage vs Temperature

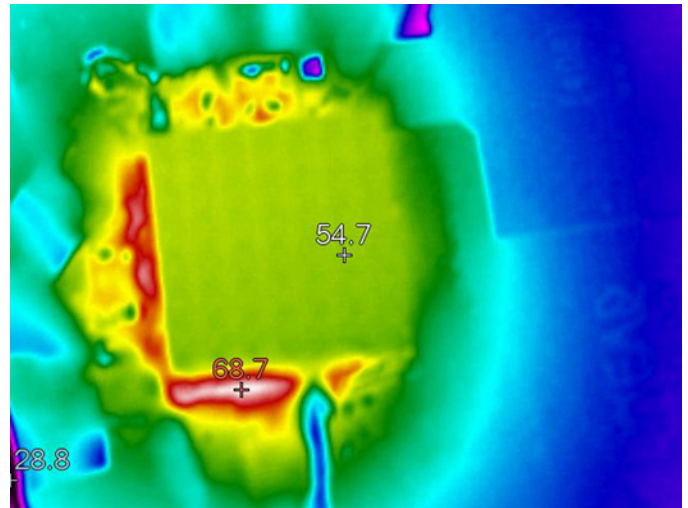


Figure 5. Thermal Plot for 12V Input to 1.8V at 10A Output 1, 1.8V at 10A Output 2, and 5V at 8A Output 3 with 200LFM of Airflow

The expression shows that the junction voltage of the PNP connected diode decreases linearly if  $I_0$  were constant from a value  $V_{G0}$  of 1.2V at absolute zero to a decreasing value with increased temperature.

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If we take this equation and differentiate it with respect to temperature  $T$ , then:

$$\frac{dV_D}{dt} = -\frac{V_{G0} - V_D}{T}$$

This  $dV_D/dT$  change as a function of temperature is the typical  $\sim -2.0\text{mV}/^\circ\text{C}$ . This equation is simplified for the first order derivation.

Solving for  $T$ ,  $T = -(V_{G0} - V_D)/dV_D$  provide the temperature.

1st Example: Figure 4 for  $27^\circ\text{C}$ , or  $300^\circ\text{C}$  Kelvin the diode voltage is  $0.598\text{V}$ , thus,  $300^\circ\text{C} = -(1200\text{mV} - 598\text{mV})/ -2.0\text{mV}/^\circ\text{C}$

2nd Example: Figure 4 for  $75^\circ\text{C}$ , or  $350^\circ\text{C}$  Kelvin the diode voltage is  $0.50\text{V}$ , thus,  $350^\circ\text{C} = -(1200\text{mV} - 500\text{mV})/ -2.0\text{mV}/^\circ\text{C}$

Converting the Kelvin scale to Celsius is simply taking the Kelvin temp and subtracting  $-273^\circ\text{C}$  Kelvin from it.

A typical forward voltage is measured and placed in the electrical characteristics section of the data sheet, and Figure 4 is the plot of this forward voltage. Measure this forward voltage at  $27^\circ\text{C}$  to establish a reference point. Then use the above expression while measuring the forward voltage over temperature will provide a general temperature monitor.

The diode connected PNP transistor at the TEMP pins can be used to monitor the internal temperature of the LTM4633. A general temperature monitor can be implemented by connecting a resistor between TEMP and  $V_{IN}$  to set the current to  $100\mu\text{A}$ , and then monitoring the diode voltage drop with temperature. See Figure 19 for an example.

### Safety Considerations

The LTM4633 module does not provide galvanic isolation from  $V_{IN}$  to any of the three  $V_{OUTS}$ . There is no internal fuse. If required, a slow blow fuse with a rating higher than the maximum input current can be used to protect

the unit in case of a catastrophic failure. An inline circuit breaker function can also be used instead of a fuse.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation.

### Layout Checklist/Example

The high integration of LTM4633 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

Use large PCB copper areas for high current paths, including  $V_{IN}$ , GND,  $V_{OUT1}$ ,  $V_{OUT2}$ , and  $V_{OUT3}$ . It helps to minimize the PCB conduction loss and thermal stress. Place high frequency ceramic input and output capacitors next to the  $V_{IN}$ , GND and the  $V_{OUT}$  pins to minimize high frequency noise.

Place a dedicated power ground layer underneath the unit. To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

Do not put vias directly on the pads, unless they are capped or plated over. Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit. Bring out test points on the signal pins for monitoring. Figure 6 gives a good example of the recommended layout.

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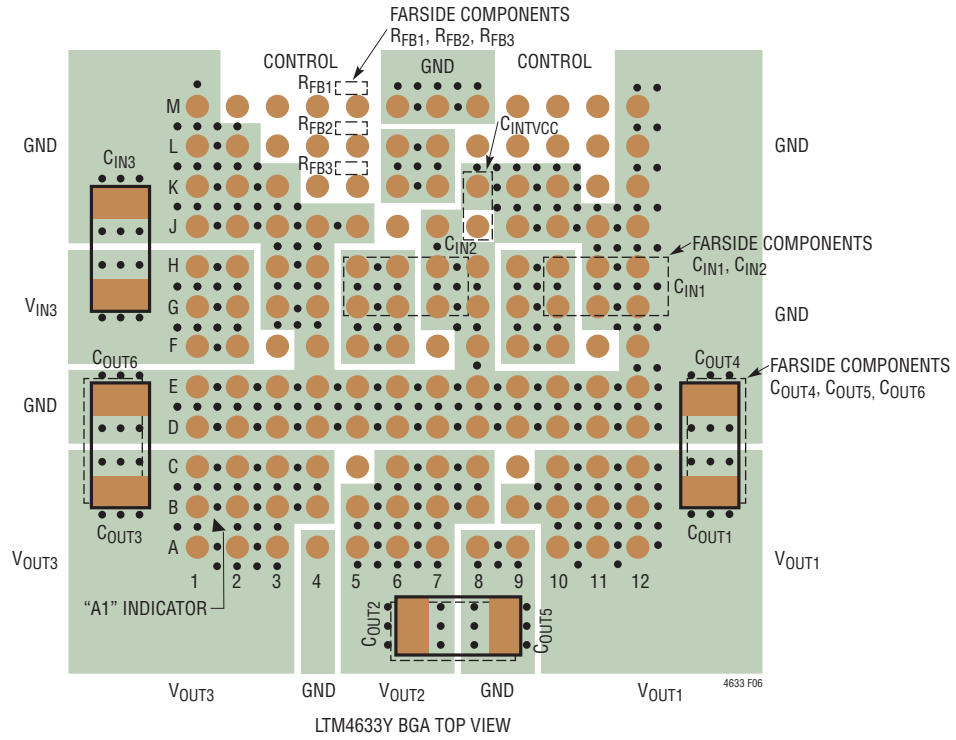


Figure 6. Recommended PCB Layout

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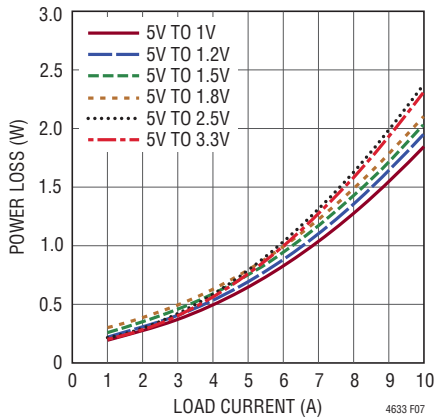


Figure 7. 5V Input Power Loss

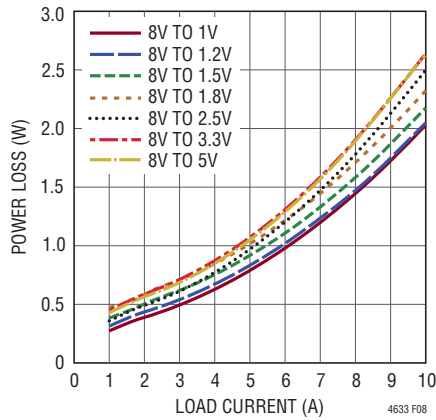


Figure 8. 8V Input Power Loss

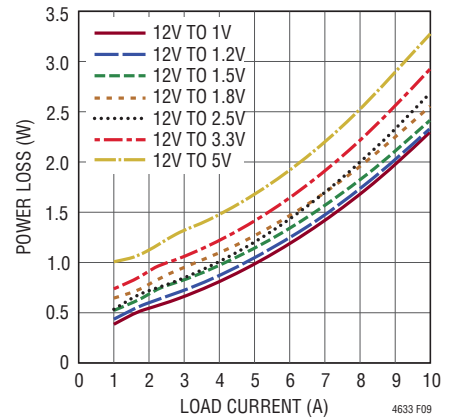


Figure 9. 12V Input Power Loss

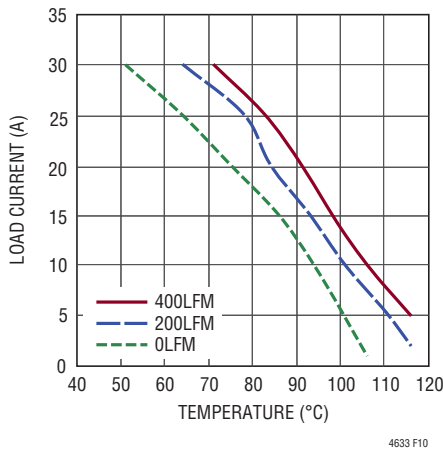


Figure 10. 12V<sub>IN</sub>, 1V<sub>OUT</sub>, No Heat Sink, All Channels at 10A Each

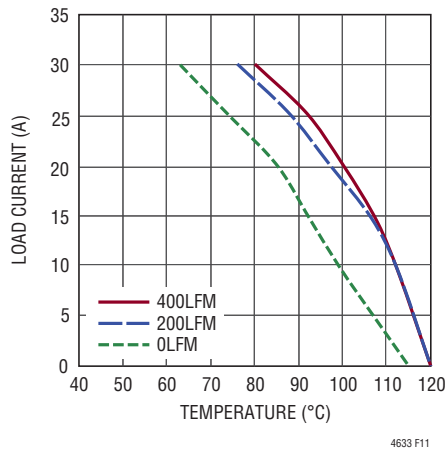


Figure 11. 12V<sub>IN</sub>, 1V<sub>OUT</sub>, With Heat Sink, All Channels at 10A Each

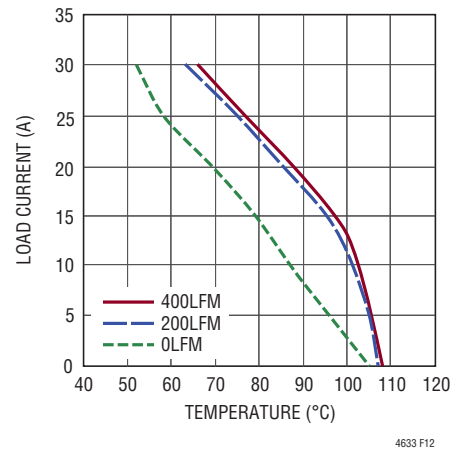


Figure 12. 12V<sub>IN</sub>, 1.8V<sub>OUT</sub>, No Heat Sink, All Channels at 10A Each

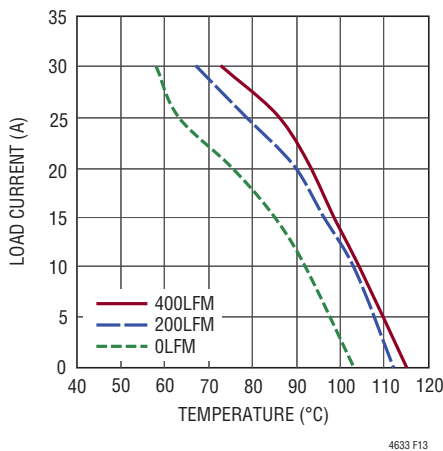


Figure 13. 12V<sub>IN</sub>, 1.8V<sub>OUT</sub>, With Heat Sink, All Channels at 10A Each

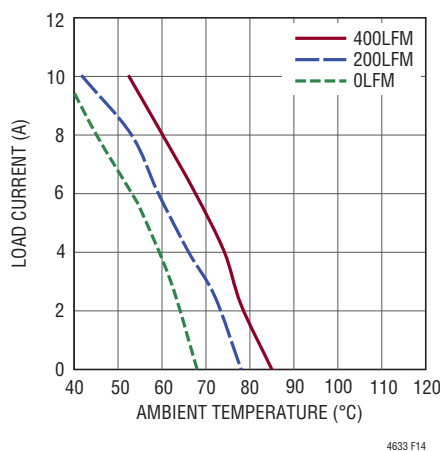


Figure 14. 12V<sub>IN</sub>, 1.8V<sub>OUT</sub> at 20A, 5V<sub>OUT</sub> Derating, No Heat Sink

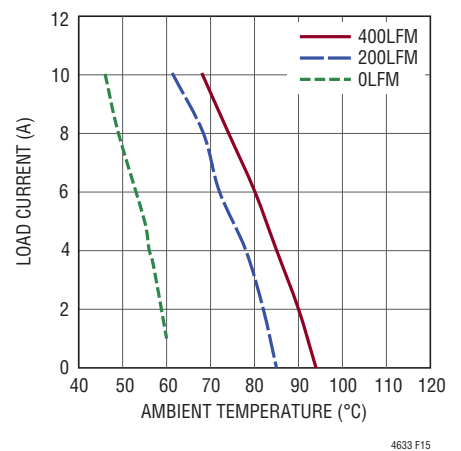


Figure 15. 12V<sub>IN</sub>, 1.8V<sub>OUT</sub> at 20A, 5V<sub>OUT</sub> Derating, with Heat Sink

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**Table 2. 1.0V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figures 10	12	Figure 7 to 9	0	None	7.5
Figures 10	12	Figure 7 to 9	200	None	6
Figures 10	12	Figure 7 to 9	400	None	5
Figures 11	12	Figure 7 to 9	0	BGA Heat Sink	6
Figures 11	12	Figure 7 to 9	200	BGA Heat Sink	4.75
Figures 11	12	Figure 7 to 9	400	BGA Heat Sink	4.0

**Table 3. 1.8V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figures 12	12	Figure 7 to 9	0	None	7.5
Figures 12	12	Figure 7 to 9	200	None	6
Figures 12	12	Figure 7 to 9	400	None	5
Figures 13	12	Figure 7 to 9	0	BGA Heat Sink	6
Figures 13	12	Figure 7 to 9	200	BGA Heat Sink	4.75
Figures 13	12	Figure 7 to 9	400	BGA Heat Sink	4.0

**Table 4. 5V Output, 1.8V Output at 20A on Ch1 and Ch2**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figures 14	12	Figure 7 to 9	0	None	7.5
Figures 14	12	Figure 7 to 9	200	None	6
Figures 14	12	Figure 7 to 9	400	None	5
Figures 15	12	Figure 7 to 9	0	BGA Heat Sink	6
Figures 15	12	Figure 7 to 9	200	BGA Heat Sink	4.75
Figures 15	12	Figure 7 to 9	400	BGA Heat Sink	4.0

**Heat Sink Manufacturer Part Number Website**

Aavid Thermalloy	375424B00034G	www.aavid.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com



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**Table 5. Output Voltage Response Versus Component Matrix (Refer to Figure 16) 0 to 5A Load Step Typical Measured Values**

C <sub>OUT1</sub> CERAMIC VENDORS	VALUE	PART NUMBER	C <sub>OUT2</sub> BULK VENDORS	VALUE	PART NUMBER	ESR	C <sub>IN</sub> BULK VENDORS	VALUE	PART NUMBER
TDK	100μF 6.3V	C4532X5R0J107MZ	Sanyo POSCAP	470μF 2.5V	2R5TPD470M5	9mΩ	Sanyo	56μF 25V	25SVP56M
Murata	100μF 6.3V	GRM32ER60J107M	Sanyo POSCAP	470μF 6.3V	6TPD470M	9mΩ			
AVX	100μF 6.3V	18126D107MAT							

V <sub>OUT</sub>	C <sub>IN</sub> (CERAMIC)	C <sub>IN</sub> (BULK)*	C <sub>OUT1</sub> (CERAMIC)	C <sub>OUT2</sub> (BULK)	C <sub>FF</sub>	V <sub>IN</sub>	DROOP	PEAK-TO-PEAK DEVIATION AT 7A LOAD STEP	~RECOVERY TIME	LOAD STEP	R <sub>FB</sub>	FREQ
1V	22μF × 3	56μF	100μF × 2	470μF	220pF	5V, 12V	39mV	80mV	100μs	5A/μs	242kΩ	700kHz
1V	22μF × 3	56μF	100μF × 3	220μF	220pF	5V, 12V	38mV	78mV	100μs	5A/μs	242kΩ	700kHz
1.2V	22μF × 3	56μF	100μF × 2	470μF	220pF	5V, 12V	40mV	90mV	100μs	5A/μs	121kΩ	700kHz
1.2V	22μF × 3	56μF	100μF × 3	220μF	220pF	5V, 12V	43mV	88mV	100μs	5A/μs	121kΩ	700kHz
1.5V	22μF × 3	56μF	100μF × 2	470μF	220pF	5V, 12V	50mV	100mV	100μs	5A/μs	69.8kΩ	700kHz
1.5V	22μF × 3	56μF	100μF × 3	220μF	220pF	5V, 12V	63mV	120mV	100μs	5A/μs	69.8kΩ	700kHz
1.8V	22μF × 3	56μF	100μF × 2	220μF	100pF	5V, 12V	65mV	120mV	100μs	5A/μs	48.7kΩ	700kHz
1.8V	22μF × 3	56μF	100μF × 4	None	100pF	5V, 12V	67mV	130mV	100μs	5A/μs	48.7kΩ	700kHz
2.5V	22μF × 3	56μF	100μF	220μF	220pF	5V, 12V	121mV	240mV	100μs	5A/μs	28.7kΩ	700kHz
2.5V	22μF × 3	56μF	100μF × 2	None	100pF	5V, 12V	120mV	240mV	100μs	5A/μs	28.7kΩ	700kHz
3.3V	22μF × 3	56μF	100μF × 2	None	100pF	5V, 12V	140mV	300mV	100μs	5A/μs	19.1kΩ	700kHz
3.3V	22μF × 3	56μF	100μF	None	47pF	5V, 12V	180mV	320mV	100μs	5A/μs	19.1kΩ	700kHz
5V	22μF × 3	56μF	100μF × 2	None	100pF	12V	220mV	400mV	100μs	5A/μs	11.5kΩ	700kHz
5V	22μF × 3	56μF	100μF × 3	None	330pF	12V	220mV	400mV	100μs	5A/μs	11.5kΩ	700kHz

\*Bulk capacitance is optional if V<sub>IN</sub> has very low input impedance.