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38V, 10A DC/DC µModule Regulator with Advanced Input and Load Protection

FEATURES

- **Wide Operating Input Voltage Range: 4.5V to 38V**
- **10A DC Typical, 12A Peak Output Current**
- **Output Range: 0.6V to 6V**
- **±1.5% Maximum Total Output DC Voltage Error**
- **Differential Remote Sense Amplifier for POL Regulation**
- **Internal Temperature, Analog Indicator Output**
- **Overcurrent Foldback and Overtemperature Protection**
- **Current Mode Control/Fast Transient Response**
- **Parallelable for Higher Output Current**
- Selectable Pulse-Skipping Operation
- Soft-Start/Voltage Tracking/Pre-Bias Start-Up
- 15mm × 15mm × 5.01mm BGA Package
- SnPb or RoHS Compliant Finish

Input Protection

- UVLO, Overvoltage Shutdown and Latchoff Thresholds
- N-Channel Overvoltage Power-Interrupt MOSFET Driver
- Surge Stopper Capable with Few External Components

Load Protection

- Robust, Resettable Latchoff Overvoltage Protection
- N-Channel Overvoltage Crowbar Power MOSFET Driver

APPLICATIONS

- Ruggedized Electronics
- Avionics and Industrial Equipment

DESCRIPTION

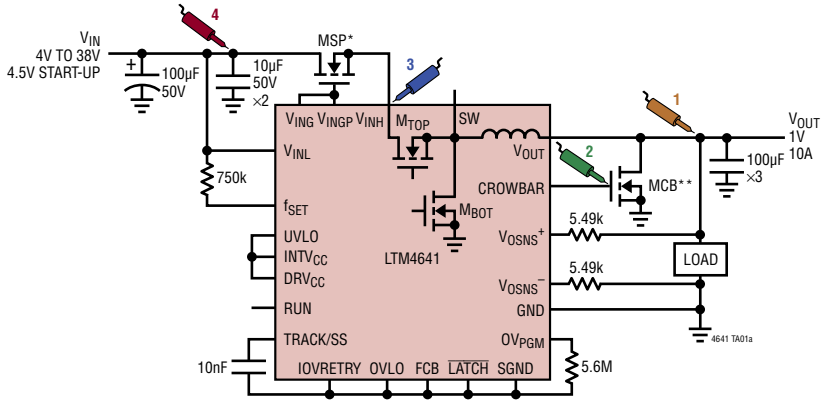
The LTM®4641 is a switch mode step-down DC/DC µModule® (micromodule) regulator with advanced input and load protection features. Trip detection thresholds for the following faults are customizable: input undervoltage, overtemperature, input overvoltage and output overvoltage. Select fault conditions can be set for latchoff or hysteretic restart response—or disabled. Included in the package are the switching controller and housekeeping ICs, power MOSFETs, inductor, overvoltage drivers, biasing circuitry and supporting components. Operating from input voltages of 4V to 38V (4.5V start-up), the device supports output voltages from 0.6V to 6V, set by an external resistor network remote sensing the point-of-load's voltage.

The LTM4641's high efficiency design can deliver up to 10A continuous current with a few input and output capacitors. The regulator's constant on-time current mode control architecture enables high step-down ratios and fast response to transient line and load changes. The LTM4641 is offered in a 15mm × 15mm × 5.01mm with SnPb or RoHS compliant terminal finish.

Click to view associated TechClip Videos.

TYPICAL APPLICATION

µModule Regulator with Input Disconnect and Fast Crowbar Output Overvoltage Protection

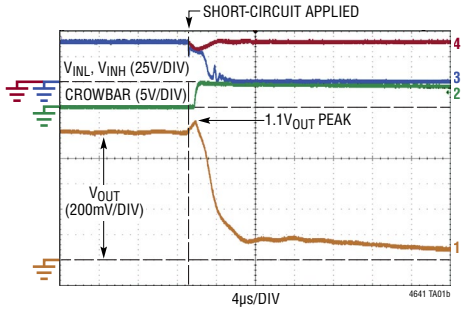


SGND CONNECTS TO GND INTERNAL TO µMODULE REGULATOR

*MSP: (OPTIONAL) SERIES-PASS OVERVOLTAGE POWER INTERRUPT MOSFET, NXP PSMN014-60LS

**MCB: (OPTIONAL) OUTPUT OVERVOLTAGE CROWBAR MOSFET, NXP PH2625L

1V Load Protected from M_{TOP} Short-Circuit at $38V_{IN}$



TESTED AT WORST-CASE CONDITION: NO LOAD

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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Terminal Voltages

- V_{INL}, V_{INH}, SW, f_{SET} ..... –0.3V to 40V
- V_{OUT} ..... –0.3V to 9.2V
- V_{ING} ..... –0.3V to V_{INH} + 20V
- $INTV_{CC}$, DRV_{CC}, RUN, TRACK/SS, PGOOD, CROWBAR, HYST ..... –0.3V to 6V
- FCB, TMR ..... -0.3V to $INTV_{CC}$ + 0.3V
- COMP ..... –0.3V to 2.7V
- V_{OSNS}^+, V_{ORB}^+ ..... –0.6V to 9.7V
- V_{OSNS}^-, V_{ORB}^- ..... V_{OSNS}^+ – 2.7V to V_{OSNS}^+ + 0.3V
- $\overline{OTBH}$, UVLO, IOVRETRY, OVLO, $\overline{LATCH}$ ..... –0.3V to 7.5V
- TEMP, OV_{PGM} ..... –0.3V to 1.5V

Terminal Currents

- $INTV_{CC}$ (Continuous) ..... –30mA
- $INTV_{CC}$ (Continuous; CROWBAR Sourcing 15mA) ..... –15mA
- CROWBAR (Continuous) ..... –15mA
- V_{INGP} (Continuous) ..... –50mA to 15mA
- $1V_{REF}$ (Continuous) ..... –1mA to 1mA

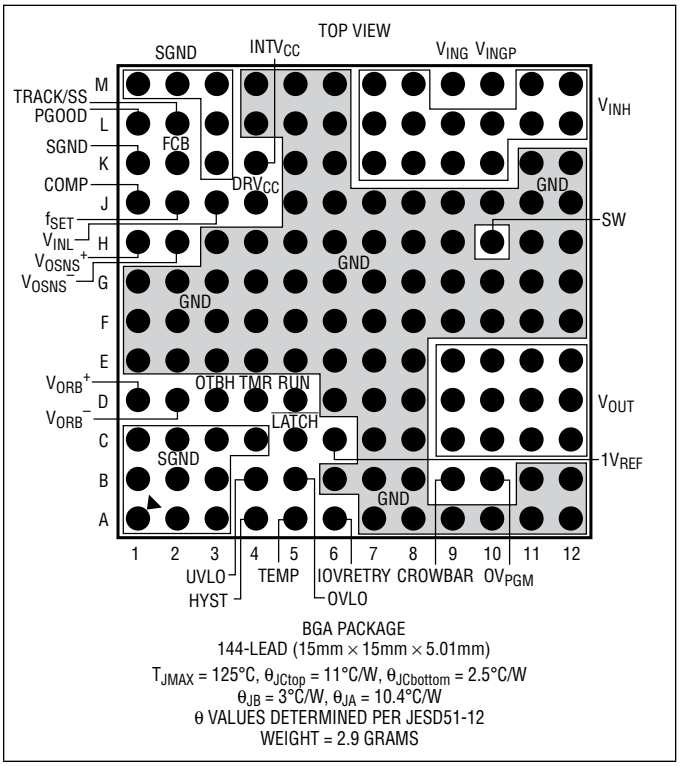
Internal Operating Temperature Range (Note 2)

- E- and I-Grades ..... –40°C to 125°C
- MP-Grade ..... –55°C to 125°C

Storage Temperature Range ..... –55°C to 125°C

Peak Package Body Temperature (SMT Reflow) ... 245°C

PIN CONFIGURATION



BGA PACKAGE
144-LEAD (15mm × 15mm × 5.01mm)
T_{JMAX} = 125°C, θ_{JCtop} = 11°C/W, $\theta_{JCbottom}$ = 2.5°C/W
θ_{JB} = 3°C/W, θ_{JA} = 10.4°C/W
θ VALUES DETERMINED PER JESD51-12
WEIGHT = 2.9 GRAMS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4641EY#PBF	SAC305 (RoHS)	LTM4641Y	e1	BGA	4	–40°C to 125°C
LTM4641IY#PBF	SAC305 (RoHS)	LTM4641Y	e1	BGA	4	–40°C to 125°C
LTM4641IY	SnPb (63/37)	LTM4641Y	e0	BGA	4	–40°C to 125°C
LTM4641MPY#PBF	SAC305 (RoHS)	LTM4641Y	e1	BGA	4	–55°C to 125°C
LTM4641MPY	SnPb (63/37)	LTM4641Y	e0	BGA	4	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INH} = V_{INL} = 28V, per the typical application shown in Figure 45, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	4.5		38	V
V_{OUT}	Output Voltage Range	Use R_{SET1A} = R_{SET1B} ≤ 8.2kΩ. R_{fSET} Values Recommended in Table 1	●	0.6		6	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load, and Prior to UVLO	4.5V ≤ V_{IN} ≤ 38V, 0A ≤ I_{OUT} ≤ 10A V_{IN} = 4V (Ramped Down from 4.5V), I_{OUT} = 0A	● ●	1.773 1.773	1.800 1.800	1.827 1.827	V V
Input Specifications							
$V_{RUN(ON,OFF)}$	RUN On/Off Threshold	Run Rising, Turn On Run Falling, Turn Off	● ●	 0.8	1.25 1.15	2	V V
$I_{RUN(ON)}$	RUN Pull-Up Current	V_{RUN} = 0V V_{RUN} = 3.3V	● ●	–580 –220	–520 –165	–460 –110	µA µA
$I_{RUN(OFF)}$	RUN Pull-Down Current, Switching Inhibited	V_{RUN} = 3.3V, UVLO = 0V (M_{HYST} On)			1		nA
$V_{INL(UVLO)}$	V_{INL} Undervoltage Lockout	V_{INL} Rising V_{INL} Falling Hysteresis	● ● ●	 3.5 300	4.2 3.8 400	4.5 4	V V mV
$I_{INRUSH(VINH)}$	Input Inrush Current Through V_{INH}, at Start-Up	C_{SS} = Open			230		mA
$I_{Q(VINH)}$	Power Stage Bias Current (I_{VINH}) at No Load	I_{OUT} = 0A and: FCB ≥ 0.84V (Pulse-Skipping Mode) FCB ≤ 0.76V (Forced Continuous Mode) Shutdown, RUN = 0			 8 29 0.2		 mA mA mA
$I_{Q(VINL)}$	Control Bias Current (I_{VINL})	$INTV_{CC}$ Connected to DRV_{CC} and: V_{IN} = 28V, I_{OUT} = 0A V_{IN} = 28V, I_{OUT} = 10A V_{IN} = 28V, Shutdown, RUN = 0			 14.5 15.5 5		 mA mA mA
$I_{S(VINH)}$	Power Stage Input Current (I_{VINH}) at Full Load	I_{OUT} = 10A and: V_{IN} = 4.5V V_{IN} = 28V V_{IN} = 38V			 4.65 790 590		 A mA mA
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	(Note 3)	●	0		10	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{IN} from 4.5V to 38V, I_{OUT} = 0A	●		0.02	0.15	%
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	I_{OUT} from 0A to 10A (Note 3)	●		0.04	0.15	%
$V_{OUT(AC)}$	Output Voltage Ripple Amplitude	I_{OUT} = 0A			16		mV_{P-P}
f_S	Output Voltage Ripple Frequency	I_{OUT} = 0A I_{OUT} = 10A			290 330		kHz kHz
$V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A			10		mV
t_{START}	V_{IN}-to-V_{OUT} Start-Up Time	RUN Electrically Open Circuit, Time Between Application of V_{IN} to V_{OUT} Becoming Regulated, OV_{PGM} = 1.5V, C_{TMR} = C_{SS} = Open			3		ms
$t_{RUN(ON-DELAY)}$	RUN-to-V_{OUT} Turn-On Response Time	V_{IN} Established, (TMR-Set POR Time Expired) Time Between RUN Releasing from GND to PGOOD Going Logic High, C_{SS} = Open, OV_{PGM} = 1.5V			175	400	µs
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load Step	I_{OUT} from 0A to 5A at 5A/µs I_{OUT} from 5A to 0A at 5A/µs			40 40		mV mV
$t_{SETTLE(LS)}$	Settling Time for Dynamic Load Step	I_{OUT} from 0A to 5A at 5A/µs I_{OUT} from 5A to 0A at 5A/µs			20 20		µs µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INH} = V_{INL} = 28V, per the typical application shown in Figure 45, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{OUT(PK)}$	Output Current Limit	5.1kΩ Pull-Up from PGOOD to 5V Source, I_{OUT} Ramped Up Until V_{OUT} Below PGOOD Lower Threshold, PGOOD Pulls Logic Low			24		A
$I_{VINH(IOUT\_SHORT)}$	Power Stage Input Current During Output Short Circuit	V_{OUT} Electrically Shorted to GND			45		mA
Control Section							
V_{FB}	Differential Feedback Voltage from V_{OSNS}^+ to V_{OSNS}^-	I_{OUT} = 0A	●	591	600	609	mV
$I_{TRACK/SS}$	TRACK/SS Pull-Up Current	$V_{TRACK/SS}$ = 0V		–0.45	–1		µA
V_{FCB}	FCB Threshold			0.76	0.8	0.84	V
I_{FCB}	FCB Pin Current	V_{FCB} = 0.8V			0	±1	µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			43	75	ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			220	300	ns
$V_{OSNS(DM)}$	Remote Sense Pin-Pair Differential Mode Input Range	Valid Differential V_{OSNS}^+ -to- V_{OSNS}^- Range (Use R_{SET1A} = R_{SET1B} ≤ 8.2k)	●	0		2.7	V
$V_{OSNS(CM)}$	Remote Sense Pin-Pair Common Mode Input Range	Valid V_{OSNS}^- Common Mode Range Valid V_{OSNS}^+ Common Mode Range (Use R_{SET1A} = R_{SET1B} ≤ 8.2k)	● ●	–0.3		 3	V V
$R_{IN(VOSNS+)}$	Input Resistance	V_{OSNS}^+ to GND		16318	16400	16482	Ω
$INTV_{CC}$, DRV_{CC}, $1V_{REF}$							
V_{INTVCC}	Internal V_{CC} Voltage	6V ≤ V_{IN} ≤ 38V, $INTV_{CC}$ Not Connected to DRV_{CC}, DRV_{CC} = 5.3V	●	5.1	5.3	5.4	V
$\frac{\Delta V_{INTVCC(LOAD)}}{V_{INTVCC}}$	$INTV_{CC}$ Load Regulation	RUN = 0V, $INTV_{CC}$ Not Connected to DRV_{CC}, DRV_{CC} = 5.3V and: I_{INTVCC} Varied from 0mA to –20mA I_{INTVCC} Varied from 0mA to –30mA			 –0.7 –1	 ±2 ±3	 % %
$V_{INTVCC(LOWLINE)}$	$INTV_{CC}$ Voltage at Low Line	V_{IN} = 4.5V, R_{SET1A} = R_{SET1B} = 0Ω (~0.6V_{OUT}, R_{fSET} Value Recommended in Table 1)	●	4.2	4.3		V
$DRV_{CC(UVLO)}$	DRV_{CC} Undervoltage Lockout	DRV_{CC} Rising DRV_{CC} Falling	● ●	3.9 3.2	4.05 3.35	4.2 3.5	V V
I_{DRVCC}	DRV_{CC} Current	$INTV_{CC}$ Not Connected to DRV_{CC}, DRV_{CC} = 5.3V, R_{SET1A}, R_{SET1B} and R_{SET2} Setting V_{OUT} to: 1.8V_{OUT}, R_{fSET} = 2MΩ, 0A ≤ I_{OUT} ≤ 10A 6.0V_{OUT}, R_{fSET} = Open, 0A ≤ I_{OUT} ≤ 10A (Use R_{SET1A} = R_{SET1B} ≤ 8.2k)			 11 20	 18 27	 mA mA
$V_{1VREF(DC)}$	$1V_{REF}$ DC Voltage Regulation	I_{1VREF} = 0mA I_{1VREF} = ±1mA	● ●	0.985 0.980	1.000 1.000	1.015 1.020	V V
PGOOD Output							
$V_{PGOOD(TH)}$	Power Good Window, Logic State Transition Thresholds	Ramping Differential V_{OSNS}^+ – V_{OSNS}^- Voltage: Up, PGOOD Goes Logic Low → High Up, PGOOD Goes Logic High → Low Down, PGOOD Goes Logic Low → High Down, PGOOD Goes Logic High → Low		 533 645 621 525	 556 660 644 540	 579 675 667 555	 mV mV mV mV
$V_{PGOOD(HYST)}$	Hysteresis	Differential V_{OSNS}^+ – V_{OSNS}^- Voltage Returning		8	16	24	mV
$V_{PGOOD(VOL)}$	Logic-Low Output Voltage	I_{PGOOD} = 5mA	●		75	400	mV
$t_{PGOOD(DELAY)}$	PGOOD Logic-Low Blanking Time	Delay Between Differential V_{OSNS}^+ – V_{OSNS}^- Voltage Exiting PGOOD Valid Window to PGOOD Going Logic Low (Note 4)			12		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INH} = V_{INL} = 28V, per the typical application shown in Figure 45, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Interrupt MOSFET Drive							
V_{VING}	Gate Drive Voltage for Power-Interrupt MOSFET, MSP	V_{IN} = 4.5V, 0A ≤ I_{OUT} ≤ 10A, V_{ING} Sourcing 1µA V_{IN} = 28V, 0A ≤ I_{OUT} ≤ 10A, V_{ING} Sourcing 1µA V_{IN} = 38V, 0A ≤ I_{OUT} ≤ 10A, V_{ING} Sourcing 1µA V_{IN} = 4V (Ramped Down from 4.5V), I_{OUT} = 0A, V_{ING} Sourcing 1µA	● ● ● ●	11.5 35 45 10.5	13.3 38.4 48.4 11.5	15.5 41 51.5 14.2	V V V V
$I_{VING(UP)}$	V_{ING} Pull-Up Current	V_{ING} Tied to V_{INGP}, and: V_{IN} = 4.5V, V_{ING} Pulled to 6.5V V_{IN} = 28V, V_{ING} Pulled to 30V	 ● ●	 350 425	 475 550	 600 675	 µA µA
$I_{VING\_DOWN(CROWBAR\ ACTIVE,CROWBAR\ INACTIVE)}$	V_{ING} Pull-Down Current	V_{ING} Tied to V_{INGP}, Pulled to 33V, and: RUN Pulled to 0V (CROWBAR Inactive) OV_{PGM} Pulled to 0V (CROWBAR Active)	 ● ●	 3 24	 20 27	 30 30	 mA mA
$t_{VING(OVP\_DELAY)}$	V_{ING} OVP Pull-Down Delay	OV_{PGM} Driven from 650mV to 550mV, V_{ING} Discharge Response Time	●		1.3	2.6	µs
$I_{VINGP(LEAK)}$	Zener Diode Leakage Current	V_{INGP} Driven to (V_{INH} + 10V)			1		nA
$V_{INGP(CLAMP)}$	Zener Diode Breakdown Voltage	V_{INGP}-to-V_{INH} Differential Voltage; I_{VINGP} = 5mA			15		V
Fault Pins and Functions							
V_{OVPGM}	Default Output Overvoltage Program Setting	OV_{PGM} Electrically Open Circuit	●	650	666	680	mV
$I_{OVPGM(UP)}$	OV_{PGM} Pull-Up Current	OV_{PGM} = 0V	●	–2.07	–2	–1.91	µA
$I_{OVPGM(DOWN)}$	OV_{PGM} Pull-Down Current	OV_{PGM} = 1V	●	0.945	1	1.06	µA
OVP_{TH}	Output Overvoltage Protection Inception Threshold	Ramping Up Differential V_{OSNS}^+-to-V_{OSNS}^- Voltage Until CROWBAR Outputs Logic High	●	647	666	683	mV
OVP_{ERR}	Output Overvoltage Protection Inception Error	Difference Between OVP_{TH} and V_{OVPGM} (OVP_{TH}-V_{OVPGM})	●	–12	0	12	mV
$t_{CROWBAR(OVP\_DELAY)}$	CROWBAR Response Time	OVP_{GM} Driven from 650mV to 550mV	●		400	500	ns
$V_{CROWBAR(OH)}$	CROWBAR Output, Active High Voltage	OVP_{GM} Pulled to 0V and: $I_{CROWBAR}$ = –100µA, I_{INTVCC} = –20mA $I_{CROWBAR}$ = –4mA, I_{INTVCC} = –20mA	 ● ●	 4.3 4.2	 4.65 4.55	 5 4.9	 V V
$V_{CROWBAR(OL)}$	CROWBAR Output, Passive Low Voltage	$I_{CROWBAR}$ = 1µA	●		260	500	mV
$V_{CROWBAR(OVERSHOOT)}$	CROWBAR Peak Voltage Overshoot at V_{INL} Start-Up and Shutdown	V_{INL} Ramped Up from/Down to 0V	●		550	900	mV
$V_{CROWBAR(TH)}$	CROWBAR Latchoff Threshold	CROWBAR Ramped Up Until HYST Goes Logic Low	●	1.4	1.5	1.6	V
V_{TEMP}	TEMP Voltage	RUN = 0V, T_A = 25°C RUN = 0V, T_A = 125°C (See Figure 10 for Reference)		950	980 585	1010	mV mV
$OT_{TH(INCEPTION)}$	TEMP Overtemperature Inception Threshold	Ramping TEMP Downward Until HYST Outputs Logic Low	●	428	438	448	mV
$OT_{TH(RECOVER)}$	TEMP Overtemperature Recovery Threshold	Ramping TEMP Upward Until HYST Outputs Logic High	●	501	514	527	mV
$UVOV_{TH}$	UVLO/OVLO/IOVRETRY Undervoltage/Overvoltage Inception Thresholds	Ramping UVLO, OVLO or IOVRETRY Positive Until HYST Toggles Its State	●	488	500	512	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INH} = V_{INL} = 28V, per the typical application shown in Figure 45, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{UVOVD}	UVLO/OVLO/IOVRETRY/ TEMP Response Time	±50mV Overdrive (All Pins) ±5mV Overdrive, UVLO/OVLO/IOVRETRY Pins Only (Note 4)	● 	 50	25 125	100 500	µs µs
I_{UVOV}	Input Current of UVLO, OVLO and IOVRETRY	UVLO = 0.55V or OVLO = 0.45V or IOVRETRY = 0.45V	●			±30	nA
$V_{HOUSEKEEPING(UVLO)}$	Housekeeping Circuitry UVLO	Voltage on $INTV_{CC}$, $INTV_{CC}$ Rising (Note 4) Hysteresis, $INTV_{CC}$ Returning (Note 4)	 	1.9 5	2 25	2.1 50	V mV
$V_{HYST(SWITCHING\ ON)}$	HYST Voltage (M_{HYST} Off, RUN Logic High)	RUN Electrically Open Circuit RUN = 1.8V	● ●	4.9 1.85	5.1 2.1	5.25 2.35	V V
$V_{HYST(SWITCHING\ OFF,\ RUN)}$	HYST Voltage (M_{HYST} Off, RUN Logic Low)	RUN = 0V	●	170	350	480	mV
$V_{HYST(SWITCHING\ OFF,\ FAULT)}$	HYST Voltage, Switching Action Inhibited (M_{HYST} On)	UVLO < $UVOV_{TH}$ or OVLO > $UVOV_{TH}$ or IOVRETRY > $UVOV_{TH}$ or TEMP < $OT_{TH(INCEPTION)}$ or CROWBAR > $V_{CROWBAR(TH)}$ or DRV_{CC} < $DRVCC_{UVLO(FALLING)}$ (See Figures 62, 63)	●		30	65	mV
TMR_{UOTO}	Timeout and Power-On Reset Period	C_{TMR} = 1nF, Time from Fault Clearing to HYST Being Released by Internal Circuitry	●	5	9	14	ms
$V_{LATCH(IH)}$	$\overline{LATCH}$ Clear Threshold Input High		●	1.2			V
$V_{LATCH(IL)}$	$\overline{LATCH}$ Clear Threshold Input Low		●			0.8	V
$I_{\overline{LATCH}}$	$\overline{LATCH}$ Input Current	$V_{\overline{LATCH}}$ = 7.5V	●			±1	µA
$I_{TMR(UP)}$	TMR Pull-Up Current	V_{TMR} = 0V	●	–1.2	–2.1	–2.8	µA
$I_{TMR(DOWN)}$	TMR Pull-Down Current	V_{TMR} = 1.6V	●	1.2	2.1	2.8	µA
$V_{TMR(DIS)}$	Timer Disable Voltage	Referenced to $INTV_{CC}$	●	–180	–270		mV
$OTBH_{VIL}$	OTBH Low Level Input Voltage		●			0.4	V
$OTBH_{VZ}$	OTBH Pin Voltage When Left Electrically Open Circuit	–10µA ≤ I_{OTBH} ≤ 10µA	●	0.6	0.9	1.2	V
$I_{OTBH(MAX)}$	Maximum OTBH Current	OTBH Electrically Shorted to SGND	●			30	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

The LTM4641 SW absolute maximum rating of 40V is verified in ATE by regulating V_{OUT} while at $40V_{IN}$, in a controlled manner guaranteed to not affect device reliability or lifetime. Static testing of SW leakage current at $40V_{IN}$ is performed at control IC wafer level only.

Note 2: The LTM4641 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4641E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4641I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTM4641MP is tested and guaranteed over the full –55°C to 125°C operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

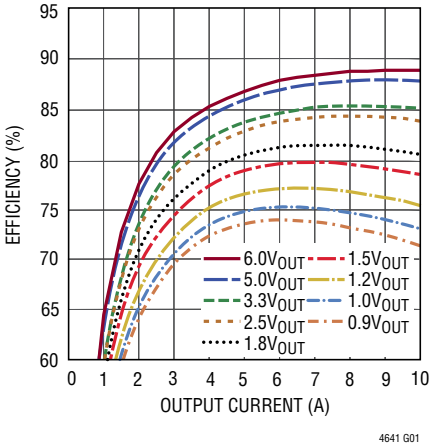
Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 4: 100% tested at wafer level only.

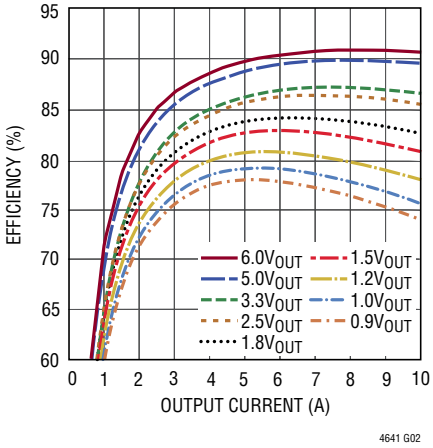
TYPICAL PERFORMANCE CHARACTERISTICS

(Figure 45 circuit with R_{fSET} per Table 1 and R_{SET1A}, R_{SET1B} and R_{SET2} per Table 2, unless otherwise noted)

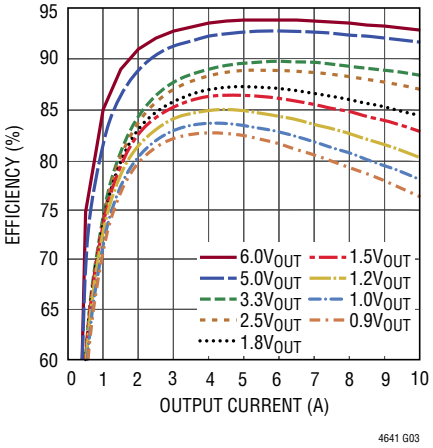
Efficiency vs Load Current at $36V_{IN}$



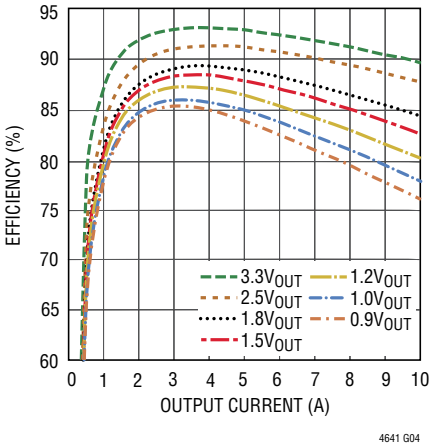
Efficiency vs Load Current at $24V_{IN}$



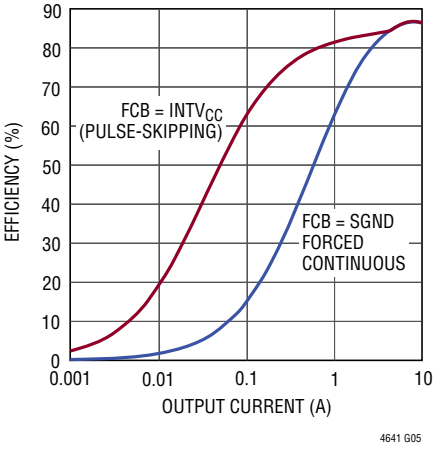
Efficiency vs Load Current at $12V_{IN}$



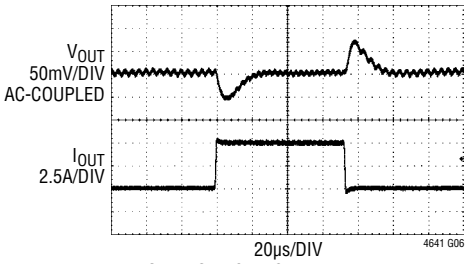
Efficiency vs Load Current at $6V_{IN}$



Pulse-Skipping vs Forced Continuous Mode Efficiency, $28V_{IN}$ to $3.3V_{OUT}$

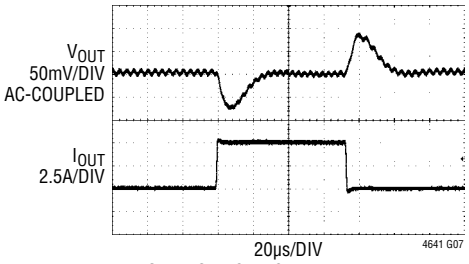


1V Transient Response, $38V_{IN}$



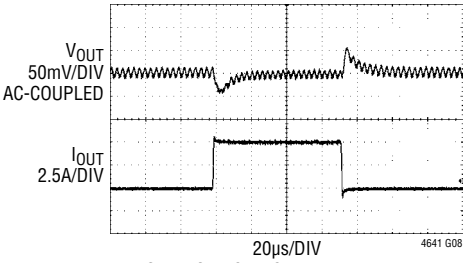
0A TO 5A LOAD STEPS AT 5A/µs
FRONT PAGE CIRCUIT WITH
OV_{PGM} = OPEN CIRCUIT

1V Transient Response, $4.5V_{IN}$



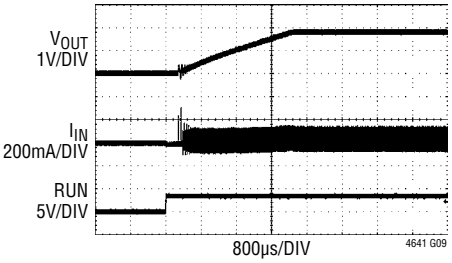
0A TO 5A LOAD STEPS AT 5A/µs
FRONT PAGE CIRCUIT WITH
OV_{PGM} = OPEN CIRCUIT

3.3V Transient Response, $28V_{IN}$ to $3.3V_{OUT}$



0A TO 5A LOAD STEPS AT 5A/µs
FIGURE 46 CIRCUIT

Output Start-Up, No Load

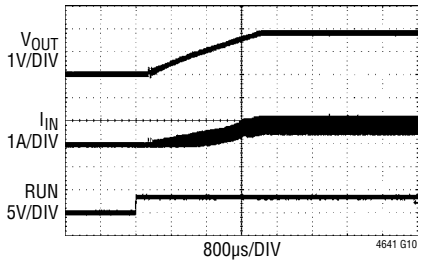


V_{IN} = 24V
$C_{IN(MLCC)} = 2 \times 10\mu F$ X7R

TYPICAL PERFORMANCE CHARACTERISTICS

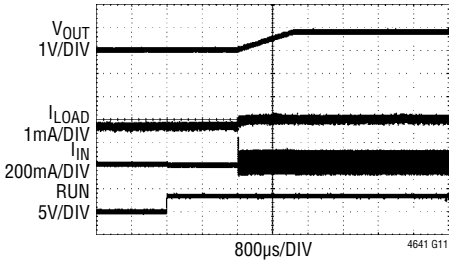
(Figure 45 circuit with R_{fSET} per Table 1 and R_{SET1A}, R_{SET1B} and R_{SET2} per Table 2, unless otherwise noted)

Output Start-Up, 10A Load



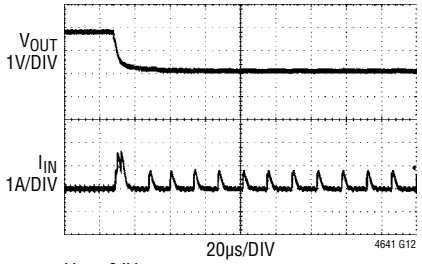
V_{IN} = 24V
$C_{IN(MLCC)}$ = 2 × 10µF X7R

Output Start-Up, Pre-Bias Condition



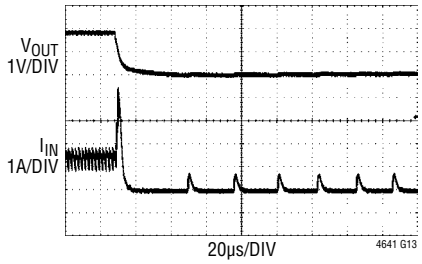
V_{IN} = 24V
$C_{IN(MLCC)}$ = 2 × 10µF X7R

Output Short-Circuit, No Initial Load



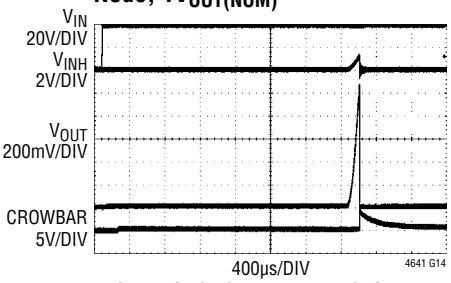
V_{IN} = 24V
$C_{IN(MLCC)}$ = 2 × 10µF X7R

Output Short-Circuit, 10A Initial Load



V_{IN} = 24V
$C_{IN(MLCC)}$ = 2 × 10µF X7R

Start-Up with V_{INH} Shorted to SW Node, $1V_{OUT(NOM)}$



FRONT PAGE CIRCUIT WITH V_{INH} SHORT CIRCUITED TO SW PRIOR TO POWER-UP. APPLYING UP TO $38V_{IN}$. NO LOAD

Start-Up with V_{INH} Shorted to SW Node, $3.3V_{OUT(NOM)}$

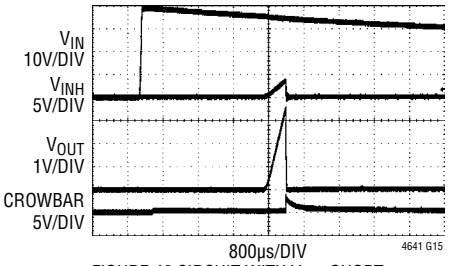


FIGURE 46 CIRCUIT WITH V_{INH} SHORT CIRCUITED TO SW PRIOR TO POWER-UP. APPLYING UP TO $38V_{IN}$. NO LOAD

Autonomous Restart with V_{INH} Shorted to SW Node, $3.3V_{OUT(NOM)}$

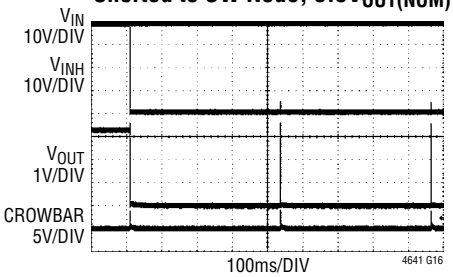
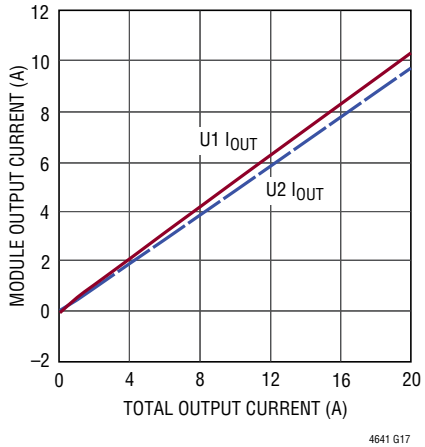
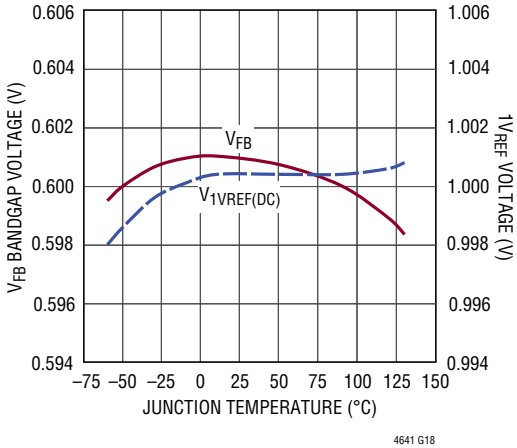


FIGURE 46 CIRCUIT, SHORT CIRCUITING V_{INH} TO SW IN SITU, OPERATING AT $38V_{IN}$ AND NO LOAD. $\overline{LATCH}$ CONNECTED TO $INTV_{CC}$ AND C_{TMR} = 47nF

Paralleled Modules, Current-Sharing Performance. cf. Figure 66 Circuit. $28V_{IN}$



Control IC Bandgap and $1V_{REF}$ Voltages vs Temperature. $28V_{IN}$



PIN FUNCTIONS

SGND (A1-A3; B1-B3; C1-C4; K1, K3; L3; M1-M3): Signal Ground Pins. This is the return ground path for all analog control and low power circuitry. SGND is tied to GND internal to the µModule regulator in a manner that promotes the best internal signal integrity—therefore, SGND should not be connected to GND in the user's PCB layout. See the Layout Checklist/Example section of the Applications Information section for more information pertaining to SGND and layout. All SGND pins are electrically connected to each other, internally.

HYST (A4): Input Undervoltage Hysteresis Programming Pin. Normally used as an output, but can be used as an input. If the LTM4641's inherent, default undervoltage lockout (UVLO) settings are satisfactory, $4.5V_{IN(RISING, MAX)}$ and $4V_{IN(FALLING, MAX)}$, HYST can be left electrically open circuit. See the Applications Information section to customize the LTM4641's UVLO thresholds.

HYST is a logic-high output with moderate pull-up strength that commands LTM4641's internal control IC to regulate the module's output voltage when conditions on the RUN, UVLO, OVLO, IOVRETRY, TEMP, CROWBAR, $INTV_{CC}$ and DRV_{CC} pins permit it (any recent latchoff events notwithstanding, otherwise OTBH and LATCH can also play a role). When a fault condition is detected, internal circuitry (M_{HYST}; see Figure 1) drives HYST logic low and the LTM4641's output is turned off. HYST can be used as a fault-indicator. See the Applications Information section.

HYST is pulled low when the RUN pin is pulled low, via an internal Schottky diode. HYST can be driven low by external open-collector/open-drain circuitry directly—as an alternate to the RUN pin interface. However, external circuitry should never drive HYST high, since doing so (indiscriminately) could cause thermal overstress to M_{HYST}, when M_{HYST} is on.

TEMP (A5): Power Stage Temperature Indicator and Overtemperature Detection Pin. When left electrically open circuit, TEMP's voltage varies according to an internal NTC (negative temperature coefficient) thermistor, residing in close proximity to LTM4641's power stage. When TEMP falls below 438mV (corresponding to a thermistor and power stage temperature of ~145°C), the LTM4641 pulls HYST low to inhibit regulation of its output voltage. HYST may be deasserted when TEMP subsequently exceeds 514mV (nominally corresponding to a cool-off hysteresis of ~10°C), depending on the OTBH setting. (See OTBH and the Applications Information section.)

To disable the µModule regulator's overtemperature shutdown feature, connect the TEMP and $1V_{REF}$ pins. The thermal shutdown inception threshold can also be modified, see the Applications Information section.

IOVRETRY (A6): Nonlatching Input Overvoltage Threshold Programming Pin. The LTM4641 pulls HYST low to inhibit regulation of its output voltage when IOVRETRY exceeds 0.5V. The LTM4641 can resume switching action when IOVRETRY is below 0.5V. If no nonlatching input overvoltage shutdown behavior is desired, connect this pin to SGND. Do not leave this pin open circuit.

GND (A7-A12; B6-B8, B11-B12; C7-C8; D6-D8; E1-E8; F1-F12; G1-G12; H3-H9, H11-H12; J5-J12; K5-K6, K11-K12; L4-L6; M4-M6): Power ground pins for input and output returns. See the Layout Checklist/Example section of the Applications Information section. All GND pins are electrically connected to each other, internally.

UVLO (B4): Input Undervoltage Lockout Programming Pin. The LTM4641 pulls HYST low to inhibit regulation of its output voltage whenever UVLO is less than 0.5V. The LTM4641 can resume switching action when UVLO exceeds 0.5V. Do not leave this pin open circuit.

If the LTM4641's default UVLO settings are used, $4.5V_{IN(RISING, MAX)}$ and $4V_{IN(FALLING, MAX)}$, then the UVLO pin should be electrically connected to $1V_{REF}$ or $INTV_{CC}$. Otherwise, see HYST and the Applications Information section for using a resistor-divider network to implement personalized UVLO rising and UVLO falling settings.

OVLO (B5): Input Overvoltage Latchoff Programming Pin. LTM4641 pulls HYST low to inhibit regulation of its output voltage when OVLO exceeds 0.5V. If OVLO subsequently falls below 0.5V, the module's output remains latched off; the LTM4641 cannot resume regulation of the output voltage until either the $\overline{LATCH}$ pin is toggled high or V_{INL} is power cycled. If input overvoltage latchoff behavior is not desired, electrically short this pin to SGND. Do not leave this pin open circuit.

PIN FUNCTIONS

CROWBAR (B9): Crowbar Output Pin. Normally logic low, with moderate pull-down strength to SGND.

When an output overvoltage (OOV) condition is detected, the LTM4641's fast OOV comparator pulls CROWBAR logic high through a series-connected internal diode. If utilizing LTM4641's OOV feature, CROWBAR should connect to the gate of a logic-level N-channel MOSFET configured to crowbar the module's output voltage (MCB, in Figure 1).

Furthermore, the LTM4641 latches off its output when CROWBAR nominally exceeds 1.5V and latches HYST logic low (see HYST).

If not using the OOV protection features of the LTM4641, leave CROWBAR electrically open circuit.

OV_{PGM} (B10): Output Overvoltage Threshold Programming Pin. The voltage on this pin sets the trip threshold for the inverting input pin of LTM4641's fast OOV comparator. When left electrically open circuit, resistors internal to the LTM4641 nominally bias OV_{PGM} to 666mV (OV_{PTH})—11% above the nominal V_{FB} feedback voltage (600mV) that the control loop strives to present to the noninverting input pin of LTM4641's fast OOV comparator. The aforementioned voltages correspond proportionally to the module's OOV inception threshold and V_{OUT}'s nominal voltage of regulation, respectively. Altering the OV_{PGM} voltage provides a means to adjust the OOV threshold; its DC-bias setpoint can be tightened with simple connections to external components (see the Applications Information section). Trace route lengths and widths to this sensitive analog node should be minimized. Minimize stray capacitance to this node unless altering the OOV threshold as described in the Applications Information section and Appendix F.

$\overline{LATCH}$ (C5): Latchoff Reset Pin. When a latchoff fault occurs, the LTM4641 turns off its output and latches M_{HYST} on to indicate a fault condition has occurred (see HYST). To configure the LTM4641 for latched off response to latchoff faults, connect $\overline{LATCH}$ to SGND. As long as $\overline{LATCH}$ is logic low, the LTM4641 will not unlatch. Regulation can be resumed by cycling V_{INL} or by toggling $\overline{LATCH}$ from logic low to high. It is also permissible to connect $\overline{LATCH}$ to $INTV_{CC}$; this configures the LTM4641 for autonomous restart with a timeout delay (programmed by C_{TMR}—see TMR).

If no latchoff faults are present when $\overline{LATCH}$ transitions from logic low to logic high, the LTM4641 immediately unlatches. If any latchoff fault is present when $\overline{LATCH}$ is logic high, a timeout delay timing requirement is imposed: the LTM4641 will not unlatch until all latchoff fault-monitoring pins meet operationally valid states for the full duration of the timeout delay. If $\overline{LATCH}$ becomes logic low before that timeout delay has expired, the LTM4641 remains latched off and the timeout delay is reset. Unlatching the LTM4641 can be reattempted by pulling $\overline{LATCH}$ logic high at a later time.

The following are latchoff fault conditions:

- CROWBAR activates (see CROWBAR)
- Input latchoff overvoltage fault (see OVLO)
- Latchoff overtemperature fault (when OTBH is logic low; see TEMP and OTBH)

$\overline{LATCH}$ is a high impedance input and must not be left electrically open circuit. $\overline{LATCH}$ can be driven by a µController in intelligent systems: a reasonable implementation for unlatching the LTM4641 is to pull $\overline{LATCH}$ logic high for the maximum anticipated timeout delay time—after which, HYST can be observed to indicate whether the LTM4641 has become unlatched.

$1V_{REF}$ (C6): Buffered 1V Reference Output Pin. Minimize capacitance on this pin, to assure the OV_{PGM} and TEMP pins are operational in a timely manner at power-up. $1V_{REF}$ should never be externally loaded except as explained in the Applications Information section.

V_{OUT} (C9-C12; D9-D12; E9-E12): Power Output Pins of the LTM4641 DC/DC Converter Power Stage. All V_{OUT} pins are electrically connected to each other, internally. Apply output load between these pins and the GND pins. It is recommended to place output decoupling capacitance directly between these pins and the GND pins. Review Table 9. See the Layout Checklist/Example section of the Applications Information section.

V_{ORB}^+ (D1): V_{OSNS}^+ Readback Pin. This pin connects to V_{OSNS}^+ internal to the µModule regulator. It is recommended to route this pin (differentially with V_{ORB}^-) to a test point so as to allow the user a way to confirm the integrity

PIN FUNCTIONS

of the remote-sense connections prior to powering up the LTM4641. V_{ORB}^+ can also be connected as a redundant feedback connection to V_{OSNS}^+ on the user's motherboard.

V_{ORB}^- (D2): V_{OSNS}^- Readback Pin. This pin connects to V_{OSNS}^- internal to the µModule regulator. It is recommended to route this pin (differentially with V_{ORB}^+) to a test point so as to allow the user a way to confirm the integrity of the remote-sense connections prior to powering up the LTM4641. V_{ORB}^- can also be connected as a redundant feedback connection to V_{OSNS}^- on the user's motherboard.

OTBH (D3): Overtemperature Behavior Programming Pin. When an overtemperature condition is detected (see TEMP), HYST pulls logic low to inhibit switching. If OTBH is connected to SGND, the LTM4641 latches HYST low. If OTBH is left floating, output voltage regulation can resume when the overtemperature event clears.

TMR (D4): Timeout Delay Timer and Power-On Reset (POR) Programming Pin. Connect a capacitor (C_{TMR}) from TMR to SGND to program the POR and timeout delay time of the LTM4641; 9ms delay time per nanofarad of capacitance. The minimum delay time is ~90µs, when TMR is left electrically open circuit. Even though they use the same capacitor, the power-on reset and timeout delay timers operate independently of each other. Any nonlatching fault or latching fault will reset the respective timer to the full delay time without impacting the other timer.

The timeout delay time programmed by a C_{TMR} capacitor can be negated by pulling TMR to $INTV_{CC}$.

RUN (D5): Run (On/Off) Control Pin. A RUN pin voltage below 0.8V will turn off the module. A voltage above 2V will command the module to turn on, if HYST is not asserted low by M_{HYST}. The LTM4641 contains a moderate (10k) pull-up resistor from HYST to $INTV_{CC}$, and a pull-up Schottky diode from RUN to HYST (see Figure 1). When RUN is pulled logic low, HYST is pulled logic low via the internal Schottky diode. RUN is compatible with direct-drive (totem-pole output drive) as well as open-collector/open-drain interfaces.

V_{OSNS}^+ (H1): Positive Input to the Remote Sense Differential Amplifier. This pin connects to the positive side of the output voltage remote sense point (V_{OUT} potential) via a resistor (R_{SET1A}). When regulating the output voltage, the LTM4641 control loop drives the differential voltage between V_{OSNS}^+ and V_{OSNS}^- to the lesser of TRACK/SS and 0.6V. V_{OSNS}^+ is connected to V_{ORB}^+ internal to the module (see V_{ORB}^+). A resistor may be needed from V_{OSNS}^+ to V_{OSNS}^- for some output voltage settings. (See the Applications Information section: Setting the Output Voltage.) Minimize stray capacitance to this pin to protect the integrity of the output voltage feedback signal.

V_{OSNS}^- (H2): Negative Input to the Remote Sense Differential Amplifier. This pin connects to the negative side of the output voltage remote sense point (GND potential) via a resistor (R_{SET1B}). When switching action is on, the LTM4641 control loop drives the differential voltage between V_{OSNS}^+ and V_{OSNS}^- to the lesser of TRACK/SS and 0.6V. V_{OSNS}^- is connected to V_{ORB}^- internal to the module (see V_{ORB}^-). A resistor may be needed from V_{OSNS}^+ to V_{OSNS}^- for some output voltage settings. (See the Applications Information section.) Minimize stray capacitance to this pin to protect the integrity of the output voltage feedback signal.

SW (H10): Switching Node of the Power Stage. Mainly used for testing purposes, however, one may optionally connect a snubber (series-configured capacitor C_{SW} and resistor R_{SW}) from SW to GND to reduce radiated EMI—in exchange for a minor compromise to power conversion efficiency. (See the Applications Information section.)

COMP (J1): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold of LTM4641's valley current mode control loop—and correspondingly, the commanded trough of the power inductor current—increases as this control voltage increases. It can be useful to make COMP available for observation on a PCB via or test pad with an oscilloscope probe. However, stray capacitance and trace lengths to this sensitive analog node should be minimized.

f_{SET} (J2): Switching Frequency Setting and Adjustment Pin. This pin interfaces directly to the I_{ON} pin of LTM4641's internal control IC. Current flow into the I_{ON} pin programs the on-time of the control loop's one-shot timer and power control MOSFET, M_{TOP}. Minimize stray capacitance and any tracelengths to this pin.

For applications requiring regulated output voltages of 3V or less at any time including during voltage rail tracking,

PIN FUNCTIONS

an on-time adjustment with a resistor to f_{SET} is required. Otherwise, f_{SET} can be left open circuit. See the Applications Information section for details.

V_{INL} (J3): Input Voltage Pin, Low Current for Power Control and Logic Bias. Feeds LTM4641's internal 5.3V LDO (see $INTV_{CC}$). Apply input voltage bias between this pin and GND. Decouple to GND with a capacitor (0.1µF to 1µF). This pin powers the heart of LTM4641's DC/DC controller and internal housekeeping ICs. V_{INL} bias current is within ~5mA of the sum of $INTV_{CC}$ and CROWBAR loading currents.

If using the advanced output overvoltage (OOV) protection features of the LTM4641, connect V_{INL} to either the drain of the external power-interrupt power MOSFET, identified on the front page schematic as MSP, or a separate input bias supply. If not making use of the advanced OOV protection features, V_{INL} and V_{INH} can connect directly to the same input power source.

LDO losses can be eliminated by connecting V_{INL}, $INTV_{CC}$, and DRV_{CC} if a low power auxiliary ~5V rail is available to power the resulting node. (See the Applications Information section, Figure 47 and Figure 49.)

DRV_{CC} (J4): Power MOSFET Driver Input Power Pin. DRV_{CC} is normally connected to $INTV_{CC}$. It must be kept within two diode drops (2 • V_{BE} or ~1.2V at 25°C) of $INTV_{CC}$. DRV_{CC} powers the internal MOSFET driver that interfaces to the switching MOSFETs (M_{TOP} and M_{BOT}) within LTM4641's power stage. It is pinned out separately from $INTV_{CC}$ to allow gate-driver current to be observed, and to allow an auxiliary ~5V to 6V bias supply to optionally provide the MOSFET driver bias current. The $INTV_{CC}$/DRV_{CC} pin pair can be biased from up to 6V (absolute maximum) from an external supply with 50mA peak sourcing capability, to reduce the LTM4641's $INTV_{CC}$ LDO losses (see Applications Information section and Figure 51). When DRV_{CC} is connected directly to $INTV_{CC}$, no bypass capacitance is needed except in rare applications where very fast output voltage ramp up is required (e.g., no soft-start capacitor on TRACK/SS, or rail-tracking rails with sub-60µs turn-on rise-time). Otherwise, ~2.2µF to 4.7µF X7R MLCC local bypassing to GND is recommended. Higher impedance sources may require higher bypass capacitance, to mitigate DRV_{CC} sag during V_{OUT} start-up.

An undervoltage lockout detector monitors DRV_{CC}. HYST is pulled low and switching action is inhibited if DRV_{CC} is less than 4.2V rising (maximum) and 3.5V falling (maximum).

FCB (K2): Forced Continuous/Pulse-Skipping Mode Operation Programming Pin. Connect this pin to SGND to force continuous mode operation of the synchronous power MOSFETs (M_{TOP} and M_{BOT}) at all output load conditions. Connect this pin to $INTV_{CC}$ to enable pulse-skipping mode operation: the freewheeling power switching MOSFET (M_{BOT}) is turned off of to prevent reverse flow of output current (I_{OUT}) at light loads. See Appendix E for more details. This is a high impedance input and must not be left electrically open circuit.

$INTV_{CC}$ (K4): Internal 5.3V LDO Output. LDO operates off of V_{INL}. The INTVCC rail biases low power control and housekeeping circuitry. $INTV_{CC}$ is usually connected to DRV_{CC} to power the MOSFET drivers interfacing to the switching power MOSFETs. No decoupling capacitance is needed on this pin unless it is being used to bias external circuitry (not common); do not apply more than 4.7µF (±20% tolerance) of external decoupling capacitance. The $INTV_{CC}$/DRV_{CC} pin pair can be overdriven by an external supply, from up to 6V (absolute maximum) with 50mA peak sourcing capability, to eliminate power losses otherwise incurred by the LTM4641's V_{INL}-to-$INTV_{CC}$ linear regulator (see the Applications Information section and Figure 51).

V_{INH} (K7-10; L7-12; M7-8, 11-12): Input Voltage Pin, High Current to the Power Converter Stage of the LTM4641. All V_{INH} pins are electrically connected to each other internally. Devote a large copper plane to connect as many of the V_{INH} pins to each other as is feasible. This will help form a low impedance electrical connection between the input source and the LTM4641's power stage. It will also provide a thermal path for removing heat from the BGA package and minimize junction temperature rise of the LTM4641 for a given application.

If utilizing the advanced output overvoltage (OOV) protection features of the LTM4641, connect V_{INH} to the source pin(s) of the external power-interrupt MOSFET, identified on the front page schematic as MSP, with a short wide trace, or preferably a small copper plane capable of adequately

PIN FUNCTIONS

handling the input current to LTM4641's power stage. *Do not* decouple the V_{INH} pins with any bypass capacitance in this case. Instead, place all decoupling capacitance directly between the drain of MSP to GND.

If not utilizing the advanced OOV protection features of the LTM4641, *do* decouple the V_{INH} pins to GND with local ceramic and bulk decoupling capacitance (see the Applications Information section).

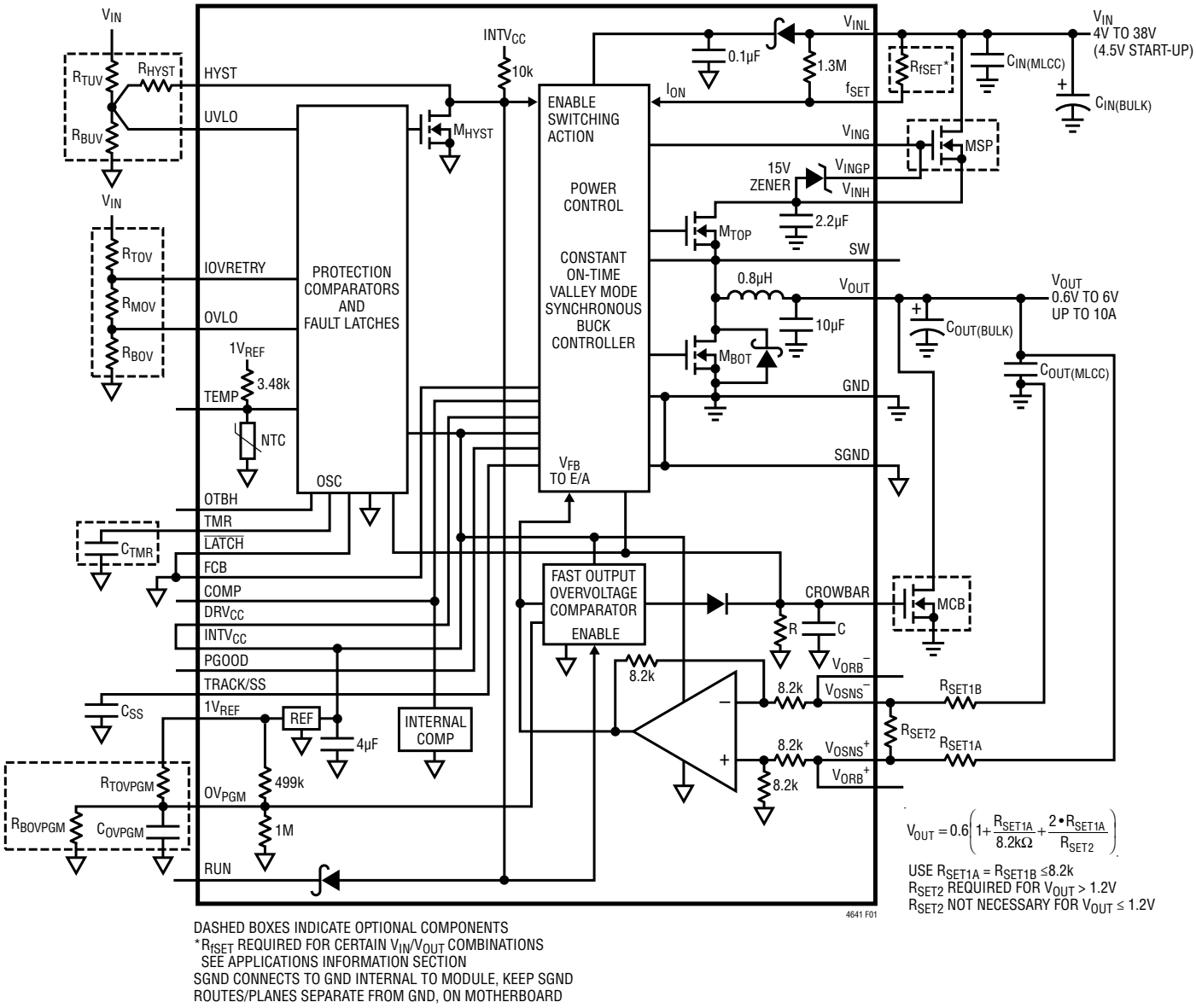
PGOOD (L1): Output Voltage Power Good Indicator. This is an open-drain logic output pin that is pulled to ground when the output voltage (and accordingly, the divided-down representation of the output voltage, V_{FB}, as presented to the control loop) is outside ±10% of the nominal target for regulation.

TRACK/SS (L2): Output Voltage Tracking and Soft-Start Programming Pin. This pin has a 1.0µA pull-up current source, typical. A capacitor can be placed from this pin to SGND to obtain an output voltage soft-start ramp-up rate whose turn-on time is 0.6ms per nanofarad of capacitance. Alternatively, when a voltage is applied to TRACK/SS through a resistor-divider network from another rail, the LTM4641 output is able to track the external voltage to satisfy coincident and ratiometric rail-voltage sequencing requirements. See the Applications Information section.

V_{ING} (M9): Gate Drive Output Pin. If utilizing the advanced output overvoltage (OOV) protection features of the LTM4641, connect V_{ING} to V_{INGP} and to the gate of the external power-interrupt N-channel MOSFET feeding V_{INH}, identified on the front page schematic as MSP; otherwise, leave this pin electrically open circuit.

V_{INGP} (M10): Gate Drive Protection Pin. If utilizing the advanced OOV protection features of the LTM4641, connect V_{INGP} to V_{ING} and to the gate of the external power-interrupt N-channel MOSFET feeding V_{INH}, MSP; otherwise, leave this pin electrically open circuit.

SIMPLIFIED BLOCK DIAGRAM



DASHED BOXES INDICATE OPTIONAL COMPONENTS
*R_{fSET} REQUIRED FOR CERTAIN V_{IN}/V_{OUT} COMBINATIONS
SEE APPLICATIONS INFORMATION SECTION
SGND CONNECTS TO GND INTERNAL TO MODULE, KEEP SGND ROUTES/PLANES SEPARATE FROM GND, ON MOTHERBOARD

Figure 1. Simplified Block Diagram. cf. Functional Block Diagram in Appendix A, Figure 62

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$C_{IN(MLCC)}$ + $C_{IN(BULK)}$	External Input Capacitor Requirement	I_{OUT} = 10A, 2 × 10µF or 4 × 4.7µF		20		µF
$C_{OUT(MLCC)}$ + $C_{OUT(BULK)}$	External Output Capacitor Requirement	I_{OUT} = 10A, 3 × 100µF or 6 × 47µF		300		µF

OPERATION

Introduction

The LTM4641 contains a buck-topology regulator employing a constant on-time current mode control scheme, including built-in power MOSFET devices with fast switching speed and a power inductor. In its most basic configuration (see Figure 45), the module operates as a standalone nonisolated switching mode DC/DC step-down power supply. It can provide up to 10A of output current with a few external input and output capacitors and output feedback resistors. The supported output voltage range is from 0.6V DC to 6V DC. The supported input voltage range is 4V to 38V, with a maximum start-up voltage of 4.5V (over temperature). Power conversion from lower input voltages can be realized if an auxiliary bias supply is available to power LTM4641's control and housekeeping bias input pin, V_{INL}. The LTM4641 Simplified Block Diagram is found in Figure 1. For a more detailed look, the Functional Block Diagram is found in Appendix A, Figure 62.

Motivation

Pulsed loading conditions and abnormal disturbances within the electrical systems found in industrial, vehicle, aeronautic, and military applications can induce wildly varying voltage transients (surges) on what is nominally a 24V DC to 28V DC distributed bus (28V DC bus). The duration of such disturbances can extend for periods of time between a millisecond to a minute in length, with excursions sometimes reaching (or exceeding) 40V and falling below 6V.

While switching buck regulators are of universal interest due to their compact size and ability to deliver DC/DC power conversion at high efficiency, FMEA (failure modes and effects analysis) leads one to believe that there is no way to reduce the severity rating and effects of an electrical short from the input source to the output load—however improbable. The LTM4641 challenges this notion by protecting the load from seeing excessive voltage stress, even when its high side switching MOSFET is short circuited.

Power µModule Regulator Reliability

First and foremost, Linear Technology µModule products adhere to rigorous testing and high reliability control, fabrication, and manufacturing processes—as is required of all its products. Furthermore, as part of its commitment to excellence, the Linear Technology Quality Control program periodically updates its Reliability Data report for LTM4600 series products to include cumulative data obtained from ongoing and routine in-house testing relating to operational life, highly accelerated stress, power and temperature cycling, thermal and mechanical shock, and much more. To view the latest report visit http://www.linear.com/docs/13557.

The LTM4641 easily supports high step-down ratios with few external components. The additional protection features when implemented provide an extra degree of insurance beyond other µModule regulators.

Overview

When configured as shown in Figure 46, the LTM4641 can regulate an output voltage between 0.6V and 6V from an input voltage between 4V and 38V ($4.5V_{IN}$ start-up, maximum).

If an optional N-channel power MOSFET, MSP, is placed between the input power source (V_{IN}) and the power stage input pins (V_{INH}), MSP's role becomes that of a resettable electronic power-interrupt switch. The gate of MSP is operated by V_{ING}, and its gate-to-source voltage is assured to be clamped by a built-in 15V Zener diode accessed via V_{INGP}. When switching action is engaged, V_{ING} charges the gate of MSP to nominally 10V above V_{INH} potential—suitable for driving a standard-logic MOSFET—and MSP becomes enhanced to pull V_{INH} up to the input source supply's electrical potential. The switching regulator steps down V_{INH} potential to V_{OUT} when MSP is on. When switching action is inhibited by pulling the RUN pin low or when a fault condition is detected by LTM4641's internal circuitry—such as an output overvoltage (OOV) condition—the gate of MSP is discharged and MSP turns off. The input source supply is thus disconnected from LTM4641's power stage input (V_{INH}).

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

The operation of MSP as a power interrupter provides a critical element of robust OOV protection: it removes a means for input power to flow through a damaged power stage to any precious loads on the output voltage rail, even when input power is cycled.

For even greater resilience to a short-circuit between V_{INH} and the SW switching node of the power stage, an external logic-level N-channel power MOSFET, MCB, is optionally placed—in a crowbar configuration—on the output of the power module. When an OOV condition is detected, CROWBAR turns on MCB (within 500ns, maximum) to discharge the output capacitors and transform any residual energy in LTM4641's power stage into a trivial amount of heat—energy which would otherwise have only served to inject charge into (further pump up the voltage on) the output capacitors, where precious loads reside.

The control and monitoring circuitry within the LTM4641 power module provide the following:

- Fast, accurate, latching output overvoltage detector (<500ns response time, <±12mv threshold error)
- N-channel output overvoltage crowbar power MOSFET drive
- Accurate (<±2.4%) nonlatching and resettable latching input overvoltage shutdown thresholds
- N-channel overvoltage power-interrupt MOSFET drive
- Accurate (<±2.4%) Input UVLO rising and UVLO falling thresholds
- Built-in and adjustable overtemperature shutdown protection, programmable for resettable latching or nonlatching (hysteretic restart) response
- Analog temperature indicator output pin
- Adjustable power-on reset and timeout delay time
- Latchoff behavior that can be altered to instead provide autonomous restart after timeout delay time expires
- Parallelable for higher output power
- Differential remote sensing of POL voltage
- Internal loop compensation
- Output current foldback protection
- Selectable pulse-skipping mode operation
- Output voltage soft-start and rail tracking
- Power-up into pre-biased conditions without sinking current from the output capacitors
- Adjustable switching frequency
- Power good indicator
- RUN enable pin

Novel and simple circuit implementations with LTM4641 and a few external components enable surge ride-through protection and overtemperature detection of a power-interrupt MOSFET. (See Figure 47, for example.) The aforementioned features enabled by LTM4641 are grouped by function and described in the remainder of the Applications Information section.

Power (V_{INH}) and Bias (V_{INL}) Input Pins

LTM4641's power stage (V_{INH}) and control bias (V_{INL}) input pins are brought out separately to allow freedom for implementing more sophisticated system configurations, such as: fully utilizing LTM4641's advanced output overvoltage (OOV) protection features to protect the load (e.g., front page schematic or Figure 46); providing rudimentary input surge ride-through protection (Figure 47); performing DC/DC down conversion from a power rail below LTM4641's inherent UVLO thresholds (from a 3.3V bus in Figure 49).

If V_{INH} and V_{INL} are powered from separate rails, it is recommended to power up V_{INL} prior to or concurrently with V_{INH}. V_{INL} should have a final value of at minimum 3.5V within 2ms of V_{INH} exceeding 3.5V. The recommendation to sequence V_{INL} ahead of or closely with V_{INH} is not related at all to module device reliability but stems rather from a desire to assure that the control section of LTM4641 drives the MOSFETs in LTM4641's power stage deterministically whenever any appreciable V_{INH} voltage is present. It is always permissible for V_{INL} voltage to be present—regardless of the state of V_{INH}—however, realize that there is no UVLO detection on V_{INH}.

To prevent the control section from trying to regulate through a dropout condition or commencing switching activity in the absence of V_{INH} potential, it is recommended

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

to implement a custom UVLO falling setting above the dropout curve in Figure 4 (see also Figure 11).

LT3010-5 is shown in Figure 47 to provide bias for V_{INL}, to enable ride-through of 80V transients on V_{IN}. UVLO detection of V_{IN} is realized in this example by D2 creating a discharge path for V_{INL} in the event of loss of V_{IN}.

V_{INH} and V_{INL} have no specific power-down sequencing requirement, only that V_{INL} should stay above 3.5V whenever V_{INH} is above 3.5V.

V_{INL} and V_{INH} sequencing is inherently addressed by the LTM4641 in the Figure 45 and Figure 46 circuits.

The V_{IN} and V_{INL} start-up and shutdown waveforms of the Figure 47 circuit—but with 1Ω output load and TMR tied to $INTV_{CC}$—are shown in Figure 2. The effect of the timing capacitor, C_{TMR}, that normally generates a power-on reset (POR) delay at start-up is negated by tying TMR to $INTV_{CC}$. The ~3ms V_{IN}-to-V_{OUT} start-up delay time seen in Figure 2 is due to POR of the LTM4641's fault-monitoring circuitry and soft-start ramp (C_{SS}).

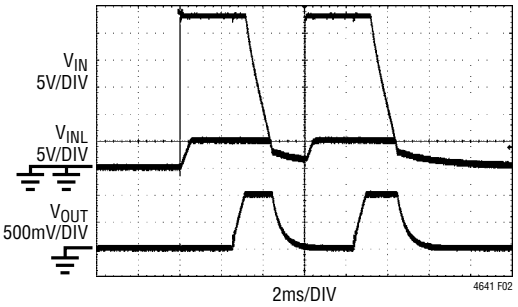


Figure 2. Start-Up and Shutdown Waveforms of Figure 47 Circuit. TMR Tied to $INTV_{CC}$ to Highlight V_{IN} and V_{INL} Sequencing without POR Delay. 1Ω Load

Switching Frequency (On Time) Selection and Voltage Dropout Criteria (Achievable V_{IN}-to-V_{OUT} Step-Down Ratios)

The LTM4641 controller employs a current mode constant on-time architecture, in which the COMP voltage corresponds to the trough inductor current at which the internal high side power MOSFET (M_{TOP}) is commanded on by the control loop—for a duration of time proportional to controller's I_{ON} pin current (Refer to Figure 1). Regulation is maintained by a pulsed frequency modulation (PFM) scheme. During a load transient step-up, the control loop will command a higher inductor trough current to compensate for a deficiency in output voltage; the effective switching frequency will increase until the output voltage returns to normal (an overcurrent event, notwithstanding). During a load transient step-down, the control loop will command a lower inductor trough current to compensate for an excess of output voltage; the effective switching frequency will decrease until the output voltage returns to normal. The control loop perceives inductor current-sense information via the voltage signal that appears across the synchronous power MOSFET, M_{BOT}, when M_{BOT} is on (this is commonly referred to in the industry as $R_{DS(ON)}$ current sensing).

The on-time of the one-shot timer—and hence the power control MOSFET, M_{TOP},—is given, in units of seconds, by:

$$t_{ON} = \frac{0.7V \bullet 10pF}{I_{ION}} \quad (1)$$

where I_{ION} is in units of amperes. For output voltages greater than 3V, and for non-rail-tracking applications, no external R_{fSET} resistor is needed, and the I_{ION} current (units: amperes) is set solely by the V_{INL} voltage (units: volts) and the internal 1.3MΩ V_{INL}-to-f_{SET} resistor:

$$I_{ION} = \frac{V_{INL}}{1.3M\Omega} \quad (2)$$

The switching frequency of operation of the LTM4641's buck converter power stage at full load in this scenario is given, in Hz, by:

$$f_{SW} = \frac{V_{OUT}}{0.7V \bullet 1.3M\Omega \bullet 10pF} \quad (3)$$

where V_{OUT} is the desired nominal output voltage, in units of volts.

An external R_{fSET} resistor can be applied when setting V_{OUT} greater than 3V, if desired, to obtain increased switching frequency. Usually, increasing switching frequency comes from a desire to reduce output voltage ripple and/or output capacitance requirement—but at a moderate penalty to DC/DC conversion efficiency. There are some limitations to how low an R_{fSET} value can be applied in practice due

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

to non-zero minimum off-time, dropout voltage, and maximum achievable switching frequency of operation.

When an R_{fSET} resistor external to the LTM4641 is connected between V_{INL} and f_{SET} to decrease the default on-time setting, the total I_{ON} current (units: amperes) is given by:

$$I_{ION} = \frac{V_{INL}}{1.3M\Omega} + \frac{V_{INL}}{R_{fSET}} = \frac{V_{INL}}{1.3M\Omega \,||\, R_{fSET}} \quad (4)$$

where V_{INL} is in units of volts and R_{fSET} is in units of ohms. R_{fSET} is needed for output voltage settings less than or equal to $3V_{OUT}$, and for rail-tracking applications.

The minimum on-time the LTM4641 supports is 43ns, typical, but guard banded conservatively to 75ns, maximum. Therefore, for a conservative design, t_{ON} should be larger than 75ns, typical. From Equation 1, it follows that I_{ION} should be designed to be less than 93.3µA.

When an external R_{fSET} resistor is applied between V_{INL} and R_{fSET} (and V_{INL} and V_{INH} are operating from the same rail—Figure 45 and Figure 46), the switching frequency of operation of the power stage at full load, in Hz, is given by:

$$f_{SW} = \frac{V_{OUT}}{0.7V \bullet (1.3M\Omega \,||\, R_{fSET}) \bullet 10pF} \quad (5)$$

where R_{fSET} is in ohms, and V_{OUT} is the desired nominal output voltage, in units of volts.

In the general case, the switching frequency of the buck converter power stage at full load is given, in Hz, by:

$$f_{SW} = \frac{V_{OUT}}{V_{INH} \bullet t_{ON}} = \frac{V_{OUT} \bullet I_{ION}}{V_{INH} \bullet 0.7V \bullet 10pF} \quad (6)$$

See Appendix C for a detailed discussion on the following topics:

- Why should the switching controller be operated at a higher switching frequency (i.e., programmed for a shorter on-time with R_{fSET}) than that yielded by the internal 1.3MΩ V_{INL}-to-f_{SET} resistor alone…

  …for nominal output voltages of 3V and less?

  …in rail-tracking applications?

- When V_{INL} and V_{INH} are operated from separate supplies…

  … why should R_{fSET} ordinarily connect to the V_{IN} power source rather than V_{INH} (Figure 49)?

  …when is it okay for R_{fSET} to connect to V_{INH} (Figure 47)?

For application circuits of the form found in Figure 45, Figure 46, Figure 47 and Figure 51: see Figure 3 for the maximum recommended value of R_{fSET} as a function of nominal target output voltage, and resulting full-load switching frequency corresponding to those R_{fSET} values.

Figure 3 can also be interpreted to provide the lowest recommended switching frequency for a given target output voltage. Table 1 summarizes nominal values of R_{fSET} endorsed for some popular output voltages; use of commonly available ±5% tolerance resistors or better with ±100ppm/°C temperature coefficient or better is recommended.

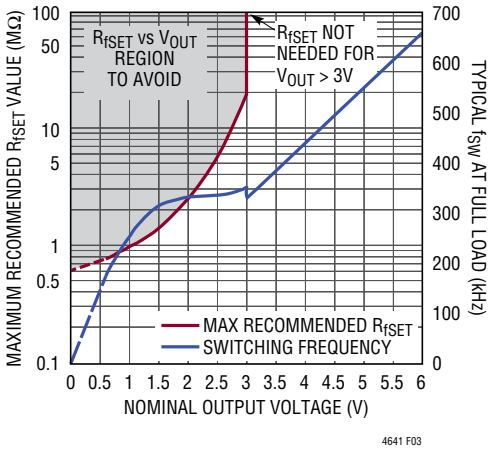


Figure 3. Maximum Recommended R_{fSET} (Nominal Values) for Non-Tracking Applications, and Resulting Full-Load Operating Switching Frequency vs Nominal Output Voltage

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

Table 1. Endorsed R_{fSET} Resistor Value vs Output Voltage for Non-Tracking Applications—and Resulting Full-Load Switching Frequency (cf. Figure 45, Figure 46, Figure 47, and Figure 51 Circuits)

$V_{OUT(NOM)}$ (V)	R_{fSET} (MΩ) (Nearest EIA-Standard Values)	f_{SW} (kHz)
0.6	0.787	175
0.7	0.825	200
0.8	0.887	215
0.9	0.931	235
1.0	1.00	255
1.2	1.13	285
1.5	1.43	315
1.8	2.00	325
2.0	2.55	330
2.5	5.76	335
Greater Than 3.0	∞ (Not Used)	See Figure 2
3.3	∞ (Not Used)	360
5.0	∞ (Not Used)	550
6.0	∞ (Not Used)	660

In rail-tracking applications, it is recommended to use the R_{fSET} value corresponding to the lowest voltage needed to be regulated during output voltage ramp down. For example: to ramp V_{OUT} down to 0.5V requires R_{fSET} to be not more than 750kΩ (nominal) per Figure 3.

It is often permissible to use lower R_{fSET} values than those indicated in Figure 3 and Table 1 if, for example, lower output ripple voltage and/or a lower output capacitance is desired. However, be aware of three guiding principles:

I. Minimum On-Time. Ensure $I_{ION} < 93.3\mu A$. See Equations 1 and 4.

II. Minimum Off-Time and Dropout Operation. The minimum off-time, $t_{OFF(MIN)}$, is the shortest time required for the LTM4641 to perform the following tasks: turn on its power synchronous MOSFET (M_{BOT}), trip the control loop's current comparator, and turn off M_{BOT}. The minimum input voltage on V_{INH}, in volts, that one can regulate the output at and still avoid dropout is given by:

$$V_{IN(DROPOUT)} = V_{OUT} \bullet \left(1 + \frac{t_{OFF(MIN)}}{t_{ON}}\right) + R_{PS} \bullet I_{OUT} \quad (7)$$

where:

- V_{OUT} is nominal output voltage in volts.
- $t_{OFF(MIN)}$ is the minimum length of time M_{BOT} can be on, after M_{TOP} turns off. For a conservative design, use a value of 300ns, taken from the Electrical Characteristics Table.
- t_{ON} is the on-time of the power control MOSFET, M_{TOP}, as programmed by the current flowing into the I_{ON} pin of LTM4641's internal control IC.
- R_{PS} is the series resistance of the module's power stage, from V_{INH} to V_{OUT}. For $V_{IN} \geq 6V$, this is less than 50mΩ, even at extreme temperatures ($T_J \approx 125°C$). For $V_{IN} < 6V$, the effective series resistance increases due to drop in $INTV_{CC}$ voltage and corresponding decreased gate-drive enhancement of M_{TOP}. Printed circuit board (PCB) and/or cable resistance present in the copper planes and/or wires that physically connect the output of the module to the load adds to R_{PS}'s effective value.
- I_{OUT} is the load current on V_{OUT} in amperes.

For applications of the form shown in Figure 45, Figure 46 and Figure 47: the minimum allowable V_{INH} voltage of operation to avoid dropout for $3V < V_{OUT} \leq 6V$ is shown in Figure 4. The curves are a result of realizing that $V_{IN(DROPOUT)}$ equals V_{INH} (neglecting MSP voltage drop) when dropout actually occurs, and that Equations 1 and 2 yield an expression for t_{ON} as a function of V_{INH}. M_{TOP} will be less fully enhanced during its on-time if DRV_{CC} is less than its nominal value of 5.3V (for example, when $V_{INL} < 6V$ and when DRV_{CC} bias is provided by $INTV_{CC}$). DRV_{CC}'s effect on R_{PS} at low line is illustrated in Figure 4.

III. Maximum Attainable f_{SW}. The maximum attainable switching frequency of operation (in units of Hz) for a given on-time (t_{ON}, in seconds) is governed simply by:

$$f_{MAX} = \frac{1}{t_{ON} + t_{OFF(MIN)}} \quad (8)$$

where a conservative value of 300ns can be used for $t_{OFF(MIN)}$.

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

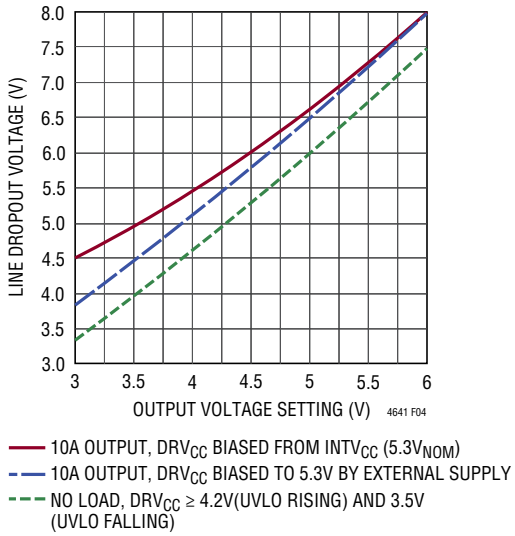


Figure 4. Line Dropout Voltage vs Output Voltage at No Load and Full Load. Figure 45, Figure 46 and Figure 47 Circuit Applications. R_{fSET} = Open and R_{SET1A}, R_{SET1B}, R_{SET2} Values Setting V_{OUT} for Regulation at or Above 3V

Given that the PFM control scheme increases switching frequency (to as high as f_{MAX}) to maintain regulation during a transient load step-up, the design guidance is: set the steady-state operating frequency f_{SW} to be less than f_{MAX}. Furthermore, when the LTM4641 is in dropout operation, the switching frequency of the converter *is* f_{MAX}.

It is best to avoid operation in dropout scenarios, because the control loop will rail COMP high to command M_{TOP} at highest possible duty cycle. If input voltage "snaps upwards" at a sufficiently high slew rate when COMP has railed, the control loop may be unable provide satisfactory line rejection.

See Figure 11 to set the UVLO falling response of LTM4641 above the computed $V_{IN(DROPOUT)}$ voltage; this will inhibit switching action for $V_{IN} < V_{IN(DROPOUT)}$. Input voltage ripple, and any line sag between the input source supply and the V_{INH} pins—and voltage drop across the power interrupt MOSFET, MSP, if used—must be taken into account by the system designer.

Setting the Output Voltage; the Differential Remote Sense Amplifier

A built-in differential remote-sense amplifier enables precision regulation at the point-of-load (POL), compensating for any voltage drops in the system's output distribution path: the total variation of LTM4641's output DC voltage over line, load, and temperature is better than ±1.5%.

The basic feedback connection between the POL and the module's feedback sense pins is shown in Figure 5.

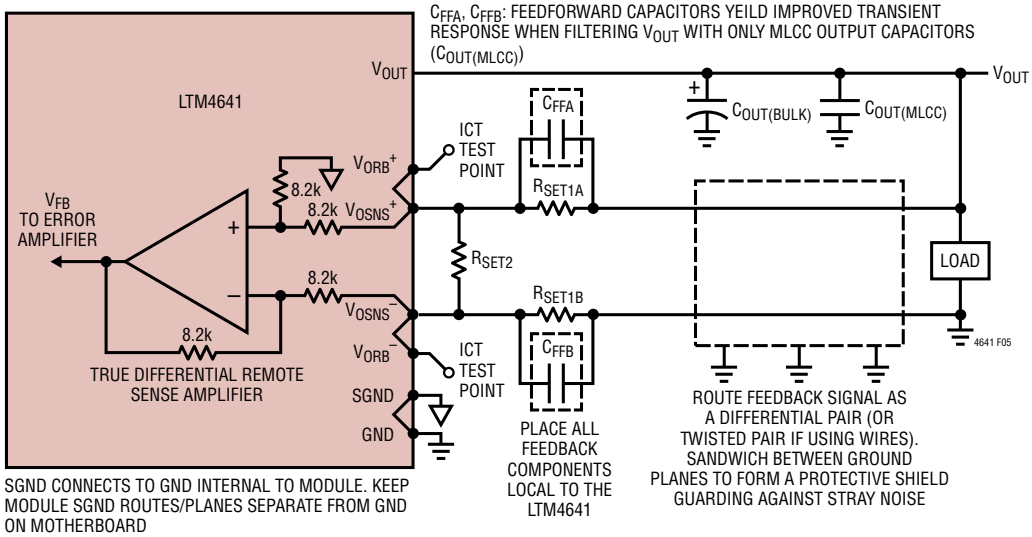


Figure 5. Basic Feedback Remote Sense Connections and Techniques; Setting the Output Voltage

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

The output voltage at the POL is differentially sensed via a symmetrical impedance-divider network. In Figure 1 and Figure 5, it is seen that the control loop regulates the output voltage such that the differential V_{OSNS}^+-to-V_{OSNS}^- feedback signal voltage is the lesser of the TRACK/SS pin voltage or the regulator's nominal bandgap voltage of 600mV. The arrangement and values of the resistors in the symmetrical impedance-divider network set the output voltage.

The remote sense pins (V_{OSNS}^+, V_{OSNS}^-) have redundant connections internal to the module to readback pins (V_{ORB}^+, V_{ORB}^-). The readback pins provide a means to verify the integrity of the feedback signal connection during motherboard ICT (in circuit test). The importance of verifying the integrity of the connection of the feedback signal to the output voltage prior to powering up the input voltage cannot be understated. If one or both feedback pins are left electrically floating due to manufacturing assembly defect, for example, or if the remote-sense pins are short circuited to each other, the control loop and overvoltage-detector circuitry have no awareness of the actual output voltage condition. A compromised feedback connection presents a very real danger of (1) the control loop commanding on M_{TOP} at the highest possible duty cycle—due to the lack of negative feedback—and (2) the LTM4641's protection circuitry being unaware of any issue. In a production environment, modern day ICT can easily catch any such stuffing or assembly errors; in a lab or prototyping environment, an ohmmeter can do the job.

For many applications that use a mixture of MLCC and bulk (low ESR tantalum or polymer) output capacitors, the symmetrical impedance-divider network that feeds back the POL's voltage to the module need only be constructed with resistors R_{SET1A} and R_{SET1B}, for output voltages of $1.2V_{OUT}$ and lower. R_{SET2} must be present for output voltages in excess of $1.2V_{OUT}$. R_{SET1A} and R_{SET1B} should always have the same nominal value. Applications with MLCC-only output capacitors (see Output Capacitors and Loop Stability in following pages) will demonstrate improved transient response when feedforward capacitors C_{FFA} and C_{FFB}, nominally equal in value, are installed electrically in parallel with R_{SET1A} and R_{SET1B}, respectively.

Use of 0.1% tolerance resistors (or better) for R_{SET1A}, R_{SET1B}, and R_{SET2} are recommended—with temperature coefficients of resistance suitable for one's operating range of PCB temperature—to assure that output voltage error introduced by resistor value variation is acceptable for the application. SMT resistors with T.C.R.s of ±25ppm/°C and better are readily available in the marketplace.

For output voltage settings less than or equal to $1.2V_{OUT}$, R_{SET2} is not needed, and R_{SET1A} and R_{SET1B} are given by:

$$R_{SET1A} = R_{SET1B} = \left(\frac{V_{OUT}}{0.6V} - 1\right) \bullet 8.2k\Omega \quad (9)$$

For output voltages above $1.2V_{OUT}$, R_{SET1A} (and R_{SET1B}) should be set equal to 8.2kΩ (or less, if 8.2kΩ is not a convenient value for the user), and R_{SET2} is then given by:

$$R_{SET2} = \frac{2 \bullet R_{SET1A}}{\frac{V_{OUT}}{0.6} - \frac{R_{SET1A}}{8.2k\Omega} - 1} \quad (10)$$

It is always permissible to select a value for R_{SET1A} (and R_{SET1B}) less than that given by Equation 9—and then calculate a valid value for R_{SET2} from Equation 10—as long as R_{SET1A} and R_{SET1B} are designed to withstand the higher resulting power dissipation.

When V_{OUT} is in regulation, the voltages at V_{OSNS}^+ and V_{OSNS}^- are given by:

$$V_{VOSNS}^+ = \left(\frac{0.6V}{(8.2k\Omega \,||\, R_{SET1A} \,||\, R_{SET2})} + \frac{\Delta V_{GND}}{R_{SET1A}}\right) \bullet (R_{SET1A} \,||\, 16.4k\Omega) \quad (11)$$

and

$$V_{VOSNS}^- = V_{VOSNS}^+ - 0.6V \quad (12)$$

respectively. ΔV_{GND} is the voltage drop between ground at the POL and LTM4641's SGND pins in volts. This voltage drop is usually entirely a result of I • R drop in the output distribution path—largest when maximum load current is being drawn:

$$\Delta V_{GND} = V_{GND(POL)} - V_{SGND(LTM4641)} \quad (13)$$

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

With R_{SET1A}, R_{SET1B}, and R_{SET2} determined, double-check the output voltage setting with:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_{SET1A}}{8.2k\Omega} + \frac{2 \bullet R_{SET1A}}{R_{SET2}}\right) \quad (14)$$

Some recommended values for R_{SET1A}, R_{SET1B}, and R_{SET2} for popular output voltages are shown in Table 2.

Table 2. Recommended R_{SET1A}, R_{SET1B} and R_{SET2} Values for Some Popular Output Voltages, cf. Figure 5 Feedback Connections.

V_{OUT}	R_{SET1A}, R_{SET1B}	R_{SET2}
0.6V	0Ω	∞ (Not Used)
0.7V	1.37kΩ	∞ (Not Used)
0.8V	2.74kΩ	∞ (Not Used)
0.9V	4.12kΩ	∞ (Not Used)
1.0V	5.49kΩ	∞ (Not Used)
1.2V	8.2kΩ	∞ (Not Used)
1.5V	8.2kΩ	33.2kΩ
1.8V	8.2kΩ	16.5kΩ
2.0V	8.2kΩ	12.4kΩ
2.5V	8.2kΩ	7.5kΩ
3.3V	8.2kΩ	4.7kΩ
5.0V	8.2kΩ	2.61kΩ
6.0V	8.2kΩ	2.05kΩ

See Appendix D for a detailed discussion on the following topics:

- What is the rationale for using a symmetrical resistor network?
- What should I do if I cannot shield the differential sense feedback lines with GND? (I anticipate differential mode noise in the feedback signal?)
- What should I do if the module and the load(s) are separated by a significant distance (~50cm or more), or if the load current flows through a cable assembly or power connector? (I anticipate common mode noise in the feedback signal?)

Input Capacitors

The LTM4641 module should be connected to a low AC impedance, nominally DC output voltage source. MLCC input bypass capacitors must be provided externally, as close in proximity to the module as possible (see Figure 43). If external MOSFET MSP is not used (Figure 45), two 10µF or four 4.7µF ceramic capacitors should be electrically connected directly between the V_{INH} and GND pins. If MSP is used (Figure 46, Figure 47 and Figure 49), then MSP must be placed as close to the LTM4641's V_{INH} pins as possible, and two 10µF or four 4.7µF ceramic capacitors should be electrically connected directly between the drain of MSP and GND (see Figure 44). A 47µF to 100µF surface mount bulk capacitor can be used to supplement input power bypassing, and can share the burden of any local ceramic capacitors in filtering the power stage's ripple current. If low impedance power planes are used to bring V_{IN} to the vicinity of the module, input source impedance will be low enough that bulk capacitors will not be needed. A localized bulk input capacitor is needed when an underdamped LC-resonant tank is formed by routing long input leads or traces (low ESR inductance) bypassed only with MLCCs (ultralow ESR capacitance).

Neglecting the inductor peak-to-peak current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1-D)} \quad (15)$$

where η is the power conversion efficiency of the LTM4641 module and D is the duty cycle on-time of M_{TOP}. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or a polymer capacitor.

For a buck converter, the switching duty cycle of M_{TOP} can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (16)$$

Output Capacitors and Loop Stability/Loop Compensation

The current mode constant on-time architecture enables very high step-down input-to-output ratios with compelling transient response. It also enables cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. The LTM4641 is internally compensated to yield stability over all operating conditions.

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The output capacitors $C_{OUT(BULK)}$ and $C_{OUT(MLCC)}$ must be chosen with low enough effective series resistance (ESR) to meet the output voltage ripple requirements and provide localized bypassing for the load. Although the LTM4641 provides fast transient response, the output voltage at the POL is reliant on nearby charge stored in a reservoir of ceramic capacitors $C_{OUT(MLCC)}$ to minimize sag and overshoot in the initial microseconds of a high dI/dt transient load step-up and step-down, respectively. If used, $C_{OUT(BULK)}$ can be comprised of low ESR tantalum or low ESR polymer capacitor(s); these capacitors then serve as a local reservoir to replenish the MLCCs during transient load events. It is also possible to use $C_{OUT(MLCC)}$ only, however, the use of feedforward capacitors, C_{FF}, should then be installed in the remote-sense feedback path, to obtain an optimized transient response (see Figure 5 feedback connections).

The $C_{OUT(MLCC)}$ ceramic capacitors should be at least X5R-type material. X5R-type and X7R-type MLCCs are recommended when operating PCB temperatures are not more than 85°C and 125°C, respectively. Both materials are renown in the industry for having a relatively low capacitance change over their respective temperature range of operation (±15%). However, X5R and X7R MLCCs do exhibit significant loss of capacitance with applied DC voltage and are subject to aging effects, and this must be taken into account in any system design. Refer to the capacitor manufacturer's specifications for details.

The typical output capacitance range is between 200µF to 800µF. The system designer should use discretion in determining whether additional output filtering may be needed, if further reduction of output ripple—or output voltage deviation during dynamic load or line transient events—is required.

In Table 9, guidelines are provided for output capacitor selection, for various operating conditions. The table optimizes total equivalent ESR and total bulk capacitance for the transient load step performance. Stability criteria is considered. The Linear Technology LTpowerCAD™ design tool is available for transient simulation and stability analysis, if desired.

Pulse-Skipping Mode vs Forced Continuous Mode

In applications where high DC/DC conversion efficiency at light-load currents is highly desired—when the input voltage source is a battery, for example—pulse-skipping mode operation should be employed. Pulse-skipping mode operation prevents power flow from the output capacitors to the input source. Be aware, however, due to M_{BOT}'s resulting asynchronous operation at light load, applications employing pulse-skipping mode may necessitate more output capacitance and/or a higher OV_{PGM} setting than operation in forced continuous mode would.

Pulse-skipping mode is activated by connecting FCB to $INTV_{CC}$. Forced continuous operation is activated by connecting FCB to SGND.

Be aware that in pulse-skipping mode and ultralight loads (say, less than 20mA out), the V_{ING} voltage may appear as a sawtooth waveform as a result of being charge-pumped at a slower rate, to conserve energy.

See Appendix E for more information on how pulse-skipping mode works.

Soft-Start, Rail-Tracking and Start-Up Into Pre-Bias

The TRACK/SS pin can be used to either soft-start the output of the LTM4641 regulator, or make LTM4641's output voltage track another rail coincidentally or ratiometrically. When RUN or HYST is low, the TRACK/SS pin is discharged. When RUN and HYST are released, TRACK/SS sources a microamp of current.

When a soft-start capacitor, C_{SS}, is applied to the pin, the current source is responsible for generating an output voltage turn-on time of 0.6ms per nanofarad of capacitance. The power stage is high impedance (M_{TOP} and M_{BOT} are off) until the TRACK/SS pin voltage exceeds V_{FB}, the remote-sense differential amplifier's output voltage. This allows power-up into pre-biased output voltage conditions without sinking of current from the output capacitors. When TRACK/SS exceeds the control IC's 600mV bandgap voltage, V_{FB} is regulated at 600mV and V_{OUT} reaches its nominal output voltage.

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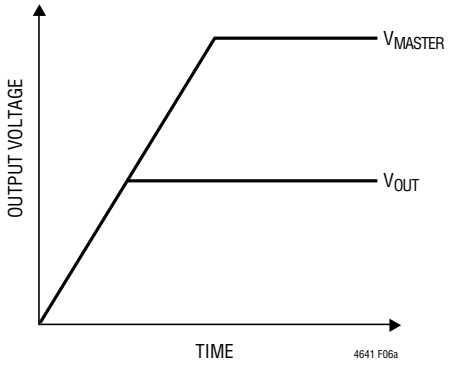
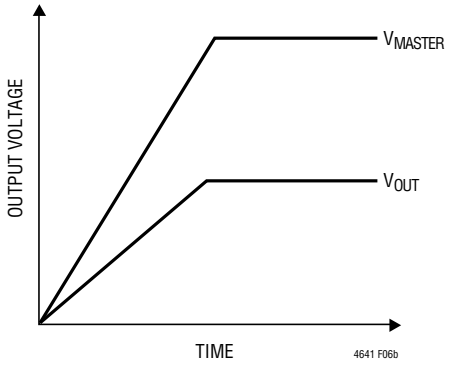
Figure 6 shows idealized output voltage waveforms for applications in which LTM4641's output (V_{OUT}) tracks a master rail (V_{MASTER}) coincidently and ratiometrically, respectively.



(6a) Coincident Tracking



(6b) Ratiometric Tracking

Figure 6. Two Different Modes of Output Voltage Tracking

To configure LTM4641 for coincident or ratiometric tracking, begin the design (initially) the same way as for nontracking applications:

(1) Determine the R_{SET1A} , R_{SET1B}, and R_{SET2} values appropriate for the final, "full-scale" (FS) output voltage.

(2) Determine the R_{fSET} resistor needed to guarantee ramp down of the output voltage to the desired value. For example, if it is necessary for V_{OUT} to ramp down to 0.8V while tracking the master rail, then R_{fSET} is recommended from Table 1 to be ~887kΩ. If ramp-down tracking is not needed, then R_{fSET} can be chosen according to Table 1 (or Figure 3) and the FS output voltage of the LTM4641 generated rail.

(3) Choose output capacitors and input capacitors for the design in the same manner as is done for nontracking applications.

To fulfill a coincident rail-tracking requirement, recognize that when the output voltage of the master rail reaches the tracking rail's nominal FS voltage, the TRACK/SS pin of the LTM4641 (tracking slave) needs to be 600mV. This can be satisfied by forming a resistor-divider network composed of R_{TAC} and R_{TBC}, interfacing V_{OUT_MASTER} to TRACK/SS of the LTM4641 tracking slave, and terminating to SGND of the LTM4641 tracking slave. In Figure 7 and Figure 8, U1 generates a master rail while U2 generates a coincident-tracking rail that follows U1's output. Values of R_{TAC} and R_{TBC} are selected such that:

$$R_{TAC} = \left(\frac{V_{OUT\_SLAVE\_C\ (FS\ OUTPUT)}}{0.6V} - 1 \right) \bullet R_{TBC} \quad (17)$$

In the example circuit of Figure 7, the master rail generated by U1 ramps up its output to 1.8V. The coincident-tracking rail is generated by U2 and has a nominal FS output voltage of 1V. Values of R_{TAC} and R_{TBC} are determined such that when U1's output reaches 1V, the TRACK/SS pin of U2 reaches ~600mV; choosing R_{TBC} to be 10kΩ yields R_{TAC} = (1V/0.6V – 1) • 10kΩ, or ~6.65kΩ. It is common to choose resistor values of 10k or less for this task, so that voltage offset errors introduced by the 1µA current source on TRACK/SS working into the R_{TAC}/R_{TBC} network are sufficiently small.

To fulfill a ratiometric rail-tracking requirement, recognize that when the output voltage of the master rail reaches its final FS value, the TRACK/SS pin of the LTM4641 (tracking slave) needs to reach 600mV. This can be satisfied by forming a resistor-divider network composed of R_{TAR} and R_{TBR}, interfacing V_{OUT_MASTER} to TRACK/SS of the LTM4641 tracking slave, and terminating to SGND of the LTM4641 tracking slave. In Figure 7 and Figure 8, U3 generates a ratiometric-tracking rail that follows U1's output. Values of R_{TAR} and R_{TBR} are selected such that:

$$R_{TAR} = \left(\frac{V_{OUT\_MASTER\ (FS\_OUTPUT)}}{0.6V} - 1 \right) \bullet R_{TBR} \quad (18)$$