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Dual 9A or Single 18A µModule Regulator with Digital Power System Management

FEATURES

- **Dual, Fast, Analog Loops with Digital Interface for Control and Monitoring**
- **Wide Input Voltage Range: 4.5V to 17V**
- **Output Voltage Range: 0.5V to 5.5V**
- **±0.5% Maximum DC Output Error Over Temperature**
- **±2.5% Current Readback Accuracy at 9A Load**
- **400kHz PMBus-Compliant I²C Serial Interface**
- **Integrated 16-Bit ΔΣ ADC**
- **Supports Telemetry Polling Rates Up to 125Hz**
- **Constant Frequency Current Mode Control**
- **Parallel and Current Share Multiple Modules**
- All 7-Bit Slave Addresses Supported
- Drop-In Pin-Compatible to Dual 13A LTM4676A and Dual 18A LTM4677
- 16mm × 11.9mm × 3.51mm BGA Package

Readable Data:

- Input and Output Voltages, Currents, and Temperatures
- Running Peak Values, Uptime, Faults and Warnings
- Onboard EEPROM Fault Log Record

Writable Data and Configurable Parameters:

- Output Voltage, Voltage Sequencing and Margining
- Digital Soft-Start/Stop Ramp
- OV/UV/OT, UVLO, Frequency and Phasing

APPLICATIONS

- System Optimization in Prototype and Production

DESCRIPTION

The LTM®4675 is a dual 9A or single 18A step-down µModule® (micromodule) DC/DC regulator with 70ms turn-on time. It features remote configurability and telemetry-monitoring of power management parameters over PMBus—an open standard I²C-based digital interface protocol. The LTM4675 is comprised of fast analog control loops, precision mixed-signal circuitry, EEPROM, power MOSFETs, inductors and supporting components.

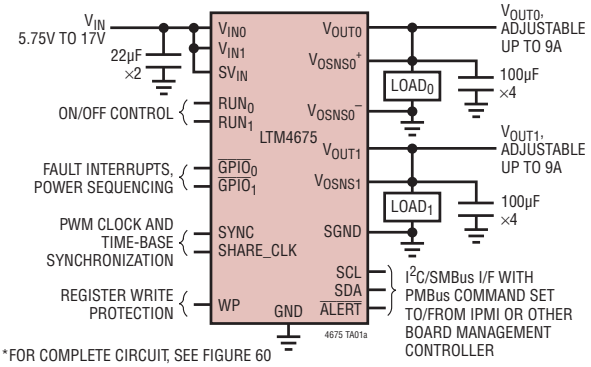
The LTM4675's 2-wire serial interface allows outputs to be margined, tuned and ramped up and down at programmable slew rates with sequencing delay times. Input and output currents and voltages, output power, temperatures, uptime and peak values are readable. Custom configuration of the EEPROM contents is not required. At start-up, output voltages, switching frequency, and channel phase angle assignments can be set by pin-strapping resistors. The LTpowerPlay™ GUI and DC1613 USB-to-PMBus converter and demo kits are available.

The LTM4675 is offered in a 16mm × 11.9mm × 3.51mm BGA package available with SnPb or RoHS compliant terminal finish.

Click to view associated Video Design Idea.

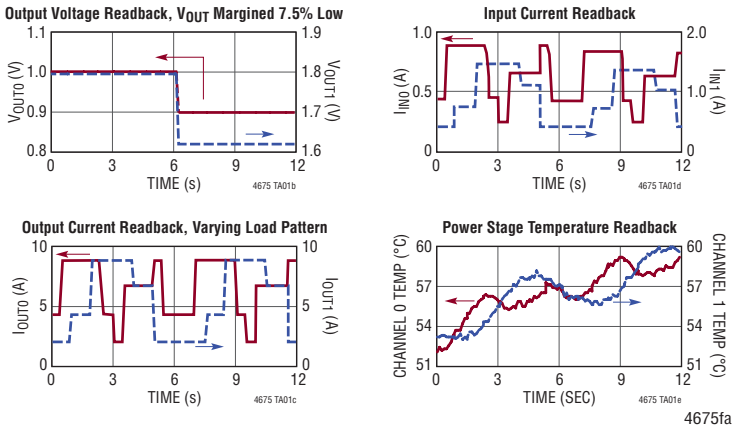
TYPICAL APPLICATION

Dual 9A µModule Regulator with Digital Interface for Control and Monitoring*



*FOR COMPLETE CIRCUIT, SEE FIGURE 60

Using PMBus and LTpowerPlay to Monitor Telemetry and Margin V_{OUT0}/V_{OUT1} During Load Pattern Tests. 10Hz Polling Rate. $12V_{IN}$



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ABSOLUTE MAXIMUM RATINGS

(Note 1)

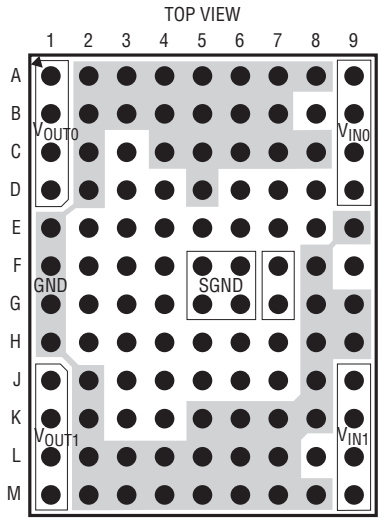
Terminal Voltages:

V_{IN}*n* (Note 4), SV_{IN} ..... –0.3V to 20V
V_{OUT}*n* ..... –0.3V to 6V
V_{OSNS0}^+, V_{ORB0}^+, V_{OSNS1}, V_{ORB1}, $INTV_{CC}$ .... –0.3V to 6V
RUN_n, SDA, SCL, $\overline{ALERT}$ ..... –0.3V to 5.5V
$F_{SWPHCFG}$, $V_{OUTn}CFG$, $V_{TRIMn}CFG$, ASEL .. –0.3V to 2.75V
V_{DD33}, $\overline{GPIO_n}$, SYNC, SHARE_CLK, WP,
$COMP_{na}$, V_{OSNS0}^-, V_{ORB0}^- ..... –0.3V to 3.6V
SGND ..... –0.3V to 0.3V

Temperatures

Internal Operating Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Package Body Temperature... 245°C

PIN CONFIGURATION



BGA PACKAGE
108-LEAD (16mm × 11.9mm × 3.51mm)

T_{JMAX} = 125°C, θ_{JCtop} = 5.9°C/W, $\theta_{JCbottom}$ = 2.1°C/W, θ_{JB} = 2.7°C/W, θ_{JA} = 16°C/W

θ VALUES DETERMINED PER JESD51-12

WEIGHT = 1.7 GRAMS

ORDER INFORMATION

http://www.linear.com/product/LTM4675#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (See Note 2)
		DEVICE	FINISH CODE			
LTM4675EY#PBF	SAC305 (RoHS)	LTM4675Y	e1	BGA	4	–40°C to 125°C
LTM4675IY#PBF	SAC305 (RoHS)	LTM4675Y	e1	BGA	4	–40°C to 125°C
LTM4675IY	SnPb (63/37)	LTM4675Y	e0	BGA	4	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage	Test Circuit 1 Test Circuit 2; VIN_OFF < VIN_ON = 4.25V	● ●	5.75 4.5		17 5.75	V V
V_{OUTn}	Range of Output Voltage Regulation	V_{OUT0} Differentially Sensed on V_{OSNS0}^+/V_{OSNS0}^- Pin-Pair; V_{OUT1} Differentially Sensed on V_{OSNS1}/SGND Pin-Pair; Commanded by Serial Bus or with Resistors Present at Start-Up on $V_{OUTnCFG}$ and/or $V_{TRIMnCFG}$	● ●	0.5 0.5		5.5 5.5	V V
$V_{OUTn(DC)}$	Output Voltage, Total Variation with Line and Load	(Note 5 V_{OUTn} Low Range ($MFR\_PWM\_MODE_n[1] = 1_b$), FREQUENCY_SWITCH = 425kHz) Digital Servo Engaged ($MFR\_PWM\_MODE_n[6] = 1_b$) Digital Servo Disengaged ($MFR\_PWM\_MODE_n[6] = 0_b$)	 ● 	 0.995 0.985	 1.000 1.000	 1.005 1.015	 V V
Input Specifications							
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	Test Circuit 1, V_{OUTn} =1V, V_{IN} = 12V; No Load Besides Capacitors; TON_RISE_n = 3ms			400		mA
$I_{Q(SVIN)}$	Input Supply Bias Current	Forced Continuous Mode, $MFR\_PWM\_MODE_n[0] = 1_b$ RUN_n = 5V, RUN_{1-n} = 0V Shutdown, $RUN_0 = RUN_1$ = 0V	 	 	 40 20	 	 mA mA
$I_{S(VINn,PSM)}$	Input Supply Current in Pulse-Skipping Mode Operation	Pulse-Skipping Mode, $MFR\_PWM\_MODE_n[0] = 0_b$, I_{OUTn} = 100mA			20		mA
$I_{S(VINn,FCM)}$	Input Supply Current in Forced-Continuous Mode Operation	Forced Continuous Mode, $MFR\_PWM\_MODE_n[0] = 1_b$ I_{OUTn} = 100mA I_{OUTn} = 9A	 	 	 40 927	 	 mA mA
$I_{S(VINn,SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, RUN_n = 0V			50		µA
Output Specifications							
I_{OUTn}	Output Continuous Current Range	(Note 6)		0		9	A
$\frac{\Delta V_{OUTn(LINE)}}{V_{OUTn}}$	Line Regulation Accuracy	Digital Servo Engaged ($MFR\_PWM\_MODE_n[6] = 1_b$) Digital Servo Disengaged ($MFR\_PWM\_MODE_n[6] = 0_b$) SV_{IN} and V_{INn} Electrically Shorted Together and $INTV_{CC}$ Open Circuit; I_{OUTn} = 0A, 5.75V ≤ V_{IN} ≤ 17V, V_{OUT} Low Range ($MFR\_PWM\_MODE_n[1] = 1_b$) FREQUENCY_SWITCH = 425kHz (Referenced to $12V_{IN}$) (Note 5)	 ●	 	0.03 0.03	 ±0.2	% %/V
$\frac{\Delta V_{OUTn(LOAD)}}{V_{OUTn}}$	Load Regulation Accuracy	Digital Servo Engaged ($MFR\_PWM\_MODE_n[6] = 1_b$) Digital Servo Disengaged ($MFR\_PWM\_MODE_n[6] = 0_b$) 0A ≤ I_{OUTn} ≤ 9A, V_{OUT} Low Range, ($MFR\_PWM\_MODE_n[1] = 1_b$) FREQUENCY_SWITCH = 425kHz (Note 5)	 ●	 	0.03 0.2	 0.5	% %
$V_{OUTn(AC)}$	Output Voltage Ripple				10		mV_{P-P}
f_S (Each Channel)	V_{OUTn} Ripple Frequency	FREQUENCY_SWITCH Set to 500kHz (0xFBE8)	●	462.5	500	537.5	kHz
$\Delta V_{OUTn(START)}$	Turn-On Overshoot	TON_RISE_n = 3ms (Note 12)			8		mV
t_{START}	Turn-On Start-Up Time	Time from V_{IN} Toggling from 0V to 12V to Rising Edge of $\overline{GPIO}_n$. TON_DELAY_n = 0ms, TON_RISE_n = 3ms, $MFR\_GPIO\_PROPAGATE_n$ = 0x0100, $MFR\_GPIO\_RESPONSE_n$ = 0x0000	●		60	70	ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{DELAY(0ms)}$	Turn-On Delay Time	Time from First Rising Edge of RUN_n to Rising Edge of $\overline{GPIO}_n$. TON_DELAY_n = 0ms, TON_RISE_n = 3ms, $MFR\_GPIO\_PROPAGATE_n$ = 0x0100, $MFR\_GPIO\_RESPONSE_n$ = 0x0000. V_{IN} Having Been Established for at Least 70ms	●	2.75	3.1	3.5	ms
$\Delta V_{OUTn(LS)}$	Peak Output Voltage Deviation for Dynamic Load Step	Load: 0A to 4.5A and 4.5A to 0A at 4.5A/µs, Figure 60 Circuit, V_{OUTn} = 1V, V_{IN} = 12V (Note 12)			50		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0A to 4.5A and 4.5A to 0A at 4.5A/µs, Figure 60 Circuit, V_{OUTn} = 1V, V_{IN} = 12V (Note 12)			35		µs
$I_{OUTn(OCL\_PK)}$	Output Current Limit, Peak	Cycle-by-Cycle Inductor Peak Current Limit Inception			15.8		A
$I_{OUTn(OCL\_AVG)}$	Output Current Limit, Time Averaged	Time-Averaged Output Inductor Current Limit Inception Threshold, Commanded by $IOUT\_OC\_FAULT\_LIMIT_n$ (Note 12)			10.8A; See $I_{O-RB-ACC}$ Specification (Output Current Readback Accuracy)		
Control Section							
V_{FBCM0}	Channel 0 Feedback Input Common Mode Range	V_{OSNS0}^- Valid Input Range (Referred to SGND) V_{OSNS0}^+ Valid Input Range (Referred to SGND)	● ●	–0.1		0.3 5.7	V V
V_{FBCM1}	Channel 1 Feedback Input Common Mode Range	SGND Valid Input Range (Referred to GND) V_{OSNS1} Valid Input Range (Referred to SGND)	● ●	–0.3		0.3 5.7	V V
$V_{OUT-RNG0}$	Full-Scale Command Voltage, Range 0	(Notes 7, 15) V_{OUTn} Commanded to 5.500V, $MFR\_PWM\_MODE_n[1] = 0_b$ Resolution LSB Step Size		5.422	 12 1.375	5.576	V Bits mV
$V_{OUT-RNG1}$	Full-Scale Command Voltage, Range 1	(Notes 7, 15) V_{OUTn} Commanded to 2.750V, $MFR\_PWM\_MODE_n[1] = 1_b$ Resolution LSB Step Size		2.711	 12 0.6875	2.788	V Bits mV
$R_{VSENSE0}^+$	V_{OSNS0}^+ Impedance to SGND	$0.05V \le V_{VOSNS0}^+ - V_{SGND} \le 5.5V$			41		kΩ
$R_{VSENSE1}$	V_{OSNS1} Impedance to SGND	$0.05V \le V_{VOSNS1} - V_{SGND} \le 5.5V$			37		kΩ
$t_{ON(MIN)}$	Minimum On-Time	(Note 8)			90		ns
Analog OV/UV (Overvoltage/Undervoltage) Output Voltage Supervisor Comparators (VOUT_OV/UV_FAULT_LIMIT and VOUT_OV/UV_WARN_LIMIT Monitors)							
N_{OV/UV_COMP}	Resolution, Output Voltage Supervisors	(Note 15)			8		Bits
V_{OV-RNG}	Output OV Comparator Threshold Detection Range	(Note 15) High Range Scale, $MFR\_PWM\_MODE_n[1] = 0_b$ Low Range Scale, $MFR\_PWM\_MODE_n[1] = 1_b$		 1 0.5		 5.6 2.7	 V V
V_{OU-STP}	Output OV and UV Comparator Threshold Programming LSB Step Size	(Note 15) High Range Scale, $MFR\_PWM\_MODE_n[1] = 0_b$ Low Range Scale, $MFR\_PWM\_MODE_n[1] = 1_b$			 22 11		 mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OV-ACC}	Output OV Comparator Threshold Accuracy	(See Note 14)					
		$2V \le V_{VOSNS0}^+ - V_{VOSNS0}^- \le 5.6V$, $MFR\_PWM\_MODE_0[1] = 0_b$	●			±2	%
		$1V \le V_{VOSNS0}^+ - V_{VOSNS0}^- \le 2.7V$, $MFR\_PWM\_MODE_0[1] = 1_b$	●			±2	%
		$0.5V \le V_{VOSNS0}^+ - V_{VOSNS0}^- < 1V$, $MFR\_PWM\_MODE_0[1] = 1_b$	●			±20	mV
		$2V \le V_{VSENSE1} - V_{SGND} \le 5.6V$, $MFR\_PWM\_MODE_1[1] = 0_b$	●			±2	%
		$1.5V \le V_{VSENSE1} - V_{SGND} \le 2.7V$, $MFR\_PWM\_MODE_1[1] = 1_b$	●			±2	%
		$0.5V \le V_{VSENSE1} - V_{SGND} < 1.5V$, $MFR\_PWM\_MODE_1[1] = 1_b$	●			±30	mV
V_{UV-RNG}	Output UV Comparator Threshold Detection Range	(Note 15)					
		High Range Scale, $MFR\_PWM\_MODE_n[1] = 0_b$		1		5.4	V
		Low Range Scale, $MFR\_PWM\_MODE_n[1] = 1_b$		0.5		2.7	V
V_{UV-ACC}	Output UV Comparator Threshold Accuracy	(See Note 14)					
		$2V \le V_{VSENSE0}^+ - V_{VSENSE0}^- \le 5.4V$, $MFR\_PWM\_MODE_0[1] = 0_b$	●			±2	%
		$1V \le V_{VSENSE0}^+ - V_{VSENSE0}^- \le 2.7V$, $MFR\_PWM\_MODE_0[1] = 1_b$	●			±2	%
		$0.5V \le V_{VSENSE0}^+ - V_{VSENSE0}^- < 1V$, $MFR\_PWM\_MODE_0[1] = 1_b$	●			±20	mV
		$2V \le V_{VOSNS1} - V_{SGND} \le 5.4V$, $MFR\_PWM\_MODE_1[1] = 0_b$	●			±2	%
		$1.5V \le V_{VOSNS1} - V_{SGND} \le 2.7V$, $MFR\_PWM\_MODE_1[1] = 1_b$	●			±2	%
		$0.5V \le V_{VOSNS1} - V_{SGND} < 1.5V$, $MFR\_PWM\_MODE_1[1] = 1_b$	●			±30	mV
$t_{PROP-OV}$	Output OV Comparator Response Times	Overdrive to 10% Above Programmed Threshold				35	µs
$t_{PROP-UV}$	Output UV Comparator Response Times	Underdrive to 10% Below Programmed Threshold				50	µs
Analog OV/UV SV_{IN} Input Voltage Supervisor Comparators (Threshold Detectors for VIN_ON and VIN_OFF)							
$N_{SVIN-OV/UV-COMP}$	SV_{IN} OV/UV Comparator Threshold-Programming Resolution	(Note 15)			8		Bits
$SV_{IN-OU-RANGE}$	SV_{IN} OV/UV Comparator Threshold-Programming Range		●	4.5		20	V
$SV_{IN-OU-STP}$	SV_{IN} OV/UV Comparator Threshold-Programming LSB Step Size	(Note 15)			82		mV
$SV_{IN-OU-ACC}$	SV_{IN} OV/UV Comparator Threshold Accuracy	$9V < SV_{IN} \le 20V$	●			±2.5	%
		$4.5V \le SV_{IN} \le 9V$	●			±225	mV
$t_{PROP-SVIN-HIGH-VIN}$	SV_{IN} OV/UV Comparator Response Time, High V_{IN} Operating Configuration	Test Circuit 1, and:					
		VIN_ON = 9V; SV_{IN} Driven from 8.775V to 9.225V	●			35	µs
		VIN_OFF = 9V; SV_{IN} Driven from 9.225V to 8.775V	●			35	µs
$t_{PROP-SVIN-LOW-VIN}$	SV_{IN} OV/UV Comparator Response Time, Low V_{IN} Operating Configuration	Test Circuit 2, and:					
		VIN_ON = 4.5V; SV_{IN} Driven from 4.225V to 4.725V	●			35	µs
		VIN_OFF = 4.5V; SV_{IN} Driven from 4.725V to 4.225V	●			35	µs
Channels 0 and 1 Output Voltage Readback ($READ\_VOUT_n$)							
N_{VO-RB}	Output Voltage Readback Resolution and LSB Step Size	(Note 15)			16 244		Bits µV
$V_{O-F/S}$	Output Voltage Full-Scale Digitizable Range	V_{RUNn} = 0V (Notes 7, 15)			8		V
$V_{O-RB-ACC}$	Output Voltage Readback Accuracy	Channel 0: $1V \le V_{VOSNS0}^+ - V_{VOSNS0}^- \le 5.5V$	●	Within ±0.5% of Reading			
		Channel 0: $0.6V \le V_{VOSNS0}^+ - V_{VOSNS0}^- < 1V$	●	Within ±5mV of Reading			
		Channel 1: $1V \le V_{VOSNS1} - V_{SGND} \le 5.5V$	●	Within ±0.5% of Reading			
		Channel 1: $0.6V \le V_{VOSNS1} - V_{SGND} < 1V$	●	Within ±5mV of Reading			

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{CONVERT-VO-RB}$	Output Voltage Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15) MFR_ADC_CONTROL=0x0D (Notes 9, 15) MFR_ADC_CONTROL=0x05 or 0x09 (Notes 9, 15)			100 27 8		ms ms ms
Input Voltage (SV_{IN}) Readback (READ_VIN)							
$N_{SVIN-RB}$	Input Voltage Readback Resolution and LSB Step Size	(Notes 10, 15)			10 15.625		Bits mV
$SV_{IN-F/S}$	Input Voltage Full-Scale Digitizable Range	(Notes 11, 15)			38.91		V
$SV_{IN-RB-ACC}$	Input Voltage Readback Accuracy	READ_VIN, 4.5V ≤ SV_{IN} ≤ 17V	●		Within ±2% of Reading		
$t_{CONVERT-SVIN-RB}$	Input Voltage Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15) MFR_ADC_CONTROL=0x01 (Notes 9, 15)			100 8		ms ms
Channels 0 and 1 Output Current (READ_IOUT$_n$), Duty Cycle (READ_DUTY_CYCLE$_n$), and Computed Input Current (MFR_READ_IIN$_n$) Readback							
N_{IO-RB}	Output Current Readback Resolution and LSB Step Size	(Notes 10, 12)			10 15.6		Bits mA
$I_{O-F/S}$, $I_{I-F/S}$	Output Current Full-Scale Digitizable Range and Input Current Range of Calculation	(Note 12)			±40		A
$I_{O-RB-ACC}$	Output Current, Readback Accuracy	READ_IOUT$_n$, Channels 0 and 1, 0 ≤ I_{OUTn} ≤ 9A, Forced-Continuous Mode, MFR_PWM_MODE$_n$[1:0] = 10_b	●		Within 225mA of Reading		
$I_{O-RB(9A)}$	Full Load Output Current Readback	I_{OUTn} = 9A (Note 12). See Histograms in Typical Performance Characteristics			9		A
N_{II-RB}	Computed Input Current, Readback Resolution and LSB Step Size	(Notes 10, 12)			10 1.95		Bits mA
$I_{I-RB-ACC}$	Computed Input Current, Readback Accuracy, Neglecting I_{SVIN}	MFR_READ_IIN$_n$, Channels 0 and 1, 0 ≤ I_{OUTn} ≤ 9A, Forced-Continuous Mode, MFR_PWM_MODE$_n$[1:0] = 10_b, MFR_IIN_OFFSET$_n$ = 0mA	●		Within 140mA of Reading		
$t_{CONVERT-IO-RB}$	Output Current Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15) MFR_ADC_CONTROL=0x0D (Notes 9, 15) MFR_ADC_CONTROL=0x06 or 0x0A (Notes 9, 15)			100 27 8		ms ms ms
$t_{CONVERT-II-RB}$	Computed Input Current, Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15)			100		ms
$N_{DUTY-RB}$	Resolution, Duty Cycle Readback	(Notes 10, 15)			10		Bits
D_{RB-ACC}	Duty Cycle TUE	READ_DUTY_CYCLE$_n$, 16.3% Duty Cycle (Note 15)				±3	%
$t_{CONVERT-DUTY-RB}$	Duty Cycle Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15)			100		ms
Temperature Readback for Channel 0, Channel 1, and Controller (Respectively: READ_TEMPERATURE_1$_0$, READ_TEMPERATURE_1$_1$, and READ_TEMPERATURE_2)							
T_{RES-RB}	Temperature Readback Resolution	Channel 0, Channel 1, and Controller (Note 15)			0.0625		°C
$T_{RB-CH-ACC(72mV)}$	Channel Temperature TUE, Switching Action Off	Channels 0 and 1, PWM Inactive, RUN_n = 0V, ΔV_{TSNSna} = 72mV	●		Within ±3°C of Reading		

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$T_{RB-CH-ACC(ON)}$	Channel Temperature TUE, Switching Action On	READ_TEMPERATURE_1$_n$, Channels 0 and 1, PWM Active, RUN_n = 5V (Note 12)			Within ±3°C of Reading		
$T_{RB-CTRL-ACC(ON)}$	Control IC Die Temperature TUE, Switching Action On	READ_TEMPERATURE_2, PWM Active, RUN_0 = RUN_1 = 5V (Note 12)			Within ±1°C of Reading		
$t_{CONVERT-TEMP-RB}$	Temperature Readback Update Rate	MFR_ADC_CONTROL=0x00 (Notes 9, 15) MFR_ADC_CONTROL=0x06 or 0x0A (Notes 9, 15)			100 8		ms ms
$INTV_{CC}$ Regulator							
V_{INTVCC}	Internal V_{CC} Voltage No Load	6V ≤ V_{IN} ≤ 17V		4.8	5	5.2	V
$\frac{\Delta V_{INTVCC(LOAD)}}{V_{INTVCC}}$	$INTV_{CC}$ Load Regulation	0mA ≤ I_{INTVCC} ≤ 50mA			0.5	±2	%
V_{DD33} Regulator							
V_{VDD33}	Internal V_{DD33} Voltage			3.2	3.3	3.4	V
$I_{LIM(VDD33)}$	V_{DD33} Current Limit	V_{DD33} Electrically Short-Circuited to GND			70		mA
V_{VDD33_OV}	V_{DD33} Overvoltage Threshold	(Note 15)			3.5		V
V_{VDD33_UV}	V_{DD33} Undervoltage Threshold	(Note 15)			3.1		V
V_{DD25} Regulator							
V_{VDD25}	Internal V_{DD25} Voltage				2.5		V
$I_{LIM(VDD25)}$	V_{DD25} Current Limit	V_{DD25} Electrically Short-Circuited to GND			50		mA
Oscillator and Phase-Locked Loop (PLL)							
f_{OSC}	Oscillator Frequency Accuracy	FREQUENCY_SWITCH = 500kHz (0xFBE8) 250kHz ≤ FREQUENCY_SWITCH ≤ 1MHz (Note 15)	● 			±7.5 ±7.5	% %
f_{SYNC}	PLL SYNC Capture Range	(Note 16)	●	225		1100	kHz
$V_{TH,SYNC}$	SYNC Input Threshold	V_{SYNC} Rising (Note 15) V_{SYNC} Falling (Note 15)			1.5 1		V V
$V_{OL,SYNC}$	SYNC Low Output Voltage	I_{SYNC} = 3mA	●		0.3	0.4	V
I_{SYNC}	SYNC Leakage Current in Frequency Slave Mode	0V ≤ V_{SYNC} ≤ 3.6V MFR_CONFIG_ALL[4]=1_b	●			±5	µA
θ_{SYNC}-θ0	SYNC-to-Channel 0 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT0) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 000_b, $01X_b$ MFR_PWM_CONFIG[2:0] = 101_b MFR_PWM_CONFIG[2:0] = 001_b MFR_PWM_CONFIG[2:0] = $1X0_b$			 0 60 90 120		 Deg Deg Deg Deg
θ_{SYNC}-θ1	SYNC-to-Channel 1 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT1) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 011_b MFR_PWM_CONFIG[2:0] = 000_b MFR_PWM_CONFIG[2:0] = 010_b, $10X_b$ MFR_PWM_CONFIG[2:0] = 001_b MFR_PWM_CONFIG[2:0] = 110_b			 120 180 240 270 300		 Deg Deg Deg Deg Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EEPROM Characteristics							
Endurance	(Note 13)	0°C ≤ T_J ≤ 85°C During EEPROM Write Operations (Note 3)	●	10,000			Cycles
Retention	(Note 13)	$T_J < T_{J(MAX)}$, with Most Recent EEPROM Write Operation Having Occurred at 0°C ≤ T_J ≤ 85°C (Note 3)	●	10			Years
Mass_Write	Mass Write Operation Time	Execution of STORE_USER_ALL Command, 0°C ≤ T_J ≤ 85°C (ATE-Tested at T_J = 25°C) (Notes 3, 13)			440	4100	ms
Digital I/Os							
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN_n, $\overline{GPIO}_n$ (Note 15) SHARE_CLK, WP (Note 15)		2.0 1.8			V V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN_n, $\overline{GPIO}_n$ (Note 15) SHARE_CLK, WP (Note 15)				1.4 0.6	V V
V_{HYST}	Input Hysteresis	SCL, SDA (Note 15)			80		mV
V_{OL}	Output Low Voltage	SCL, SDA, $\overline{ALERT}$, RUN_n, $\overline{GPIO}_n$, SHARE_CLK: I_{SINK} = 3mA	 ●		 0.3	 0.4	 V
I_{OL}	Input Leakage Current	SDA, SCL, $\overline{ALERT}$, RUN_n: 0V ≤ V_{PIN} ≤ 5.5V $\overline{GPIO}_n$ and SHARE_CLK: 0V ≤ V_{PIN} ≤ 3.6V	● ●			±5 ±2	µA µA
t_{FILTER}	Input Digital Filtering	RUN_n (Note 15) $\overline{GPIO}_n$ (Note 15)			10 3		µs µs
C_{PIN}	Input Capacitance	SCL, SDA, RUN_n, $\overline{GPIO}_n$, SHARE_CLK, WP (Note 15)				10	pF
PMBus Interface Timing Characteristics							
f_{SMB}	Serial Bus Operating Frequency	(Note 15)		10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start	(Note 15)		1.3			µs
$t_{HD,STA}$	Hold Time After Repeated Start Condition	Time Period After Which First Clock Is Generated (Note 15)		0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time	(Note 15)		0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time	(Note 15)		0.6			µs
$t_{HD,DAT}$	Data Hold Time	Receiving Data (Note 15) Transmitting Data (Note 15)		0 0.3		 0.9	µs µs
$t_{SU,DAT}$	Data Setup Time	Receiving Data (Note 15)		0.1			µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer Timeout	Measured from the Last PMBus Start Event: Block Reads, MFR_CONFIG_ALL[3]=0_b (Note 15) Non-Block Reads, MFR_CONFIG_ALL[3]=0_b (Note 15) MFR_CONFIG_ALL[3]=1_b (Note 15)			 150 32 250		 ms ms ms
t_{LOW}	Serial Clock Low Period	(Note 15)		1.3		10000	µs
t_{HIGH}	Serial Clock High Period	(Note 15)		0.6			µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listing under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating conditions for extended periods may affect device reliability and lifetime.

Note 2: The LTM4675 is tested under pulsed-load conditions such that $T_J \approx T_A$. The LTM4675E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4675I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The LTM4675's EEPROM temperature range for valid write commands is 0°C to 85°C. To achieve guaranteed EEPROM data retention, execution of the "STORE_USER_ALL" command—i.e., uploading RAM contents to NVM—outside this temperature range is not recommended. However, as long as the LTM4675's EEPROM temperature is less than 130°C, the LTM4675 *will* obey the STORE_USER_ALL command. Only when EEPROM temperature exceeds 130°C, the LTM4675 will not act on any STORE_USER_ALL transactions: instead, the LTM4675 NACKs the serial command and asserts its relevant CML (communications, memory, logic) fault bits. EEPROM temperature can be queried prior to commanding STORE_USER_ALL; see the Applications Information section.

Note 4: The two power inputs—V_{IN0} and V_{IN1}—and their respective power outputs—V_{OUT0} and V_{OUT1}—are tested independently in production. A shorthand notation is used in this document that allows these parameters to be refered to by "$V_{IN}n$" and "$V_{OUT}n$", where *n* is permitted to take on a value of 0 or 1. This italicized, subscripted "*n*" notation and convention is extended to encompass all such pin names, as well as register names with channel-specific, i.e., paged data. For example, VOUT_COMMAND$_n$ refers to the VOUT_COMMAND command code data located in Pages 0 and 1, which in turn relate to Channels 0 (V_{OUT0}) and Channel 1 (V_{OUT1}). Registers containing non-page-specific data, i.e., whose data is "global" to the module or applies to both of the module's Channels lack the italicized, subscripted "*n*", e.g., FREQUENCY_SWITCH.

Note 5: $V_{OUT}n_{(DC)}$ and line and load regulation tests are performed in production with digital servo disengaged (MFR_PWM_MODE$_n$[6] = 0_b) and low $V_{OUT}n$ range selected (MFR_PWM_MODE$_n$[1]) = 1_b. The digital servo control loop is exercised in production (setting MFR_PWM_MODE$_n$[6] = 1_b), but convergence of the output voltage to its final settling value is not necessarily observed in final test—due to potentially long time constants involved—and is instead guaranteed by the output voltage readback accuracy specification. Evaluation in application demonstrates capability; see the Typical Performance Characteristics section.

Note 6: See output current derating curves for different V_{IN}, V_{OUT}, and T_A, located in the Applications Information section.

Note 7: Even though V_{OUT0} and V_{OUT1} are specified for 6V absolute maximum, the maximum recommended regulation-command voltage is: 5.5V for a high-V_{OUT} range setting of MFR_PWM_MODE$_n$[1]=0_b; 2.5V for a low-V_{OUT} range setting of MFR_PWM_MODE$_n$[1]=1_b.

Note 8: Minimum on-time is tested at wafer sort.

Note 9: Data conversion is performed in round-robin (cyclic) fashion. All telemetry signals are continuously digitized, and reported data is based on measurements not older than 100ms, typical. Some telemetry parameters can be digitized at a faster update rate by configuring MFR_ADC_CONTROL.

Note 10: The following telemetry parameters are formatted in PMBus-defined "Linear Data Format", in which each register contains a word comprised of 5 most significant bits—representing a signed exponent, to be raised to the power of 2—and 11 least significant bits—representing a signed mantissa: input voltage (on SV_{IN}), accessed via the READ_VIN command code; output currents ($I_{OUT}n$), accessed via the READ_IOUT$_n$ command codes; module input current ($I_{VIN0} + I_{VIN1} + I_{SVIN}$), accessed via the READ_IIN command code; channel input currents ($I_{VIN}n + 1/2 \bullet I_{SVIN}$), accessed via the MFR_READ_IIN$_n$ command codes;and duty cycles of channel 0 and channel 1 switching power stages, accessed via the READ_DUTY_CYCLE$_n$ command codes. This data format limits the resolution of telemetry readback data to 10 bits even though the internal ADC is 16 bits and the LTM4675's internal calculations use 32-bit words.

Note 11: The absolute maximum rating for the SV_{IN} pin is 20V. Input voltage telemetry (READ_VIN) is obtained by digitizing a voltage scaled down from the SV_{IN} pin.

Note 12: These typical parameters are based on bench measurements and are not production tested.

Note 13: EEPROM endurance and retention are guaranteed by wafer-level testing for data retention. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification, and whose EEPROM data was written to at $0°C \le T_J \le 85°C$. Downloading NVM contents to RAM by executing the RESTORE_USER_ALL or MFR_RESET commands is valid over the entire operating temperature range and does not influence EEPROM characteristics.

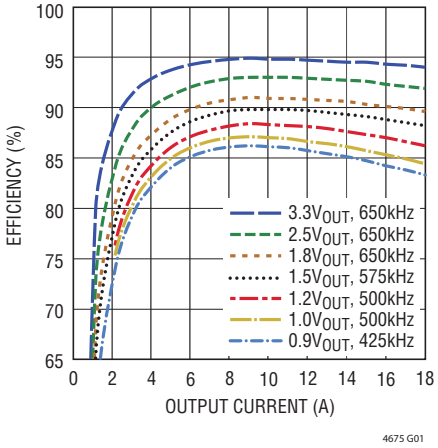
Note 14: Channel 0 OV/UV comparator threshold accuracy for MFR_PWM_MODE$_0$[1] = 1_b tested in ATE at $V_{VOSNS0}^+ – V_{VOSNS0}^-$ = 0.5V and 2.7V. 1V condition tested at IC-Level, only. Channel 1 OV/UV comparator threshold accuracy for MFR_PWM_MODE$_1$[1] = 1_b tested in ATE with V_{VOSNS1}-V_{SGND} = 0.5V and 2.7V. 1.5V condition tested at IC-level, only.

Note 15: Tested at IC-level ATE.

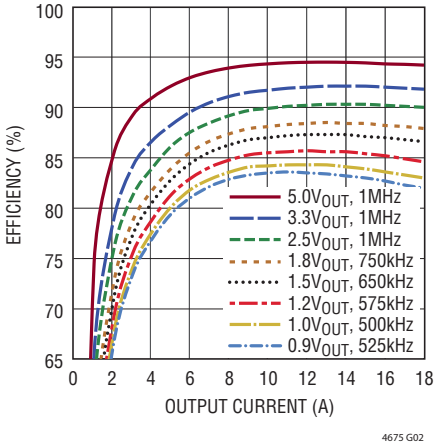
Note 16: PLL SYNC capture range tested with FREQUENCY_SWITCH set to frequency slave mode (0x0000), with MFR_CONFIG_ALL[4] = 1_b, and with SYNC driven by external clock. Low end of SYNC capture range (225kHz) verified at V_{IN} = 5.75V and $V_{OUT}n$ = 2.5V. High end of SYNC capture range (1.1MHz) verified at V_{IN} = 12V and $V_{OUT}n$ = 3.3V.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, $12V_{IN}$ to $1V_{OUT}$, unless otherwise noted.

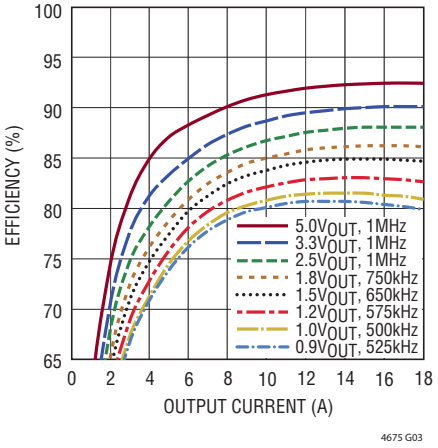
Efficiency vs Load Current at $5V_{IN}$



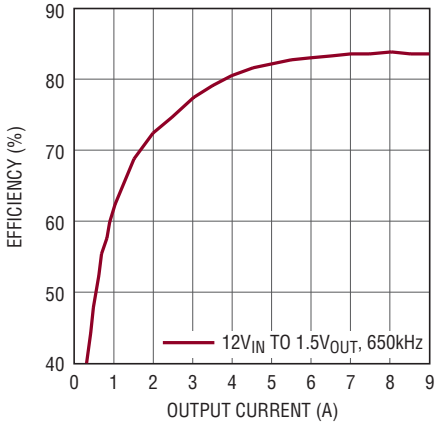
Efficiency vs Load Current at $8V_{IN}$



Efficiency vs Load Current at $12V_{IN}$



Single Phase Single Output Pulse-Skipping (Discontinuous) Mode Efficiency, V_{IN} = SV_{IN} = V_{INn}, $INTV_{CC}$ Open, $MFR\_PWM\_MODE_n[0] = 0_b$



Dual Phase Single Output Load Transient Response, $12V_{IN}$ to $1V_{OUT}$

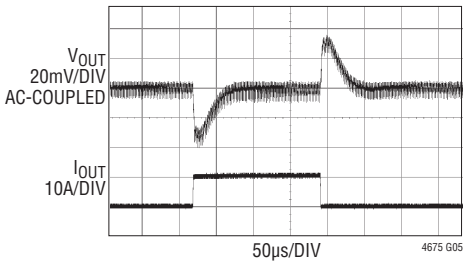


FIGURE 27 CIRCUIT AT $12V_{IN}$, $INTV_{CC}$ PIN OPEN CIRCUIT AND $VOUT\_COMMAND_n$ SET TO 1.000V. 8A TO 18A LOAD STEP AT 10A/µs

Single Phase Single Output Load Transient Response, $12V_{IN}$ to $1V_{OUT}$

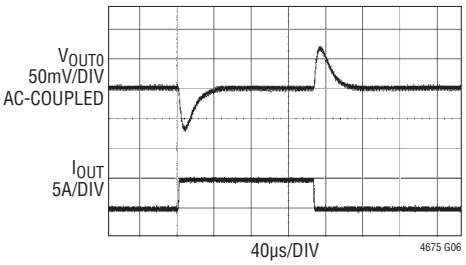


FIGURE 60 CIRCUIT AT $12V_{IN}$ 0A TO 5A LOAD STEP AT 5A/µs

Dual Phase Single Output Load Transient Response, $5V_{IN}$ to $1V_{OUT}$

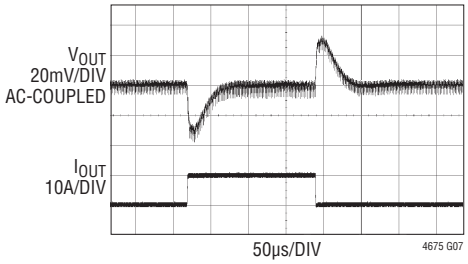


FIGURE 27 CIRCUIT AT $5V_{IN}$, $VOUT\_COMMAND_n$ SET TO 1.000V. 8A TO 18A LOAD STEP AT 10A/µs

Dual Output Concurrent Rail Start-Up/Shutdown

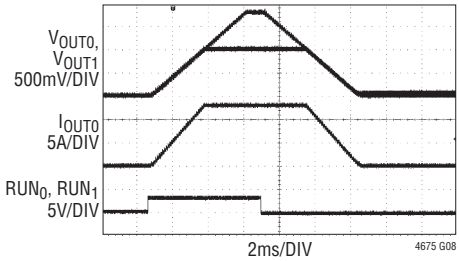


FIGURE 60 CIRCUIT AT $12V_{IN}$, 112mΩ LOAD ON V_{OUT0}, NO LOAD ON V_{OUT1}. TON_RISE_0 = 3ms, TON_RISE_1 = 5.297ms, $TOFF\_DELAY_1$ = 0ms, $TOFF\_DELAY_0$ = 2.43ms, $TOFF\_FALL_1$ = 5.328ms, $TOFF\_FALL_0$ = 3ms, $ON\_OFF\_CONFIG_n$ = 0x1E

Dual Output Start-Up/Shutdown with a Pre-Biased Load

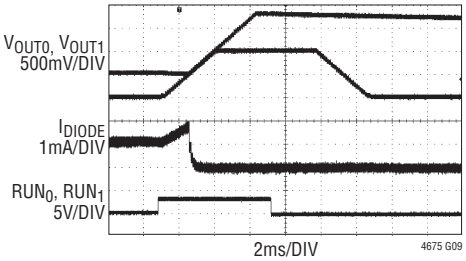


FIGURE 60 CIRCUIT AT $12V_{IN}$, 112mΩ LOAD ON V_{OUT0}, 500Ω ON V_{OUT1}. V_{OUT1} PRE-BIASED THROUGH A DIODE. TON_RISE_0 = 3ms, TON_RISE_1 = 5.297ms, $TOFF\_DELAY_1$ = 0ms, $TOFF\_DELAY_0$ = 2.43ms, $TOFF\_FALL_1$ = 5.328ms, $TOFF\_FALL_0$ = 3ms, $ON\_OFF\_CONFIG_1$ = 0x1F $ON\_OFF\_CONFIG_0$ = 0x1E

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, $12V_{IN}$ to $1V_{OUT}$, unless otherwise noted.

Single Phase Single Output Short-Circuit Protection at No Load

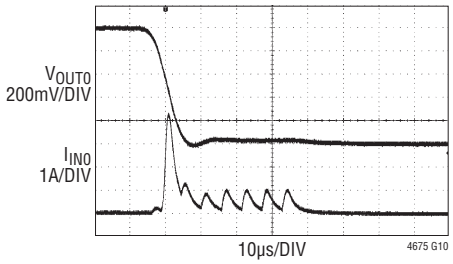


FIGURE 60 CIRCUIT AT $12V_{IN}$, NO LOAD ON V_{OUT0} PRIOR TO APPLICATION OF SHORT CIRCUIT

Single Phase Single Output Short-Circuit Protection at Full Load

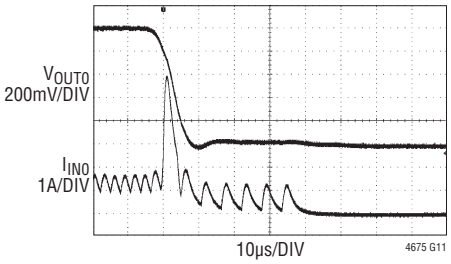
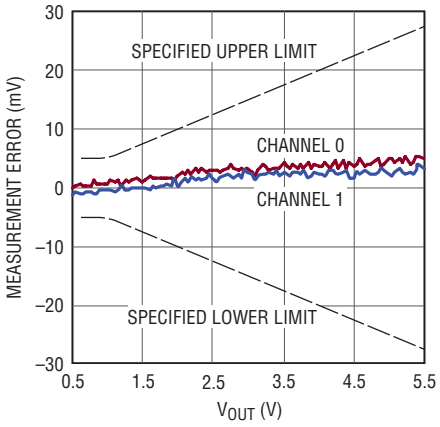
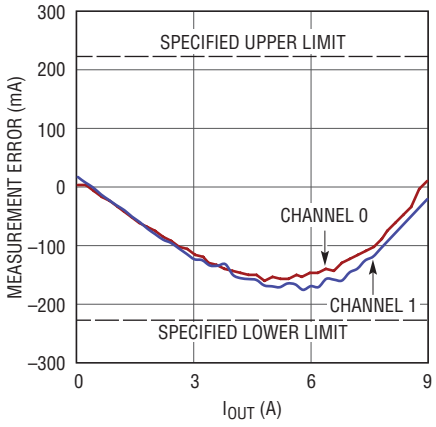


FIGURE 60 CIRCUIT AT $12V_{IN}$, 112mΩ LOAD ON V_{OUT0} PRIOR TO APPLICATION OF SHORT CIRCUIT

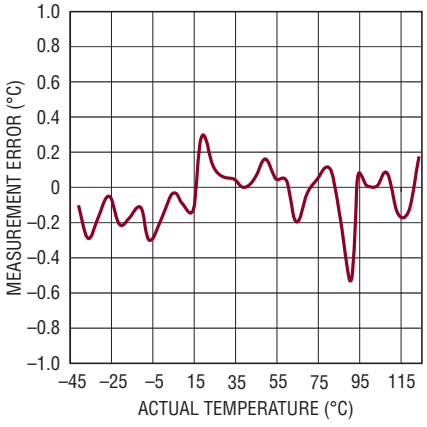
READ_VOUT$_n$ (Output Voltage Readback) Error vs V_{OUTn} I_{OUTn} = No Load, RUN_{1-n} = 0V



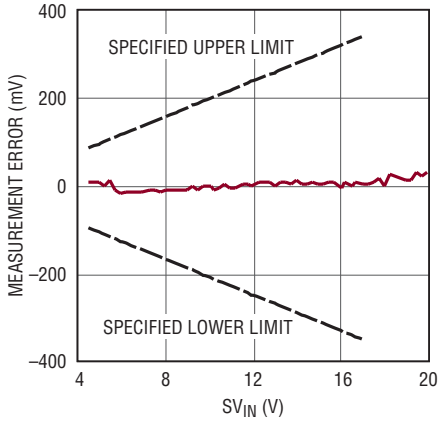
READ_IOUT$_n$ (Output Current Readback) Error vs I_{OUTn}



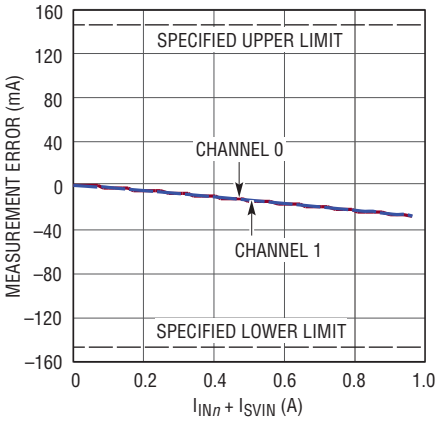
READ_TEMPERATURE_2 (Control IC Temperature Error) vs Junction Temperature, RUN_n = 0V



READ_VIN (Input Voltage Readback Telemetry) Error vs SV_{IN}, RUN_n = 0V



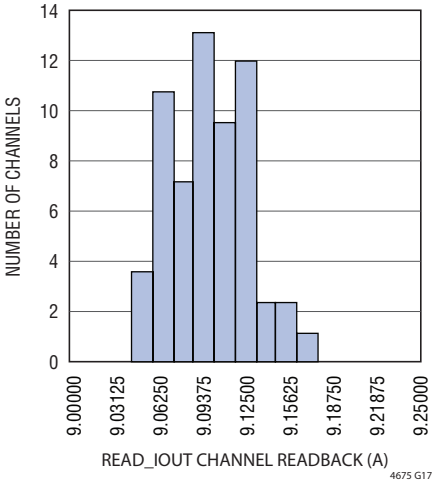
MFR_READ_IIN$_n$ (Input Current Readback) Error vs (I_{VINn} + I_{SVIN}), $MFR\_PWM\_MODE_n[0]=1_b$, I_{OUTn} Swept from 0A to 9A, One Channel at a Time, RUN_{1-n} = 0V



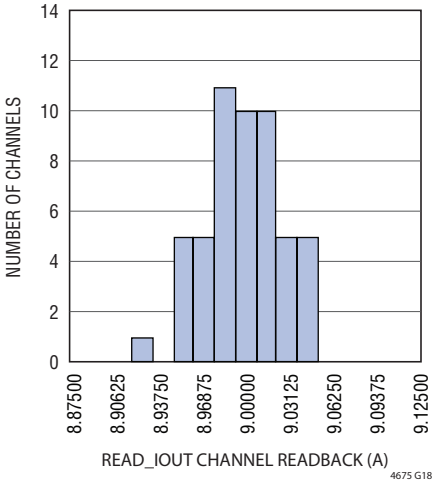
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, 12V_{IN} to 1V_{OUT}, unless otherwise noted.

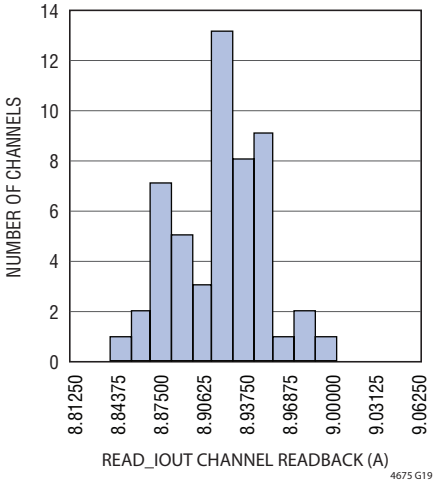
READ_IOUT of 26 LTM4675s (DC2053) 12V_{IN}, 1V_{OUT}, T_J = –40°C, I_{OUTn} = 9A, System Having Reached Thermally Steady-State Condition, No Airflow



READ_IOUT of 26 LTM4675s (DC2053) 12V_{IN}, 1V_{OUT}, T_J = 25°C, I_{OUTn} = 9A, System Having Reached Thermally Steady-State Condition, No Airflow



READ_IOUT of 26 LTM4675s (DC2053) 12V_{IN}, 1V_{OUT}, T_J = 125°C, I_{OUTn} = 9A, System Having Reached Thermally Steady-State Condition, No Airflow



PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (A2-8, B2-7, C2, C4-8, D2, D5, E1, E9, F1, F8, G1, G8-9, H1, H8-9, J2, J8, K2, K5-8, L2-7, M2-8): Power Ground of the LTM4675. Power return for V_{OUT0} and V_{OUT1}.

V_{OUT0} (A1, B1, C1, D1): Channel 0 Output Voltage.

V_{OSNS0}^+ (D7): Channel 0 Positive Differential Voltage Sense Input. Together, V_{OSNS0}^+ and V_{OSNS0}^- serve to kelvin-sense the V_{OUT0} output voltage at V_{OUT0}'s point of load (POL) and provide the differential feedback signal directly to Channel 0's control loop and voltage supervisor circuits. V_{OUT0} can regulate up to 5.5V output. Command V_{OUT0}'s target regulation voltage by serial bus. Its initial command value at SV_{IN} power-up is dictated by NVM (non-volatile memory) contents (factory default: 1.000V)—or, optionally, may be set by configuration resistors; see $V_{OUT0CFG}$, $V_{TRIM0CFG}$ and the Applications Information section.

V_{OSNS0}^- (E7): Channel 0 Negative Differential Voltage Sense Input. See V_{OSNS0}^+.

V_{ORB0}^+ (D8): Channel 0 Positive Readback Pin. Shorted to V_{OSNS0}^+ internal to the LTM4675. If desired, place a test point on this node and measure its impedance to V_{OUT0} on one's hardware (e.g., motherboard, during in circuit test (ICT) post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OSNS0}^+ and V_{OUT0}.

V_{ORB0}^- (E8): Channel 0 Negative Readback Pin. Shorted to V_{OSNS0}^- internal to the LTM4675. If desired, place a test point on this node and measure its impedance to GND on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OSNS0}^- and GND (V_{OUT0} power return).

V_{OUT1} (J1, K1, L1, M1): Channel 1 Output Voltage.

V_{OSNS1} (H7): Channel 1 Positive Voltage Sense Input. Connect V_{OSNS1} to V_{OUT1} at the POL. This provides the feedback signal for Channel 1's control loop and voltage supervisor circuits. V_{OUT1} can regulate up to 5.5V output. Command V_{OUT1}'s target regulation voltage by serial bus. Its initial command value at SV_{IN} power-up is dictated by

PIN FUNCTIONS

NVM (non-volatile memory) contents (factory default: 1.000V)—or, optionally, may be set by configuration resistors; see $V_{OUT1CFG}$, $V_{TRIM1CFG}$ and the Applications Information section.

SGND (F5-6, G5-6): Channel 1 Negative Voltage Sense Input. See V_{OSNS1}. Additionally, SGND is the signal ground return path of the LTM4675. If desired, one may place a test point on one of the four SGND pins and measure its impedance to GND on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between the other three SGND pins and GND (V_{OUT1} power return). SGND is not electrically connected to GND internal to the LTM4675. Connect SGND to GND local to the LTM4675.

V_{ORB1} (J7): Channel 1 Positive Readback Pin. Shorted to V_{OSNS1} internal to the LTM4675. At one's option, place a test point on this node and measure its impedance to V_{OUT1} on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OUT1} and V_{OSNS1}.

V_{IN0} (A9, B9, C9, D9): Positive Power Input to Channel 0 Switching Stage. Provide sufficient decoupling capacitance in the form of multilayer ceramic capacitors (MLCCs) and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. MLCCs should be placed as close to the LTM4675 as physically possible. See Layout Recommendations in the Applications Information section.

V_{IN1} (J9, K9, L9, M9): Positive Power Input to Channel 1 Switching Stage. Provide sufficient decoupling capacitance in the form of MLCCs and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. MLCCs should be placed as close to the LTM4675 as physically possible. See Layout Recommendations in the Applications Information section.

SW_0 (B8): Switching Node of Channel 0 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. May be routed a short distance to a local test point to monitor switching action of Channel 0, if desired, but do not route near any sensitive signals; otherwise, leave electrically isolated (open).

SW_1 (L8): Switching Node of Channel 1 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. May be routed a short distance to a local test point to monitor switching action of Channel 1, if desired, but do not route near any sensitive signals; otherwise, leave open.

SV_{IN} (F9): Input Supply for LTM4675's Internal Control IC. In most applications, SV_{IN} connects to V_{IN0} and/or V_{IN1}, in which case no external decoupling beyond that already allocated for V_{IN0}/V_{IN1} is required. If SV_{IN} is operated from an auxiliary supply separate from V_{IN0}/V_{IN1}, decouple this pin to GND with a capacitor (0.1µF to 1µF).

$INTV_{CC}$ (F7, G7): Internal Regulator, 5V Output. When operating the LTM4675 from $5.75V \le SV_{IN} \le 17V$, an LDO generates $INTV_{CC}$ from SV_{IN} to bias internal control circuits and the MOSFET drivers of the LTM4675. No external decoupling is required. $INTV_{CC}$ is regulated regardless of the RUN_n pin state. When operating the LTM4675 with $4.5V \le SV_{IN} < 5.75V$, $INTV_{CC}$ *must* be electrically shorted to SV_{IN}.

V_{DD33} (J5): Internally Generated 3.3V Power Supply Output Pin. This pin should only be used to provide external current for the pull-up resistors required for $\overline{GPIO}_n$, SHARE_CLK, and SYNC, and may be used to provide external current for pull-up resistors on RUN_n, SDA, SCL and $\overline{ALERT}$. No external decoupling is required.

V_{DD25} (J4): Internally Generated 2.5V Power Supply Output Pin. Do not load this pin with external current; it is used strictly to bias internal logic and provides current for the internal pull-up resistors connected to the configuration-programming pins. No external decoupling is required.

ASEL (G2): Serial Bus Address Configuration Pin. On any given I^2C/SMBus serial bus segment, every device must have its own unique slave address. If this pin is left open, the LTM4675 powers up to its default slave address of 0x4F (hexadecimal), i.e., 1001111_b (industry standard convention is used throughout this document: 7-bit slave addressing). The lower four bits of the LTM4675's slave address can be altered from this default value by connecting a resistor from this pin to SGND. Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state.

PIN FUNCTIONS

$F_{SWPHCFG}$ (H2): Switching Frequency, Channel Phase-Interleaving Angle and Phase Relationship to SYNC Configuration Pin. If this pin is left open—or, if the LTM4675 is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4675's switching frequency (FREQUENCY_SWITCH) and channel phase relationships (with respect to the SYNC clock; MFR_PWM_CONFIG[2:0]) are dictated at SV_{IN} power-up according to the LTM4675's NVM contents. Default factory values are: 500kHz operation; Channel 0 at 0°; and Channel 1 at 180°C (convention throughout this document: a phase angle of 0° means the channel's switch node rises coincident with the falling edge of the SYNC pulse). Connecting a resistor from this pin to SGND (and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0_b) allows a convenient way to configure multiple LTM4675s with identical NVM contents for different switching frequencies of operation and phase interleaving angle settings of intra- and extra-module-paralleled channels—all, without GUI intervention or the need to "custom pre-program" module NVM contents. (See the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state.

$V_{OUT0CFG}$ (G3): Output Voltage Select Pin for V_{OUT0}, Coarse Setting. If the $V_{OUT0CFG}$ and $V_{TRIM0CFG}$ pins are both left open—or, if the LTM4675 is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4675's target V_{OUT0} output voltage setting ($VOUT\_COMMAND_0$) and associated power-good and OV/UV warning and fault thresholds are dictated at SV_{IN} power-up according to the LTM4675's NVM contents. A resistor* connected from this pin to SGND—in combination with resistor pin settings on $V_{TRIM0CFG}$, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0_b—can be used to configure the LTM4675's Channel 0 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. (See the Applications Information section.) Connecting resistor(s) from $V_{OUT0CFG}$ to SGND and/or $V_{TRIM0CFG}$ to SGND in this manner allows a convenient way to configure multiple LTM4675s with identical NVM contents for different output voltage settings—all without GUI intervention or the need to "custom-pre-program" module NVM contents. Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs* on $V_{OUT0CFG}/V_{TRIM0CFG}$ can affect the V_{OUT0} range setting ($MFR\_PWM\_MODE_0$[1]) and loop gain.

$V_{TRIM0CFG}$ (H3): Output Voltage Select Pin for V_{OUT0}, Fine Setting. Works in combination with $V_{OUT0CFG}$ to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 0, at SV_{IN} power-up. (See $V_{OUT0CFG}$ and the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs* on $V_{OUT0CFG}/V_{TRIM0CFG}$ can affect the V_{OUT0} range setting ($MFR\_PWM\_MODE_0$[1]) and loop gain.

$V_{OUT1CFG}$ (G4): Output Voltage Select Pin for V_{OUT1}, Coarse Setting. If the $V_{OUT1CFG}$ and $V_{TRIM1CFG}$ pins are both left open—or, if the LTM4675 is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4675's target V_{OUT1} output voltage setting ($VOUT\_COMMAND_1$) and associated OV/UV warning and fault thresholds are dictated at SV_{IN} power-up according to the LTM4675's NVM contents, in precisely the same fashion that the $V_{OUT0CFG}$ and $V_{TRIM0CFG}$ pins affect the respective settings of V_{OUT0}/Channel 0. (See $V_{OUT0CFG}$, $V_{TRIM0CFG}$ and the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs* on $V_{OUT1CFG}/V_{TRIM1CFG}$ can affect the V_{OUT1} range setting ($MFR\_PWM\_MODE_1$[1]) and loop gain.

$V_{TRIM1CFG}$ (H4): Output Voltage Select Pin for V_{OUT1}, Fine Setting. Works in combination with $V_{OUT1CFG}$ to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 1, at SV_{IN} power-up. (See $V_{OUT1CFG}$ and the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs* on $V_{OUT1CFG}/V_{TRIM1CFG}$ can affect the V_{OUT1} range setting ($MFR\_PWM\_MODE_1$[1]) and loop gain.

*In applications where V_{OUT0} and V_{OUT1} are paralleled, the respective $V_{OUTnCFG}$ and $V_{TRIMnCFG}$ pin-pairs can be electrically connected together; common RCONFIG resistors can be applied, whose values are half of what is prescribed in Table 2 and Table 3. See Figure 34, for example.

PIN FUNCTIONS

SYNC (E5): PWM Clock Synchronization Input and Open-Drain Output Pin. The setting of the FREQUENCY_SWITCH command dictates whether the LTM4675 is a "sync master" or "sync slave" module. When the LTM4675 is a sync master, FREQUENCY_SWITCH contains the commanded switching frequency of Channels 0 and 1—in PMBus linear data format—and it drives its SYNC pin low for 500ns at a time, at this commanded rate. In contrast, a sync slave uses MFR_CONFIG_ALL[4]=1_b and does not pull its SYNC pin low. The LTM4675's PLL synchronizes the LTM4675's PWM clock to the waveform present on the SYNC pin—and therefore, a resistor pull-up to 3.3V is required in the application, regardless of whether the LTM4675 is a sync master or slave. EXCEPTION: driving the SYNC pin with an external clock is permissible; see the Applications Information section for details.

SCL (E4): Serial Bus Clock Open-Drain Input (Can Be an Input and Output, if Clock Stretching is Enabled). A pull-up resistor to 3.3V is required in the application for digital communication to the SMBus master(s) that nominally drive this clock. The LTM4675 will never encounter scenarios where it would need to engage clock stretching unless SCL communication speeds exceed 100kHz—and even then, LTM4675 will not clock stretch unless clock stretching is enabled by means of setting MFR_CONFIG_ALL[1] = 1_b. The factory-default NVM configuration setting has MFR_CONFIG_ALL[1] = 0_b: clock stretching disabled. If communication on the bus at clock speeds above 100kHz is required, the user's SMBus master(s) need to implement clock stretching support to assure solid serial bus communications, and only then should MFR_CONFIG_ALL[1] be set to 1_b. When clock stretching is enabled, SCL becomes a bidirectional, open-drain output pin on LTM4675.

SDA (D4): Serial Bus Data Open-Drain Input and Output. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{ALERT}}$ (E3): Open-Drain Digital Output. A pull-up resistor to 3.3V is required in the application only if SMBALERT interrupt detection is implemented in one's SMBus system.

SHARE_CLK (H5): Share Clock, Bidirectional Open-Drain Clock Sharing Pin. Nominally 100kHz. Used for synchronizing the time base between multiple LTM4675s (and any other Linear Technology devices with a SHARE_CLK pin)—to realize well-defined rail sequencing and rail tracking. Tie the SHARE_CLK pins of all such devices together; all devices with a SHARE_CLK pin will synchronize to the fastest clock. A pull-up resistor to 3.3V is required when synchronizing the time base between multiple devices. If synchronizing the time base between multiple devices is not needed and MFR_CHAN_CONFIG$_n$[2] = 0_b, only then is a pull-up resistor not required.

$\overline{\text{GPIO}}_0$, $\overline{\text{GPIO}}_1$ (E2 and F2, Respectively): Digital, Programmable General Purpose Inputs and Outputs. Open-drain outputs and/or high impedance inputs. The LTM4675's factory-default NVM configurations for MFR_GPIO_PROPAGATE$_n$—0x6893—and MFR_GPIO_RESPONSE$_n$—0xC0—are such that: (1) when a channel-specific fault condition is detected—such as channel OT (overtemperature) or output UV/OV—the respective $\overline{\text{GPIO}}_n$ pin pulls logic low; (2) when a non-channel specific fault condition is detected—such as input OV or control IC OT—both $\overline{\text{GPIO}}_n$ pins pull logic low; (3) the LTM4675 ceases switching action on Channel 0 and 1 when its respective $\overline{\text{GPIO}}_n$ pin is logic low. Most significantly, this default configuration provides for graceful integration and inter-operation of LTM4675 with paralleled channel(s) of other LTM4675(s)—in terms of properly coordinating efforts in starting, ceasing, and resuming switching action and output voltage regulation, in unison—all without GUI intervention or the need to "custom-preprogram" module NVM contents. Pull-up resistors from $\overline{\text{GPIO}}_n$ to 3.3V are required for proper operation in the vast majority of applications. (Only if the LTM4675's MFR_GPIO_RESPONSE$_n$ value were set to 0x00 might pull-ups be unnecessary. See the Applications Information section for details.)

PIN FUNCTIONS

WP (K4): Write Protect Pin, Active High. An internal 10µA current source pulls this pin to V_{DD33}. If WP is open circuit or logic high, only I^2C writes to PAGE, OPERATION, CLEAR_FAULTS, MFR_CLEAR_PEAKS and MFR_EE_UNLOCK are supported. Additionally, individual faults can be cleared by writing 1_b's to bits of interest in registers prefixed with "STATUS". If WP is low, I^2C writes are unrestricted.

RUN_0, RUN_1 (F3 and F4, Respectively): Enable Run Input for Channels 0 and 1, Respectively. Open-drain input and output. Logic high on these pins enables the respective outputs of the LTM4675. These open-drain output pins hold the pin low until the LTM4675 is out of reset and SV_{IN} is detected to exceed VIN_ON. A pull-up resistor to 3.3V is required in the application. Do not pull RUN logic high with a low impedance source.

$TSNS_0$ (C3 and D3): Temperature Sensor Node for Channel 0. Pads C3 and D3 are connected to each other internal to the module. It is permissible to leave these pads electrically open circuit and to only solder these pins to mounting pads on the PC board for mechanical integrity purposes. However, it is acceptable to electrically connect C3 to D3 on the PC board.

$TSNS_{1a}$, $TSNS_{1b}$ (J3 and K3, Respectively): Channel 1 Temperature Excitation/Measurement and Thermal Sensor Pins, Respectively. In most applications, connect $TSNS_{1a}$ to $TSNS_{1b}$. This allows the LTM4675 to monitor the Power Stage Temperature of Channel 1. See the Applications Information section for information on how to use $TSNS_{1a}$ to monitor a temperature sensor external to the module, e.g., a PN junction on the die of a microprocessor.

$COMP_{0a}$, $COMP_{1a}$ (E6 and H6, Respectively): Current Control Threshold and Error Amplifier Compensation Nodes for Channels 0 and 1, Respectively. The trip threshold of each channel's current comparator increases with a respective rise in $COMP_{na}$ voltage. Small filter capacitors (22pF) internal to the LTM4675 on these COMP pins (terminated to SGND) introduce high frequency roll off of the error-amplifier response, yielding good noise rejection in the control loop. See $COMP_{0b}$/$COMP_{1b}$.

$COMP_{0b}$, $COMP_{1b}$ (D6 and J6, Respectively): Internal Loop Compensation Networks for Channels 0 and 1, Respectively. For the vast majority of applications, the internal, default loop compensation of the LTM4675 is suitable to apply "as is", and yields very satisfactory results: apply the default loop compensation to the control loops of Channels 0 and 1 by simply connecting $COMP_{0a}$ to $COMP_{0b}$ and $COMP_{1a}$ to $COMP_{1b}$, respectively. In contrast, when more specialized applications require a personal touch the optimization of control loop response, this can be easily accomplished by connecting (an) R-C network(s) from $COMP_{0a}$ and/or $COMP_{1a}$—terminated to SGND—and leaving $COMP_{0b}$ and/or $COMP_{1b}$ open, as desired.

SIMPLIFIED BLOCK DIAGRAM

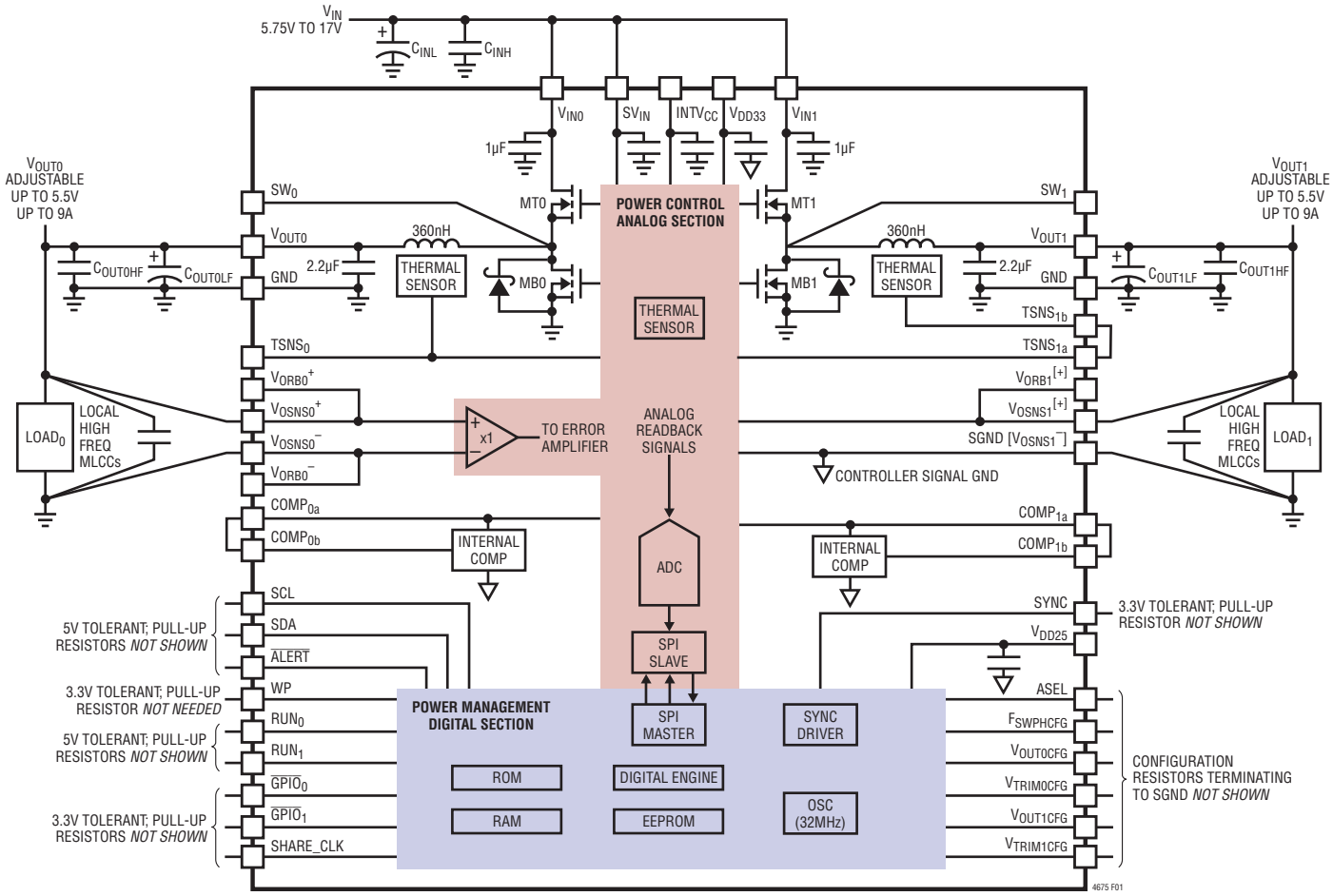


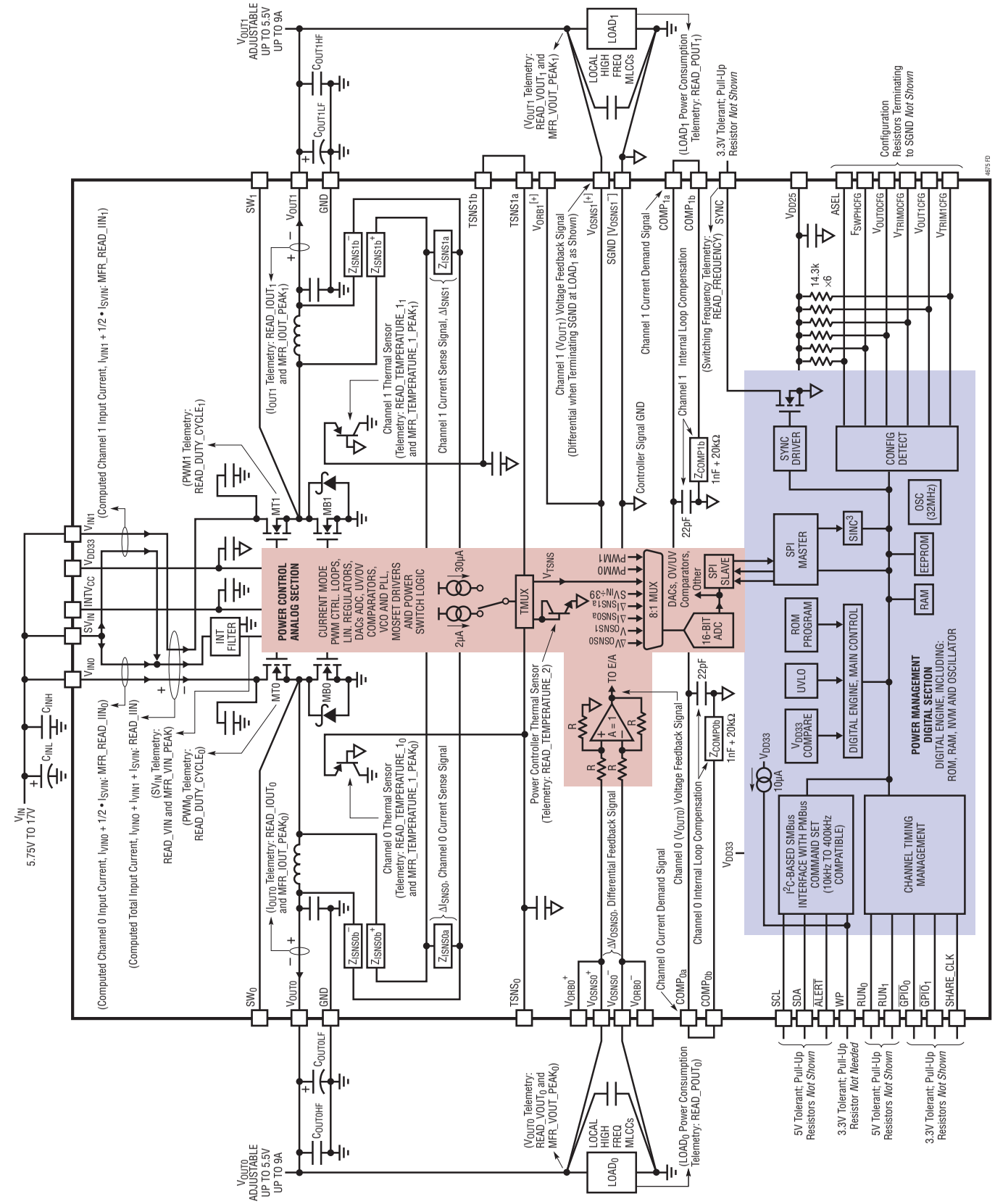
Figure 1. Simplified LTM4675 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Using Figure 1 configuration.

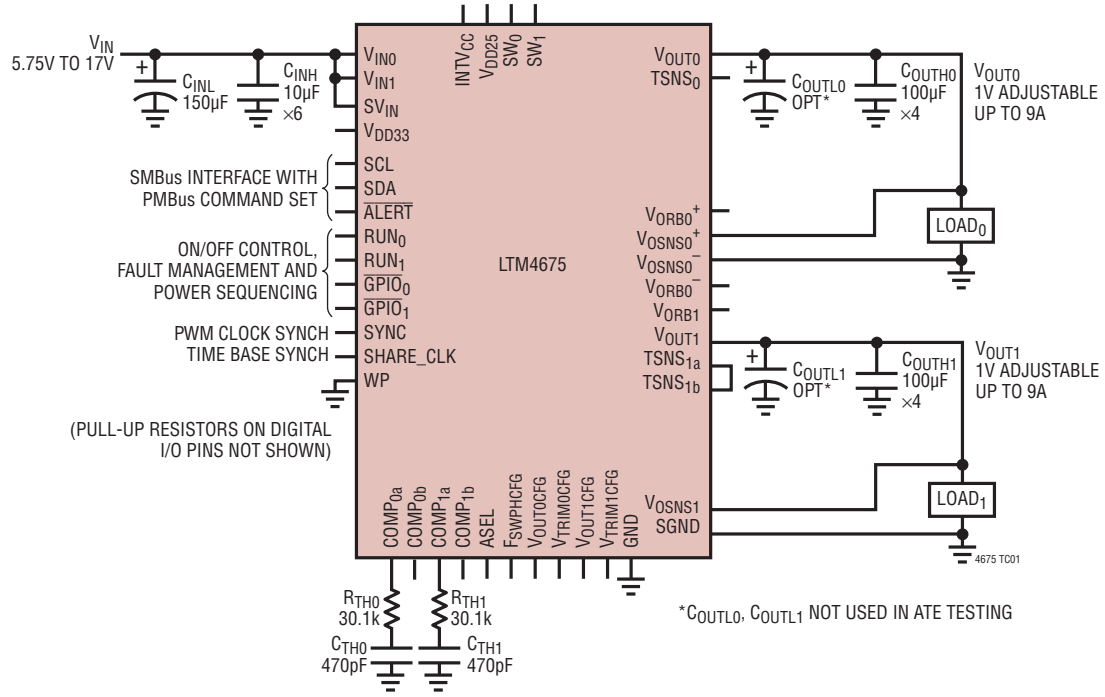
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{INH}	External High Frequency Input Capacitor Requirement (5.75V ≤ V_{IN} ≤ 17V, V_{OUTn} Commanded to 1.000V)	I_{OUT0} = 9A, 2 × 22µF, or 3 × 10µF I_{OUT1} = 9A, 2 × 22µF, or 3 × 10µF	30	44		µF
$C_{OUTn}HF$	External High Frequency Output Capacitor Requirement (5.75V ≤ V_{IN} ≤ 17V, V_{OUTn} Commanded to 1.000V)	I_{OUT0} = 9A I_{OUT1} = 9A		400 400		µF µF

FUNCTIONAL DIAGRAM

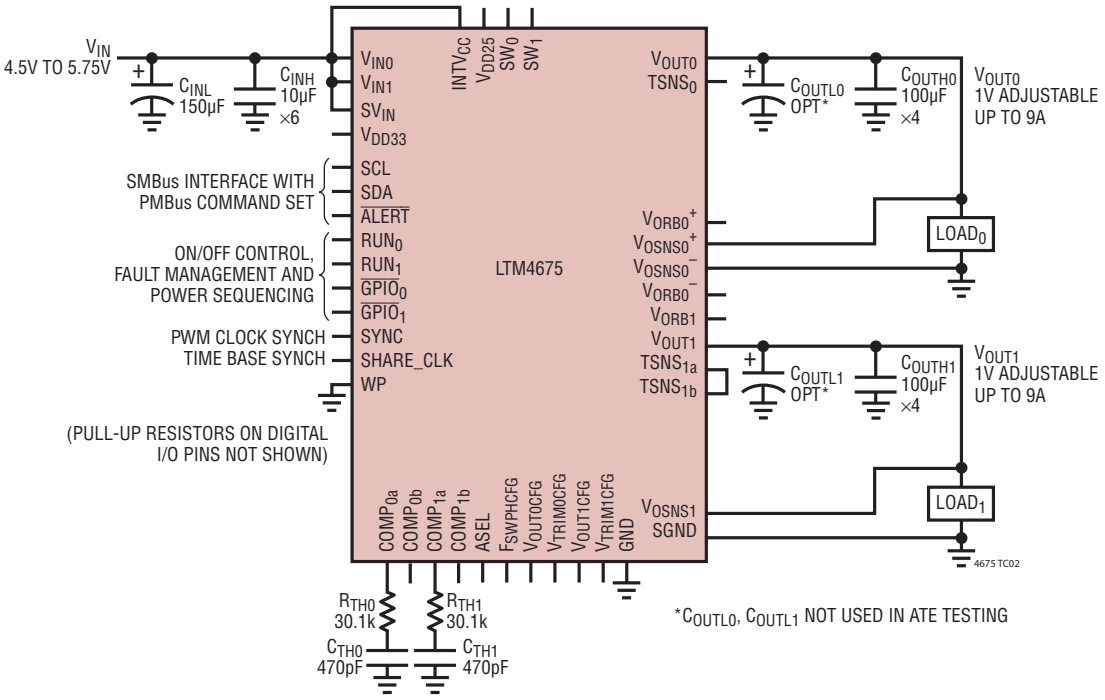


TEST CIRCUITS

Test Circuit 1. LTM4675 ATE High V_{IN} Operating Range Configuration, 5.75V ≤ V_{IN} ≤ 17V



Test Circuit 2. LTM4675 ATE Low V_{IN} Operating Range Configuration, 4.5V ≤ V_{IN} ≤ 5.75V



OPERATION

POWER MODULE INTRODUCTION

The LTM4675 is a highly configurable dual 9A output standalone nonisolated switching mode step-down DC/DC power supply with built-in EEPROM NVM (non-volatile memory) and I²C-based PMBus/SMBus 2-wire serial communication interface capable of 400kHz SCL bus speed. Two output voltages can be regulated (V_{OUT0}, V_{OUT1}—collectively, V_{OUTn}) with a few external input and output capacitors and pull-up resistors. Readback telemetry data of average input and output voltages and currents, Channel PWM duty cycles, and module temperatures are continually digitized cyclically by an integrated 16-bit ADC (analog-to-digital converter). Many fault thresholds and responses are customizable. Data can be autonomously saved to EEPROM when a fault occurs, and the resulting fault log can be retrieved over I²C at a later time, for analysis.

The LTM4675 provides precisely regulated output voltages between 0.6VDC to 5.5VDC (±0.5% above 1VDC, ±5mV below 1VDC). The target output voltage can be set according to pin-strapping resistors ($V_{OUTnCFG}$ and $V_{TRIMnCFG}$ pins), NVM/register settings, and altered on the fly via the I²C interface. The output voltage can be modified by the user at any time with a write to PMBus VOUT_COMMAND. Executing this command has a typical latency less than 10ms. Writes to PMBus OPERATION have a typical latency less than 1ms. The NVM factory-default switching frequency is 500kHz and the phase-interleaving angle between its two channels is 180°. Channel switching frequency, phase angle, and phase relationship with respect to the falling edge of the SYNC pin waveform can be configured according to a pin-strap resistor ($F_{SWPHCFG}$ pin) and NVM/register settings—though, not on the fly during regulation. The 7-bit I²C slave address of the module defaults to the value retrieved from MFR_ADDRESS[6:0] at power-up (factory default: 0x4F), but the least significant four bits of the address are set by resistor pin-strapping the ASEL pin. Bits[6:4] of MFR_ADDRESS can be written and stored to EEPROM. Between the ASEL resistor pin-strap and user-configurable MFS_ADDRESS[6:4], the LTM4675 can take on any 7-bit slave address desired. With the exception of the ASEL pin, the module can be configured to ignore all pin-strap resistors, if desired (see MFR_CONFIG_ALL[6]).

Table 1 provides a summary of LTM4675's supported PMBus commands. For details on the supported commands, payloads and data formats see Appendix C: PMBus Command Details.

For introductory information about the PMBus Specification, see Appendix A: Similarity Between PMBus, SMBus and I²C 2-Wire Interface. For information about the data communication link layer and timing diagrams, see Appendix B: PMBus Serial Digital Interface.

Major features of the LTM4675 strictly from a DC/DC converter power delivery point of view are as follows:

- Up to 9A Output Current Delivery from Each of Two Integrated Power Stages (See Front Page Figure)—or Up to 18A Output, Combined (See Figure 27 and Figure 34).
- Wide Input Voltage Range: DC/DC Step-Down Conversion from 5.75V to 17V Input (See Figure 60).
- DC/DC Step-Down Conversion from 4.5V to 5.75V Input, Connecting SV_{IN} to $INTV_{CC}$ (See Figure 27).
- DC/DC Step-Down Conversion Possible from Less Than 4.5V Input When an Auxiliary 5V Bias Supply Powers SV_{IN} and $INTV_{CC}$ (See Figure 29).
- Output Voltage Range: 0.5V to 5.5V on both V_{OUT0} and V_{OUT1}.
- Differential Remote Sensing of V_{OUT0} (V_{OSNS0}^+/V_{OSNS0}^-). For paralleled outputs, the V_{OSNS0}^+/V_{OSNS0}^- pin-pair can be configured as the feedback path for both V_{OUT0} and V_{OUT1} (see Figure 34 and, optionally, MFR_PWM_CONFIG[7]).
- Start-Up Into a Pre-Biased Load Without Sinking Current.
- Four LTM4675s Can Be Paralleled to Deliver Up to ~70A (See Figure 31).
- One LTM4675 Can Be Paralleled with Three LTM4620A or LTM4630 Modules to Deliver Up to 122A; Infer Rail Status and Telemetry of Paralleled LTM4620A or LTM4630 via the Sole LTM4675 (See Figure 32).
- Discontinuous Mode Operation Available for Higher Light-Load Efficiency (MFR_PWM_MODE$_n$[0]).
- Output Current Limit and Overvoltage Protection.
- Three Integrated Temperature Sensors, Over/Undertemperature Protection.
- Constant Frequency Peak Current Mode Control.

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- Configurable Switching Frequency, 250kHz to 1MHz; Synchronizable to External Clock; Seven Configurable Channel Phase Interleaving Settings.
- Internal Loop Compensation Provided; External Loop Compensation Can Be Applied, if Preferred.
- Low Profile (16mm × 11.9mm × 3.51mm) BGA Package Power Solution Requires Only Input and Output Capacitors; at Most, Nine Pull-Up Resistors for Open-Drain Digital Signals; at Most, Six Pull-Down Resistors to Configure All Possible Pin-Strapping Options.

Features of the LTM4675 that enable power system management, rail sequencing, and fault monitoring and reporting are as follows:

- I^2C-based PMBus/SMBus 2-Wire Serial Communication Interface (SDA, SCL) with $\overline{ALERT}$ Interrupt Pin, SCL Clock Capable of 400kHz Bus Communication Speeds with Clock Low Extending—or 100kHz, Otherwise.
- Configurable Output Voltage.
- Configurable Input Undervoltage Comparators (UVLO Rising, UVLO Falling).
- Configurable Switching Frequency.
- Configurable Current Limit.
- Configurable Output Over/Undervoltage Comparators.
- Configurable Turn-On and Turn-Off Delay Times.
- Configurable Output Ramp Rise and Fall Times.
- Non-Volatile Configuration Memory (NVM EEPROM) to Configure Aforementioned Settings, and More—Yielding Standalone Operation, if Desired, and Also Enabling In-Situ Changes to the LTM4675's Configuration in Embedded Designs.
- Monitoring and Reporting of Telemetry Data: Average Output and Input Currents and Voltages, Internal Temperatures, and Power Stage Duty Cycles—Continuously Digitized Cyclically by a 16-Bit ADC.
  - Peak Observed Output Current and Voltage, Input Voltage, and Module Temperatures Can Be Polled and Cleared/Reset.
  - ADC Latency Not Greater Than 100ms, Nominal.
  - Option to Monitor One External Temperature in Lieu of Channel 1 (V_{OUT1}) Module Power Stage Temperature.
- Monitoring, Reporting, and Configurable Response to Latching and Non-Latching Individual Fault and/or Warning Status, Including but Not Limited to:
  - Output Over/Undervoltages.
  - Input (SV_{IN}) Over/Undervoltages.
  - Module Input and Power Stage Output Overcurrents.
  - Module Power Stage Over/Under Temperatures.
  - Internal Control IC Overtemperature.
  - Communication, Memory and Logic (CML) Faults.
- Fault Logging Upon Detection of a Fault Condition. The LTM4675 Can Be Configured to Automatically Upload a Fault Log to Its NVM, Consisting of: an Uptime Counter, Peak Observed Telemetry, Telemetry Gathered from the Six Most Recent Rounds of Cyclical ADC Data Leading Up to the Detection of the Fault That Triggered Fault Log Writing, and Fault Status Associated with That ADC History.
- Two Configurable Open-Drain General Purpose Input/Output Pins ($\overline{GPIO_0}$, $\overline{GPIO_1}$), Which Can Be Used for:
  - Fault Reporting, e.g., as a System Interrupt Signal.
  - Coordinating Turn-On/Off of the LTM4675 in Multiphase/Multirail Systems.
  - Propagating an Unfiltered Power Good Signal (Output of a V_{OUTn} Undervoltage Comparator) to Command Turn-On/Off of a Downstream Rail.
- A Write Protect (WP) Pin and Configurable WRITE_PROTECT Register to Protect the Internal Configuration of RAM and NVM Against Unintended Changes via I^2C.
- Time-Base Interconnect (SHARE_CLK, 100kHz Heartbeat) for Synchronization in the Time Domain Between Multiple LTM4675s.
- Optional External Configuration Resistors (RCONFIGs) for Setting Start-Up Output Voltages, Switching Frequency and Channel-to-Channel Phase Interleaving Angle.
- Any 7-Bit Slave Address Can Be Assigned to the LTM4675 (0x4F Default), Configured by Resistor Pin Strapping the ASEL Pin and User-Editable Bits [7:4] of MFR_ADDRESS.

OPERATION

POWER MODULE CONFIGURABILITY AND READBACK DATA

This section of the data sheet describes all the configurable features and readable data of the LTM4675 accessible via I²C. The relevant command code name(s) are indicated by use of all capital letters, e.g., "VIN_ON". Refer to Table 1 and Appendix C: PMBus Command Details of this data sheet for details of the command code, payload size, data format and factory-default value. Specific register bits of some registers are indicated with the use of brackets, i.e., "[" and "]". The least significant bit (LSB) of a register is bit number zero, indicated by "[0]". The most significant bit of a byte-long (8-bit-long) register is bit number seven, indicated by "[7]". The most significant bit (MSB) of a word-long (16-bit-long) register is bit number fifteen, indicated by "[15]". Multiple bits of a register can be alluded to with the use of a colon, e.g., bits 2, 1 and 0 of the MFR_PWM_CONFIG register are indicated by "MFR_PWM_CONFIG[2:0]". Bits can take on values of 0_b or 1_b. The subscripted "$_b$" suffix indicates the number's value is in binary. Values in hexadecimal are indicated with a "0x" prefix. For example, decimal value "89" is indicated by 0x59 and 01011001_b (8-bit-long values), as well as 0x0059 and 0000000001011001_b (16-bit-long values).

One further shorthand notion the reader will notice is the italicized "$_n$" or "n". "n" can take on a value of 0 or 1—and provides an easy way to refer to registers which are paged commands, i.e., register names which have the same command code value but can be configured independently (or yield channel-specific telemetry) for Channel 0 (Page 0, or 0x00) vs Channel 1 (Page 1, or 0x01). Registers lacking an "$_n$" are therefore easily identified as being global in nature, i.e., common to both Channels/Outputs. For example, the switching frequency setting commanded by register FREQUENCY_SWITCH is common to both channels, and lacks "$_n$". Another example: the READ_VIN register contains the digitized input voltage as seen at the SV_{IN} pin, and SV_{IN} is unique, i.e., common to both Channels. In contrast, the nominal commanded output voltage is indicated by the register VOUT_COMMAND$_n$. The "$_n$" indicates that VOUT_COMMAND can be set differently for Channel 0 vs Channel 1. Executing the PAGE Command (Command Code 0x00) with payload 0x00 sets the LTM4675 to write/read data pertaining to Channel 0 in all subsequent I²C transactions until the Page is changed. Executing the PAGE Command with payload 0x01 sets the LTM4675 to write/read data pertaining to Channel 1 in all subsequent I²C transactions until the Page is changed. Executing the PAGE Command with payload 0xFF sets the LTM4675 to write data pertaining to Channels 0 and 1 in all subsequent I²C write transactions until the Page is changed. Reads from and writes to global registers do not require setting the Page to 0xFF. Reads from channel-specific (i.e., non-global) registers when the Page is set to 0xFF result in the LTM4675 reporting the value on Page 0x00 (i.e., Channel 0-specific data).

The list below itemizes aspects of the LTM4675 relating to power supply functions that are configurable by I²C communications—provided the state of the WP (write protect) pin and the WRITE_PROTECT register value permit the I²C writes—and by EEPROM settings:

- Output start-up voltages (VOUT_COMMAND$_n$), the maximum commandable output voltages (VOUT_MAX$_n$), output margin high (VOUT_MARGIN_HIGH$_n$) and margin low (VOUT_MARGIN_LOW$_n$) command voltages, and output over/undervoltage warning and fault thresholds (VOUT_OV_WARN_LIMIT$_n$, VOUT_OV_FAULT_LIMIT$_n$, VOUT_UV_WARN_LIMIT$_n$, and VOUT_UV_FAULT_LIMIT$_n$). Additionally, these values can be configured at SV_{IN} power-up according to resistor-pin strapping of the $V_{OUT0CFG}$, $V_{TRIM0CFG}$, $V_{OUT1CFG}$ and/or $V_{TRIM1CFG}$ pins, provided MFR_CONFIG_ALL[6] = 0_b.
- Output voltages, on the fly, including transition rate ($\Delta V/\Delta t$), VOUT_TRANSITION_RATE$_n$—either by I²C writes to the VOUT_COMMAND$_n$, VOUT_MARGIN_HIGH$_n$, or VOUT_MARGIN_LOW$_n$ registers, and/or to the OPERATION$_n$ register.
- Input undervoltage-lockout, rising (VIN_ON) and input undervoltage lockout, falling (VIN_OFF), based on the SV_{IN} pin voltage.
- Switching frequency (FREQUENCY_SWITCH) and channel phase-interleaving angle (MFR_PWM_CONFIG[2:0]). However, these parameters can be changed via I²C communications only when the LTM4675's channels are off, i.e., not switching. The LTM4675 synchronizes

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its switching frequency to a clock signal supplied to its SYNC pin when MFR_CONFIG_ALL[4]=1_b. These parameters can be configured at SV_{IN} power-up according to resistor-pin strapping of the $F_{SWPHCFG}$ pin, provided MFR_CONFIG_ALL[6] = 0_b.

- Output voltage turn-on and turn-off sequencing and associated watchdog timers, namely:
  - Output voltage turn-on delay time (the time delay from the LTM4675 being commanded to turn on, e.g., by the RUN_n pin toggling from logic low to high, before switching action commences. TON_DELAY_n).
  - Output voltage soft-start ramp-up time (TON_RISE_n).
  - The amount of time ($TON\_MAX\_FAULT\_LIMIT_n$) permitted to elapse after the LTM4675 is commanded to turn on, e.g., by the RUN_n pin toggling from logic low to high, after which, if the output voltage fails to exceed the output undervoltage fault threshold ($VOUT\_UV\_FAULT\_LIMIT_n$), the LTM4675's output (V_{OUTn}) is declared to have not come up in a timely manner.
  - The LTM4675's response to any such aforementioned $TON\_MAX\_FAULT\_LIMIT_n$ event ($TON\_MAX\_FAULT\_RESPONSE_n$).
  - Output voltage soft-stop ramp-down time ($TOFF\_FALL_n$).
  - Output voltage turn-off delay time (the time delay from the LTM4675 being commanded to turn off, e.g., by the RUN_n pin toggling from logic high to low, before switching action ceases. $TOFF\_DELAY_n$).
  - When commanded to turn off its output—or, when turning off its output in response to a fault—configuring whether the LTM4675's output (V_{OUTn}) becomes high impedance ("High-Z" or "three state"—turning off both MT*n* and MB*n* in the power stage). ("Immediate Off", $ON\_OFF\_CONFIG_n$[0] = 1_b vs configuring the output voltage to be ramped down according to $TOFF\_FALL_n$ and/or $TOFF\_DELAY_n$ settings, $ON\_OFF\_CONFIG_n$[0] = 0_b).
  - The amount of time ($TOFF\_MAX\_WARN\_LIMIT_n$) permitted to elapse after the LTM4675 is supposed to have turned off its output, i.e., at the end of the period dictated by $TOFF\_FALL_n$, after which, If the output voltage has not fallen below 12.5% of the former target voltage of regulation, the LTM4675's output (V_{OUTn}) is declared to have not powered down in a timely manner.
- Configurable output voltage restart time. Subsequent to the RUN_n pin being pulled low, the LTM4675 pulls RUN_n logic low, itself, and the output cannot be restarted until a minimum time has elapsed—the restart delay time. This delay assures proper sequencing of all system rails. The minimum restart delay processed by the LTM4675 is the longer of ($TOFF\_DELAY_n$ + $TOFF\_FALL_n$ + 136ms) vs the commanded $MFR\_RESTART\_DELAY_n$ register value. At the end of this delay, the LTM4675 releases its RUN_n pin.
- Configurable fault-hiccup retry delay time. When a fault occurs in which the LTM4675's fault response behavior to that fault is to reattempt power-up of its output voltage after said fault ceases to be present (e.g., "Infinite Retry"), the delay time for the LTM4675 to re-engage switching action is the longer of the $MFR\_RETRY\_DELAY_n$ time vs the time required for the output to decay below 12.5% of the formerly commanded output voltage value (unless this lattermost criteria, i.e., requiring the output to decay below 12.5% is negated by the setting of $MFR\_CHAN\_CONFIG_n$[0] to "1_b"—which is the LTM4675's factory-NVM default setting).
- Output over/undervoltage fault responses ($VOUT\_OV\_FAULT\_RESPONSE_n$, $VOUT\_UV\_FAULT\_RESPONSE_n$).
- Time-averaged current limit warning and instantaneous peak (cycle-by-cycle) fault thresholds, and fault response ($IOUT\_OC\_WARN\_LIMIT_n$, $IOUT\_OC\_FAULT\_LIMIT_n$, $IOUT\_OC\_FAULT\_RESPONSE_n$).
- Channel (V_{OUT0}, V_{OUT1}) overtemperature warning and fault thresholds, and fault response ($OT\_WARN\_LIMIT_n$, $OT\_FAULT\_LIMIT_n$, $OT\_FAULT\_RESPONSE_n$).
- Channel (V_{OUT0}, V_{OUT1}) undertemperature fault thresholds and fault response ($UT\_FAULT\_LIMIT_n$, $UT\_FAULT\_RESPONSE_n$).
- Input overvoltage fault threshold and response (VIN_OV_FAULT_LIMIT, VIN_OV_FAULT_RESPONSE), based on the SV_{IN} pin voltage.

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- Input undervoltage warning threshold (VIN_UV_WARN_LIMIT) based on the SV_{IN} pin voltage.
- Module input overcurrent warning threshold (IIN_OC_WARN_LIMIT)

The control IC within the LTM4675 module ceases switching action if control IC temperature exceeds 160°C (Note 12). The control IC resumes operation after a 10°C cool-down hysteresis. Note that these typical parameters are based on measurements in a lab oven and are not production tested. This overtemperature protection is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

TIME-AVERAGED AND PEAK READBACK DATA

Time-averaged telemetry readback data accessible via I^2C communications follow:

- Channel output current (READ_IOUT$_n$) and peak observed value of READ_IOUT$_n$ (MFR_IOUT_PEAK$_n$).
- Channel output voltage (READ_VOUT$_n$) and peak observed value of READ_VOUT$_n$ (MFR_VOUT_PEAK$_n$).
- Channel output power (READ_POUT$_n$).
- Channel input current (MFR_READ_IIN$_n$) and module input current (READ_IIN).
- Channel temperatures (READ_TEMPERATURE_1$_n$) and peak observed values of READ_TEMPERATURE_1$_n$ (MFR_TEMPERATURE_1_PEAK$_n$).
- Control IC temperature (READ_TEMPERATURE_2) and peak observed value (MFR_TEMPERATURE_2_PEAK).
- Input voltage (READ_VIN), based on the voltage of the SV_{IN} pin, and peak observed value of READ_VIN (MFR_VIN_PEAK).
- Channel topside power MOSFET (MTn) duty cycle (READ_DUTY_CYCLE$_n$)

Digitized cyclical telemetry is available at a 10Hz update rate, typical. Through the use of the MFR_ADC_CONTROL command, some signals of interest can be digitized more frequently—up to a 125Hz update rate, typical. Availability of newly digitized telemetry data can be made known via the MFR_ADC_TELEMETRY_STATUS command.

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Peak observed values of telemetry readback data can be cleared with the MFR_CLEAR_PEAKS I^2C command, provided the WRITE_PROTECT register value permits it. (Executing MFR_CLEAR_PEAKS can be performed regardless of the state of the WP pin.)

Details on the LTM4675's Fault Log Feature follow:

- Fault logging is enabled when MFR_CONFIG_ALL[7] = 1_b.
- A fault log is present in NVM when STATUS_MFR_SPECIFIC$_n$[3]Reports "1_b", which is propagated to the MFR Bit (Bit 12) of the STATUS_WORD register.
- Retrieving fault log data, if present, is performed with the MFR_FAULT_LOG command. 147 bytes of data are retrieved using the PMBus-defined variant to the SMBus block read protocol.
- The fault log contents in NVM, if present, are cleared by executing the MFR_FAULT_LOG_CLEAR command.
- The fault log will not be written if a fault log is already present in NVM.
- The LTM4675 can be forced to write a fault log to its NVM by executing the MFR_FAULT_LOG_STORE command; the LTM4675 will behave as if a channel faulted off. Note the command is NACKed and a CML fault is reported if a fault log is already present at the time of executing MFR_FAULT_LOG_STORE.

When an external stimulus pulls the LTM4675's $\overline{GPIO}_n$ pin(s) logic low, the respective channel ($V_{OUT}n$) either: takes no action on it, i.e., ignores it completely—if MFR_GPIO_RESPONSE$_n$ = 0x00; or, turns off immediately,