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16-Bit IF/Baseband Receiver Subsystem

FEATURES

- **Integrated 16-Bit, High-Speed ADC, Passive Filter and Fixed Gain Differential Amplifier**
- **Up to 300MHz IF Range**
  Lowpass and Bandpass Filter Versions
- **Low Noise, Low Distortion Amplifiers**
  Fixed Gain: 8dB, 14dB, 20dB or 26dB
  50Ω, 200Ω or 400Ω Input Impedance
- **75dB SNR, 83dB SFDR (LTM9001-AD)**
- **Integrated Bypass Capacitance, No External Components Required**
- Optional Internal Dither
- Optional Data Output Randomizer
- LVDS or CMOS Outputs
- 3.3V Single Supply
- Power Dissipation: 1.65W
- Clock Duty Cycle Stabilizer
- 11.25mm × 11.25mm × 2.32mm LGA Package

APPLICATIONS

- Telecommunications
- High Sensitivity Receivers
- Cellular Base Stations
- Spectrum Analyzers

DESCRIPTION

The LTM®9001 is an integrated system in a package (SiP) that includes a high-speed 16-bit A/D converter, matching network, anti-aliasing filter and a low noise, differential amplifier with fixed gain. It is designed for digitizing wide dynamic range signals with an intermediate frequency (IF) range up to 300MHz. The amplifier allows either AC- or DC-coupled input drive. A lowpass or bandpass filter network can be implemented with various bandwidths. Contact Linear Technology regarding semi-custom configurations.

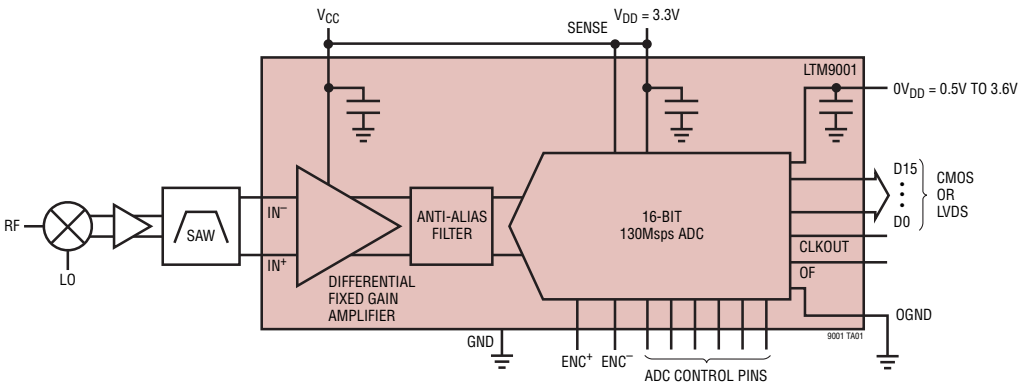
The LTM9001 is perfect for IF receivers in demanding communications applications, with AC performance that includes 72dBFS noise floor and 82dB spurious free dynamic range (SFDR) at 162.5MHz (LTM9001-AA).

The digital outputs can be either differential LVDS or single-ended CMOS. There are two format options for the CMOS outputs: a single bus running at the full data rate or two demultiplexed buses running at half data rate. A separate output power supply allows the CMOS output swing to range from 0.5V to 3.3V.

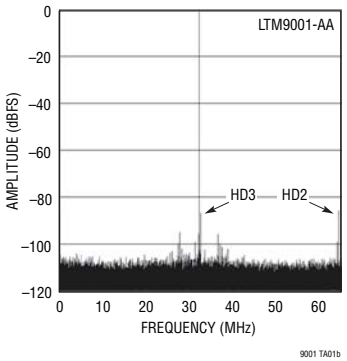
The differential ENC+ and ENC– inputs may be driven with a sine wave, PECL, LVDS, TTL or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycles.

TYPICAL APPLICATION

Simplified IF Receiver Channel



64k Point FFT, f_{IN} = 162.4MHz, –1dBFS, PGA = 1

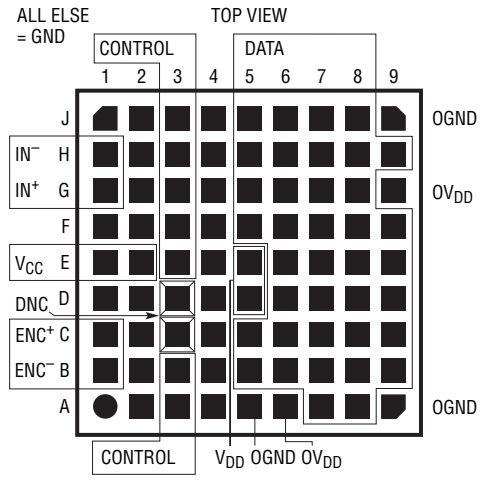


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 3.6V
Supply Voltage (V_{DD}) ..... –0.3V to 4V
Digital Output Supply Voltage (OV_{DD}) ..... –0.3V to 4V
Analog Input Current (IN^+, IN^-) ..... ±10mA
Digital Input Voltage
(Except AMPSHDN) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage
(AMPSHDN) ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)
Operating Temperature Range
LTM9001C ..... 0°C to 70°C
LTM9001I ..... –40°C to 85°C
Storage Temperature Range ..... –45°C to 125°C
Maximum Junction Temperature ..... 125°C

PIN CONFIGURATION



LGA PACKAGE
T_{JMAX} = 125°C, θ_{JA} = 15°C/W, θ_{JCtop} = 19°C/W
θ_{JA} DERIVED FROM 60mm × 70mm PCB WITH 4 LAYERS
WEIGHT = 0.71g

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9001CV-AA#PBF	LTM9001V-AA	81-Lead (11.25mm × 11.25mm × 2.3mm) LGA	0°C to 70°C
LTM9001IV-AA#PBF	LTM9001V-AA	81-Lead (11.25mm × 11.25mm × 2.3mm) LGA	–40°C to 85°C
LTM9001CV-AD#PBF	LTM9001V-AD	81-Lead (11.25mm × 11.25mm × 2.3mm) LGA	0°C to 70°C
LTM9001IV-AD#PBF	LTM9001V-AD	81-Lead (11.25mm × 11.25mm × 2.3mm) LGA	–40°C to 85°C
LTM9001CV-BA#PBF	LTM9001V-BA	81-Lead (11.25mm × 11.25mm × 2.3mm) LGA	0°C to 70°C
LTM9001IV-BA#PBF	LTM9001V-BA	81-Lead (11.25mm × 11.25mm × 2.3mm) LGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G_{DIFF}	Gain	DC, LTM9001-AA f_{IN} = 162.5MHz (Note 3)	●	19.1	19.7 19	20.3	dB dB
		DC, LTM9001-AD f_{IN} = 70MHz (Note 3)	●	13.4	14 13.5	14.7	dB dB
		DC, LTM9001-BA f_{IN} = 140MHz (Note 3)	●	7.1	8.2 7.8	9.4	dB dB
G_{TEMP}	Gain Temperature Drift	V_{IN} = Maximum, (Note 3)			2		mdB/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{INCM}	Input Common Mode Voltage Range	$(IN^+ + IN^-)/2$			1.0–1.6		V
V_{IN}	Input Voltage Range at –1dBFS	LTM9001-AA at 162.5MHz LTM9001-AD at 70MHz LTM9001-BA at 140MHz			233 424 820		mV_{P-P} mV_{P-P} mV_{P-P}
R_{INDIFF}	Differential Input Impedance	LTM9001-AA LTM9001-AD LTM9001-BA			200 200 400		Ω Ω Ω
C_{INDIFF}	Differential Input Capacitance	Includes Parasitic			1		pF
V_{OS}	Offset Error (Note 6)	Including Amplifier and ADC (LTM9001-AA) Including Amplifier and ADC (LTM9001-AD) Including Amplifier and ADC (LTM9001-BA)	● ● ●	–8 –11 –20	–3.2 –6 –10	–0.5 –0.5 –0.5	mV mV mV
	Offset Drift	Including Amplifier and ADC			±10		µV/°C
	Full-Scale Drift	Internal Reference External Reference			±30 ±15		ppm/°C ppm/°C
CMRR	Common Mode Rejection Ratio				60		dB
I_{SENSE}	SENSE Input Leakage Current	0V < SENSE < V_{DD}	●	–3		3	µA
I_{MODE}	MODE Pin Pull-Down Current to GND				10		µA
I_{LVDS}	LVDS Pin Pull-Down Current to GND				10		µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				70		fs_{RMS}

CONVERTER CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	16			Bits
Integral Linearity Error	Differential Input LTM9001-Ax (Notes 5, 7) Differential Input LTM9001-BA (Notes 5, 7)	● ●		±2.4	±8 ±10	LSB LSB
Differential Linearity Error	Differential Input (Notes 5, 7)	●		±0.3	±1	LSB
Transition Noise	External Reference			1		LSB_{RMS}

DYNAMIC ACCURACY

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	162.5MHz Input (PGA = 0) LTM9001-AA 162.5MHz Input (PGA = 1) LTM9001-AA	 ●	 67.2	72 68.5		dBFS dBFS
		70MHz Input (PGA = 0) LTM9001-AD 70MHz Input (PGA = 1) LTM9001-AD	●	71.2	75 72		dBFS dBFS
		140MHz Input (PGA = 0) LTM9001-BA 140MHz Input (PGA = 1) LTM9001-BA	●	67	69.2 67.2		dBFS dBFS

DYNAMIC ACCURACY

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SFDR	Spurious Free Dynamic Range, 2nd or 3rd Harmonic	162.5MHz Input (PGA = 0) LTM9001-AA			78		dBc
		162.5MHz Input (PGA = 1) LTM9001-AA	●	72	82		dBc
		70MHz Input (PGA = 0) LTM9001-AD	●	72.6	83		dBc
		70MHz Input (PGA = 1) LTM9001-AD			86		dBc
		140MHz Input (PGA = 0) LTM9001-BA	●	64	72		dBc
		140MHz Input (PGA = 1) LTM9001-BA			82		dBc
SFDR	Spurious Free Dynamic Range 4th or Higher	162.5MHz Input (PGA = 0) LTM9001-AA			95		dBc
		162.5MHz Input (PGA = 1) LTM9001-AA	●	86	95		dBc
		70MHz Input (PGA = 0) LTM9001-AD	●	84.5	95		dBc
		70MHz Input (PGA = 1) LTM9001-AD			98		dBc
		140MHz Input (PGA = 0) LTM9001-BA	●	86	95		dBc
		140MHz Input (PGA = 1) LTM9001-BA			104		dBc
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	162.5MHz Input (PGA = 0) LTM9001-AA			71.4		dBFS
		162.5MHz Input (PGA = 1) LTM9001-AA	●	67	68		dBFS
		70MHz Input (PGA = 0) LTM9001-AD	●	71.2	74.3		dBFS
		70MHz Input (PGA = 1) LTM9001-AD			72		dBFS
		140MHz Input (PGA = 0) LTM9001-BA	●	64	67.5		dBFS
		140MHz Input (PGA = 1) LTM9001-BA			66.4		dBFS
SFDR	Spurious Free Dynamic Range at –25dBFS, Dither “OFF”	162.5MHz Input (PGA = 0) LTM9001-AA			90		dBFS
		162.5MHz Input (PGA = 1) LTM9001-AA			93		dBFS
	Spurious Free Dynamic Range at –15dBFS, Dither “OFF”	70MHz Input (PGA = 0) LTM9001-AD			85		dBFS
		70MHz Input (PGA = 1) LTM9001-AD			87		dBFS
	Spurious Free Dynamic Range at –15dBFS, Dither “OFF”	140MHz Input (PGA = 0) LTM9001-BA			91		dBFS
		140MHz Input (PGA = 1) LTM9001-BA			92		dBFS
SFDR	Spurious Free Dynamic Range at –25dBFS, Dither “ON”	162.5MHz Input (PGA = 0) LTM9001-AA			95		dBFS
		162.5MHz Input (PGA = 1) LTM9001-AA	●	90	100		dBFS
	Spurious Free Dynamic Range at –15dBFS, Dither “ON”	70MHz Input (PGA = 0) LTM9001-AD	●	90	92		dBFS
		70MHz Input (PGA = 1) LTM9001-AD			88		dBFS
	Spurious Free Dynamic Range at –15dBFS, Dither “ON”	140MHz Input (PGA = 0) LTM9001-BA	●	90	95		dBFS
		140MHz Input (PGA = 1) LTM9001-BA			96		dBFS
IMD_3	Third Order Intermodulation Distortion; 1MHz Tone Spacing, 2 Tones at –7dBFS	f_{IN} = 162.5MHz LTM9001-AA			–78		dB
		f_{IN} = 70MHz LTM9001-AD			–84		dB
		f_{IN} = 140MHz LTM9001-BA			–84		dB
IIP_3	Equivalent Third Order Input Intercept Point, 2 Tone	f_{IN} = 162.5MHz LTM9001-AA			24		dBm
		f_{IN} = 70MHz LTM9001-AD			26.5		dBm
		f_{IN} = 140MHz LTM9001-BA			29.2		dBm

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Encode Inputs (ENC+, ENC–)							
V_{ID}	Differential Input Voltage		●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set			1.6		V
		Externally Set		1.2		3.1	V
R_{IN}	Input Resistance				100		Ω
C_{IN}	Input Capacitance	(Note 7)			3		pF

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (DITH, PGA, ADCSHDN, RAND)							
V_{IH}	High Level Input Voltage	V_{DD} = 3.3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3.3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Input Capacitance	(Note 7)			1.5		pF
Logic Inputs (AMPSHDN)							
V_{IH}	High Level Input Voltage	V_{CC} = 3.3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.3V	●			0.8	V
I_{IH}	Input High Current	V_{IN} = 2V			1.3		µA
I_{IL}	Input Low Current	V_{IN} = 0.8V			0.1		µA
C_{IN}	Input Capacitance	(Note 7)			1.5		pF
Logic Outputs (CMOS Mode)							
OV_{DD} = 3.3V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –10µA V_{DD} = 3.3V, I_O = –200µA	 ●	 3.1	3.299 3.29		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 10µA V_{DD} = 3.3V, I_O = 1.6mA	 ●		0.01 0.1	 0.4	V V
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3.3V			50		mA
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 1.6mA			0.1		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 1.6µA			0.1		V
Logic Outputs (LVDS Mode)							
Standard LVDS							
V_{OD}	Differential Output Voltage	100Ω Differential Load	●	247	350	454	mV
V_{OS}	Output Common Mode Voltage	100Ω Differential Load	●	1.125	1.2	1.375	V
Low Power LVDS							
V_{OD}	Differential Output Voltage	100Ω Differential Load	●	125	175	250	mV
V_{OS}	Output Common Mode Voltage	100Ω Differential Load	●	1.125	1.2	1.375	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	ADC Analog Supply Voltage	(Note 8)	●	3.135	3.3	3.465	V
V_{CC}	Amplifier Supply Voltage			2.85		3.5	V
I_{CC}	Amplifier Supply Current		●		100	136	mA
P_{SHDN}	Total Shutdown Power	AMPSHDN = ADCSHDN = 3.3V			10		mW

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Standard LVDS Output Mode							
OV_{DD}	Output Supply Voltage	(Note 8)	●	3	3.3	3.6	V
I_{VDD}	Analog Supply Current	LTM9001-Ax LTM9001-BA	● ●		400 465	500 550	mA mA
I_{OVDD}	Output Supply Current		●		74	90	mA
P_{DISS}	Power Dissipation	LTM9001-Ax LTM9001-BA	● ●		1564 1779	1947 2112	mW mW
Low Power LVDS Output Mode							
OV_{DD}	Output Supply Voltage	(Note 8)	●	3	3.3	3.6	V
I_{VDD}	Analog Supply Current	LTM9001-Ax LTM9001-BA	● ●		400 465	500 550	mA mA
I_{OVDD}	Output Supply Current		●		41	50	mA
P_{DISS}	Power Dissipation	LTM9001-Ax LTM9001-BA	● ●		1455 1670	1815 1980	mW mW
CMOS Output Mode							
OV_{DD}	Output Supply Voltage	(Note 8)	●	0.5		3.6	V
I_{VDD}	Analog Supply Current	LTM9001-Ax LTM9001-BA	● ●		380 460	450 530	mA mA
P_{DISS}	ADC Power Dissipation	LTM9001-Ax LTM9001-BA	● ●		1320 1584	1650 1914	mW mW
$P_{DISS(TOTAL)}$	Total Power Dissipation	LTM9001-Ax LTM9001-BA			1650 1914		mW mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency (Note 8)	LTM9001-Ax LTM9001-BA	● ●	1 1		130 160	MHz MHz
t_L	ENC Low Time (Note 7)	Duty Cycle Stabilizer Off (LTM9001-Ax) Duty Cycle Stabilizer Off (LTM9001-BA) Duty Cycle Stabilizer On (LTM9001-Ax) Duty Cycle Stabilizer On (LTM9001-BA)	● ● ● ●	3.65 2.97 2.6 2.1	3.846 3.125 3.846 3.125	1000 1000 1000 1000	ns ns ns ns
t_H	ENC High Time (Note 7)	Duty Cycle Stabilizer Off (LTM9001-Ax) Duty Cycle Stabilizer Off (LTM9001-BA) Duty Cycle Stabilizer On (LTM9001-Ax) Duty Cycle Stabilizer On (LTM9001-BA)	● ● ● ●	3.65 2.97 2.6 2.1	3.846 3.125 3.846 3.125	1000 1000 1000 1000	ns ns ns ns
LVDS Output Mode (Standard and Low Power)							
t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.5	4	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1.3	2.5	4	ns
t_{SKEW}	DATA to CLKOUT Skew	(t_C – t_D) (Note 7)	●	–0.6	0	0.6	ns
t_{RISE}	Output Rise Time				0.5		ns
t_{FALL}	Output Fall Time				0.5		ns
	Data Latency				7		Cycles

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Output Mode							
t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.7	4	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1.3	2.7	4	ns
t_{SKEW}	DATA to CLKOUT Skew	(t_C – t_D) (Note 7)	●	–0.6	0	0.6	ns
	Data Latency	Full Rate CMOS Demuxed			7 7		Cycles Cycles

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: Gain is measured from IN^+/IN^- through the ADC. The amplifier gain is attenuated by the filter, (See the typical performance characteristics section for "IF Frequency Response").

Note 4: V_{CC} = V_{DD} = 3.3V, f_{SAMPLE} = maximum sample frequency, LVDS outputs, differential ENC^+/ENC^- = $2V_{P-P}$ with 1.6V common mode, input range = –1dBFS with PGA = 0 with differential drive, AC-coupled inputs, unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a "best fit straight line" to the transfer curve. The deviation is measured from the center of the quantization band.

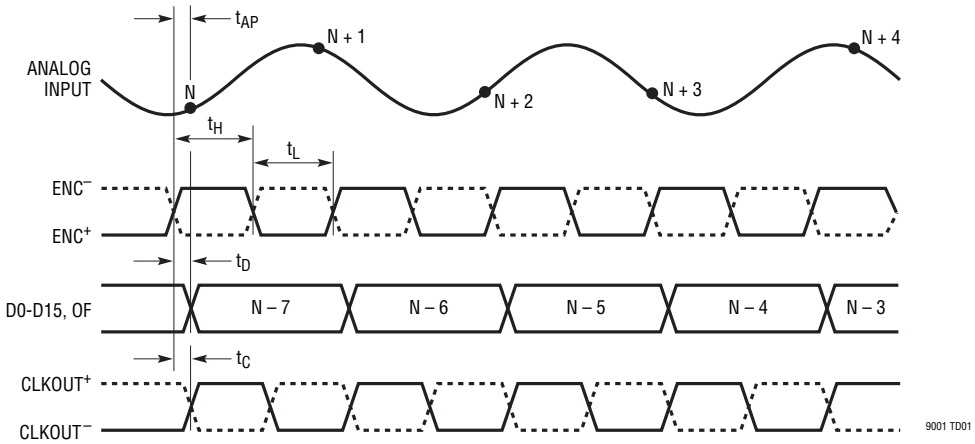
Note 6: Offset error is the voltage applied between the IN^+ and IN^- pins required to make the output code flicker between 0000 0000 0000 0000 and 1111 1111 1111 1111.

Note 7: Guaranteed by design, not subject to test.

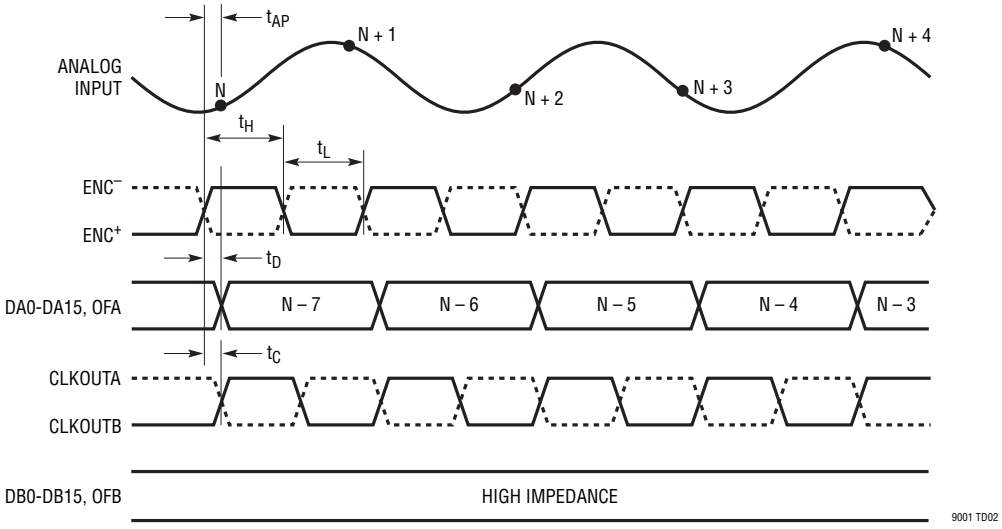
Note 8: Recommended operating conditions.

TIMING DIAGRAM

LVDS Output Mode Timing
All Outputs are Differential and Have LVDS Levels

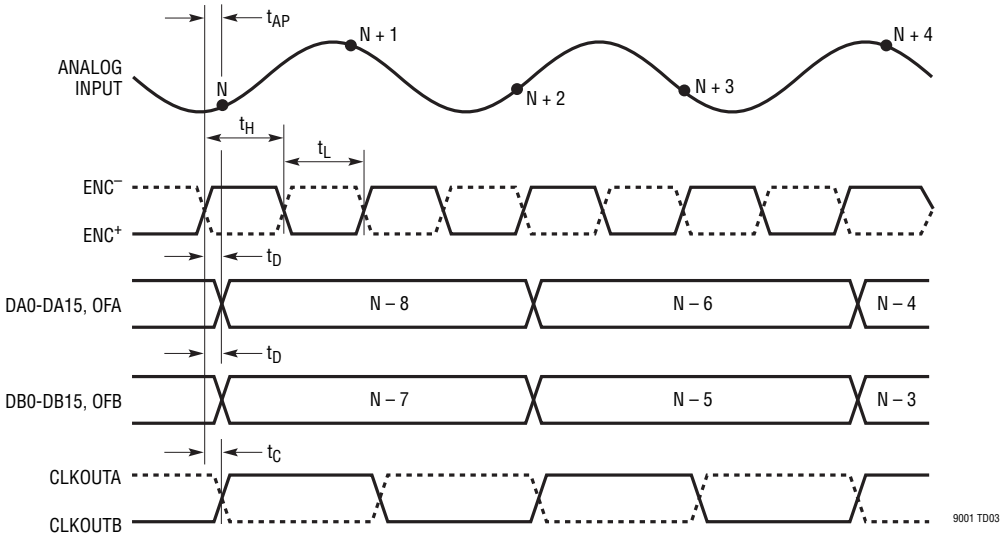


Full-Rate CMOS Output Mode Timing
All Outputs are Single-Ended and Have CMOS Levels



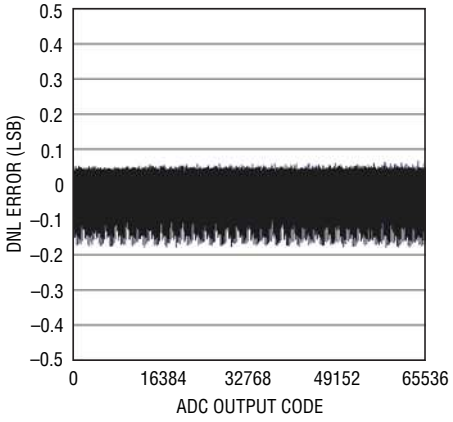
TIMING DIAGRAM

Demultiplexed CMOS Output Mode Timing
All Outputs are Single-Ended and Have CMOS Levels

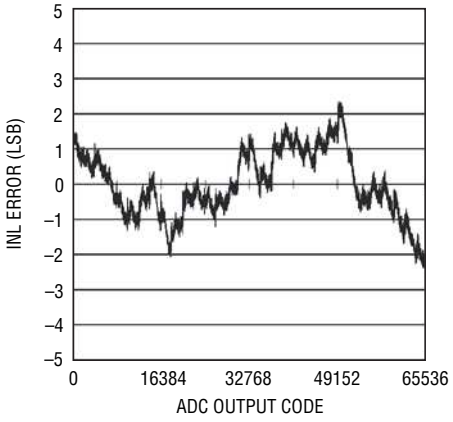


TYPICAL PERFORMANCE CHARACTERISTICS (LTM9001-AA)

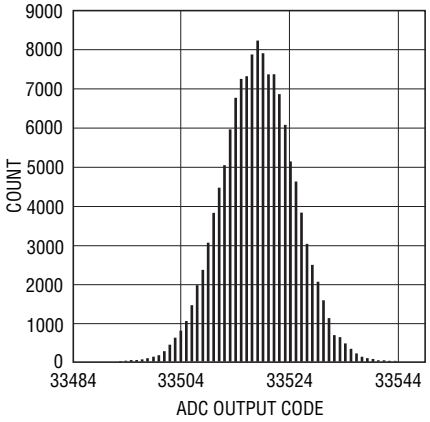
Differential Non-Linearity (DNL) vs Output Code



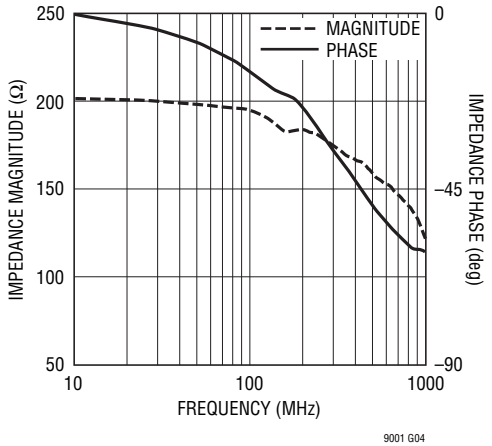
Best Fit Integral Non-Linearity (INL) vs Output Code



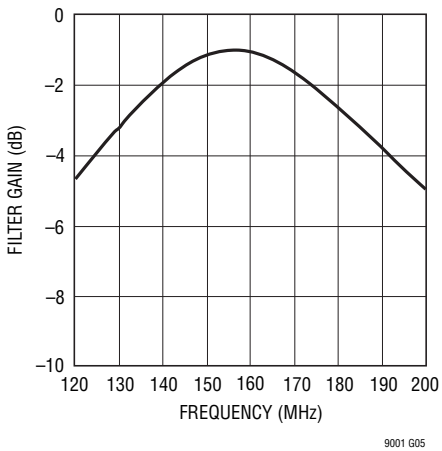
Shorted Inputs Histogram with 130k Samples



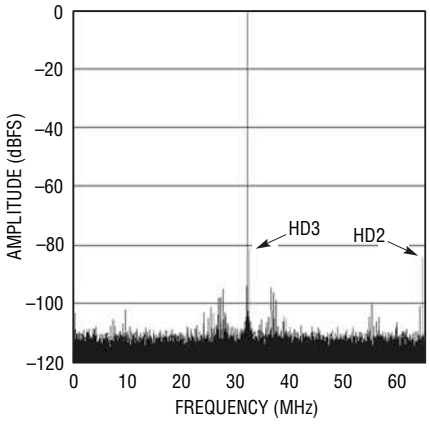
Input Impedance vs Frequency



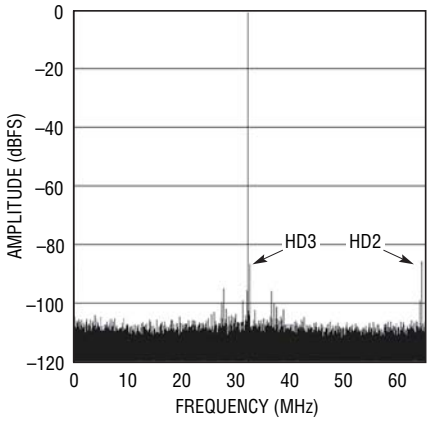
IF Frequency Response



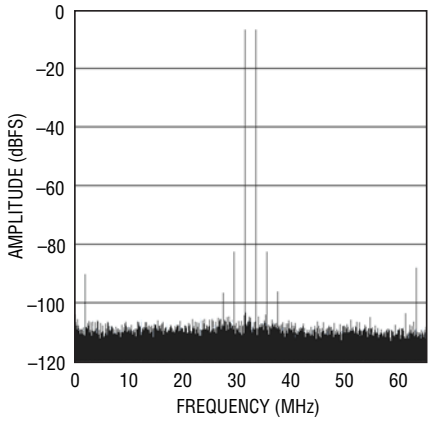
64k Point FFT, f_{IN} = 162.4MHz, –1dBFS, PGA = 0, RAND "Off", Dither "Off"



64k Point FFT, f_{IN} = 162.4MHz, –1dBFS, PGA = 1, RAND "Off", Dither "Off"

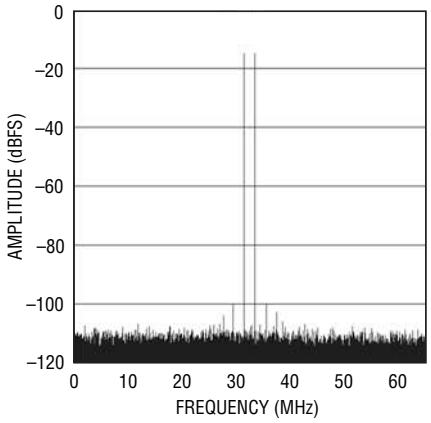


64k Point 2-Tone FFT, f_{IN} = 161.5MHz, and 163.5MHz, –7dBFS, PGA = 0, RAND "Off", Dither "Off"

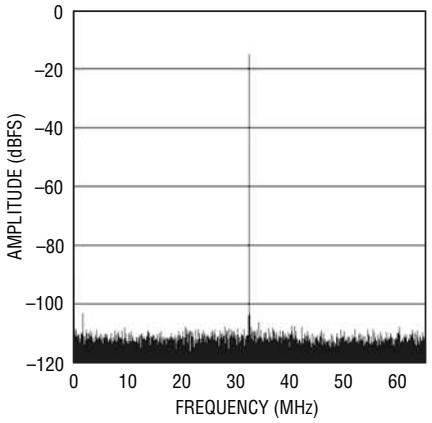


TYPICAL PERFORMANCE CHARACTERISTICS (LTM9001-AA)

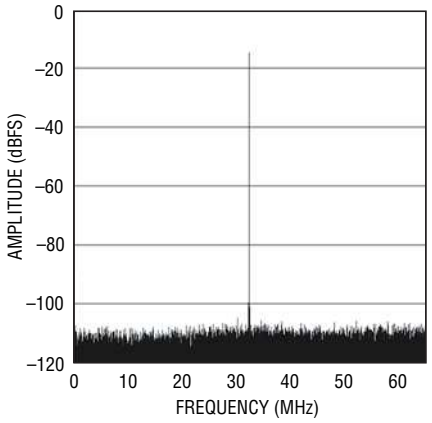
64k Point 2-Tone FFT, f_{IN} = 161.5MHz, and 163.5MHz, –15dBFS, PGA = 0, RAND "Off", Dither "Off"



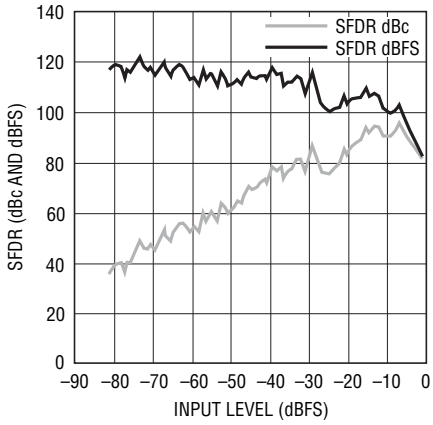
64k Point FFT, f_{IN} = 162.4MHz, –15dBFS, PGA = 0, RAND "Off", Dither "Off"



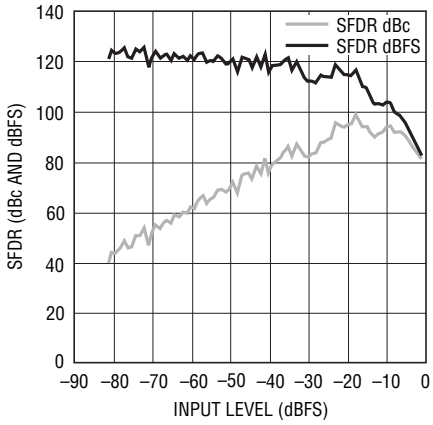
64k Point FFT, f_{IN} = 162.4MHz, –15dBFS, PGA = 0, RAND "Off", Dither "On"



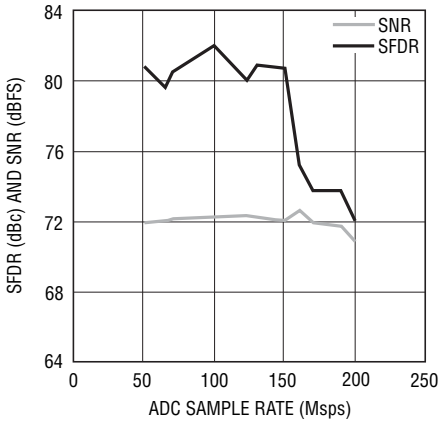
SFDR vs Input Level, f_{IN} = 162.4MHz, PGA = 0, RAND "Off", Dither = "Off"



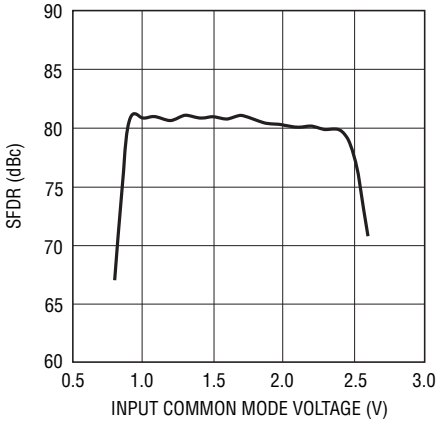
SFDR vs Input Level, f_{IN} = 162.4MHz, PGA = 0, RAND "Off", Dither = "On"



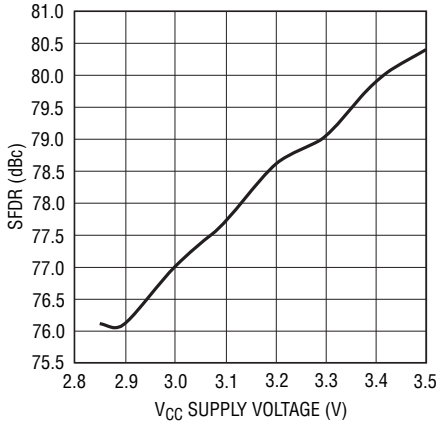
SFDR and SNR vs Sample Rate, f_{IN} = 162.4MHz, –1dBFS, PGA = 0, RAND "Off", Dither "Off"



SFDR vs Input Common Mode Voltage, f_{IN} = 162.4MHz, –1dBFS, PGA = 0

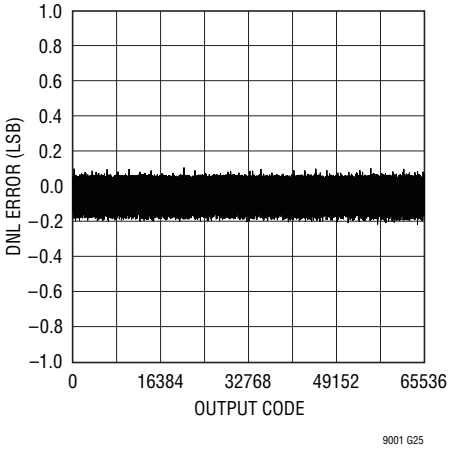


SFDR vs V_{CC} Supply Voltage, f_{IN} = 162.4MHz, –1dBFS, PGA = 0

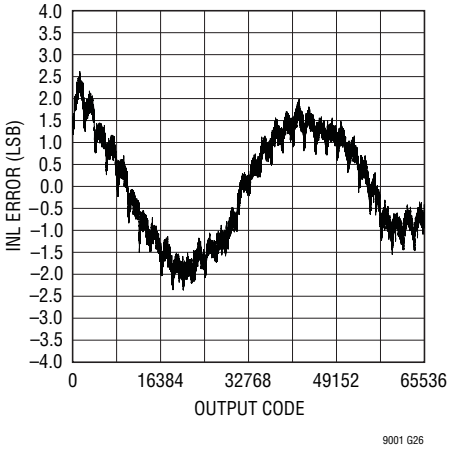


TYPICAL PERFORMANCE CHARACTERISTICS (LTM9001-AD)

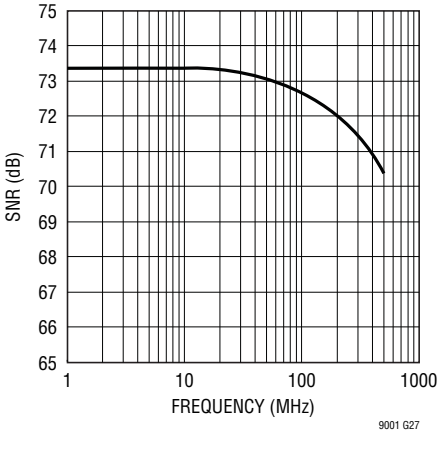
Differential Non-Linearity (DNL) vs Output Code



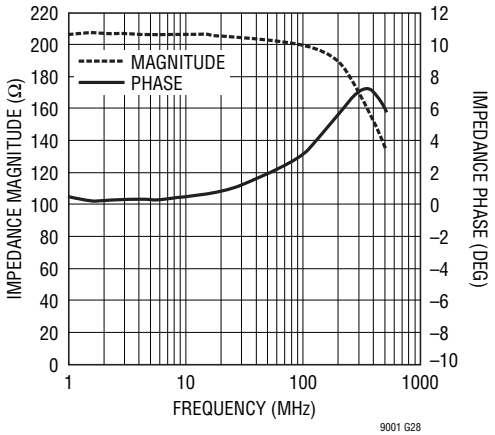
Best Fit Integral Non-Linearity (INL) vs Output Code



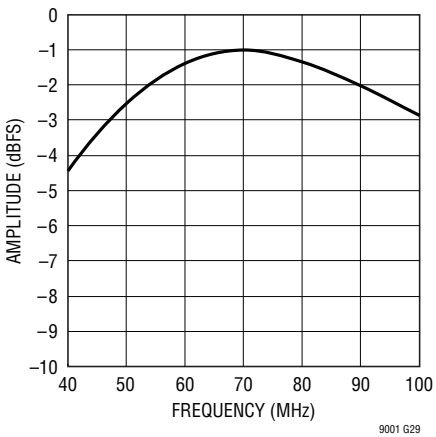
SNR vs Frequency



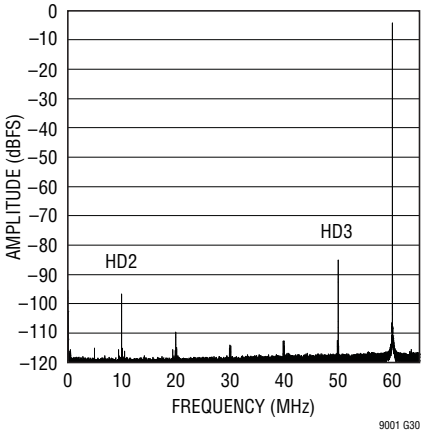
Input Impedance vs Frequency



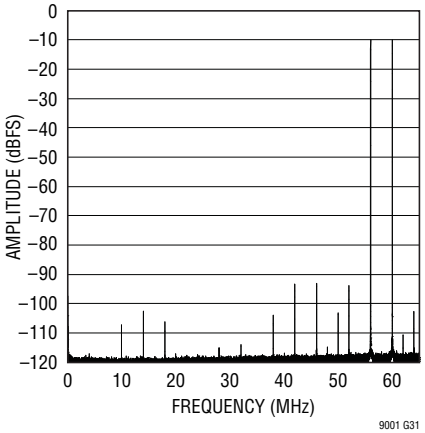
IF Frequency Response



64k Point FFT, f_{IN} = 70MHz, –1dBFS, PGA = 0, RAND "Off", Dither "Off"

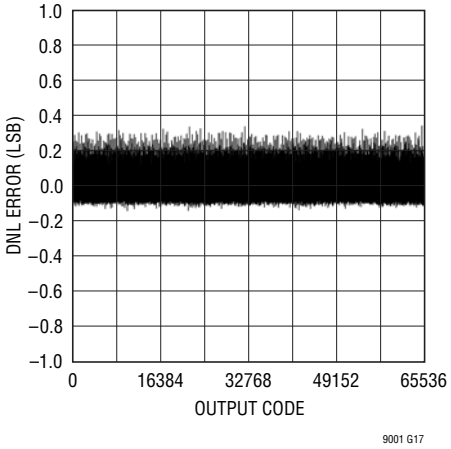


64k Point 2-Tone FFT, f_{IN} = 70MHz, and fin = 74MHz, –7dBFS Per Tone, PGA = 0, RAND "Off", Dither "Off"

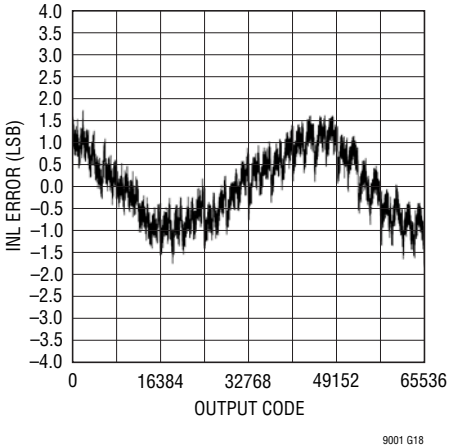


TYPICAL PERFORMANCE CHARACTERISTICS (LTM9001-BA)

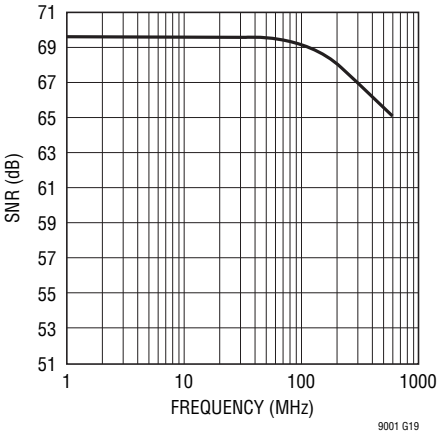
Differential Non-Linearity (DNL) vs Output Code



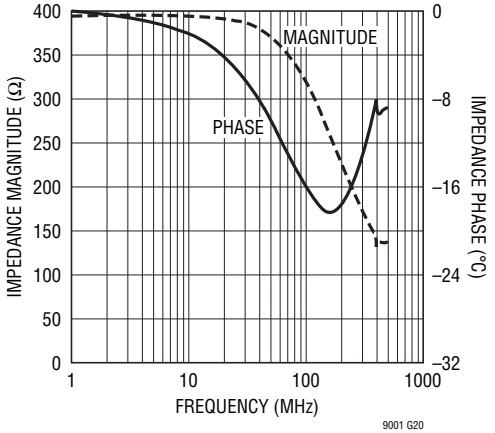
Best Fit Integral Non-Linearity (INL) vs Output Code



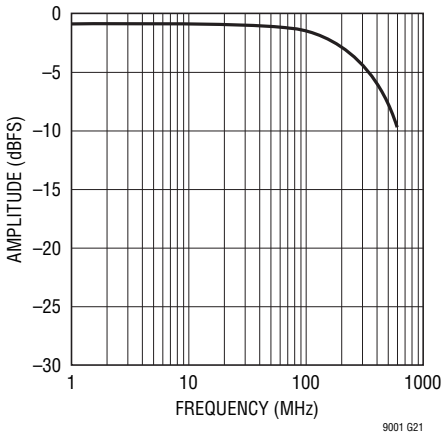
SNR vs Frequency



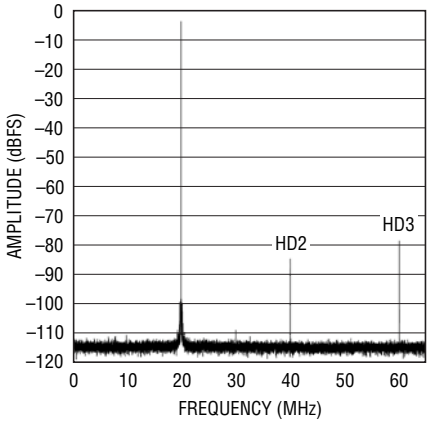
Input Impedance vs Frequency



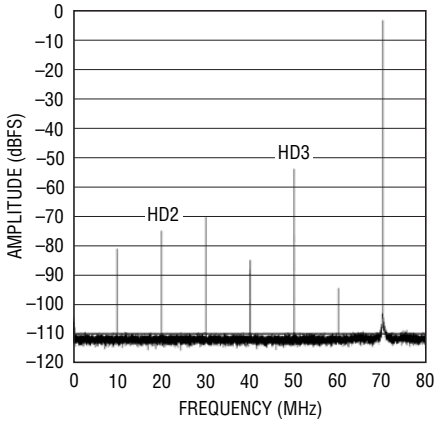
IF Frequency Response



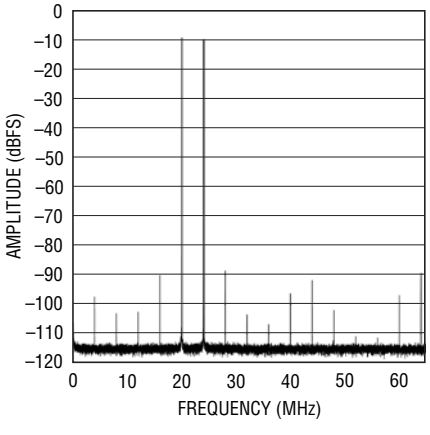
64k Point FFT, f_{IN} = 140MHz, –1dBFS, PGA = 0, RAND "Off", Dither "Off"



64k Point FFT, f_{IN} = 250MHz, –1dBFS, PGA = 0, RAND "Off", Dither "Off"



64k Point 2-Tone FFT, f_{IN} = 136MHz, –7dBFS Per Tone, PGA = 0, RAND "Off", Dither "Off"



PIN FUNCTIONS

Supply Pins

V_{CC} (Pins E1, E2): 3.3V Analog Supply Pin for Amplifier. The voltage on this pin provides power for the amplifier stage only and is internally bypassed to GND.

V_{DD} (Pins E5, D5): 3.3V Analog Supply Pin for ADC. This supply is internally bypassed to GND.

OV_{DD} (Pins A6, G9): Positive Supply for the ADC Output Drivers. This supply is internally bypassed to OGND.

GND (Pins A1, A2, A4, B2, B4, C2, C4, D1, D2, D4, E4, F1, F2, F4, G2, G4, H2, H4, J1, J2, J4): Analog Ground.

OGND (Pins A5, A9, G8, J9): ADC Output Driver Ground.

Analog Inputs

IN^+ (Pin G1): Positive (Non-Inverting) Amplifier Input.

IN^- (Pin H1): Negative (Inverting) Amplifier Input.

DNC (Pins C3, D3): Do Not Connect. These pins are used for testing and should not be connected on the PCB. They may be soldered to unconnected pads and should be well isolated. The DNC pins connect to the signal path prior to the ADC inputs; therefore, care should be taken to keep other signals away from these sensitive nodes.

ENC^+ (Pin C1): Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC^+. This input is internally biased to 1.6V through a 6.2k resistor. Output data can be latched on the rising edge of ENC^+. The Encode pins have a differential 100Ω input impedance.

ENC^- (Pin B1): Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC^-. This input is internally biased to 1.6V through a 6.2k resistor. Bypass to ground with a 0.1µF capacitor for a single-ended encode signal. The encode pins have a differential 100Ω input impedance.

Control Inputs

SENSE (Pin J3): Reference Mode Select and External Reference Input. Tie SENSE to V_{DD} to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set the maximum full-scale input range.

AMPSHDN (Pin H3): Power Shutdown Pin for Amplifier. This pin is a logic input referenced to analog ground. AMPSHDN = low results in normal operation. AMPSHDN = high results in powered down amplifier with typically 3mA amplifier supply current.

MODE (Pin G3): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to $1/3V_{DD}$ selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to $2/3V_{DD}$ selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to V_{DD} selects 2's complement output format and disables the clock duty cycle stabilizer.

RAND (Pin F3): Digital Output Randomization Selection Pin. RAND = low results in normal operation. RAND = high selects D1 to D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. This mode of operation reduces the effects of digital output interference.

PGA (Pin E3): Programmable Gain Amplifier Control Pin. PGA = low selects the normal (maximum) input voltage range. PGA = high selects a 3.5dB reduced input range for slightly better distortion performance at the expense of SNR.

ADCSHDN (Pin B3): Power Shutdown Pin for ADC. ADCSHDN = low results in normal operation. ADCSHDN = high results in powered down analog circuitry and the digital outputs are placed in a high impedance state.

DITH (Pin A3): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation.

LVDS (Pin F5): Data Output Mode Select Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to $1/3V_{DD}$ selects demultiplexed CMOS mode. Connecting LVDS to $2/3V_{DD}$ selects low power LVDS mode. Connecting LVDS to V_{DD} selects standard LVDS mode.

PIN FUNCTIONS

Digital Outputs

For CMOS Mode, Full Rate or Demultiplexed

DA0 to DA15 (Pins E9 to H5): Digital Outputs, A Bus. DA15 is the MSB. Output bus for full rate CMOS mode and demultiplexed mode.

CLKOUTA (Pin E8): Inverted Data Valid Output. CLKOUTA will toggle at the sample rate in full rate CMOS mode or at 1/2 the sample rate in demultiplexed mode. Latch the data on the rising edge of CLKOUTA.

OFB (Pin E6): Overflow/Underflow Digital Output for the B Bus. OFB is high when an overflow or underflow has occurred on the B bus. OFB is in a high impedance state in full rate CMOS mode.

DB0 to DB15 (Pins B5 to D9): Digital Outputs, B Bus. DB15 is the MSB. Active in demultiplexed mode. The B bus is in a high impedance state in full rate CMOS mode.

CLKOUTB (Pin E7): Data Valid Output. CLKOUTB will toggle at the sample rate in full rate CMOS mode or at 1/2 the sample rate in demultiplexed mode. Latch the data on the falling edge of CLKOUTB.

OFA (Pin G5): Overflow/Underflow Digital Output for the A Bus. OFA is high when an overflow or underflow has occurred on the A bus.

For LVDS Mode, Standard or Low Power

$D0^-/D0^+$ to $D15^-/D15^+$ (Pins B5 to G6): LVDS Digital Outputs. All LVDS outputs require differential 100Ω termination resistors at the LVDS receiver. $D15^+/D15^-$ is the MSB.

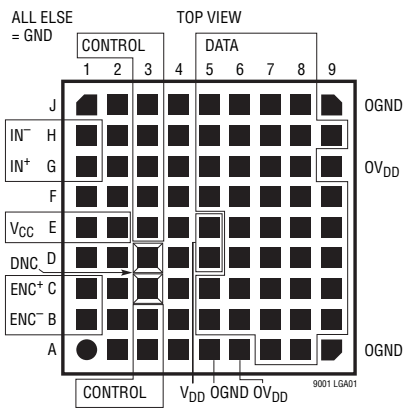
$CLKOUT^-/CLKOUT^+$ (Pins E6, E7): LVDS Data Valid Output. Latch data on the rising edge of $CLKOUT^+$, falling edge of $CLKOUT^-$.

OF^-/OF^+ (Pins H5, G5): Overflow/Underflow Digital Output. OF is high when an over or under flow has occurred.

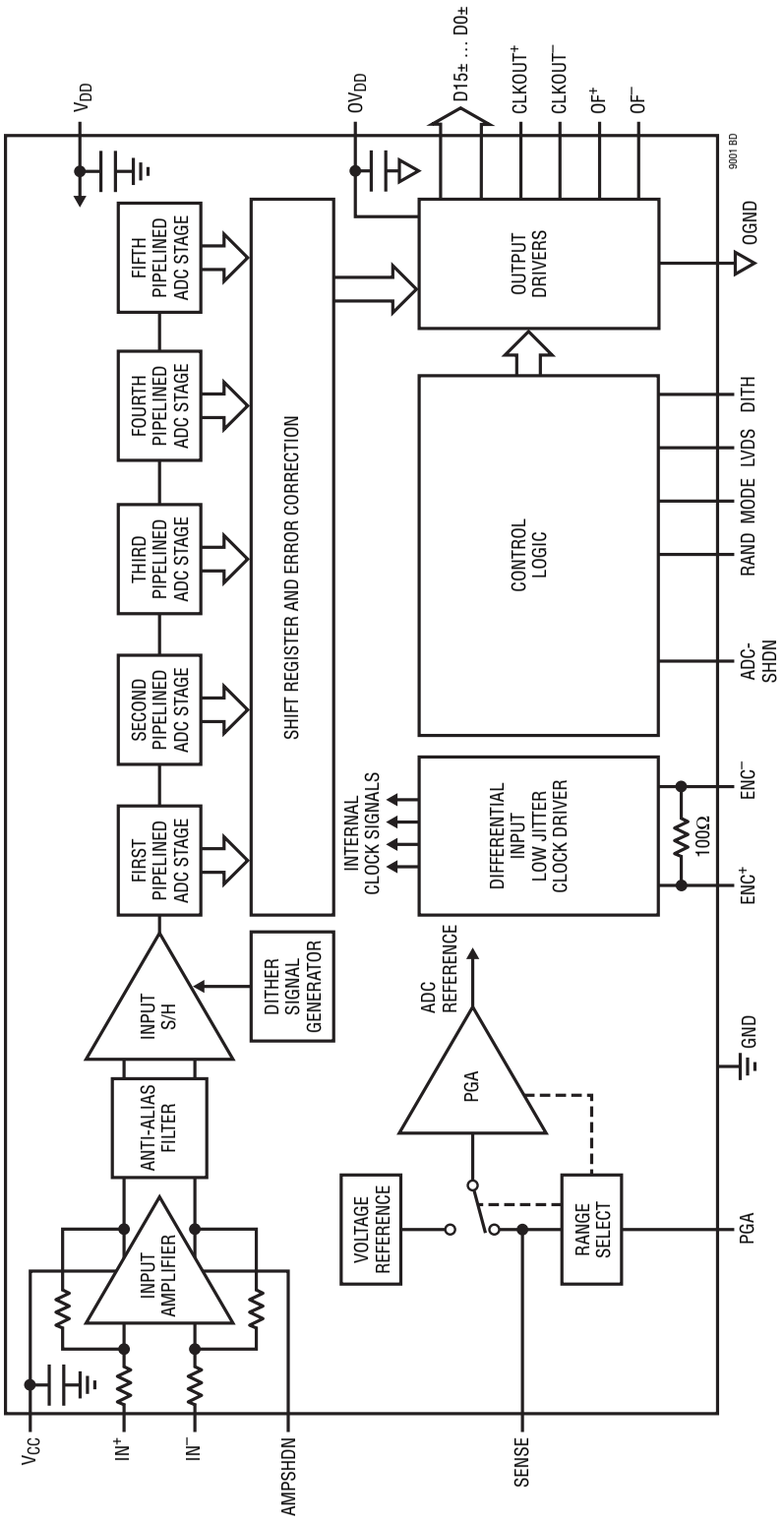
Pin Configuration (LVDS Outputs/CMOS Outputs)

	1	2	3	4	5	6	7	8	9
J	GND	GND	SENSE	GND	$D14^+/DA12$	$D14^-/DA11$	$D12^+/DA8$	$D12^-/DA7$	OGND
H	IN^-	GND	AMPSHDN	GND	$OF^-/DA15$	$D15^-/DA13$	$D13^-/DA9$	$D11^-/DA5$	$D11^+/DA6$
G	IN^+	GND	MODE	GND	OF^+/OFA	$D15^+/DA14$	$D13^+/DA10$	OGND	OV_{DD}
F	GND	GND	RAND	GND	LVDS	$D9^-/DA1$	$D9^+/DA2$	$D10^-/DA3$	$D10^+/DA4$
E	V_{CC}	V_{CC}	PGA	GND	V_{DD}	$CLKOUT^-/OFB$	$CLKOUT^+/CLKOUTB$	$D8^-/CLKOUTA$	$D8^+/DA0$
D	GND	GND	DNC	GND	V_{DD}	$D6^-/DB12$	$D6^+/DB13$	$D7^-/DB14$	$D7^+/DB15$
C	ENC^+	GND	DNC	GND	$D0^+/DB1$	$D4^-/DB8$	$D4^+/DB9$	$D5^-/DB10$	$D5^+/DB11$
B	ENC^-	GND	ADCSHDN	GND	$D0^-/DB0$	$D1^-/DB2$	$D1^+/DB3$	$D3^+/DB7$	$D3^-/DB6$
A	GND	GND	DITH	GND	OGND	OV_{DD}	$D2^-/DB4$	D2+/DB5	OGND

Top View of LGA Pinout (Looking Through Component)



FUNCTIONAL BLOCK DIAGRAM



OPERATION

DYNAMIC PERFORMANCE DEFINITIONS

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output.

Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = -20Log\left(\sqrt{(V2^2 + V3^2 + V4^2 + ...Vn^2)}/V1\right)$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics.

Intermodulation Distortion

If the input signal consists of more than one spectral component, the transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the input, nonlinearities in the transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc.

For example, the 3rd order IMD terms include (2fa + fb), (fa + 2fb), (2fa – fb) and (fa – 2fb). The 3rd order IMD is defined as the ration of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

Spurious Free Dynamic Range (SFDR)

The ratio of the RMS input signal amplitude to the RMS value of the peak spurious spectral component expressed in dBc. SFDR may also be calculated relative to full-scale and expressed in dBFS.

Aperture Delay Time

Aperture delay is the time from when a rising ENC^+ equals the $ENC^–$ voltage to the instant that the input signal is held by the sample and-hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20log\ (2\pi \bullet f_{IN} \bullet t_{JITTER})$$

DESCRIPTION

The LTM9001 is an integrated system in a package (SiP) µModule® receiver that includes a high-speed, sampling 16-bit A/D converter, matching network, anti-aliasing filter and a low noise, differential amplifier with fixed gain. It is designed for digitizing high frequency, wide dynamic range signals with an intermediate frequency (IF) range up to 300MHz.

OPERATION

The following sections describe in further detail the functional operation of the LTM9001. The SiP technology allows the LTM9001 to be customized and this is described in the first section. The remaining outline follows the basic functional elements as shown in Figure 1.

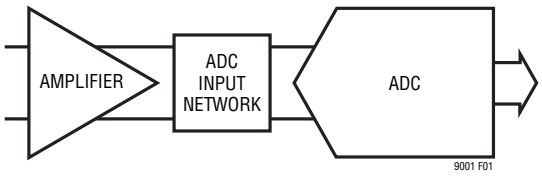


Figure 1. Basic Functional Elements

SEMI-CUSTOM OPTIONS

The µModule construction affords a new level of flexibility in application-specific standard products. Standard ADC and amplifier components can be integrated regardless of their process technology and matched with passive components to a particular application. The LTM9001-AA, as the first example, is configured with a 16-bit ADC sampling at rates up to 130Msps. The amplifier gain is 20dB with an input impedance of 200Ω and an input range of 233mV$_{P-P}$. The matching network is designed to optimize the interface between the amplifier output and the ADC under these conditions. Additionally, there is a 2-pole bandpass filter designed for 162.5MHz ±25MHz.

However, other options are possible through Linear Technology's semi-custom development program. Linear Technology has in place a program to deliver other speed, resolution, IF range, gain and filter configurations for a wide range of applications. See Table 1 for the LTM9001-AA configuration and potential options. These semi-custom designs are based on existing ADCs and amplifiers with an appropriately modified matching network. The final subsystem is then tested to the exact parameters defined for the application. The final result is a fully integrated, accurately tested and reliable solution. For more details on the semi-custom receiver subsystem program, contact Linear Technology.

Note that not all combinations of options in Table 1 are possible at this time and specified performance may differ significantly from existing values. This data sheet discusses devices with LVDS and CMOS outputs. The lower speed options that only support CMOS outputs are available on a separate data sheet. The CMOS-only options have a different pin assignment.

AMPLIFIER INFORMATION

The amplifiers used in the LTM9001 are low noise and low distortion fully differential ADC drivers. The amplifiers are very flexible in terms of I/O coupling. They can be AC- or DC-coupled at the inputs. Users are advised to keep the input common mode voltage between 1V and 1.6V for proper operation. If the inputs are AC-coupled, the input common mode voltage is automatically biased. The input signal can be either single-ended or differential with almost no difference in distortion performance.

Table 1. Semi-Custom Options

AMPLIFIER IF RANGE	AMPLIFIER INPUT IMPEDANCE	AMPLIFIER GAIN	FILTER	ADC SAMPLE RATE	ADC RESOLUTION	OUTPUT	PART NUMBER
300MHz	200Ω	20dB	162.5MHz BPF, 50MHz BW	130Msps	16-bit	LVDS/CMOS	LTM9001-AA
300MHz	200Ω	14dB	70MHz BPF, 25MHz BW	130Msps	16-bit	LVDS/CMOS	LTM9001-AD
300MHz	400Ω	8dB	DC-300MHz LPF	160Msps	16-bit	LVDS/CMOS	LTM9001-BA
Select Combination of Options from Columns Below							
DC-300MHz	50Ω	26dB	LPF TBD	160Msps	16-bit	LVDS/CMOS	
DC-140MHz	200Ω	20dB	BPF TBD	130Msps	14-bit	LVDS/CMOS	
DC-70MHz	200Ω	14dB		105Msps		CMOS	
DC-35MHz	400Ω	8dB		80Msps		CMOS	
	200Ω	6dB		65Msps		CMOS	
				40Msps		CMOS	
				25Msps		CMOS	
				10Msps		CMOS	

OPERATION

ADC INPUT NETWORK

The passive network between the amplifier output stage and the ADC input stage can be configured for bandpass or lowpass response with different cutoff frequencies and bandwidths. The LTM9001-AA, for example, implements a 2-pole bandpass filter centered at 162.5MHz with 50MHz bandwidth. Note that the filter attenuates the signal at 162.5MHz by 1dB, making the overall gain of the subsystem 19dB.

For production test purposes the filter is designed to allow DC inputs into the ADC.

CONVERTER INFORMATION

The analog-to-digital converter (ADC) is a CMOS pipelined multistep converter with a front-end PGA. As shown in the Functional Block Diagram, the converter has five pipelined ADC stages; a sampled analog input will result in a digitized value seven cycles later (see the Timing Diagram section). The encode input is differential for improved common mode noise immunity.

APPLICATIONS INFORMATION

INPUT SPAN

The LTM9001 is configured with a fixed input span and input impedance. With the amplifier gain and the ADC input network described above for LTM9001-AA, the full-scale input range of the driver circuit is 233mV$_{P-P}$. The recommended ADC input span is achieved by tying the SENSE pin to V_{DD}. However, the ADC input span can be changed by applying a DC voltage to the SENSE pin.

Input Impedance and Matching

The differential input impedance of the LTM9001 can be 50Ω, 200Ω or 400Ω. In some applications the differential inputs may need to be terminated to a lower value impedance, e.g. 50Ω, in order to provide an impedance match for the source. Several choices are available.

One approach is to use a differential shunt resistor (Figure 2). Another approach is to employ a wide band transformer (Figure 3). Both methods provide a wide band match. The termination resistor or the transformer must be placed close to the input pins in order to minimize the reflection due to input mismatch.

Table 2. Differential Amplifier Input Termination Values

Z_{IN}	R_T FIG 2
400Ω	57Ω
200Ω	66.5Ω
50Ω	None

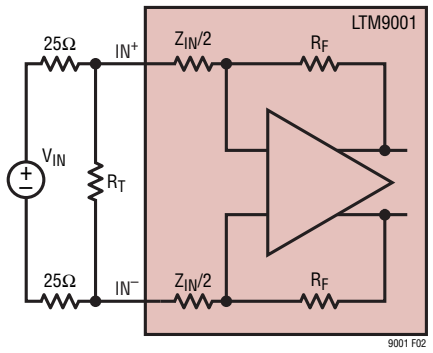


Figure 2. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor (See Table 2 for R_T Values)

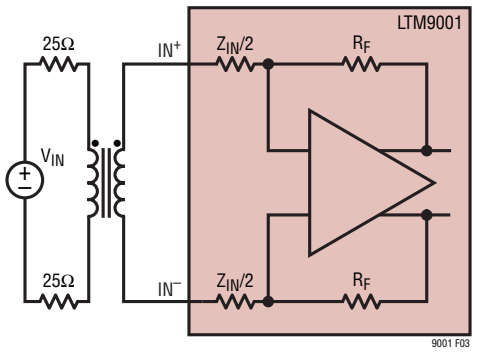


Figure 3. Input Termination for Differential 50Ω Input Impedance Using a Wideband Transformer

APPLICATIONS INFORMATION

Alternatively, one could apply a narrowband impedance match at the inputs for frequency selection and/or noise reduction.

Referring to Figure 4, amplifier inputs can be easily configured for single-ended input without a balun. The signal is fed to one of the inputs through a matching network while the other input is connected to the same impedance. In general, the single-ended input impedance and termination resistor R_T are determined by the combination of R_S, $Z_{IN}/2$ and R_F.

Table 3. Single-Ended Amplifier Input Termination Values

Z_{IN}	R_T FIG 4
400Ω	59Ω
200Ω	68.5Ω
50Ω	150Ω

The LTM9001 amplifier is stable with all source impedances. The overall differential gain is affected by the source impedance in Figure 5:

$$A_V = | V_{OUT}/V_{IN} | = (1000/(R_S + Z_{IN}/2))$$

The noise performance of the amplifier also depends upon the source impedance and termination. For example, an input 1:4 transformer in Figure 3 improves the input noise figure by adding 6dB voltage gain at the inputs.

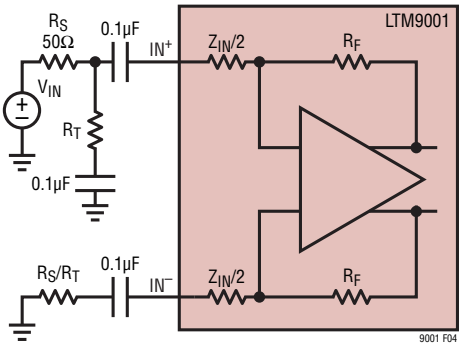


Figure 4. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor

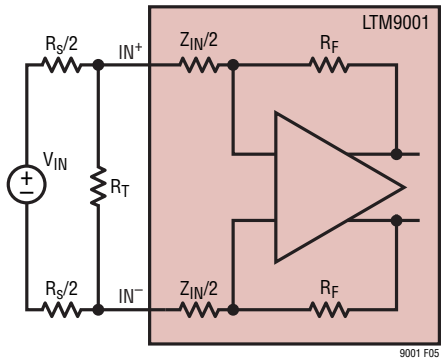


Figure 5. Calculate Differential Gain

Reference and SENSE Pin Operation

Figure 6 shows the converter reference circuitry consisting of a 2.5V bandgap reference, a programmable gain amplifier and control circuit. There are three modes of reference operation: internal reference, 1.25V external reference or 2.5V external reference. To use the internal reference, tie the SENSE pin to V_{DD}. To use an external reference, simply apply either a 1.25V or 2.5V reference voltage to the SENSE input pin. Both 1.25V and 2.5V applied to SENSE will result in the maximum full-scale range.

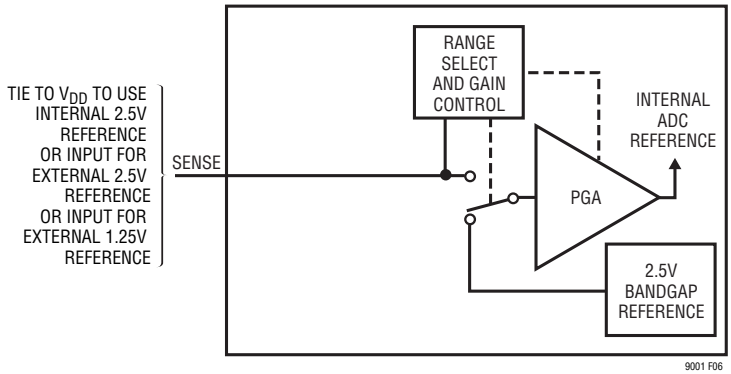


Figure 6. Reference Circuit

APPLICATIONS INFORMATION

PGA Pin

The PGA pin selects between two gain settings for the ADC front-end. PGA = low selects the maximum input span; PGA = high selects a 3.5dB lower input span. The high input range has the best SNR. For applications with high linearity requirements, the low input range will have improved distortion; however, the SNR will be 1.8dB worse. See the Typical Performance Characteristics section.

Driving the Encode Inputs

The noise performance of the converter can depend on the encode signal quality as much as the analog input. The encode inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter. In applications where jitter is critical (high input frequencies), take the following into consideration:

1. Differential drive should be used.
2. Use the largest amplitude possible. If using transformer coupling, use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a fixed frequency sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs such that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.2V to V_{DD}. Each input may be driven from ground to V_{DD} for single-ended drive.

The encode clock inputs have a differential 100Ω input impedance. For 50Ω inputs e.g. signal generators, an additional 100Ω impedance will provide an impedance match, as shown in Figure 7b.

Maximum and Minimum Encode Rates

The maximum encode rate for the LTM9001-Ax is 130Msps and 160Msps for LTM9001-BA. For the ADC to operate properly the encode signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 3.65ns (LTM9001-Ax, or 2.97ns for LTM9001-BA) for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS. When using a single-ended encode signal asymmetric rise and fall times can result in duty cycles that are far from 50%.

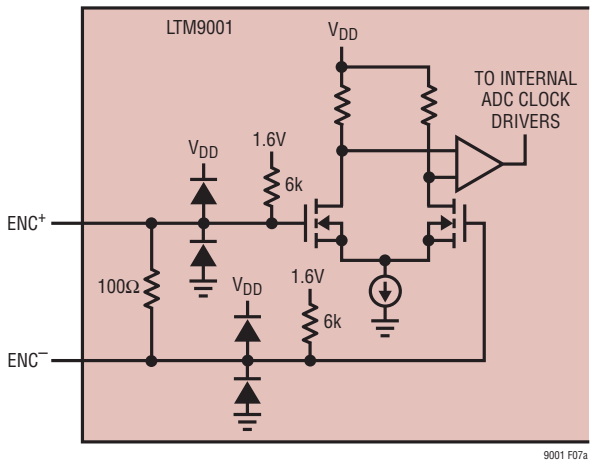


Figure 7a. Equivalent Encode Input Circuit

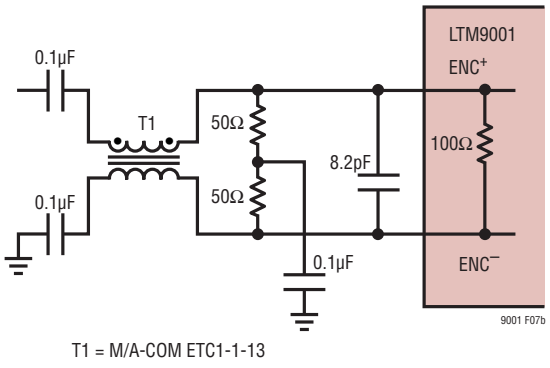


Figure 7b. Transformer Driven Encode

APPLICATIONS INFORMATION

An optional clock duty cycle stabilizer can be used if the input clock does not have a 50% duty cycle. This circuit uses the rising edge of ENC to sample the analog input. The falling edge of ENC is ignored and an internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 30% to 70% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin must be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the sample rate is determined by the droop of the sample and hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTM9001 is 1Msps.

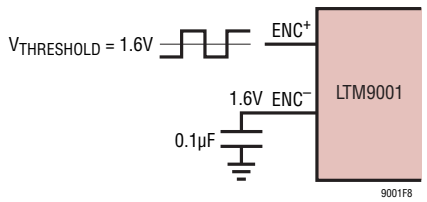


Figure 8. Single-Ended ENC Drive, Not Recommended for Low Jitter

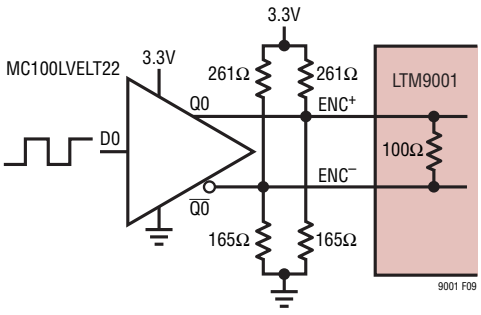


Figure 9. ENC Drive Using a CMOS to PECL Translator

DIGITAL OUTPUTS

Digital Output Modes

The LTM9001 can operate in four digital output modes: standard LVDS, low power LVDS, full rate CMOS, and demultiplexed CMOS. The LVDS pin selects the mode of operation. This pin has a four level logic input, centered at 0, $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD}. An external resistive divider can be used to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 4 shows the logic states for the LVDS pin.

Table 4. LVDS Pin Function

LVDS	DIGITAL OUTPUT MODE
0V(GND)	Full-Rate CMOS
$1/3V_{DD}$	Demultiplexed CMOS
$2/3V_{DD}$	Low Power LVDS
V_{DD}	LVDS

Digital Output Buffers (CMOS Modes)

Figure 10 shows an equivalent circuit for a single output buffer in CMOS mode, full-rate or demultiplexed. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and eliminates the need for external damping resistors.

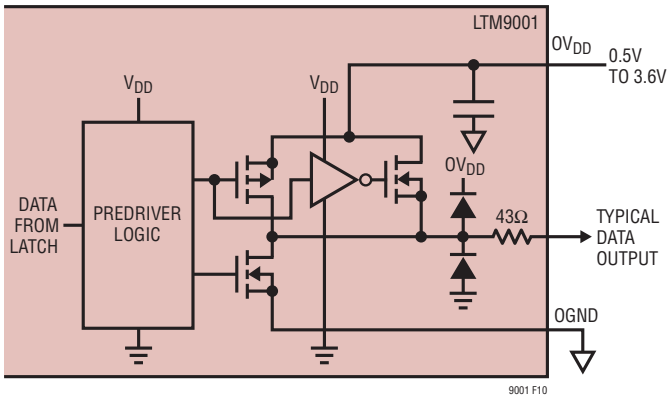


Figure 10. Equivalent Circuit for a Digital Output Buffer

APPLICATIONS INFORMATION

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTM9001 should drive a minimum capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF. A resistor in series with the output may be used but is not required since the ADC has a series resistor of 43Ω on chip.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Digital Output Buffers (LVDS Modes)

Figure 11 shows an equivalent circuit for an LVDS output pair. A 3.5mA current is steered from OUT^+ to OUT^- or vice versa, which creates a ±350mV differential voltage across the 100Ω termination resistor at the LVDS receiver.

A feedback loop regulates the common mode output voltage to 1.2V. For proper operation each LVDS output pair must be terminated with an external 100Ω termination resistor, even if the signal is not used (such as OF^+/OF^- or $CLKOUT^+/CLKOUT^-$). To minimize noise the PC board traces for each LVDS output pair should be routed close together. To minimize clock skew all LVDS PC board traces should have about the same length.

In low power LVDS mode 1.75mA is steered between the differential outputs, resulting in ±175mV at the LVDS receiver's 100Ω termination resistor. The output common mode voltage is 1.2V, the same as standard LVDS mode.

Data Format

The LTM9001 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. This pin has a four level logic input, centered at 0, $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD}. An external resistive divider can be used to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 5 shows the logic states for the MODE pin.

Table 5. MODE Pin Function

MODE	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0V(GND)	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

An overflow output bit (OF) indicates when the converter is overranged or underranged. In CMOS mode, a logic high on the OFA pin indicates an overflow or underflow on the A data bus, while a logic high on the OFB pin indicates an overflow on the B data bus. In LVDS mode, a differential logic high on OF^+/OF^- pins indicates an overflow or underflow.

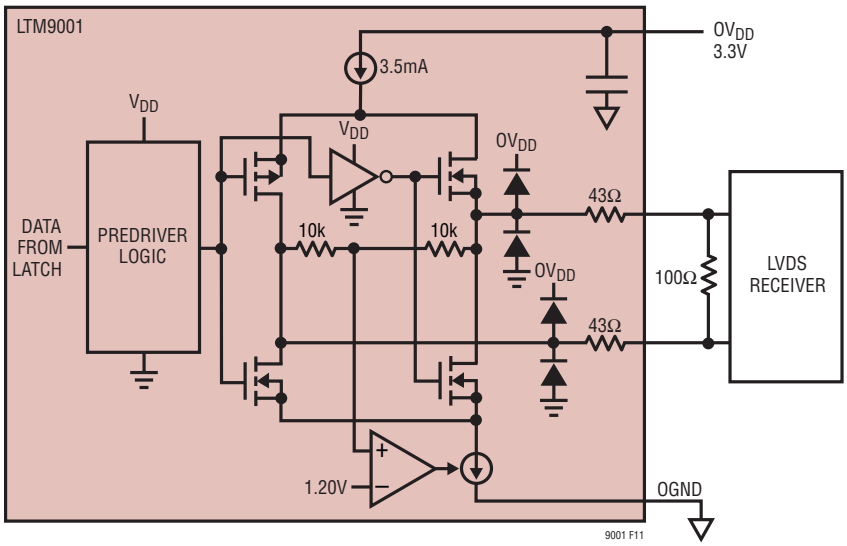


Figure 11. Equivalent Output Buffer in LVDS Mode

APPLICATIONS INFORMATION

Output Clock

The ADC has a delayed version of the encode input available as a digital output, CLKOUT. The CLKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode.

In both CMOS modes, A bus data will be updated as CLKOUTA falls and CLKOUTB rises. In demultiplexed CMOS mode the B bus data will be updated as CLKOUTA falls and CLKOUTB rises.

In full rate CMOS mode, only the A data bus is active; data may be latched on the rising edge of CLKOUTA or the falling edge of CLKOUTB.

In demultiplexed CMOS mode CLKOUTA and CLKOUTB will toggle at 1/2 the frequency of the encode signal. Both the A bus and the B bus may be latched on the rising edge of CLKOUTA or the falling edge of CLKOUTB.

Digital Output Randomizer

Interference from the ADC digital outputs is sometimes unavoidable. Interference from the digital outputs may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can result in discernible unwanted tones in the ADC output spectrum.

By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized, trading a slight increase in the noise floor for a large reduction in unwanted tone amplitude.

The digital output is "randomized" by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied; that is, an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT output are not affected. The output randomizer function is active when the RAND pin is high.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For

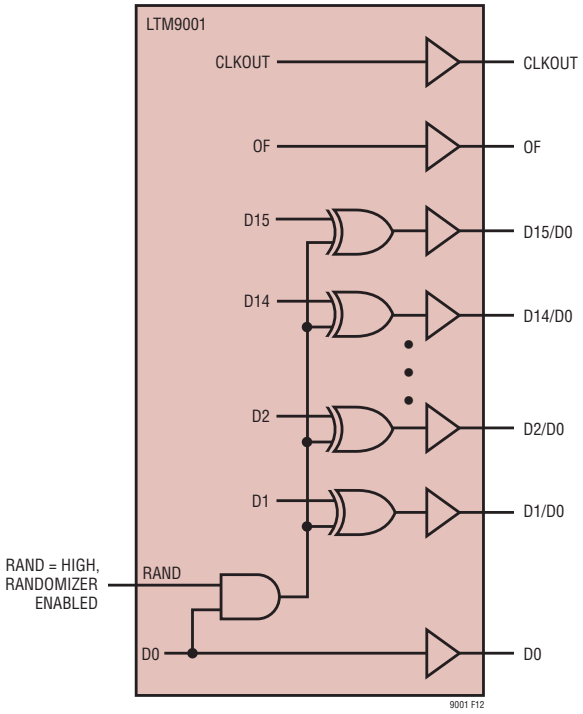


Figure 12. Functional Equivalent of Digital Output Randomizer

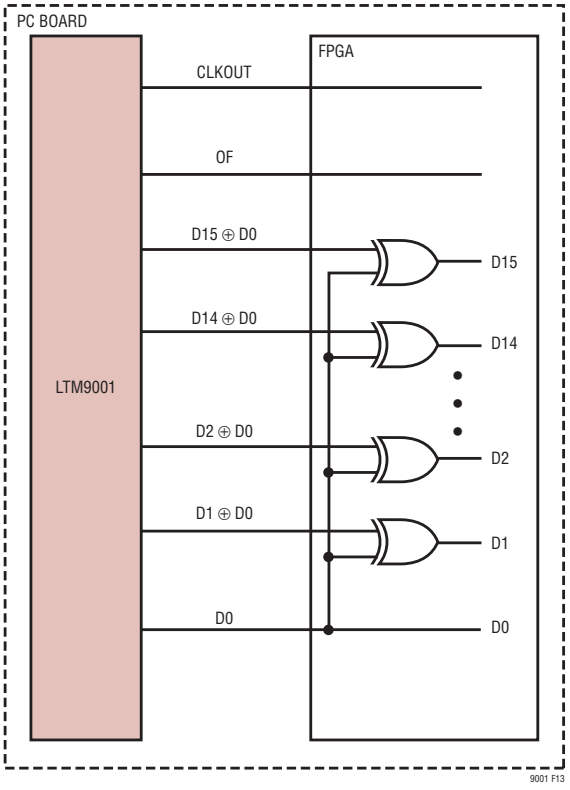


Figure 13. Derandomizing a Randomized Digital Output

APPLICATIONS INFORMATION

example, if the converter is driving a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply. OV_{DD} can be powered with any logic voltage up to the 3.6V. OGND can be powered with any voltage from ground up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Internal Dither

The LTM9001 is a 16-bit receiver subsystem with a very linear transfer function; however, at low input levels even slight imperfections in the transfer function will result in unwanted tones. Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input location on the ADC transfer curve, resulting in improved SFDR for low signal levels.

As shown in Figure 14, the output of the sample-and-hold amplifier is summed with the output of a dither DAC. The dither DAC is driven by a long sequence pseudo-random number generator; the random number fed to the dither DAC is also subtracted from the ADC result. If the dither DAC is precisely calibrated to the ADC, very little of the dither signal will be seen at the output. The dither signal that does leak through will appear as white noise. The dither DAC will cause a small elevation in the noise floor of the ADC, as compared to the noise floor with dither off.

For best noise performance with the dither signal on, the driving impedance connected across pins IN^+/IN^- should closely match that of the module (see Table 1). A source impedance that is resistive and matches that of the module within 10% will give the best results.

Supply Sequencing

The V_{CC} pin provides the supply to the amplifier and the V_{DD} pin provides the supply to the ADC. The amplifier and the ADC are separate integrated circuits within the LTM9001; however, there are no supply sequencing considerations beyond standard practice. It is recommended that the amplifier and ADC both use the same low noise, 3.3V supply, but the amplifier may be operated from a lower voltage level if desired. Both devices can operate from the same 3.3V linear regulator but place a ferrite bead between the V_{CC} and V_{DD} pins. Separate linear regulators can be used without additional supply sequencing circuitry if they have common input supplies.

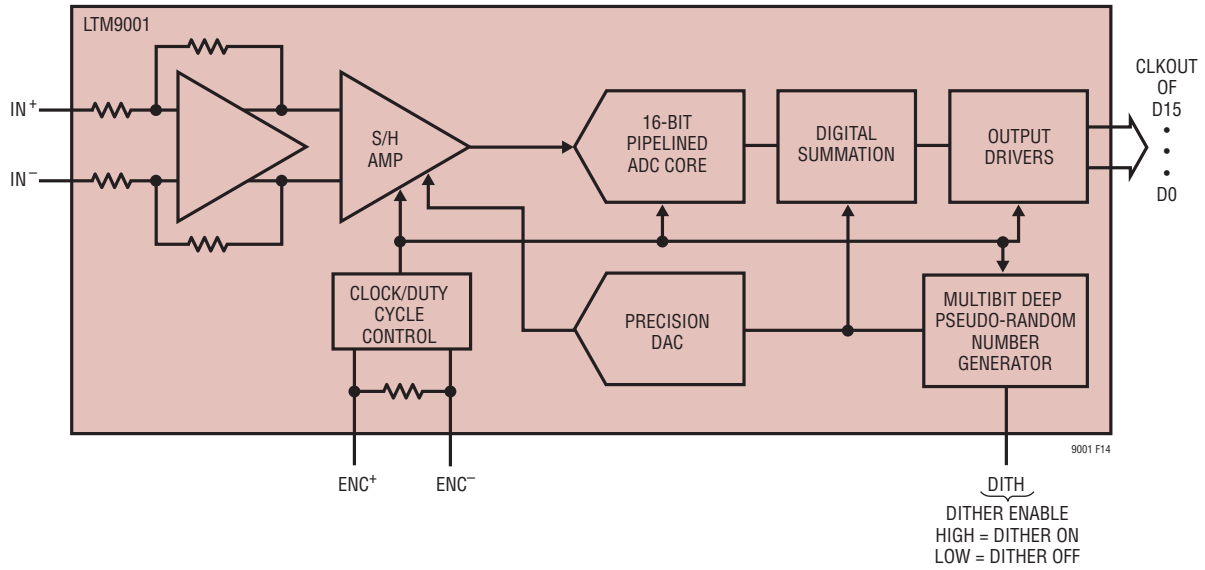


Figure 14. Functional Equivalent Block Diagram of Internal Dither Circuit