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14-Bit Dual-Channel IF/ Baseband Receiver Subsystem

FEATURES

- **Integrated Dual 14-Bit, High-Speed ADC, Passive Filters and Fixed Gain Differential Amplifiers**
- **Up to 300MHz IF Range**
  Lowpass and Bandpass Filter Versions
- **Integrated Low Noise, Low Distortion Amplifiers**
  Fixed Gain: 8dB, 14dB, 20dB or 26dB
  50Ω, 200Ω or 400Ω Input Impedance
- **Integrated Bypass Capacitance, No External Components Required**
- 66dB SNR Up to 140MHz Input (LTM9002-AA)
- 76dB SFDR Up to 140MHz Input (LTM9002-AA)
- Auxiliary 12-Bit DACs for Gain Adjustment
- Clock Duty Cycle Stabilizer
- Single 3V to 3.3V Supply
- Low Power: 1.3W (665mW/ch.)
- Shutdown and Nap Modes
- 15mm × 11.25mm LGA Package

APPLICATIONS

- Telecommunications
- Direct Conversion Receivers
- Main and Diversity Receivers
- Cellular Base Stations

DESCRIPTION

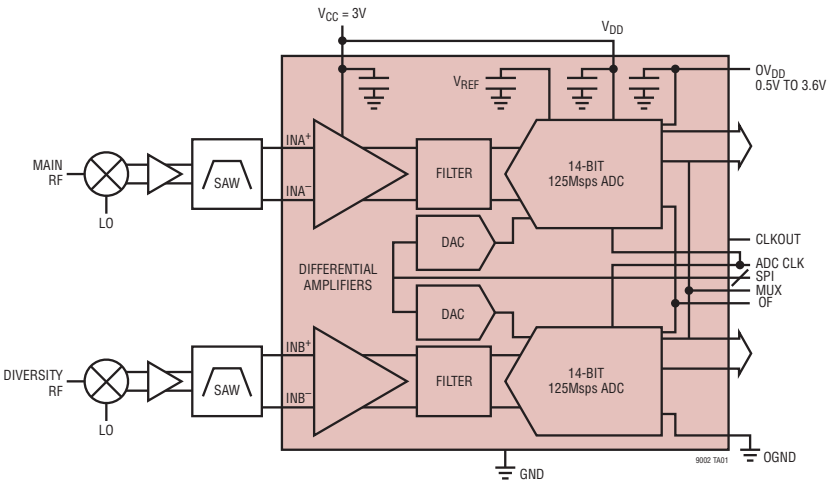
The LTM®9002 is a 14-bit dual-channel IF receiver subsystem. Utilizing an integrated system in a package (SiP) technology, it includes a dual high-speed 14-bit A/D converter, matching network, anti-aliasing filter and two low noise, differential amplifiers. It is designed for digitizing wide dynamic range signals with an intermediate frequency (IF) up to 300MHz. The amplifiers allow either AC- or DC-coupled input drive. Lowpass or bandpass filter networks can be implemented with various bandwidths. Contact Linear Technology regarding customization.

The LTM9002 is perfect for demanding communications applications, with AC performance that includes 66dB SNR and 76dB spurious free dynamic range (SFDR). Auxiliary DACs allow gain balancing between channels.

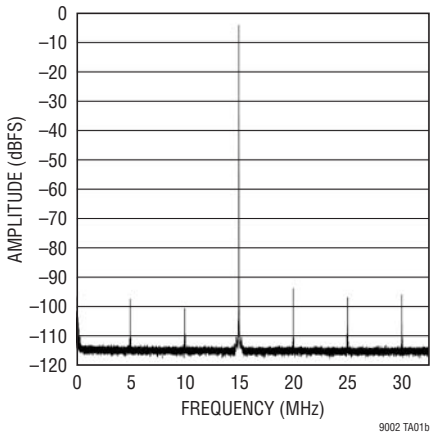
A single 3V supply allows low power operation. A separate output supply allows the outputs to drive 0.5V to 3.3V logic. An optional multiplexer allows both channels to share a digital output bus. Two single-ended CLK inputs can be driven together or independently. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION

Dual Channel IF Receiver



64k Point FFT, f_{IN} = 15MHz, –1dBFS, SENSE = V_{DD}, Channel A (LTM9002-LA)

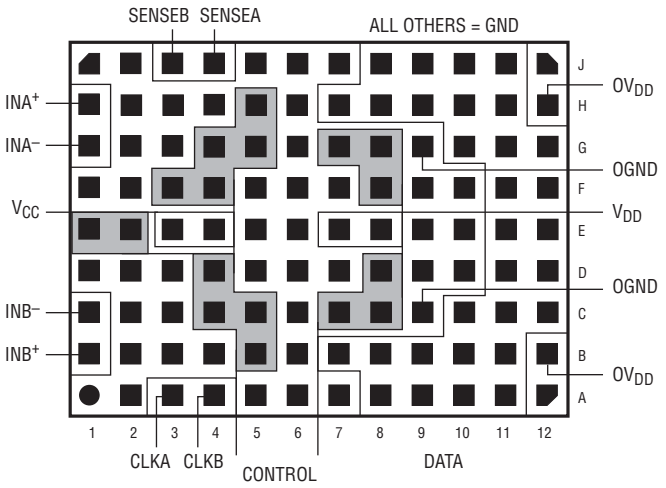


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 3.6V
Supply Voltage (V_{DD}, OV_{DD})..... –0.3V to 4V
Digital Output Ground Voltage (OGND)..... –0.3V to 1V
Input Current (IN^+, IN^-).....±10mA
DAC Digital Input Voltage
($\overline{CS}$/LD, SDI, SCK) ..... –0.3V to 6V
Digital Input Voltage
(Except AMPSHDN) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage
(AMPSHDN).....–0.3V to (V_{CC} + 0.3V)
Digital Output Voltage .....–0.3V to (OV_{DD} + 0.3V)
Operating Temperature Range
LTM9002C..... 0°C to 70°C
LTM9002I.....–40°C to 85°C
Storage Temperature Range.....–65°C to 125°C

PIN CONFIGURATION



LGA PACKAGE
108-LEAD (15mm × 11.25mm × 2.32mm)

T_{JMAX} = 125°C, θ_{JA} = 19°C/W, θ_{JCTOP} = 16°C/W, θ_{JCBOT} = 6°C/W
θ_{JA} DERIVED FROM 101.5mm × 114.5mm PCB WITH 4 LAYERS
WEIGHT = 0.935g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9002CV-AA#PBF	LTM9002CV-AA#PBF	LTM9002VAA	108-Lead (15mm × 11.25mm × 2.3mm) LGA	0°C to 70°C
LTM9002CV-LA#PBF	LTM9002CV-LA#PBF	LTM9002VLA	108-Lead (15mm × 11.25mm × 2.3mm) LGA	0°C to 70°C
LTM9002IV-AA#PBF	LTM9002IV-AA#PBF	LTM9002VAA	108-Lead (15mm × 11.25mm × 2.3mm) LGA	–40°C to 85°C
LTM9002IV-LA#PBF	LTM9002IV-LA#PBF	LTM9002VLA	108-Lead (15mm × 11.25mm × 2.3mm) LGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G_{DIFF}	Gain	DC, LTM9002-AA f_{IN} = 140MHz	●	25	26 25	27	dB dB
		Channel A, DC (LTM9002-LA) f_{IN} = 15MHz Channel B, DC (LTM9002-LA) f_{IN} = 15MHz	● ● 	19.4 7.5 	20 19 8 7	20.6 8.5 	dB dB dB dB
G_{TEMP}	Gain Temperature Drift	V_{IN} = MAX, (Note 3)			1.5		mdB/°C
	Gain Matching	External Reference			5		mdB
V_{IN}	Input Voltage Range for –1dBFS	Both Channels, f_{IN} = 140MHz (LTM9002-AA)			100		mV_{P-P}
		Channel A, f_{IN} = 15MHz (LTM9002-LA)			200		mV_{P-P}
		Channel B, f_{IN} = 15MHz (LTM9002-LA)			800		mV_{P-P}
V_{INCM}	Input Common Mode Voltage Range			1		1.5	V
R_{INDIFF}	Differential Input Impedance	Both Channels (LTM9002-AA)			50		Ω
		Channel A (LTM9002-LA) Channel B (LTM9002-LA)			200 400		Ω Ω
C_{INDIFF}	Differential Input Capacitance	Includes Parasitic			1		pF
V_{OS}	Offset Error (Note 5)	Including Amplifier and ADC	●	–5	0.3	5	mV
	Offset Matching				0.3		mV
	Offset Drift	Including Amplifier and ADC			±10		µV/°C
CMRR	Common Mode Rejection Ratio				50		dB
I_{SENSE}	SENSE Input Leakage	0V < SENSE < 1V	●	–3		3	µA
I_{MODE}	MODE Input Leakage	0V < MODE < V_{DD}	●	–3		3	µA
t_{AP}	Sample and Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				0.2		ps_{RMS}

CONVERTER CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Characteristics							
	Resolution (No Missing Codes)	LTM9002-AA	●	14			Bits
		LTM9002-LA	●	12			Bits
INL	Integral Linearity Error (Note 4)	LTM9002-AA			±1.5		LSB
		LTM9002-LA			±0.3		LSB
DNL	Differential Linearity Error	LTM9002-AA	●	–1	±0.6	1	LSB
		LTM9002-LA	●	–1	±0.2	1	LSB

DYNAMIC ACCURACY

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Input = –1dBFS. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	70MHz Input (Both Channels), LTM9002-AA			66		dBFS
		140MHz Input (Both Channels), LTM9002-AA	●	61.5	66		dBFS
		15MHz Input (Channel A), LTM9002-LA	●	67.7	69.9		dBFS
		15MHz Input (Channel B), LTM9002-LA	●	68.5	71.1		dBFS
SFDR	Spurious Free Dynamic Range, 2nd or 3rd Harmonic	70MHz Input (Both Channels), LTM9002-AA			82		dBc
		140MHz Input (Both Channels), LTM9002-AA	●	67.5	76		dBc
		15MHz Input (Channel A), LTM9002-LA	●	75	86.2		dBc
		15MHz Input (Channel B), LTM9002-LA	●	72.7	85.5		dBc
SFDR	Spurious Free Dynamic Range 4th or Higher	70MHz Input (Both Channels), LTM9002-AA			90		dBc
		140MHz Input (Both Channels), LTM9002-AA	●	74.2	90		dBc
		15MHz Input (Channel A), LTM9002-LA	●	78.8	88.5		dBc
		15MHz Input (Channel B), LTM9002-LA	●	79.8	90.7		dBc
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	70MHz Input (Both Channels), LTM9002-AA			66		dBFS
		140MHz Input (Both Channels), LTM9002-AA	●	60.7	66		dBFS
		15MHz Input (Channel A), LTM9002-LA	●	67.1	69.7		dBFS
		15MHz Input (Channel B), LTM9002-LA	●	67.9	70.8		dBFS
IMD3	Third Order Inter-Modulation Distortion; 1MHz Tone Spacing, Two Tones –7dBFS	70MHz Input, LTM9002-AA			77		dBc
		140MHz Input, LTM9002-AA			73		dBc
		15MHz Input, LTM9002-LA			77		dBc
	Crosstalk	140MHz Input, LTM9002-AA			–110		dB
		15MHz Input, LTM9002-LA			–110		dB

AUXILIARY DAC CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Not applicable for LTM9002-LA) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		●	12			Bits
Monotonicity		●	12			Bits
Full-Scale Range	Internal Reference			1.5		V
Settling Time	±0.024% (±1LSB at 12 Bits), No External Sense Capacitor			83.5		µs

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (CLK, $\overline{OE}$, ADCSHDN, MUX, $\overline{CS}$/LD, SCK, SDI)							
V_{IH}	High Level Input Voltage	V_{DD} = 3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 6)			3		pF

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (AMPSHDN)							
V_{IL}	Low Level Input Voltage		●			0.8	V
V_{IH}	High Level Input Voltage		●	2.4			V
I_{IL}	Input Low Current	AMPSHDN = 0.8V	●			0.5	µA
I_{IH}	Input High Current	AMPSHDN = 2.4V	●		1.4	3	µA
Logic Outputs							
OV_{DD} = 3V							
C_{OZ}	Hi-Z Output Capacitance	$\overline{OE}$ = 3V (Note 6)			3		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3V			50		mA
V_{OH}	High Level Output Voltage	I_O = –10µA I_O = –200µA	 ●	 2.7	2.995 2.99		V V
V_{OL}	Low Level Output Voltage	I_O = 10µA I_O = 1.6mA	 ●		0.005 0.09	 0.4	V V
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.1		V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Amplifier and Auxiliary DAC Operating Supply Range		●	2.85	3.0	3.4	V
V_{DD}	ADC Analog Supply Voltage		●	2.85	3.0	3.5	V
O_{VDD}	Output Supply Voltage		●	0.5	3.0	3.6	V
I_{CC}	Amplifier	DAC Powered Up, Both Amplifiers Enabled, LTM9002-AA	●		180	207	mA
		Both Amplifiers Enabled, LTM9002-LA	●		90	120	mA
$I_{CC(SHDN)}$	Amplifier Shutdown Supply Current	AMPSHDN = 3V, DAC Powered Down			0.7		mA
$I_{DD(ADC)}$	ADC Supply Current	LTM9002-AA	●		263	313	mA
		LTM9002-LA	●		140	159	mA
$P_{D(SHDN)}$	ADC Shutdown Power (Each Channel)	ADCSHDN = AMPSHDN = 3V, $\overline{OE}$ = 3V, No CLK			2		mW
$P_{D(NAP)}$	ADC Nap Mode Power (Each Channel)	ADCSHDN = AMPSHDN = 3V, $\overline{OE}$ = 0V, No CLK			15		mW
$P_{D(AMP)}$	Amplifier Power Dissipation	DAC Powered Up, LTM9002-AA			540		mW
		LTM9002-LA			270		mW
$P_{D(ADC)}$	ADC Power Dissipation	LTM9002-AA	●		790	939	mW
		LTM9002-LA	●		420	477	mW
$P_{D(TOTAL)}$	Total Power Dissipation	f_{SAMPLE} = MAX, LTM9002-AA f_{SAMPLE} = MAX, LTM9002-LA			1329 690		mW mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 6) (Not applicable for LTM9002-LA)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	LTM9002-AA	●	1		125	MHz
		LTM9002-LA	●	1		65	MHz
t_L	CLK Low Time	Duty Cycle Stabilizer Off (Note 6), LTM9002-AA Duty Cycle Stabilizer On (Note 6), LTM9002-AA	● ●	3.8 3	4 4	500 500	ns ns
t_H	CLK High Time	Duty Cycle Stabilizer Off (Note 6), LTM9002-AA Duty Cycle Stabilizer On (Note 6), LTM9002-AA	● ●	3.8 3	4 4	500 500	ns ns
t_L	CLK Low Time	Duty Cycle Stabilizer Off (Note 6), LTM9002-LA Duty Cycle Stabilizer On (Note 6), LTM9002-LA	● ●	7.3 5	7.7 7.7	500 500	ns ns
t_H	CLK High Time	Duty Cycle Stabilizer Off (Note 6), LTM9002-LA Duty Cycle Stabilizer On (Note 6), LTM9002-LA	● ●	7.3 5	7.7 7.7	500 500	ns ns
t_{AP}	Absolute Aperture Delay				0		ns
t_D	CLK to DATA Delay	C_L = 5pF (Note 6)	●	1.4	2.7	5.4	ns
t_C	CLK to CLKOUT Delay	C_L = 5pF (Note 6)	●	1.4	2.7	5.4	ns
	DATA to CLKOUT Skew	(t_D – t_C) (Note 6)	●	–0.6	0	0.6	ns
t_{MD}	MUX to DATA Delay	C_L = 5pF (Note 6)	●	1.4	2.7	5.4	ns
	DATA Access Time After $\overline{OE}\downarrow$	C_L = 5pF (Note 6)	●		4.3	10	ns
	BUS Relinquish Time	(Note 6)	●		3.3	8.5	ns
Pipeline Latency					5		Cycles
SPI Interface for Aux DACs, V_{DD} = 2.7V to 3.6V							
t_1	SDI Valid to SCK Setup			4			ns
t_2	SDI Valid to SCK Hold			4			ns
t_3	SCK High Time			9			ns
t_4	SCK Low Time			9			ns
t_5	$\overline{CS}$/LD Pulse Width			10			ns
t_6	LSB SCK High to $\overline{CS}$/LD			7			ns
t_7	$\overline{CS}$/LD Low to SCK High			7			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge			7			ns
	SCK Frequency 50% Duty Cycle					50	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: OV_{DD} = V_{CC} = V_{DD} = 3V, f_{SAMPLE} = MAX, input range = V_{IN} with differential drive, CLKA = CLKB, V_{INCM} = 1.25V, AMPSHDN = ADCSHDN = 0V, unless otherwise noted.

Note 4: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

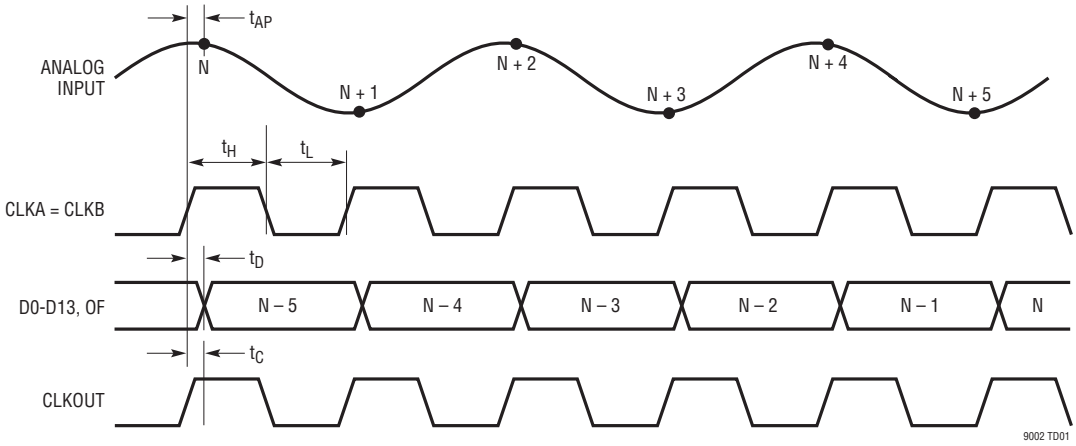
Note 5: Offset error is the output code resulting when the inputs are shorted together. The output code is converted to millivolts.

Note 6: Guaranteed by design, not subject to test.

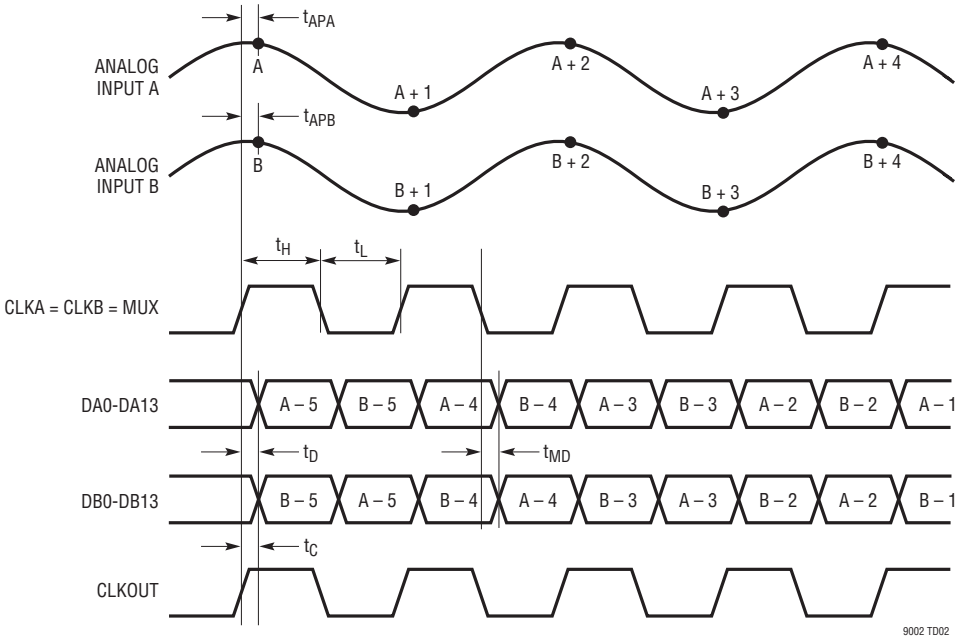
Note 7: V_{DD} = 3V, f_{SAMPLE} = MAX, input range = V_{IN} with differential drive. The supply current and power dissipation are the sum total for both channels with both channels active.

TIMING DIAGRAMS

Dual Digital Output Bus Timing

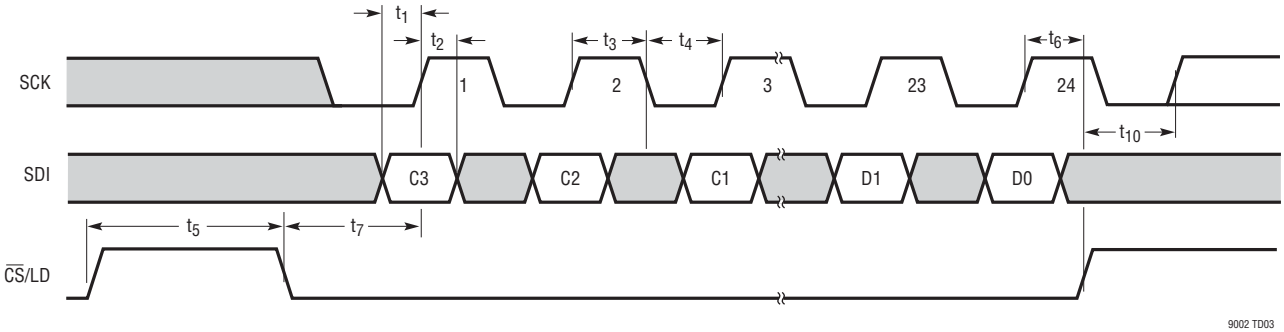


Multiplexed Digital Output Bus Timing



TIMING DIAGRAMS

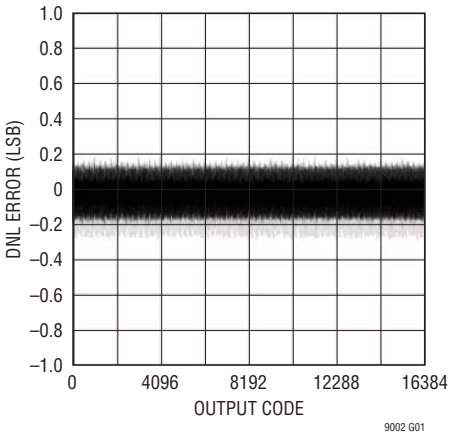
Auxiliary DAC Timing



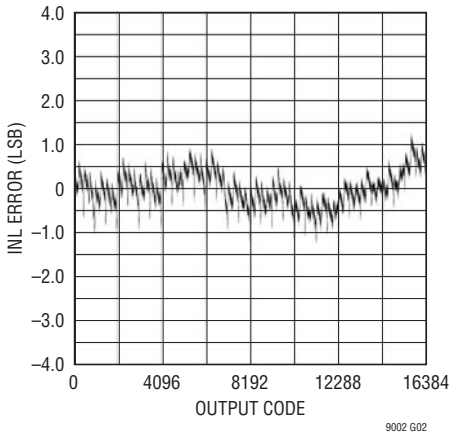
TYPICAL PERFORMANCE CHARACTERISTICS

(LTM9002-AA)

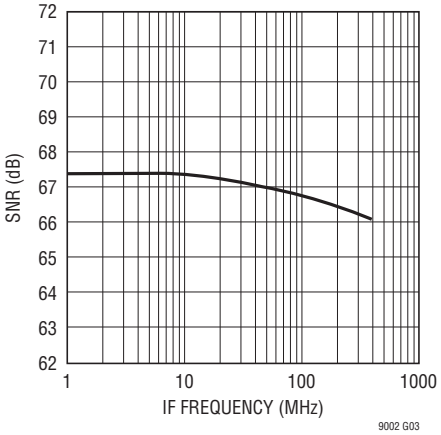
Differential Non-Linearity (DNL) vs Output Code



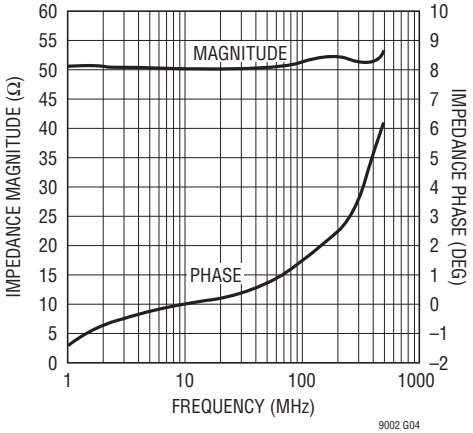
Integral Non-Linearity (INL), Best Fit vs Output Code



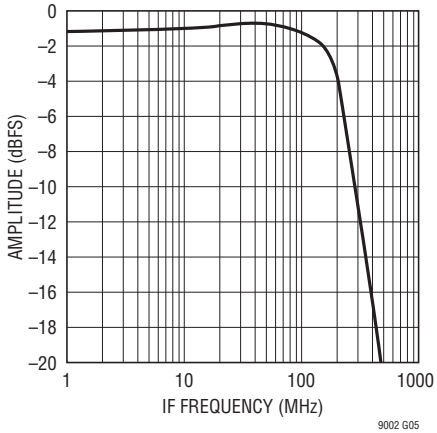
SNR vs Frequency



Input Impedance vs Frequency



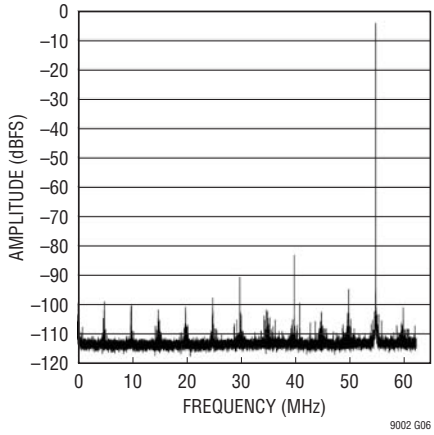
IF Frequency Response



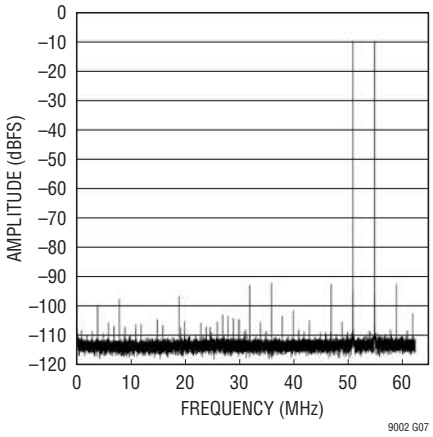
TYPICAL PERFORMANCE CHARACTERISTICS

(LTM9002-AA)

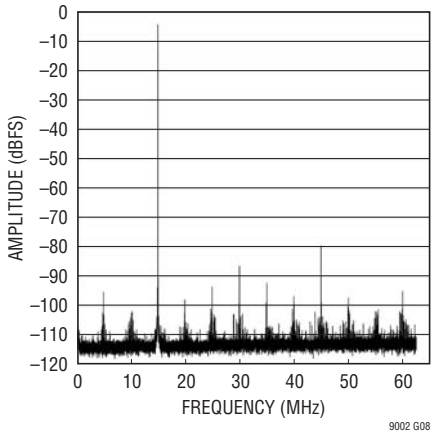
64k Point FFT, f_{IN} = 70MHz, –1dBFS, SENSE = V_{DD}



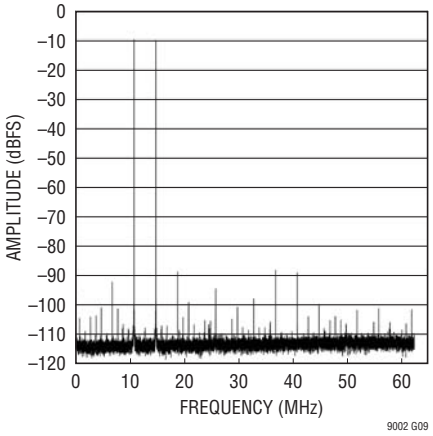
64k Point 2-Tone FFT, f_{IN} = 70MHz and f_{IN} = 74MHz, –7dBFS Per Tone, SENSE = V_{DD}



64k Point FFT, f_{IN} = 140MHz, –1dBFS, SENSE = V_{DD}

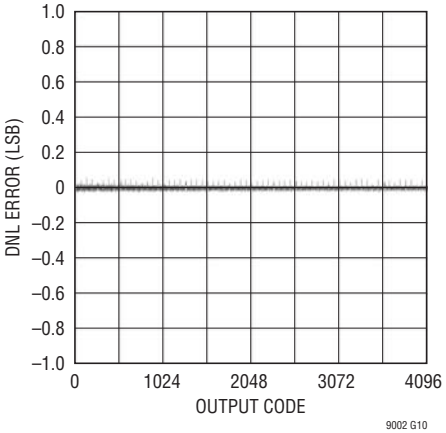


64k Point 2-Tone FFT, f_{IN} = 136MHz and f_{IN} = 140MHz, –7dBFS Per Tone, SENSE = V_{DD}

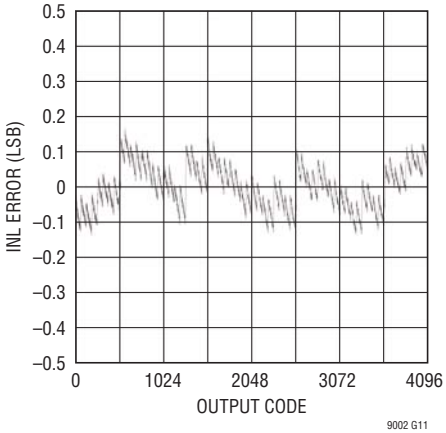


(LTM9002-LA)

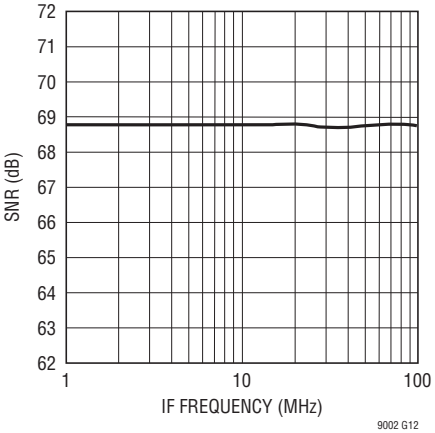
Differential Non-Linearity (DNL) vs Output Code



Integral Non-Linearity (INL), Best Fit vs Output Code

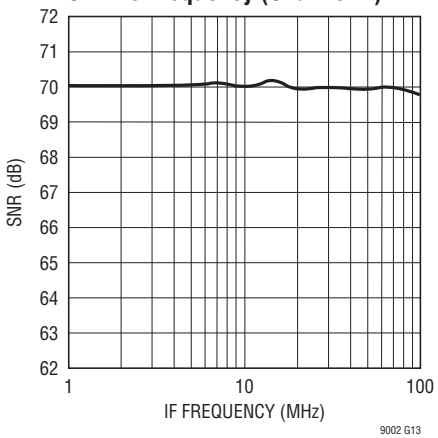


SNR vs Frequency (Channel A)

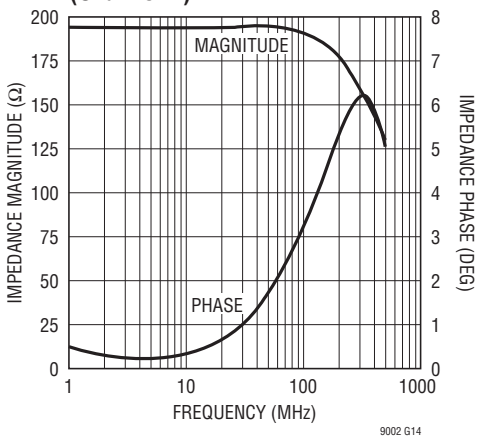


TYPICAL PERFORMANCE CHARACTERISTICS (LTM9002-LA)

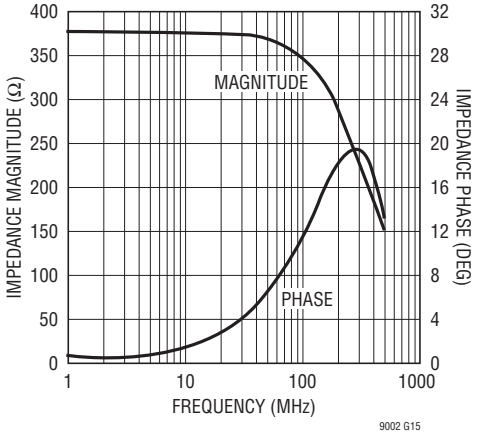
SNR vs Frequency (Channel B)



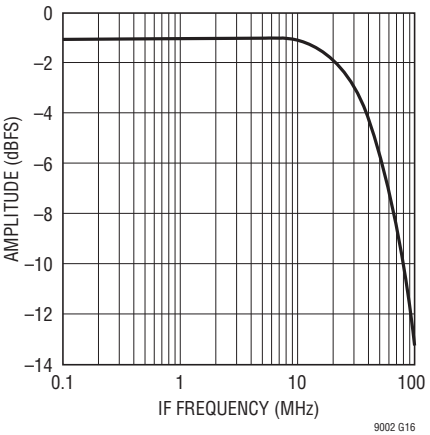
Input Impedance vs Frequency (Channel A)



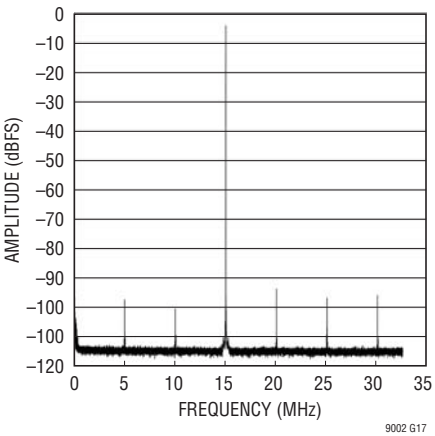
Input Impedance vs Frequency (Channel B)



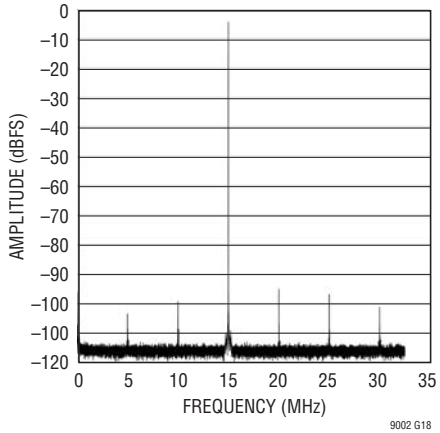
IF Frequency Response



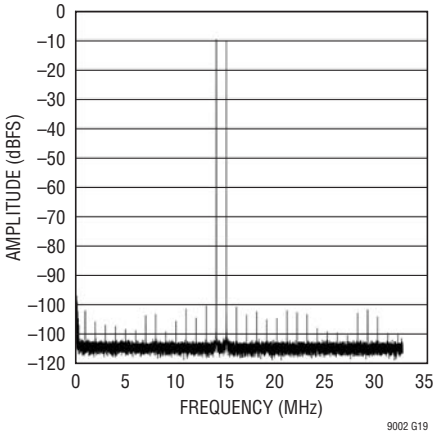
64k Point FFT, f_{IN} = 15MHz, –1dBFS, SENSE = V_{DD} (Channel A)



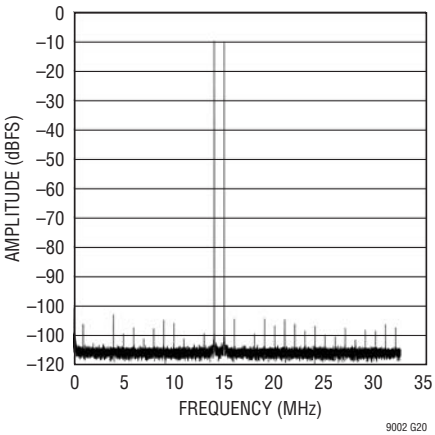
64k Point FFT, f_{IN} = 15MHz, –1dBFS, SENSE = V_{DD} (Channel B)



64k Point 2-Tone FFT, f_{IN} = z and f_{IN} = 15MHz, –7dBFS Per Tone, SENSE = V_{DD} (Channel A)



64k Point 2-Tone FFT, f_{IN} = 14MHz and f_{IN} = 15MHz, –7dBFS Per Tone, SENSE = V_{DD} (Channel B)



PIN FUNCTIONS

Supply Pins

GND (Pins A1-2, A5-7, B2-4, B6, C2-3, C6, D1-3, D5-7, D9-10, E5-6, E9-10, F1-2, F5-7, F9-10, G2-3, G6, H2-4, H6, J1-2, J5-7): ADC Power Ground.

OGND (Pins A12, C9, G9, J12): Output Driver Ground.

OV_{DD} (Pins B12, H12): Positive supply for the ADC output drivers. The specified operating range is 0.5V to 3.6V. OV_{DD} is internally bypassed to OGND.

V_{CC} (Pins E3, E4): Amplifier and Auxiliary DAC Power Supply. The specified operating range is 2.85V to 3.465V. The voltage on this pin provides power for the amplifier stage and auxiliary DACs only and is internally bypassed to GND. Note that LTM9002-LA does not have auxiliary DACs.

V_{DD} (Pins E7, E8): Analog 3V Supply for ADC. The specified operating range is 2.7V to 3.6V. V_{DD} is internally bypassed to GND.

Analog Inputs

CLKA (Pin A3): Channel A ADC Clock Input. The input sample starts on the positive edge.

CLKB (Pin A4): Channel B ADC Clock Input. The input sample starts on the positive edge.

DNC1 (Pin H5): Do Not Connect. These pins are used for testing and should not be connected on the PCB. They should be soldered to unconnected pads and should be well isolated. The DNC pins connect to the signal path prior to the ADC inputs; therefore, care should be taken to keep other signals away from these sensitive nodes. DNC1 connects near the channel A positive differential analog input.

DNC2 (Pin G5): Do Not Connect. These pins are used for testing and should not be connected on the PCB. They should be soldered to unconnected pads and should be well isolated. The DNC pins connect to the signal path prior to the ADC inputs; therefore, care should be taken to keep other signals away from these sensitive nodes. DNC2 connects near the channel A negative differential analog input.

DNC3 (Pin C5): Do Not Connect. These pins are used for testing and should not be connected on the PCB. They should be soldered to unconnected pads and should be well isolated. The DNC pins connect to the signal path prior to the ADC inputs; therefore, care should be taken to keep other signals away from these sensitive nodes. DNC3 connects near the channel B positive differential analog input.

DNC4 (Pin B5): Do Not Connect. These pins are used for testing and should not be connected on the PCB. They should be soldered to unconnected pads and should be well isolated. The DNC pins connect to the signal path prior to the ADC inputs; therefore, care should be taken to keep other signals away from these sensitive nodes. DNC4 connects near the channel B negative differential analog input.

DNC5 (Pin G4): Do Not Connect. This pin is used for testing and should not be connected on the PCB. It should be soldered to an unconnected pad and should be well isolated. This is a test point for the auxiliary DAC channel A voltage output.

DNC6 (Pin C4): Do Not Connect. This pin is used for testing and should not be connected on the PCB. It should be soldered to an unconnected pad and should be well isolated. This is a test point for the auxiliary DAC channel B voltage output.

INA^- (Pin G1): Channel A Negative (Inverting) Amplifier Input.

INA^+ (Pin H1): Channel A Positive (Noninverting) Amplifier Input.

INB^- (Pin C1): Channel B Negative (Inverting) Amplifier Input.

INB^+ (Pin B1): Channel B Positive (Noninverting) Amplifier Input.

PIN FUNCTIONS

Control Pins

ADCSHDNA (Pin G7): Channel A Shutdown Mode Selection Pin. Connecting ADCSHDNA to GND and $\overline{OEA}$ to GND results in normal operation with the outputs enabled. Connecting ADCSHDNA to GND and $\overline{OEA}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting ADCSHDNA to V_{DD} and $\overline{OEA}$ to GND results in nap mode with the outputs at high impedance. Connecting ADCSHDNA to V_{DD} and $\overline{OEA}$ to V_{DD} results in sleep mode with the outputs at high impedance.

ADCSHDNB (Pin C7): Channel B Shutdown Mode Selection Pin. Connecting ADCSHDNB to GND and $\overline{OEB}$ to GND results in normal operation with the outputs enabled. Connecting ADCSHDNB to GND and $\overline{OEB}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting ADCSHDNB to V_{DD} and $\overline{OEB}$ to GND results in nap mode with the outputs at high impedance. Connecting ADCSHDNB to V_{DD} and $\overline{OEB}$ to V_{DD} results in sleep mode with the outputs at high impedance.

AMPSHDNA (Pin E1): Power Shutdown Pin for Channel A Amplifier. This pin is a logic input referenced to analog ground. AMPSHDN = low results in normal operation. AMPSHDN = high results in powered down amplifier with a <1mA amplifier supply current.

AMPSHDNB (Pin E2): Power Shutdown Pin for Channel B Amplifier. This pin is a logic input referenced to analog ground. AMPSHDN = low results in normal operation. AMPSHDN = high results in powered down amplifier with a <1mA amplifier supply current.

MODE (Pin G8): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Note that MODE controls both channels. Connecting MODE to GND selects straight binary output format and turns the clock duty cycle stabilizer off. 1/3 V_{DD} selects straight binary output format and turns the clock duty cycle stabilizer on. 2/3 V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

MUX (Pin C8): Digital Output Multiplexer Control. If MUX = high, channel A comes out on DAx; channel B comes out on DBx. If MUX = low, the output busses are swapped and channel A comes out on DBx; channel B comes out on DAx. To multiplex both channels onto a single output bus, connect MUX, CLKA and CLKB together.

$\overline{OEA}$ (Pin F8): Channel A Output Enable Pin. Refer to ADCSHDNA pin function.

$\overline{OEB}$ (Pin D8): Channel B Output Enable Pin. Refer to ADCSHDNB pin function.

SENSEA (Pin J4): Channel A Reference Programming Pin. Connecting SENSEA to V_{DD} selects the internal reference and the higher input range. Connecting to 1.5V selects the lower range. An external reference greater than 0.5V and less than 1V applied to SENSEA selects an input range of $\pm V_{SENSEA}$/GAIN. See SENSE Pin Operation section.

SENSEB (Pin J3): Channel B Reference Programming Pin. Connecting SENSEB to V_{DD} selects the internal reference and the higher input range. Connecting to 1.5V selects the lower range. An external reference greater than 0.5V and less than 1V applied to SENSEB selects an input range of $\pm V_{SENSEB}$/GAIN. See SENSE Pin Operation section.

Digital Inputs (Not Connected on LTM9002-LA)

$\overline{CS}$/LD (Pin F3): Serial Interface Chip Select/Load Input for Auxiliary DAC. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 3) is executed.

SCK (Pin F4): Serial Interface Clock Input for Auxiliary DAC. CMOS and TTL compatible.

SDI (Pin D4): Serial Interface Data Input for Auxiliary DAC. Data is applied to SDI for transfer to the device at the rising edge of SCK. The auxiliary DAC accepts input word lengths of either 24 or 32 bits.

PIN FUNCTIONS

Digital Outputs

CLKOUT (Pin E12, LTM9002-AA): ADC Data Ready Clock Output. Latch data on the falling edge of CLKOUT. CLKOUT is derived from CLKB. Tie CLKA to CLKB for simultaneous operation.

OFB (Pin E12, LTM9002-LA): Overflow/Underflow Output. High when an overflow or underflow has occurred on channel B.

DA0 – DA13 (Refer to Pin Configuration Table): Channel A ADC Digital Outputs. DA13 is the MSB for LTM9002-AA; DA11 is the MSB for LTM9002-LA.

DB0 – DB13 (Refer to Pin Configuration Table): Channel B ADC Digital Outputs. DB13 is the MSB for LTM9002-AA; DB11 is the MSB for LTM9002-LA.

OF (Pin H7, LTM9002-AA): Overflow/Underflow Output. High when an overflow or underflow has occurred on either channel A or channel B.

OFA (Pin H7, LTM9002-LA): Overflow/Underflow Output. High when an overflow or underflow has occurred on channel A.

Pin Configuration (LTM9002-AA)

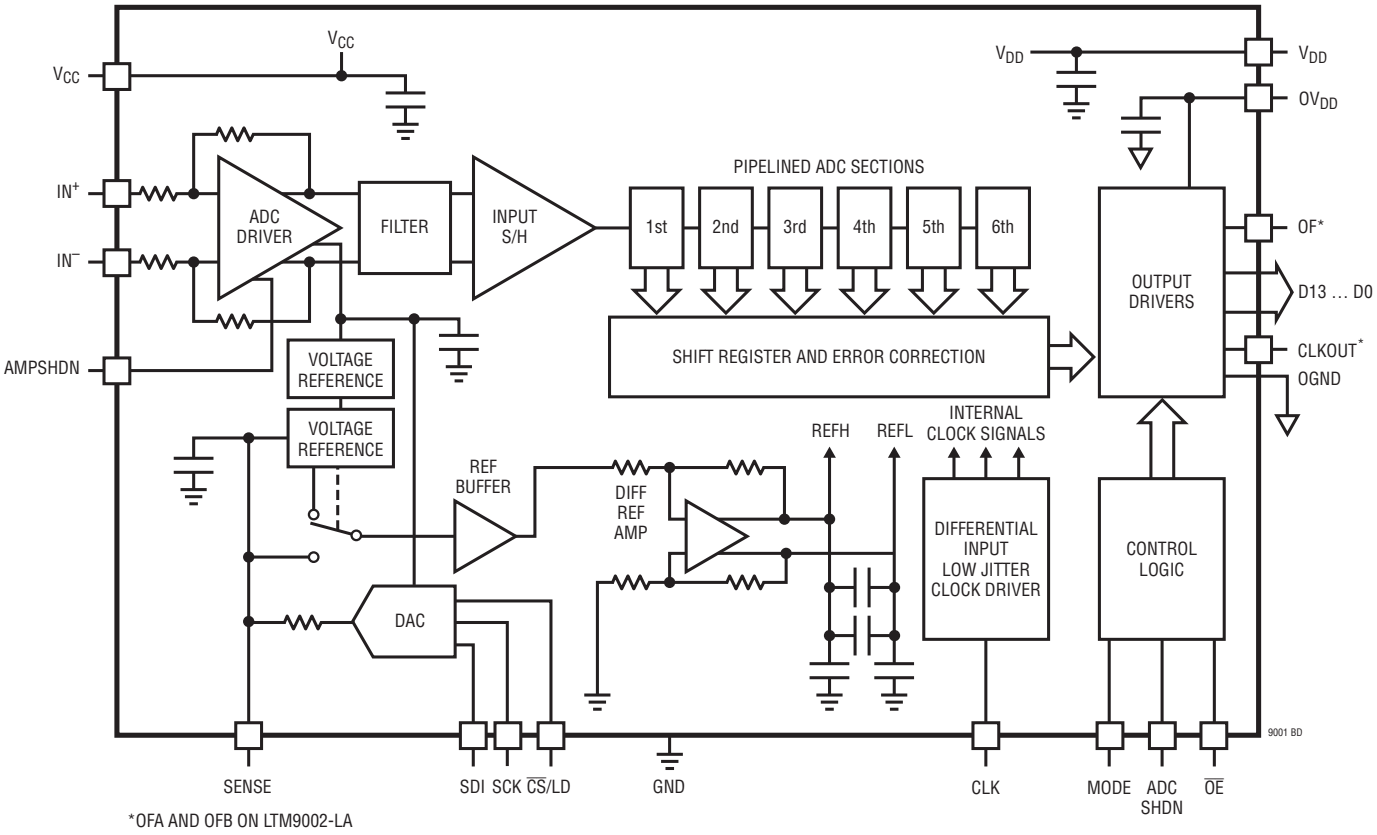
	1	2	3	4	5	6	7	8	9	10	11	12
J	GND	GND	SENSEB	SENSEA	GND	GND	GND	DA8	DA5	DA6	DA7	OGND
H	INA^+	GND	GND	GND	DNC1	GND	OF	DA10	DA12	DA11	DA9	OV_{DD}
G	INA^-	GND	GND	DNC5	DNC2	GND	ADC SHDNA	MODE	OGND	DA13	DA4	DA3
F	GND	GND	$\overline{CS}$/LD	SCK	GND	GND	GND	$\overline{OEA}$	GND	GND	DA2	DA1
E	AMP SHDNA	AMP SHDNB	V_{CC}	V_{CC}	GND	GND	V_{DD}	V_{DD}	GND	GND	DA0	CLKOUT
D	GND	GND	GND	SDI	GND	GND	GND	$\overline{OEB}$	GND	GND	DB13	DB12
C	INB^-	GND	GND	DNC6	DNC3	GND	ADC SHDNB	MUX	OGND	DB1	DB11	DB10
B	INB^+	GND	GND	GND	DNC4	GND	DB0	DB4	DB2	DB3	DB5	OV_{DD}
A	GND	GND	CLKA	CLKB	GND	GND	GND	DB6	DB9	DB8	DB7	OGND

Pin Configuration (LTM9002-LA)

	1	2	3	4	5	6	7	8	9	10	11	12
J	GND	GND	SENSEB	SENSEA	GND	GND	GND	DA6	DA3	DA4	DA5	OGND
H	INA^+	GND	GND	GND	DNC1	GND	OFA	DA8	DA10	DA9	DA7	OV_{DD}
G	INA^-	GND	GND	DNC5	DNC2	GND	ADC SHDNA	MODE	OGND	DA11	DA2	DA1
F	GND	GND	NC	NC	GND	GND	GND	$\overline{OEA}$	GND	GND	DA0	NC
E	AMP SHDNA	AMP SHDNB	V_{CC}	V_{CC}	GND	GND	V_{DD}	V_{DD}	GND	GND	NC	OFB
D	GND	GND	GND	NC	GND	GND	GND	$\overline{OEB}$	GND	GND	DB11	DB10
C	INB^-	GND	GND	DNC6	DNC3	GND	ADC SHDNB	MUX	OGND	NC	DB9	DB8
B	INB^+	GND	GND	GND	DNC4	GND	NC	DB2	DB0	DB1	DB3	OV_{DD}
A	GND	GND	CLKA	CLKB	GND	GND	GND	DB4	DB7	DB6	DB5	OGND

BLOCK DIAGRAM

Functional Block Diagram (Only One Channel is Shown)



*OFA AND OFB ON LTM9002-LA

OPERATION

DYNAMIC PERFORMANCE DEFINITIONS

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\sqrt{\left(V2^2 + V3^2 + V4^2 + \ldots Vn^2\right)} / V1$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. The 3rd order intermodulation products are 2fa + fb, 2fb + fa, 2fa – fb and 2fb – fa. The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Aperture Delay Time

The time from when CLK reaches mid supply to the instant that the input signal is held by the sample and hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal-to-noise ratio due to the jitter alone will be:

$$SNRJITTER = -20\log(2\pi) \bullet f_{IN} \bullet t_{JITTER}$$

Crosstalk

The amount of signal coupled from one channel into the other. This is measured by applying a full-scale sinusoidal input on channel A, shorting the inputs of channel B and taking the ratio of the signal powers in an FFT.

OPERATION

Description

The LTM9002 is an integrated system in a package (SiP) that includes two high-speed 14-bit A/D converters, matching networks, anti-aliasing filters and two low noise, differential amplifiers with fixed gain. These amplifiers need not be the same, so that the gains and input impedances of the two channels are different. Also included is a pair of auxiliary DACs to allow for digital, full-scale adjustment of each channel. The LTM9002 is designed for digitizing high frequency, wide dynamic range signals with input frequencies up to 300MHz. Typical applications include digitizing in-phase and quadrature channels or main and diversity channels in base station applications.

The following sections describe in further detail the operation of each section. The SiP technology allows the LTM9002 to be customized and this is described in the first section. The outline of the remaining sections follows the basic functional elements as shown in Figure 1.

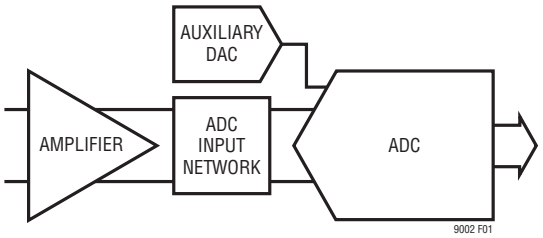


Figure 1. Basic Functional Elements

Semi-Custom Options

The µModule construction affords a new level of flexibility in application-specific standard products. Standard ADC and amplifier components can be integrated regardless of their process technology and matched with passive components to a particular application. The LTM9002-AA, as the first example, is configured with a dual 14-bit ADC sampling at rates up to 125Msps. The amplifier gain is 26dB with an input impedance of 50Ω and an input range of $100mV_{P-P}$ (–16dBm). The matching network is designed to optimize the interface between the amplifier output and the ADC under these conditions. Additionally, there is a 3rd order lowpass filter with a cutoff at 170MHz. The auxiliary DACs allow adjustment of the full-scale range with 12-bit resolution.

However, other options are possible through Linear Technology's semi-custom development program. Linear Technology has in place a program to deliver other speed, resolution, IF range, gain and filter configurations for nearly any specified application. These semi-custom designs are based on existing ADCs and amplifiers with an appropriately modified matching network. The final subsystem is then tested to the exact parameters defined for the application. The final result is a fully integrated, accurately tested and optimized solution in the same package. For more details on the semi-custom receiver subsystem program, contact Linear Technology.

Table 1. Semi-Custom Options

AMPLIFIER IF RANGE	AMPLIFIER INPUT IMPEDANCE	AMPLIFIER GAIN	FILTER	ADC SAMPLE RATE	ADC RESOLUTION	AUXILIARY DAC	PART NUMBER
300MHz	50Ω	26dB	170MHz LPF	125Msps	14-Bit	12-Bit, SPI	LTM9002-AA
140MHz	200Ω (Channel A) 400Ω (Channel B)	20dB (Channel A) 8dB (Channel B)	25MHz LPF	65Msps	12-Bit	None	LTM9002-LA
Select Combination of Options from Columns Below							
DC-300MHz	50Ω	26dB	TBD	125Msps	14-Bit	12-Bit, I^2C	
DC-140MHz	200Ω	20dB		105Msps	12-Bit	None	
DC-70MHz	200Ω	14dB		80Msps	10-Bit		
DC-35MHz	400Ω	8dB		65Msps			
				40Msps			
				25Msps			
				10Msps			

OPERATION

Note that not all combinations in Table 1 are possible at this time and specified performance may differ significantly from existing values.

AMPLIFIER OPERATION

The amplifiers used in the LTM9002 are low noise and low distortion fully differential op amps/ADC drivers with operation from DC to 2GHz (–3dB bandwidth). The amplifiers are composed of fully differential amplifiers with on chip feedback and output common mode voltage control circuitry. Differential gain and input impedance are set by internal resistors in the feedback network.

Table 2. Amplifier Gain and Input Impedance

GAIN (dB)	GAIN (V/V)	Z_{IN} (DIFFERENTIAL)
8	2.5	400Ω
14	5	200Ω
20	10	200Ω
26	20	50Ω

The amplifiers are very flexible in terms of I/O coupling. They can be AC- or DC-coupled at the inputs. Due to the internal connection between input and output, users are advised to keep input common mode voltage between 1V and 1.7V for proper operation. If the inputs are AC-coupled, the input common mode voltage is automatically biased close to the ADC input common mode voltage and thus no external circuitry is needed for bias. The input signal can be either single-ended or differential with some difference in distortion performance.

ADC INPUT NETWORK

The passive network between the amplifier output stage and the ADC input stage provides a 3rd order topology that can be configured for bandpass or lowpass response and different cutoff frequencies and bandwidths. LTM9002-AA, for example, implements a lowpass filter designed for 170MHz.

CONVERTER OPERATION

As shown in the Block Diagram, the analog-to-digital converter (ADC) is a dual CMOS pipelined multistep converter. The converter has six pipelined ADC stages; a sampled analog input will result in a digitized value six cycles later (see the Timing Diagram section). The CLK inputs are single-ended. The ADC has two phases of operation, determined by the state of the CLK input pins.

Each pipelined stage shown in the Block Diagram contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and visa versa.

When CLK is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "Input S/H" shown in the Block Diagram. At the instant that CLK transitions from low to high, the sampled input is held. While CLK is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of CLK. When CLK goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When CLK goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third, fourth and fifth stages, resulting in a fifth stage residue that is sent to the sixth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

AUXILIARY DAC OPERATION

The full-scale voltage span of each ADC is controlled by an auxiliary voltage output DAC connected to SENSE. Series resistance in the DAC output allows an external voltage to override the DAC.

The internal reference sets both auxiliary DACs to a full-scale range to 1.5V. Programming the DAC to generate an internal voltage greater than or less than the external

OPERATION

reference adjusts the ADC span proportionately; see Adjusting the full-scale input range. Powering down the auxiliary DAC disables the ADC span trim control. When the auxiliary DAC is powered down, connect SENSE to V_{DD} or an external reference.

Power-On Reset

The auxiliary DACs clear the outputs to zero-scale when power is first applied, making system initialization consistent and repeatable.

Transfer Function

The digital-to-analog transfer function is;

$$V_{OUT(IDEAL)} = (k/2^N) V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and V_{REF} is 1.5V, the internal reference voltage of the ADC.

Serial Interface

All serial interface pins ($\overline{CS}$/LD, SCK and SDI) have TTL input levels and are 5V tolerant. The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, activating the SDI and SCK buffers and enabling the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 12-bit input code, ordered MSB-to-LSB, followed by 4 don't-care bits. Data can only be transferred to the device when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 3.

The command (C3-C0) and address (A3-A0) assignments are shown in Table 3. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register of the selected DAC, *n*. An update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 12-bit input code, and is converted to an analog voltage at the DAC output. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

While the minimum input word is 24-bits, it may optionally be extended to 32-bits to accommodate microprocessors which have a minimum word width of 16 bits (2 bytes). To use the 32-bit word width, 8 don't-care bits are transferred to the device first, followed by the 24-bit word as just described. Figure 4 shows the 32-bit sequence.

Power-Down Mode

Either or both DAC channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address, *n*. The 16-bit data word is ignored.

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 3. The selected DAC is powered up as its voltage output is updated. If both DACs are powered down, then the main bias generation circuit block has been automatically shut down in addition to the individual DAC amplifiers and reference inputs. In this case, the power-up delay time is 700µs (for V_{CC} = 3V).

Table 3. Auxiliary DAC Commands

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register *n*
0	0	0	1	Update (Power-Up) DAC Register *n*
0	0	1	0	Write to Input Register *n*, Update (Power Up) All *n*
0	0	1	1	Write to and Update (Power-Up) *n*
0	1	0	0	Power Down *n*
1	1	1	1	No Operation
ADDRESS (*n*)*				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
1	1	1	1	All DACs

*Command and address codes not shown are reserved and should not be used.

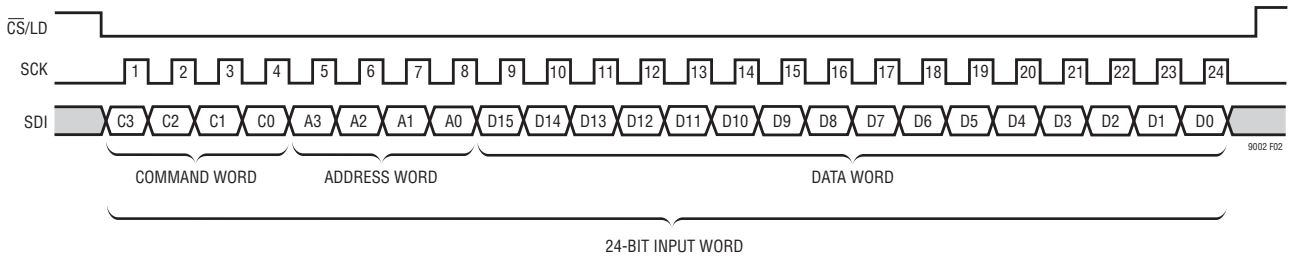


Figure 2. Auxiliary DAC 24-Bit Load Sequence (Minimum Input Word)

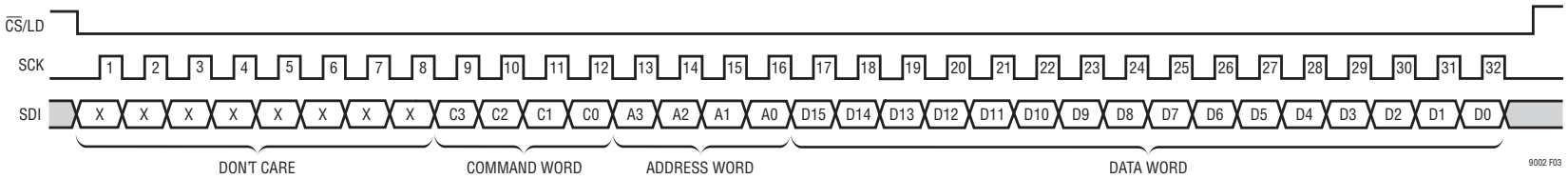


Figure 3. Auxiliary DAC 32-Bit Load Sequence

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INPUT SPAN

The LTM9002 is configured with a given input span and input impedance. With the amplifier gain and the ADC input network described above for LTM9002-AA, the full-scale input range of the driver circuit is $0.1V_{P-P}$. The recommended ADC input span is achieved by tying the SENSE pin to V_{DD}. However, the ADC input span can be changed if required for the application. The resulting input span at the IN^+/IN^- pins is the ADC input span divided by the gain.

The LTM9002 is intended to be driven through the IN^+ and IN^- pins. The DNC pins are used for test purposes and are not intended to be used in the application. These are test points within the ADC input filter network. However, care should be taken with these pins as they connect directly to the internal signal path. They should be soldered to an unconnected pad and should be well isolated.

Input Impedance and Matching

The input impedance of the amplifier is 50Ω, 200Ω or 400Ω depending on the gain of the amplifier. In some applications the differential inputs may need to be terminated to a lower value impedance, e.g. 50Ω, in order to provide an impedance match for the source. Several choices are available.

One approach is to use a differential shunt resistor (Figure 4). Another approach is to employ a wide band transformer and shunt resistor (Figure 5). Both methods provide a wide band match. The termination resistor or the transformer must be placed close to the input pins in order to minimize the reflection due to input mismatch.

Alternatively, one could apply a narrowband impedance match at the inputs for frequency selection and/or noise reduction.

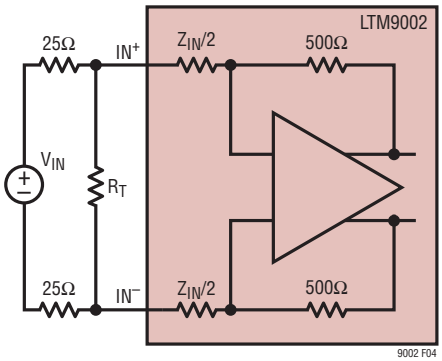

Figure 4. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor

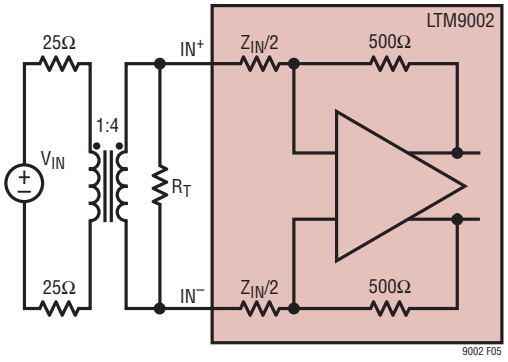

Figure 5. Input Termination for Differential 50Ω Input Impedance Using a Balun

Referring to Figure 6, amplifier inputs can be easily configured for single-ended input without a balun. The signal is fed to one of the inputs through a matching network while the other input is connected to the same matching network and a source resistor. Because the return ratios of the two feedback paths are equal, the two outputs have the same gain and thus symmetrical swing. In general, the single-ended input impedance and termination resistor R_T are determined by the combination of R_S, R_G and R_F, see Table 5.

Table 4. Differential Amplifier Input Termination Values

GAIN (dB)	$Z_{IN}/2$	R_T FIGURE 4	R_T FIGURE 5
8	200Ω	57Ω	400Ω
14	100Ω	66.5Ω	None
20	100Ω	66.5Ω	None
26	25Ω	None	None

Table 5. Single-Ended Amplifier Input Termination Values

GAIN (dB)	$Z_{IN}/2$	R_T FIGURE 6
8	200Ω	59Ω
14	100Ω	68.5Ω
20	100Ω	66.5Ω
26	25Ω	150Ω

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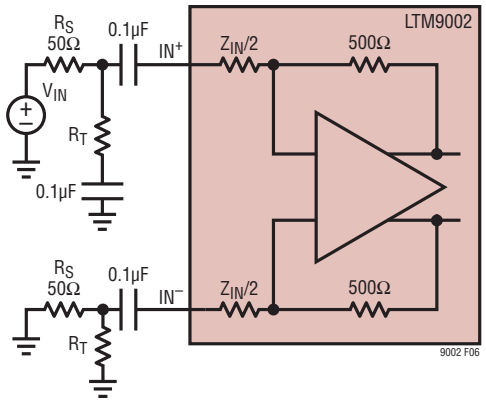

Figure 6. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor

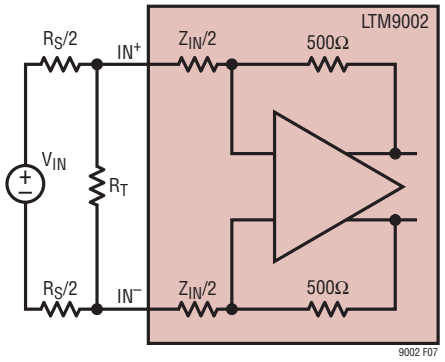

Figure 7. Calculate Differential Gain

The amplifier is unconditionally stable, i.e. differential stability factor Kf > 1 and stability measure B1 > 0. However, the overall differential gain is affected by the source impedance in Figure 7:

$$AV = | V_{OUT}/V_{IN} | = (500/(R_S + Z_{IN}/2)$$

The noise performance of the amplifier also depends upon the source impedance and termination. For example, an input 1:4 transformer in Figure 5 improves the input noise figure by adding 6dB gain at the inputs. A trade-off between gain and noise is obvious when constant noise figure circle and constant gain circle are plotted within the input Smith Chart, based on which users can choose the optimal source impedance for a given gain and noise requirement.

SENSE Pin Operation

The internal voltage reference can be configured for two pin-selectable input ranges of 0.1V (±50mV differential) or 0.5V (±25mV differential) for LTM9002-AA. Tying the SENSE pin to V_{DD} selects the higher range; tying the SENSE pin to 1.5V selects the lower range. For other versions of LTM9002, the input span is either $2V_{P-P}$ divided by the gain or $1V_{P-P}$ divided by the gain.

An external reference can be used by applying its output directly or through a resistive divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. The SENSE pin is internally bypassed to ground with a 1µF ceramic capacitor.

Input Range

The input range can be set based on the application. The 0.1V input range (LTM9002-AA) will provide the best SNR performance while maintaining excellent SFDR. The lower input range will have slightly better SFDR performance, but the SNR will degrade by 5dB. See the Typical Performance Characteristics section.

Adjusting the Full-Scale Input Range

To trim the full-scale range of one channel to match that of the other channel, first set the desired range for both channels by applying an external reference to SENSEA and SENSEB as shown in Figure 8. Set the DAC codes to approximately match the external reference voltage. Apply a full-scale voltage to the input of each channel. Read the output of both channels and adjust the setting for the DAC of one channel until the desired channel matching has been achieved.

The adjustment range and step size depends on the resistor values chosen for or the source resistance of the external reference circuit. The external reference is connected to the SENSE pin which has 10k (±1%) series impedance with the internal DAC voltage. For the circuit shown in Figure 8, the step size is 76µV and the code representing 1V is 0xAAB (0.666748 decimal). In this example, the SENSE voltage trim range is from approximately 0.79V to 1.1V including offset and gain errors. Therefore, the effective input span can be trimmed from ±39.6mV to 55.2mV with a step size of 3.8µV. However, it is not recommended to

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exceed ±50mV. The internal 1000pF capacitor provides a corner frequency of 64kHz when used with the 2.5k external resistor. An additional 0.1µF bypass capacitor may be required at the SENSE pin.

The auxiliary DACs can be used without an external reference in applications that are not sensitive to close-in phase noise such as CCD imaging or oversampling of low amplitude signals. Without an external reference, the DAC step size will be 366µV at the SENSE pin which results in a 18µV step for the input span. In this case, the SENSE pin may be bypassed with 0.1µF capacitor.

The auxiliary DACs must be subsequently set each time the LTM9002 is powered up.

Driving the Clock Inputs

The CLK inputs can be driven directly with a CMOS or TTL level signal. A sinusoidal clock can also be used along with a low-jitter squaring circuit before the CLK pin (Figure 9).

The noise performance of the ADC can depend on the clock signal quality as much as on the analog input. Any noise present on the CLK signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter. In applications where jitter is critical, such as when digitizing high input frequencies, use as large an amplitude as possible. Also, if the ADC is clocked with a sinusoidal signal, filter the CLK signal to reduce wideband noise and distortion products generated by the source.

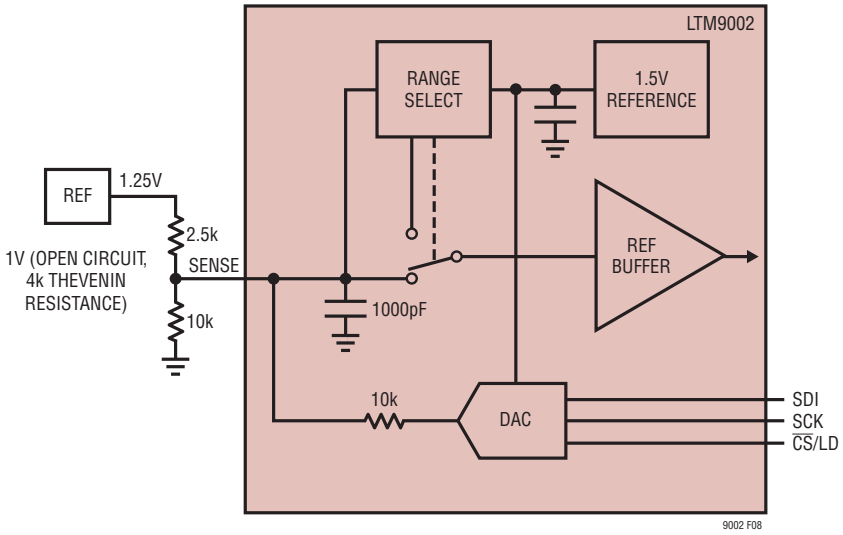

Figure 8. Using an External Reference

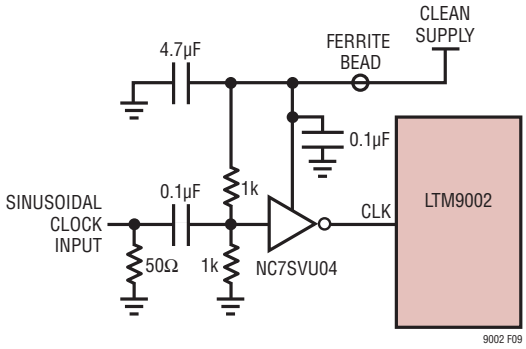

Figure 9. Sinusoidal Single-Ended CLK Driver

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It is recommended that CLKA and CLKB are shorted together and driven by the same clock source. If a small time delay is desired between when the two channels sample the analog inputs, CLKA and CLKB can be driven by two different signals. If this time delay exceeds 1ns, the performance of the part may degrade. CLKA and CLKB should not be driven by asynchronous signals.

Figure 10 and Figure 11 show alternatives for converting a differential clock to the single-ended CLK input. The use of a transformer provides no incremental contribution to phase noise. The LVDS or PECL to CMOS translators provide little degradation below 70MHz, but at 140MHz will degrade the SNR compared to the transformer solution. The nature of the received signals also has a large bearing on how much SNR degradation will be experienced. For high crest factor signals such as WCDMA or OFDM, where the nominal power level must be at least 6dB to 8dB below full-scale, the use of these translators will have a lesser impact.

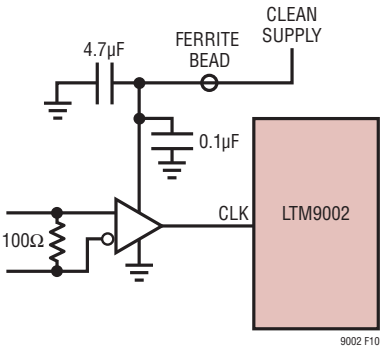

Figure 10. CLK Driver Using an LVDS or PECL to CMOS Converter

The transformer in the example may be terminated with the appropriate termination for the signaling in use. The use of a transformer with a 1:4 impedance ratio may be desirable in cases where lower voltage differential signals are considered. The center tap may be bypassed to ground through a capacitor close to the ADC if the differential signals originate on a different plane. The use of a capacitor at the input may result in peaking, and depending on transmission line length may require a 10Ω to 20Ω series resistor to act as both a lowpass filter for high frequency noise that may be induced into the clock line by neighboring digital signals, as well as a damping mechanism for reflections.

Maximum and Minimum Conversion Rates

The maximum conversion rate for the LTM9002-AA is 125Msps and the LTM9002-LA is 65Msps. The lower limit of the sample rate is determined by the droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTM9002 is 1Msps.

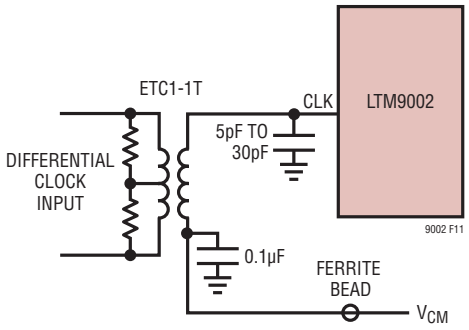

Figure 11. LVDS or PECL CLK Driver Using a Transformer

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Clock Duty Cycle Stabilizer

An optional clock duty cycle stabilizer circuit ensures high performance even if the input clock has a non 50% duty cycle. Using the clock duty cycle stabilizer is recommended for most applications. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

This circuit uses the rising edge of the CLK pin to sample the analog input. The falling edge of CLK is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 40% to 60% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require a hundred clock cycles for the PLL to lock onto the input clock.

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. If the duty cycle stabilizer is disabled, care should be taken to make the sampling clock have a 50% (±5%) duty cycle.

DIGITAL OUTPUTS

Table 6 shows the relationship between the analog input voltage, the digital data bits, and the overflow bit. Note that OF is high when an overflow or underflow has occurred on either channel A or channel B.

Table 6. Output Codes vs Input Voltage, 100mV Input Span

$IN^+ – IN^-$ (SENSE = V_{DD})	OF	D13 - D0 (OFFSET BINARY)	D13 - D0 (2'S COMPLEMENT)
≥ 50mV	1	11 1111 1111 1111	01 1111 1111 1111
	0	11 1111 1111 1111	01 1111 1111 1111
	0	11 1111 1111 1110	01 1111 1111 1110
0.000000V	0	10 0000 0000 0001	00 0000 0000 0001
	0	10 0000 0000 0000	00 0000 0000 0000
	0	01 1111 1111 1111	11 1111 1111 1111
	0	01 1111 1111 1110	11 1111 1111 1110
≤ –50mV	0	00 0000 0000 0001	10 0000 0000 0001
	0	00 0000 0000 0000	10 0000 0000 0000
	1	00 0000 0000 0000	10 0000 0000 0000

Digital Output Modes

Figure 12 shows an equivalent circuit for a single output buffer. Each buffer is powered by O_{VDD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

As with all high speed/high resolution converters the digital output loading can affect the performance. The digital outputs of the ADC should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. For full-speed operation, the capacitive load should be kept under 10pF.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

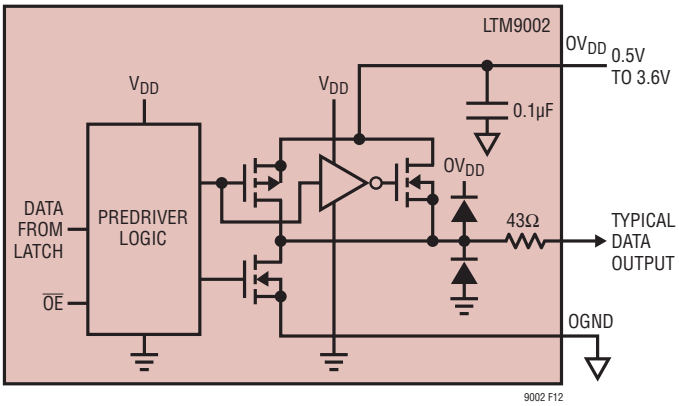

Figure 12. Digital Output Buffer

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Data Format

Using the MODE pin, the ADC parallel digital output can be selected for offset binary or 2's complement format. Note that MODE controls both channel A and channel B. Connecting MODE to GND or 1/3 V_{DD} selects straight binary output format. Connecting MODE to 2/3 V_{DD} or V_{DD} selects 2's complement output format. An external resistive divider can be used to set the 1/3 V_{DD} or 2/3 V_{DD} logic values. Table 7 shows the logic states for the MODE pin.

Table 7. MODE Pin Function

MODE PIN	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0	Straight Binary	Off
1/3V_{DD}	Straight Binary	On
2/3V_{DD}	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

For LTM9002-AA, when OF outputs a logic high the converter is either overranged or underranged on channel A or channel B. Note that both channels share a common OF pin. OF is disabled when channel A is in sleep or nap mode. For LTM9002-LA, OFA and OFB indicate either condition for the respective channel.

Output Clock

The LTM9002-AA has a delayed version of the CLKB input available as a digital output, CLKOUT. The falling edge of the CLKOUT pin can be used to latch the digital output data. CLKOUT is disabled when channel B is in sleep or nap mode.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same supply that powers the logic being driven. For example, if the converter drives a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply.

OV_{DD} can be powered with any voltage from 500mV up to 3.6V, independent of V_{DD}. OGND can be powered with any voltage from GND up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Output Enable

The outputs may be disabled with the output enable pin, $\overline{OE}$. $\overline{OE}$ high disables all data outputs including OF. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full-speed operation. The output Hi-Z state is intended for use during test or initialization. Channels A and B have independent output enable pins ($\overline{OEA}$, $\overline{OEB}$.)

Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting ADCSHDN to GND results in normal operation. Connecting ADCSHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode, which powers down all circuitry including the reference and the ADC typically dissipates 1mW. When exiting sleep mode, it will take 700µs to 1ms for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting ADCSHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode and the ADC typically dissipates 30mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap modes, all digital outputs are disabled and enter the Hi-Z state.

Channels A and B have independent ADCSHDN pins (ADCSHDNA, ADCSHDNB.) Channel A is controlled by ADCSHDNA and $\overline{OEA}$, and channel B is controlled by ADCSHDNB and $\overline{OEB}$. The nap, sleep and output enable modes of the two channels are completely independent, so it is possible to have one channel operating while the other channel is in nap or sleep mode.

Digital Output Multiplexer

The digital outputs of the ADC can be multiplexed onto a single data bus. The MUX pin is a digital input that swaps the two data busses. If MUX is high, channel A comes out on DAx; channel B comes out on DBx. If MUX is low,