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14-Bit, 65Msps/40Msps/ 25Msps Low Power Octal ADCs

FEATURES

- **8-Channel Simultaneous Sampling ADC**
- **73dB SNR**
- **90dB SFDR**
- Low Power: 88mW/59mW/46mW per Channel
- Single 1.8V Supply
- Serial LVDS Outputs: 1 or 2 Bits per Channel
- Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$
- 800MHz Full Power Bandwidth S/H
- Shutdown and Nap Modes
- Serial SPI Port for Configuration
- Internal Bypass Capacitance, No External Components
- 140-Pin (11.25mm × 9mm) BGA Package

APPLICATIONS

- Communications
- Cellular Base Stations
- Software Defined Radios
- Portable Medical Imaging
- Multichannel Data Acquisition
- Nondestructive Testing

DESCRIPTION

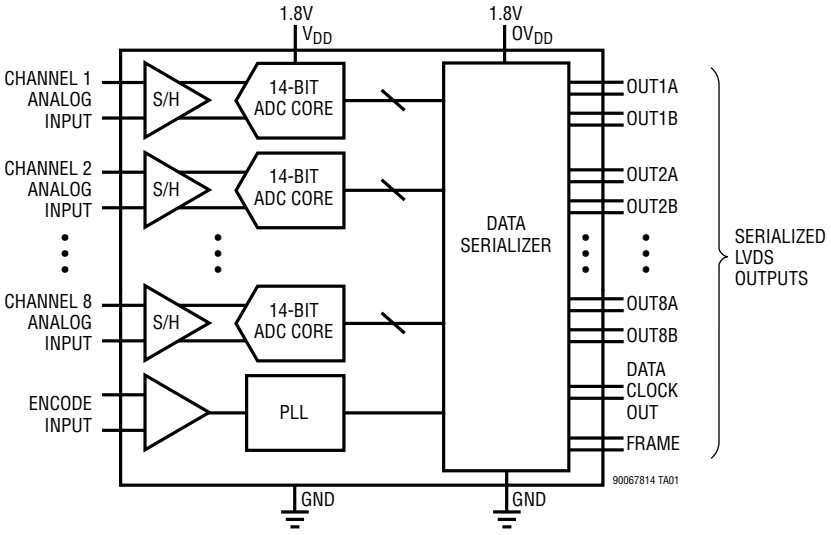
The LTM®9008-14/LTM9007-14/LTM9006-14 are 8-channel, simultaneous sampling 14-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. AC performance includes 73dB SNR and 90dB spurious free dynamic range (SFDR). Low power consumption per channel reduces heat in high channel count applications. Integrated bypass capacitance and flowthrough pinout reduces overall board space requirements.

DC specs include ±1LSB INL (typ), ±0.3LSB DNL (typ) and no missing codes over temperature. The transition noise is a low $1.2LSB_{RMS}$.

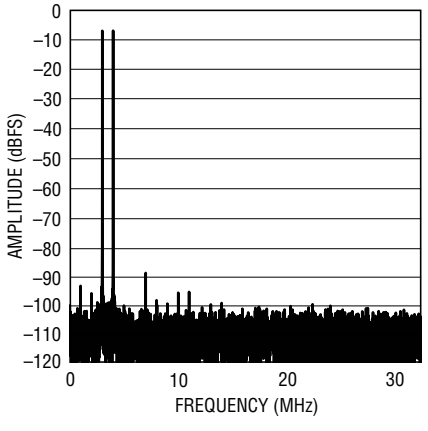
The digital outputs are serial LVDS to minimize the number of data lines. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode).

The ENC^+ and ENC^- inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL, or CMOS inputs. An internal clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION



LTM9008-14, 65Msps, 2-Tone FFT, f_{IN} = 70MHz and 75MHz

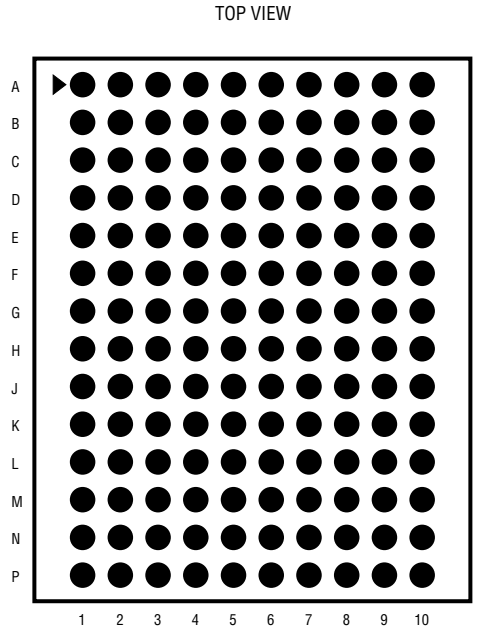


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages
V_{DD}, OV_{DD} ..... –0.3V to 2V
Analog Input Voltage (A_{IN}^+, A_{IN}^-,
PAR/$\overline{SER}$, SENSE) (Note 3) ..... –0.3V to (V_{DD} + 0.2V)
Digital Input Voltage (ENC^+, ENC^-, $\overline{CS}$,
SDI, SCK) (Note 4) ..... –0.3V to 3.9V
SDO (Note 4) ..... –0.3V to 3.9V
Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)
Operating Temperature Range
LTM9008C, LTM9007C, LTM9006C ..... 0°C to 70°C
LTM9008I, LTM9007I, LTM9006I ..... –40°C to 85°C
Storage Temperature Range ..... –55°C to 125°C

PIN CONFIGURATION



BGA PACKAGE
140-LEAD (11.25mm × 9.00mm × 2.72mm)

T_{JMAX} = 150°C, θ_{JA} = 30°C/W, θ_{JC} = 25°C/W, θ_{JB} = 15°C/W, $\theta_{JCbottom}$ = 12°C/W

ORDER INFORMATION

http://www.linear.com/product/LTM9008-14#orderinfo

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9008CY-14#PBF	LTM9008CY-14#PBF	LTM9008Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	0°C to 70°C
LTM9008IY-14#PBF	LTM9008IY-14#PBF	LTM9008Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	–40°C to 85°C
LTM9007CY-14#PBF	LTM9007CY-14#PBF	LTM9007Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	0°C to 70°C
LTM9007IY-14#PBF	LTM9007IY-14#PBF	LTM9007Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	–40°C to 85°C
LTM9006CY-14#PBF	LTM9006CY-14#PBF	LTM9006Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	0°C to 70°C
LTM9006IY-14#PBF	LTM9006IY-14#PBF	LTM9006Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		LTM9008-14 MIN	LTM9008-14 TYP	LTM9008-14 MAX	LTM9007-14 MIN	LTM9007-14 TYP	LTM9007-14 MAX	LTM9006-14 MIN	LTM9006-14 TYP	LTM9006-14 MAX	UNITS
Resolution (No Missing Codes)		●	14			14			14			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	–4.1	±1.2	4.1	–2.75	±1	2.75	–2.75	±1	2.75	LSB
Differential Linearity Error	Differential Analog Input	●	–0.9	±0.3	0.9	–0.8	±0.3	0.8	–0.8	±0.3	0.8	LSB
Offset Error	(Note 7)	●	–12	±3	12	–12	±3	12	–12	±3	12	mV
Gain Error	Internal Reference External Reference	 ●	 –2.5	–1.3 –1.3	 0.5	 –2.5	–1.3 –1.3	 0.5	 –2.6	–1.3 –1.3	 0.5	%FS %FS
Offset Drift				±20			±20			±20		µV/°C
Full-Scale Drift	Internal Reference External Reference			±35 ±25			±35 ±25			±35 ±25		ppm/°C ppm/°C
Gain Matching	External Reference			±0.2			±0.2			±0.2		%FS
Offset Matching				±3			±3			±3		mV
Transition Noise	External Reference			1.2			1.2			1.2		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	1.7V < V_{DD} < 1.9V	●		1 to 2		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Analog Input (Note 8)	●	V_{CM} – 100mV	V_{CM}	V_{CM} + 100mV	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
I_{INCM}	Analog Input Common Mode Current	Per Pin, 65Msps Per Pin, 40Msps Per Pin, 25Msps			81 50 31		µA µA µA
I_{IN1}	Analog Input Leakage Current	0 < A_{IN}^+, A_{IN}^- < V_{DD}, No Encode	●	–1		1	µA
I_{IN2}	PAR/$\overline{SER}$ Input Leakage Current	0 < PAR/$\overline{SER}$ < V_{DD}	●	–3		3	µA
I_{IN3}	SENSE Input Leakage Current	0.625 < SENSE < 1.3V	●	–6		6	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter				0.15		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
BW-3B	Full-Power Bandwidth	Figure 6 Test Circuit			800		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTM9008-14 MIN	LTM9008-14 TYP	LTM9008-14 MAX	LTM9007-14 MIN	LTM9007-14 TYP	LTM9007-14 MAX	LTM9006-14 MIN	LTM9006-14 TYP	LTM9006-14 MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input			73.7			73.5			72.9		dBFS
		30MHz Input	●	71.8	73.7		69.6	73.4		69.6	72.9		dBFS
		70MHz Input			73.5			73.4			72.8		dBFS
		140MHz Input			73			72.8			72.3		dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input			90			90			90		dBFS
		30MHz Input	●	74	90		76.8	90		76.8	90		dBFS
		70MHz Input			89			89			89		dBFS
		140MHz Input			84			84			84		dBFS
	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input			90			90			90		dBFS
		30MHz Input	●	84	90		84	90		84	90		dBFS
		70MHz Input			90			90			90		dBFS
		140MHz Input			90			90			90		dBFS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input			73.6			73.3			72.8		dBFS
		30MHz Input	●	71	73.5		69.5	73.2		69.5	72.7		dBFS
		70MHz Input			73.2			73.1			72.5		dBFS
		140MHz Input			72.5			72.3			71.9		dBFS
	Crosstalk, Near Channel	10MHz Input (Note 12)			–90			–90			–90		dBc
	Crosstalk, Far Channel	10MHz Input (Note 12)			–105			–105			–105		dBc

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	0.5 • V_{DD} – 25mV	0.5 • V_{DD}	0.5 • V_{DD} + 25mV	V
V_{CM} Output Temperature Drift			±25		ppm/°C
V_{CM} Output Resistance	–600µA < I_{OUT} < 1mA		4		Ω
V_{REF} Output Voltage	I_{OUT} = 0	1.225	1.250	1.275	V
V_{REF} Output Temperature Drift			±25		ppm/°C
V_{REF} Output Resistance	–400µA < I_{OUT} < 1mA		7		Ω
V_{REF} Line Regulation	1.7V < V_{DD} < 1.9V		0.6		mV/V

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC⁺, ENC⁻)							
Differential Encode Mode (ENC⁻ Not Tied to GND)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	 ●	 1.1	1.2	 1.6	V V
V_{IN}	Input Voltage Range	ENC⁺, ENC⁻ to GND	●	0.2		3.6	V
R_{IN}	Input Resistance	(See Figure 10)			10		kΩ
C_{IN}	Input Capacitance				3.5		pF
Single-Ended Encode Mode (ENC⁻ Tied to GND)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V			1.26		V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V			0.54		V
V_{IN}	Input Voltage Range	ENC⁺ to GND			0 to 3.6		V
R_{IN}	Input Resistance	(See Figure 11)			30		kΩ
C_{IN}	Input Capacitance				3.5		pF
DIGITAL INPUTS ($\overline{CS}$, SDI, SCK in Serial or Parallel Programming Mode. SDO in Parallel Programming Mode)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
C_{IN}	Input Capacitance				3		pF
SDO OUTPUT (Serial Programming Mode. Open-Drain Output. Requires 2kΩ Pull-Up Resistor if SDO Is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
C_{OUT}	Output Capacitance				3		pF
DIGITAL DATA OUTPUTS							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	247 125	350 175	454 250	mV mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	1.125 1.125	1.250 1.250	1.375 1.375	V V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		LTM9008-14 MIN	LTM9008-14 TYP	LTM9008-14 MAX	LTM9007-14 MIN	LTM9007-14 TYP	LTM9007-14 MAX	LTM9006-14 MIN	LTM9006-14 TYP	LTM9006-14 MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{VDD}	Analog Supply Current	Sine Wave Input	●		357	400		232	275		175	250	mA
I_{OVDD}	Digital Supply Current	1-Lane Mode, 1.75mA Mode			32			32			30		mA
		1-Lane Mode, 3.5mA Mode			60			58			56		mA
		2-Lane Mode, 1.75mA Mode	●		50	58		48	54		48	54	mA
		2-Lane Mode, 3.5mA Mode	●		94	104		92	102		90	100	mA
P_{DISS}	Power Dissipation	1-Lane Mode, 1.75mA Mode			700			475			369		mW
		1-Lane Mode, 3.5mA Mode			751			522			416		mW
		2-Lane Mode, 1.75mA Mode	●		733	824		504	592		401	547	mW
		2-Lane Mode, 3.5mA Mode	●		812	907		583	679		477	630	mW
P_{SLEEP}	Sleep Mode Power				2			2			2		mW
P_{NAP}	Nap Mode Power				170			170			170		mW
$P_{DIFFCLK}$	Power Decrease With Single-Ended Encode Mode Enabled (No Decrease for Sleep Mode)				40			40			40		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTM9008-14 MIN	LTM9008-14 TYP	LTM9008-14 MAX	LTM9007-14 MIN	LTM9007-14 TYP	LTM9007-14 MAX	LTM9006-14 MIN	LTM9006-14 TYP	LTM9006-14 MAX	UNITS
f_S	Sampling Frequency	(Notes 10,11)	●	5		65	5		40	5		25	MHz
t_{ENCL}	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off	●	7.3	7.69	100	11.88	12.5	100	19	20	100	ns
		Duty Cycle Stabilizer On	●	2	7.69	100	2	12.5	100	2	20	100	ns
t_{ENCH}	ENC High Time (Note 8)	Duty Cycle Stabilizer Off	●	7.3	7.69	100	11.88	12.5	100	19	20	100	ns
		Duty Cycle Stabilizer On	●	2	7.69	100	2	12.5	100	2	20	100	ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				0			0			0		ns

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Data Outputs (R_{TERM} = 100Ω Differential, C_L = 2pF to GND on Each Output)							
t_{SER}	Serial Data Bit Period	2-Lanes, 16-Bit Serialization			$1/(8 \cdot f_S)$		s
		2-Lanes, 14-Bit Serialization			$1/(7 \cdot f_S)$		s
		2-Lanes, 12-Bit Serialization			$1/(6 \cdot f_S)$		s
		1-Lane, 16-Bit Serialization			$1/(16 \cdot f_S)$		s
		1-Lane, 14-Bit Serialization			$1/(14 \cdot f_S)$		s
		1-Lane, 12-Bit Serialization			$1/(12 \cdot f_S)$		s
t_{FRAME}	FR to DCO Delay	(Note 8)	●	$0.35 \cdot t_{SER}$	$0.5 \cdot t_{SER}$	$0.65 \cdot t_{SER}$	s
t_{DATA}	DATA to DCO Delay	(Note 8)	●	$0.35 \cdot t_{SER}$	$0.5 \cdot t_{SER}$	$0.65 \cdot t_{SER}$	s
t_{PD}	Propagation Delay	(Note 8)	●	$0.7n + 2 \cdot t_{SER}$	$1.1n + 2 \cdot t_{SER}$	$1.5n + 2 \cdot t_{SER}$	s
t_R	Output Rise Time	Data, DCO, FR, 20% to 80%			0.17		ns
t_F	Output Fall Time	Data, DCO, FR, 20% to 80%			0.17		ns
	DCO Cycle-Cycle Jitter	t_{SER} = 1ns			60		ps_{P-P}
	Pipeline Latency				6		Cycles

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Port Timing (Note 8)							
t_{SCK}	SCK Period	Write Mode Read Back Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Setup Time		●	5			ns
t_H	SCK to $\overline{CS}$ Setup Time		●	5			ns
t_{DS}	SDI Setup Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Read Back Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●			125	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 65MHz (LTM9008), 40MHz (LTM9007), or 25MHz (LTM9006), 2-lane output mode, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111 in 2's complement output mode.

Note 8: Guaranteed by design, not subject to test.

Note 9: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 65MHz (LTM9008), 40MHz (LTM9007), or 25MHz (LTM9006), 2-lane output mode, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted. The supply current and power dissipation specifications are totals for the entire device, not per channel.

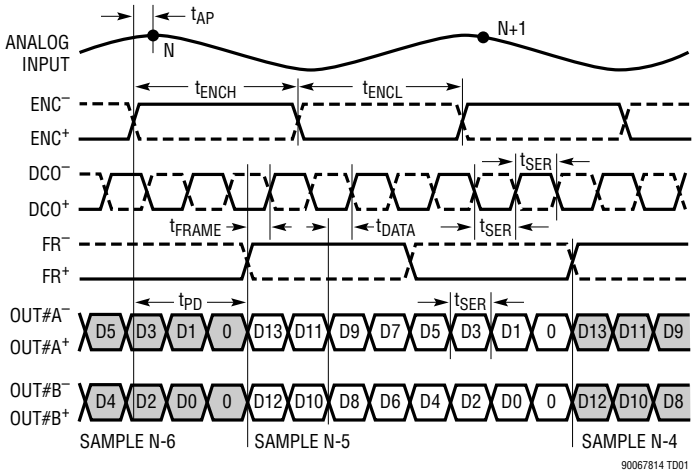
Note 10: Recommended operating conditions.

Note 11: The maximum sampling frequency depends on the speed grade of the part and also which serialization mode is used. The maximum serial data rate is 1000Mbps so t_{SER} must be greater than or equal to 1ns.

Note 12: Near-channel crosstalk refers to Ch. 1 to Ch.2, and Ch.7 to Ch.8. Far-channel crosstalk refers to Ch.1 to Ch.7, Ch.1 to Ch.8, Ch.2 to Ch.7, and Ch.2 to Ch.8.

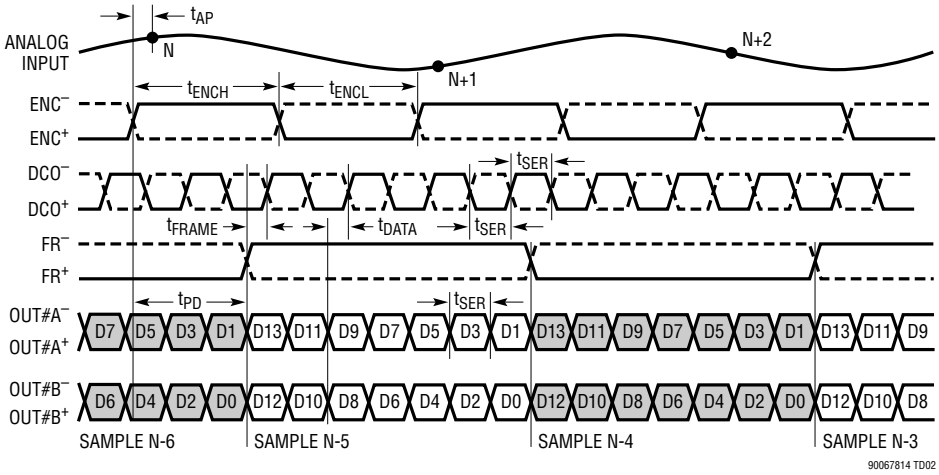
TIMING DIAGRAMS

2-Lane Output Mode, 16-Bit Serialization*



*SEE THE DIGITAL OUTPUTS SECTION

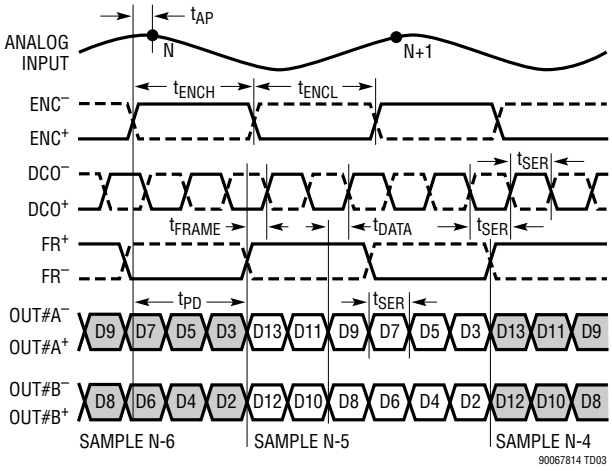
2-Lane Output Mode, 14-Bit Serialization



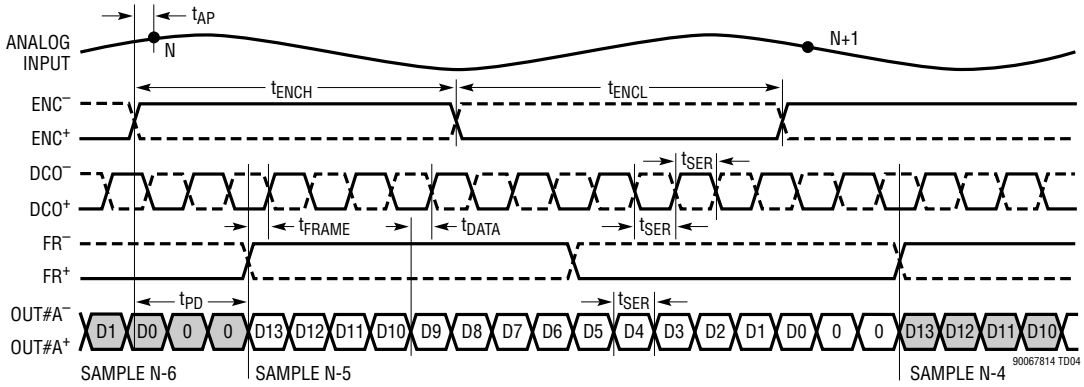
NOTE THAT IN THIS MODE FR+/FR– HAS TWO TIMES THE PERIOD OF ENC+/ENC–

TIMING DIAGRAMS

2-Lane Output Mode, 12-Bit Serialization

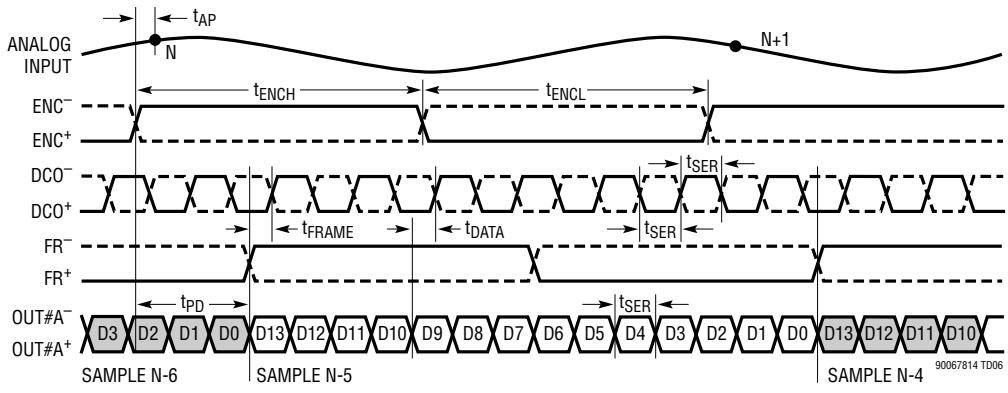


1-Lane Output Mode, 16-Bit Serialization



OUT#B+, OUT#B– ARE DISABLED

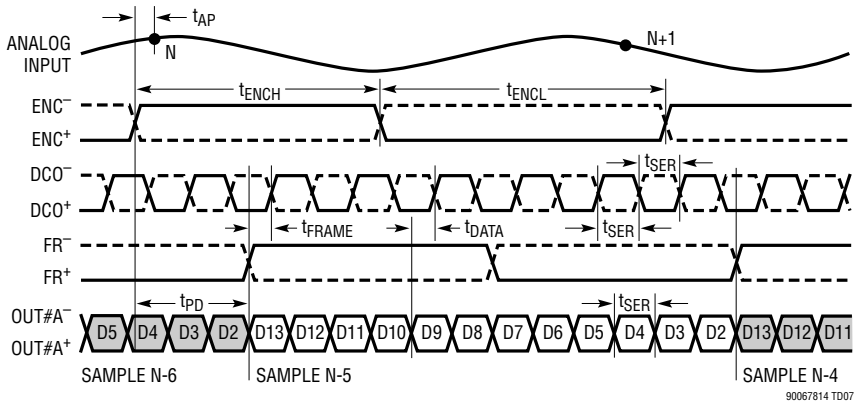
1-Lane Output Mode, 14-Bit Serialization



OUT#B+, OUT#B– ARE DISABLED

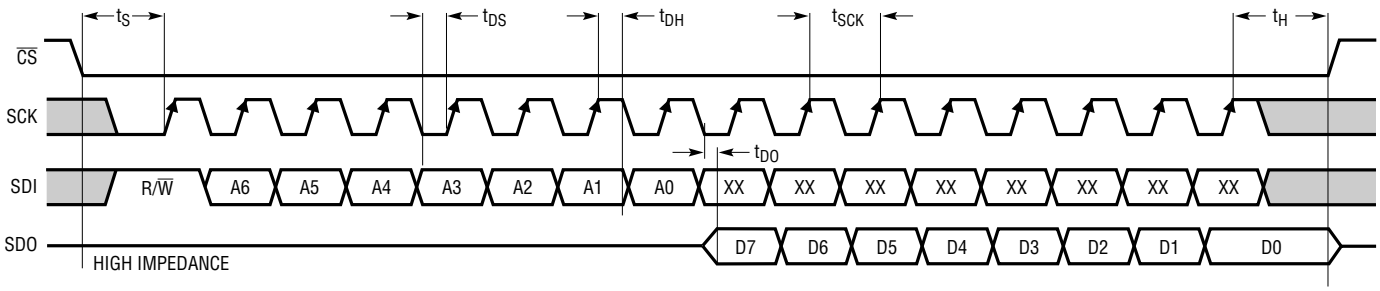
TIMING DIAGRAMS

1-Lane Output Mode, 12-Bit Serialization

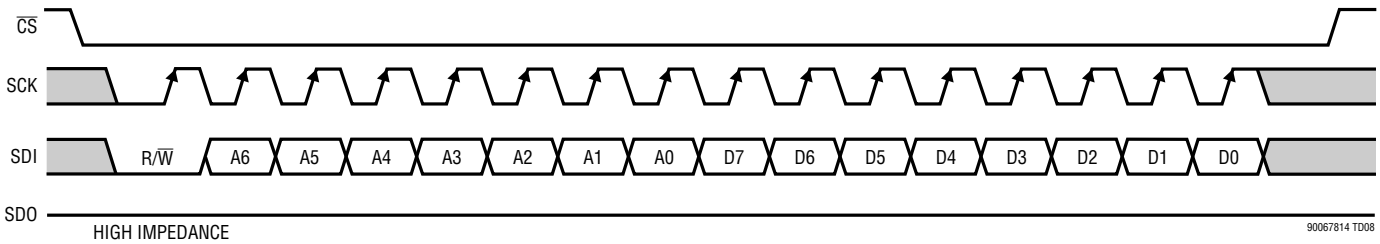


OUT#B+, OUT#B– ARE DISABLED

SPI Port Timing (Readback Mode)

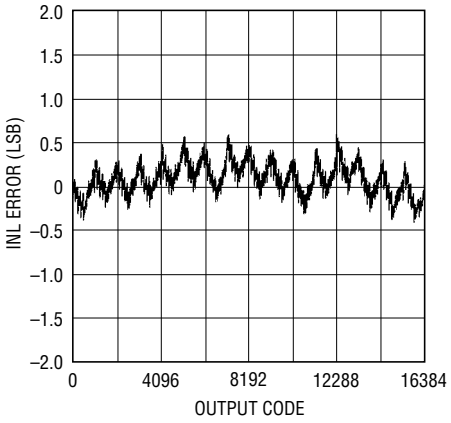


SPI Port Timing (Write Mode)

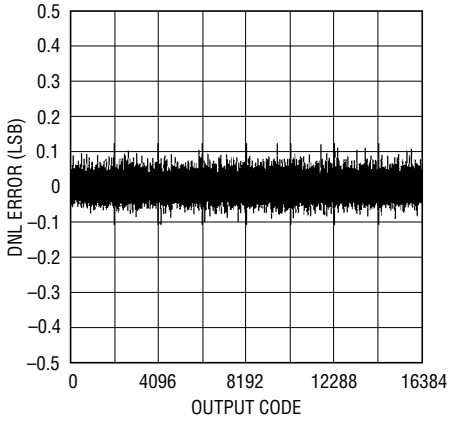


TYPICAL PERFORMANCE CHARACTERISTICS

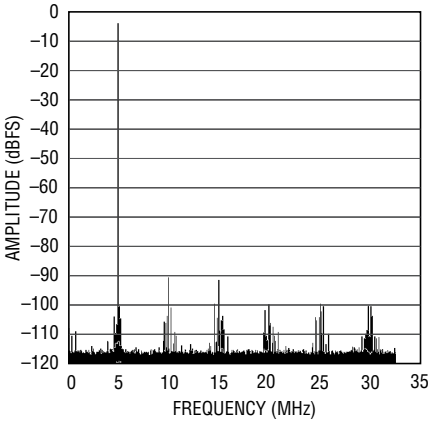
LTM9008-14: Integral Nonlinearity (INL) vs Output Code



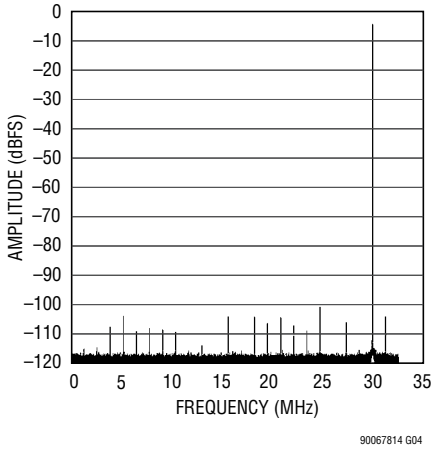
LTM9008-14: Differential Nonlinearity (DNL) vs Output Code



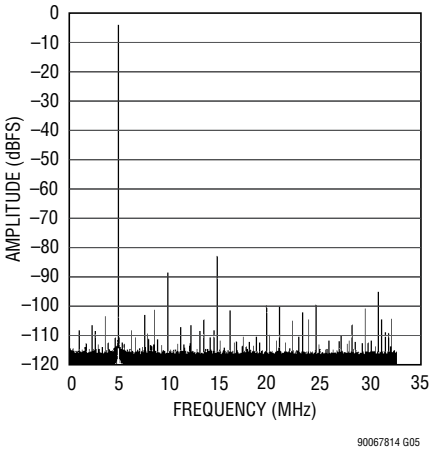
LTM9008-14: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, SENSE = V_{DD}



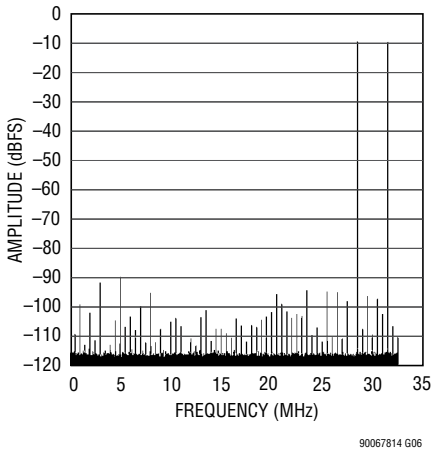
LTM9008-14: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, SENSE = V_{DD}



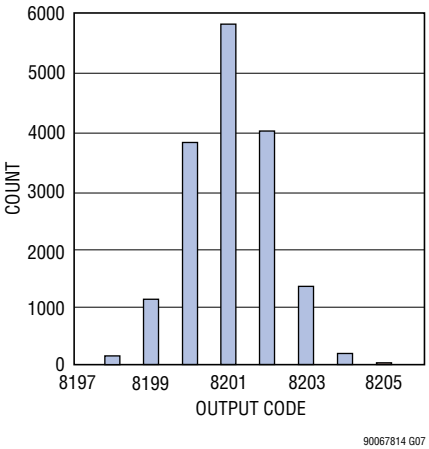
LTM9008-14: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, SENSE = V_{DD}



LTM9008-14: 64k Point 2-Tone FFT, f_{IN} = 28.5MHz and f_{IN} = 31.5MHz, –7dBFS per Tone, SENSE = V_{DD}

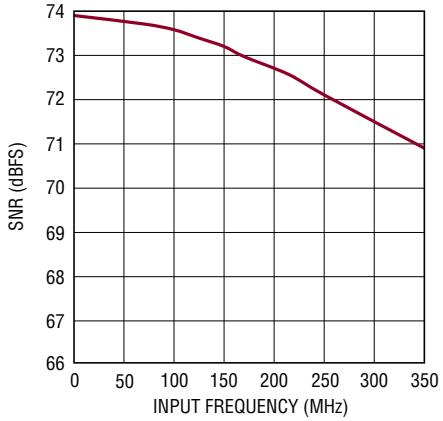


LTM9008-14: Shorted Input Histogram

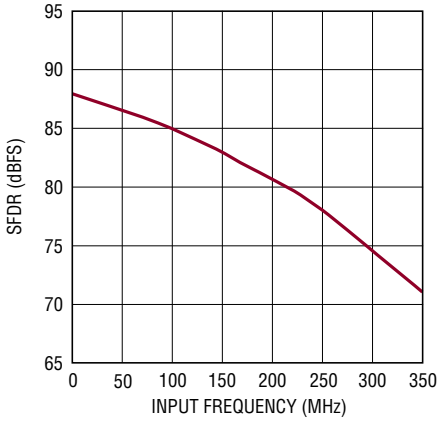


TYPICAL PERFORMANCE CHARACTERISTICS

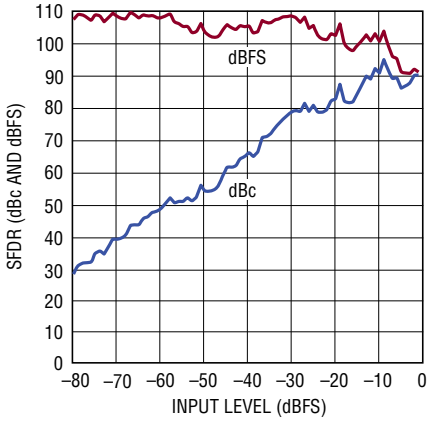
LTM9008-14: SNR vs Input Frequency, –1dBFS, 2V Range, 65Msps



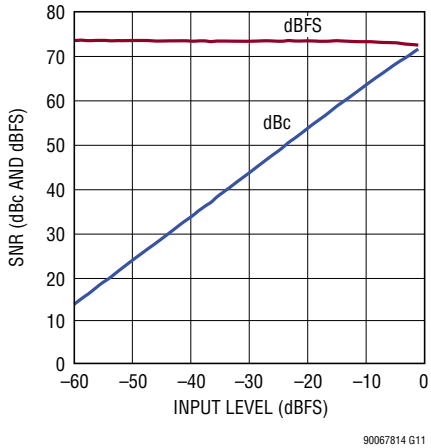
LTM9008-14: SFDR vs Input Frequency, –1dBFS, 2V Range, 65Msps



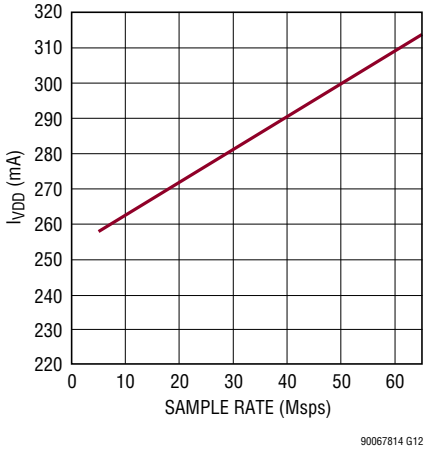
LTM9008-14: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 65Msps



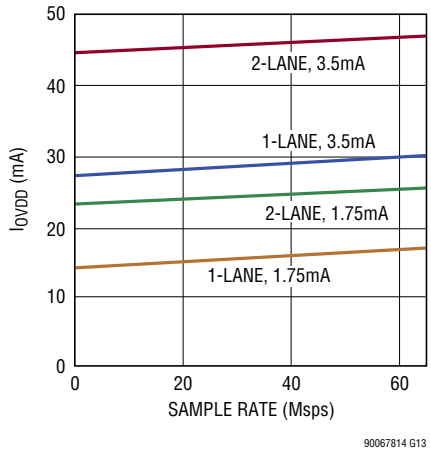
LTM9008-14: SNR vs Input Level, f_{IN} = 70MHz, 2V Range, 65Msps



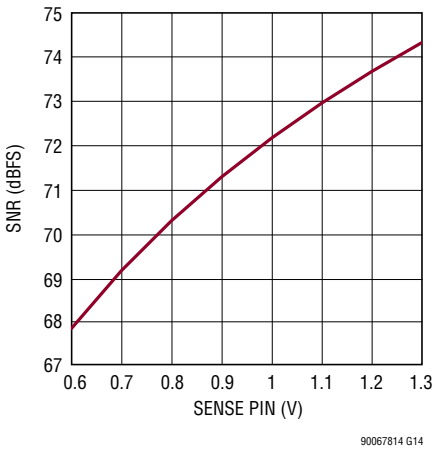
LTM9008-14: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dBFS



I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, –1dBFS

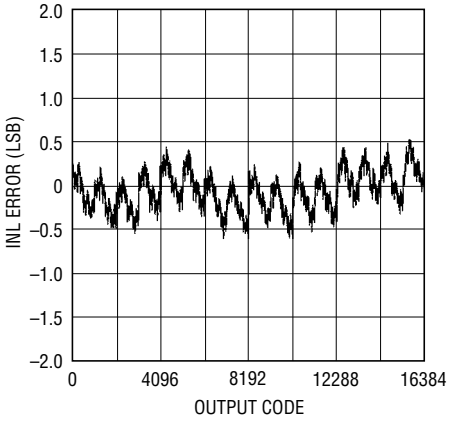


LTM9008-14: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS

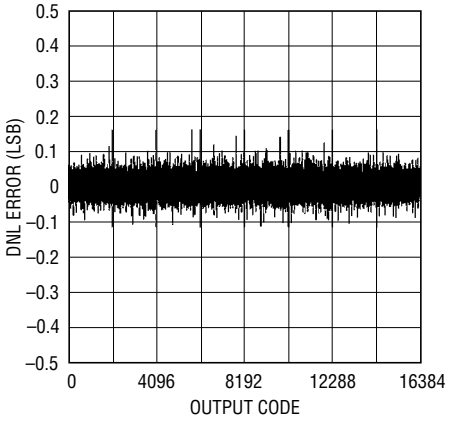


TYPICAL PERFORMANCE CHARACTERISTICS

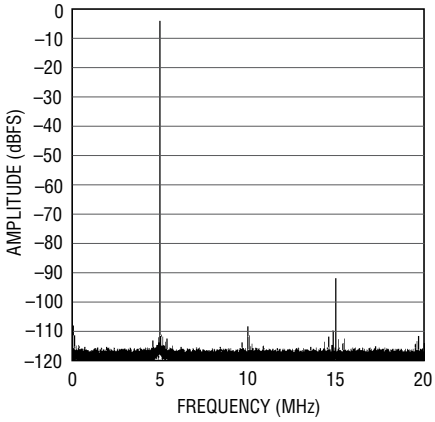
LTM9007-14: Integral Nonlinearity (INL) vs Output Code



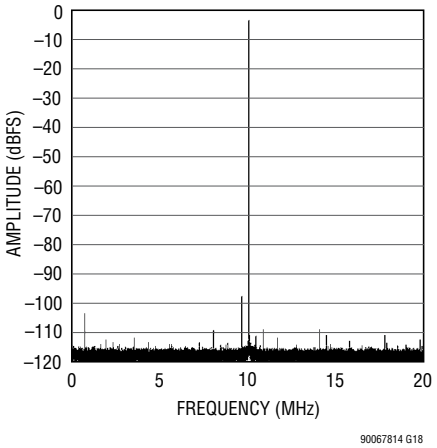
LTM9007-14: Differential Nonlinearity (DNL) vs Output Code



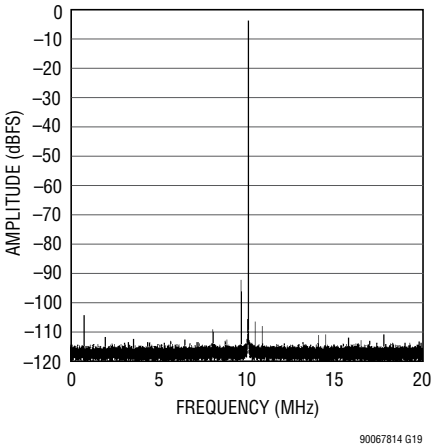
LTM9007-14: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, SENSE = V_{DD}



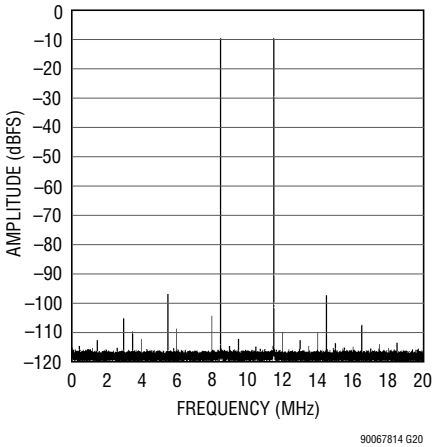
LTM9007-14: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, SENSE = V_{DD}



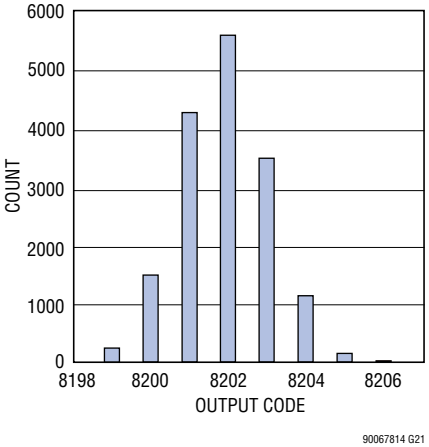
LTM9007-14: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, SENSE = V_{DD}



LTM9007-14: 64k Point 2-Tone FFT, f_{IN} = 28.5MHz and f_{IN} = 31.5MHz, –7dBFS per Tone, SENSE = V_{DD}

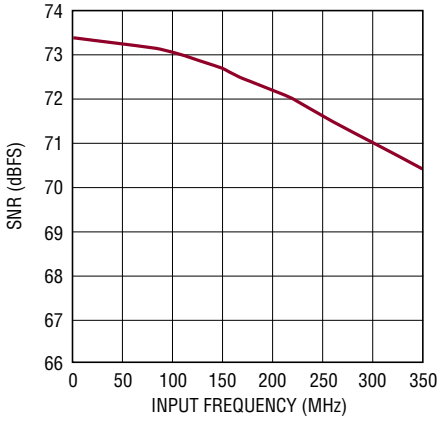


LTM9007-14: Shorted Input Histogram

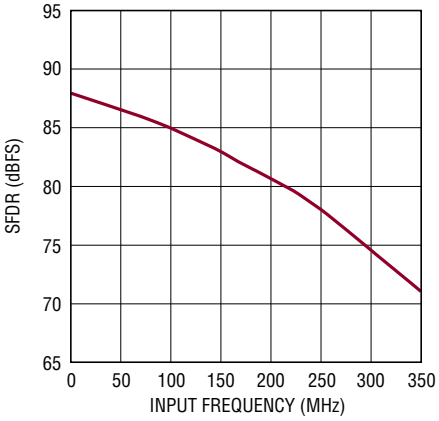


TYPICAL PERFORMANCE CHARACTERISTICS

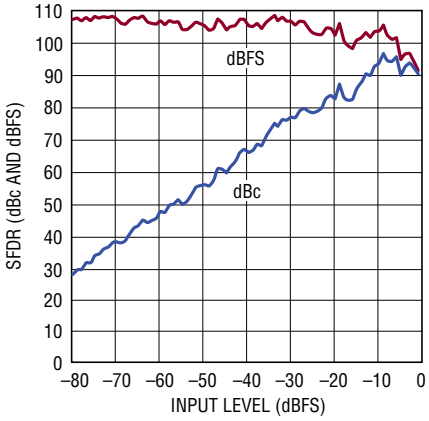
LTM9007-14: SNR vs Input Frequency, –1dBFS, 2V Range, 40Msps



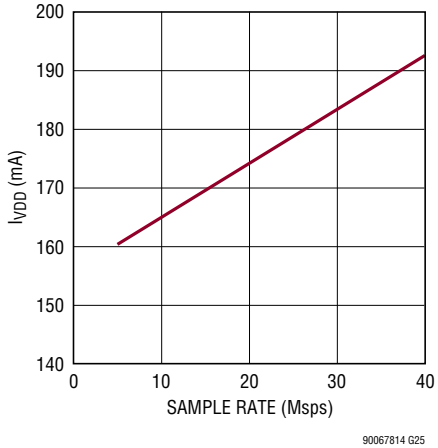
LTM9007-14: SFDR vs Input Frequency, –1dBFS, 2V Range, 40Msps



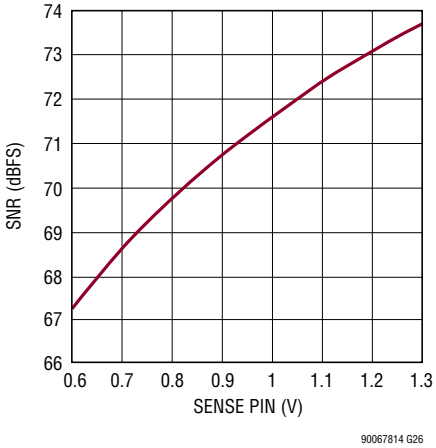
LTM9007-14: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 40Msps



LTM9007-14: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dBFS

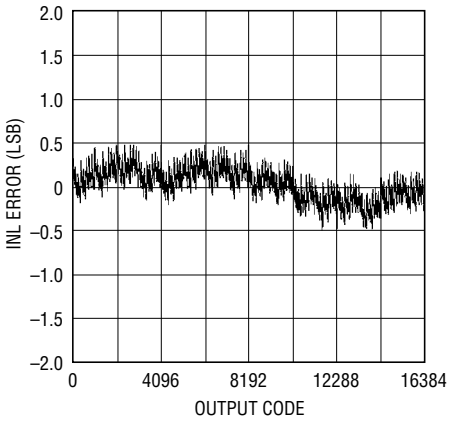


LTM9007-14: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS

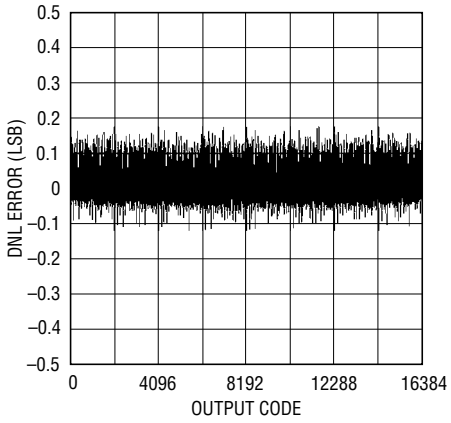


TYPICAL PERFORMANCE CHARACTERISTICS

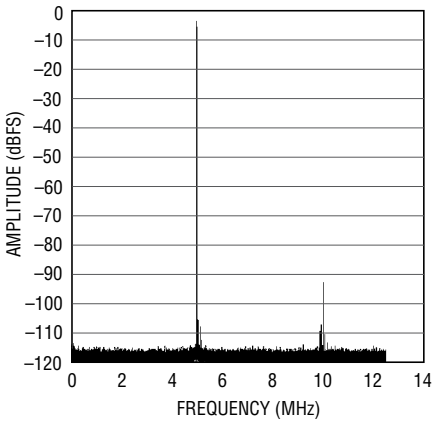
LTM9006-14: Integral Nonlinearity (INL) vs Output Code



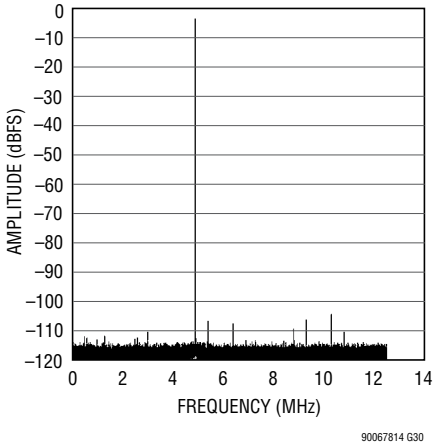
LTM9006-14: Differential Nonlinearity (DNL) vs Output Code



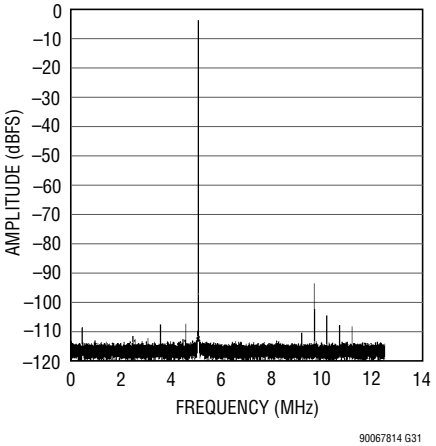
LTM9006-14: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, SENSE = V_{DD}



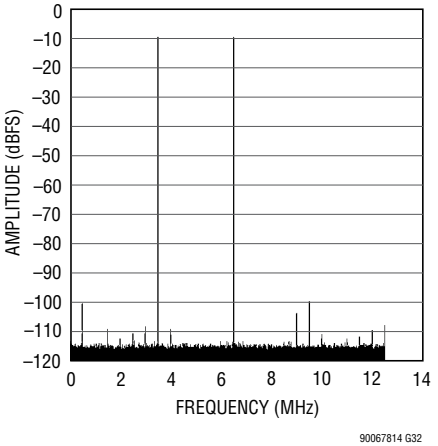
LTM9006-14: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, SENSE = V_{DD}



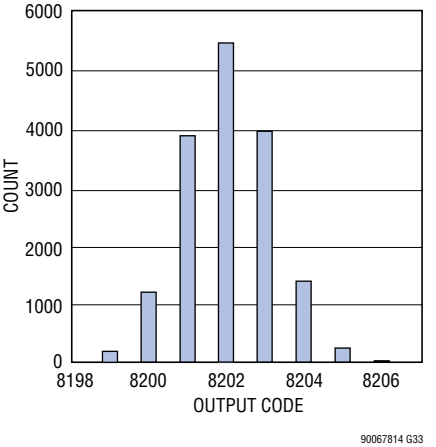
LTM9006-14: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, SENSE = V_{DD}



LTM9006-14: 64k Point 2-Tone FFT, f_{IN} = 28.5MHz and 31.5MHz, –7dBFS per Tone, SENSE = V_{DD}

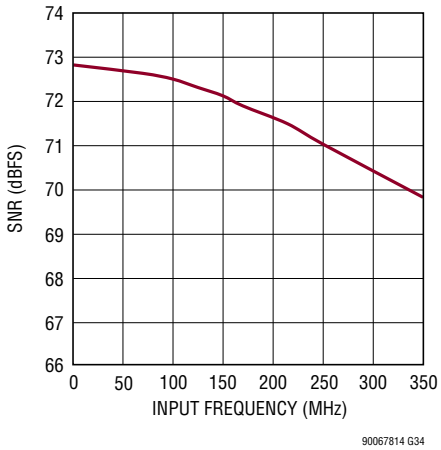


LTM9006-14: Shorted Input Histogram

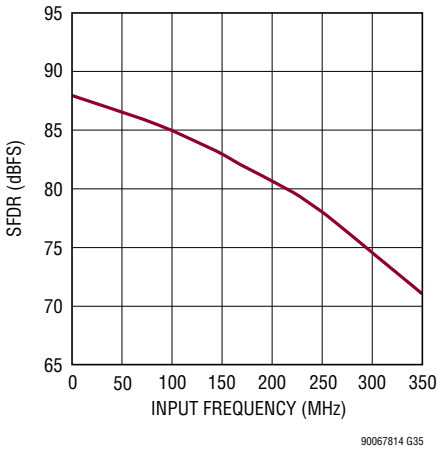


TYPICAL PERFORMANCE CHARACTERISTICS

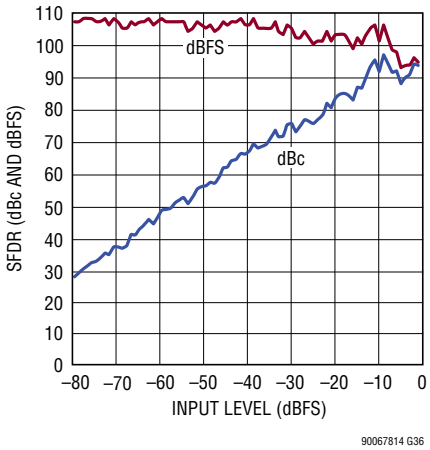
LTM9006-14: SNR vs Input Frequency, –1dBFS, 2V Range, 25Msps



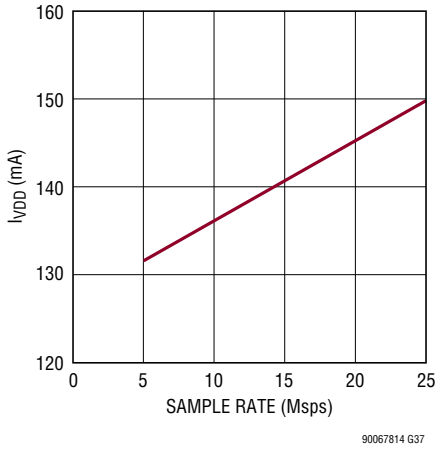
LTM9006-14: SFDR vs Input Frequency, –1dBFS, 2V Range, 25Msps



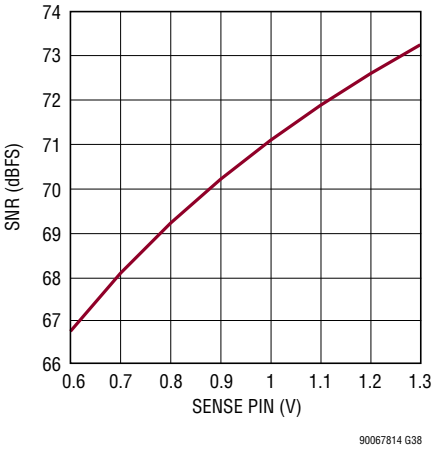
LTM9006-14: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 25Msps



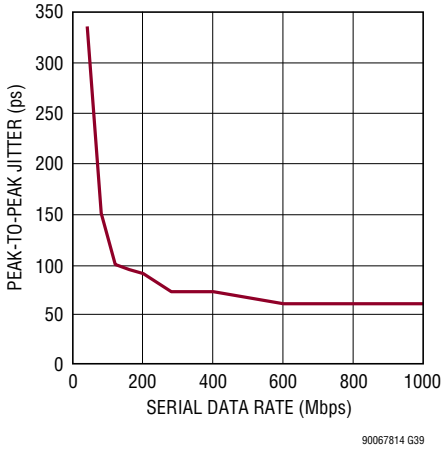
LTM9006-14: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dBFS



LTM9006-14: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



DCO Cycle-Cycle Jitter vs Serial Data Rate



PIN FUNCTIONS

A_{IN1}^+ (B2): Channel 1 Positive Differential Analog Input.

A_{IN1}^- (B1): Channel 1 Negative Differential Analog Input.

V_{CM14} (B3): Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 1 and 4. V_{CM} is internally bypassed to ground with a 0.1µF ceramic capacitor. No external capacitance is required.

A_{IN2}^+ (C2): Channel 2 Positive Differential Analog Input.

A_{IN2}^- (C1): Channel 2 Negative Differential Analog Input.

A_{IN3}^+ (E2): Channel 3 Positive Differential Analog Input.

A_{IN3}^- (E1): Channel 3 Negative Differential Analog Input.

V_{CM23} (F3): Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 2 and 3. V_{CM} is internally bypassed to ground with a 0.1µF ceramic capacitor. No external capacitance is required.

A_{IN4}^+ (G2): Channel 4 Positive Differential Analog Input.

A_{IN4}^- (G1): Channel 4 Negative Differential Analog Input.

A_{IN5}^+ (H1): Channel 5 Positive Differential Analog Input.

A_{IN5}^- (H2): Channel 5 Negative Differential Analog Input.

V_{CM67} (J3): Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 6 and 7. V_{CM} is internally bypassed to ground with a 0.1µF ceramic capacitor. No external capacitance is required.

A_{IN6}^+ (K1): Channel 6 Positive Differential Analog Input.

A_{IN6}^- (K2): Channel 6 Negative Differential Analog Input.

A_{IN7}^+ (M1): Channel 7 Positive Differential Analog Input.

A_{IN7}^- (M2): Channel 7 Negative Differential Analog Input.

V_{CM58} (N3): Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 5 and 8. V_{CM} is internally bypassed to ground with a 0.1µF ceramic capacitor. No external capacitance is required.

A_{IN8}^+ (N1): Channel 8 Positive Differential Analog Input.

A_{IN8}^- (N2): Channel 8 Negative Differential Analog Input

V_{DD} (D3, D4, E3, E4, K3, K4, L3, L4): 1.8V Analog Power Supply. V_{DD} is internally bypassed to ground with 0.1µF ceramic capacitors.

ENC+ (P5): Encode Input. Conversion starts on the rising edge.

ENC– (P6): Encode Complement Input. Conversion starts on the falling edge.

$\overline{CS}$A (L5): In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CS}$A is the serial interface chip select input for registers controlling channels 1, 4, 5 and 8. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ selects 2-lane or 1-lane output mode. $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

$\overline{CS}$B (M5): In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CS}$B is the serial interface chip select input for registers controlling channels 2, 3, 6 and 7. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ selects 2-lane or 1-lane output mode. $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

SCK (L6): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SCK is the serial interface clock input. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK selects 3.5mA or 1.75mA LVDS output currents. SCK can be driven with 1.8V to 3.3V logic.

SDI (M6): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDI is the serial interface data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDI can be used to power down the part. SDI can be driven with 1.8V to 3.3V logic.

GND (See Pin Configuration Table): ADC Power Ground. Use multiple vias close to pins.

PIN FUNCTIONS

OV_{DD} (G9, G10): Output Driver Supply. OV_{DD} is internally bypassed to ground with a 0.1µF ceramic capacitor.

SDOA (E6): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDOA is the optional serial interface data output for registers controlling channels 1, 4, 5 and 8. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain N-channel MOSFET output that requires an external 2k pull-up resistor from 1.8V to 3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDOA is an input that enables internal 100Ω termination resistors on the digital outputs of channels 1, 4, 5 and 8. When used as an input, SDO can be driven with 1.8V to 3.3V logic through a 1k series resistor.

SDOB (D6): Serial Data Output Pin for Channels 2, 3, 6 and 7. See description for SDOA.

PAR/$\overline{SER}$ (A7): Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. $\overline{CS}$A, $\overline{CS}$B, SCK, SDI, SDOA and SDOB become a serial interface that control the A/D operating modes. Connect to V_{DD} to enable parallel programming mode where $\overline{CS}$A, $\overline{CS}$B, SCK, SDI, SDOA and SDOB become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{SER}$ should be connected directly to ground or the V_{DD} of the part and not be driven by a logic signal.

V_{REF} (B6): Reference Voltage Output. V_{REF} is internally bypassed to ground with a 1µF ceramic capacitor, nominally 1.25V.

SENSE (C5): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±1V input range. Connecting SENSE to ground selects the internal reference and a ±0.5V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of ±0.8 • V_{SENSE}. SENSE is internally bypassed to ground with a 0.1µF ceramic capacitor.

LVDS Outputs

All pins in this section are differential LVDS outputs. The output current level is programmable. There is an optional internal 100Ω termination resistor between the pins of each LVDS output pair.

$OUT1A^-$/$OUT1A^+$, $OUT1B^-$/$OUT1B^+$ (E7/E8, C8/D8): Serial Data Outputs for Channel 1. In 1-lane output mode only $OUT1A^-$/$OUT1A^+$ are used.

$OUT2A^-$/$OUT2A^+$, $OUT2B^-$/$OUT2B^+$ (B8/A8, D7/C7): Serial Data Outputs for Channel 2. In 1-lane output mode only $OUT2A^-$/$OUT2A^+$ are used.

$OUT3A^-$/$OUT3A^+$, $OUT3B^-$/$OUT3B^+$ (D10/D9, E10/E9): Serial Data Outputs for Channel 3. In 1-lane output mode only $OUT3A^-$/$OUT3A^+$ are used.

$OUT4A^-$/$OUT4A^+$, $OUT4B^-$/$OUT4B^+$ (C9/C10, F7/F8): Serial Data Outputs for Channel 4. In 1-lane output mode only $OUT4A^-$/$OUT4A^+$ are used.

$OUT5A^-$/$OUT5A^+$, $OUT5B^-$/$OUT5B^+$ (J8/J7, K8/K7): Serial Data Outputs for Channel 5. In 1-lane output mode only $OUT5A^-$/$OUT5A^+$ are used.

$OUT6A^-$/$OUT6A^+$, $OUT6B^-$/$OUT6B^+$ (K9/K10, L9/L10): Serial Data Outputs for Channel 6. In 1-lane output mode only $OUT6A^-$/$OUT6A^+$ are used.

$OUT7A^-$/$OUT7A^+$, $OUT7B^-$/$OUT7B^+$ (M7/L7, P8/N8): Serial Data Outputs for Channel 7. In 1-lane output mode only $OUT7A^-$/$OUT7A^+$ are used.

$OUT8A^-$/$OUT8A^+$, $OUT8B^-$/$OUT8B^+$ (L8/M8, M10/M9): Serial Data Outputs for Channel 8. In 1-lane output mode only $OUT8A^-$/$OUT8A^+$ are used.

FRA^-/FRA^+ (H7/H8): Frame Start Outputs for Channels 1, 4, 5 and 8.

FRB^-/FRB^+ (J9/J10): Frame Start Outputs for Channels 2, 3, 6 and 7.

$DCOA^-$/$DCOA^+$ (G8/G7): Data Clock Outputs for Channels 1, 4, 5 and 8.

$DCOB^-$/$DCOB^+$ (F10, F9): Data Clock Outputs for Channels 2, 3, 6 and 7.

PIN CONFIGURATION TABLE

	1	2	3	4	5	6	7	8	9	10
A	GND	GND	GND	GND	GND	GND	PAR/$\overline{SER}$	$OUT2A^+$	GND	GND
B	A_{IN1}^-	A_{IN1}^+	V_{CM14}	GND	GND	V_{REF}	GND	$OUT2A^-$	GND	GND
C	A_{IN2}^-	A_{IN2}^+	GND	GND	SENSE	GND	$OUT2B^+$	$OUT1B^-$	$OUT4A^-$	$OUT4A^+$
D	GND	GND	V_{DD}	V_{DD}	GND	SDOB	$OUT2B^-$	$OUT1B^+$	$OUT3A^+$	$OUT3A^-$
E	A_{IN3}^-	A_{IN3}^+	V_{DD}	V_{DD}	GND	SDOA	$OUT1A^-$	$OUT1A^+$	$OUT3B^+$	$OUT3B^-$
F	GND	GND	V_{CM23}	GND	GND	GND	$OUT4B^-$	$OUT4B^+$	$DCOB^+$	$DCOB^-$
G	A_{IN4}^-	A_{IN4}^+	GND	GND	GND	GND	$DCOA^+$	$DCOA^-$	OV_{DD}	OV_{DD}
H	A_{IN5}^+	A_{IN5}^-	GND	GND	GND	GND	FRA^-	FRA^+	GND	GND
J	GND	GND	V_{CM67}	GND	GND	GND	$OUT5A^+$	$OUT5A^-$	FRB^-	FRB^+
K	A_{IN6}^+	A_{IN6}^-	V_{DD}	V_{DD}	GND	GND	$OUT5B^+$	$OUT5B^-$	$OUT6A^-$	$OUT6A^+$
L	GND	GND	V_{DD}	V_{DD}	$\overline{CS}A$	SCK	$OUT7A^+$	$OUT8A^-$	$OUT6B^-$	$OUT6B^+$
M	A_{IN7}^+	A_{IN7}^-	GND	GND	$\overline{CS}B$	SDI	$OUT7A^-$	$OUT8A^+$	$OUT8B^+$	$OUT8B^-$
N	A_{IN8}^+	A_{IN8}^-	V_{CM58}	GND	GND	GND	GND	$OUT7B^+$	GND	GND
P	GND	GND	GND	GND	ENC^+	ENC^-	GND	$OUT7B^-$	GND	GND

Top View of BGA Package (Looking Through Component).

FUNCTIONAL BLOCK DIAGRAM

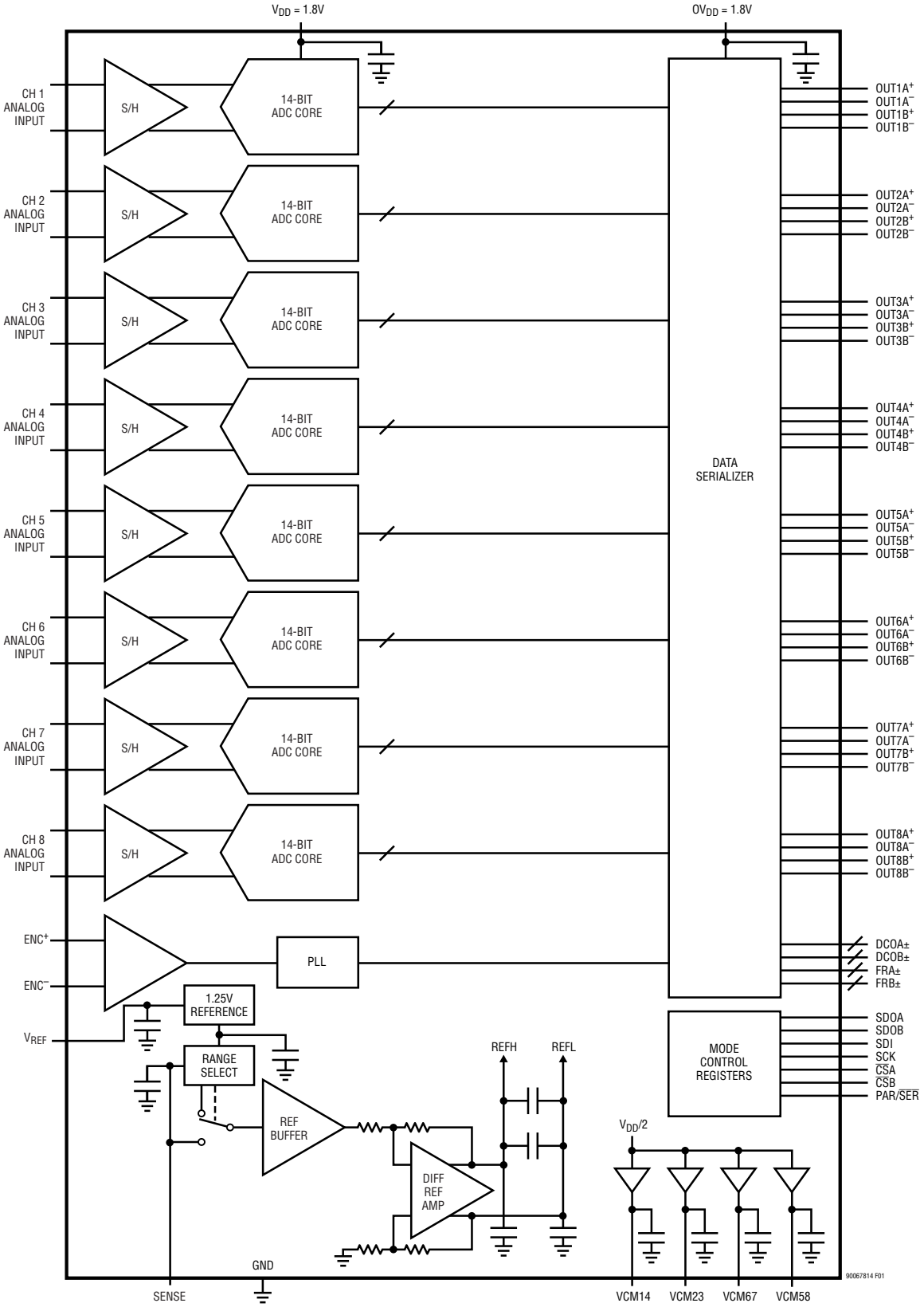


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTM9008-14/LTM9007-14/LTM9006-14 are low power, 8-channel, 14-bit, 65Msps/40Msps/25Msps A/D converters that are powered by a single 1.8V supply. The analog inputs should be driven differentially. The encode input can be driven differentially for optimal jitter performance, or single-ended for lower power consumption. The digital outputs are serial LVDS to minimize the number of data lines. Each channel outputs two bits at a time (2-lane mode) or one bit at a time (1-lane mode). Many additional features can be chosen by programming the mode control registers through a serial SPI port.

ANALOG INPUT

The analog inputs are differential CMOS sample-and-hold circuits (Figure 2). The inputs should be driven differentially around a common mode voltage set by the appropriate V_{CM} output pins, which are nominally $V_{DD}/2$. For the 2V input range, the inputs should swing from V_{CM} – 0.5V to V_{CM} + 0.5V. There should be 180° phase difference between the inputs.

The eight channels are simultaneously sampled by a shared encode circuit (Figure 2).

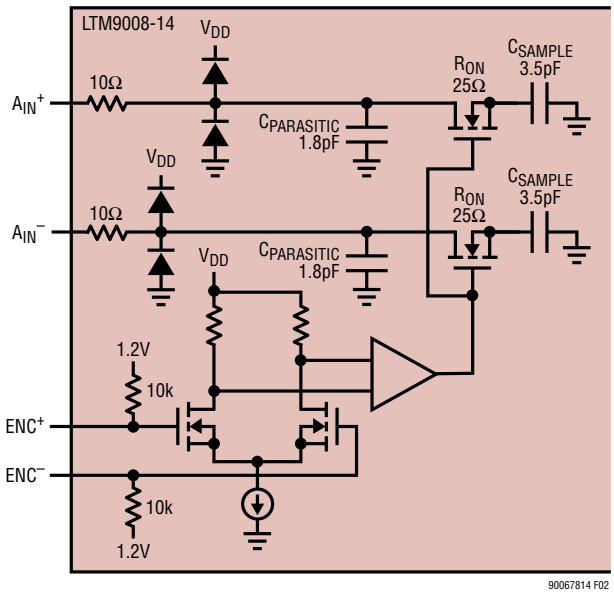


Figure 2. Equivalent Input Circuit. Only One of the Eight Analog Channels Is Shown

INPUT DRIVE CIRCUITS

Input Filtering

If possible, there should be an RC low pass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wideband noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's input frequency.

Transformer Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with a center-tapped secondary. The center tap is biased with V_{CM}, setting the A/D input at its optimal DC level. At higher input frequencies a transmission line balun transformer (Figures 4 to 6) has better balance, resulting in lower A/D distortion.

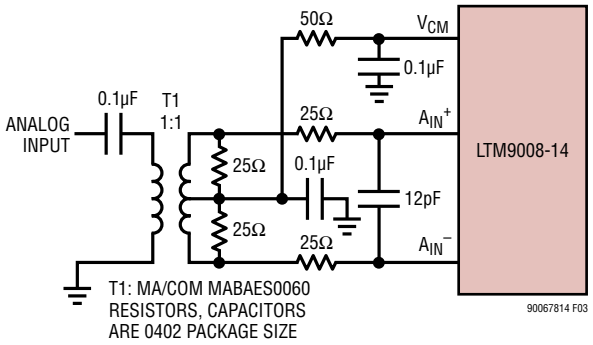


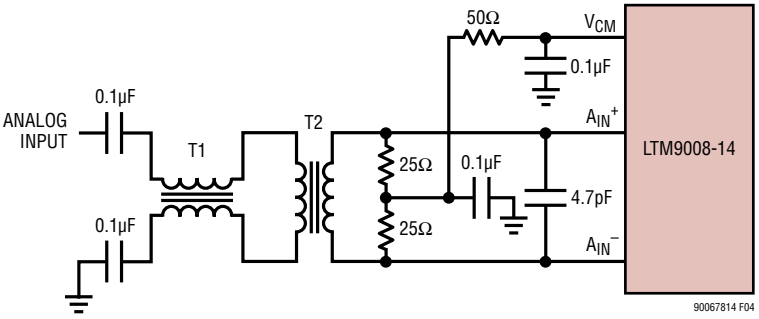
Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

APPLICATIONS INFORMATION

Amplifier Circuits

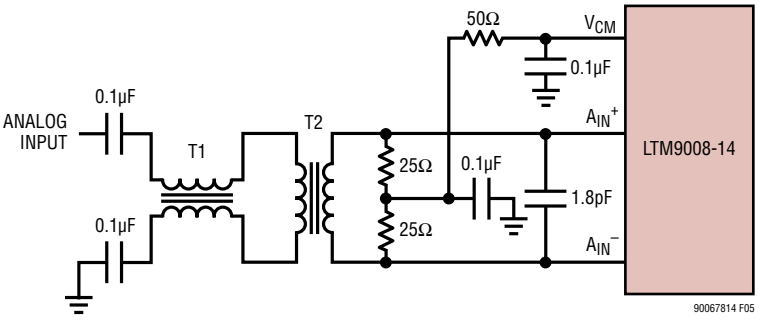
Figure 7 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC-coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion. See back page for a DC-coupled example.

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 4 to 6) should convert the signal to differential before driving the A/D.



T1: MA/COM MABA-007159-000000
T2: MA/COM MABAES0060
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

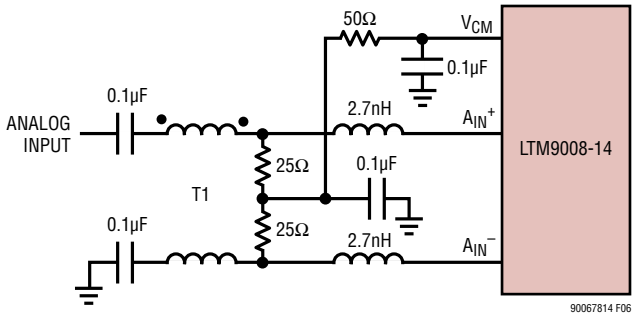
Figure 4. Recommended Front End Circuit for Input Frequencies from 70MHz to 170MHz



T1: MA/COM MABA-007159-000000
T2: COILCRAFT WBC1-1LB
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 5. Recommended Front End Circuit for Input Frequencies from 170MHz to 300MHz

APPLICATIONS INFORMATION



T1: MA/COM ETC1-1-13
RESISTORS, CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 6. Recommended Front End Circuit for Input Frequencies Above 300MHz

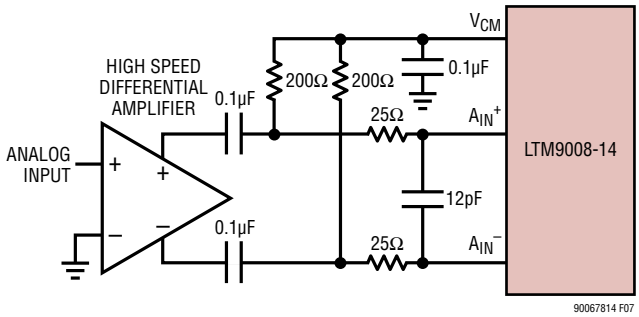


Figure 7. Front End Circuit Using a High Speed Differential Amplifier

APPLICATIONS INFORMATION

Reference

The LTM9008-14/LTM9007-14/LTM9006-14 has an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 9).

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be 1.6 • V_{SENSE}. The reference is shared by all eight ADC channels, so it is not possible to independently adjust the input range of individual channels.

The V_{REF}, SENSE, REFH and REFL pins are internally bypassed, as shown in Figure 8.

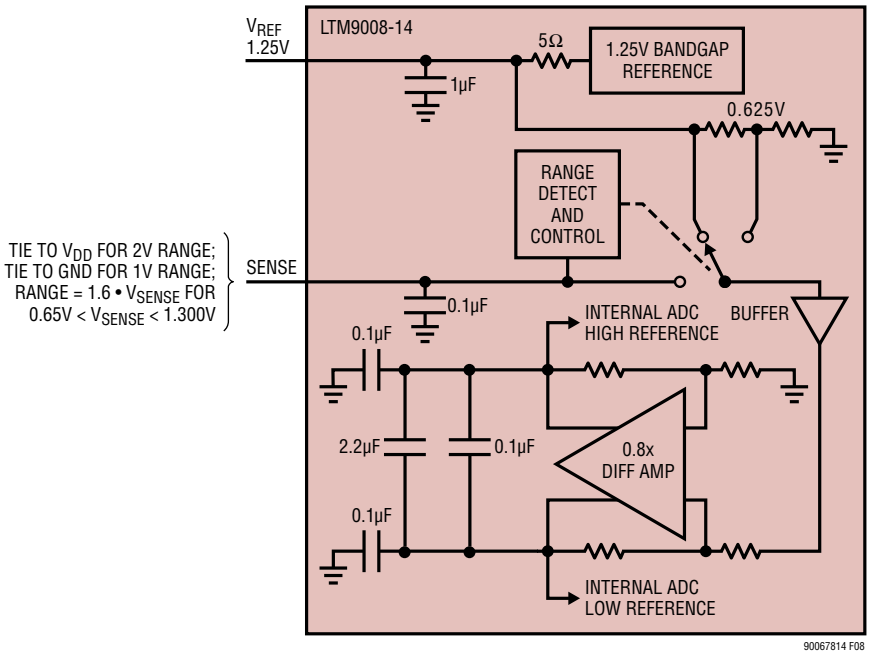


Figure 8. Reference Circuit

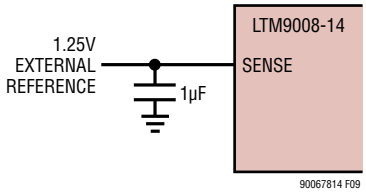


Figure 9. Using an External 1.25V Reference

APPLICATIONS INFORMATION

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 10), and the single-ended encode mode (Figure 11).

The differential encode mode is recommended for sinusoidal, PECL, or LVDS encode inputs (Figures 12 and 13).

The encode inputs are internally biased to 1.2V through 10k equivalent resistance. The encode inputs can be taken above V_{DD} (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC^- should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance ENC^+ should have fast rise and fall times.

The single-ended encode mode should be used with CMOS encode inputs. To select this mode, ENC^- is connected to ground and ENC^+ is driven with a square wave encode

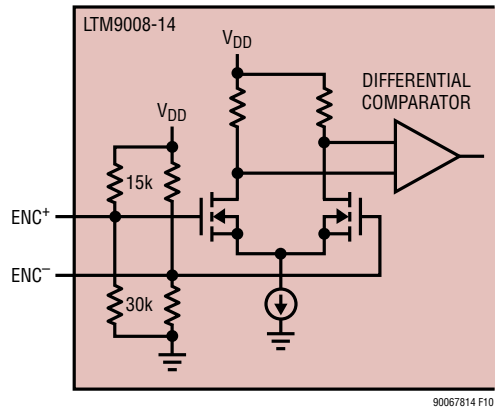


Figure 10. Equivalent Encode Input Circuit for Differential Encode Mode

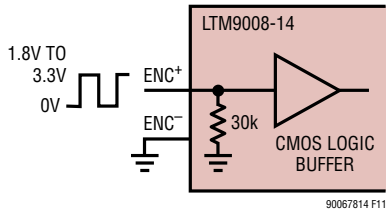


Figure 11. Equivalent Encode Input Circuit for Single-Ended Encode Mode

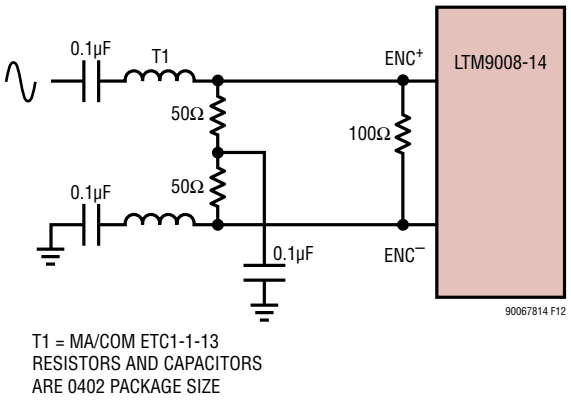


Figure 12. Sinusoidal Encode Drive

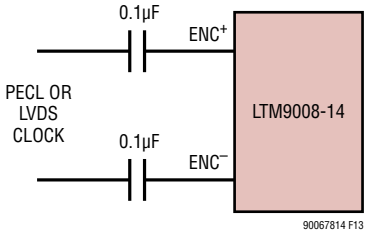


Figure 13. PECL or LVDS Encode Drive