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Anyside™ High Voltage Isolated Switch Controller with I²C Command and Telemetry

FEATURES

- **UL-CSA Recognition Pending: 5kV$_{RMS}$ for One Minute**
- **Reinforced Insulation**
- **Integrated Isolated Power Supply**
- **Adjustable Turn-On Ramp Rate and Current Limit**
- **I²C/SMBus Interface**
- **10-Bit ADC Monitors Current and Two Uncommitted Channels**
- **High Common Mode Transient Immunity: ≥ 30kV/µs**
- Fault Status Alert and Power Good Outputs
- Independent 3V to 5.5V Logic Supply
- ±20kV ESD Across the Isolation Barrier
- Maximum Continuous Working Voltage: 690V$_{RMS}$
- 14.6mm Creepage Distance
- Low Current Shutdown Mode (<10µA)
- 22mm × 9mm × 5.16mm BGA Package

APPLICATIONS

- High Voltage DC Hot Swap
- Live Backplane Insertion
- Isolated Distributed Power Systems
- Power Monitors
- Industrial Control Systems
- Breaking Ground Loops

DESCRIPTION

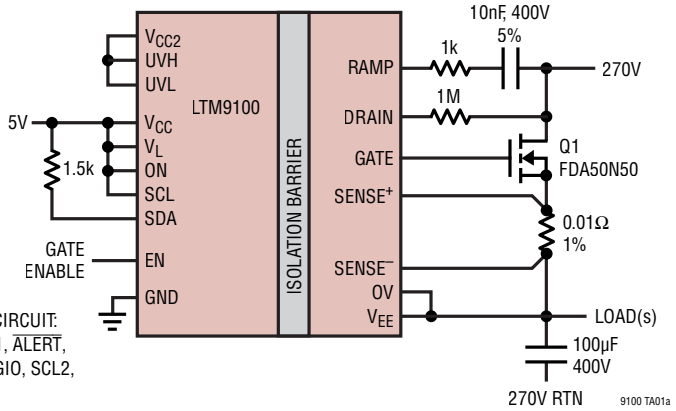
The LTM®9100 µModule® (micromodule) controller is a complete, galvanically isolated switch controller with I²C interface, for use as a load switch or hot swap controller. The load is soft started and controlled by an external N-channel MOSFET switch. Overcurrent protection minimizes MOSFET stress during start-up, input step and output short-circuit conditions. Owing to the isolated, floating character of the switch, it is easily configured for use in high side, low side and floating applications.

A single 5V supply powers both sides of the switch controller through an integrated, isolated DC/DC converter. A separate logic supply input allows easy interfacing with logic levels from 3V to 5.5V, independent of the main supply. Isolated measurements of load current and two additional voltage inputs are made by a 10-bit ADC, and accessed via the I²C interface.

The logic and I²C interface is separated from the switch controller by a 5kV$_{RMS}$ isolation barrier, making the LTM9100 ideal for systems where the switch operates on buses up to 1000V$_{DC}$, as well as for providing galvanic isolation in systems where a ground path is broken to allow large common mode voltage swings. Uninterrupted communication is guaranteed for common mode transients of up to 30kV/µs.

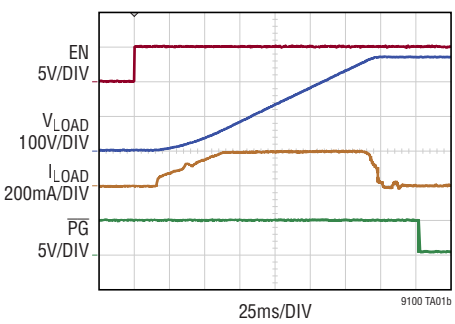
TYPICAL APPLICATION

Isolated High Side Load Switch Driver



PINS NOT USED IN THIS CIRCUIT: ADIN, ADIN2, ADR0, ADR1, $\overline{\text{ALERT}}$, $\overline{\text{ALERT2}}$, EN2, $\overline{\text{PG}}$, $\overline{\text{PG2}}$, PGIO, SCL2, SDA2, SS, TMR, V_S

270V Load Soft-Start



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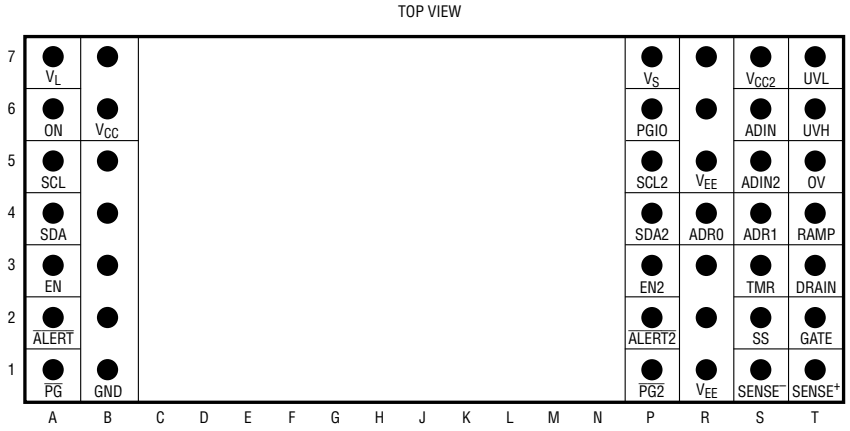
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{CC} to GND ..... –0.3V to 6V
V_L to GND ..... –0.3V to 6V
V_{CC2} to V_{EE} ..... –0.3V to 5.5V
V_S to V_{EE} (Note 3) ..... –0.3V to 10.65V
DRAIN to V_{EE} (Note 4) ..... –0.3V to 3.5V
$\overline{PG}$, $\overline{ALERT}$, EN, SDA, SCL,
ON to GND .....–0.3V to (V_L + 0.3V)
SCL2, SDA2, ADR0, ADR1, $\overline{ALERT2}$, $\overline{PG2}$, ADIN, ADIN2,
RAMP, OV, SS, EN2,
TMR to V_{EE} .....–0.3V to (V_{CC2} + 0.3V)
GATE to V_{EE} ..... –0.3V to (V_S + 0.3V)
UVL, UVH to V_{EE} ..... –0.3V to 10V
PGIO to V_{EE} ..... –0.3V to 80V
$SENSE^+$ to $SENSE^-$..... –0.3V to 0.3V
$SENSE^-$ to V_{EE} ..... –0.3V to 0.3V
Ambient Operating Temperature Range (Note 5)
LTM9100C ..... 0°C to 70°C
LTM9100I .....–40°C to 85°C
LTM9100H .....–40°C to 105°C
Maximum Internal Operating Temperature..... 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Body Reflow Temperature ..... 245°C

PIN CONFIGURATION



BGA PACKAGE
42-LEAD (22mm × 9mm × 5.16mm)

T_{JMAX} = 125°C, PCB = JESD51-9 2s2p: θ_{JA} = 25.6°C/W, θ_{JCtop} = 24.8°C/W, $\theta_{JCbottom}$ = 11.7°C/W, θ_{JB} = 12.1°C/W
HEAT FLOW: θ_{JA} = NORMAL, θ_{JCtop} = 100%, $\theta_{JCbottom}$ = 100%, θ_{JB} = 100% WEIGHT = 2g

ORDER INFORMATION

http://www.linear.com/product/LTM9100#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTM9100CY#PBF	SAC305 (RoHS)	LTM9100Y	e1	BGA	3	0°C to 70°C
LTM9100IY#PBF						–40°C to 85°C
LTM9100HY#PBF						–40°C to 105°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- This product is not recommended for second side reflow. For more information, go to www.linear.com/BGA-assy
- Recommended BGA PCB Assembly and Manufacturing Procedures: www.linear.com/BGA-assy
- BGA Package and Tray Drawings: www.linear.com/packaging
- This product is moisture sensitive. For more information, go to: www.linear.com/BGA-assy

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CC}	Input Supply Range		●	4.5		5.5	V
I_{CC}	Input Supply Current	ON = 0V ON = V_L, No Load	● ●		0 50	10 70	µA mA
V_L	Logic Input Supply Range		●	3		5.5	V
	Logic Input Supply Current	ON = 0V ON = V_L	● ●		0 3.2	10 4.5	µA mA
	V_L Undervoltage Lockout Threshold	V_L Rising	●	2.3		2.7	V
	V_L Undervoltage Lockout Hysteresis				100		mV
V_S	Regulated Output Voltage	I_{LOAD} = 0mA to 35mA	●	9.65	10.4	11.15	V
V_Z	Shunt Regulator Voltage at V_S	I_S = 10mA, V_{CC} = 0V	●	10.4	11.2	12	V
	Shunt Regulator Load Regulation	I_S = 10mA to 25mA, V_{CC} = 0V	●		370	600	mV
I_S	V_S Supply Current	V_S = 10.4V, V_{CC} = 0V	●		7	12	mA
	V_S Undervoltage Lockout Threshold	V_S Rising, V_{CC} = 0V	●	8.5	9	9.5	V
	V_S Undervoltage Lockout Hysteresis	V_{CC} = 0V	●	0.3	0.7	1.1	V
V_{CC2}	Regulated Output Voltage	I_{LOAD} = 0mA to 15mA	●	4.75	5	5.25	V
Gate Drive (EN = V_L, UVL = UVH = V_{CC2}, OV = 0V, unless otherwise noted)							
V_{GATEH}	GATE Pin Output High Voltage	V_S = 10.4V, V_{CC} = 0V	●	9.75	10	10.25	V
$I_{GATE(UP)}$	GATE Pin Pull-Up Current	V_{GATE} = 4V	●	–7.5	–11.5	–15.5	µA
$I_{GATE(OFF)}$	GATE Turn-Off Current	V_{SENSE} = 400mV, V_{GATE} = 4V EN = 0V, V_{GATE} = 4V	● ●	45 120	100 175	150 250	mA mA
$t_{PHL(SENSE)}$	SENSE High to Current Limit Propagation Delay	V_{SENSE} = 100mV to GATE Low V_{SENSE} = 300mV to GATE Low	● ●		0.5 0.2	1.5 0.5	µs µs
	GATE Off Propagation Delay	EN↓ to GATE Low OV↑, UVL↓ to GATE Low	● ●		0.2 1.4	0.5 2	µs µs
	Circuit Breaker Gate Off Delay	V_{SENSE} = 300mV to $\overline{PG2}$↑	●	440	530	620	µs
I_{RAMP}	RAMP Pin Current	V_{SS} = 2.56V	●	–18	–20	–22	µA
V_{SS}	SS Pin Clamp Voltage		●	2.43	2.56	2.69	V
	SS Pin Pull-Up Current	V_{SS} = 0V	●	–7	–10	–13	µA
	SS Pin Pull-Down Current	EN = 0V, V_{SS} = 2.56V	●	6	12	20	mA
Input Pins							
	EN, ON Input Threshold Voltage		●	0.33 • V_L		0.67 • V_L	V
	EN, ON Input Hysteresis	(Note 6)			150		mV
$V_{UVH(TH)}$	UVH Threshold Voltage	V_{UVH} Rising	●	2.518	2.56	2.598	V
$V_{UVL(TH)}$	UVL Threshold Voltage	V_{UVL} Falling	●	2.248	2.291	2.328	V
$\Delta V_{UV(HYST)}$	UV Hysteresis	UVH and UVL Tied Together	●	236	269	304	mV
δV_{UV}	UVH, UVL Hysteresis				15		mV
	UVL Reset Threshold Voltage	V_{UVL} Falling	●	1.12	1.21	1.30	V
	UVL Reset Hysteresis				60		mV
$V_{OV(TH)}$	OV Pin Threshold Voltage	V_{OV} Rising	●	1.735	1.770	1.805	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	OV Pin Hysteresis		●	18	37.5	62	mV
	Current Limit Sense Voltage Threshold	$SENSE^+ – SENSE^–$	●	45	50	55	mV
	PGIO Pin Input Threshold Voltage	V_{PGIO} Rising	●	1.10	1.25	1.40	V
	PGIO Pin Input Hysteresis				100		mV
	Input Current	ON, EN, UVH, UVL, OV, $SENSE^+$ $SENSE^–$	● ●		0 –10	±2 –20	µA µA
Timer							
	TMR Pin High Threshold	V_{TMR} Rising	●	2.43	2.56	2.69	V
	TMR Pin Low Threshold	V_{TMR} Falling	●	40	75	110	mV
	TMR Pin Pull-Up Current	Turn-On and Auto-Retry (Except OC) Delays, V_{TMR} = 0.2V	●	–7	–10	–13	µA
		Power Good and OC Auto-Retry Delays, V_{TMR} = 0.2V	●	–3.5	–5	–7	µA
	TMR Pin Pull-Down Current	Delays Except OC Auto-Retry, V_{TMR} = 2.56V	●	6	12	20	mA
		OC Auto-Retry Delays, V_{TMR} = 2.56V	●	3	5	7	µA
Output Pins							
V_{OH}	Output High Voltage	$\overline{ALERT}$, I_{LOAD} = –4mA, $\overline{PG}$, I_{LOAD} = –2mA	●	V_L – 0.4			V
V_{OL}	Output Low Voltage	$\overline{ALERT}$, I_{LOAD} = 4mA, $\overline{PG}$, I_{LOAD} = 2mA PGIO, I_{LOAD} = 3mA $\overline{ALERT2}$, $\overline{PG2}$, PGIO, I_{LOAD} = 500µA	● ● ●		 0.8 0.15	0.4 1.6 0.4	V V V
	Input Current	PGIO = 80V	●		0	10	µA
	Short-Circuit Current	$0V \le \overline{ALERT} \le V_L$ $0V \le \overline{PG} \le V_L$ $0V \le \overline{ALERT2}, \overline{PG2} \le V_{CC2}$ $0V \le EN2 \le V_{CC2}$	● ●		 ±30 ±30 	±85 ±2	mA mA mA mA
ADC							
	Resolution (No Missing Codes)	(Note 6)	●	10			Bits
INL	Integral Nonlinearity	SENSE ADIN, ADIN2	● ●		±0.5 ±0.25	±2.5 ±1.25	LSB LSB
	Offset Error	SENSE ADIN, ADIN2	● ●			±2.25 ±1.25	LSB LSB
	Full-Scale Voltage	SENSE ADIN, ADIN2	● ●	62.8 2.514	64 2.560	65.2 2.606	mV V
	Total Unadjusted Error	SENSE ADIN, ADIN2	● ●			±1.8 ±1.6	% %
	Conversion Rate		●	5.5	7.3	9	Hz
	ADIN, ADIN2 Pin Input Resistance	ADIN, ADIN2 = 1.28V	●	2	10		MΩ
	ADIN, ADIN2 Pin Input Current	ADIN, ADIN2 = 2.56V	●		0	±2	µA
I^2C Interface							
	ADR0, ADR1 Input High Threshold		●	V_{CC2} – 0.8	V_{CC2} – 0.5	V_{CC2} – 0.3	V
	ADR0, ADR1 Input Low Threshold		●	0.3	0.5	0.8	V
	ADR0, ADR1 Input Current	ADR0, ADR1 = 0V, V_{CC2} ADR0, ADR1 = 0.8V, (V_{CC2} – 0.8V)	● ●	 ±10		±80 	µA µA
	Input Threshold Voltage	SCL, SDA SDA2	● ●	0.3 • V_L 0.3 • V_{CC2}		0.7 • V_L 0.7 • V_{CC2}	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Input Current	SCL, SDA = V_L or 0V	●			±2	µA
	Input Hysteresis	SCL, SDA SDA2			0.05 • V_L 0.05 • V_{CC2}		mV mV
V_{OH}	Output High Voltage	SCL2, I_{LOAD} = –2mA	●	V_{CC2} – 0.4			V
V_{OL}	Output Low Voltage	SDA, I_{LOAD} = 3mA, SCL2, I_{LOAD} = 2mA SDA2, No Load, SDA = 0V	● ●			0.4 0.45	V V
	Input Pin Capacitance	SCL, SDA, SDA2 (Note 6)	●			10	pF
	Bus Capacitive Load	SCL2, Standard Speed (Note 6) SCL2, Fast Speed SDA, SDA2, SR ≥ 1V/µs, Standard Speed (Note 6) SDA, SDA2, SR ≥ 1V/µs, Fast Speed	● ● ● ●			400 200 400 200	pF pF pF pF
	Minimum Bus Slew Rate	SDA, SDA2		1			V/µs
	Short-Circuit Current	SDA2 = 0, SDA = V_L 0V ≤ SCL2 ≤ V_{CC2} SDA = 0, SDA2 = V_{CC2} SDA = V_L, SDA2 = 0	●		 ±30 6 –1.8	100	mA mA mA mA
ESD (HBM) (Note 6)							
	Isolation Boundary	(V_{CC2}, V_S, V_{EE}) to (V_{CC}, V_L, GND) in Any Combination			±20		kV
	Isolated Side Interface Pins	GATE to (V_S, V_{EE}) in Any Combination (RAMP, DRAIN, $SENSE^+$, $SENSE^–$) to (V_{CC2}, V_{EE}) in Any Combination			±8		kV
	All Other Pins				±3.5		kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Timing							
t_{PHL}, t_{PLH}	Propagation Delay	($\overline{PG2}$, $\overline{ALERT2}$) to ($\overline{PG}$, $\overline{ALERT}$), C_L = 15pF (Figure 1) EN to EN2 (0.5 • V_L to 0.1 • V_{CC2}), C_L = 15pF (Figure 1)	●	35	60	150	ns
t_R, t_F	Rise and Fall Time	$\overline{ALERT}$, C_L = 15pF (Figure 1) $\overline{PG}$, C_L = 15pF (Figure 1)	● ●		7 30	30 50	ns ns
t_{PZH}, t_{PZL}	ON Enable Time	ON↑ to ($\overline{PG}$, $\overline{ALERT}$), R_L = 1kΩ, C_L = 15pF (Figure 2)	●			320	µs
t_{PHZ}, t_{PLZ}	ON Disable Time	ON↓ to ($\overline{PG}$, $\overline{ALERT}$), R_L = 1kΩ, C_L = 15pF (Figure 2)	●			70	ns
I^2C Interface Timing							
	Maximum Data Rate	(Note 7)	●	400			kHz
t_{PHL}, t_{PLH}	Propagation Delay	SCL to SCL2, C_L = 15pF (Figure 1) SDA to SDA2, R_L = Open, C_L = 15pF (Figure 3) SDA2 to SDA, R_L = 1.1kΩ, C_L = 15pF (Figure 3)	● ● ●		150 150 300	225 250 500	ns ns ns
	Low Period of SCL Clock	(Note 6)		1.3			µs

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, and GND = V_{EE} = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	High Period of SCL Clock	(Note 6)		600			ns
	Hold Time (Repeated) Start	(Note 6)		600			ns
	Set-Up Time Repeated Start	(Note 6)		600			ns
$t_{HD(DAT)}$	Data Hold Time	(Note 6)			600		ns
$t_{SU(DAT)}$	Data Set-Up Time	(Note 6)		100			ns
	Set-Up Time for Stop	(Note 6)		600			ns
	Stop to Start Bus Free Time	(Note 6)		1.3			µs
t_R	Rise Time	SDA2, C_L = 200pF (Figure 3) SDA, R_L = 1.1kΩ, C_L = 200pF (Figure 3) SCL2, C_L = 200pF (Figure 1)	● ● ●	40 40		350 250 250	ns ns ns
t_F	Fall Time	SDA2, C_L = 200pF (Figure 3) SDA, R_L = 1.1kΩ, C_L = 200pF (Figure 3) SCL2, C_L = 200pF (Figure 1)	● ● ●	40 40		250 250 250	ns ns ns
t_{PZL}	ON Enable Time	ON↑ to SDA, R_L = 1kΩ, C_L = 15pF (Figure 2)	●			320	µs
t_{PLZ}	ON Disable Time	ON↓ to SDA, R_L = 1kΩ, C_L = 15pF (Figure 2)	●			70	ns
	Pulse Width of Spikes Suppressed by Input Filter	SDA, SDA2, SCL	●	0		50	ns
Power Supply							
	Power-Up Time	ON↑ to V_S (Min) ON↑ to V_{CC2} (Min)	● ●		0.2 0.2	1.5 2	ms ms

ISOLATION CHARACTERISTICS

Specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Rated Dielectric Insulation Voltage	1 Minute, Derived from 1 Second Test 1 Second (Notes 8, 9)	5 6			kV_{RMS} kV_{RMS}
	Common Mode Transient Immunity	V_{CC} = V_L = ON = 5V, ΔV_{CM} = 1kV, Δt = 33ns (Note 6)	30	50		kV/µs
V_{IORM}	Maximum Continuous Working Voltage	(Notes 6,10)	1000 690			V_{PEAK} V_{RMS}
	Partial Discharge	V_{PD} = 1840V_{PEAK} (Note 8)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 6)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 6)		0.017		mm
DTI	Distance Through Insulation	(Note 6)		0.2		mm
	Input to Output Resistance	(Notes 6, 8)	1	5		TΩ
	Input to Output Capacitance	(Notes 6, 8)		5		pF
	Creepage Distance	(Note 6)		14.6		mm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to 0V unless otherwise noted.

Note 3: An internal shunt regulator limits the V_S pin to a minimum of 10.65V. Driving this pin to voltages beyond 10.65V may damage the part. The pin can be safely tied to higher voltages through a resistor that limits the current to less than 50mA.

Note 4: An internal clamp limits the DRAIN pin to a minimum of 3.5V. Driving this pin to voltages beyond the clamp may damage the part. The pin can be safely tied to higher voltages through a resistor that limits the current to less than 2mA.

Note 5: This µModule includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure. Thermal shutdown will result in the loss of the internally generated supply voltages (V_S and V_{CC2}) and subsequent shutdown of the GATE pin. Thermal shutdown is not internally latched, the part will automatically restart once the junction temperature decreases and start-up conditions are met. Note that any I^2C data configuration is lost on power failure.

Note 6: Guaranteed by design and not subject to production test.

Note 7: Maximum data rate is guaranteed by other measured parameters and is not tested directly.

Note 8: Device is considered a 2-terminal device. Pin group A1 through B7 shorted together and pin group P1 through T7 shorted together.

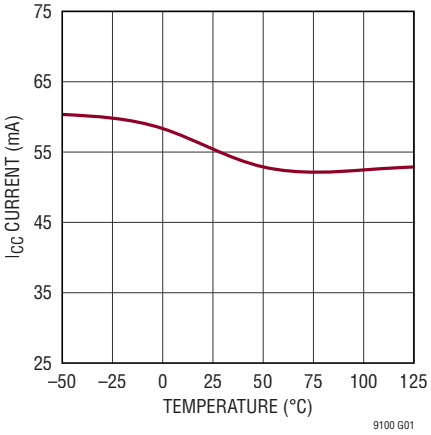
Note 9: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

Note 10: The DC continuous working voltage is equivalent to the peak value.

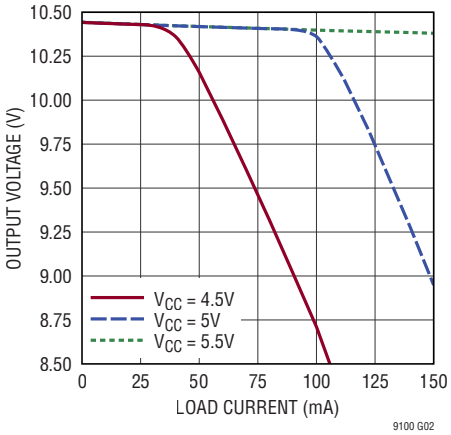
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

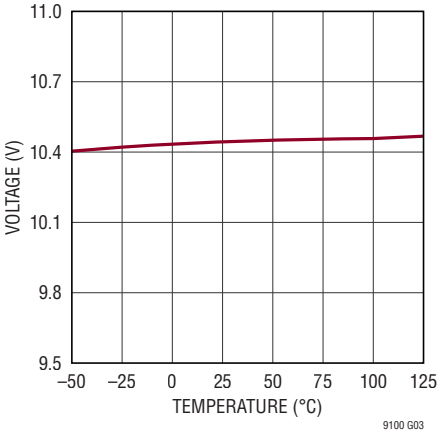
V_{CC} Supply Current vs Temperature



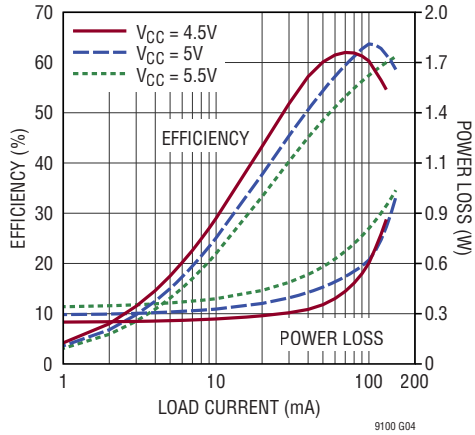
V_S Output Voltage vs Load Current



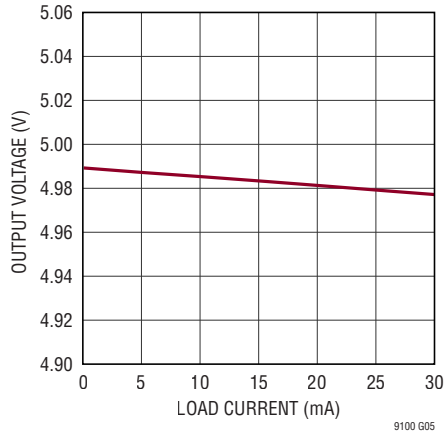
V_S Output Voltage vs Temperature



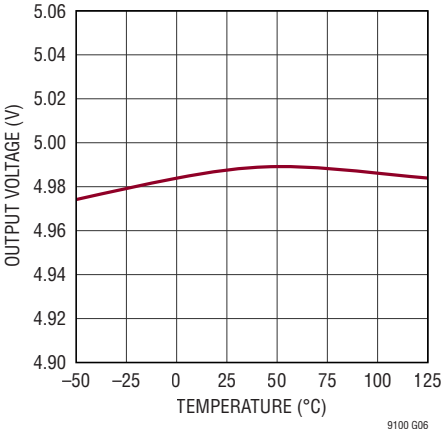
V_S Efficiency and Power Loss vs Load Current



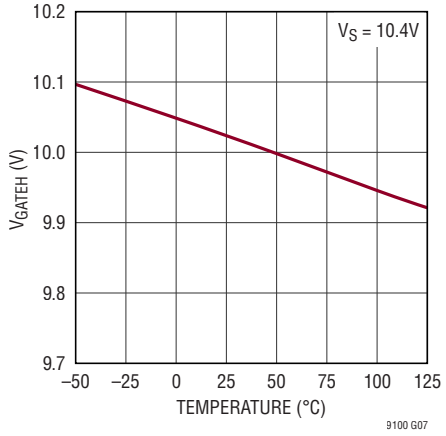
V_{CC2} Output Voltage vs Load Current



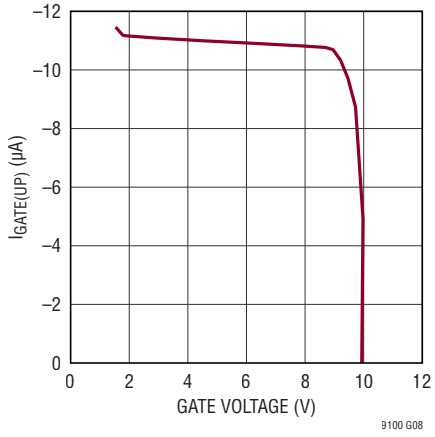
V_{CC2} Output Voltage vs Temperature



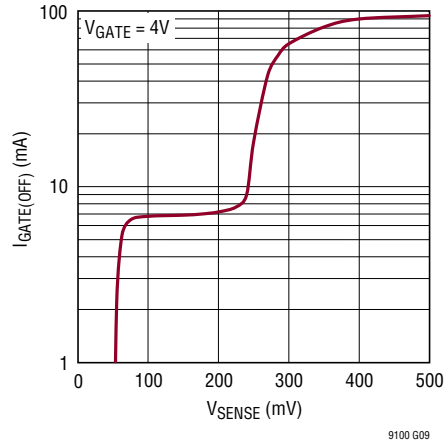
Gate Output High Voltage vs Temperature



Gate Pull-Up Current vs Gate Voltage



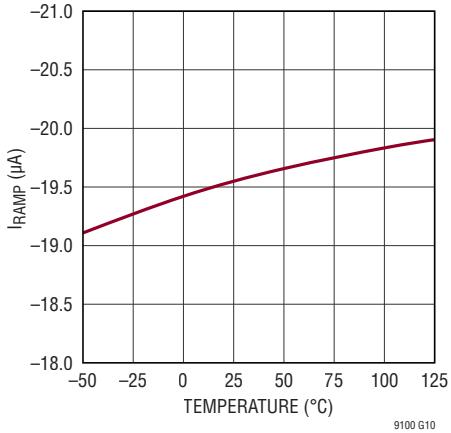
Gate Turn-Off Current vs SENSE Voltage



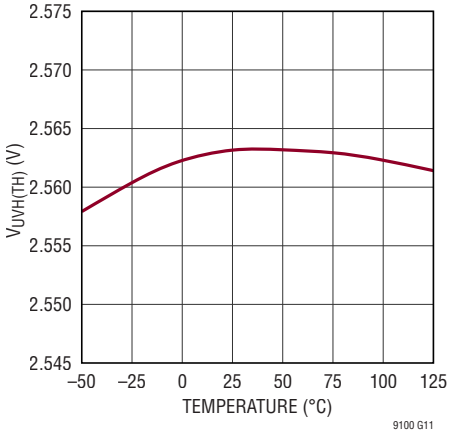
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

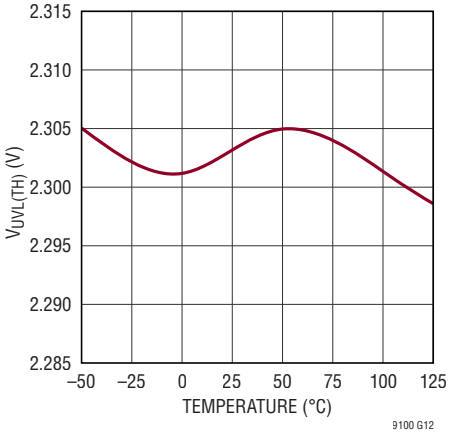
Ramp Pin Current vs Temperature



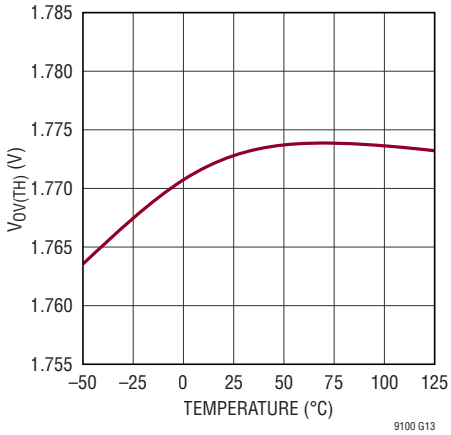
UVH Threshold vs Temperature



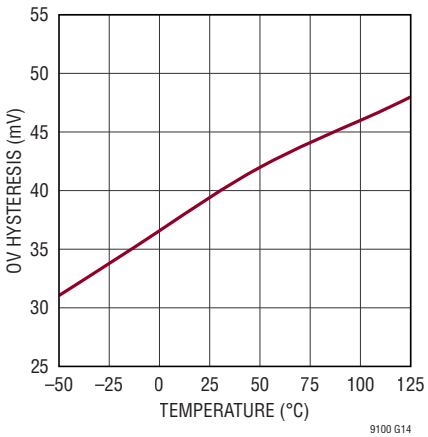
UVL Threshold vs Temperature



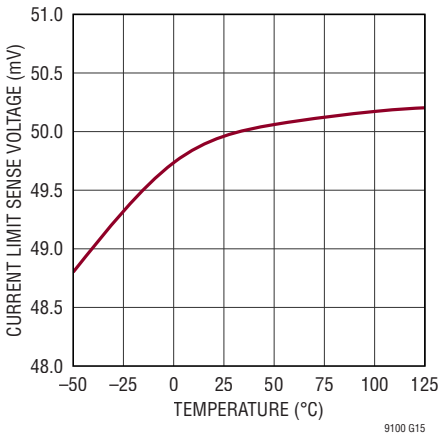
OV Threshold vs Temperature



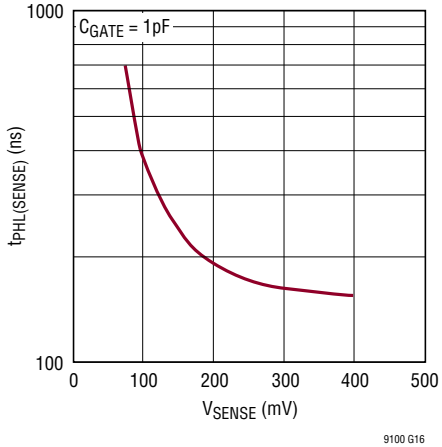
OV Hysteresis vs Temperature



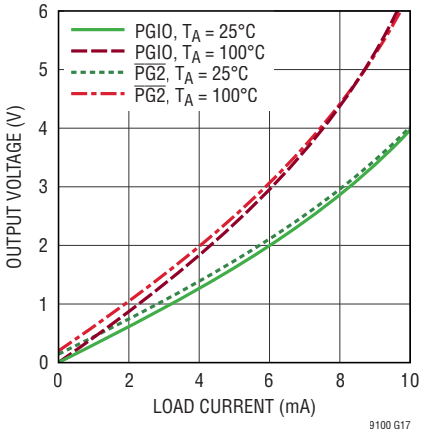
Current Limit Voltage vs Temperature



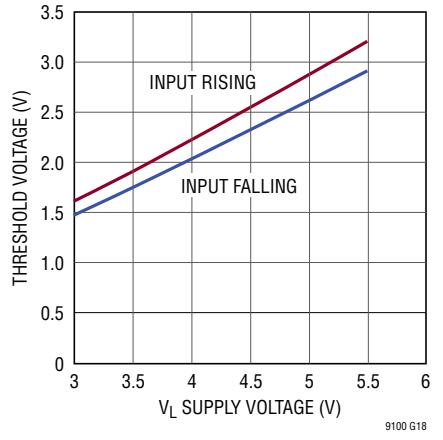
Current Limit Propagation Delay ($t_{PHL(SENSE)}$) vs V_{SENSE}



$\overline{PG2}$, PGIO Output Low Voltage vs Load Current



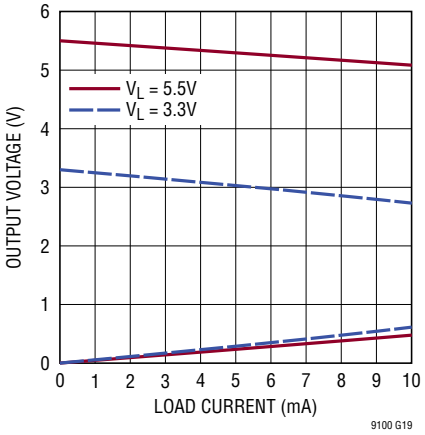
Logic Input Threshold vs V_L Supply Voltage



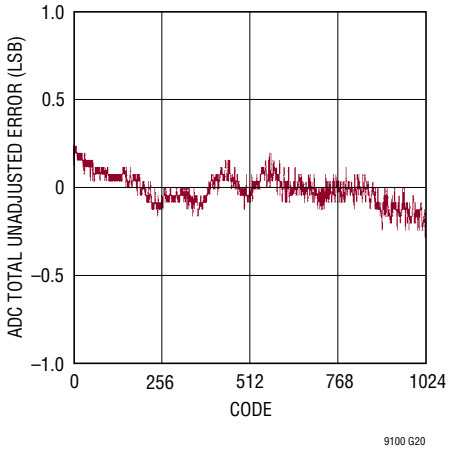
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

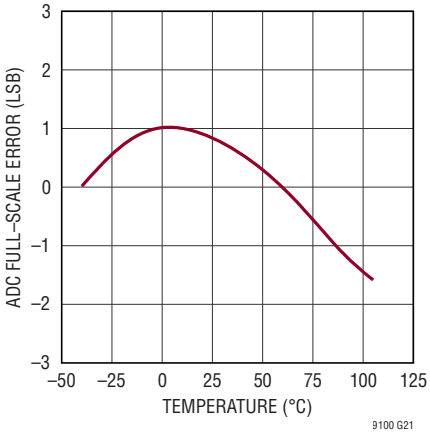
Logic Output Voltage vs Load Current



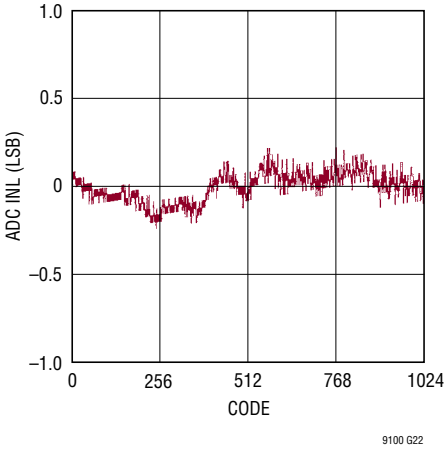
ADC Total Unadjusted Error vs Code (ADIN Pin)



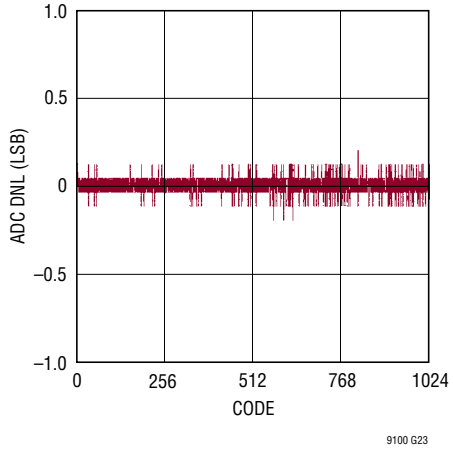
ADC Full-Scale Error vs Temperature (ADIN Pin)



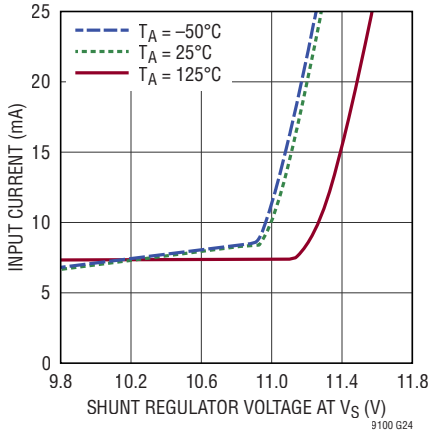
ADC INL vs Code (ADIN Pin)



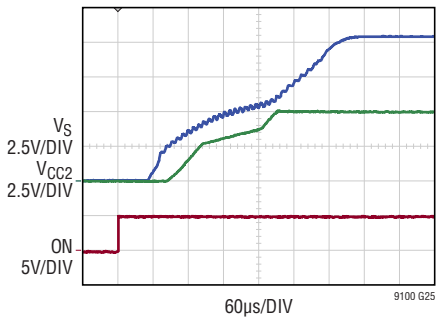
ADC DNL vs Code (ADIN Pin)



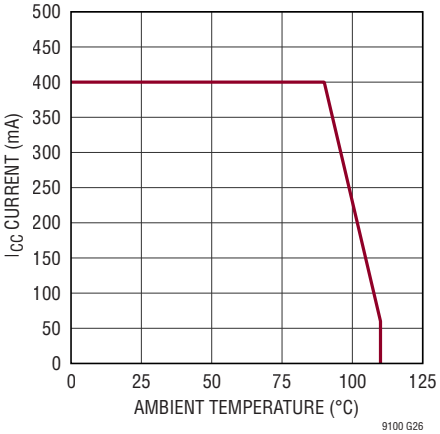
Input Current vs Shunt Regulator Voltage



Power-On Sequence



Derating for 125°C Maximum Internal Operating Temperature



PIN FUNCTIONS

Logic Side

$\overline{PG}$ (A1): Power Good Status Output, Referenced to V_L and GND. This logic pin pulls low and stays latched two timer delays after the isolated side power switch is on (when GATE reaches approximately 9.5V and DRAIN is within 1.77V of V_{EE}). The power good output is reset in all GATE pull-down events except an overvoltage fault. Under the condition of an isolation communication failure this output is in a high impedance state. A communication failure may occur due to extreme electromagnetic events including common mode transients or electrical overstress. Communication is automatically re-established if permanent damage has not occurred.

$\overline{ALERT}$ (A2): Fault Alert Output, Referenced to V_L and GND. This logic pin pulls low when an isolated side fault occurs as configured by the I²C ALERT register. See Applications Information. Under the condition of an isolation communication failure this output is in a high impedance state.

EN (A3): GATE Enable Input, Referenced to V_L and GND. A rising edge turns on the isolated side GATE pin while a falling edge turns it off. This pin is also used to configure the state of bit 3 (GATE_CTRL) in the I²C CONTROL (D) register (and hence the GATE pin) at power-up. For example if EN is tied high, then register bit D3 goes high one timer cycle after power-up. Likewise, if the EN pin is tied low, then the GATE pin remains low after power-up until the EN pin is transitioned high. The GATE pin may be controlled directly by I²C via register bit D3. A high to low transition clears any driver faults. Connect to V_L if not used.

SDA (A4): Serial I²C Data Pin, Referenced to V_L and GND. Bidirectional logic pin connected to isolated side SDA2 pin and configurable switch driver through isolation barrier. An external pull-up resistor or current source is required. Under the condition of an isolation communication failure this pin is in a high impedance state. Connect to V_L if not used.

SCL (A5): Serial I²C Clock Pin, Referenced to V_L and GND. Logic input connected to isolated side SCL2 pin and configurable switch driver through isolation barrier. An external pull-up resistor or current source is required. Connect to V_L if not used.

ON (A6): Module Enable Pin. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state, and the isolated side is unpowered. The ON pin may be used to enable the isolated side power switch driver by connecting EN to V_L. A low to high transition of ON would then enable the isolated side gate drive after the internal isolated side supply voltage exceeds approximately 9V followed by a timer delay. Connect to V_L if not used.

V_L (A7): Logic Supply. Interface supply voltage for pins $\overline{PG}$, $\overline{ALERT}$, EN, SDA, SCL, and ON. Operating voltage is 3V to 5.5V. Internally bypassed with 1µF.

GND (B1 TO B5): Circuit Ground.

V_{CC} (B6, B7): Isolated Power Converter Supply Voltage. Operating voltage is 4.5V to 5.5V. Internally bypassed with 1µF. This pin may be left unconnected or grounded if V_S is driven by an external voltage.

Isolated Side

$\overline{PG2}$ (P1): Power Good Status Output, Referenced to V_{CC2} and V_{EE}. This logic pin pulls low and stays latched two timer delays after the power switch is on (when GATE reaches approximately 9.5V and DRAIN is within 1.77V of V_{EE}). The power good output is reset in all GATE pull-down events except an overvoltage fault. Internally connected to V_{CC2} by a 10k resistor.

$\overline{ALERT2}$ (P2): Fault Alert Output, Referenced to V_{CC2} and V_{EE}. This logic pin pulls low when an isolated side fault occurs as configured by the I²C ALERT register. See Applications Information. Internally connected to V_{CC2} through a 10k resistor.

EN2 (P3): Enable Output, Referenced to V_{CC2} and V_{EE}. Logic output connected to logic side EN pin through isolation barrier and 4k resistor and to the switch driver. EN2 may be driven externally, see Applications Information. Internally connected to V_{EE} through 4k and 10k resistors.

SDA2 (P4): Serial I²C Data Pin, Referenced to V_{CC2} and V_{EE}. Bidirectional logic pin connected to logic side SDA pin through isolation barrier and to the switch driver. Allows for I²C bus expansion. Output is biased high by a

PIN FUNCTIONS

1.8mA current source. Under the condition of an isolation communication failure this output defaults to a high state.

SCL2 (P5): Serial I^2C Clock Output, Referenced to V_{CC2} and V_{EE}. Logic output connected to logic side SCL pin through isolation barrier and to the switch driver. Allows for I^2C bus expansion. Clock is unidirectional from logic to isolated side. Under the condition of an isolation communication failure this output defaults to a high state.

PGIO (P6): General Purpose Input/Output. Logic input and open-drain output. Default is output which pulls low two timer delays after the $\overline{PG}$ pin goes low to indicate a second power good output. Configure according to Table 4.

V_S (P7): 10.4V Nominal Isolated Supply Output Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 10.4V. V_S may be driven by an external supply if V_{CC} is not connected or grounded. If driven externally connect pin to a positive supply through a dropping resistor, see Applications Information. An internal shunt regulator clamps V_S (V_Z) at 11.2V. An undervoltage lockout (UVLO) circuit holds GATE low until V_S is above 9V. Internally bypassed with 1µF.

V_{EE} (R1 to R3, R5 to R7): Isolated Circuit Common.

ADR0, ADR1 (R4, S4): Serial Bus Address Inputs, Referenced to V_{CC2} and V_{EE}. Connecting these pins to V_{EE}, V_{CC2}, or floating configures one of nine possible addresses. See Table 1 in Applications Information.

$SENSE^-$ (S1): Negative Current Limit Sense Input. Kelvin connection for external current sense resistor (R_S). Internally filtered with 220pF.

SS (S2): Soft-Start Input. This pin is used to ramp inrush current during start-up, thereby effecting control over di/dt. Pin connected internally to a 220nF capacitor, additional external capacitance (C_{SS}) may be added. An internal 10µA current source charges the internal and external capacitance creating a voltage ramp. This voltage is converted to a current to charge the GATE pin up and to ramp the output voltage down. The SS pin is internally clamped to 2.56V limiting $I_{GATE(UP)}$ to 11.5µA and I_{RAMP} to 20µA.

TMR (S3): Delay Timer Input. This pin is used to create timing delays at power-up, when power good outputs pull down and when auto-retrying after faults (except overvoltage fault). Pin connected internally to a 47nF capacitor, additional external capacitance (C_{TMR}) may be added to extend the nominal delay beyond 12ms. Internal pull-up currents of 10µA and 5µA and pull-down currents of 5µA and 12mA configure the delay periods as multiples of a nominal delay t_D = 12ms + 256ms • C_{TMR}/µF. Delays for power-up and auto-retry following an undervoltage fault are the same as the nominal delay. Delays for sequenced power good outputs are twice the nominal delay. Delay for auto-retry following overcurrent fault are four times the nominal delay.

ADIN2, ADIN (S5, S6): ADC Inputs, Referenced to V_{EE}. A voltage between 0V and 2.56V applied to these pins is measured by the internal module ADC. Connect to V_{EE} if unused.

V_{CC2} (S7): 5V Nominal Isolated Supply Output Voltage. Linear regulated output generated from V_S with a UVLO threshold of 4.25V. This voltage powers up the isolated data converter and logic control circuitry. Internally bypassed with 1µF.

$SENSE^+$ (T1): Positive Current Limit Sense Input. Load current through an external current sense resistor (R_S) is monitored and controlled by an active current limit amplifier to 50mV/R_S. Once V_{SENSE} reaches 50mV, a circuit breaker timer starts and turns off the switch after 530µs. In the event of a catastrophic short-circuit, if V_{SENSE} crosses 250mV, a fast response comparator immediately pulls the GATE pin down to turn off the MOSFET. Internally filtered with 220pF.

GATE (T2): N-Channel MOSFET Switch (FET) Gate Drive Output. This pin is pulled up by an internal current source I_{GATE} (11.5µA when the SS pin reaches its clamping voltage). GATE stays low until V_S and V_{CC2} cross the UVLO thresholds, EN is high, UV and OV conditions are satisfied and the adjustable power-up timer delay expires. During turn-off, caused by faults or undervoltage lockout, a 110mA pull-down current between GATE and V_{EE} is activated. Internally filtered with 220pF. Under the condition of an isolation communication failure the switch is turned off.

DRAIN (T3): Drain Sense Input. Connect an external resistor between this pin and the drain terminal of the FET. Size the resistor for 50µA nominal current, do not exceed

PIN FUNCTIONS

2mA. The voltage at this pin is internally clamped to 4V. When the DRAIN pin voltage is less than 1.77V and the GATE pin voltage is approximately 9.5V the power good output is asserted after two timer delays. Internally filtered with 220pF.

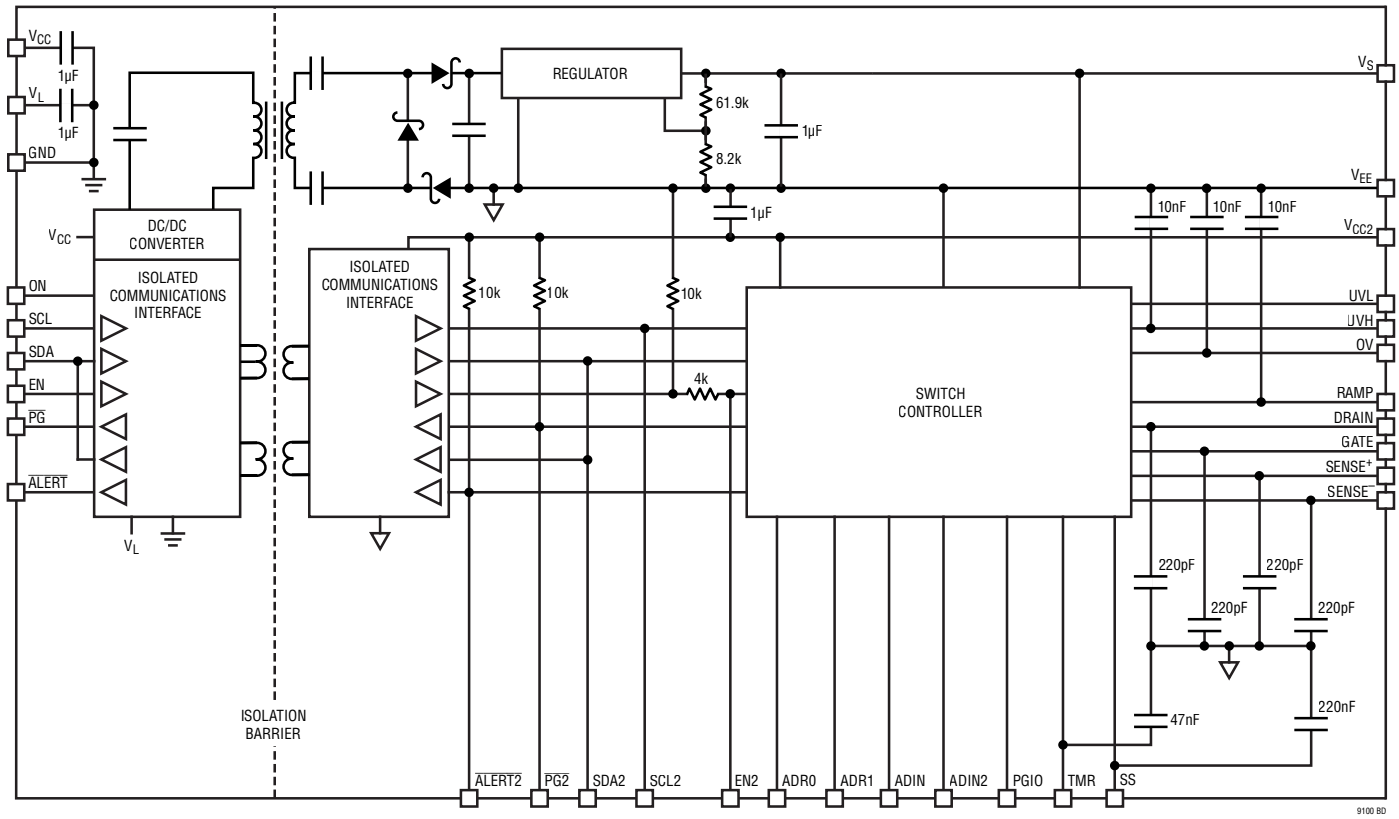
RAMP (T4): Inrush Current Ramp Control Pin. The inrush current is adjusted by placing a capacitor (C_R) between the RAMP pin and the drain terminal of the FET. At start-up, the GATE pin is pulled up by $I_{GATE(UP)}$ until the FET begins to turn on. A current, I_{RAMP}, then flows through C_R to ramp down the drain voltage. The value of I_{RAMP} is controlled by the SS pin voltage. When the SS pin reaches its clamp voltage (2.56V), I_{RAMP} = 20µA. For a capacitive load the RAMP rate of the FET drain voltage (V_{DRAIN}) and the load capacitor C_L set the inrush current: $I_{INRUSH} = (C_L/C_R) \bullet I_{RAMP}$. Internally filtered with 10nF; see Applications Information.

OV (T5): Overvoltage Detection Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at this pin rises above 1.77V, the FET is turned off. The overvoltage condition does not affect the status of the power good outputs. Internally filtered with 10nF. Connect to V_{EE} if not used.

UVH (T6): Undervoltage High Level Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at the UVH pin rises above 2.56V and UVL is above 2.291V, the FET is allowed to turn on. Internally filtered with 10nF. Connect to V_{CC2} if not used.

UVL (T7): Undervoltage Low Level Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at the UVL pin drops below 2.291V and UVH is below 2.56V, the FET is turned off and the power good outputs go high. Pulling this pin below 1.21V resets faults and allows the FET to turn back on. Connect to V_{CC2} if unused.

BLOCK DIAGRAM



TEST CIRCUITS

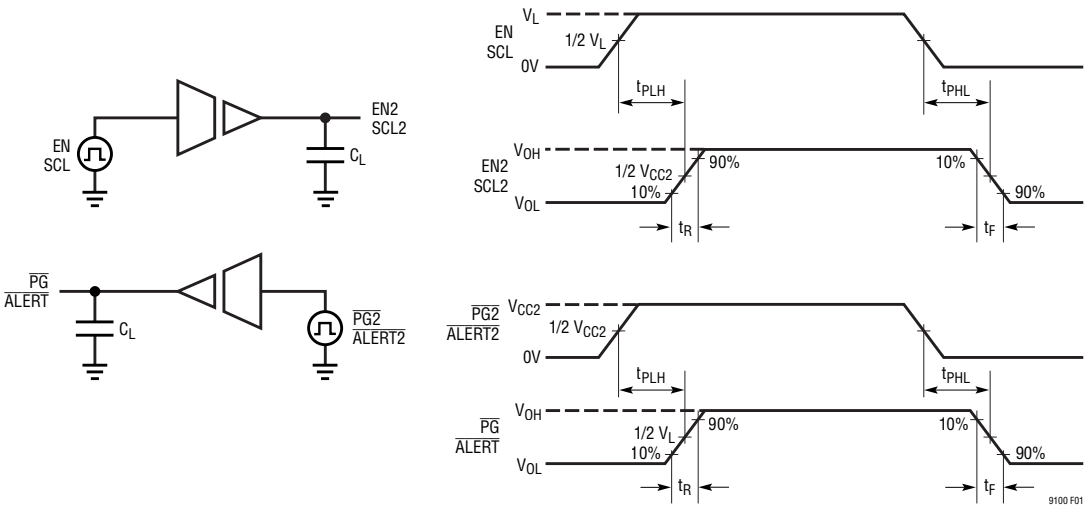


Figure 1. Logic Timing Measurements

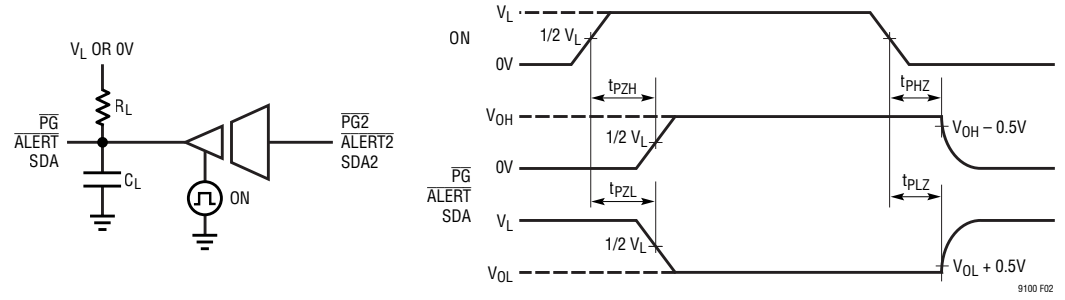


Figure 2. ON Enable/Disable Time

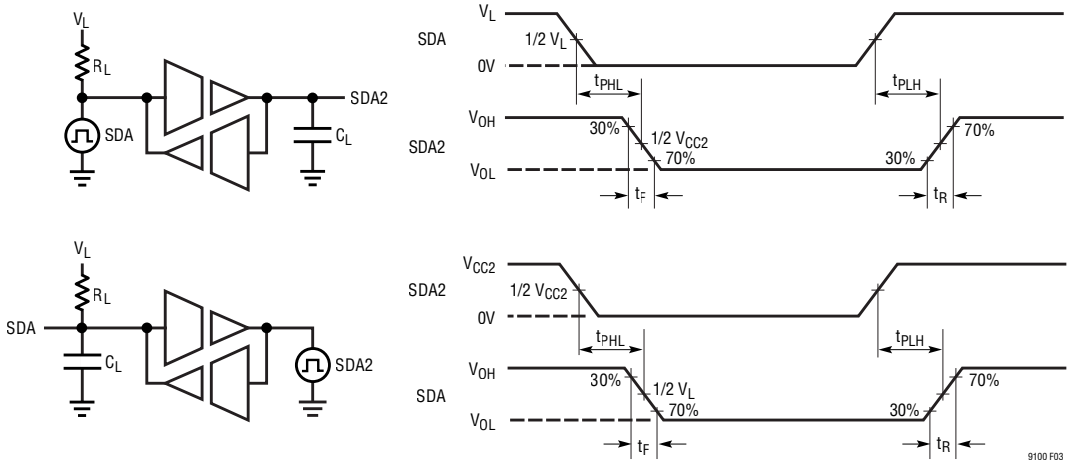


Figure 3. I²C Timing Measurements

APPLICATIONS INFORMATION

Overview

The LTM9100 µModule switch controller provides a galvanically-isolated robust driver interface, complete with decoupling capacitors. The LTM9100 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM9100 blocks high voltage differences and eliminates ground loops and is extremely tolerant of common mode transients between ground planes. Error-free operation is maintained through common-mode events as fast as 70kV/µs providing excellent noise isolation.

The LTM9100 is designed to turn a supply voltage on and off in a controlled manner. In normal operation after initial power up and time delay (TMR), the GATE pin turns on a FET passing power to the load. The GATE pin is powered by an internal isolated DC/DC converter with output voltage (V_S) of approximately 10.4V.

An amplifier connected to the SENSE pins is used for overcurrent and short-circuit protection. It monitors the load current through an external sense resistor R_S. In an overcurrent condition, the current is limited to 50mV/R_S by regulating GATE. If the overcurrent condition remains for more than 530µs, GATE is turned off.

The DRAIN and GATE voltages are monitored to determine if the FET is fully enhanced. Upon successful turn on of the FET, two power good signals are presented on the $\overline{PG}$ and PGIO pins. They allow enabling and sequencing of loads. The PGIO pin can also be configured for a general purpose input or output.

The isolated side logic circuits are powered by an internally generated 5V supply (V_{CC2}). Prior to turning on the FET, both the internal gate drive supply voltage V_S and V_{CC2} voltages must exceed their undervoltage lockout thresholds. In addition, the control inputs UVH, UVL, OV and EN are monitored. The FET is held off until all start-up conditions are met.

A 10-bit analog-to-digital converter (ADC) is included in the LTM9100. The ADC measures the SENSE voltage as well as voltages at the ADIN2 and ADIN pins, for auxiliary functions such as sensing bus voltage or temperature, etc.

An I^2C interface is provided to read the ADC data registers. It also allows the host to poll the device and determine if a fault has occurred. If the ALERT line is used as an interrupt, the host can respond to a fault in real time. Two three-state pins, ADR0 and ADR1, are used to program eight possible device addresses.

The interface can also be pin configured for a single-wire broadcast mode, sending ADC data and fault status through the SDA pin to the host without clocking the SCL line. This single-wire, one-way communication can simplify system design.

The LTM9100 is ideally suited for distributed DC power systems and off-line power converter systems requiring an isolated communication and control interface. A basic 200W –48V distributed power application circuit using the LTM9100 is shown in Figure 4.

APPLICATIONS INFORMATION

µModule Technology

The LTM9100 utilizes isolator µModule technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the µModule substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The µModule technology provides the means to combine the isolated signaling with multiple regulators and powerful isolated DC/DC converter in one small package.

DC/DC Converter

The LTM9100 contains a fully integrated DC/DC converter, including the transformer, so that no external components are necessary for powering the isolated side. The logic side contains a full-bridge driver, running at 2MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a symmetric voltage doubler. This topology reduces common mode voltage perturbations on the isolated side ground, and eliminates transformer saturation caused by secondary imbalances.

The DC/DC converter is connected to a low dropout regulator (LDO) to provide a regulated 10.4V output (V_S) for the GATE driver supply. V_S is decoupled internally by a 1µF capacitor.

The data converter and logic control circuits are powered by an internal linear regulator that derives 5V from the V_S supply. The 5V output is available at the V_{CC2} pin for driving external circuits (up to 15mA load current). V_{CC2} is decoupled internally by a 1µF capacitor.

Powering the LTM9100 from the Bus

The internal isolated power converter may be disabled by floating or grounding the V_{CC} pin. Isolated power may then be derived from the external bus voltage by using either a low or high side circuit depending upon the application's location of the LTM9100.

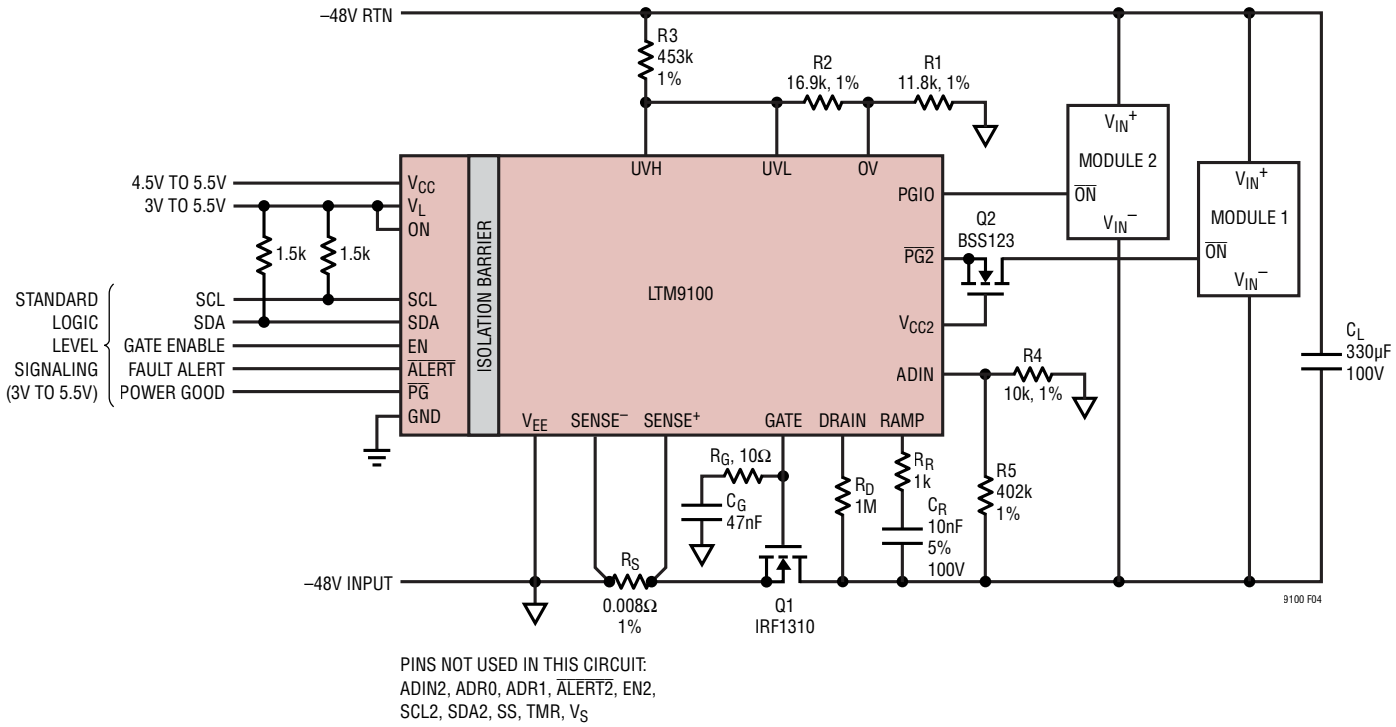


Figure 4. –48V/200W Low Side Hot Swap Controller Using LTM9100 with Current and Input Voltage Monitoring (5.6A Current Limit, 0.66A Inrush)

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Low Side Applications

Isolated power may be derived through a current limiting resistor (R_{LIM}) to the V_S pin (Figure 5) for low side configurations where V_{EE} is referenced to the negative side of the bus supply voltage. An internal shunt regulator clamps the voltage at V_S to 11.2V (V_Z) and provides power to the GATE driver. R_{LIM} should be chosen to accommodate the maximum isolated side supply current requirement of the LTM9100 (10mA), plus the supply current required by any external devices connected to V_S and V_{CC2}, at the minimum VBUS operation voltage. Alternative means of current limiting can also be used, e.g. an analog (active) current limiter (ACL).

$$R_{LIM} \leq \frac{VBUS_{(MIN)} - V_{Z(MAX)}}{I_{S(EXT)} + I_{CC2(EXT)} + 10mA}$$

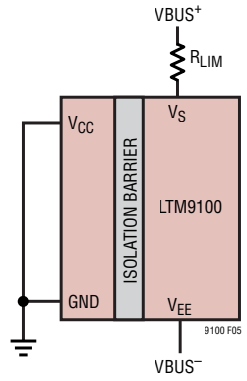

Figure 5. Isolated Side Power Derived From External Bus

$$P_{MAX} = \frac{[VBUS_{(MAX)} - V_{Z(MIN)}]^2}{R_{LIM}}$$

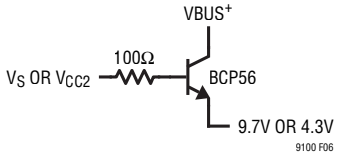

Figure 6. NPN Buffer Relieves R_{LIM} of Excessive Dissipation when Supplying External Loads

High Side Applications

For high side applications it is necessary to generate a voltage > V_Z volts above the bus voltage to power the LTM9100 once the FET is fully conducting; drain voltage near V_{EE}. Initially the LTM9100 can be powered directly from the bus until the FET drain drops below the minimum V_S voltage for operation. Note the V_S supply current flows through the load and will charge any load capacitance even when GATE is off. If the LTM9100 is configured to turn on the GATE upon application of bus voltage this is not an issue.

For bus voltages ≤100V the circuit of Figure 7 may be used. The step-up converter circuit provides an output voltage ~12V higher than the bus voltage, connecting to V_S through an ACL (depletion MOSFET Q1, R_{LIM}). For bus voltages >100V it is necessary to preregulate the input voltage to the step up converter, as shown in Figure 8. Any type of step up converter can be used to provide the boosted voltage: flyback, boost, charge pump, etc. Transistors Q1, Q3, and diode D1 must be selected based on the bus voltage and power dissipation.

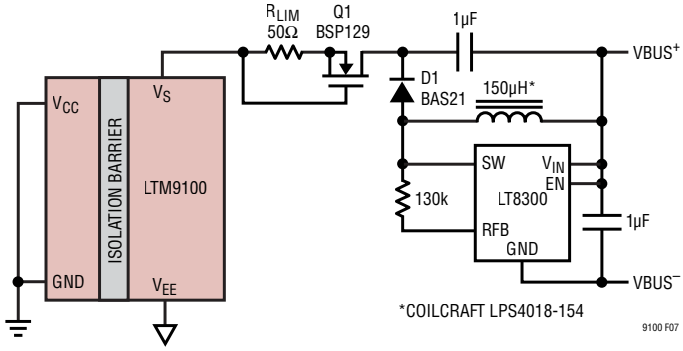

Figure 7. V_S Supply for VBUS ≤ 100V

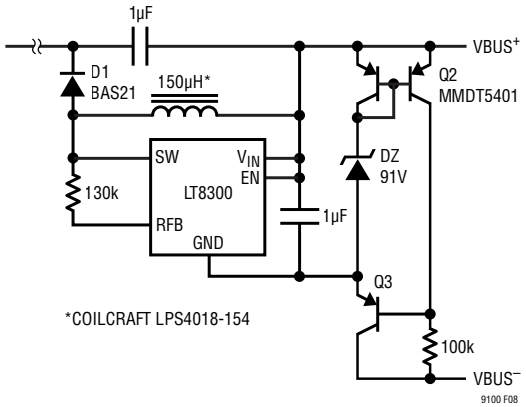

Figure 8. Preregulator for VBUS > 100V

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Switching the PowerPath™

For either low side or high side configuration, the internal DC/DC converter may be subsequently enabled and external isolated side converter disabled to minimize power dissipation. The circuit of Figure 9 uses the power good signals to automatically switch the power converter path once the main FET is on.

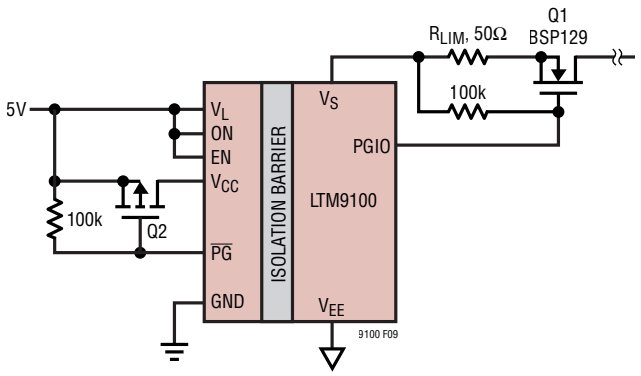

Figure 9. External-to-Internal PowerPath Switch-Over

V_L Logic Supply

A separate logic supply pin V_L allows the LTM9100 to interface with any logic signal from 3V to 5.5V as shown in Figure 10. Simply connect the desired logic supply to V_L.

There is no interdependency between V_{CC} and V_L; they may simultaneously operate at any voltage within their specified operating ranges and sequence in any order. V_{CC} and V_L are decoupled internally by 1µF capacitors.

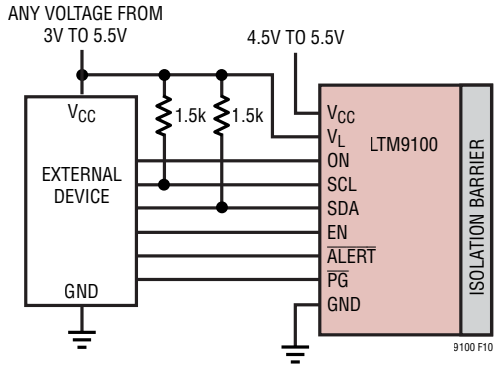

Figure 10. V_{CC} and V_L Are Independent

Hot Plugging Safely

Caution must be exercised in applications where power is plugged into the LTM9100's power supplies, V_{CC} or V_L, due to the integrated ceramic decoupling capacitors. The parasitic cable inductance along with the high-Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTM9100. Refer to Linear Technology Application Note AN88, entitled Ceramic Input Capacitors Can Cause Overvoltage Transients for a detailed discussion.

Channel Timing Uncertainty

Multiple channels are supported across the isolation boundary by encoding and decoding of the inputs and outputs. Up to three signals are assembled as a serial packet and transferred across the isolation barrier. The time required to transfer all three bits is 50ns typical, and sets the limit for how often a signal can change on the opposite side of the barrier. The technique used assigns SCL on the logic side and $\overline{PG2}$ on the isolated side the highest priority such that there is no jitter on the associated output channels, only delay. This preemptive scheme will produce a certain amount of uncertainty on the other isolation channels. The resulting pulse width uncertainty on these low priority channels is typically ±6ns, but may vary up to ±44ns if the low priority channels are not encoded within the same high priority serial packet.

Initial Start-Up and Inrush Control

Several conditions must be satisfied before the FET turn-on sequence is started. First the voltage at V_S must exceed its 9V undervoltage lockout level. Next the internal supply V_{CC2} must cross its 4.25V undervoltage lockout level. This generates a 100µs to 160µs power-on-reset pulse during which the FAULT register bits are cleared and the CONTROL register bits are set or cleared as described in the register section. After the power-on-reset pulse, the voltages at the UVH, UVL and OV pins must satisfy UVH > 2.56V, UVL > 2.291V and OV < 1.77V. All the above conditions must be satisfied throughout the duration of the start-up delay that is set by a combination of internal and external (C_{TMR}) capacitance connected to the TMR pin. C_{TMR} is charged with a pull-up current of 10µA until

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the voltage at TMR reaches 2.56V. C_{TMR} is then quickly discharged with a 12mA current. The initial delay expires when TMR is brought below 75mV. The duration of the start-up delay is given by:

$$t_D \cong 12ms + 256ms \bullet \frac{C_{TMR}}{1\mu F}$$

If any of the above conditions is violated before the start-up delay expires, C_{TMR} is quickly discharged and the turn-on sequence is restarted. After all the conditions are validated throughout the start-up delay, the EN pin is then checked. If it is high, the FET will be turned on. Otherwise, the FET will be turned on when the EN pin is raised or bit 3 (GATE_CTRL) in the CONTROL (D) register is set to 1 through the I^2C interface, when configured for I^2C only control.

The FET turn-on sequence follows by charging an internal and external (C_{SS}) capacitor at the SS pin with a 10µA pull-up current and the voltage at SS (V_{SS}) is converted to a current ($I_{GATE(UP)}$) of 11.5µA • V_{SS}/2.56V for GATE pull-up. When the GATE reaches the FET threshold voltage, current starts to flow through the FET and a current (I_{RAMP}) of 20µA • V_{SS}/2.56V flows out of the RAMP pin and through an external capacitor (C_R) connected between RAMP and the drain voltage. The SS voltage is clamped to 2.56V, which corresponds to $I_{GATE(UP)}$ = 11.5µA and I_{RAMP} = 20µA. The RAMP pin voltage is regulated at 1.1V and the ramp rate of V_{DRAIN} determines the inrush current for capacitive load:

$$I_{INRUSH} = 20\mu A \bullet \frac{C_L}{C_R}$$

The ramp rate of V_{SS} determines the di/dt of the inrush current:

$$\frac{dI_{INRUSH}}{dt} = 20\mu A \bullet \frac{C_L}{C_R} \bullet \frac{1\mu F}{256ms \bullet (C_{SS} + 220nF)}$$

If C_{SS} is absent externally, the SS ramps from 0V to 2.56V in approximately 56ms.

When V_{DRAIN} is ramped down to V_{EE}, I_{GATE} returns to the GATE pin and pulls the GATE up to V_{GATEH}. Figure 11 illustrates the start-up sequence of the LTM9100.

During live board insertion or input power step, an internal clamp turns on to hold the RAMP pin low. Resistor R_R and an internal 10nF capacitor to V_{EE} suppress noise at the RAMP pin. For proper operation, $R_R \bullet C_R$ should not exceed 50µs. Additional capacitance may be added from RAMP to V_{EE} for additional noise filtering.

Power Good Monitors

When the voltage across the FET falls below 1.77V and GATE pulls above approximately 9V, an internal power good signal is latched and a series of two delay cycles are started as shown in Figure 11. When the first delay cycle with a duration of $2t_D$ expires, the $\overline{PG2}$ and $\overline{PG}$ pins pull low as power good signals. When the second delay cycle ($2t_D$) expires, the PGIO pin pulls low as another power good signal. The $2t_D$ timer delay is obtained by charging the capacitance on TMR with a 5µA current and discharging with 12mA when TMR reaches 2.56V. The power good signals at $\overline{PG}$ and PGIO are reset in all FET turn-off conditions except the overvoltage fault.

Turn-Off Sequence and Auto-Retry

In any of the following conditions, the FET is turned off by pulling down GATE with a 110mA current, and the capacitances at SS and TMR are discharged with 12mA currents.

1. The EN (or EN2) pin is low or register bit D3 is set to 0.
2. The voltage at UVL is lower than 2.291V and the voltage at UVH is lower than 2.56V (undervoltage fault).
3. The voltage at OV is higher than 1.77V (overvoltage fault).
4. The voltage at V_S is lower than 8.5V (V_S undervoltage lockout).
5. The voltage at V_{CC2} is lower than 4.25V (V_{CC2} undervoltage lockout).
6. V_{SENSE} > 50mV and the condition lasts longer than 530µs (overcurrent fault).

For conditions 1, 4, 5, after the condition is cleared, the LTM9100 will automatically enter the FET turn-on sequence as previously described.

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For any of the fault conditions 2, 3, 6, the FET off mode is programmable by the corresponding auto-retry bit in the CONTROL register. If the auto-retry bit is set to 0, the FET is latched off upon the fault condition. If the auto-retry bit is set to 1, after the fault condition is cleared, the delay timer is started. After the timer expires, the FET enters the auto-retry mode and GATE is pulled up. The auto-retry delay following the undervoltage fault has a duration of t_D. The auto-retry delay following the overcurrent fault has a duration of $4t_D$ for extra cooling time. The auto-retry following the overvoltage fault does not have a delay. The auto-retry control bits and their defaults at power up are listed in Table 4. Note that the LTM9100 defaults to latch-off following the overcurrent fault.

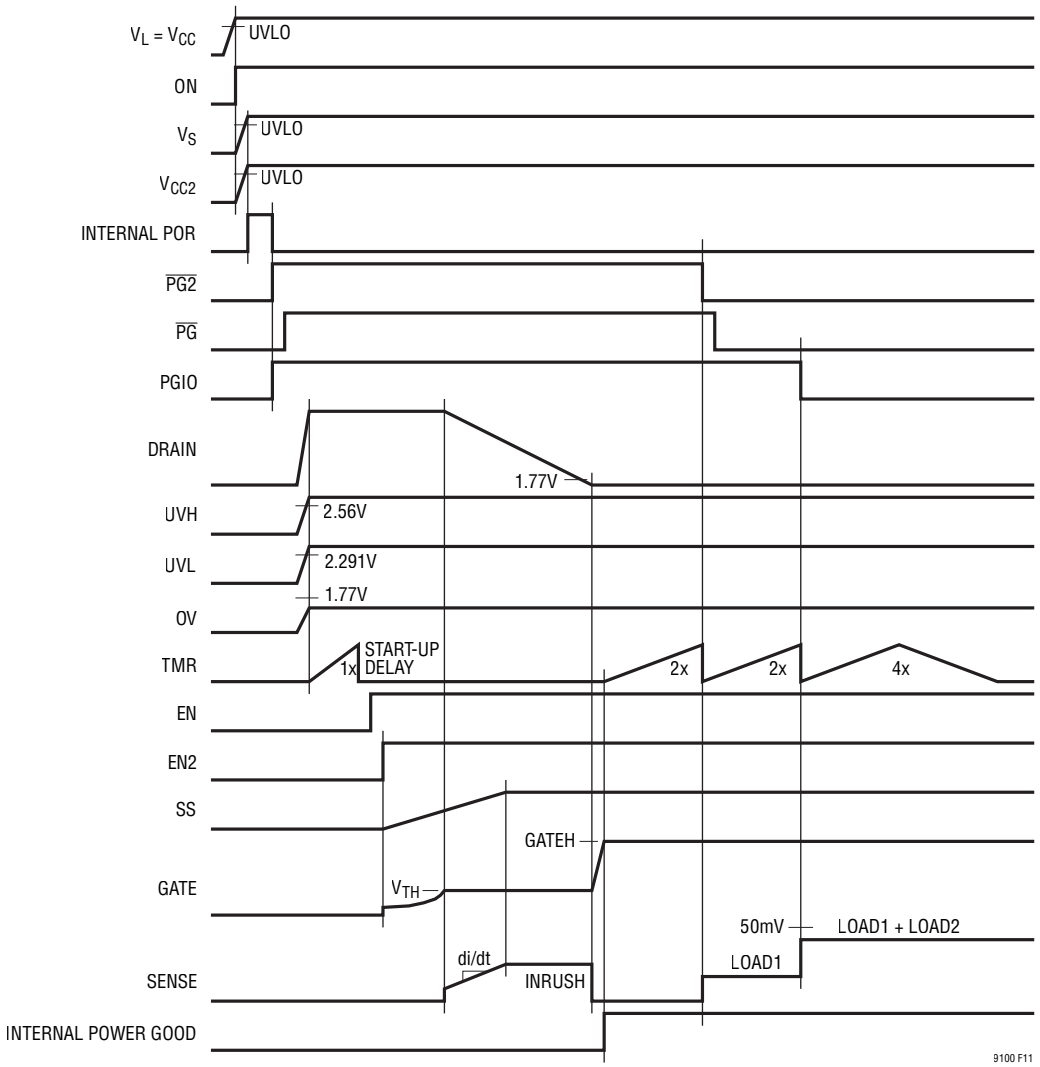

Figure 11. LTM9100 Turn-On Sequence

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Turning the GATE Pin (External FET) On

Many methods of on/off control are possible using the ON, EN, EN2, UV/OV or PGIO pins along with the I^2C port. The EN pin works well with logic inputs or floating switch contacts; I^2C control is intended for systems where the board operates only under command of a central control processor and the ON pin is useful with systems with low standby current requirements. The UV (UVH, UVL) and OV pins are useful with signals referenced to V_{EE}. PGIO controls nothing directly, but is useful for I^2C monitoring of connection sense or other important signals.

On/off control is possible with or without I^2C intervention. Even when operating autonomously, the I^2C port can still exercise control over the GATE output, although depending on how they are connected, EN, EN2, and ON could subsequently override conditions set by I^2C. UV, OV and other fault conditions seize control as needed to turn off the GATE output, regardless of the state of EN, EN2, ON or the I^2C port. Figure 12 shows five configurations of on/off control of the LTM9100.

Logic Control with Isolation: Figure 12a shows an application using logic signal control. Rising and falling edges of either the ON pin or EN pin, with alternate pin tied high, turn the GATE output on and off. Rising edge control of ON results in a delay of the GATE signal by the power converter turn-on time and one t_D period, the falling edge will also be delayed by the converter discharge time (stored energy) and supply loading on V_S and V_{CC2}. The GATE will respond immediately to changes on the EN pin. The status of EN can be examined or overridden through the I^2C port at register bit D3. Register bit D3 is set low whenever V_{CC2} drops below its UVLO threshold. The status of the GATE pin output is indicated by register bit A7 (GATE_STAT), which is equal to register bit D3 and the absence of UV, OV, and other faults.

Bootstrapped Power Connection: Figure 12b shows a low side application with control power derived on the isolated side. With EN2 tied high on the isolated side, GATE rises one t_D period after power is applied. The logic supply (V_L) or ON pin may be toggled either before or after the bus voltage is applied provided the EN pin is tied high, without interfering with the GATE signal.

Ejector Switch or Loop-Through Connection Sense: Floating switch contacts, or a connection sense loop work well with the EN or EN2 pins. Figure 12c illustrates this configuration using the EN2 pin and includes a debounce delay.

Short Pin to RTN: Figure 12d uses the UV divider string to detect board insertion. The short pin connection could also be wired to work in conjunction with either the ON or EN pins.

I^2C Only Control: To lock out EN and ON, use the configuration shown in Figure 12e and control the GATE pin with register bit D3. The circuit defaults off at power up with EN2 tied to V_{EE}. To default on, do not connect EN2. The PGIO pin can be used as an input to monitor a connection sense or other control signal. PGIO is configured as an input by setting register bits D6 and D7 high; its input state is stored at register bit A6.

Overcurrent Protection and Overcurrent Fault

The LTM9100 features two levels of protection from short-circuit and overcurrent conditions. Load current is monitored by the SENSE pins and resistor R_S. There are two distinct thresholds for the voltage at SENSE: 50mV for engaging the active current limit loop and starting a 530µs circuit breaker timer and 250mV for a fast GATE pull-down to limit peak current in the event of a catastrophic short-circuit or an input step.

In an overcurrent condition, when the voltage drop across R_S exceeds 50mV, the current limit loop is engaged and an internal 530µs circuit breaker timer is started. The current limit loop servos the GATE to maintain a constant output current of $50mV/R_S$. When the circuit breaker timer expires, the FET is turned off by pulling GATE down with a 110mA current, the capacitors at SS and TMR are discharged and the power good signals are reset. At this time, the overcurrent present bit A2 and the overcurrent fault bit B2 are set, and the circuit breaker timer is reset.

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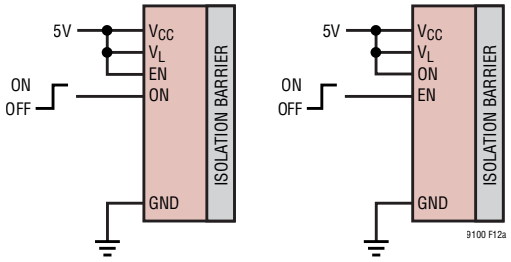
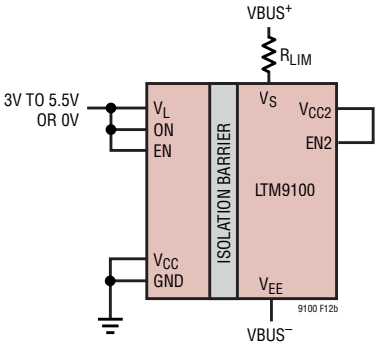
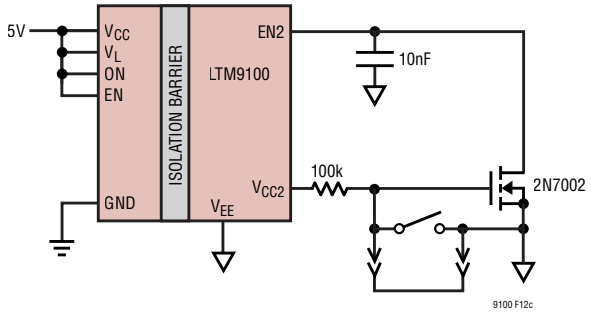


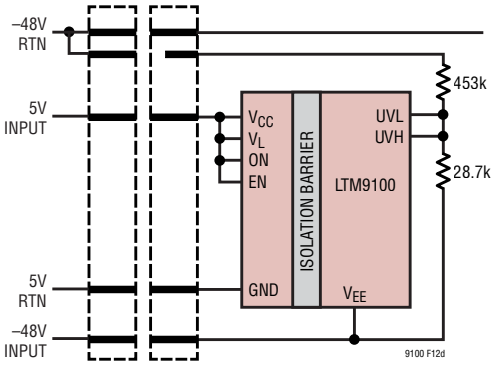
12(a) Logic Input Control



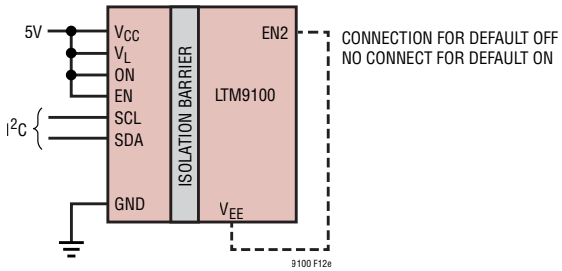
12(b) Bootstrapped Power Connection



12(c) Contact Debounce Delay Upon Insertion for Use with an Ejector Switch or Loop-Through Style Connection Sense



12(d) Short Pin Connection Sense to RTN



12(e) I²C Only Control

Figure 12. On/Off Control of the LTM9100

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After the FET is turned off, the overcurrent condition register bit A2 is cleared. If the overcurrent auto-retry register bit D2 has been set, the switch will turn on again automatically after a cooling time of $4t_D$. Otherwise, the FET will remain off until the overcurrent fault register bit B2 is reset. When the overcurrent fault bit is reset (see Resetting Faults), the FET is allowed to turn on again after a delay of $4t_D$. The $4t_D$ cooling time associated with the overcurrent fault will not be interrupted by any other fault condition. See Figure 13 for operation of LTM9100 under overcurrent condition followed by auto-retry.

In the case of a low impedance short-circuit on the load side or an input step during battery replacement, current overshoot is inevitable. A fast SENSE comparator with a threshold of 250mV detects the overshoot and immediately pulls GATE low. Once the SENSE voltage drops to 50mV, the current limit loop takes over and servos the current as previously described. If the short-circuit condition lasts longer than 530µs, the FET is shut down and the overcurrent fault is registered.

In the case of an input step, after an internal clamp pulls the RAMP pin down to 1.1V, the inrush control circuit takes over and the current limit loop is disengaged before the circuit breaker timer expires. From this point on, the device works as in the initial start-up: V_{DRAIN} is ramped down at the rate set by I_{RAMP} and C_R followed by GATE pull-up. The power good signals on the $\overline{PG}$ and PGIO pins, the TMR pin, and the SS pin are not interrupted through the input step sequence. The waveform in Figure 14 shows how the LTM9100 responds to an input step.

Note that the current limit threshold should be set sufficiently high to accommodate the sum of the load current and the inrush current to avoid engagement of the current limit loop in the event of an input step. The maximum value of the inrush current is given by:

$$I_{INRUSH} \le 0.8 \bullet \frac{45mV}{R_S} - I_{LOAD}$$

where the 0.8 factor is used as a worst-case margin combined with the minimum SENSE threshold (45mV).

The active current limit circuit is compensated using the capacitor C_G with a series resistor R_G (10Ω) connected between GATE and V_{EE}, as shown in Figure 4. The suggested value for C_G is 47nF. This value should work for most FETs (Q1).

Overvoltage Fault

An overvoltage fault occurs when the OV pin rises above its 1.77V threshold. This shuts off the FET immediately, sets the overvoltage present register bit A0 and the overvoltage fault register bit B0, and pulls the SS pin down. Note that the power good signals are not affected by the overvoltage fault. If the OV pin subsequently falls back below the threshold, the FET will be allowed to turn on again immediately (without delay) unless the overvoltage auto-retry has been disabled by clearing register bit D0.

Undervoltage Comparator and Undervoltage Fault

The LTM9100 provides two undervoltage pins, UVH and UVL, for adjustable UV threshold and hysteresis. The UVH and UVL pin have the following accurate thresholds:

for UVH rising, $V_{UVH(TH)}$ = 2.56V, turn-on

for UVL falling, $V_{UVL(TH)}$ = 2.291V, turn-off

The UVH and UVL pins have a hysteresis of δV_{UV} (15mV typical). In either a rising or a falling input supply, the undervoltage comparator works in such a way that both the UVH and the UVL pins have to cross their thresholds for the comparator output to change state.

The UVH, UVL, and OV threshold ratio is designed to match the standard telecom operating range of 43V to 71V and UV hysteresis of 4.5V when UVH and UVL are tied together as in Figure 4, where the built-in UV hysteresis referred to the UVL pin is:

$$\Delta V_{UV(HYST)} = V_{UVH(TH)} - V_{UVL(TH)} = 0.269V$$

Using R1 = 11.8k, R2 = 16.9k and R3 = 453k as in Figure 4 gives a typical operating range of 43.0V to 70.7V, with an undervoltage shutdown threshold of 38.5V and an overvoltage shutdown threshold of 72.3V.

The UV hysteresis can be adjusted by separating the UVH and UVL pins with a resistor R_H (Figure 15). To increase the UV hysteresis, the UVL tap should be placed above the UVH tap as in Figure 15a. To reduce the UV hysteresis,