



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



SmartMesh IP Network Manager 2.4GHz 802.15.4e Wireless Embedded Manager

NETWORK FEATURES

- Complete **Radio Transceiver, Embedded Processor,** and **Networking Software** for Forming a Self-Healing Mesh Network
- SmartMesh® Networks Incorporate:
 - Time Synchronized Network-Wide Scheduling
 - Per Transmission Frequency Hopping
 - Redundant Spatially Diverse Topologies
 - Network-Wide Reliability and Power Optimization
 - NIST Certified Security
- SmartMesh Networks Deliver:
 - >99.999% Network Reliability Achieved in the Most Challenging RF Environments
 - Sub 50µA Routing Nodes
- Compliant to 6LoWPAN Internet Protocol (IP) and IEEE 802.15.4e Standards

LTP5901/2-IPR FEATURES

- Manages Networks of Up to 100 Nodes
- Sub 1mA Average Current Consumption Enables Battery Powered Network Management
- RF Modular Certification Include USA, Canada, EU, Japan, Taiwan, Korea, India, Australia and New Zealand
- PCB Assembly with Chip Antenna (LTP5901-IPR) or with MMCX Antenna Connector (LTP5902-IPR)

DESCRIPTION

SmartMesh IP™ wireless sensor networks are self managing, low power internet protocol (IP) networks built from wireless nodes called motes. The [LTP™5901-IPR/LTP5902-IPR](#) is the IP manager product in the Eterna®* family of IEEE 802.15.4e printed circuit board assembly solutions, featuring a highly integrated, low power radio design by Dust Networks® as well as an ARM Cortex-M3 32-bit microprocessor running Dust's embedded SmartMesh IP networking software.

Based on the IETF 6LoWPAN and IEEE-802.15.4e standards, the LTP5901/2-IPR runs SmartMesh IP network management software to monitor and manage network performance and provide a data ingress/egress point via a UART interface. The SmartMesh IP software provided with the LTP5901/2-IPR is fully tested and validated, and is readily configured via a software application programming interface. With Dust's time-synchronized SmartMesh IP networks, all motes in the network may route, source or terminate data, while providing many years of battery powered operation.

SmartMesh IP motes deliver a highly flexible network with proven reliability and low power performance in an easy-to-integrate platform.

LT, LT, LTC, LTM, Linear Technology, Dust, Dust Networks, Eterna, SmartMesh and the Linear logo are registered trademarks and LTP, SmartMesh IP and the Dust Networks logo are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents, including 7375594, 7420980, 7529217, 7791419, 7881239, 7898322, 8222965.

* Eterna is Dust Networks' low power radio SoC architecture.

TYPICAL APPLICATION

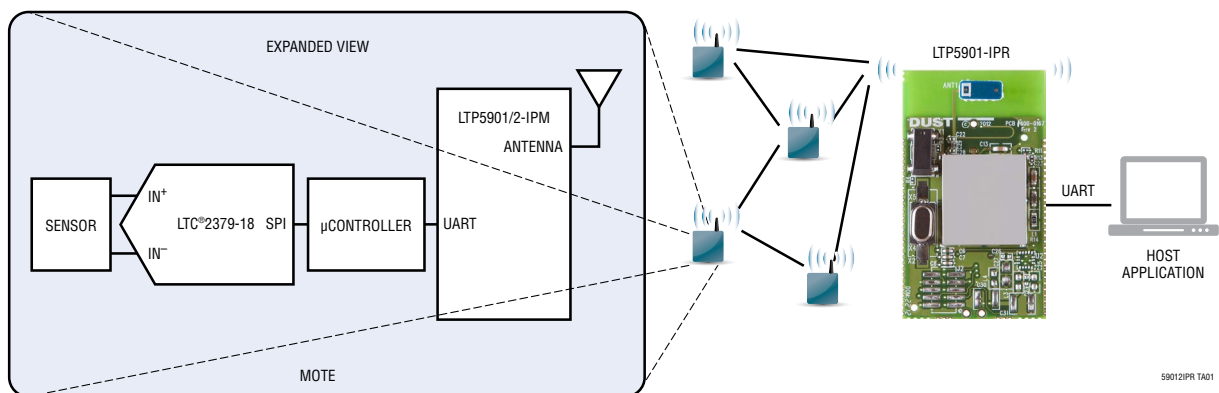


TABLE OF CONTENTS

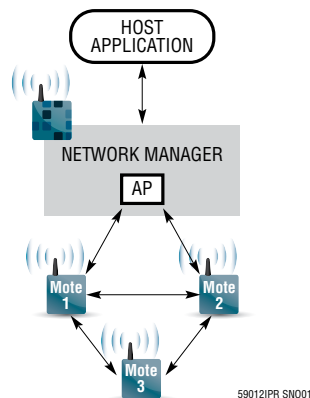
Network Features	1	Operation	22
LTP5901/2-IPR Features	1	Power Supply.....	23
Typical Application	1	Supply Monitoring and Reset	23
Description	1	Precision Timing.....	23
SmartMesh Network Overview	3	Application Time Synchronization	23
Absolute Maximum Ratings	4	Time References	23
Pin Configuration	4	Radio	24
Order Information	5	UARTs.....	24
Recommended Operating Conditions	5	API UART Protocol	24
DC Characteristics	5	CLI UART	25
Radio Specifications	6	Autonomous MAC.....	25
Radio Receiver Characteristics	6	Security	25
Radio Transmitter Characteristics	7	Temperature Sensor	25
Digital I/O Characteristics	7	Radio Inhibit	25
Temperature Sensor Characteristics	7	Software Installation.....	26
System Characteristics	8	Flash Data Retention.....	26
UART AC Characteristics	8	Networking	26
Time AC Characteristics	9	Applications Information	29
Radio_INHIBIT AC Characteristics	10	Regulatory and Standards Compliance.....	29
Flash AC Characteristics	10	Soldering Information.....	29
Flash SPI Slave AC Characteristics	10	Related Documentation	30
External Bus AC Characteristics	11	Package Description	31
Typical Performance Characteristics	14	Revision History	33
Pin Functions	19	Typical Application	34
		Related Parts	34

SMARTMESH NETWORK OVERVIEW

A SmartMesh network consists of a self-forming multi-hop, mesh of nodes, known as motes, which collect and relay data, and a network manager that monitors and manages network performance and security, and exchanges data with a host application.

SmartMesh networks communicate using a time slotted channel hopping (TSCH) link layer, pioneered by Dust Networks. In a TSCH network, all motes in the network are synchronized to within less than a millisecond. Time in the network is organized into timeslots, which enables collision-free packet exchange and per-transmission channel-hopping. In a SmartMesh network, every device has one or more parents (e.g. mote 3 has motes 1 and 2 as parents) that provide redundant paths to overcome communications interruption due to interference, physical obstruction or multi-path fading. If a packet transmission fails on one path, the next retransmission may try on a different path and different RF channel.

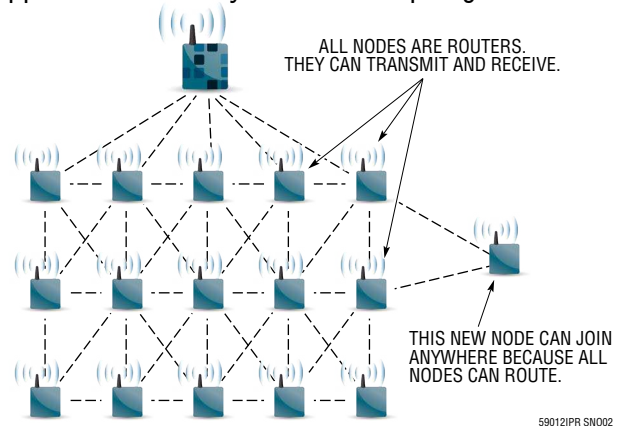
A network begins to form when the network manager instructs its onboard access point (AP) radio to begin sending advertisements—packets that contain information that enables a device to synchronize to the network and request to join. This message exchange is part of the security handshake that establishes encrypted communications between the manager or application, and mote. Once motes have joined the network, they maintain synchronization through time corrections when a packet is acknowledged.



An ongoing discovery process ensures that the network continually discovers new paths as the RF conditions change. In addition, each mote in the network tracks performance statistics (e.g. quality of used paths, and lists of potential paths) and periodically sends that information

to the network manager in packets called health reports. The network manager uses health reports to continually optimize the network to maintain >99.999% data reliability even in the most challenging RF environments.

The use of TSCH allows SmartMesh devices to sleep in-between scheduled communications and draw very little power in this state. Motes are only active in timeslots where they are scheduled to transmit or receive, typically resulting in a duty cycle of < 1%. The optimization software in the network manager coordinates this schedule automatically. When combined with the Eterna low power radio, every mote in a SmartMesh network—even busy routing ones—can run on batteries for years. By default, all motes in a network are capable of routing traffic from other motes, which simplifies installation by avoiding the complexity of having distinct routers vs non-routing end nodes. Motes may be configured as non-routing to further reduce that particular mote's power consumption and to support a wide variety of network topologies.



At the heart of SmartMesh motes and network managers is the Eterna IEEE 802.15.4e System-on-Chip (SoC), featuring Dust Networks' highly integrated, low power radio design, plus an ARM Cortex-M3 32-bit microprocessor running SmartMesh networking software. The SmartMesh networking software comes fully compiled yet is configurable via a rich set of application programming interfaces (APIs) which allows a host application to interact with the network, e.g. to transfer information to a device, to configure data publishing rates on one or more motes, or to monitor network state or performance metrics. Data publishing can be uniform or different for each device, with motes being able to publish infrequently or faster than once per second as needed.

59012iprfa

LTP5901-IPR/LTP5902-IPR

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage on VSUPPLY	4.20V
Input Voltage on AI_0/1/2/3 Inputs.....	1.98V
Voltage on Any Digital I/O Pin	-0.3V to VSUPPLY + 0.3V
Input RF Level	10dBm
Storage Temperature Range (Note 3).....	-55°C to 105°C

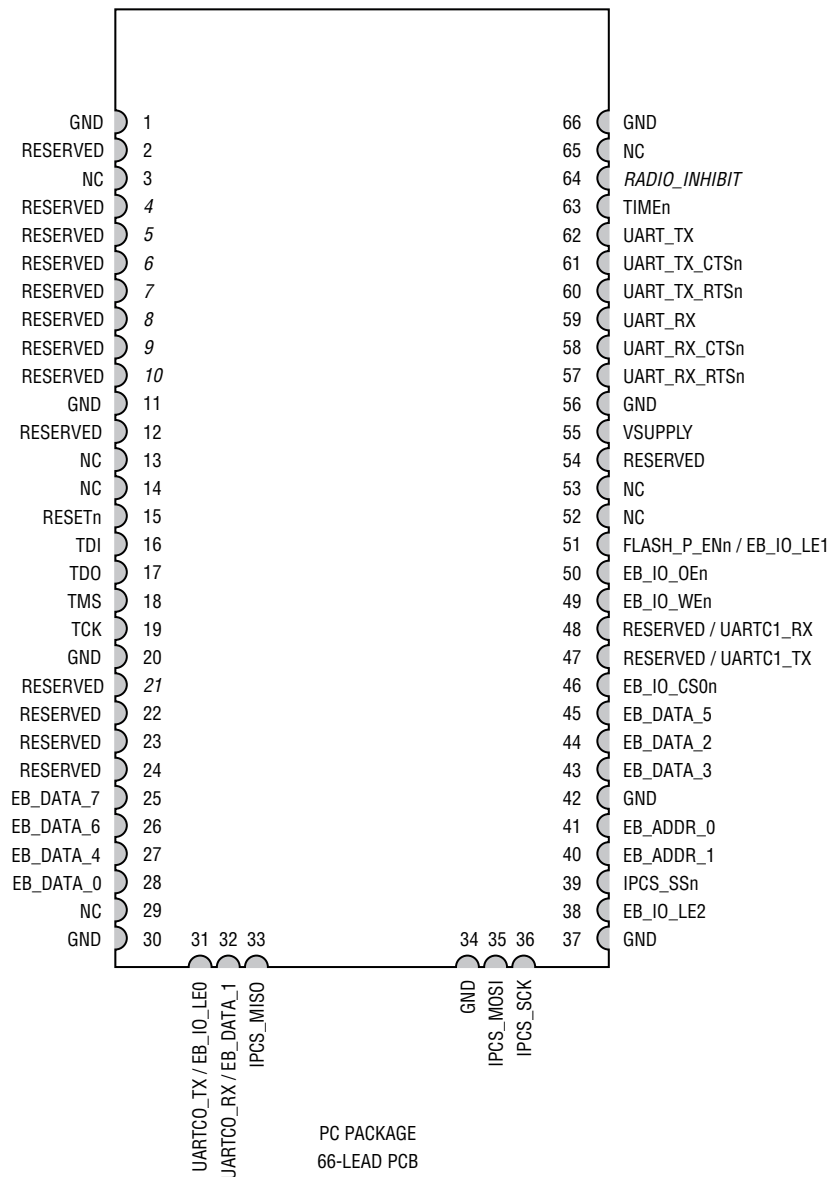
Operating Temperature Range

LTP5901I/LPT5902I	-40°C to 85°C
-------------------------	---------------

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LTP5901/LTP5902-IPR.

PIN CONFIGURATION

Pin functions shown in *italics* are currently not supported in software.



59012iprfa

ORDER INFORMATION

LEAD FREE FINISH†	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTP5901IPC-IPMA#PBF	LTP5901IPC-IPMA#PBF	66-Lead (42mm × 24mm × 5.5mm) PCB with Chip Antenna	-40°C to 85°C
LTP5902IPC-IPMA#PBF	LTP5902IPC-IPMA#PBF	66-Lead (37.5mm × 24mm × 5.5mm) PCB with MMCX Connector	-40°C to 85°C

†This product ships with the flash erased at the time of order. OEMs will need to program devices during development and manufacturing. For legacy part numbers and ordering information go to: www.linear.com/ltp5901-ipr#orderinfo or www.linear.com/ltp5902-ipr#orderinfo

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

*The temperature grade is identified by a label on the shipping container.

RECOMMENDED OPERATING CONDITIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VSUPPLY	Supply Voltage	Including Noise and Load Regulation	● 2.1		3.76	V
	Supply Noise	50Hz to 2MHz	●		250	mV
	Operating Relative Humidity	Non-Condensing	● 10		90	% RH
	Temperature Ramp Rate While Operating in Network		● -8		8	°C/min

DC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted.

OPERATION/STATE	CONDITIONS	MIN	TYP	MAX	UNITS
Power-On Reset	During Power-On Reset, Maximum 750 μs + VSUPPLY Rise Time from 1V to 1.9V		12		mA
Doze	RAM on, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Active		1.2		μA
Deep Sleep	RAM on, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Inactive		0.8		μA
In-Circuit Programming	RESETn and FLASH_P_ENn Asserted, IPCS_SCK at 8MHz		20		mA
Peak Operating Current	System Operating at 14.7MHz, Radio Transmitting, During Flash Write. Maximum Duration 4.33 ms.		30		mA
			26		mA
Active	ARM Cortex-M3, RAM and Flash Operating, Radio and All Other Peripherals Off. Clock Frequency of CPU and Peripherals Set to 7.3728MHz, V _{CORE} = 1.2V		1.3		mA
Flash Write	Single Bank Flash Write		3.7		mA
Flash Erase	Single Bank Page or Mass Erase		2.5		mA
Radio Tx	Current with Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.		5.4		mA
			9.7		mA
Radio Rx	Current with Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.		4.5		mA

LTP5901-IPR/LTP5902-IPR

RADIO SPECIFICATIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Band		●	2.4000		2.4835	GHz
Number of Channels		●		15		
Channel Separation		●		5		MHz
Channel Center Frequency	Where $k = 11$ to 25 , as Defined by IEEE.802.15.4	●		$2405 + 5 \cdot (k-11)$		MHz
Raw Data Rate		●		250		kbps
Antenna Pin ESD Protection	HBM Per JEDEC JESD22-A114F (Note 2)			± 6000		V
Range	25°C, 50% RH, +2dBi Omni-Directional Antenna, Antenna 2m Above Ground					
Indoor				100		m
Outdoor				300		m
Free Space				1200		m

RADIO RECEIVER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Sensitivity	Packet Error Rate (PER) = 1% (Note 5)			-93		dBm
Receiver Sensitivity	PER = 50%			-95		dBm
Saturation	Maximum Input Level the Receiver Will Properly Receive Packets			0		dBm
Adjacent Channel Rejection (High Side)	Desired Signal at -82dBm, Adjacent Modulated Channel 5MHz Above the Desired Signal, PER = 1% (Note 5)			22		dBc
Adjacent Channel Rejection (Low Side)	Desired Signal at -82dBm, Adjacent Modulated Channel 5MHz Below the Desired Signal, PER = 1% (Note 5)			19		dBc
Alternate Channel Rejection (High Side)	Desired Signal at -82dBm, Alternate Modulated Channel 10MHz Above the Desired Signal, PER = 1% (Note 5)			40		dBc
Alternate Channel Rejection (Low Side)	Desired Signal at -82dBm, Alternate Modulated Channel 10MHz Below the Desired Signal, PER = 1% (Note 5)			36		dBc
Second Alternate Channel Rejection	Desired Signal at -82dBm, Second Alternate Modulated Channel Either 15MHz Above or Below, PER = 1% (Note 5)			42		dBc
Co-Channel Rejection	Desired Signal at -82dBm, Undesired Signal is an 802.15.4 Modulated Signal at the Same Frequency, PER = 1%			-6		dBc
LO Feed Through				-55		dBm
Frequency Error Tolerance (Note 6)				± 50		ppm
Symbol Error Tolerance				± 50		ppm
Received Signal Strength Indicator (RSSI) Input Range				-90 to -10		dBm
RSSI Accuracy				± 6		dB
RSSI Resolution				1		dB

59012iprfa

RADIO TRANSMITTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power High Calibrated Setting Low Calibrated Setting	Delivered to a 50Ω Load		8 0		dBm dBm
Spurious Emissions 30MHz to 1000MHz 1GHz to 12.75GHz 2.4GHz ISM Upper Band Edge (Peak) 2.4GHz ISM Upper Band Edge (Average) 2.4GHz ISM Lower Band Edge	Conducted Measurement with a 50Ω Single-Ended Load, 8dBm Output Power. All Measurements Made with Max Hold. $R_{\text{BW}} = 120\text{kHz}, V_{\text{BW}} = 100\text{Hz}$ $R_{\text{BW}} = 1\text{MHz}, V_{\text{BW}} = 3\text{MHz}$ $R_{\text{BW}} = 1\text{MHz}, V_{\text{BW}} = 3\text{MHz}$ $R_{\text{BW}} = 1\text{MHz}, V_{\text{BW}} = 10\text{Hz}$ $R_{\text{BW}} = 100\text{kHz}, V_{\text{BW}} = 100\text{kHz}$		< -70 -45 -37 -49 -45		dBm dBm dBm dBm dBc
Harmonic Emissions 2nd Harmonic 3rd Harmonic	Conducted Measurement Delivered to a 50Ω Load, Resolution Bandwidth = 1MHz, Video Bandwidth = 1MHz.		-50 -45		dBm dBm

DIGITAL I/O CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)	MIN	TYP	MAX	UNITS
V_{IL}	Low Level Input Voltage		● -0.3		0.6	V
V_{IH}	High Level Input Voltage	(Note 8)	● $V_{\text{SUPPLY}} - 0.3$		$V_{\text{SUPPLY}} + 0.3$	V
V_{OL}	Low Level Output Voltage	Type 1, $I_{\text{OL(MAX)}} = 1.2\text{mA}$	●		0.4	V
V_{OH}	High Level Output Voltage	Type 1, $I_{\text{OH(MAX)}} = -0.8\text{mA}$	● $V_{\text{SUPPLY}} - 0.3$		$V_{\text{SUPPLY}} + 0.3$	V
V_{OL}	Low Level Output Voltage	Type 2, Low Drive, $I_{\text{OL(MAX)}} = 2.2\text{mA}$	●		0.4	V
V_{OH}	High Level Output Voltage	Type 2, Low Drive, $I_{\text{OH(MAX)}} = -1.6\text{mA}$	● $V_{\text{SUPPLY}} - 0.3$		$V_{\text{SUPPLY}} + 0.3$	V
V_{OL}	Low Level Output Voltage	Type 2, High Drive, $I_{\text{OL(MAX)}} = 4.5\text{mA}$	●		0.4	V
V_{OH}	High Level Output Voltage	Type 2, High Drive, $I_{\text{OH(MAX)}} = -3.2\text{mA}$	● $V_{\text{SUPPLY}} - 0.3$		$V_{\text{SUPPLY}} + 0.3$	V
	Input Leakage Current	Input Driven to V_{SUPPLY} or GND		50		nA
	Pull-Up/Pull-Down Resistance			50		kΩ

TEMPERATURE SENSOR CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Offset	Temperature Offset Error at 25°C		±0.25		$^\circ\text{C}$
Slope Error			±0.033		$^\circ\text{C}/^\circ\text{C}$

LTP5901-IPR/LTP5902-IPR

SYSTEM CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)	MIN	TYP	MAX	UNITS
	Doze to Active State Transmit			5		μs
	Doze to Radio Tx or Rx			1.2		ms
Q_{CCA}	Charge to Sample RF Channel RSSI	Charge Consumed Starting from Doze State and Completing an RSSI Measurement		4		μC
Q_{MAX}	Largest Atomic Charge Operation	Flash Erase, 21ms Max Duration	●		200	μC
	RESETn Pulse Width		●	125		μs
	Total Capacitance	Note 12	●		6	μF
	Total Inductance	Note 12	●		3	μH
	Number of Nodes in Network (Note 12)	Without external SRAM With external SRAM	●		32 100	Motes Motes
	Network Upstream Throughput (Note 12)	Without external SRAM With external SRAM	●		24 36	Pkts/s Pkts/s

UART AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 7)	MIN	TYP	MAX	UNITS
	Permitted Rx Baud Rate Error	Both Application Programming Interface (API) and Command Line Interface (CLI) UARTs	●	-2	2	%
	Generated Tx Baud Rate Error	Both API and CLI UARTs	●	-1	1	%
$t_{\text{RX_RTS to RX_CTS}}$	Assertion of UART_RX_RTSn to Assertion of UART_RX_CTSn, or Negation of UART_RX_RTSn to Negation of UART_RX_CTSn		●	0	2	ms
$t_{\text{RX_CTS to RX}}$	Assertion of UART_RX_CTSn to Start of Byte		●	0	20	ms
$t_{\text{EOP to RX_RTS}}$	End of Packet (End of the Last Stop Bit) to Negation of UART_RX_RTSn		●	0	22	ms
$t_{\text{BEG_TX_RTS to TX_CTS}}$	Assertion of UART_TX_RTSn to Assertion of UART_TX_CTSn		●	0	22	ms
$t_{\text{END_TX_CTS to TX_RTS}}$	Negation of UART_TX_CTSn to Negation of UART_TX_RTSn			2		Bit Period
$t_{\text{TX_CTS to TX}}$	Assertion of UART_TX_CTSn to Start of Byte		●	0	2	Bit Period
$t_{\text{EOP to TX_RTS}}$	End of Packet (End of the Last Stop Bit) to Negation of UART_TX_RTSn		●	0	1	Bit Period
$t_{\text{RX_INTERBYTE}}$	Receive Inter-Byte Delay		●		100	ms
$t_{\text{RX_INTERPACKET}}$	Receive Inter-Packet Delay		●	20		ms
$t_{\text{TX_INTERPACKET}}$	Transmit Inter-Packet Delay		●	1		Bit Period
$t_{\text{TX to TX_CTS}}$	Start of Byte to Negation of UART_TX_CTSn		●	0		μs

59012iprfa

UART AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

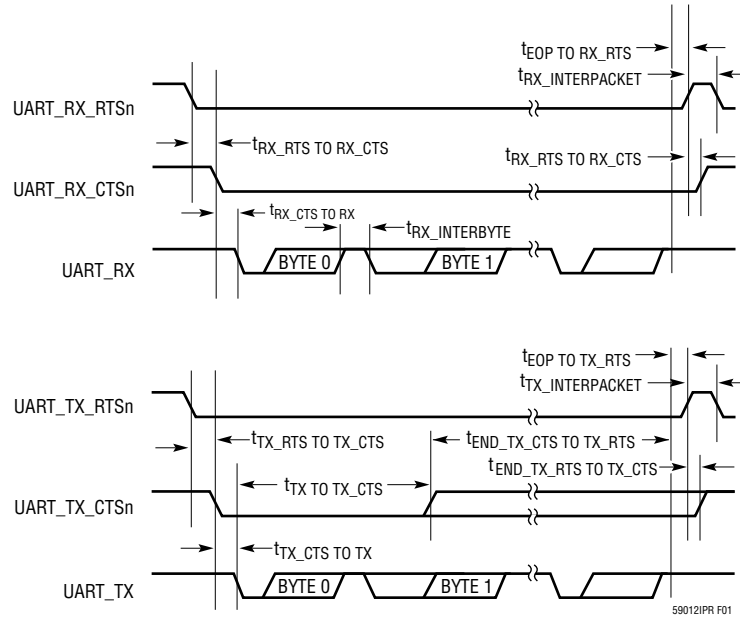


Figure 1. API UART Timing

TIME AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 7)	MIN	TYP	MAX	UNITS
t_{STROBE}	TIMEn Signal Strobe Width		●	125		μs
t_{RESPONSE}	Delay from Rising Edge of TIMEn to the Start of Time Packet on API UART		●	0	100	ms
$t_{\text{TIME_HOLD}}$	Delay from End of Time Packet on API UART to Falling Edge of Subsequent TIMEn		●	0		ns
	Timestamp Resolution (Note 9)		●	1		μs
	Network-Wide Time Accuracy (Note 10)		●	± 5		μs

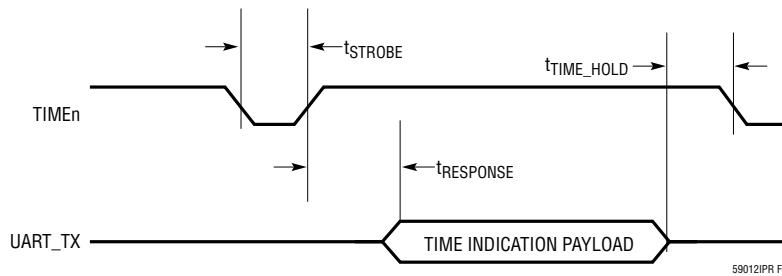


Figure 2. Timestamp Timing

RADIO_INHIBIT AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 7)	MIN	TYP	MAX	UNITS
$t_{\text{RADIO_OFF}}$	Delay from Rising Edge of RADIO_INHIBIT to Radio Disabled		●		20	ms
$t_{\text{RADIO_INHIBIT_STROBE}}$	Maximum RADIO_INHIBIT Strobe Width		●		2	s

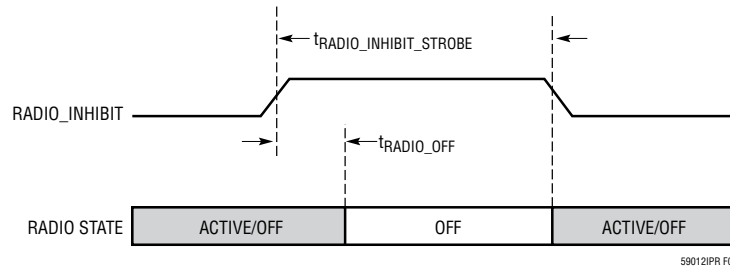


Figure 3. RADIO_INHIBIT Timing

FLASH AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 7)	MIN	TYP	MAX	UNITS
t_{WRITE}	Time to Write a 32-Bit Word (Note 11)		●		21	ms
$t_{\text{PAGE_ERASE}}$	Time to Erase a 2k Byte Page (Note 11)		●		21	ms
$t_{\text{MASS_ERASE}}$	Time to Erase 256k Byte Flash Bank (Note 11)		●		21	ms
	Data Retention	25°C 85°C 105°C			100 20 8	Years Years Years

FLASH SPI SLAVE AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 7)	MIN	TYP	MAX	UNITS
$t_{\text{FP_EN_to_RESET}}$	Setup from Assertion of FLASH_P_ENn to Assertion of RESETn		●	0		ns
$t_{\text{FP_ENTER}}$	Delay from the Assertion RESETn to the First Falling Edge of IPCS_SSn		●	125		μs
$t_{\text{FP_EXIT}}$	Delay from the Completion of the Last Flash SPI Slave Transaction to the Negation of RESETn and FLASH_P_ENn		●	10		μs
t_{SSS}	IPCS_SSn Setup to the Leading Edge of IPCS_SCK		●	15		ns
t_{SSH}	IPCS_SSn Hold from Trailing Edge of IPCS_SCK		●	15		ns
t_{CK}	IPCS_SCK Period		●	300		ns
t_{DIS}	IPCS_MOSI Data Setup		●	15		ns
t_{DIH}	IPCS_MOSI Data Hold		●	5		ns
t_{DOV}	IPCS_MISO Data Valid		●	3		ns
t_{OFF}	IPCS_MISO Data Three-State		●	0	30	ns

FLASH SPI SLAVE AC CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

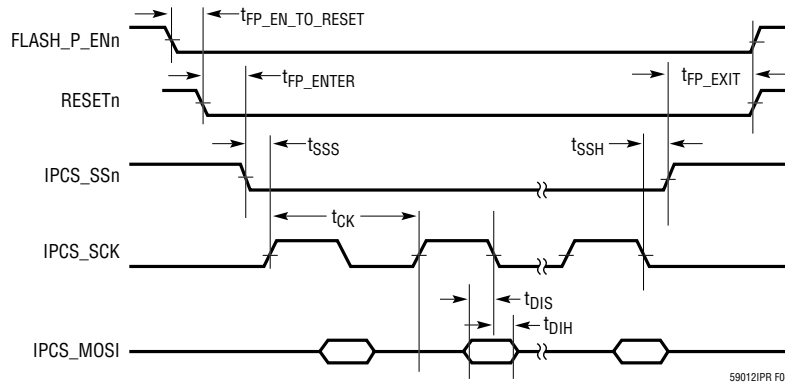


Figure 4. Flash Programming Interface Timing

EXTERNAL BUS AC CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{LEPW}	EB_IO_LE0, EB_IO_LE1, EB_IO_LE2 Pulse Width		●	100		ns
t_{AH}	EB_DATA_[7:0] Address Hold from the Rising Edge of EB_IO_LE0, EB_IO_LE1, and EB_IO_LE2	EB_DATA_[7:0] During Address Phase	●	90		ns
$t_{AV_to_DL}$	EB_ADDR_[1:0] Address Valid Until EB_DATA_[7:0] Data Latched		●	90		ns
$t_{CSn_to_OEn}$	EB_CS0n Asserted Until EB_OEn Asserted		●	150		ns
t_{CSn}	EB_CS0n Asserted		●	100		ns
$t_{SU_to_CSn}$	EB_ADDR_[1:0], EB_IO_WEn Setup to EB_CSn Asserted		●	50		ns
$t_{H_from_CSn}$	EB_ADDR_[1:0], EB_IO_WEn Hold from EB_CSn Negated		●	50		ns

EXTERNAL BUS AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

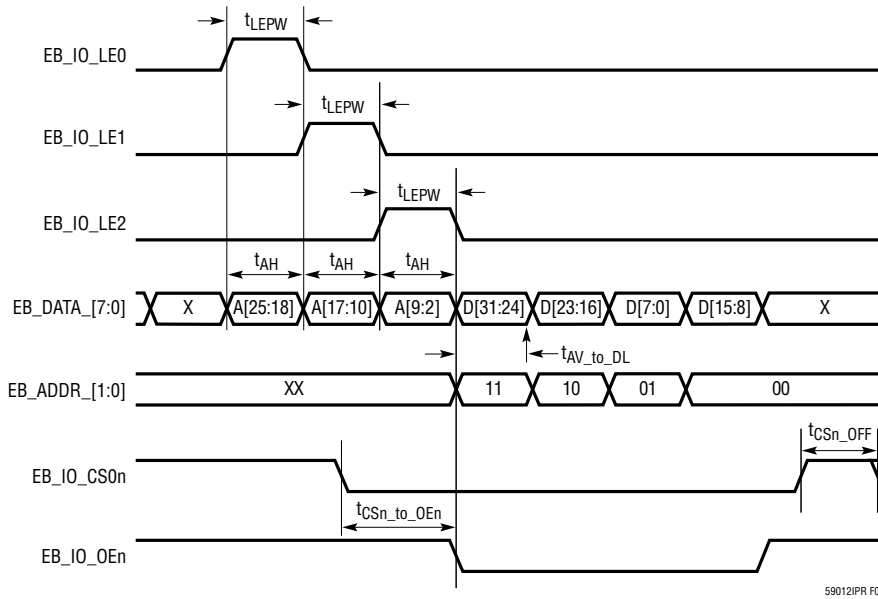


Figure 5. External Bus Read Timing

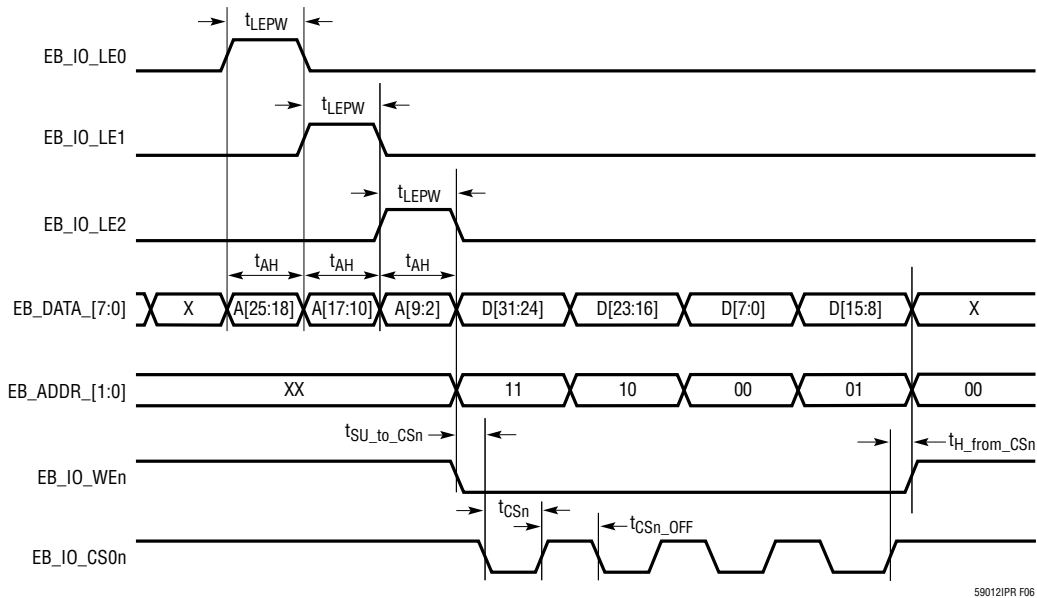


Figure 6. External Bus Write Timing

EXTERNAL BUS AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $V_{\text{SUPPLY}} = 3.6\text{V}$ unless otherwise noted. (Note 12)

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to Eterna. However, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 3: Extended storage at high temperature is discouraged, as this negatively affects the data retention of Eterna's calibration data. See FLASH Data Retention section for details.

Note 4: Actual RF range is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, and near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, range varies.

Note 5: As specified by IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low-Rate Wireless Personal Area Networks (LR-WPANS) <http://standards.ieee.org/findstds/standard/802.15.4-2011.html>.

Note 6: IEEE Std. 802.15.4-2006 requires transmitters to maintain a frequency tolerance of better than $\pm 40\text{ppm}$.

Note 7: Per pin I/O types are provided in the Pin Functions section.

Note 8: V_{IH} maximum voltage input must respect the V_{SUPPLY} maximum voltage specification.

Note 9: See the SmartMesh IP Manager API Guide for the time indication notification definition.

Note 10: Network time accuracy is a statistical measure and varies over the temperature range, reporting rate and the location of the device relative to the manager in the network. See Typical Performance Characteristics section for a more detailed description.

Note 11: Code execution from flash banks being written or erased is suspended until completion of the flash operation.

Note 12: Guaranteed by design. Not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

In mesh networks data can propagate from the manager to the nodes, downstream, or from the nodes to the manager, upstream, via a sequence of transmissions from one device to the next. As shown in Figure 8, data originating from mote P1 may propagate to the manager directly or through P2. As mote P1 may directly communicate with the manager, mote P1 is referred to as a 1-hop mote. Data originating from mote D1, must propagate through at least one other mote, P2 or P1, and as a result is referred to as a 2-hop mote. The fewest number of hops from a mote to the manager determines the hop depth.

As described in the [Application Time Synchronization](#) section, Eterna provides two mechanisms for applications to maintain a time base across a network. The synchronization performance plots that follow were generated using the more precise TIMEn input. Publishing rate is the rate a mote application sends upstream data. Synchronization improves as the publishing rate increases. Baseline synchronization performance is provided for a network operating with a publishing rate of zero. Actual performance for applications in network will improve as publishing rates increase. All synchronization testing was performed with the 1-hop mote inside a temperature chamber. Timing errors due to temperature changes and temperature differences both between the manager and this mote and between this mote and its descendents therefore propagated down through the network. The synchronization of the 3-hop and 5-hop motes to the manager was thus affected by the temperature ramps even though they were at room temperature. For 2°C/minute testing the temperature chamber was cycled between -40°C and 85°C at this rate for 24 hours. For 8°C/minute testing, the temperature chamber was rapidly cycled between 85°C and 45°C for eight hours, followed by rapid cycling between -5°C and 45°C for eight hours, and lastly, rapid cycling between -40°C and 15°C for eight hours.

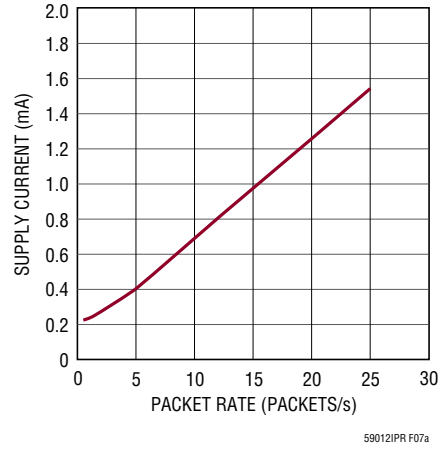


Figure 7a. Supply Current vs Packet Rate

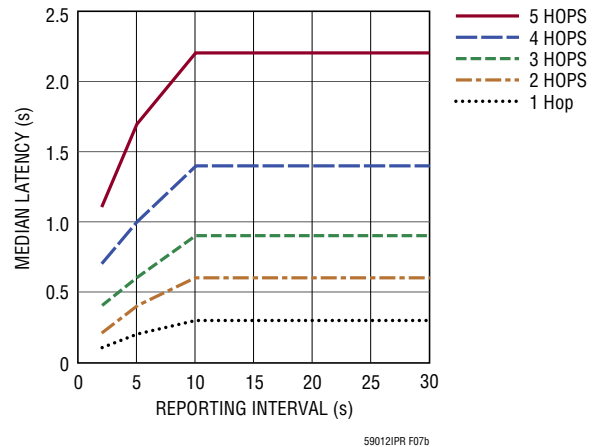


Figure 7b. Packet Latency vs Reporting Interval

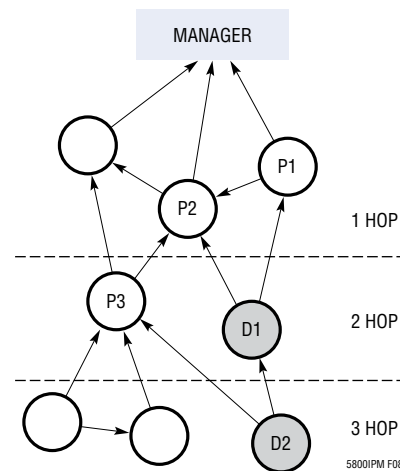
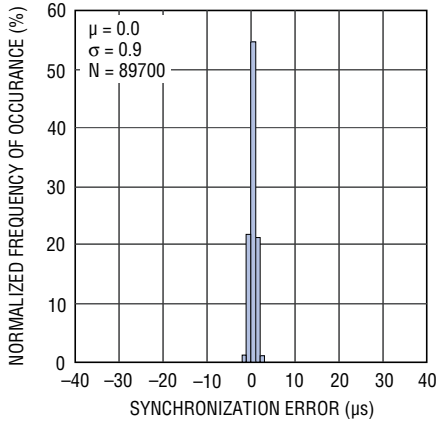


Figure 8. Example Network Graph

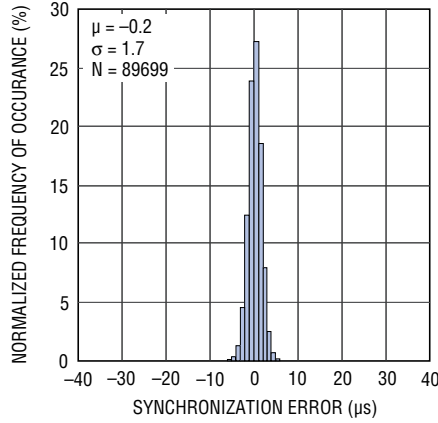
TYPICAL PERFORMANCE CHARACTERISTICS

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
1 Hop, Room Temperature



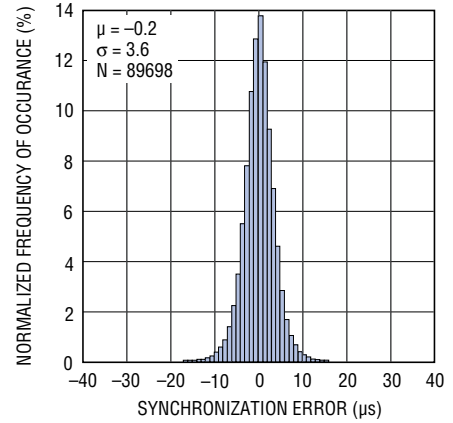
59012IPR G01

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
3 Hops, Room Temperature



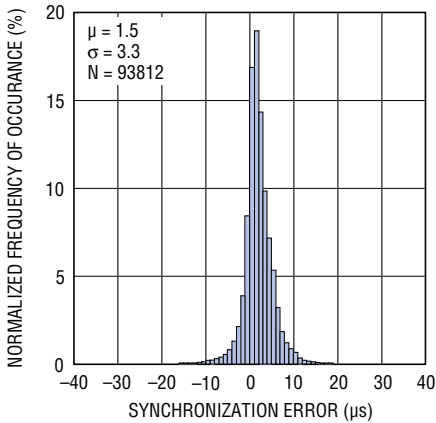
59012IPR G02

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
5 Hops, Room Temperature



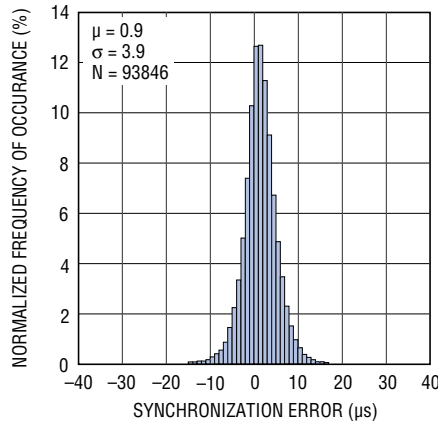
59012IPR G03

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
1 Hop, 2°C/Min.



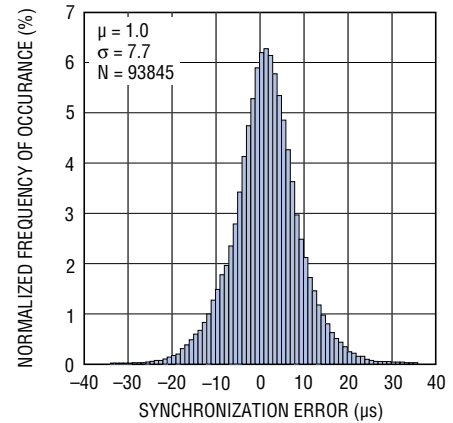
59012IPR G04

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
3 Hops, 2°C/Min.



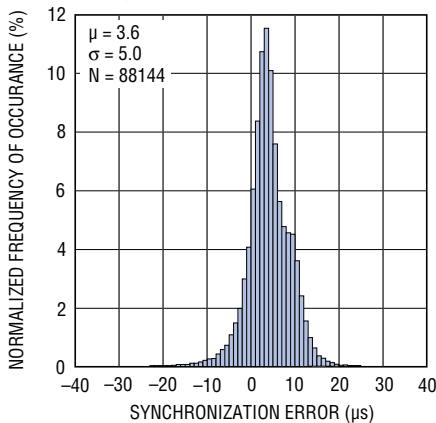
59012IPR G05

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
5 Hops, 2°C/Min.



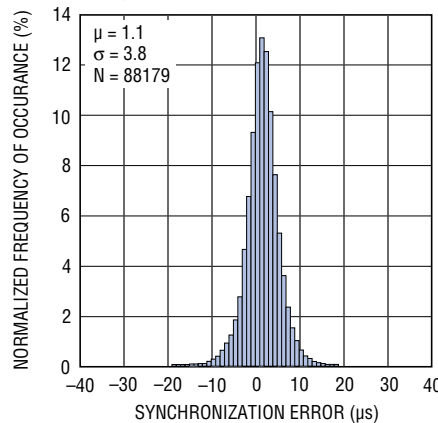
59012IPR G06

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
1 Hop, 8°C/Min.



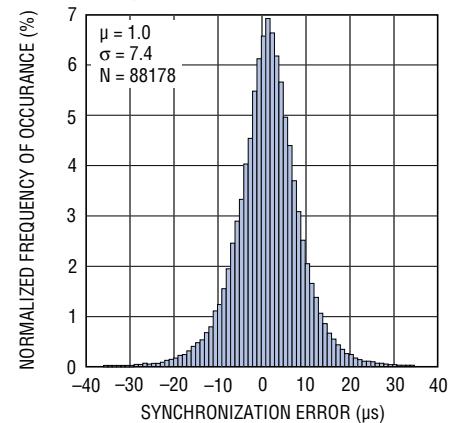
59012IPR G07

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
3 Hops, 8°C/Min.



59012IPR G08

TIMEn Synchronization Error
0 Packet/s Publishing Rate,
5 Hops, 8°C/Min.

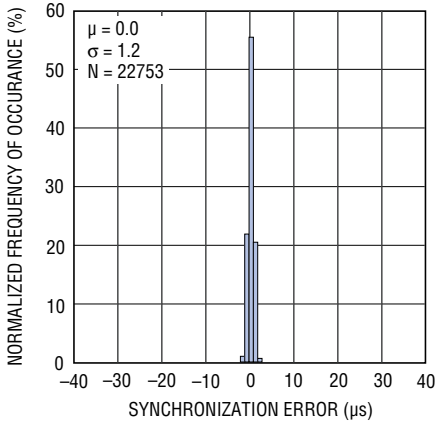


59012IPR G09

59012iprfa

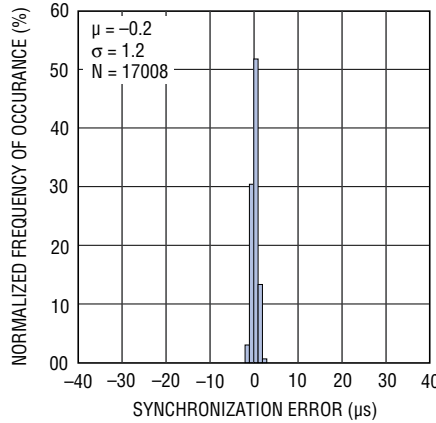
TYPICAL PERFORMANCE CHARACTERISTICS

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
1 Hop, Room Temperature**



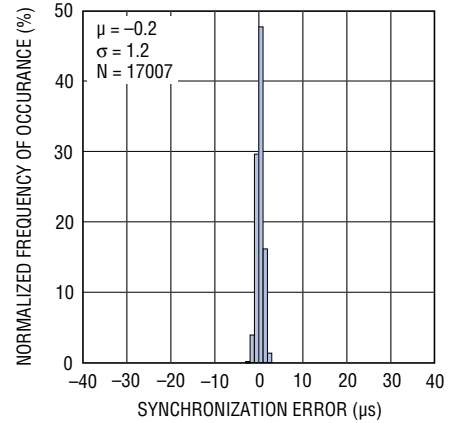
59012IPR G10

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
3 Hops, Room Temperature**



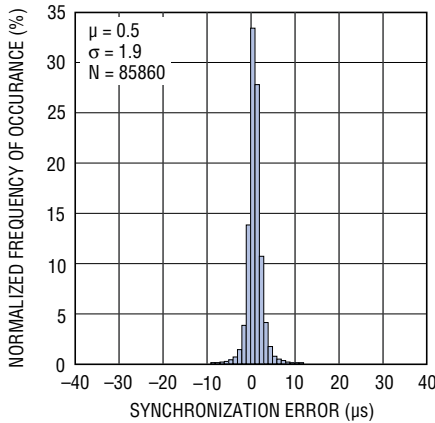
59012IPR G11

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
5 Hops, Room Temperature**



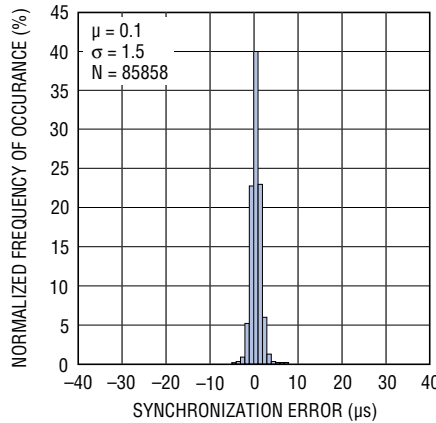
59012IPR G12

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
1 Hop, 2°C/Min.**



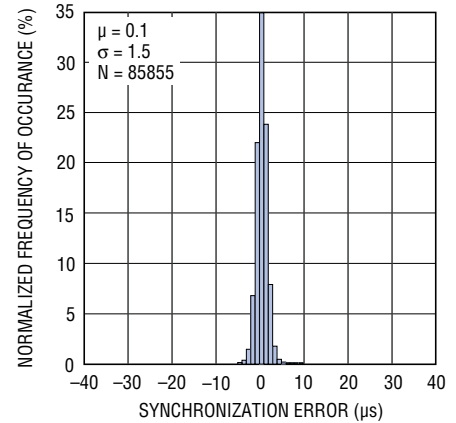
59012IPR G13

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
3 Hops, 2°C/Min.**



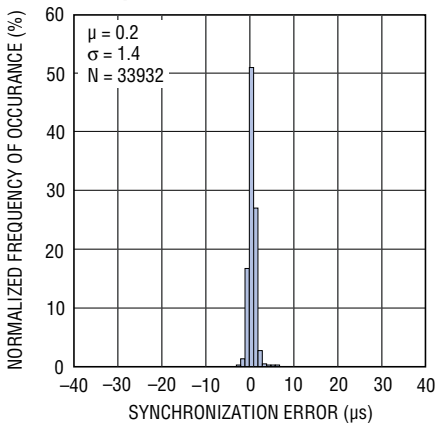
59012IPR G13

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
5 Hops, 2°C/Min.**



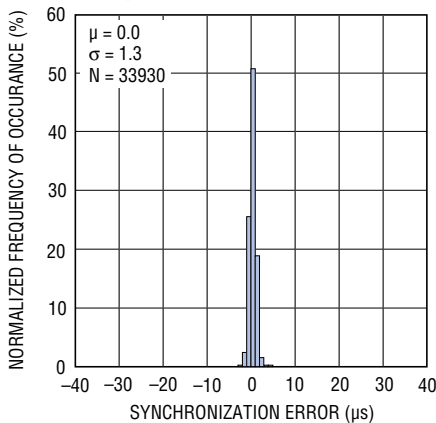
59012IPR G15

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
1 Hop, 8°C/Min.**



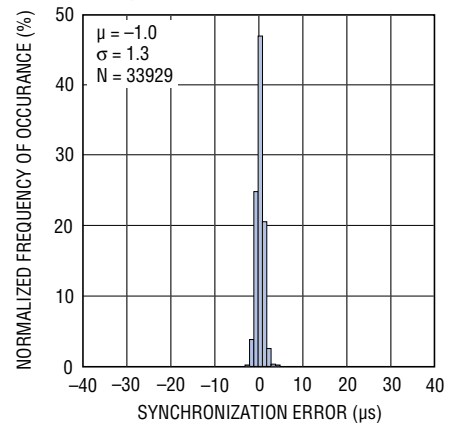
59012IPR G16

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
3 Hops, 8°C/Min.**



59012IPR G17

**TIMEn Synchronization Error
1 Packet/s Publishing Rate,
5 Hops, 8°C/Min.**



59012IPR G18

59012iprfa

TYPICAL PERFORMANCE CHARACTERISTICS

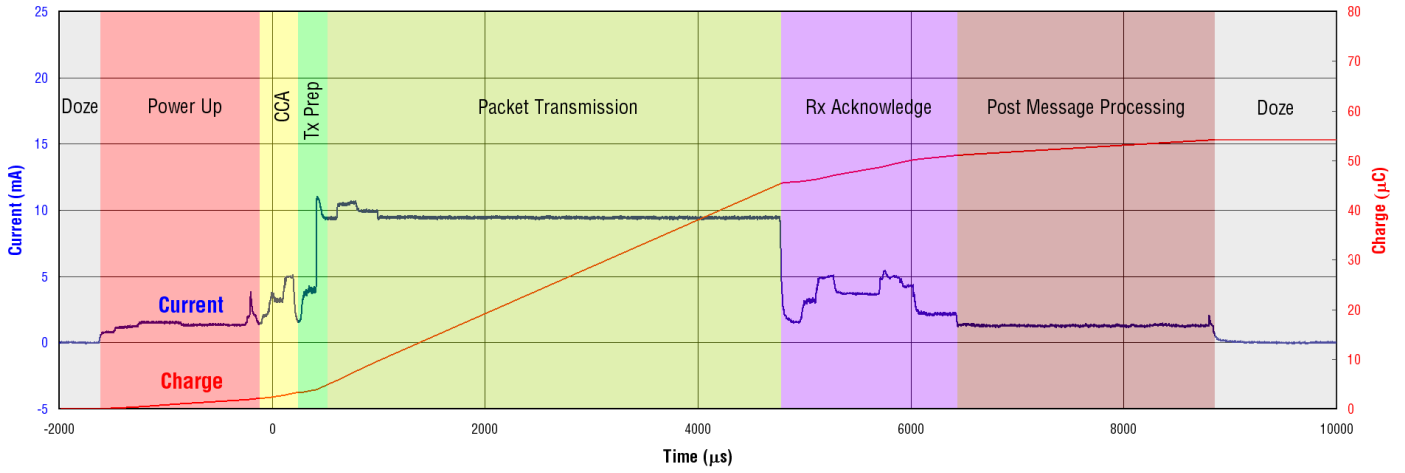
As described in the SmartMesh Network Overview section, devices in network spend the vast majority of their time inactive in their lowest power state (Doze). On a synchronous schedule a mote will wake to communicate with another mote. Regularly occurring sequences which wake, perform a significant function and return to sleep are considered atomic. These operations are considered atomic as the sequence of events can not be separated into smaller events while performing a useful function. For example, transmission of a packet over the radio is an atomic operation. Atomic operations may be characterized in either charge or energy. In a time slot where a mote successfully sends a packet, an atomic transmit includes setup prior to sending the message, sending the message, receiving the acknowledgment and the post processing needed as a result of the message being sent. Similarly in a time slot when a mote successfully receives a packet, an atomic receive includes setup prior to listening, listen-

ing until the start of the packet transition, receiving the packet, sending the acknowledge and the post processing required due to the arrival of the packet.

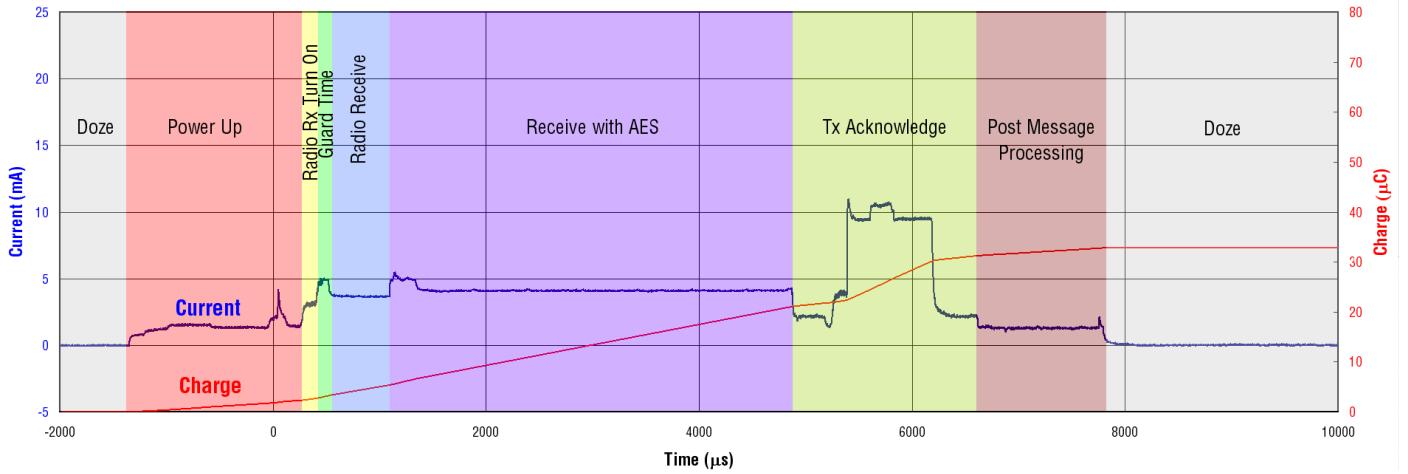
To ensure reliability each mote in the network is provided multiple time slots for each packet it nominally will send and forward. The time slots are assigned to communicate upstream with at least two different motes. When combined with frequency hopping this provides temporal, spatial and spectral redundancy. Given this approach a mote will often listen for a message that it will never receive, since the time slot is not being used by the transmitting mote. It has already successfully transmitted the packet. Since typically three timeslots are scheduled for every one packet to be sent or forwarded, motes will perform more of these atomic idle listens than atomic transmit or atomic receive sequences. Examples of transmit, receive and idle listen atomic operations are shown below.

TYPICAL PERFORMANCE CHARACTERISTICS

Atomic Operation—Maximum Length Transmit with Acknowledge, 7.25ms Time Slot (54.5 μ C Total Charge at 3.6V)



Atomic Operation—Maximum Length Receive with Acknowledge, 7.25ms Time Slot (32.6 μ C Total Charge at 3.6V)



Atomic Operation—Idle Listen, 7.25ms Time Slot (6.4 μ C Total Charge at 3.6V)

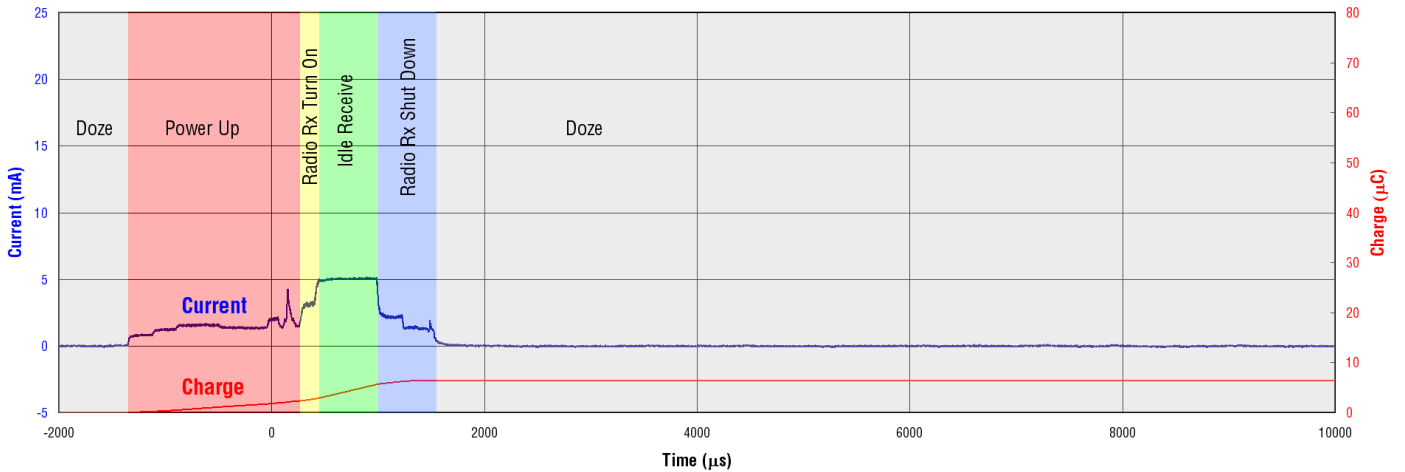


Figure 9.

PIN FUNCTIONS

Pin functions shown in italics are currently not supported in software.

The following table organizes the pins by functional groups. For those I/O with multiple functions the alternate functions are shown on the second and third line in their respective row. The **No** column provides the pin number. The second column lists the function. The **Type** column

lists the I/O type. The **I/O** column lists the direction of the signal relative to Eterna. The **Pull** column shows which signals have a fixed passive pull-up or pull-down. The Description column provides a brief signal description.

NO	POWER SUPPLY	TYPE	I/O	PULL	DESCRIPTION
1	GND	Power	-	-	Ground Connection
11	GND	Power	-	-	Ground Connection
20	GND	Power	-	-	Ground Connection
30	GND	Power	-	-	Ground Connection
34	GND	Power	-	-	Ground Connection
37	GND	Power	-	-	Ground Connection
42	GND	Power	-	-	Ground Connection
56	GND	Power	-	-	Ground Connection
66	GND	Power	-	-	Ground Connection
55	VSUPPLY	Power	-	-	Power Supply Input to Eterna

NO	RADIO	TYPE	I/O	PULL	DESCRIPTION
64	<i>RADIO_INHIBIT</i>	1 (Note 13)			<i>Radio Inhibit</i>
4	<i>GPIO17</i>	1	I/O	-	<i>General Purpose Digital I/O</i>
5	<i>GPIO18</i>	1	I/O	-	<i>General Purpose Digital I/O</i>
6	<i>GPIO19</i>	1	I/O	-	<i>General Purpose Digital I/O</i>
-	ANTENNA	N/A	N/A	-	Chip Antenna (LTP5901) or MMCX Connector (LPT5902)

NO	ANALOG	TYPE	I/O	PULL	DESCRIPTION
7	<i>AI_2</i>	Analog	I	-	Analog Input 2
8	<i>AI_1</i>	Analog	I	-	Analog Input 1
9	<i>AI_3</i>	Analog	I	-	Analog Input 3
10	<i>AI_0</i>	Analog	I	-	Analog Input 0

NO	RESET	TYPE	I/O	PULL	DESCRIPTION
15	RESETn	1	I	UP	Reset Input, Active Low

NO	JTAG	TYPE	I/O	PULL	DESCRIPTION
16	TDI	1	I	UP	JTAG Test Data In
17	TDO	1	O	-	JTAG Test Data Out
18	TMS	1	I	UP	JTAG Test Mode Select
19	TCK	1	I	DOWN	JTAG Test Clock

LTP5901-IPR/LTP5902-IPR

PIN FUNCTIONS Pin functions shown in italics are currently not supported in software.

NO	SPECIAL PURPOSE	TYPE	I/O	PULL	DESCRIPTION
63	TIMEn	1 (Note 13)	I	-	Time Capture Request, Active Low

NO	CLI AND EXTERNAL MEMORY	TYPE	I/O	PULL	DESCRIPTION
25	EB_DATA_7	1	I/O	-	External Bus Data Bit 7
26	EB_DATA_6	1	I/O	-	External Bus Data Bit 6
27	EB_DATA_4	1	I/O	-	External Bus Data Bit 4
28	EB_DATA_0	1	I/O	-	External Bus Data Bit 0
31	UART0_TX EB_IO_LE0	2	0 0	-	CLI UART 0 Transmit External Bus I/O Latch Enable 0 for External Address Bits A[25:18]
32	UART0_RX EB_DATA_1	1	I I/O	-	CLI UART 0 Receive External Bus Data Bit 1
38	EB_IO_LE2	1	0	-	External Bus I/O Latch Enable 2 for External Address Bits A[9:2]
40	EB_ADDR_1	2	0	-	External Bus Address Bit 1
41	EB_ADDR_0	2	0	-	External Bus Address Bit 0
43	EB_DATA_3	1	I/O	-	External Bus Data Bit 3
44	EB_DATA_2	1	I/O	-	External Bus Data Bit 2
45	EB_DATA_5	1	I/O	-	External Bus Data Bit 5
46	EB_IO_CS0n	2	0	-	External Bus Chip Select 0
47	UART1_TX	2	0	-	CLI UART 1 Transmit
48	UART1_RX	1	I	-	CLI UART 1 Receive
49	EB_IO_WEn	2	0	-	External Bus Write Enable Strobe
50	EB_IO_OEn	2	0	-	External Bus Output Enable Strobe

NO	IPCS SPI/FLASH PROGRAMMING (NOTE 14)	TYPE	I/O	PULL	DESCRIPTION
33	IPCS_MISO	2	0	-	SPI Flash Emulation (MISO) Master in Slave Out Port
35	IPCS_MOSI	1	I	-	SPI Flash Emulation (MOSI) Master Out Slave in Port
36	IPCS_SCK	1	I	-	SPI Flash Emulation (SCK) Serial Clock Port
39	IPCS_SSn	1	I	-	SPI Flash Emulation Slave Select, Active Low
51	FLASH_P_ENn EB_IO_LE1	1	I 0	UP UP	Flash Program Enable, Active Low External Bus I/O Latch Enable 1

NO	API UART	TYPE	I/O	PULL	DESCRIPTION
57	UART_RX_RTSn	1 (Note 13)	I	-	UART Receive (RTS) Request to Send, Active Low
58	UART_RX_CTSn	1	0	-	UART Receive (CTS) Clear to Send, Active Low
59	UART_RX	1 (Note 13)	I	-	UART Receive
60	UART_TX_RTSn	1	0	-	UART Transmit (RTS) Request to Send, Active Low
61	UART_TX_CTSn	1 (Note 13)	I	-	UART Transmit (CTS) Clear to Send, Active Low
62	UART_TX	2	0	-	UART Transmit

Note 13: These inputs are always enabled and must be driven or pulled to a valid state to avoid leakage.

Note 14: Embedded programming over the IPCS SPI bus is only available when RESETn is asserted.

PIN FUNCTIONS

VSUPPLY: System and I/O Power Supply. Provides power to the module. The digital-interface I/O voltages are also set by this voltage.

ANTENNA: Multiplexed Receiver Input and Transmitter Output Pin. The impedance presented to the MMCX connector should be 50Ω, single-ended with respect to ground.

RESETn: The asynchronous reset signal is internally pulled up. Resetting Eterna will result in the ARM Cortex-M3 rebooting and loss of network connectivity. Use of this signal for resetting Eterna is not recommended, except during power-on and in-circuit programming.

RADIO_INHIBIT: The radio inhibit function is currently not supported by software. RADIO_INHIBIT provides a mechanism for an external device to temporarily disable radio operation. Failure to observe the timing requirements defined in the RADIO_INHIBIT AC Characteristics section, may result in unreliable network operation. In designs where the RADIO_INHIBIT function is not needed the input must either be tied, pulled or actively driven low to avoid excess leakage.

TMS, TCK, TDI, TDO: JTAG port supporting software debug and boundary scan.

SLEEPn: The SLEEPn function is not currently supported in software. The SLEEPn input must either be tied, pulled or actively driven high to avoid excess leakage.

UART_RX, UART_RX_RTSn, UART_RX_CTSn, UART_TX, UART_TX_RTSn, UART_TX_CTSn: The API UART interface includes bi-directional wake up and flow control. Unused input signals must be driven or pulled to their inactive state.

TIMEn: Strobing the TIMEn input is the most accurate method to acquire the network time maintained by Eterna. Eterna

latches the network timestamp with sub-microsecond resolution on the rising edge of the TIMEn signal and produces a packet on the API serial port containing the timing information.

UART0_RX, UART0_TX, UART1_RX, UART1_TX: The CLI UART provides a mechanism for monitoring, configuration and control of Eterna during operation. On the LTP5901/2-IPR CLI UART 0 is used when Eterna is not configured to support external RAM and CLI UART 1 is used when Eterna is configured to support external RAM. For a complete description of the supported commands see the [SmartMesh IP Manager CLI Guide](#).

EB_DATA_0 through EB_DATA_7, EB_ADDR_0, EB_ADDR_1, EB_IO_LE1 through EB_IO_LE2, EB_IO_CS0n, EB_IO_WEn, EB_IO_ENn: The external bus provides a multiplexed address data bus enabling the Cortex-M3 direct access of external byte wide RAM. The additional RAM is used by network management software enabling the support of a larger network of motes with higher packet throughput. To support the addressing needed, each latch signal, EB_IO_LE0, EB_IO_LE1, and EB_IO_LE2 will strobe to latch 8-bits of address from the EB_DATA[7:0] bus. EB_IO_LE0, EB_IO_LE1, and EB_IO_LE2 correspond to address bits [25:18], [17:10] and [9:2] respectively. EB_ADDR_0 and EB_ADDR_1 correspond to the lower two bits of address. For systems with 256k bytes or less EB_IO_LE2 can be ignored. EB_IO_CS0n, EB_IO_WEn and EB_IO_OEn provide chip select, write enable and output enable control of the external RAM.

FLASH_P_ENn, IPCS_SSn, IPCS_SCK, IPCS_MISO, IPCS_SSn: The In-circuit programming control system (IPCS) bus enables in-circuit programming of Eterna's flash memory. IPCS_SCK is a clock and should be terminated appropriately for the driving source to prevent overshoot and ringing.

OPERATION

The LTP5901/LTP5902 is the world's most energy-efficient IEEE 802.15.4 compliant platform, enabling battery and energy harvested applications. With a powerful 32-bit ARM Cortex-M3, best-in-class radio, flash, RAM and purpose-built peripherals, Eterna provides a flexible, scalable and robust networking solution for applications demanding minimal energy consumption and data reliability in even the most challenging RF environments.

Shown in Figure 10, Eterna integrates purpose-built peripherals that excel in both low operating-energy consumption and the ability to rapidly and precisely cycle between operating and low power states. Items in the gray shaded region labeled analog core correspond to the analog/RF components.

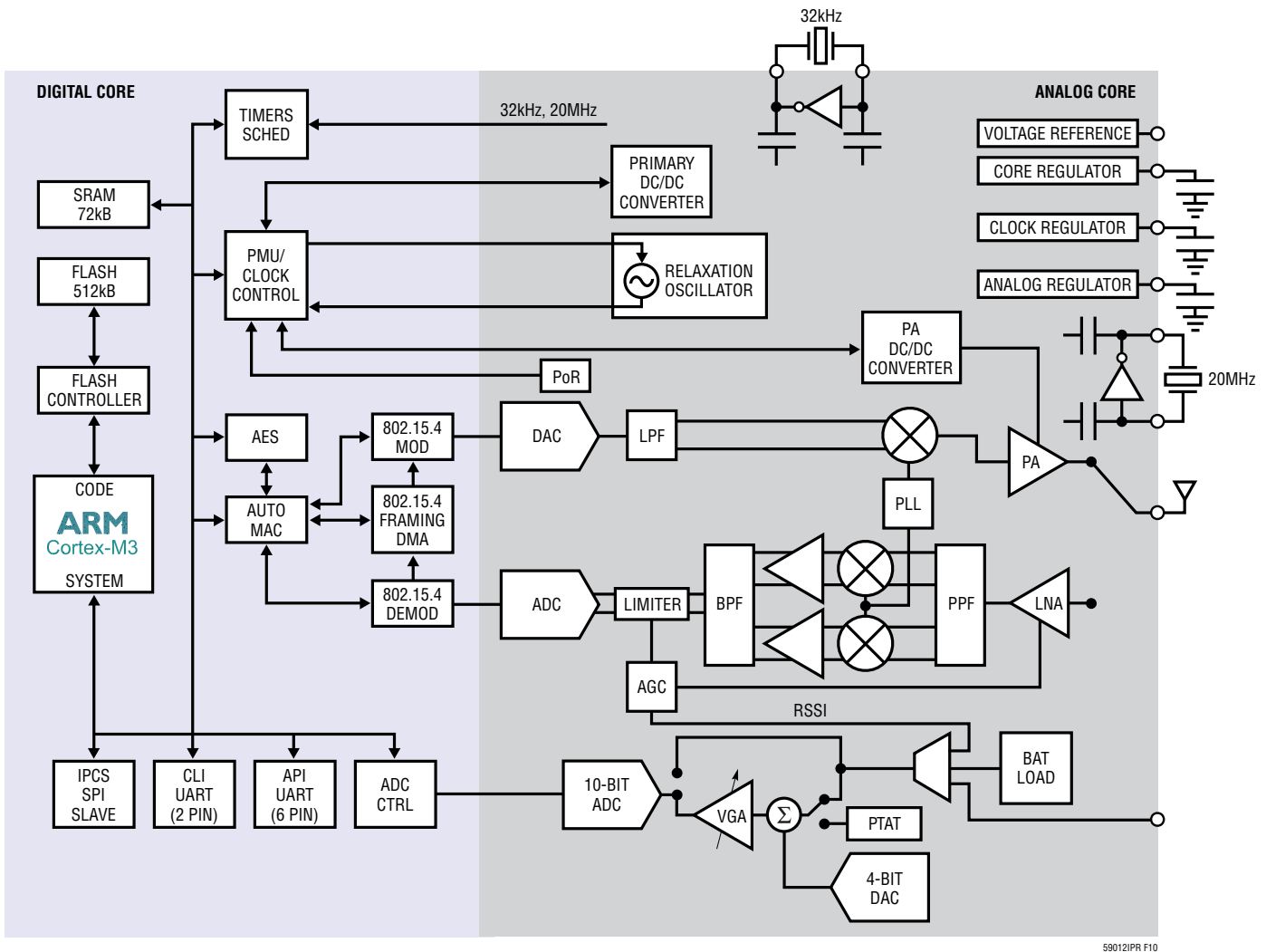


Figure 10. Eterna Block Diagram

OPERATION

POWER SUPPLY

Eterna is powered from a single pin, VSUPPLY, which powers the I/O cells and is also used to generate internal supplies. Eterna's two on-chip DC/DC converters minimize Eterna's energy consumption while the device is awake. To conserve power the DC/DC converters are disabled when the device is in low power state. Eterna's integrated power supply conditioning architecture, including the two integrated DC/DC converters and three integrated low dropout regulators, provides excellent rejection of supply noise. Eterna's operating supply voltage range is high enough to support direct connection to lithium-thionyl chloride, Li-SOCl₂, sources and wide enough to support battery operation over a broad temperature range.

SUPPLY MONITORING AND RESET

Eterna integrates a power-on reset (PoR) circuit. As the RESETn input pin is nominally configured with an internal pull-up resistor, no connection is required. For a graceful shutdown, the software and the networking layers should be cleanly halted via API commands prior to assertion of the RESETn pin. See the [SmartMesh IP Manager API Guide](#) for details on the disconnect and reset commands. Eterna includes a soft brown-out monitor that fully protects the flash from corruption in the event that power is removed while writing to flash. Integrated flash supervisory functionality, in conjunction with a fault tolerant file system, yields a robust non-volatile storage solution.

PRECISION TIMING

A major feature of Eterna over competing 802.15.4 product offerings is its low power dedicated timing hardware and timing algorithms. This functionality provides timing precision two to three orders of magnitude better than any other low power solution available at the time of publication. Improved timing accuracy allows motes to minimize the amount of radio listening time required to ensure packet reception thereby lowering even further the power consumed by SmartMesh networks. Eterna's patented timing hardware and timing algorithms provide superior performance over rapid temperature changes, further differentiating Eterna's reliability when compared

with other wireless products. In addition, precise timing enables networks to reduce spectral dead time, increasing total network throughput.

APPLICATION TIME SYNCHRONIZATION

In addition to coordinating time slots across the network, which is transparent to the user, Eterna's timing management is used to support two mechanisms to share network time. Having an accurate, shared, network-wide time base enables events to be accurately time stamped or tasks to be performed in a synchronized fashion across a network. Eterna will send a time packet through its serial interface when one of the following occurs:

- Eterna receives an API request to read time
- The TIMEn signal is asserted

The use of TIMEn has the advantage of being more accurate. The value of the timestamp is captured in hardware relative to the rising edge of TIMEn. If an API request is used, due to packet processing, the value of the timestamp may be captured several milliseconds after receipt of the packet due to packet processing. See section TIMEn AC Characteristics, for the time function's definition and specifications.

TIME REFERENCES

Eterna includes three clock sources: an internal relaxation oscillator, a low power oscillator designed for a 32.768kHz crystal, and the radio reference oscillator designed for a 20MHz crystal.

Relaxation Oscillator

The relaxation oscillator is the primary clock source for Eterna, providing the clock for the CPU, memory subsystems, and all peripherals. The internal relaxation oscillator is dynamically calibrated to 7.3728MHz. The internal relaxation oscillator typically starts up in a few μ s, providing an expedient, low energy method for duty cycling between active and low power states. Quick start-up from the doze state, defined in the State Diagram section, allows Eterna to wake up and receive data over the UART and SPI interfaces by simply detecting activity on the appropriate signals.

OPERATION

32.768kHz Crystal

Once Eterna is powered up and the 32.768kHz crystal source has begun oscillating, the 32.768kHz crystal remains operational while in the active state, and is used as the timing basis when in doze state. See the State Diagram section, for a description of Eterna's operational states.

20MHz Crystal

The 20MHz crystal source provides a frequency reference for the radio, and is automatically enabled and disabled by Eterna as needed.

RADIO

Eterna includes the lowest power commercially available 2.4GHz IEEE 802.15.4e radio by a substantial margin. (Please refer to section Radio Specifications, for power consumption numbers). Eterna's integrated power amplifier is calibrated and temperature-compensated to consistently provide power at a limit suitable for worldwide radio certifications. Additionally, Eterna uniquely includes a hardware-based autonomous MAC that handles precise sequencing of peripherals, including the transmitter, the receiver, and advanced encryption standard (AES) peripherals. The hardware-based autonomous media access controller (MAC) minimizes CPU activity, thereby further decreasing power consumption.

UARTS

The principal network interface is through the application programming interface (API) UART. A command-line interface (CLI) is also provided for support of test and debug functions. Both UARTs sense activity continuously, consuming virtually no power until data is transferred over the port and then automatically returning to their lowest power state after the conclusion of a transfer. The definition for packet encoding on the API UART interface can be found in the [SmartMesh IP Manager API Guide](#) and the CLI command definitions can be found in the [SmartMesh IP Manager CLI Guide](#).

API UART PROTOCOL

The API UART protocol was created with the goal of supporting a wide range of companion multipoint control units (MCUs) while reducing power consumption of the system. The receive half of the API UART protocol includes two additional signals in addition to UART_RX: UART_RX_RTSn and UART_RX_CTSn. The transmit half of the API UART protocol includes two additional signals in addition to UART_TX: UART_TX_RTSn and UART_TX_CTSn. The API UART protocol is referred to as Mode 4.

In the figures accompanying the protocol descriptions, signals driven by the companion processor are drawn in black and signals driven by Eterna are drawn in blue.

UART Mode 4

UART Mode 4 incorporates level-sensitive flow control on the TX channel and requires no flow control on the RX channel, supporting 115200 baud. The use of level-sensitive flow control signals enables higher data rates with the option of using a reduced set of the flow control signals; however, Mode 4 has specific limitations. First, the use of the RX flow control signals (UART_RX_RTSn and UART_RX_CTSn) for Mode 4 are optional provided the use is limited to the industrial temperature range (-40°C to 85°C); otherwise, the flow control is mandatory. If RX flow control signals are not used, UART_RX_RTSn should be tied to VSUPPLY (inactive) and UART_RX_CTSn should be left unconnected. Second, unless the companion processor is always ready to receive a packet, the companion processor must negate UART_TX_CTSn prior to the end of the current packet. Failure to negate UART_TX_CTSn prior to the end of a packet may result in back to back packets. Third, the companion processor must wait at least $t_{RX_INTERPACKET}$ between transmitting packets on UART_RX. See the [UART AC Characteristics](#) section for complete timing specifications. Packets are HDLC encoded with one stop bit and no parity bit. The flow control signals for the TX channel are shown in Figure 11. Transfers are initiated by Eterna asserting UART_TX_RTSn.

OPERATION

The UART_TX_CTSn signal may be actively driven by the companion processor when ready to receive a packet or UART_TX_CTSn may be tied low if the companion processor is always ready to receive a packet. After detecting a logic '0' on UART_TX_CTSn Eterna sends the entire packet. Following the transmission of the final byte in the packet Eterna negates UART_TX_RTSn and waits for $t_{TX_INTERPACKET}$, defined in the [UART AC Characteristics](#) section, before asserting UART_TX_RTSn again.

For details on the timing of the UART protocol, see the [UART AC Characteristics](#) section.

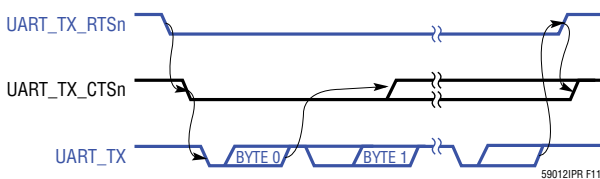


Figure 11. UART Mode 4 Transmit Flow Control

CLI UART

The command line interface (CLI) UART port is a two wire protocol (TX and RX) that operates at a fixed 9600 baud rate with one stop bit and no parity. The CLI UART interface is intended to support command line instructions and response activity.

AUTONOMOUS MAC

Eterna was designed as a system solution to provide a reliable, ultralow power, and secure network. A reliable network capable of dynamically optimizing operation over changing environments requires solutions that are far too complex to completely support through hardware acceleration alone. As described in the Precision Timing section, proper time management is essential for optimizing a solution that is both low power and reliable. To address these requirements Eterna includes the autonomous MAC, which incorporates a coprocessor for controlling all of the time-critical radio operations. The autonomous MAC provides two benefits: first, preventing variable software latency from affecting network timing and second, greatly reducing system power consumption by allowing the CPU

to remain inactive during the majority of the radio activity. The autonomous MAC, provides software-independent timing control of the radio and radio-related functions, resulting in superior reliability and exceptionally low power.

SECURITY

Network security is an often overlooked component of a complete network solution. Proper implementation of security protocols is significant in terms of both engineering effort and market value in an OEM product. Eterna system solutions provide a FIPS-197 validated encryption scheme that includes authentication and encryption at the MAC and network layers with separate keys for each mote. This not only yields end-to-end security, but if a mote is somehow compromised, communication from other motes is still secure. A mechanism for secure key exchange allows keys to be kept fresh. To prevent physical attacks, Eterna includes hardware support for electronically locking devices, thereby preventing access to Eterna's flash and RAM memory and thus the keys and code stored therein.

TEMPERATURE SENSOR

Eterna includes a calibrated temperature sensor on chip. The temperature readings are available locally through Eterna's serial API, in addition to being available via the network manager. The performance characteristics of the temperature sensor can be found in the Temperature Sensor Characteristics section.

RADIO INHIBIT

The RADIO_INHIBIT input enables an external controller to temporarily disable the radio software drivers (for example, to take a sensor reading that is susceptible to radio interference). When RADIO_INHIBIT is asserted the software radio drivers will disallow radio operations including clear channel assessment, packet transmits, or packet receipts. If the radio is active in the current time slot when RADIO_INHIBIT is asserted the radio will be disabled after the present operation completes. For details on the timing associated with RADIO_INHIBIT, see the RADIO_INHIBIT AC Characteristics section.