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SmartMesh IP Node 2.4GHz 802.15.4e Wireless Mote Module

NETWORK FEATURES

- Complete **Radio Transceiver**, **Embedded Processor**, and **Networking Software** for Forming a Self-Healing Mesh Network
- SmartMesh® Networks Incorporate:
  - Time Synchronized Network-Wide Scheduling
  - Per Transmission Frequency Hopping
  - Redundant Spatially Diverse Topologies
  - Network-Wide Reliability and Power Optimization
  - NIST Certified Security
- SmartMesh Networks Deliver:
  - >99.999% Network Reliability Achieved in the Most Challenging RF Environments
  - Sub 50µA Routing Nodes
- Compliant to 6LoWPAN Internet Protocol (IP) and IEEE 802.15.4e Standards

LTP5901-IPM/LTP5902-IPM FEATURES

- Industry-Leading Low Power Radio Technology with 4.5mA to Receive and 9.7mA to Transmit at 8dBm
- RF Modular Certification Include USA, Canada, EU, Japan, Taiwan, Korea, India, Australia and New Zealand
- PCB Assembly with Chip Antenna (LTP5901-IPM) or with MMCX Antenna Connector (LTP5902-IPM). QFN Version (LTC®5800-IPM) Available
- Micrium µCOS-II Real Time Operating System Based On-Chip Software Development Kit

DESCRIPTION

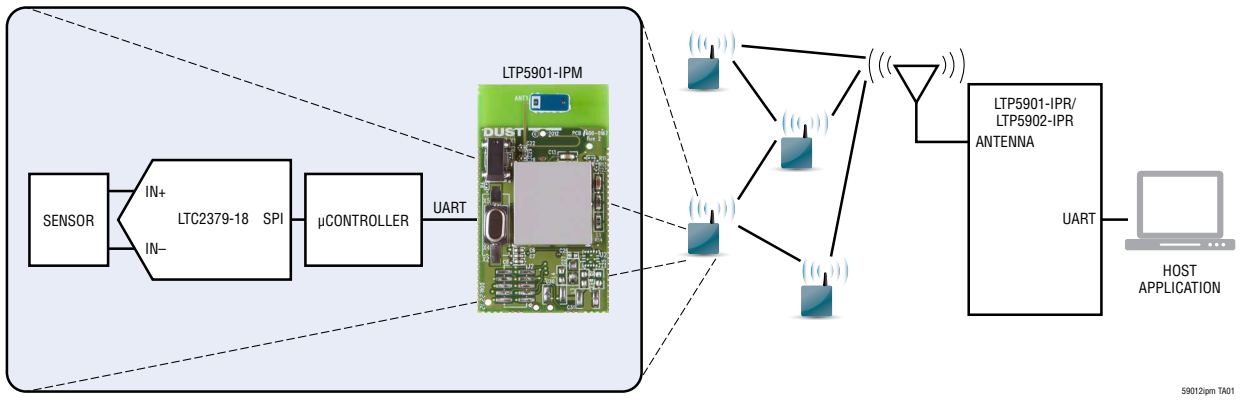
SmartMesh IP™ wireless sensor networks are self managing, low power Internet Protocol (IP) networks built from wireless nodes called motes. The LTP™5901-IPM/LTP5902-IPM is the IP mote product in the Eterna®* family of IEEE 802.15.4e printed circuit board assembly solutions, featuring a highly-integrated, low power radio design by Dust Networks® as well as an ARM Cortex-M3 32-bit microprocessor running Dust's embedded SmartMesh IP networking software. Both the LTP5901-IPM (with chip antenna), at 24mm × 42mm, and the LTP5902-IPM (with MMCX connector), at 24mm × 37mm, are designed for surface mount assembly.

With Dust's time-synchronized SmartMesh IP networks, all motes in the network may route, source or terminate data, while providing many years of battery powered operation. The SmartMesh IP software provided with the LTP5901-IPM/LTP5902-IPM is fully tested and validated, and is readily configured via a software Application Programming Interface.

SmartMesh IP motes deliver a highly flexible network with proven reliability and low power performance in an easy-to-integrate platform.

* Eterna is Dust Networks' low power radio SoC architecture.

TYPICAL APPLICATION



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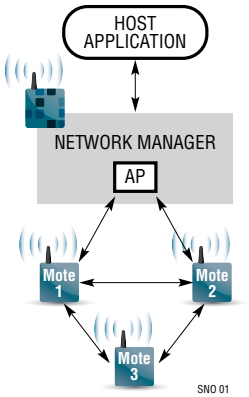
SMARTMESH NETWORK OVERVIEW

A SmartMesh network consists of a self-forming multi-hop mesh of nodes, known as motes, which collect and relay data, and a network manager that monitors and manages network performance and security, and exchanges data with a host application.

SmartMesh networks communicate using a time slotted channel hopping (TSCH) link layer, pioneered by Dust Networks. In a TSCH network, all motes in the network are synchronized to within less than a millisecond. Time in the network is organized into time slots, which enables collision-free packet exchange and per-transmission channel-hopping. In a SmartMesh network, every device has one or more parents (e.g. mote 3 has motes 1 and 2 as parents) that provide redundant paths to overcome communications interruption due to interference, physical obstruction or multi-path fading. If a packet transmission fails on one path, the next retransmission may try on a different path and different RF channel.

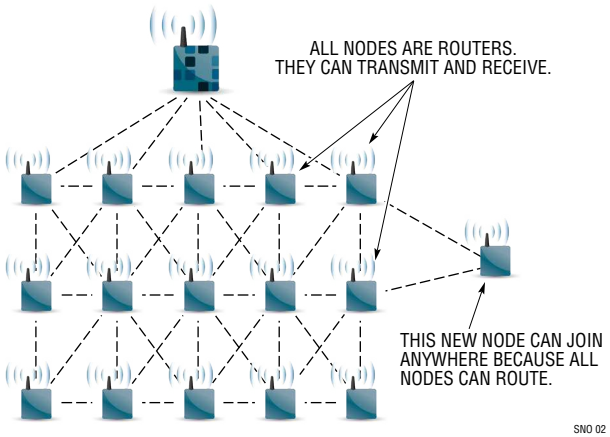
A network begins to form when the network manager instructs its on-board Access Point (AP) radio to begin sending advertisements—packets that contain information that enables a device to synchronize to the network and request to join. This message exchange is part of the security handshake that establishes encrypted communications between the manager or application, and mote. Once motes have joined the network, they maintain synchronization through time corrections when a packet is acknowledged.



An ongoing discovery process ensures that the network continually discovers new paths as the RF conditions change. In addition, each mote in the network tracks performance statistics (e.g. quality of used paths, and lists of potential paths) and periodically sends that information to the network manager in packets called health reports.

The Network Manager uses health reports to continually optimize the network to maintain >99.999% data reliability even in the most challenging RF environments.

The use of TSCH allows SmartMesh devices to sleep in between scheduled communications and draw very little power in this state. Motes are only active in time slots where they are scheduled to transmit or receive, typically resulting in a duty cycle of < 1%. The optimization software in the Network Manager coordinates this schedule automatically. When combined with the Eterna low power radio, every mote in a SmartMesh network—even busy routing ones—can run on batteries for years. By default, all motes in a network are capable of routing traffic from other motes, which simplifies installation by avoiding the complexity of having distinct routers vs non-routing end nodes. Motes may be configured as non-routing to further reduce that particular mote's power consumption and to support a wide variety of network topologies.



At the heart of SmartMesh motes and network managers is the Eterna IEEE 802.15.4e System-on-Chip (SoC), featuring Dust Networks' highly integrated, low power radio design, plus an ARM Cortex-M3 32-bit microprocessor running SmartMesh networking software. The SmartMesh networking software comes fully compiled yet is configurable via a rich set of Application Programming Interfaces (APIs) which allows a host application to interact with the network, e.g. to transfer information to a device, to configure data publishing rates on one or more motes, or to monitor network state or performance metrics. Data publishing can be uniform or different for each device, with motes being able to publish infrequently or faster than once per second as needed.

ABSOLUTE MAXIMUM RATINGS

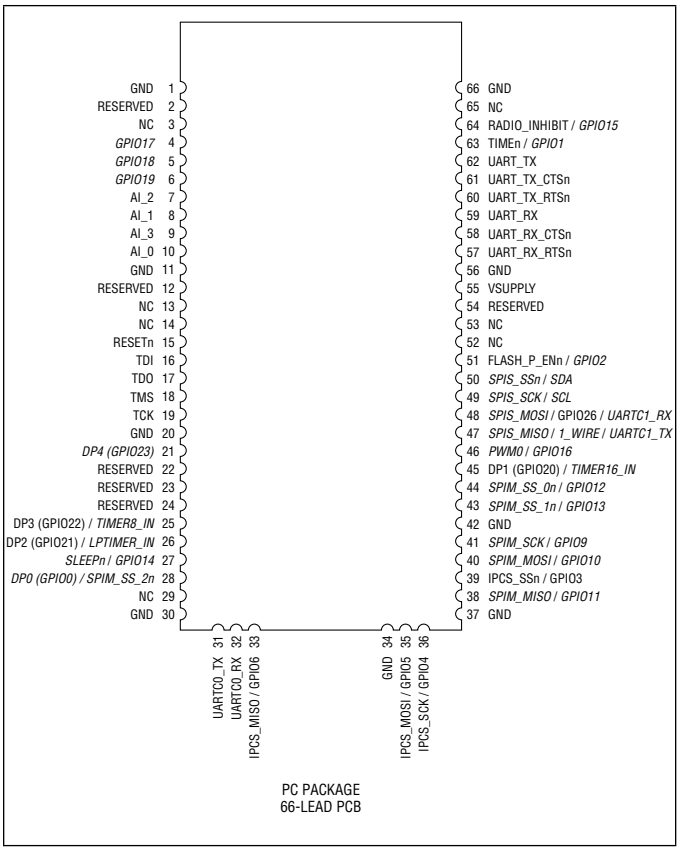
(Note 1)

Supply Voltage on VSUPPLY.....4.20V
Input Voltage on AI_0/1/2/3 Inputs.....1.98V
Voltage on Any Digital
I/O pin.....–0.3V to VSUPPLY + 0.3V
Input RF Level.....+10dBm
Storage Temperature Range (Note 3).....–55°C to 105°C
Operating Temperature Range
LTP5901I/LPT5902I.....–40°C to 85°C

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LTP5901-IPM/LTP5902-IPM.

PIN CONFIGURATION

Pin functions shown in italics are currently not supported in software.



ORDER INFORMATION

LEAD FREE FINISH†	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTP5901IPC-IPMA#PBF	LTP5901IPC-IPMA#PBF	66-Lead (42mm × 24mm × 5.5mm) PCB with Chip Antenna	–40°C to 85°C
LTP5902IPC-IPMA#PBF	LTP5902IPC-IPMA#PBF	66-Lead (37.5mm × 24mm × 5.5mm) PCB with MMCX Connector	–40°C to 85°C

†This product ships with the flash erased at the time of order. OEMs will need to program devices during development and manufacturing.
For legacy part numbers and ordering information go to: http://www.linear.com/product/LTP5901-IPM#orderinfo or
http://www.linear.com/product/LTP5902-IPM#orderinfo

*The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/

RECOMMENDED OPERATING CONDITIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VSUPPLY	Supply Voltage	Including Noise and Load Regulation	●	2.1		3.76	V
	Supply Noise	50Hz to 2MHz	●			250	mV
	Operating Relative Humidity	Non-Condensing	●	10		90	% RH
	Temperature Ramp Rate	While Operating in Network	●	–8		+8	°C/min

DC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

OPERATION/STATE	CONDITIONS		MIN	TYP	MAX	UNITS
Power-on Reset	During Power-On Reset, Maximum 750µs + VSUPPLY Rise Time from 1V to 1.9V			12		mA
Doze	RAM on, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Active			1.2		µA
Deep Sleep	RAM on, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Inactive			0.8		µA
In-Circuit Programming	RESETn and FLASH_P_ENn Asserted, IPCS_SCK at 8MHz			20		mA
Peak Operating Current +8dBm +0dBm	System Operating at 14.7MHz, Radio Transmitting, During Flash Write. Maximum Duration 4.33 ms.			 30 26		 mA mA
Active	ARM Cortex M3, RAM and Flash Operating, Radio and All Other Peripherals Off. Clock Frequency of CPU and Peripherals Set to 7.3728MHz, VCORE = 1.2V			1.3		mA
Flash Write	Single Bank Flash Write			3.7		mA
Flash Erase	Single Bank Page or Mass Erase			2.5		mA
Radio Tx +0dBm +8dBm	Current with Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.			 5.4 9.7		 mA mA
Radio Rx	Current with Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.			4.5		mA

RADIO SPECIFICATIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Band		●	2.4000		2.4835	GHz
Number of Channels		●		15		
Channel Separation		●		5		MHz
Channel Center Frequency	Where k = 11 to 25, as Defined by IEEE 802.15.4	●		2405 + 5•(k-11)		MHz
Modulation	IEEE 802.15.4 Direct Sequence Spread Spectrum (DSSS)					
Raw Data Rate		●		250		kbps
Antenna Pin ESD Protection	HBM per JEDEC JESD22-A114F (Note 2)			±6000		V
Range (Note 4) Indoor Outdoor Free Space	25°C, 50% RH, +2dBi Omni-Directional Antenna, Antenna 2m Above Ground			 100 300 1200		 m m m

RADIO RECEIVER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Sensitivity	Packet Error Rate (PER) = 1% (Note 5)			–93		dBm
Receiver Sensitivity	PER = 50%			–95		dBm
Saturation	Maximum Input Level the Receiver Will Properly Receive Packets			0		dBm
Adjacent Channel Rejection (High Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Above the Desired Signal, PER = 1% (Note 5)			22		dBc
Adjacent Channel Rejection (Low Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Below the Desired Signal, PER = 1% (Note 5)			19		dBc
Alternate Channel Rejection (High Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Above the Desired Signal, PER = 1% (Note 5)			40		dBc
Alternate Channel Rejection (Low Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Below the Desired Signal, PER = 1% (Note 5)			36		dBc
Second Alternate Channel Rejection	Desired Signal at –82dBm, Second Alternate Modulated Channel Either 15MHz Above or Below, PER = 1% (Note 5)			42		dBc
Co-Channel Rejection	Desired Signal at –82dBm, Undesired Signal is an 802.15.4 Modulated Signal at the Same Frequency, PER = 1%			–6		dBc
LO Feed Through				–55		dBm
Frequency Error Tolerance (Note 6)				±50		ppm
Symbol Error Tolerance				±50		ppm
Received Signal Strength Indicator (RSSI) Input Range				–90 to –10		dBm
RSSI Accuracy				±6		dB
RSSI Resolution				1		dB

RADIO TRANSMITTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power	Delivered to a 50Ω load					
High Calibrated Setting				8		dBm
Low Calibrated Setting				0		dBm
Spurious Emissions	Conducted Measurement with a 50Ω Single-Ended Load, +8dBm Output Power. All Measurements Made with Max Hold.					
30MHz to 1000MHz	R_{BW} = 120kHz, V_{BW} = 100Hz			<–70		dBm
1GHz to 12.75GHz	R_{BW} = 1MHz, V_{BW} = 3MHz			–45		dBm
2.4GHz ISM Upper Band Edge (Peak)	R_{BW} = 1MHz, V_{BW} = 3MHz			–37		dBm
2.4GHz ISM Upper Band Edge (Average)	R_{BW} = 1MHz, V_{BW} = 10Hz			–49		dBm
2.4GHz ISM Lower Band Edge	R_{BW} = 100kHz, V_{BW} = 100kHz			–45		dBc
Harmonic Emissions	Conducted Measurement Delivered to a 50Ω Load,					
2nd Harmonic	Resolution Bandwidth = 1MHz, Video Bandwidth = 1MHz			–50		dBm
3rd Harmonic				–45		dBm

DIGITAL I/O CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)		MIN	TYP	MAX	UNITS
V_{IL}	Low Level Input Voltage		●	–0.3		0.6	V
V_{IH}	High Level Input Voltage	(Note 8)	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 1, $I_{OL(MAX)}$ = 1.2mA	●			0.4	V
		Type 2, Low Drive, $I_{OL(MAX)}$ = 2.2mA	●			0.4	V
		Type 2, High Drive, $I_{OL(MAX)}$ = 4.5mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 1, $I_{OH(MAX)}$ = –0.8mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
		Type 2, Low Drive, $I_{OH(MAX)}$ = –1.6mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
		Type 2, High Drive, $I_{OH(MAX)}$ = –3.2mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
	Input Leakage Current	Input Driven to VSUPPLY or GND			50		nA
	Pull-Up/Pull-Down Resistance				50		kΩ

TEMPERATURE SENSOR CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Offset	Temperature Offset Error at 25°C			±0.25		°C
Slope Error				±0.033		°C/°C

ANALOG INPUT CHAIN CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Variable Gain Amplifier						
	Gain			1		8	
	Gain Error					2	%
	Offset-Digital to Analog Converter (DAC)						
	Full-Scale				1.80		V
	Resolution				4		Bits
DNL	Differential Non-Linearity					2.7	mV
	Analog to Digital Converter (ADC)						
	Full-Scale, Signal				1.80		V
	Resolution				1.8		mV
	Offset	Mid-Scale			1.4	12	LSB
DNL	Differential Non-Linearity					1	LSB
INL	Integral Non-Linearity					1	LSB
	Settling Time	10kΩ Source Impedance				10	µs
	Conversion Time					20	µs
	Current Consumption				40		µA
	Analog Inputs (Note 9)						
	Load				20		pF
	Series Input Resistance				1		kΩ

SYSTEM CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Doze to Active State Transition				5		µs
	Doze to Radio Tx or Rx				1.2		ms
Q_{CCA}	Charge to Sample RF Channel RSSI	Charge Consumed Starting from Doze State and Completing an RSSI Measurement			4		µC
Q_{MAX}	Largest Atomic Charge Operation	Flash Erase, 21ms Max Duration	●			200	µC
	RESETn Pulse Width		●	125			µs
	Total Capacitance	Note 13	●			6	µF
	Total Inductance	Note 13	●			3	µH

UART AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Permitted R_X Baud Rate Error	Both Application Programming Interface (API) and Command Line Interface (CLI) UARTs	●	–2		2	%
	Generated T_X Baud Rate Error	Both API and CLI UARTs	●	–1		1	%
$t_{RX\_RTS\ to\ RX\_CTS}$	Assertion of UART_RX_RTSn to Assertion of UART_RX_CTSn, or Negation of UART_RX_RTSn to Negation of UART_RX_CTSn		●	0		2	ms
$t_{RX\_CTS\ to\ RX}$	Assertion of UART_RX_CTSn to Start of Byte		●	0		20	ms
$t_{EOP\ to\ RX\_RTS}$	End of Packet (End of the Last Stop Bit) to Negation of UART_RX_RTSn		●	0		22	ms
$t_{BEG\_TX\_RTS\ to\ TX\_CTS}$	Assertion of UART_TX_RTSn to Assertion of UART_TX_CTSn		●	0		22	ms
$t_{END\_TX\_CTS\ to\ TX\_RTS}$	Negation of UART_TX_CTSn to Negation of UART_TX_RTSn			2			Bit Period
$t_{TX\_CTS\ to\ TX}$	Assertion of UART_TX_CTSn to Start of Byte		●	0		2	Bit Period
$t_{EOP\ to\ TX\_RTS}$	End of Packet (End of the Last Stop Bit) to Negation of UART_TX_RTSn		●	0		1	Bit Period
$t_{RX\_INTERBYTE}$	Receive Inter-Byte Delay		●			100	ms
$t_{RX\_INTERPACKET}$	Receive Inter-Packet Delay		●	20			ms
$t_{TX\_INTERPACKET}$	Transmit Inter-Packet Delay		●	1			Bit Period
$t_{TX\ to\ TX\_CTS}$	Start of Byte to Negation of UART_TX_CTSn		●	0			ns

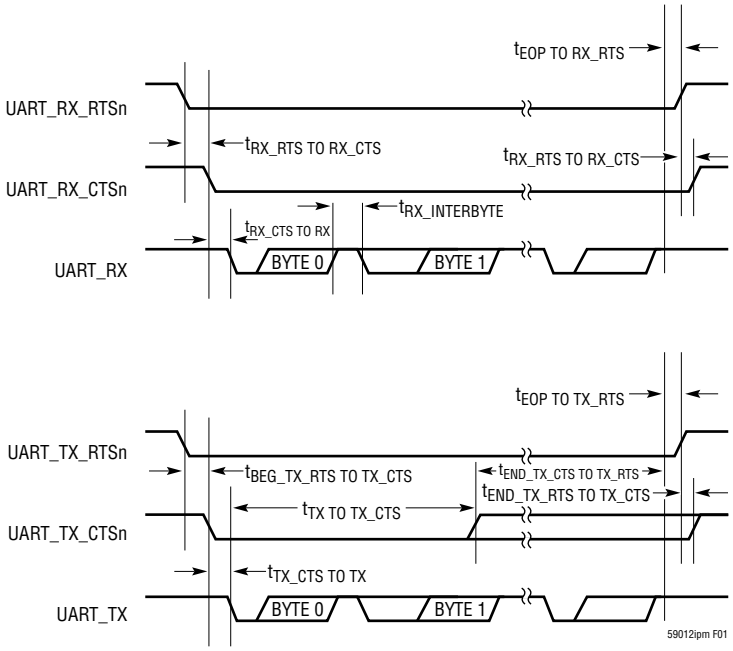


Figure 1. API UART Timing

TIMEn AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{STROBE}	TIMEn Signal Strobe Width		●	125			µs
$t_{RESPONSE}$	Delay from Rising Edge of TIMEn to the Start of Time Packet on API UART		●	0		100	ms
t_{TIME_HOLD}	Delay from End of Time Packet on API UART to Falling Edge of Subsequent TIMEn		●	0			ns
	Timestamp Resolution (Note 10)		●		1		µs
	Network-Wide Time Accuracy (Note 11)		●		±5		µs

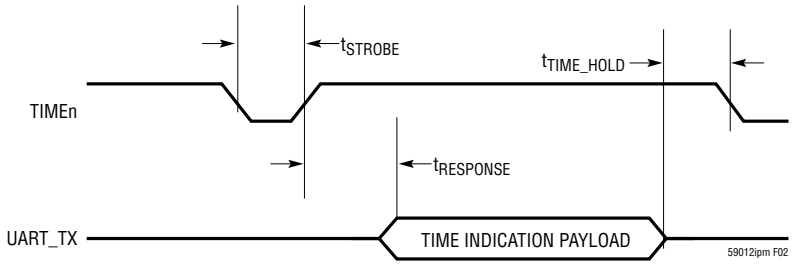


Figure 2. Timestamp Timing

RADIO_INHIBIT AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{RADIO_OFF}	Delay from Rising Edge of RADIO_INHIBIT to Radio Disabled		●			20	ms
$t_{RADIO\_INHIBIT\_STROBE}$	Maximum RADIO_INHIBIT Strobe Width		●			2	s

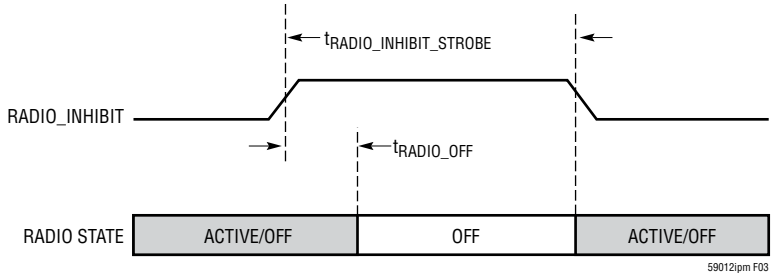


Figure 3. RADIO_INHIBIT Timing

FLASH AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{WRITE}	Time to Write a 32-Bit Word (Note 12)		●			21	µs
t_{PAGE_ERASE}	Time to Erase a 2kB Page (Note 12)		●			21	ms
t_{MASS_ERASE}	Time to Erase 256kB Flash Bank (Note 12)		●			21	ms
	Data Retention	25°C 85°C 105°C		100 20 8			Years Years Years

FLASH SPI SLAVE AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{FP\_EN\_to\_RESET}$	Setup from Assertion of FLASH_P_ENn to Assertion of RESETn		●	0			ns
t_{FP_ENTER}	Delay from the Assertion RESETn to the First Falling Edge of IPCS_SSn		●	125			µs
t_{FP_EXIT}	Delay from the Completion of the Last Flash SPI Slave Transaction to the Negation of RESETn and FLASH_P_ENn		●	10			µs
t_{SSS}	IPCS_SSn Setup to the Leading Edge of IPCS_SCK		●	15			ns
t_{SSH}	IPCS_SSn Hold from Trailing Edge of IPCS_SCK		●	15			ns
t_{CK}	IPCS_SCK Period		●	300			ns
t_{DIS}	IPCS_MOSI Data Setup		●	15			ns
t_{DIH}	IPCS_MOSI Data Hold		●	5			ns
t_{DOV}	IPCS_MISO Data Valid		●	–5		30	ns
t_{OFF}	IPCS_MISO Data Tri-State from Trailing Edge of IPCS_SSn		●	0		30	ns

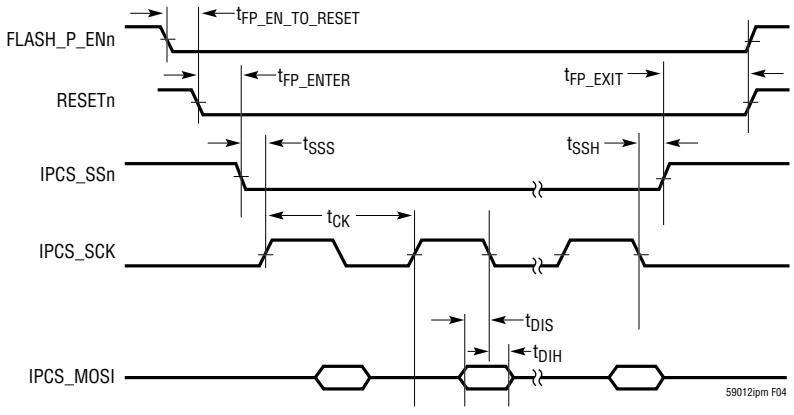


Figure 4. Flash Programming Interface Timing

SPI MASTER AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SSS}	SPIM_SSXn Setup to the Leading Edge of SPIM_SCK		●	t_{CK-30}			ns
t_{SSH}	SPIM_SSXn Hold from Trailing Edge of SPIM_SCK		●	t_{CK-30}			ns
t_{CK}	SPIM_SCK Period		●	268			ns
t_{DIS}	SPIM_MOSI Data Setup		●	30			ns
t_{DIH}	SPIM_MOSI Data Hold		●	5			ns
t_{DOV}	SPIM_MISO Data Valid		●	–5		30	ns
t_{OFF}	SPIM_MISO Data Tri-State from Trailing Edge of SPIM_SSXn		●	0		30	ns

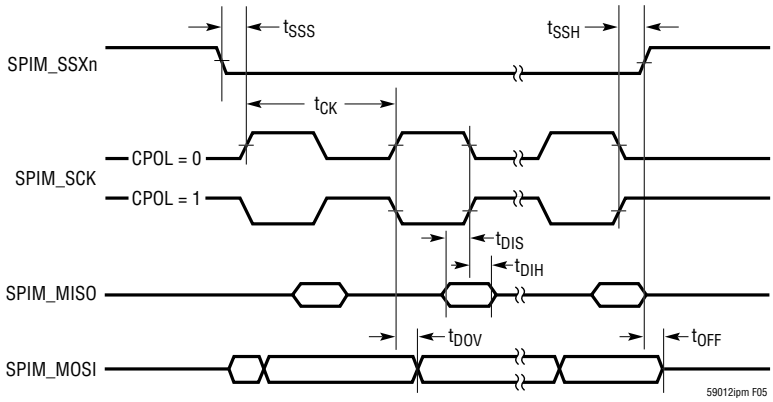


Figure 5. SPI Master Timing - CPHA = 0

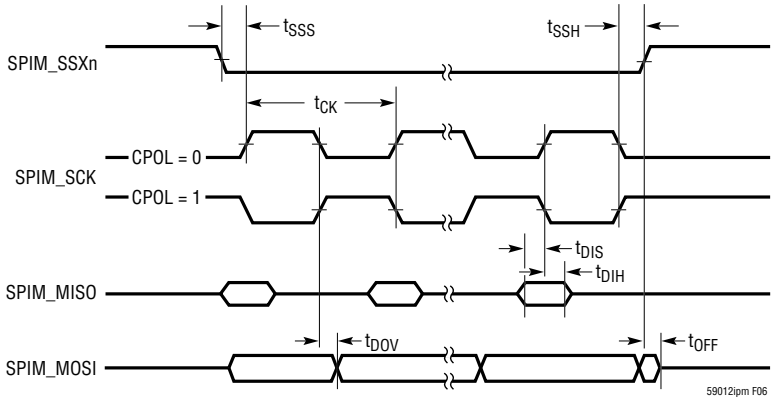


Figure 6. SPI Master Timing - CPHA = 1

I²C AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Frequency	184kHz Operation 92kHz Operation	●		184.3 92.2	188 94	kHz kHz
t_{HD_STA}	Start Hold Time (SCL from SDA)	184kHz Operation 92kHz Operation	●	1 2			µs µs
t_{SU_STA}	Setup Time for a Repeated Start	184kHz Operation, 750ns SCL Rise Time 92kHz Operation, 1.5µs SCL Rise Time	●	300 600			ns ns
t_{HD_DAT}	Data Hold Time	184kHz Operation 92kHz Operation	●	1 2			µs µs
t_{SU_DAT}	Data Setup Time	184kHz Operation 92kHz Operation	●	1 2			µs µs
t_{SU_STO}	Setup Time for Stop Condition	184kHz Operation 92kHz Operation	●	1 2			µs µs

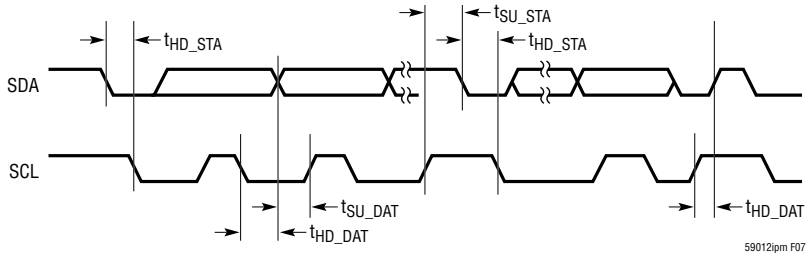


Figure 7. I²C Master Timing

1-WIRE MASTER

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{RSTL}	Reset Low		●	527	556	584	µs
t_{PS}	Presence Sample		●	60.1	69.4	79	µs
t_{BIT_PERIOD}	1_WIRE Data Bit Period		●	82	86.8	92	µs
t_{LOW0}	1_WIRE Write Data 0 Low Width		●	65	69	82	µs
t_{LOW1}	1_WIRE Write Data 1 Low Width		●	8.2	8.7	9.2	µs
t_{LOWR}	1_WIRE Read Data Low Width		●	8.2	8.7	9.2	µs
t_{RS}	Read Sample from 1_WIRE Low		●	13.2	14.6	15.0	µs

FLASH SPI SLAVE AC CHARACTERISTICS

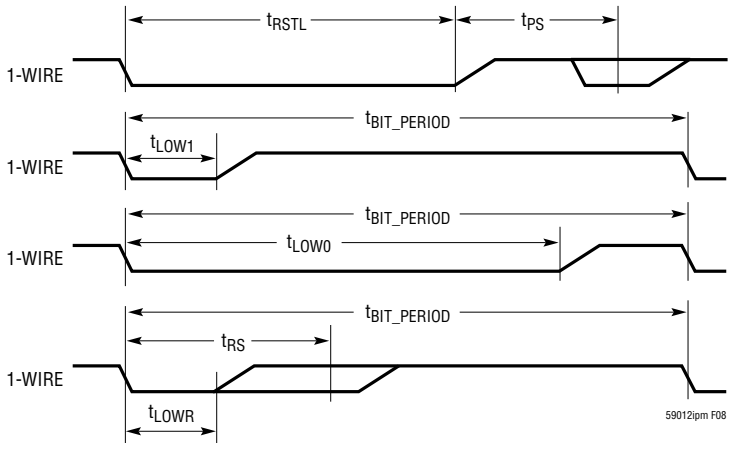


Figure 8. 1-Wire Master Timing

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to Eterna. However, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 3: Extended storage at high temperature is discouraged, as this negatively affects the data retention of Eterna's calibration data. See the FLASH Data Retention section for details.

Note 4: Actual RF range is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, and near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, range varies.

Note 5: As Specified by IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/findstds/standard/802.15.4-2011.html.

Note 6: IEEE Std. 802.15.4-2006 requires transmitters to maintain a frequency tolerance of better than ±40 ppm.

Note 7: Per-pin I/O types are provided in the Pin Functions section.

Note 8: VIH maximum voltage input must respect the VSUPPLY maximum voltage specification.

Note 9: The analog inputs to the ADC can be modeled as a series resistor to a capacitor. At a minimum the entire circuit, including the source impedance for the signal driving the analog input should be designed to settle to within ¼ LSB within the sampling window to match the performance of the ADC.

Note 10: See the SmartMesh IP Mote API Guide for the time indication notification definition.

Note 11: Network time accuracy is a statistical measure and varies over the temperature range, reporting rate and the location of the device relative to the manager in the network. See the Typical Performance Characteristics section for a more detailed description.

Note 12: Code execution from flash banks being written or erased is suspended until completion of the flash operation.

Note 13: Guaranteed by design. Not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

Network motes typically route through at least two parents the traffic destined for the manager. The supply current graphs shown in Figure 9 include a parameter called descendants. In these graphs the term descendants is short for traffic-weighted descendants and refers to an amount of activity equivalent to the number of descendants if all of the network traffic directed to the mote in question. Generally the number of descendants of a parent is more, typically 2x or more, than the number of traffic-weighted descendants. For example, with reference to Figure 10. Network Graph mote P1 has 0.75 traffic-weighted descendants. To obtain this value notice that mote D1 routes half its packets through mote P1 adding 0.5 to the traffic-weighted descendant value; the other half of D1's traffic is routed through its other parent, P2. Mote D2 routes half its packets through mote D1 (the other half going through parent P3), which we know routes half its packets to mote P1, adding another 0.25 to the traffic-weighted descendant value for a total traffic-weighted descendant value of 0.75.

As described in the Application Time Synchronization section, Eterna provides two mechanisms for applications to maintain a time base across a network. The synchronization performance plots that follow were generated using the more precise TIMEn input. Publishing rate is the rate a mote application sends upstream data. Synchronization improves as the publishing rate increases. Baseline synchronization performance is provided for a network operating with a publishing rate of zero. Actual performance for applications in network will improve as publishing rates increase. All synchronization testing was performed with the 1-hop mote inside a temperature chamber. Timing errors due to temperature changes and temperature differences both between the manager and this mote and between this mote and its descendents therefore propagated down through the network. The synchronization of the 3-hop and 5-hop motes to the manager was then affected by the temperature ramps even though they were at room temperature. For 2°C/minute testing the temperature chamber was cycled between –40°C and 85°C at this rate for 24 hours. For 8°C/minute testing, the temperature chamber was rapidly cycled between 85°C and 45°C for 8 hours, followed by rapid cycling between –5°C and 45°C for 8 hours, and lastly, rapid cycling between –40°C and 15°C for 8 hours.

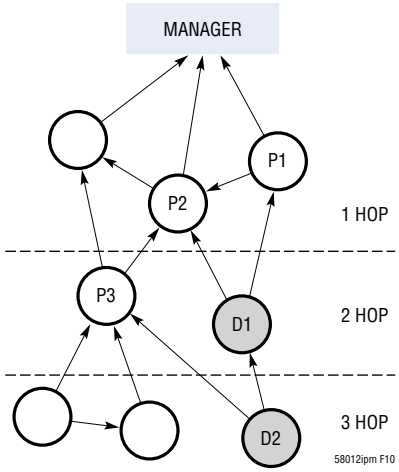


Figure 10. Example Network Graph

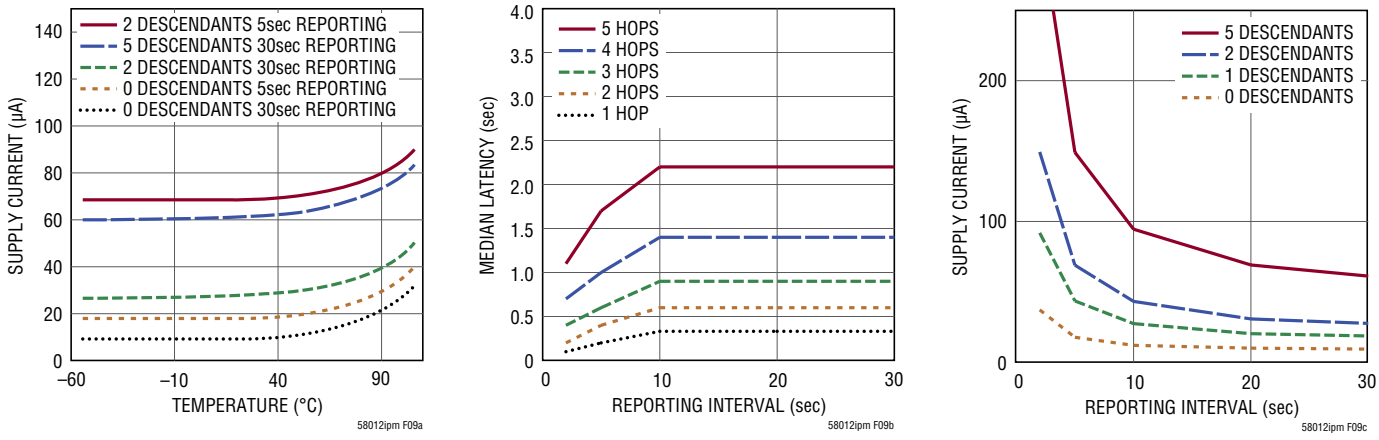
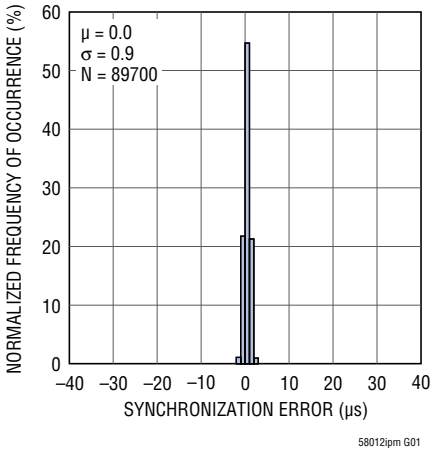


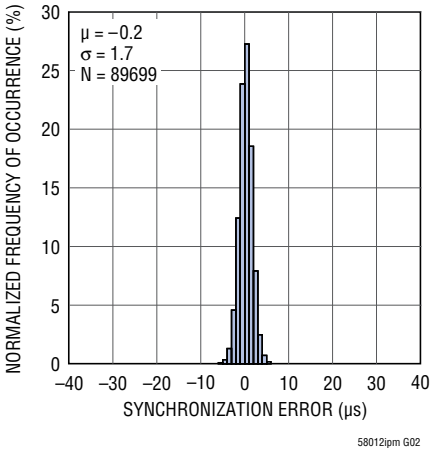
Figure 9

TYPICAL PERFORMANCE CHARACTERISTICS

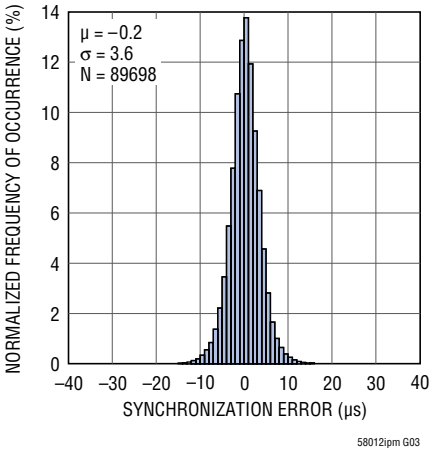
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, Room Temperature



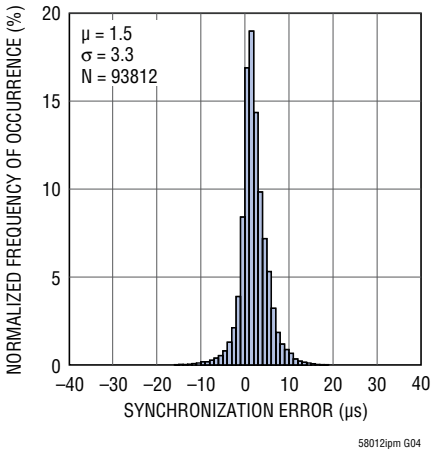
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, Room Temperature



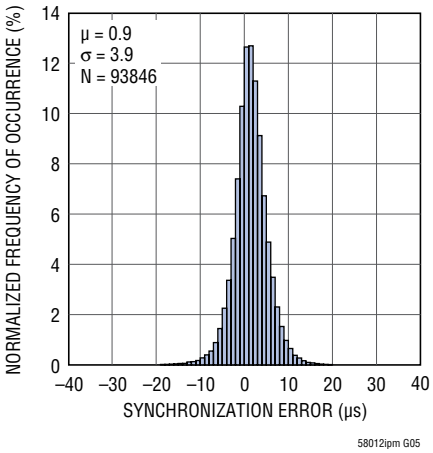
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, Room Temperature



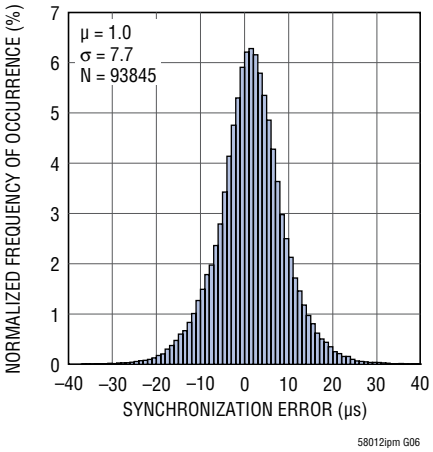
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, 2°C/Min



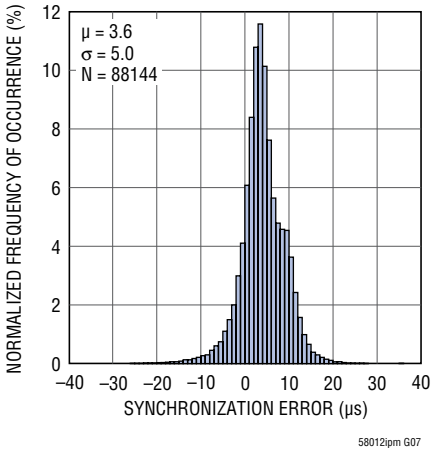
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, 2°C/Min



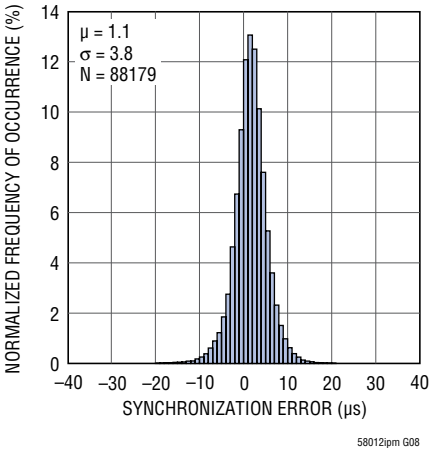
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, 2°C/Min



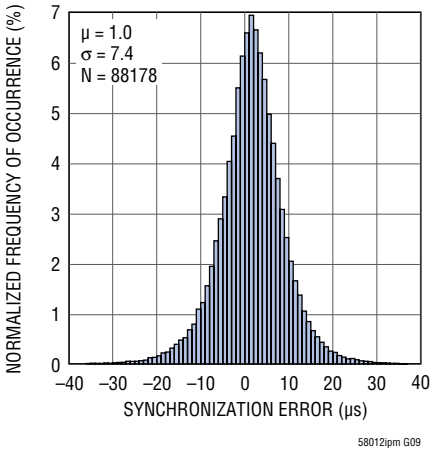
TIMEn Synchronization Error 0 Packet/s Publishing Rate, 1 Hop, 8°C/Min



TIMEn Synchronization Error 0 Packet/s Publishing Rate, 3 Hops, 8°C/Min

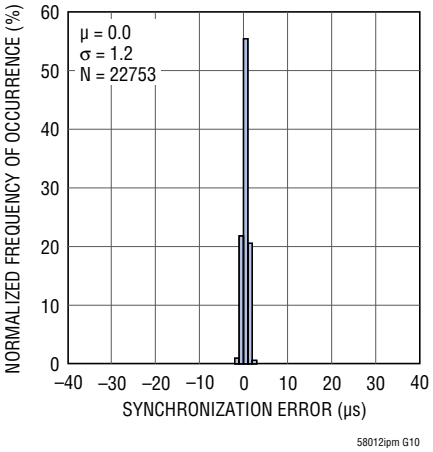


TIMEn Synchronization Error 0 Packet/s Publishing Rate, 5 Hops, 8°C/Min

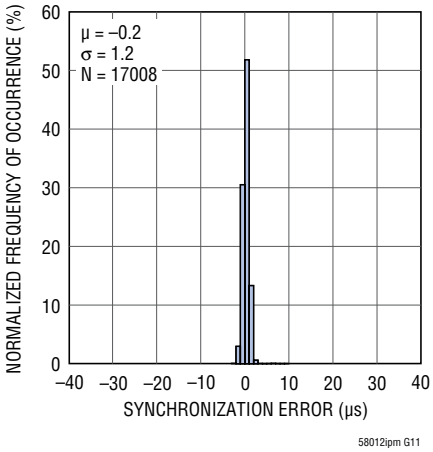


TYPICAL PERFORMANCE CHARACTERISTICS

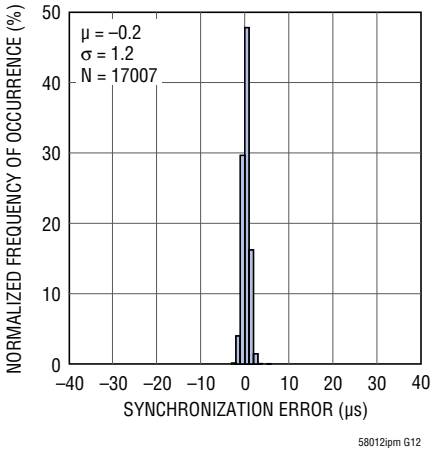
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, Room Temperature



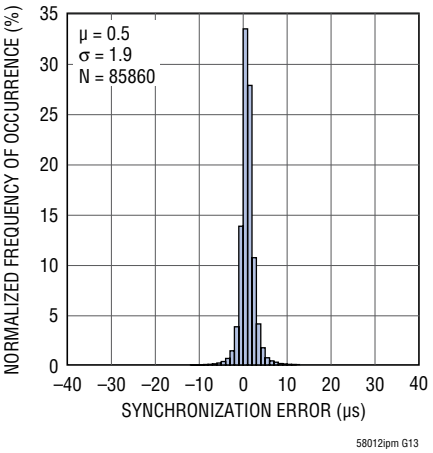
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, Room Temperature



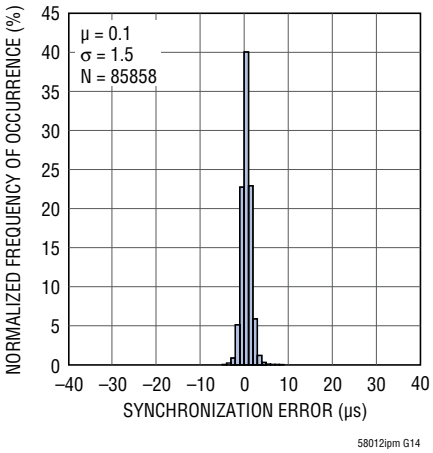
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, Room Temperature



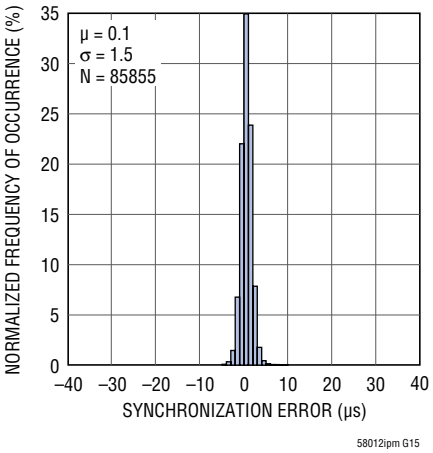
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, 2°C/Min



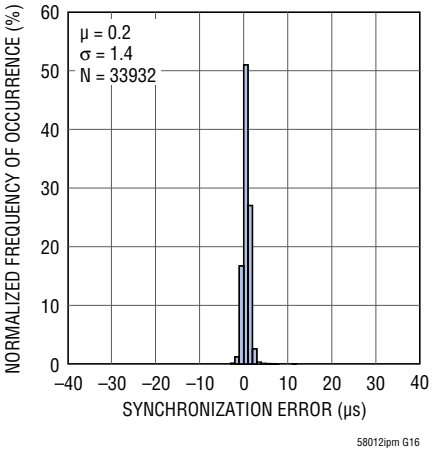
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, 2°C/Min



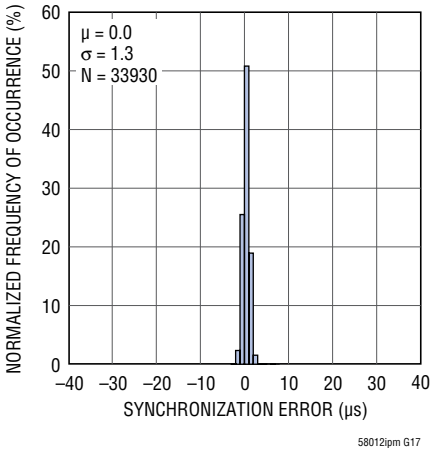
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, 2°C/Min



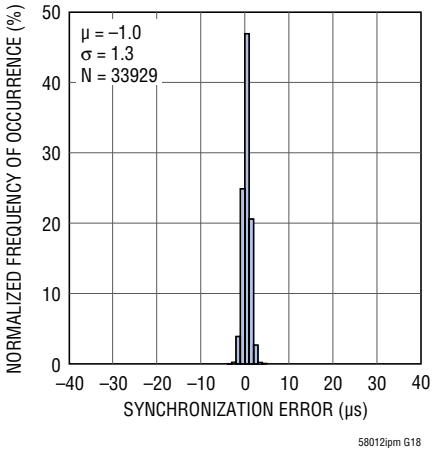
TIMEn Synchronization Error 1 Packet/s Publishing Rate, 1 Hop, 8°C/Min



TIMEn Synchronization Error 1 Packet/s Publishing Rate, 3 Hops, 8°C/Min



TIMEn Synchronization Error 1 Packet/s Publishing Rate, 5 Hops, 8°C/Min



TYPICAL PERFORMANCE CHARACTERISTICS

As described in the SmartMesh Network Overview section, devices in network spend the vast majority of their time inactive in their lowest power state (doze). On a synchronous schedule a mote will wake to communicate with another mote. Regularly occurring sequences which wake, perform a significant function and return to sleep are considered atomic. These operations are considered atomic as the sequence of events can not be separated into smaller events while performing a useful function. For example, transmission of a packet over the radio is an atomic operation. Atomic operations may be characterized in either charge or energy. In a time slot where a mote successfully sends a packet, an atomic transmit includes setup prior to sending the message, sending the message, receiving the acknowledgment and the post processing needed as a result of the message being sent. Similarly in a time slot when a mote successfully receives a packet, an atomic receive includes setup prior to listening, listening until the start of the packet transition, receiving the packet, sending the acknowledge and the post processing required due to the arrival of the packet.

To ensure reliability each mote in the network is provided multiple time slots for each packet it nominally will send and forward. The time slots are assigned to communicate upstream with at least two different motes. When combined with frequency hopping this provides temporal, spacial and spectral redundancy. Given this approach a mote will often listen for a message that it will never receive, since the time slot is not being used by the transmitting mote. It has already successfully transmitted the packet. Since typically 3 time slots are scheduled for every 1 packet to be sent or forwarded, motes will perform more of these atomic "idle listens" than atomic transmit or atomic receive sequences. Examples of transmit, receive and idle listen atomic operations are shown in Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS

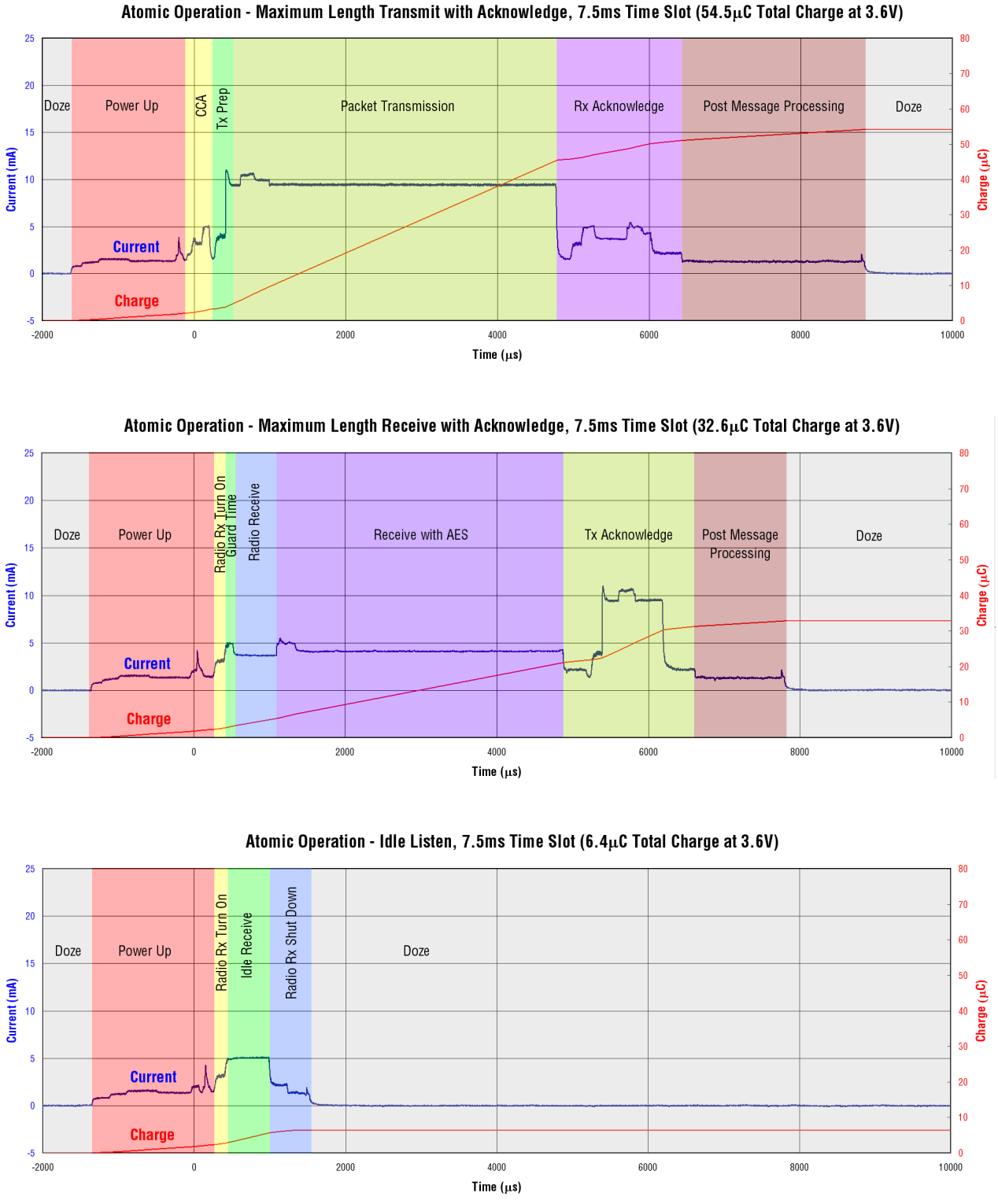


Figure 11

PIN FUNCTIONS

Pin functions shown in italics are currently not supported in software.

The following table organizes the pins by functional groups. For those I/O with multiple functions the alternate functions are shown on the second and third line in their respective row. The **No** column provides the pin number. The second column lists the function. The **Type** column lists the I/O type. The **I/O** column lists the direction of the signal relative to Eterna. The **Pull** column shows which signals have a fixed passive pull-up or pull-down. The **Description** column provides a brief signal description.

NO	POWER SUPPLY	TYPE	I/O	PULL	DESCRIPTION
1	GND	Power	-	-	Ground Connection
11	GND	Power	-	-	Ground Connection
20	GND	Power	-	-	Ground Connection
30	GND	Power	-	-	Ground Connection
34	GND	Power	-	-	Ground Connection
37	GND	Power	-	-	Ground Connection
42	GND	Power	-	-	Ground Connection
56	GND	Power	-	-	Ground Connection
66	GND	Power	-	-	Ground Connection
55	VSUPPLY	Power	-	-	Power Supply Input to Eterna

NO	RADIO	TYPE	I/O	PULL	DESCRIPTION
64	RADIO_INHIBIT	1 (Note 14)	I	-	Radio Inhibit
4	*GPIO17*	*1*	*I/O*	-	*General Purpose Digital I/O*
5	*GPIO18*	*1*	*I/O*	-	*General Purpose Digital I/O*
6	*GPIO19*	*1*	*I/O*	-	*General Purpose Digital I/O*
-	ANTENNA	N/A	N/A	-	Chip Antenna (LTP5901) or MMCX Connector (LPT5902)

NO	ANALOG	TYPE	I/O	PULL	DESCRIPTION
7	AI_2	Analog	I	-	Analog Input 2
8	AI_1	Analog	I	-	Analog Input 1
9	AI_3	Analog	I	-	Analog Input 3
10	AI_0	Analog	I	-	Analog Input 0

NO	RESET	TYPE	I/O	PULL	DESCRIPTION
15	RESETn	1	I	UP	Reset Input, Active Low

NO	JTAG	TYPE	I/O	PULL	DESCRIPTION
16	TDI	1	I	UP	JTAG Test Data In
17	TDO	1	O	-	JTAG Test Data Out
18	TMS	1	I	UP	JTAG Test Mode Select
19	TCK	1	I	DOWN	JTAG Test Clock

PIN FUNCTIONS

Pin functions shown in italics are currently not supported in software.

NO	GPIOs	TYPE	I/O	PULL	DESCRIPTION
21	DP4 (GPIO23)	1	I/O	-	General Purpose Digital I/O
25	DP3 (GPIO22) *TIMER8_EXT*	1	I/O *I*	- -	General Purpose Digital I/O *External Input to 8-Bit Timer/Counter*
26	DP2 (GPIO21) *LPTIMER_EXT*	1	I/O *I*	- -	General Purpose Digital I/O *External Input to Low Power Timer/Counter*
28	*DP0 (GPIO0)* *SPIM_SS_2n*	*1*	*I/O* *O*	- -	*General Purpose Digital I/O* *SPI Master Slave Select 2, Active Low*
45	DP1 (GPIO20) *TIMER16_EXT*	1	I/O *I*	- -	General Purpose Digital I/O *External Input to 16-Bit Timer/Counter*

NO	SPECIAL PURPOSE	TYPE	I/O	PULL	DESCRIPTION
27	*SLEEPn*	*1 (Note 14)*	*I*	-	*Deep Sleep, Active Low*
46	*PWM0* *TIMER16_OUT* *GPIO16*	*2*	*O* *O* *I/O*	- - -	*Pulse Width Modulator 0* *16-Bit Timer/Counter Match Output/PWM Output* *General Purpose Digital I/O*
63	TIMEn	1 (Note 14)	I	-	Time Capture Request, Active Low

NO	CLI	TYPE	I/O	PULL	DESCRIPTION
31	UARTC0_TX	2	O	-	CLI UART 0 Transmit
32	UARTC0_RX	1	I	UP	CLI UART 0 Receive

NO	SPI MASTER	TYPE	I/O	PULL	DESCRIPTION
38	*SPIM_MISO* *GPIO11*	*1*	*I* *I/O*	- -	*SPI Master (MISO) Master In Slave Out Port* *General Purpose Digital I/O*
40	*SPIM_MOSI* *GPIO10*	*2*	*O* *I/O*	- -	*SPI Master (MOSI) Master Out Slave In Port* *General Purpose Digital I/O*
41	*SPIM_SCK* *GPIO9*	*2*	*O* *I/O*	- -	*SPI Master (SCK) Serial Clock Port* *General Purpose Digital I/O*
43	*SPIM_SS_1n* *GPIO13*	*1*	*O* *I/O*	- -	*SPI Master Slave Select 1, Active Low* *General Purpose Digital I/O*
44	*SPIM_SS_0n* *GPIO12*	*1*	*O* *I/O*	- -	*SPI Master Slave Select 0, Active Low* *General Purpose Digital I/O*

PIN FUNCTIONS

Pin functions shown in italics are currently not supported in software.

NO	IPCS SPI/FLASH PROGRAMMING (NOTE 15)	TYPE	I/O	PULL	DESCRIPTION
33	IPCS_MISO *TIMER16_OUT* GPIO6	2	I *O* I/O	- - -	SPI Flash Emulation (MISO) Master In Slave Out Port *16-Bit Timer/Counter Match Output/PWM Output* General Purpose Digital I/O
35	IPCS_MOSI *TIMER16_EXT* GPIO5	1	I *I* I/O	- - -	SPI Flash Emulation (MOSI) Master Out Slave In Port *External Input to 16-Bit Timer/Counter* General Purpose Digital I/O
36	IPCS_SCK *TIMER8_EXT* GPIO4	1	I *I* I/O	- - -	SPI Flash Emulation (SCK) Serial Clock Port *External Input to 8-Bit Timer/Counter* General Purpose Digital I/O
39	IPCS_SSn *LPTIMER_EXT* GPIO3	1	I *I* I/O	- - -	SPI Flash Emulation Slave Select, Active Low *External Input to Low Power Timer/Counter* General Purpose Digital I/O
51	FLASH_P_ENn	1	I	UP	Flash Program Enable, Active Low

NO	I^2C/1-WIRE/SPI SLAVE	TYPE	I/O	PULL	DESCRIPTION
47	*SPIS_MISO* *UARTC1_TX* *1_WIRE*	*2*	*O* *O* *I/O*	- - -	*SPI Slave (MISO) Master In Slave Out Port* *CLI UART 1 Transmit* *1 Wire Master*
48	*SPIS_MOSI* *UARTC1_RX* GPIO26	1	*I* *I* I/O	- - -	*SPI Slave (MOSI) Master Out Slave In Port* *CLI UART 1 Receive* General Purpose Digital I/O
49	*SPIS_SCK* *SCL*	*2*	*I* *I/O*	- -	*SPI Slave (SCK) Serial Clock Port* *I^2C Serial Clock*
50	*SPIS_SSn* *SDA*	*2*	*I* *I/O*	- -	*SPI Slave Select, Active Low* *I^2C Serial Data*

NO	API UART	TYPE	I/O	PULL	DESCRIPTION
57	UART_RX_RTSn	1 (Note 14)	I	-	UART Receive (RTS) Request to Send, Active Low
58	UART_RX_CTSn	1	O	-	UART Receive (CTS) Clear to Send, Active Low
59	UART_RX	1 (Note 14)	I	-	UART Receive
60	UART_TX_RTSn	1	O	-	UART Transmit (RTS) Request to Send, Active Low
61	UART_TX_CTSn	1 (Note 14)	I	-	UART Transmit (CTS) Clear to Send, Active Low
62	UART_TX	2	O	-	UART Transmit

Note 14: These inputs are always enabled and must be driven or pulled to a valid state to avoid leakage.

Note 15: Embedded programming over the IPCS SPI bus is only avaliable when RESETn is asserted.

PIN FUNCTIONS

VSUPPLY: System and I/O Power Supply. Provides power to the module. The digital-interface I/O voltages are also set by this voltage.

ANTENNA: Multiplexed Receiver Input and Transmitter Output Pin. The impedance presented to the MMCX connector should be 50Ω, single-ended with respect to ground.

AI_0, AI_1, AI_2, AI_3: Analog Inputs. These pins are multiplexed to the analog input chain. The analog input chain, as shown in Figure 12, is software-configurable and includes a variable-gain amplifier, an offset-DAC for adjusting input range, and a 10-bit ADC. Valid input range is between 0V to 1.8V. Analog inputs can be sampled as described in section Signal/Data Acquisition and Control.

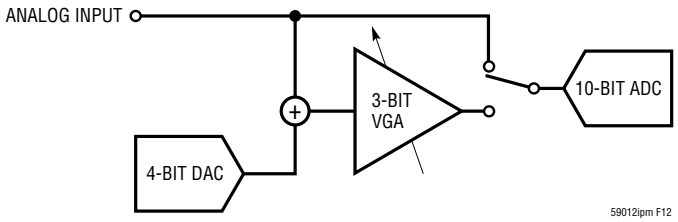


Figure 12. Analog Input Chain

RESETn: The asynchronous reset signal is internally pulled up. Resetting Eterna will result in the ARM Cortex M3 rebooting and loss of network connectivity. Use of this signal for resetting Eterna is not recommended, except during power-on and in-circuit programming.

RADIO_INHIBIT: RADIO_INHIBIT provides a mechanism for an external device to temporarily disable radio operation. Failure to observe the timing requirements defined in the RADIO_INHIBIT AC Characteristics section, may result in unreliable network operation. In designs where the RADIO_INHIBIT function is not needed the input must either be tied, pulled or actively driven low to avoid excess leakage.

TMS, TCK, TDI, TDO: JTAG Port Supporting Software Debug and Boundary Scan.

SLEEPn: The SLEEPn function is not currently supported in software. The SLEEPn input must either be tied, pulled or actively driven high to avoid excess leakage.

UART_RX, UART_RX_RTSn, UART_RX_CTSn, UART_TX, UART_TX_RTSn, UART_TX_CTSn: The API UART interface includes bidirectional wake up and flow control. Unused input signals must be driven or pulled to their inactive state.

TIMEn: Strobing the TIMEn input is the most accurate method to acquire the network time maintained by Eterna. Eterna latches the network time stamp with sub-microsecond resolution on the rising edge of the TIMEn signal and produces a packet on the API serial port containing the timing information.

UARTC0_RX, UARTC0_TX: The CLI UART provides a mechanism for monitoring, configuration and control of Eterna during operation. For a complete description of the supported commands see the SmartMesh IP Mote CLI Guide.

GPIO0, GPIO3 to GPIO6, GPIO9 to GPIO13, GPIO16, GPIO20 to GPIO23, GPIO26: General purpose I/Os that can be sampled or driven as described in the On-Chip Software Development Kit (On-Chip SDK).

FLASH_P_ENn, IPCS_SSn, IPCS_SCK, IPCS_MISO, IPCS_SSn: The In-Circuit Programming Control System (IPCS) bus enables in-circuit programming of Eterna's flash memory. IPCS_SCK is a clock and should be terminated appropriately for the driving source to prevent overshoot and ringing.

SPIM_CLK, SPIM_MISO, SPIM_MOSI, SPIM_SS_0n, SPIM_SS_1n, SPIM_SS_4n: The SPI Master bus with support for up to three SPI slave devices, via the On-Chip Software Development Kit (On-Chip SDK) provides an interface to SPI peripheral slave devices. The SPI interface is synchronous to SPIM_CLK, which should be treated as a clock signal and terminated appropriately .

1-WIRE: The 1-Wire master clock/data/power signal. See the On-Chip Software Development Kit (On-Chip SDK) for details on operating the 1-Wire Master controller.

SCL, SDA: The I^2C bus SCL and SDA should be externally pulled to V_{SUPPLY} with a 10k resistor. See the On-Chip Software Development Kit (On-Chip SDK) for details on operating the 1-Wire Master controller.

OPERATION

The LTP5901-IPM/LTP5902-IPM is the world's most energy efficient IEEE 802.15.4 compliant platform, enabling battery and energy harvested applications. With a powerful 32-bit ARM Cortex-M3, best-in-class radio, flash, RAM and purpose-built peripherals, Eterna provides a flexible, scalable and robust networking solution for applications demanding minimal energy consumption and data reliability in even the most challenging RF environments.

Shown in Figure 13, Eterna integrates purpose-built peripherals that excel in both low operating-energy consumption and the ability to rapidly and precisely cycle between operating and low-power states. Items in the gray shaded region labeled Analog Core correspond to the analog/RF components.

POWER SUPPLY

Eterna is powered from a single pin, VSUPPLY, which powers the I/O cells and is also used to generate internal supplies. Eterna's two on-chip DC/DC converters minimize Eterna's energy consumption while the device is awake. To conserve power the DC/DC converters are disabled when the device is in low power state. Eterna's power supply conditioning architecture, including the two integrated DC/DC converters and three integrated low dropout regulators, provides excellent rejection of supply noise. Eterna's operating supply voltage range is high enough to support direct connection to lithium-thionyl chloride (Li-$SOCl_2$) sources and wide enough to support battery operation over a broad temperature range.

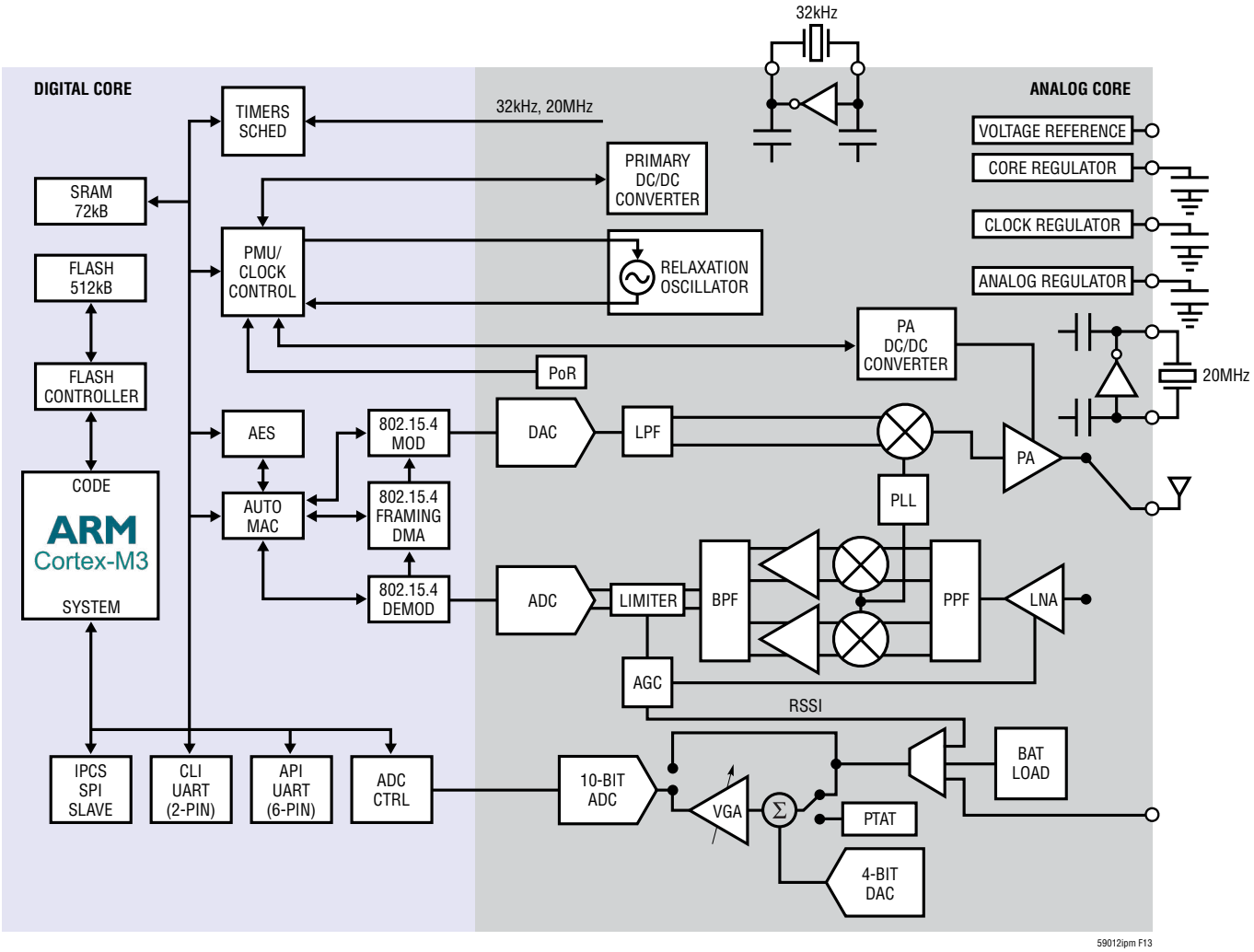


Figure 13. Eterna Block Diagram

OPERATION

SUPPLY MONITORING AND RESET

Eterna integrates a Power-on Reset (PoR) circuit. As the RESETn input pin is nominally configured with an internal pull-up resistor, no connection is required. For a graceful shutdown, the software and the networking layers should be cleanly halted via API commands prior to assertion of the RESETn pin. See the SmartMesh IP Mote API Guide for details on the disconnect and reset commands. Eterna includes a soft brown-out monitor that fully protects the flash from corruption in the event that power is removed while writing to flash. Integrated flash supervisory functionality, in conjunction with a fault tolerant file system, yields a robust nonvolatile storage solution.

PRECISION TIMING

A major feature of Eterna over competing 802.15.4 product offerings is its low-power dedicated timing hardware and timing algorithms. This functionality provides timing precision two to three orders of magnitude better than any other low-power solution available at the time of publication. Improved timing accuracy allows motes to minimize the amount of radio listening time required to ensure packet reception thereby lowering even further the power consumed by SmartMesh networks. Eterna's patented timing hardware and timing algorithms provide superior performance over rapid temperature changes, further differentiating Eterna's reliability when compared with other wireless products. In addition, precise timing enables networks to reduce spectral dead time, increasing total network throughput.

APPLICATION TIME SYNCHRONIZATION

In addition to coordinating time slots across the network, which is transparent to the user, Eterna's timing management is used to support two mechanisms to share network time. Having an accurate, shared, network-wide time base enables events to be accurately time stamped or tasks to be performed in a synchronized fashion across a network. Eterna will send a time packet through its serial interface when one of the following occurs:

- Eterna receives an API request to read time
- The TIMEn signal is asserted

The use of TIMEn has the advantage of being more accurate. The value of the timestamp is captured in hardware relative to the rising edge of TIMEn. If an API request is used, due to packet processing, the value of the timestamp may be captured several milliseconds after receipt of the packet due to packet processing. See the TIMEn AC Characteristics section for the time function's definition and specifications.

TIME REFERENCES

Eterna includes three clock sources: an internal relaxation oscillator, a low power oscillator designed for a 32.768kHz crystal, and the radio reference oscillator designed for a 20MHz crystal.

Relaxation Oscillator

The relaxation oscillator is the primary clock source for Eterna, providing the clock for the CPU, memory subsystems, and all peripherals. The internal relaxation oscillator is dynamically calibrated to 7.3728 MHz. The internal relaxation oscillator typically starts up in a few µs, providing an expedient, low energy method for duty cycling between active and low power states. Quick start-up from the doze state, defined in the State Diagram section, allows Eterna to wake up and receive data over the UART and SPI interfaces by simply detecting activity on the appropriate signals.

32.768kHz Crystal

Once Eterna is powered up and the 32.768kHz crystal source has begun oscillating, the 32.768kHz crystal remains operational while in the active state, and is used as the timing basis when in doze state. See the State Diagram section for a description of Eterna's operational states.

20MHz Crystal

The 20 MHz crystal source provides a frequency reference for the radio, and is automatically enabled and disabled by Eterna as needed.