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LV25500PQA

Bi-CMOS LSI

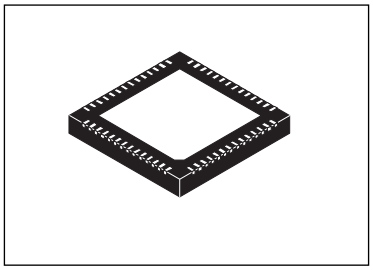
FM Multiplex Broadcasting Receive Tuner

ON Semiconductor®

http://onsemi.com

Overview

LV25500PQA is in-vehicle FM multiplex broadcasting receive only tuner IC that makes FM tuner, PLL, and the RDS demodulator single-chip.
ON Semiconductor's unique technology enables to reduce a large number of external components for high frequency like coils, ceramic filters and varicaps which were required for conventional tuner IC.
Small FM multiple tuner that can be installed also in PND etc. including AVN can be composed.



WQFN56 7x7, 0.4P

Features

- No need for adjustment work.
- The AF search processing on the main tuner side is unnecessary according to using with the main tuner together.
- The high sensitivity reception and the high strong input tolerance are united by LNA built into equipped with the WIDE-AGC function.
- The third and fifth high harmonic rejection type mixers of a local oscillation are adopted.
- The switch of UPPER/LOWER of a local oscillation and IF-BPF of injection is possible when the image signal is detected.
- The complex BPF of the image attenuation type is built into.
- IF-BPF is made built-in by LOW-IF frequency (IF = 575 kHz) adoption.
- Dynamic range of S meter is wide.
- S meter tuning-system is adopted.
- The DLL demodulation method is adopted for FM demodulation circuit.
- LPF for the carrier removal is built into.
- S meter level, the adjacent obstruction level, and the multipath can be detected and read by way of I^2C BUS.
- BPF (57 kHz) for the BPSK detection is built into.
- It becomes easy to miniaturize the tuner set with built-in the RDS demodulator.
- 36.8MHz is adopted for the crystal oscillation frequency.
- The number of external parts is little.

Functions

- FM tuner function
- Antenna dumping control function
- Local oscillation of PLL control type
- WIDE/NARROW/IF-AGC function
- DLL demodulator
- 57kHz carrier recovery and re-clock regeneration
- BPSK decode / differential decode
- ID reset function
- I^2C BUS control
- I^2C reset function
- Standby function

* I^2C Bus is a trademark of Philips Corporation.

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Specification

Absolute Maximum Ratings at Ta = 25ºC

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	V_{CC} max	Ta = 25ºC	6.0	V
Maximum input voltage	VIN1max	LNA_P, LNA_N	−0.3 to 6.0	V
	VIN2max	TEST, RST, XSTBY, XRST	−0.3 to 3.45	V
	VIN3max	SDA, SCL	−0.3 to 3.45	V
Maximum output voltage	VO1max	LPFO, BPSK, SMETER	−0.3 to 6.0	V
	VO2max	RDS-ID, RDDA, RDCL, INT, SD	−0.3 to 3.45	V
	VO3max	SDA	−0.3 to 3.45	V
Allowable power dissipation	Pd max	Ta≤85ºC (*)Specified board	1.38	W
Operating temperature	Topr		−40 to +85	ºC
Storage temperature	Tstg		−50 to +150	ºC

(*) Specified board is attached：80.0mm×80.0mm×1.0mm, glass epoxy board

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note : Machine model ESD voltage level of the pin 18 is less than 200V, because their high frequency characteristics are extremely important. Handle pins 18 with care to prevent electrostatic breakdown.

Operating Conditions at Ta = 25ºC

Parameter	Symbol	Conditions	Ratings
Recommended supply voltage	V_{CC}		5.0V
Operating supply voltage range	V_{CC} op		4.5 to 5.5V
Input High level voltage	VINH1	TEST, RST, XSTBY, XRST	3 to 3.45V
	VINH2	SDA, SCL	2.3 to 3.45V
Input Low level voltage	VINL1	TEST, RST, XSTBY, XRST	0.5V or less
	VINL2	SDA, SCL	0.9V or less
SCL clock frequency	fSCL	SCL	400kHz or less

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Range of Reception Frequency

Parameter	Symbol	Conditions	Ratings	unit
FM input frequency1	FM_EU	FM EU	87.5 to 108.0	MHz
FM input frequency2	FM_US	FM US	87.9 to 108.1	MHz
FM input frequency3	FM_JP	FM JP	76 to 90	MHz

The constant in application circuit is different in FM_EU, FM_US and FM_JP.

Electric Characteristics at Ta = 25ºC, V_{CC} = 5.0V
fc = 98.1MHz, Vin = 60dBuVEMF, fm = 1kHz, Audio filter: HPF = 100Hz, LPF = 15kHz

Parameter	Symbol	Conditions	min	typ	max	unit
Usable sensitivity 1 (S/N30dB)	SN30	22.5kHz dev, fm = 1kHz, S/N = 30dB input level	-	12	20	dBuVEMF
Usable sensitivity 2 (S/N10dB)	SN10	7.5kHz dev, fm = 76kHz, S/N = 10dB input level [1]	-	27	-	dBuVEMF
SN ratio 1	SN1	22.5kHz dev, fm = 1kHz	34	46	-	dB
SN ratio 2	SN2	7.5kHz dev, fm = 76kHz [1]	-	23	-	dB
AM suppression ratio	AMR	AM 30% mod	34	45	-	dB
Image removal ratio	IMR	22.5kHz dev, fm = 1kHz	-	46	-	dB
Audio output level 1	ADO1	7.5kHz dev, fm = 1kHz [1]	12	30	45	mVrms
Audio output level 2	ADO2	7.5kHz dev, fm = 76kHz [1]	12	23	45	mVrms
SD sensitivity	SDS	LNA input level when SD terminal is on.	13	20	27	dBuVEMF
Center frequency	f0	57kHz BPF peak frequency		57		kHz
Output (L) level voltage	VOL1	RDDA, RDCL, INT, SD IOL=0.5mA	-	-	0.5	V
	VOL2	RDS-ID,IOL=0.5mA	-	-	0.5	V
	VOL3	SDA (when V_{DD} pull up)	-	-	0.5	V
Output (H) level voltage	VOH1	RDDA, RDCL, INT, SD IOH=0.5mA	2.3	-	-	V
	VOH2	SDA (when V_{DD} pull up)	0.7*V_{DD} [2]		-	V
Current consumption 1	ICC1	When no signal input RDS mode	125	165	205	mA
Current consumption 2	ICC2	When no signal input VICS mode	120	155	190	mA

[1] Audio filter : HPF = 100Hz, LPF = OFF
[2] V_{DD} : µ-COM Supply Voltage

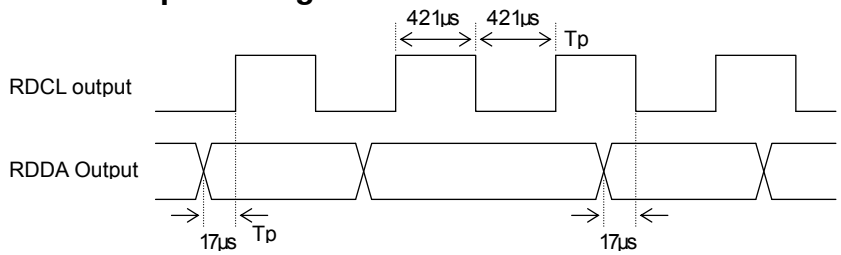
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

RDS input/output Format

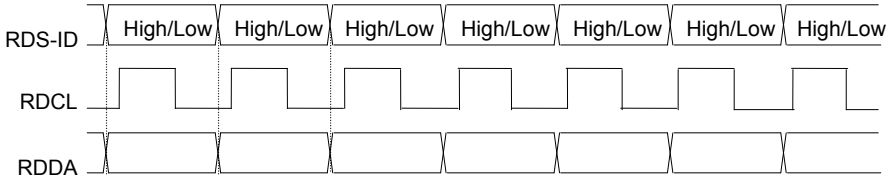
	RST Pin
RST= 0	Normal operation
RST= 1	Reset of RDS-ID and demodulator circuit

	RDS-ID
RDS-IDoutput	Active-Low

RDCL/RDDA Output timing

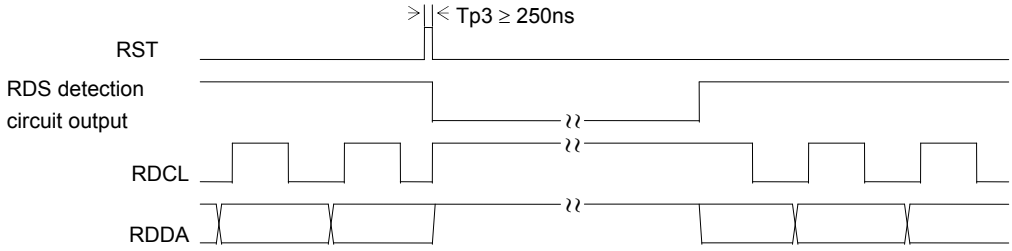


RDS-ID Output timing



Note : RDS-ID is High : data with Low RDS reliability, Low: data with High RDS reliability

RST operation



Note : RDCL and RDDA outputs keep high level after input of RST until RDS detection circuit output is detected.

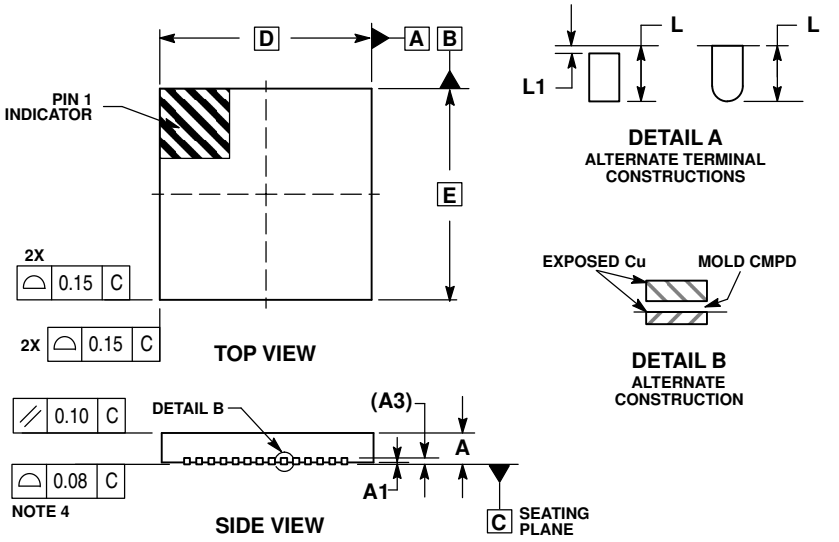
Note : When the reception channel is changed, a memory reset must be applied using RST input.

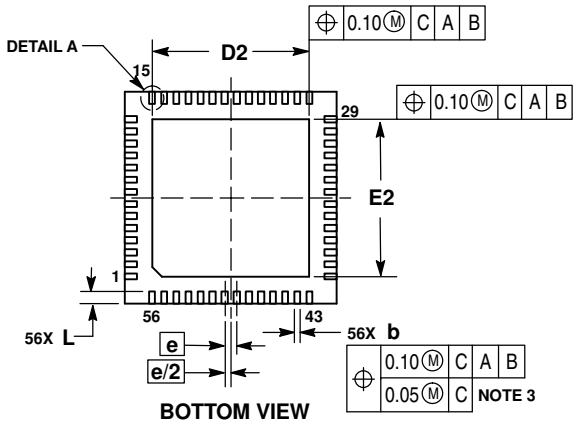
Package Dimensions

WQFN56 (7.0mm x 7.0mm)

unit : mm

WQFN56 7x7, 0.4P
CASE 510BD
ISSUE O





NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

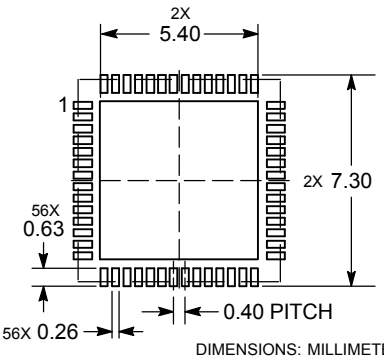
	MILLIMETERS	
DIM	MIN	MAX
A	---	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	7.00 BSC	
D2	5.10	5.30
E	7.00 BSC	
E2	5.10	5.30
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪ ”, may or may not be present.

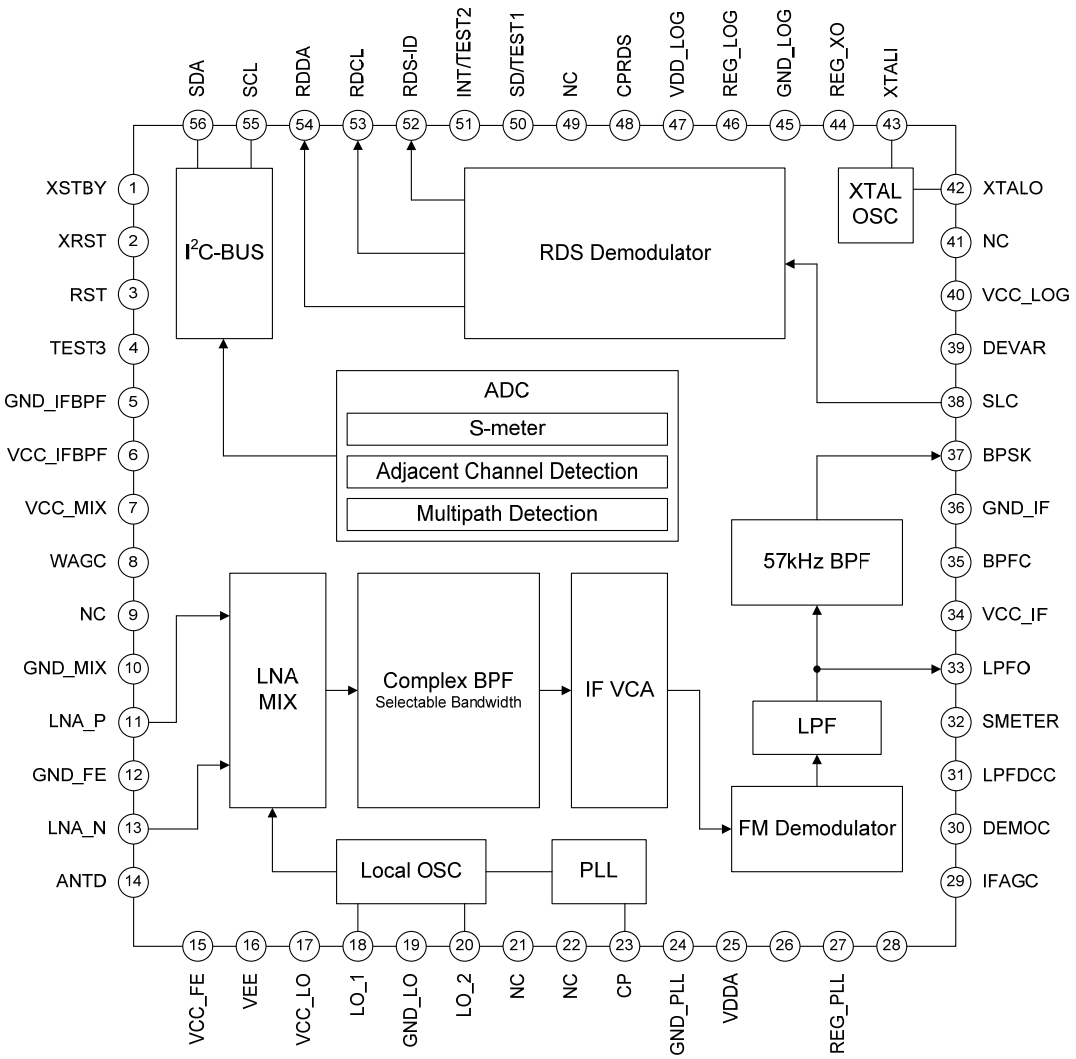
RECOMMENDED SOLDERING FOOTPRINT*



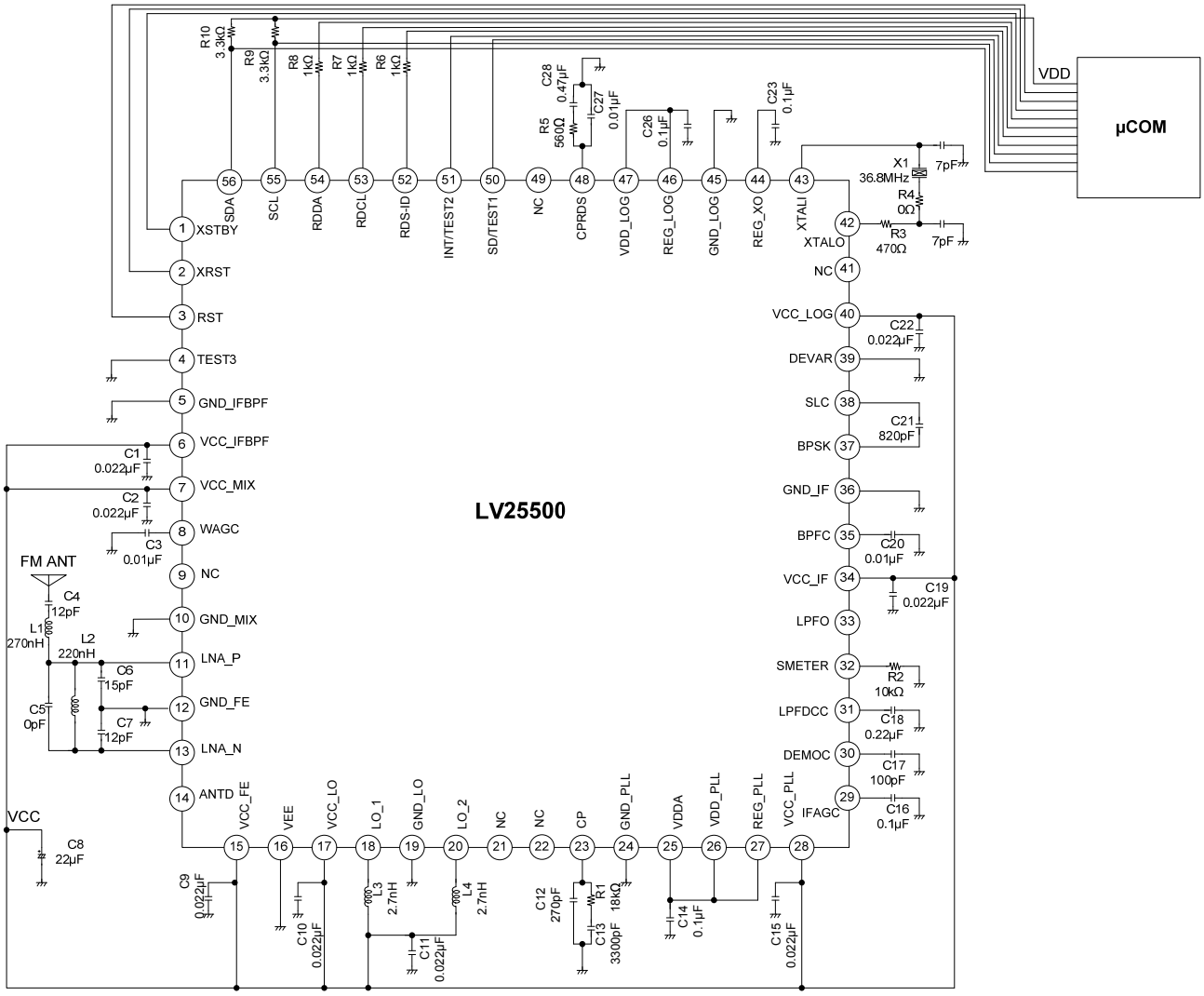
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Block Diagram



Example of application circuit (FM_US) [1] [2] [3] [4] [5]



Used Components(FM_US)

Component	Parameter	Value	Supplier	Type
L1	RF BPF coil	270nH	SAGAMI	C2012C-R27G-RC
L2	RF BPF coil	220nH	SAGAMI	C2012C-R22G-RC
L3/L4	Local OSC coil	2.7nH	SAGAMI	C2012H-2N7D-RD
X1	Crystal	36.8MHz	KDS	DSX321G

[1] The external parts for crystal oscillation circuit terminal (pin42 and pin43) need to match the quartz vibrator. R3, R4, C24, C25 are the tentative arrangement parts.

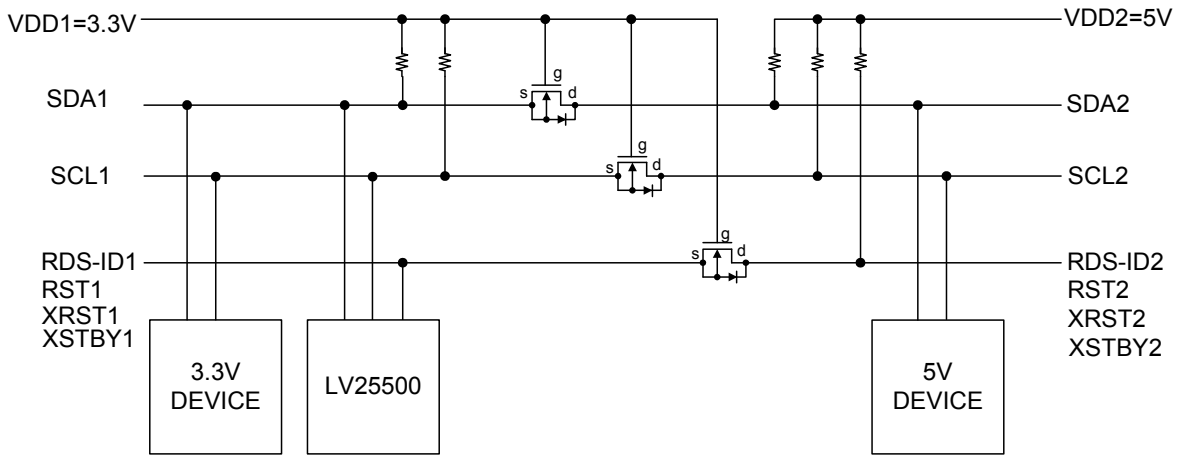
[2] Caution is required for layout of the board because the parasitic capacitance between pin42, pin43 and Power, GND, etc causes the decrease of the margin of the crystal oscillation and the deviation of the crystal frequency, etc.

[3] This IC uses the signal of FM band frequency (VCO divided into 1/4) which leaks into ANT pin. If the VCO leakage affects the performance of the system, make sure to connect an isolator on ANT pin path.

[4] REG (pin27, pin44, pin46) is only used for LV25500.

[5] This example of application circuit, the power-supply voltage becomes the circuit using 3.3V µ-COM.
The bi-directional level shifter circuit is connecting two different voltage sections in I2C-Bus system.

Example of level shift circuit



Pin description

Pin	Name	I/O	Explanation
1	XSTBY	I	Standby pin(0:stanby, 1:standby release)
2	XRST	I	Tuner reset pin (0:reset, 1:reset release)
3	RST	I	RDS–ID reset pin(Positive polarity)
4	TEST3	-	Test pin
5	GND_IFBPF	P	GND pin for IF BPF
6	VCC_IFBPF	P	VCC pin for IF BPF
7	VCC_MIX	P	VCC pin for MIXER
8	WAGC	O	Capacity pin for WAGC
9	NC	NC	No connection
10	GND_MIX	P	GND pin for MIXER
11	LNA_P	I	Input pin for LNA+
12	GND_FE	P	GND pin for LNA
13	LNA_N	I	Input pin for LNA-
14	ANTD	O	ANT dumping control pin
15	VCC_FE	P	Power-supply pin for LNA
16	VEE	P	GND pin for ESD
17	VCC_LO	P	VCC pin for local oscillation
18	LO_1	O	Inductor connection pin for local oscillation
19	GND_LO	P	GND pin for local oscillation
20	LO_2	O	Inductor connection pin for local oscillation
21	NC	NC	No connection
22	NC	NC	No connection
23	CP	O	Capacity pin for PLL charge pump
24	GND_PLL	P	GND pin for PLL logic
25	VDDA	P	Power-supply pin for logic
26	VDD_PLL	P	Power-supply pin for PLL logic
27	REG_PLL	O	Regulator capacity pin for PLL logic
28	VCC_PLL	P	Power-supply pin for Regulator
29	IFAGC	O	Capacity pin for IFAGC
30	DEMOC	O	Capacity pin for demodulation/detection
31	LPFDCC	O	Capacity pin for LPF DC cancel
32	SMETER	O	S-meter output pin
33	LPFO	O	FM demodulation output pin (After band limitation)
34	VCC_IF	P	VCC pin IF
35	BPFC	O	Capacity pin for BPF
36	GND_IF	P	GND pin for IF
37	BPSK	O	Bi-phase data career output pin
38	SLC	I	Data slicer input pin
39	DEVAR	I	Device address setting pin
40	VCC_LOG	P	VCC pin for Regulator
41	NC	NC	No connection
42	XTALO	O	Crystal resonance element connection pin
43	XTALI	I	Crystal resonance element connection pin
44	REG_XO	O	Regulator pin for crystal
45	GND_LOG	P	GND pin for control logic
46	REG_LOG	O	Regulator pin for control logic
47	VDD_LOG	P	Power-supply pin for control logic
48	CPRDS	O	PLL charge pump pin for RDS clock generation
49	NC	NC	No connection
50	SD/TEST1	O	Station detector pin/Test pin
51	INT/TEST2	O	Interrupt flag pin/Test pin
52	RDS-ID	O	RDS reliability data output pin (0:high reliability, 1:low reliability)
53	RDCL	O	RDS clock output pin
54	RDDA	O	RDS data output pin
55	SCL	I	Serial data clock input pin
56	SDA	I/O	Serial data input/output pin

I²C Bus Communication Format

Device address (in case of 39pin, DEVAR, pull down) Normal

MSB							LSB	Function
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	0	0	0	**0**	WRITE mode (**C0h**)
1	1	0	0	0	0	0	**1**	READ mode (**C1h**)

Device address (in case of 39pin, DEVAR, pull up)

MSB							LSB	Function
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	0	0	1	**0**	WRITE mode (**C2h**)
1	1	0	0	0	0	1	**1**	READ mode (**C3h**)

Register Address: Reg 0 ~ Reg 2Fh

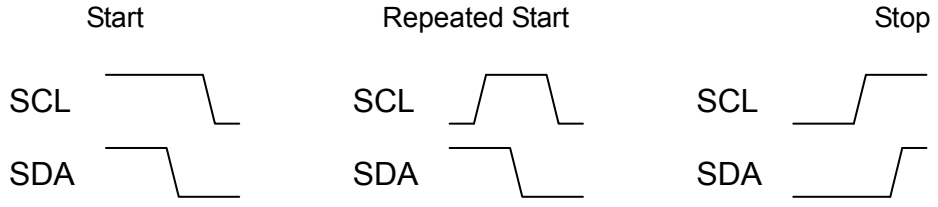
MSB							LSB	Function
A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	**0**	Reg0 : 00h
0	0	0	0	0	0	0	**1**	Reg1 : 01h
0	0	0	0	0	0	**1**	**0**	Reg2 : 02h
:	:	:	:	:	:	:	:	:
0	0	**1**	**0**	**1**	**1**	**0**	**1**	Reg29 : 2Dh
0	0	**1**	**0**	**1**	**1**	**1**	**0**	Reg30 : 2Eh
0	0	**1**	**0**	**1**	**1**	**1**	**1**	Reg31 : 2Fh

- Bus transmission format description

Format conforms to the I²C standard (see below).

- Start condition
- Repeated start condition
- Stop condition
- Write byte
- Read byte

Start, Repeated start, and stop conditions are defined under the conditions shown below.

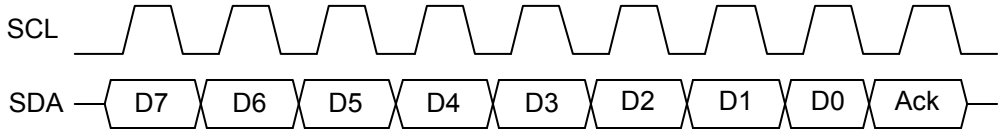


The I²C start, repeated start and stop conditions.

For detailed information such as timing, refer to the I²C specifications.

• 8Bit Write

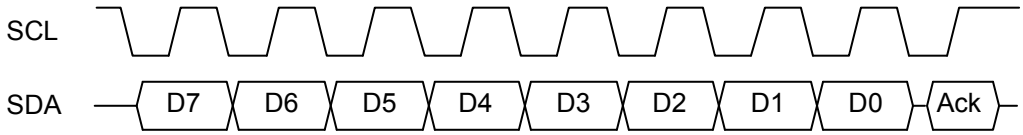
8Bit data is sent from the master microcomputer to LV25500.
For data bit, MSB first, LSB last.
Data transmission is synchronized with the SCL clock generated by the master IC. It is latched on the rising edge of SCL.
Data should not be changed while SCL is HIGH.
LV25500 outputs an ACK bit during the 8th and 9th of the falling edge of SCL.



Signal pattern of the I^2C byte write

• 8Bit Read

Read is similar with Write format but data direction is opposite.
8Bit data is sent from LV25500 to the master, and ACK is sent from the master to the LV25500.

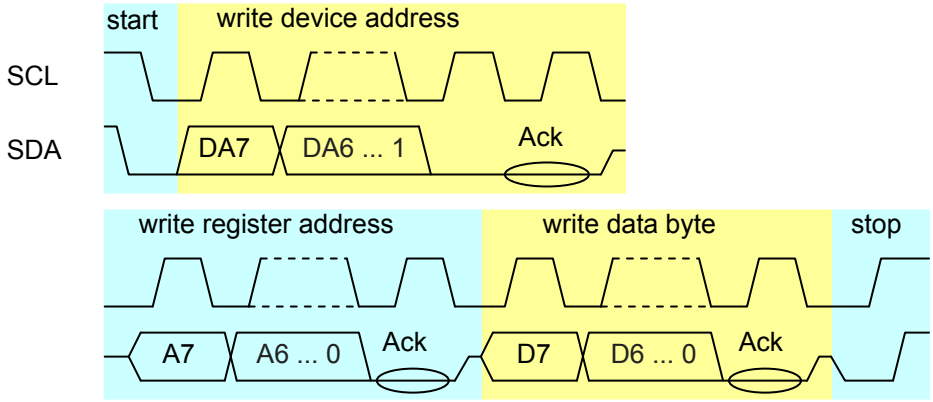


Signal pattern of the I^2C byte read

Serial clock SCL will be provided by the master side.
Data bits which are out from the LV25500 are synchronized with the falling edge. And the master side should latch the data bits on the rising edge.
LV25500 latches the ACK on the rising edge.

The following is the sequence that writes data D to the LV25500 register A. (In case of PULL DOWN)

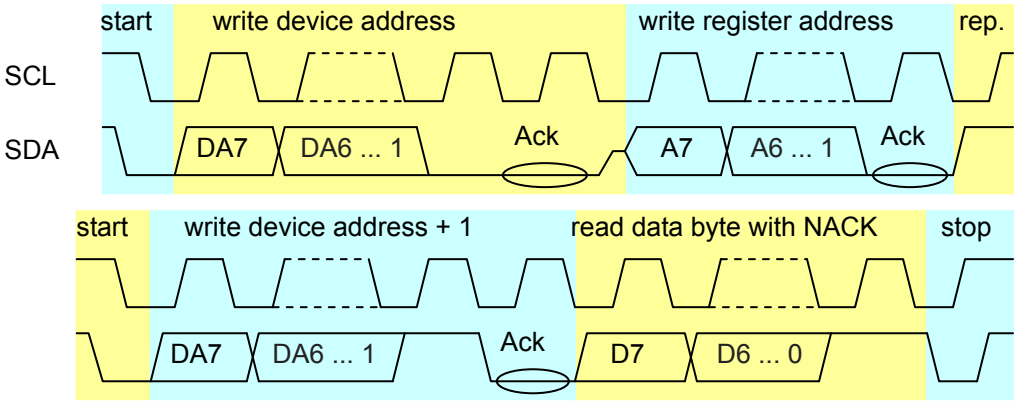
- **Write Sequence**
  - Start condition confirmation
  - Write device address(C0h)
  - Write address information A
  - Write Data D
  - Stop condition



Register write through I^2C

If more than one data was written, only the first data will be written.

- **Read Sequence**
  - Start condition confirmation
  - Write device address (C0h)
  - Write address information A
  - Repeated start condition (Or, stop + start sequence by the master)
  - Write device address +1 (C1h)
  - Read Register information D and send NACK (no more data to be read)
  - Stop condition



Register read through I^2C

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV25500PQA-NH	WQFN56 7x7, 0.4P (Pb-Free / Halogen Free)	2500 / Tape & Reel