Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LV5239TA

Bi-CMOS LSI

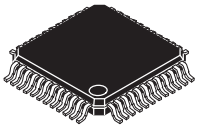
24-channel LED Driver

ON Semiconductor®

www.onsemi.com

Overview

The LV5239TA is a 24-channel LED driver IC which can select constant-current output or open drain output. 2-wire or 3-wire serial bus control can be selected by external pin.
Maximum current (3bit) and PWM-duty (8bit) are adjustable by SPI.
Up to 32 driver ICs can be connected by changing slave address.



TQFP48 EP 7x7, 0.5P

Function

- 24-channel output constant-current LED driver/open drain output LED driver (selected by external pin).
  Supports separate ON/OFF setting for each LED output, high withstand voltage (VOUT<42V).
- In the constant-current mode (OUTSCT: L), the reference current is set by the value of resistor connected to the external pin (RT1).
  Built-in D/A (3 bits) for switching current level … 6.40mA to 32.40mA (RGB drive).
  Constant current (I_O max=50mA) for full-color LEDs × 24 channels.
- In the open drain mode (OUTSCT: H), high current drive
  (I_O max=100mA) × 24 channels
- In the constant-current mode (OUTSCT: M)
  Only RGB7, RGB8 is open drain (I_O max=100mA)
- Luminance adjustment using internal PWM control (256 steps), It copes with independent PWM control for each LED output.
  - 8-bit PWM luminance dimming (0% to 99.6%)
- Selection of 2-wire or 3-wire serial bus control
  - Schmitt trigger input (3.3V/5V)
- Can set Slave address by external pin, can connect up to 32 driver ICs
- Input Power supply supports 12V
  - Internal reference output terminal (5V)
- Low current consumption
- Output malfunction protection circuits
  (thermal protection function, UVLO detection protection function, Power on RESET)

ORDERING INFORMATION

See detailed ordering and shipping information on page 28 of this data sheet.

February 2017 - Rev. 1

Publication Order Number :
LV5239TA/D

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		13.6	V
	VLED	VLED	42	V
	VREF	VREF	5.8	V
Output voltage	V_O max	LED off	42	V
Output current	I_O max	Open drain	100	mA
Allowable power dissipation	Pd max	Ta ≤ 25°C *	1.25	W
Operating temperature	Topr		−25 to +85	°C
Storage temperature	Tstg		−40 to +150	°C

* Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board. Exposed Die-pad area is not a substrate mounting.
[Warning] : If you should intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for a confirmation.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage range	V_{CC} op	SV_{CC}	3.0 to 12.8	V
	V_{LED} op	V_{LED}	3.0 to 42	V
	V_{REF} op	V_{REF}	3.0 to 5.5	V

[Warning] : The VLED terminal becomes the terminal for protection of the LED drive output. Please be connected to the power supply same as LED drive. When IC power supply (SVCC) and power supply of the LED or two kinds of power supply is more than it, please connect VLED to the highest potential and the power supply that it is.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V (=VREF)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Consumption current	$I_{CC}1$	LED off	1.8	2.3	2.9	mA
Reference current pin voltage	VRT	RT1=30kΩ	1.14	1.22	1.30	V
MAX output current	ΔIL	V_O=0.7 to 4.0V(Same channel line regulation)	−10			%
Between bits output current	$\Delta I_O L$	I_O=32.40mA (Between bits pairing characteristics)			5	%
Maximum LED driver output current 1	IMAX1	RT1=30kΩ LED OUTSCT= L	30.0	32.4	34.8	mA
LED output on resistance 1	Ron1	I_O = 10mA		10	20	Ω
OFF leak current	Ileak	LED OFF			10	μA
Power on RESET voltage	VPOR	The voltage that is canceled		2.5		V
Reset voltage	VRST	UVLO voltage		2.3		V
VREF voltage	VREF	VREF=open		4.9		V
VREF voltage	VREF1	V_{CC} = 6.0V, I_O = 10mA	4.7	5.1	5.4	V
Oscillator frequency	Fosc			1000		kHz

* Power on RESET
Reset all the data in the IC at the time of power activation. And it becomes the default setting.

* UVLO detection protection function
When SVCC decreases, it turns off LED output terminal.

* Thermal protection function
When a temperature in the IC rises, it turns off output terminal. When temperature falls, it returns by oneself.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Control circuit at Ta = 25°C, V_{CC} = 5.0V (=VREF)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
H level 1	VH1	Input H level OUTSCT	4.5		5.0	V
M level 1	VM1	Input M level OUTSCT	1.8		3.0	V
L level 1	VL1	Input L level OUTSCT	−0.2		0.5	V
H level 2	VH2	Input H level CTLSCT	3.5		5.0	V
L level 2	VL2	Input L level CTLSCT	−0.2		0.5	V
H level 3	VH3	Input H level RESET	4.0		5.0	V
L level 3	VL3	Input L level RESET	−0.2		1.0	V
H level 4	VH4	Input H level SCLK, SDATA, SDEN	4.0		5.0	V
L level 4	VL4	Input L level SCLK, SDATA, SDEN	−0.2		1.0	V
H level 5	VH5	Input H level A0 to A4	3.5		5.0	V
L level 5	VL5	Input L level A0 to A4	−0.2		0.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 3.3V (=VREF)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Consumption current	$I_{CC}1$	LED off		2.1		mA
Reference current pin voltage	VRT	RT1=30kΩ	1.14	1.22	1.30	V
MAX output current	ΔIL	V_O=0.7 to 4.0V(Same channel line regulation)	−10			%
Between bits output current	$\Delta I_O L$	I_O=32.40mA (Between bits pairing characteristics)			5	%
Maximum LED driver output current 1	IMAX1	RT1=30kΩ LED OUTSCT= L		32.4		mA
LED output on resistance 1	Ron1	I_O = 10mA		10	20	Ω
OFF leak current	Ileak	LED OFF			10	μA
Power on RESET voltage	VPOR	The voltage that is canceled		2.5		V
Reset voltage	VRST	UVLO voltage		2.3		V
VREF voltage	VREF	VREF=open		3.2		V
Oscillator frequency	Fosc			1000		kHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

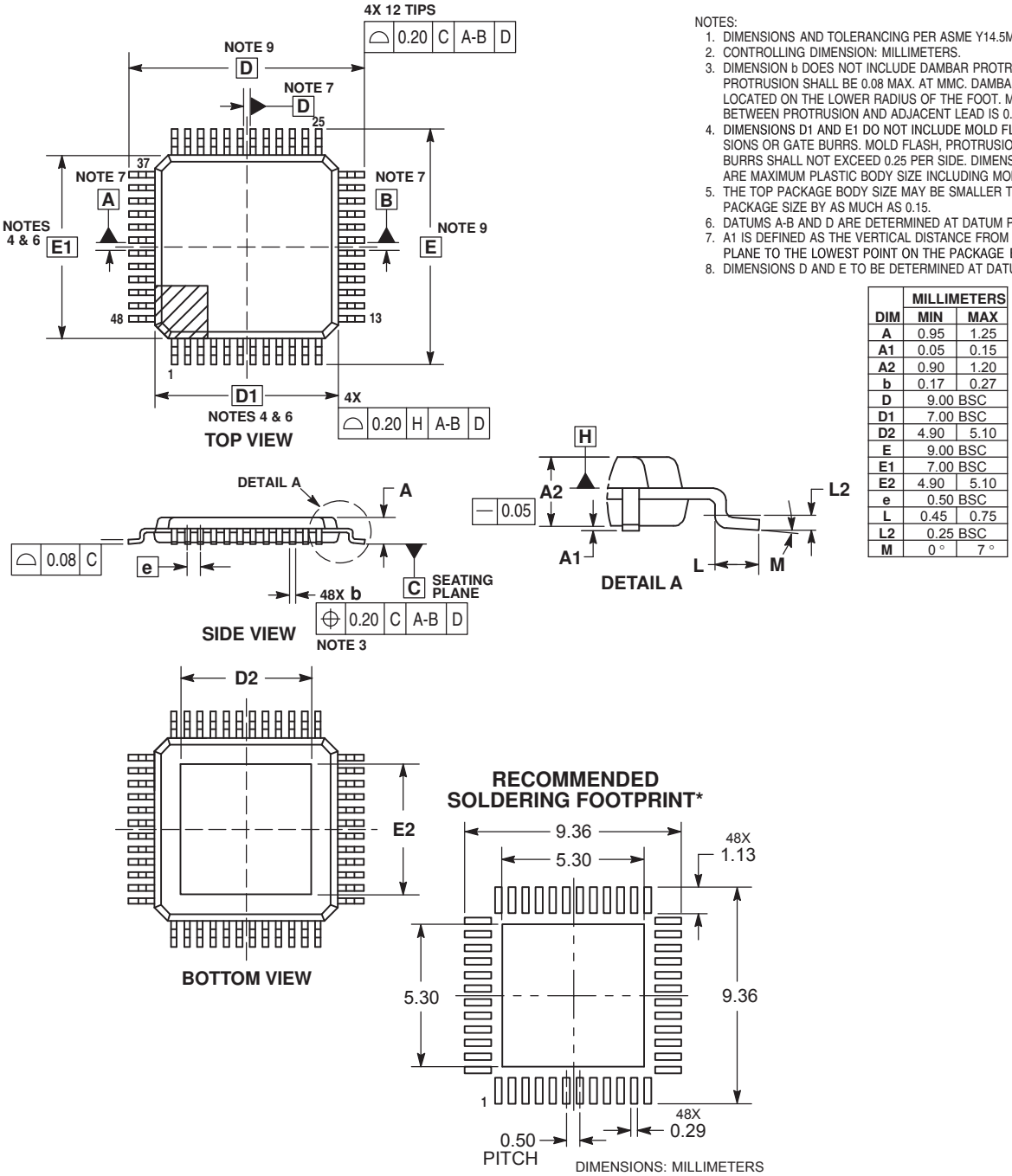
Control circuit at Ta = 25°C, V_{CC} = 3.3V (=VREF)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
H level 1	VH1	Input H level OUTSCT	2.8		3.3	V
M level 1	VM1	Input M level OUTSCT	1.2		1.7	V
L level 1	VL1	Input L level OUTSCT	−0.2		0.5	V
H level 2	VH2	Input H level CTLSCT	2.3		3.3	V
L level 2	VL2	Input L level CTLSCT	−0.2		0.5	V
H level 3	VH3	Input H level RESET	2.7		3.3	V
L level 3	VL3	Input L level RESET	−0.2		0.6	V
H level 4	VH4	Input H level SCLK, SDATA, SDEN	2.7		3.3	V
L level 4	VL4	Input L level SCLK, SDATA, SDEN	−0.2		0.6	V
H level 5	VH5	Input H level A0 to A4	2.3		3.3	V
L level 5	VL5	Input L level A0 to A4	−0.2		0.5	V

Package Dimensions

unit : mm

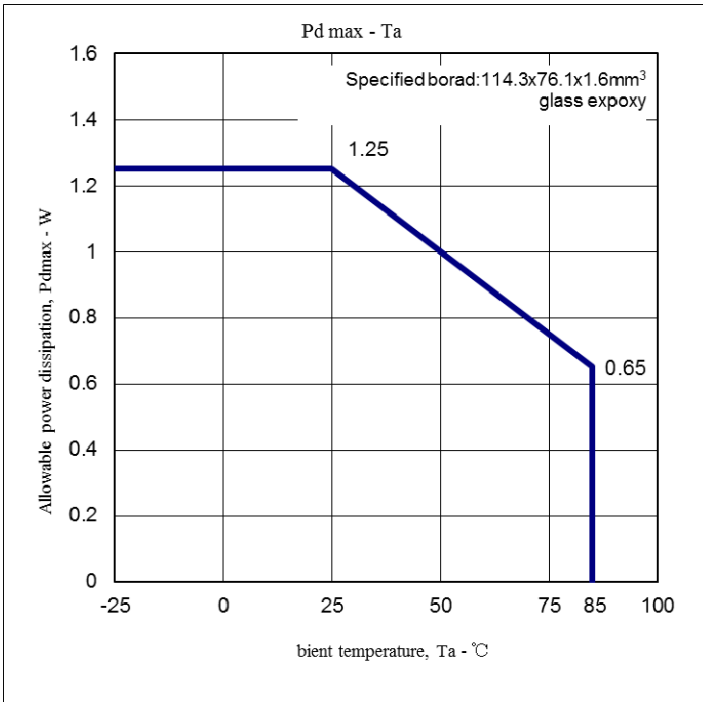
TQFP48 EP 7x7, 0.5P
CASE 932F
ISSUE C



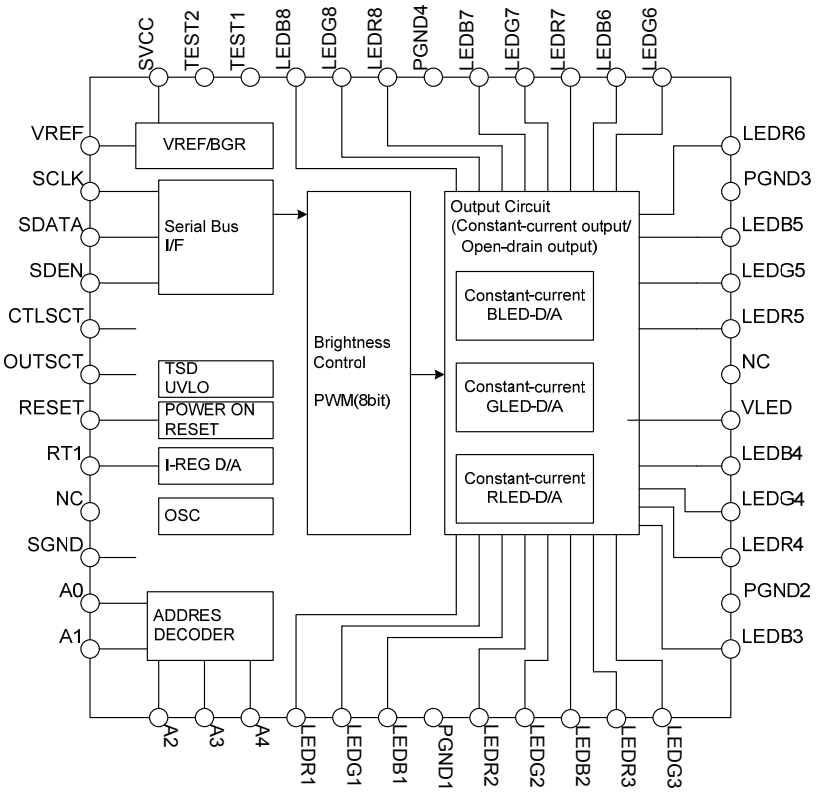
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

	MILLIMETERS	
DIM	MIN	MAX
A	0.95	1.25
A1	0.05	0.15
A2	0.90	1.20
b	0.17	0.27
D	9.00 BSC	
D1	7.00 BSC	
D2	4.90	5.10
E	9.00 BSC	
E1	7.00 BSC	
E2	4.90	5.10
e	0.50 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	7 °

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

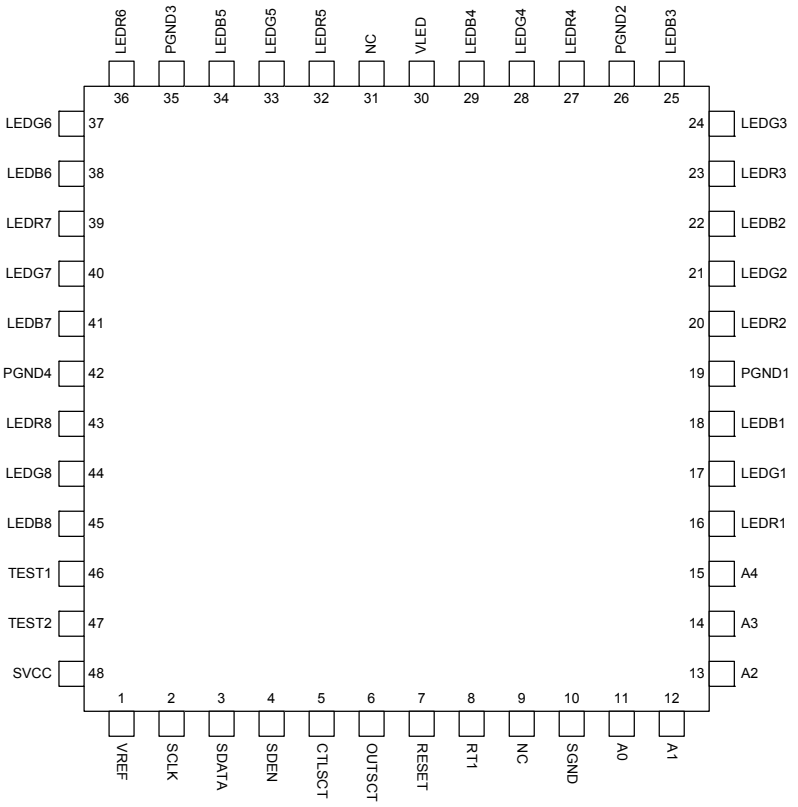


Block Diagram



[Warning] : The VLED terminal becomes the terminal for protection of the LED drive output. Please be connected to the power supply same as LED drive. When IC power supply (SVCC) and power supply of the LED or two kinds of power supply is more than it, please connect VLED to the highest potential and the power supply that it is.

Pin Assignment



Pin Descriptions

Pin No.	Pin name	I/O	Description	Pin Circuit
1	VREF	O	5V reference output pin	
2	SCLK	I	Serial clock signal input pin	TYPE1
3	SDATA	I	Serial data signal input pin	TYPE1
4	SDEN	I	Serial enable signal input pin	TYPE1
5	CTLSCT	I	Select pin for 2-wire or 3-wire serial bus (L: 3-wire serial, H: 2-wire serial)	TYPE2
6	OUTSCT	I	Output type switching control pin, refer to “OUTSCT Settings” on page8 in detail.	TYPE3
7	RESET	I	Reset signal input pin	TYPE4
8	RT1	O	LED current setting resistor connection pin. Maximum current = 1.22x800/RT	TYPE5
9	NC		No connection	
10	SGND	-	Analog circuit GND pin	
11	A0	I	Slave address setting pin, refer to “Slave address setting” on page14 in detail.	TYPE6
12	A1	I	Slave address setting pin, refer to “Slave address setting” on page14 in detail.	TYPE6
13	A2	I	Slave address setting pin, refer to “Slave address setting” on page14 in detail.	TYPE6
14	A3	I	Slave address setting pin, refer to “Slave address setting” on page14 in detail.	TYPE6
15	A4	I	Slave address setting pin, refer to “Slave address setting” on page14 in detail.	TYPE6
16	LEDR1	O	LEDR1 output pin	TYPE7
17	LEDG1	O	LEDG1 output pin	TYPE7
18	LEDB1	O	LEDB1 output pin	TYPE7
19	PGND1	-	GND pin dedicated for LED driver	
20	LEDR2	O	LEDR2 output pin	TYPE7
21	LEDG2	O	LEDG2 output pin	TYPE7
22	LEDB2	O	LEDB2 output pin	TYPE7
23	LEDR3	O	LEDR3 output pin	TYPE7
24	LEDG3	O	LEDG3 output pin	TYPE7
25	LEDB3	O	LEDB3 output pin	TYPE7
26	PGND2	-	GND pin dedicated for LED driver	
27	LEDR4	O	LEDR4 output pin	TYPE7

Continued on next page.

Continued from preceding page.

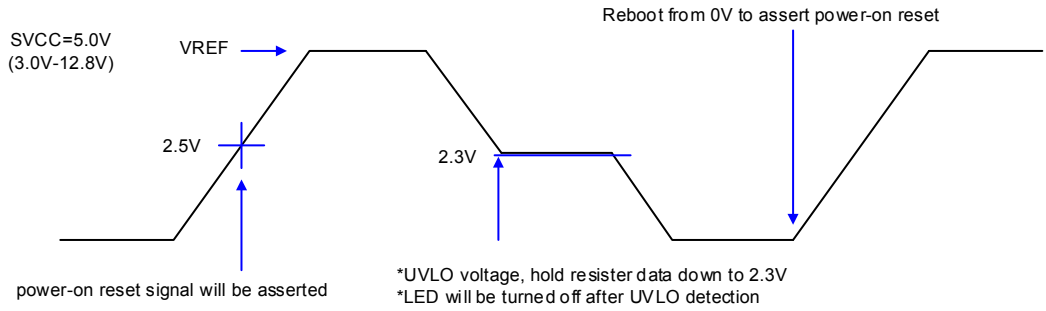
Pin No.	Pin name	I/O	Description	Pin Circuit
28	LEDG4	O	LEDG4 output pin	TYPE7
29	LEDB4	O	LEDB4 output pin	TYPE7
30	VLED		Output protection pin	
31	NC		No connection	
32	LEDR5	O	LEDR5 output pin	TYPE7
33	LEDG5	O	LEDG5 output pin	TYPE7
34	LEDB5	O	LEDB5 output pin	TYPE7
35	PGND3	-	GND pin dedicated for LED driver	
36	LEDR6	O	LEDR6 output pin	TYPE7
37	LEDG6	O	LEDG6 output pin	TYPE7
38	LEDB6	O	LEDB6 output pin	TYPE7
39	LEDR7	O	LEDR7 output pin	TYPE7
40	LEDG7	O	LEDG7 output pin	TYPE7
41	LEDB7	O	LEDB7 output pin	TYPE7
42	PGND4	-	GND pin dedicated for LED driver	
43	LEDR8	O	LEDR8 output pin	TYPE7
44	LEDG8	O	LEDG8 output pin	TYPE7
45	LEDB8	O	LEDB8 output pin	TYPE7
46	TEST1	I	Test1 pin (connected to GND)	TYPE8
47	TEST2	I	Test2 pin (connected to GND)	TYPE9
48	SV_{CC}	-	Power supply pin	

OUTSCT Settings

	LED Driver Output Pin	
OUTSCT pin	LED1, LED2, LED3, LED4, LED5, LED6	LED7,LED8
L=-0.2 to 0.3V	Constant current output Set maximum current by built-in D/A (3 bits) 6.40mA to 32.40mA, RT1=30kΩ (f=1MHz)	Constant current output Set maximum current by built-in D/A (3 bits) 6.40mA to 32.40mA, RT1=30kΩ (f=1MHz)
H=4.7 to 5.0V	Open drain output Set current by external resistor. R_{ON}=10Ω	Open drain output Set current by external resistor. R_{ON}=10Ω
M=1.8 to 3.0V	Constant current output Set maximum current by built-in D/A (3 bits) 6.40mA to 32.40mA, RT1=30kΩ (f=1MHz)	Open drain output Set current by external resistor. R_{ON}=10Ω

Power on RESET Settings

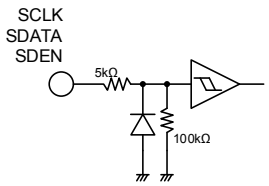
The data of built-in resister will be reset by power-on reset to prevent false operation.
Need to start up from SVCC=0V to assert power-on reset signal.
Please reboot Device from SVCC=0V.



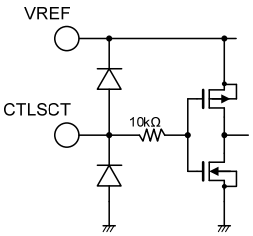
SPI will be available after 100usec from power-on reset.

Pin Circuit

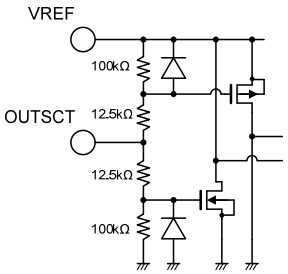
<TYPE1>
SCLK, SDATA, SDEN



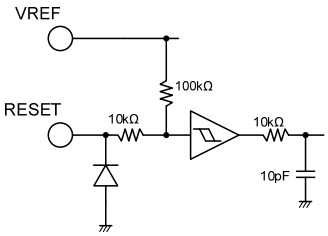
<TYPE2>
CTLSCT



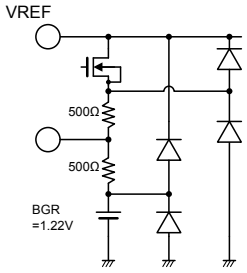
<TYPE3>
OUTSCT



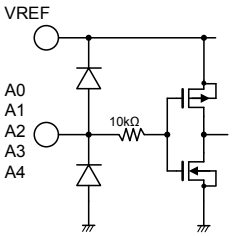
<TYPE4>
RESET



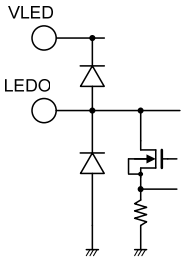
<TYPE5>
RT1



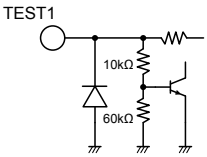
<TYPE6>
A0~A4



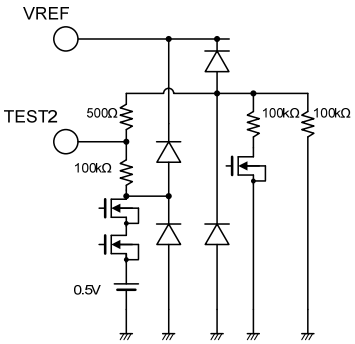
<TYPE7>
LEDR1~8, LEDG1~8, LEDB1~8



<TYPE8>
TEST1



<TYPE9>
TEST2



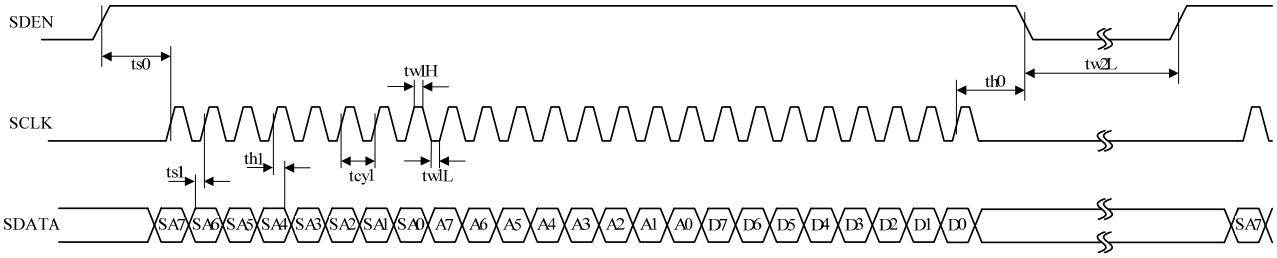
Serial Bus Communication Specifications

1) Serial bus transfer timing conditions

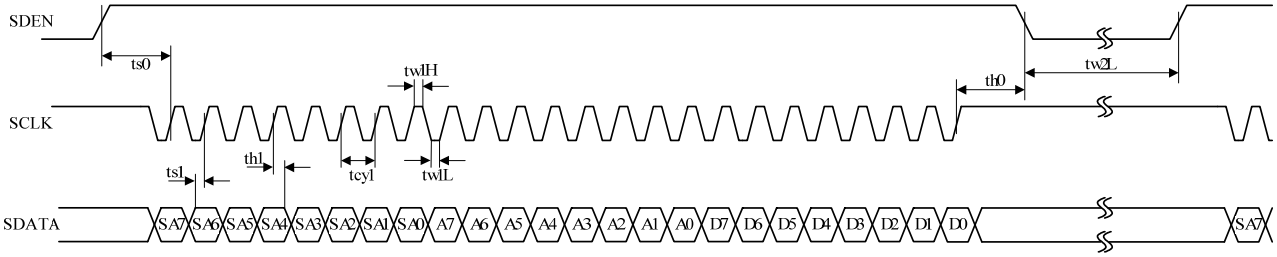
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle time	tcy1	SCLK clock period	200	-	-	ns
Data setup time	ts0	SDEN setup time relative to the rise of SCLK	90	-	-	ns
	ts1	SDATA setup time relative to the rise of SCLK	60	-	-	ns
Data hold time	th0	SDEN hold time relative to the fall of SCLK	200	-	-	ns
	th1	SDATA hold time relative to the fall of SCLK	60	-	-	ns
Pulse width	tw1L	Low period pulse width of SCLK	90	-	-	ns
	tw1H	High period pulse width of SCLK	90	-	-	ns
	tw2L	Low period pulse width of SDEN	1	-	-	μs

2) 3-wire serial bus transfer formats
3-wire; SCLK, SDATA, and SDEN.

SCLK starts from “L” level



SCLK starts from “H” level



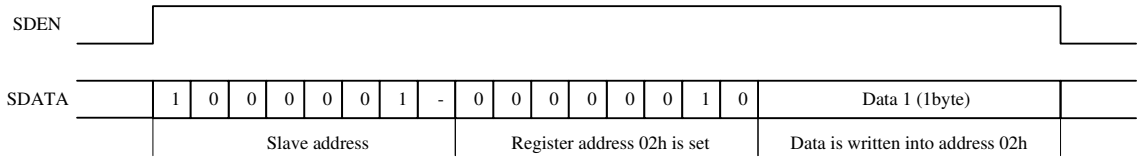
Minimum Data length : 24bits
Slave address (8bit) + Resister address (8bit) + Data (8bit)
Clock frequency : 5MHz or less
When 24 SCLK clock signals have been input during SDEN is High level, the SDATA is taken in at the rising edge of SCLK.
Note: If the number of SCLK clock is equal to or lower than 23, SDATA is not taken in. If it is 25 or more, the register address is automatically incremented and data will be taken in by every 1byte.

Data organization

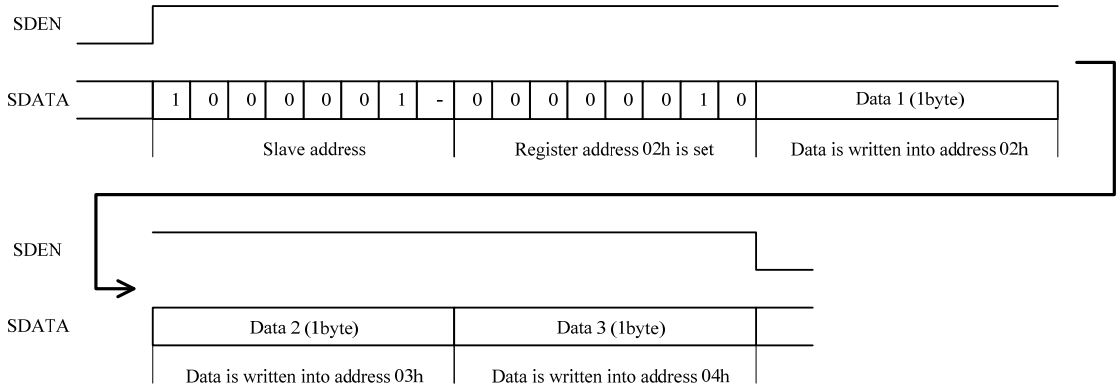
The slave address is assigned by the first byte, and the register address on the serial map is specified by the next byte. The third byte transfers the data to the address specified by the register address and if the data subsequently continues even after this, the register address is automatically incremented for the fourth and subsequent bytes. As a result, it is possible to send the data continuously from the specified addresses. Data of less than one byte is ignored. However, when the address reaches 1fh, the next byte to be transferred becomes 00h.

Serial data transfer example (slave address=1000 001-)

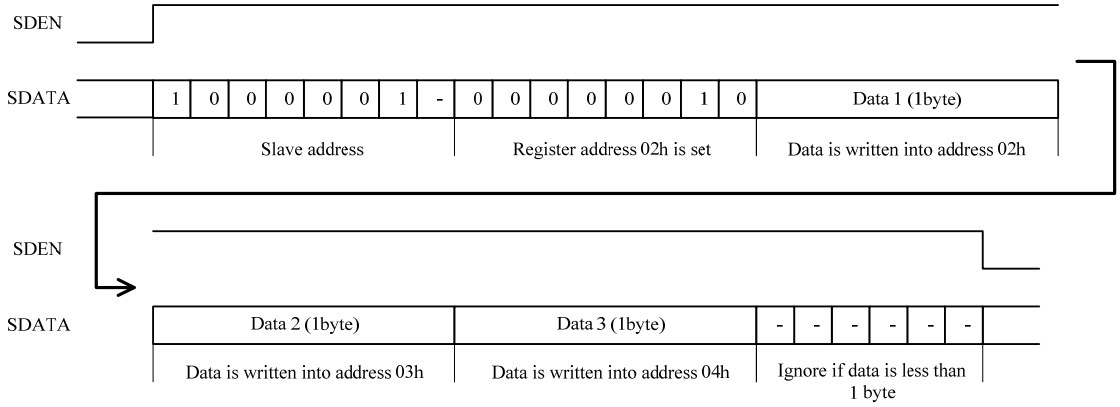
When I set register address 02h and write in data (the smallest data length)



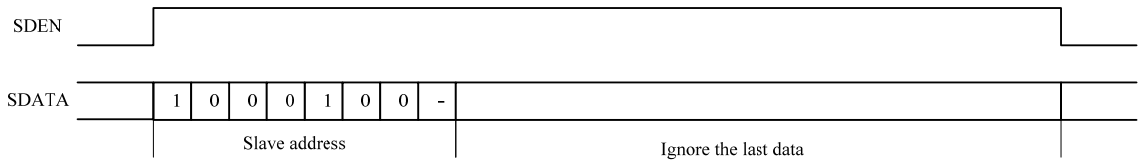
When I set register address 02h and write in data for 3 bytes



When I set register address 02h and write in data for 3 byte, and following data is less than a signal byte

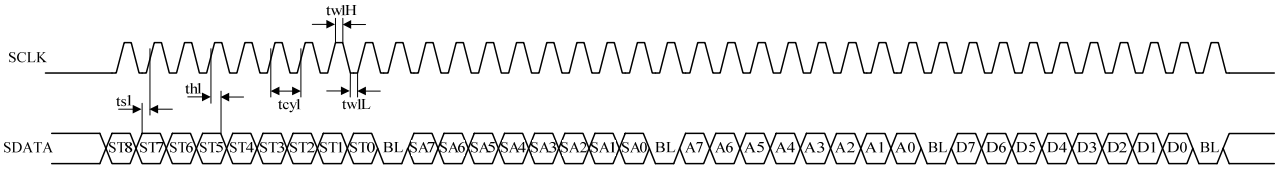


When slave address does not accord

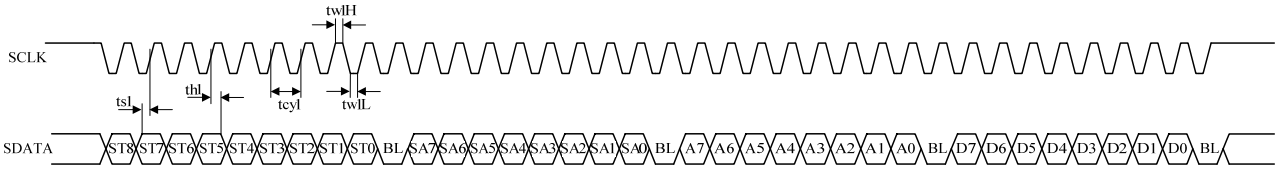


3) 2-wire serial bus transfer formats
2-wire ; SCLK, SDATA.

SCLK starts from “L” level



SCLK starts from “H” level



Minimum Data length : 37bits
Start condition (“111111111”) + BLANK (“0”) + Slave address (8bit) + BLANK + (“0”) +
Resister address (8bit) + BLANK (“0”) + Data (8bit) + BLANK (“0”)
Clock frequency : 5MHz or less

Note: When SCLK is less than 27th clock track, and BLANK is different from communication format such as “1”, after start detection, will not take in SDATA.
When SCLK is higher than 28th clock track, start detection is confirmed, register address is incremented every 1byte (8bit) + BLANK (“0”).

Data organization

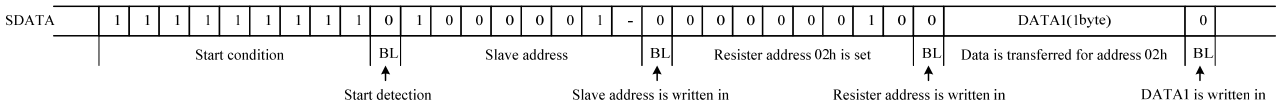
bit	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	BL	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	BL	A7	A6	A5	A4	A3	A2	A1	A0	BL	D7	D6	D5	D4	D3	D2	D1	D0	BL
SDATA	1	1	1	1	1	1	1	1	1	0	1	0						-	0									0									0
Parameter	Start condition									BLANK	Slave address								BLANK	Register address								BLANK	Data								BLANK

Fix slave address
Fix register address
Fix Data

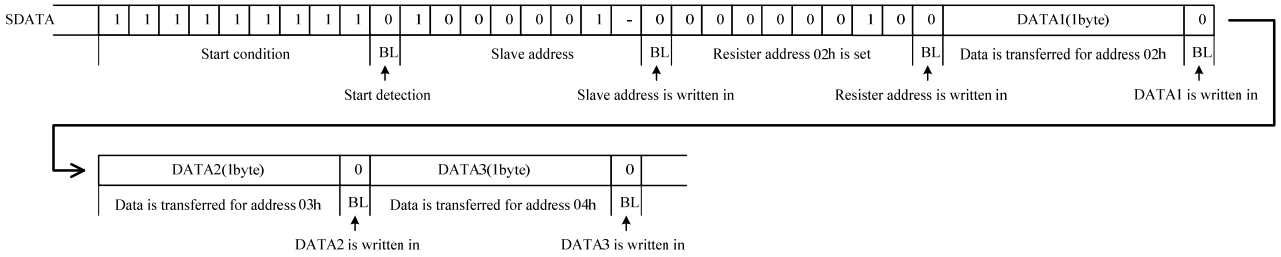
Even if SCLK and SDATA are in the state of standby or under receiving serial data, serial communication will restart by Start condition (“111111111”) + BLANK (“0”).
After start detection, slave address will be fixed after receiving BLANK”0”.
Same as slave address, register address will be fixed after receiving BLANK”0”.
The third byte is the register which is assigned by “Register address”, data will be fixed after receiving BLANK”0”.
When data continues after this, register address will be automatically incremented after the fourth byte and a data transfer is completed after receiving BLANK”0”.
Data can be set in series by automatic address increment. And after reached to “1fh”, next address will be “00h”.
If the BLANK is “1”, including slave address and register address, the single byte data just before it will not be written, also, subsequent data is will not be written until Start condition will be detected.

Serial data transfer example (slave address=1000 001-)

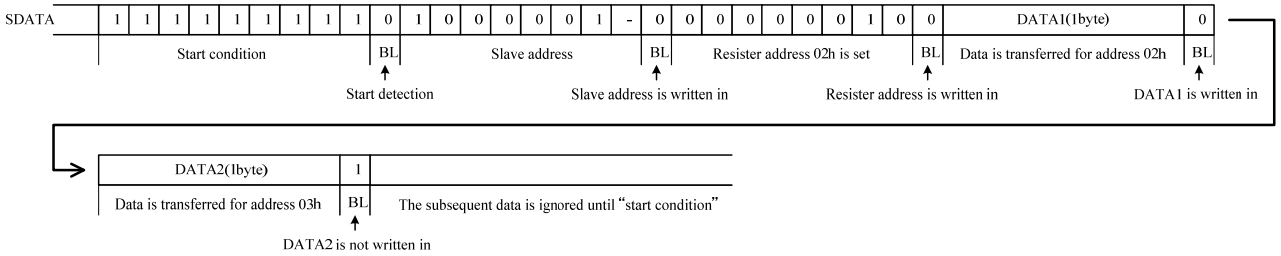
When I set register address 02h and write in data (the smallest data length)



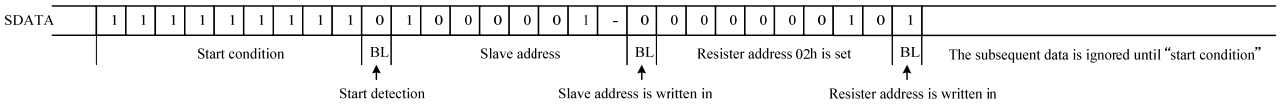
When I set register address 02h and write in data for 3 bytes



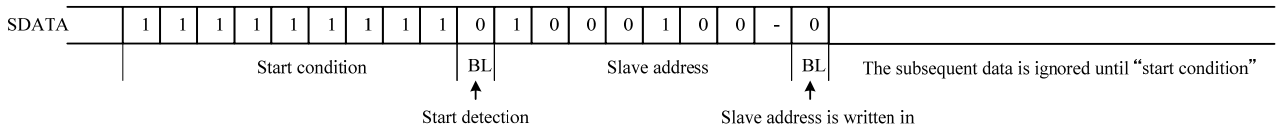
When I set register address 02h and write in data for 1 byte, and BLANK after the following byte in the case of “1”



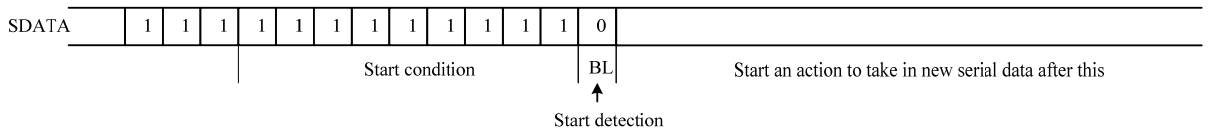
When I set register address 02h, but BLANK after the byte in the case of “1”



When slave address does not accord



SDATA continues more than 10bit; and in the case of 1 "" (start detection of this case)



Slave address setting

Slave address can set by A0~A4 pin as below

	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
ADDRESS	1	0	A4	A3	A2	A1	A0	-

Terminal PIN (Input)				
A4	A3	A2	A1	A0
L	L	L	L	L
L	L	L	L	H
L	L	L	H	L
L	L	L	H	H
L	L	H	L	L
L	L	H	L	H
L	L	H	H	L
L	L	H	H	H
L	H	L	L	L
L	H	L	L	H
L	H	L	H	L
L	H	L	H	H
L	H	H	L	L
L	H	H	L	H
L	H	H	H	L
L	H	H	H	H
H	L	L	L	L
H	L	L	L	H
H	L	L	H	L
H	L	L	H	H
H	L	H	L	L
H	L	H	L	H
H	L	H	H	L
H	L	H	H	H
H	H	L	L	L
H	H	L	L	H
H	H	L	H	L
H	H	L	H	H
H	H	H	L	L
H	H	H	L	H
H	H	H	H	L
H	H	H	H	H

SLAVE ADDRESS							
SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
1	0	0	0	0	0	0	-
1	0	0	0	0	0	1	-
1	0	0	0	0	1	0	-
1	0	0	0	0	1	1	-
1	0	0	0	1	0	0	-
1	0	0	0	1	0	1	-
1	0	0	0	1	1	0	-
1	0	0	0	1	1	1	-
1	0	0	1	0	0	0	-
1	0	0	1	0	0	1	-
1	0	0	1	0	1	0	-
1	0	0	1	0	1	1	-
1	0	0	1	1	0	0	-
1	0	0	1	1	0	1	-
1	0	0	1	1	1	0	-
1	0	0	1	1	1	1	-
1	0	1	0	0	0	0	-
1	0	1	0	0	0	1	-
1	0	1	0	0	1	0	-
1	0	1	0	0	1	1	-
1	0	1	0	1	0	0	-
1	0	1	0	1	0	1	-
1	0	1	0	1	1	0	-
1	0	1	0	1	1	1	-
1	0	1	1	0	0	0	-
1	0	1	1	0	0	1	-
1	0	1	1	0	1	0	-
1	0	1	1	0	1	1	-
1	0	1	1	1	0	0	-
1	0	1	1	1	0	1	-
1	0	1	1	1	1	0	-
1	0	1	1	1	1	1	-

:LV5239

Register Map

Addr.	Resister	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
00h	LEDR Current						I_LEDR[2:0]			LEDR current setting (LEDR1~LED8)
							0	0	0	approximately 20% of Imax (6.4mA @ RT=30k)
							0	0	1	approximately 31% of Imax (10.15mA @ RT=30k)
							0	1	0	approximately 43% of Imax (13.90mA @ RT=30k)
							0	1	1	approximately 54% of Imax (17.65mA @ RT=30k)
							1	0	0	approximately 66% of Imax (21.15mA @ RT=30k)
							1	0	1	approximately 77% of Imax (24.90mA @ RT=30k)
							1	1	0	approximately 88% of Imax (28.65mA @ RT=30k)
							1	1	1	Imax=1.22x800/RT (32.4mA @ RT=30k)
	PWM	PWM[2:0]								PWM cycle time setting
		0	0	0						0.5ms
		0	0	1						1.0ms
		0	1	0						2.0ms
		0	1	1						4.0ms
		1	0	0						8.0ms
		1	0	1						Inhibition
		1	1	0						Inhibition
		1	1	1						Inhibition
01h	LEDG Current						I_LEDG[2:0]			LEDG current setting (LEDG1~LEDG8)
							0	0	0	approximately 20% of Imax (6.4mA @ RT=30k)
							0	0	1	approximately 31% of Imax (10.15mA @ RT=30k)
							0	1	0	approximately 43% of Imax (13.90mA @ RT=30k)
							0	1	1	approximately 54% of Imax (17.65mA @ RT=30k)
							1	0	0	approximately 66% of Imax (21.15mA @ RT=30k)
							1	0	1	approximately 77% of Imax (24.90mA @ RT=30k)
							1	1	0	approximately 88% of Imax (28.65mA @ RT=30k)
							1	1	1	Imax=1.22x800/RT (32.4mA @ RT=30k)
02h	LEDB Current						I_LEDB[2:0]			LEDB current setting (LEDB1~8)
							0	0	0	approximately 20% of Imax (6.4mA @ RT=30k)
							0	0	1	approximately 31% of Imax (10.15mA @ RT=30k)
							0	1	0	approximately 43% of Imax (13.90mA @ RT=30k)
							0	1	1	approximately 54% of Imax (17.65mA @ RT=30k)
							1	0	0	approximately 66% of Imax (21.15mA @ RT=30k)
							1	0	1	approximately 77% of Imax (24.90mA @ RT=30k)
							1	1	0	approximately 88% of Imax (28.65mA @ RT=30k)
							1	1	1	Imax=1.22x800/RT (32.4mA @ RT=30k)
03h	PWM SEL LEDR	R8	R7	R6	R5	R4	R3	R2	R1	Select PWM or Full on for LEDR1~LEDR8
										0 : PWM mode 1 : Full on
04h	PWM SEL LEDG	G8	G7	G6	G5	G4	G3	G2	G1	Select PWM or Full on for LEDG1~LEDG8
										0 : PWM mode 1 : Full on
05h	PWM SEL LEDB	B8	B7	B6	B5	B4	B3	B2	B1	Select PWM or Full on for LEDB1~LEDB8
										0 : PWM mode 1 : Full on
06h	LEDR1 PWM Duty	R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	PWM duty setting for LEDR1
										00h : 0.0% Duty(%)=R1[7:0]/256 ffh : 99.6%

Continued on next page.

Continued from preceding page.

Addr.	Resister	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
07h	LEDG1 PWM	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	PWM duty setting for LEDG1
	Duty									00h : 0.0% Duty(%)=G1[7:0]/256 ffh : 99.6%
08h	LEDB1 PWM	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	PWM duty setting for LEDB1
	Duty									00h : 0.0% Duty(%)=B1[7:0]/256 ffh : 99.6%
09h	LEDR2 PWM	R2[7]	R2[6]	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	PWM duty setting for LEDR2
	Duty									00h : 0.0% Duty(%)=R2[7:0]/256 ffh : 99.6%
0ah	LEDG2 PWM	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	PWM duty setting for LEDG2
	Duty									00h : 0.0% Duty(%)=G2[7:0]/256 ffh : 99.6%
0bh	LEDB2 PWM	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	PWM duty setting for LEDB2
	Duty									00h : 0.0% Duty(%)=B2[7:0]/256 ffh : 99.6%
0ch	LEDR3 PWM	R3[7]	R3[6]	R3[5]	R3[4]	R3[3]	R3[2]	R3[1]	R3[0]	PWM duty setting for LEDR3
	Duty									00h : 0.0% Duty(%)=R3[7:0]/256 ffh : 99.6%
0dh	LEDG3 PWM	G3[7]	G3[6]	G3[5]	G3[4]	G3[3]	G3[2]	G3[1]	G3[0]	PWM duty setting for LEDG3
	Duty									00h : 0.0% Duty(%)=G3[7:0]/256 ffh : 99.6%
0eh	LEDB3 PWM	B3[7]	B3[6]	B3[5]	B3[4]	B3[3]	B3[2]	B3[1]	B3[0]	PWM duty setting for LEDB3
	Duty									00h : 0.0% Duty(%)=B3[7:0]/256 ffh : 99.6%
0fh	LEDR4 PWM	R4[7]	R4[6]	R4[5]	R4[4]	R4[3]	R4[2]	R4[1]	R4[0]	PWM duty setting for LEDR4
	Duty									00h : 0.0% Duty(%)=R4[7:0]/256 ffh : 99.6%
10h	LEDG4 PWM	G4[7]	G4[6]	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]	PWM duty setting for LEDG4
	Duty									00h : 0.0% Duty(%)=G4[7:0]/256 ffh : 99.6%
11h	LEDB4 PWM	B4[7]	B4[6]	B4[5]	B4[4]	B4[3]	B4[2]	B4[1]	B4[0]	PWM duty setting for LEDB4
	Duty									00h : 0.0% Duty(%)=B4[7:0]/256 ffh : 99.6%
12h	LEDR5 PWM	R5[7]	R5[6]	R5[5]	R5[4]	R5[3]	R5[2]	R5[1]	R5[0]	PWM duty setting for LEDR5
	Duty									00h : 0.0% Duty(%)=R5[7:0]/256 ffh : 99.6%
13h	LEDG5 PWM	G5[7]	G5[6]	G5[5]	G5[4]	G5[3]	G5[2]	G5[1]	G5[0]	PWM duty setting for LEDG5
	Duty									00h : 0.0% Duty(%)=G5[7:0]/256 ffh : 99.6%
14h	LEDB5 PWM	B5[7]	B5[6]	B5[5]	B5[4]	B5[3]	B5[2]	B5[1]	B5[0]	PWM duty setting for LEDB5
	Duty									00h : 0.0% Duty(%)=B5[7:0]/256 ffh : 99.6%
15h	LEDR6 PWM	R6[7]	R6[6]	R6[5]	R6[4]	R6[3]	R6[2]	R6[1]	R6[0]	PWM duty setting for LEDR6
	Duty									00h : 0.0% Duty(%)=R6[7:0]/256 ffh : 99.6%
16h	LEDG6 PWM	G6[7]	G6[6]	G6[5]	G6[4]	G6[3]	G6[2]	G6[1]	G6[0]	PWM duty setting for LEDG6
	Duty									00h : 0.0% Duty(%)=G6[7:0]/256 ffh : 99.6%

Continued on next page.

Continued from preceding page.

Addr.	Resister	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
17h	LEDB6 PWM	B6[7]	B6[6]	B6[5]	B6[4]	B6[3]	B6[2]	B6[1]	B6[0]	PWM duty setting for LEDB1
	Duty									00h : 0.0% Duty(%)=B6[7:0]/256 ffh : 99.6%
18h	LEDR7 PWM	R7[7]	R7[6]	R7[5]	R7[4]	R7[3]	R7[2]	R7[1]	R7[0]	PWM duty setting for LEDR7
	Duty									00h : 0.0% Duty(%)=R7[7:0]/256 ffh : 99.6%
19h	LEDG7 PWM	G7[7]	G7[6]	G7[5]	G7[4]	G7[3]	G7[2]	G7[1]	G7[0]	PWM duty setting for LEDG7
	Duty									00h : 0.0% Duty(%)=G7[7:0]/256 ffh : 99.6%
1ah	LEDB7 PWM	B7[7]	B7[6]	B7[5]	B7[4]	B7[3]	B7[2]	B7[1]	B7[0]	PWM duty setting for LEDB7
	Duty									00h : 0.0% Duty(%)=B7[7:0]/256 ffh : 99.6%
1bh	LEDR8 PWM	R8[7]	R8[6]	R8[5]	R8[4]	R8[3]	R8[2]	R8[1]	R8[0]	PWM duty setting for LEDR8
	Duty									00h : 0.0% Duty(%)=R8[7:0]/256 ffh : 99.6%
1ch	LEDG8 PWM	G8[7]	G8[6]	G8[5]	G8[4]	G8[3]	G8[2]	G8[1]	G8[0]	PWM duty setting for LEDG8
	Duty									00h : 0.0% Duty(%)=G8[7:0]/256 ffh : 99.6%
1dh	LEDB8 PWM	B8[7]	B8[6]	B8[5]	B8[4]	B8[3]	B8[2]	B8[1]	B8[0]	PWM duty setting for LEDB8
	Duty									00h : 0.0% Duty(%)=B8[7:0]/256 ffh : 99.6%

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5239TAZ-NH	TQFP48 EP 7x7, 0.5P (Pb-Free / Halogen Free)	1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF