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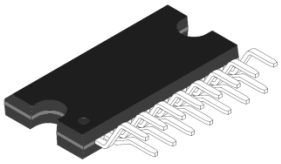
LV56851UV

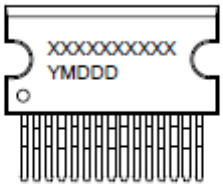
Linear Voltage Regulator, Multiple-Output, System Power Supply IC, for Automotive Infotainment System

ON Semiconductor®
www.onsemi.com



HZIP15

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " •", may or may not be present.

ORDERING INFORMATION

Ordering Code:
LV56851UV-XH

Package
HZIP15
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
720 / Tube

Overview

The LV56851UV is a multiple output linear voltage regulator IC, which allows reduction of quiescent current. The LV56851UV is specifically designed to address automotive infotainment systems power supply requirements.

The LV56851UV integrates 5 linear regulator outputs, 1 high side power switch, I2C-bus communication, ACC detection, battery voltage detection, over-current limiter, overvoltage protection and thermal shut down.

Features

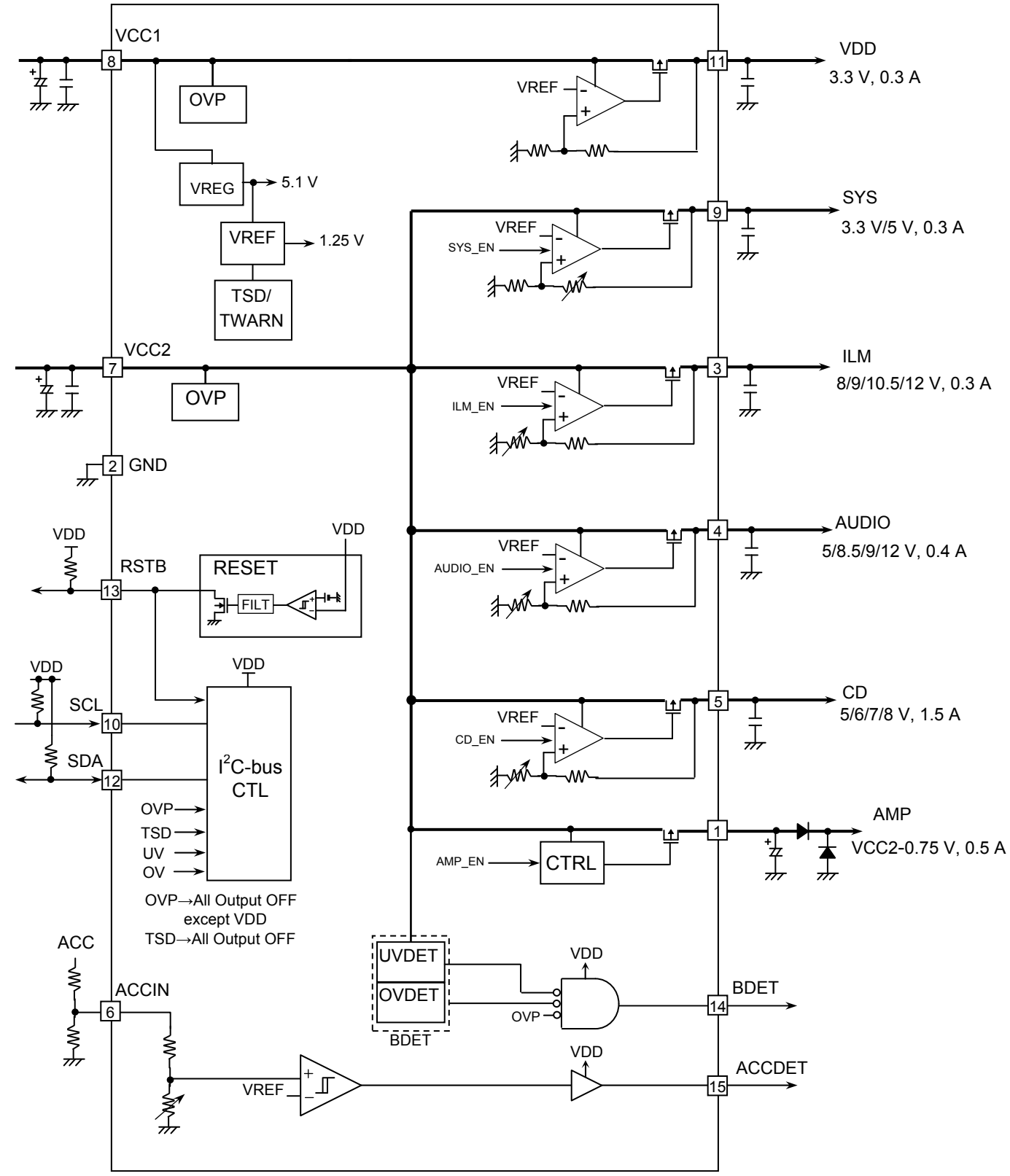
- Low consumption current: 60μA (typ, VDD output is in operation)
- 5 regulator outputs
  VDD for microcontroller: 3.3 V,Iomax: 300 mA
  For system: 3.3/5 V, Iomax: 300 mA
  For audio: 5/8.5/9/12 V, Iomax: 400 mA
  For illumination: 8/9/10.5/12 V, Iomax: 300 mA
  For CD: 5/6/7/8 V, Iomax: 1500 mA
- 1 high side switch
  AMP: Imax: 500 mA, voltage difference between input and output: 0.75 V
- ACC detection circuit
  Detection Voltage 2.7/3.2/3.6/4.2 V
- Battery voltage detection (BDET) : VCC2
  Low voltage detection(UVDET): 6.5/7.5(hys=0.5 V or 1.5 V)/8 V
  Over voltage detection(OVDET): detection voltage 18 V
- I2C-bus communication interface
  Each output except VDD is independently enabled/disabled. SYS/ILM/CD/AUDIO/ACC/UV voltage setting.
  Read back supported: Output voltage setting, Output over-current, Detections(ACC/UV/OVDET/OVP/TWARN)
- RESET
  Detection Voltage 2.8 V(typ, 0.85*VDD), N-MOS Open-Drain output
- Supply input
  VCC1: For internal reference voltage, control circuitry, VDD output.
  VCC2: For AUDIO/ILM/CD/AMP/SYS
- Over-current protection
- Overvoltage protection(OVP): VCC1,VCC2 Typ 21 V
  (All outputs except VDD are turned off)
- Thermal shutdown: Typ 175°C , Thermal Warning: Typ 140°C
- Package : HZIP15
- AEC-Q100 (Grade 3) Qualified and PPAP capable

Typical Applications

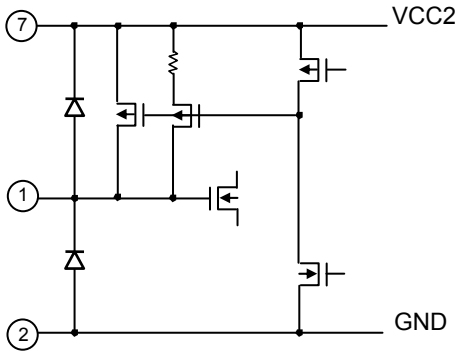
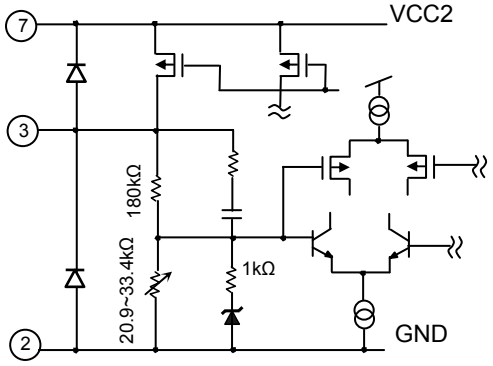
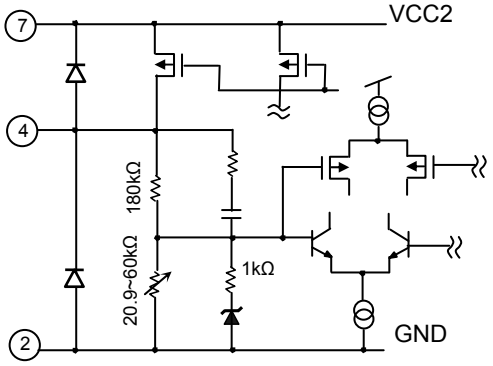
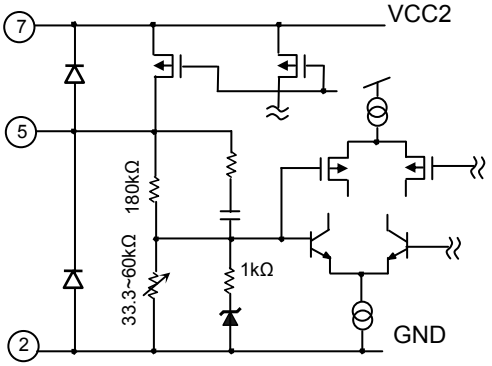
- Automotive infotainment

* I^2C Bus is a trademark of Philips Corporation.

BLOCK DIAGRAM



PIN EQUIVALENT CIRCUITS

Pin #	Pin name	Function	Equivalent circuit
1	AMP	AMP output VCC2-0.75 V	
2	GND	GND	
3	ILM	ILM output 8 V~12 V	
4	AUDIO	AUDIO output 5 V~12 V	
5	CD	CD output 5 V~8 V	

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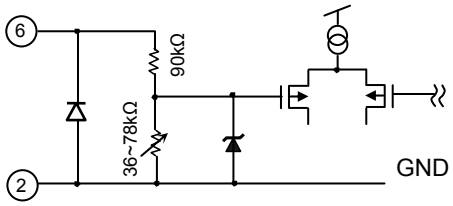
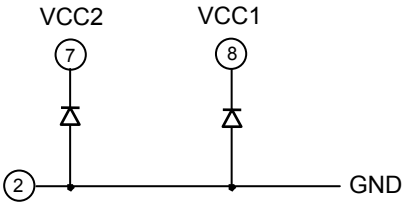
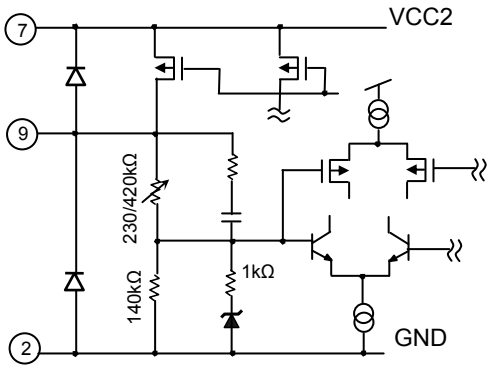
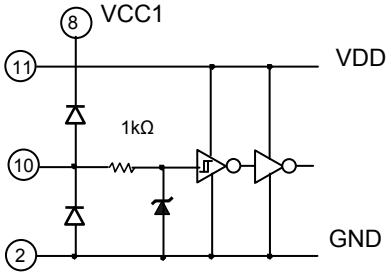
Pin #	Pin name	Function	Equivalent circuit
6	ACCIN	ACC detection input	
7	VCC2	Supply terminal	
8	VCC1	Supply terminal	
9	SYS	SYS output 3.3 V/5 V	
10	SCL	I^{2}C-bus clock input	

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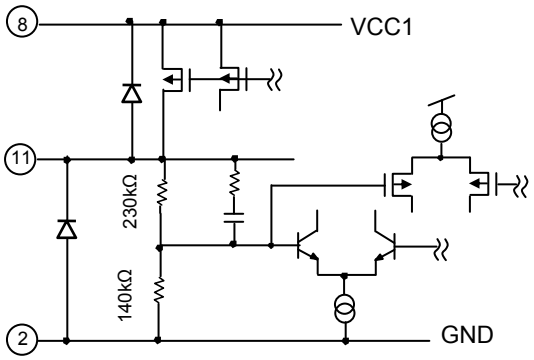
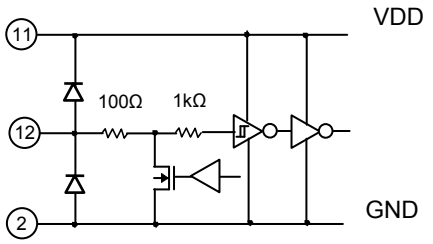
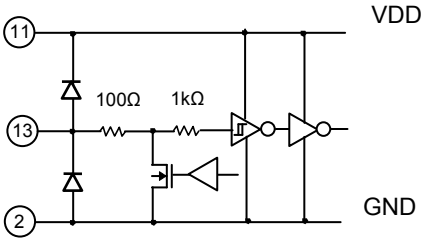
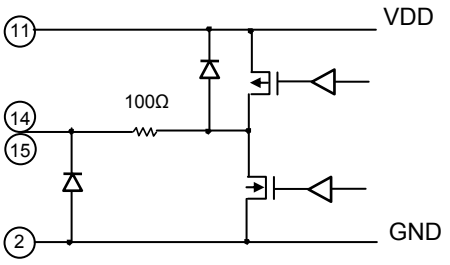
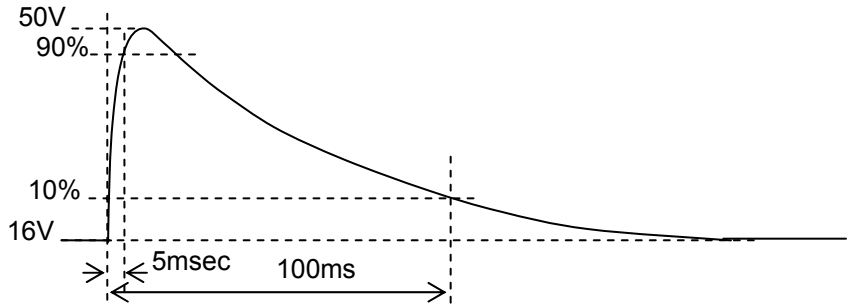
Pin #	Pin name	Function	Equivalent circuit
11	VDD	VDD output 3.3 V	
12	SDA	I^2C-bus data input	
13	RSTB	RESET Open-drain output	
14	BDET	BDET output	
15	ACCDET	ACCDET output	

MAXIMUM RATINGS / Ta = 25°C (Note 1)

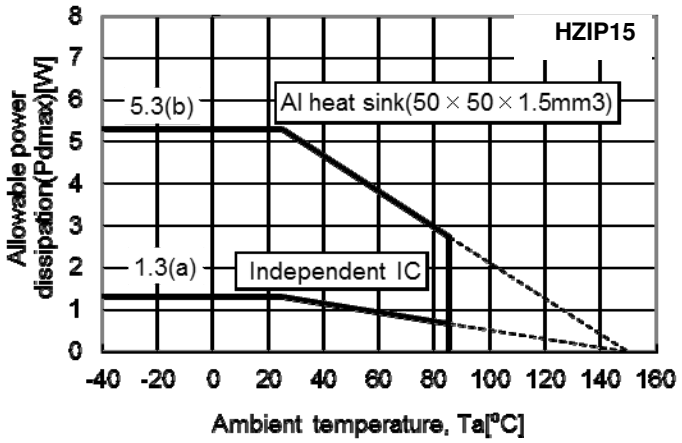
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc max	VCC1,VCC2	36	V
Input voltage	Vio max	SDA,SCL,ACCDET,BDET,RSTB,SYS,VDD ILM,AUDIO,CD ACCIN, AMP	7 14 36	V
Allowable power dissipation	Pd max Ta ≤ 25°C	-Independent IC -Al heatsink (50 * 50 * 1.5 mm^3) is used -Size of heatsink: infinite	1.3 5.3 26	W
Peak supply voltage	Vcc peak	VCC1/VCC2/ACCIN • See the test waveform below	50	V
Operating ambient temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C
Junction temperature	Tjmax		+150	°C

1. Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

• Waveform of surge test (VCC1,VCC2,ACCIN)



• Allowable power dissipation derating curve



(a) Independent IC
(b)Aluminum heat-sink (50×50×1.5 mm3)
Heat-sink tightening condition
tightening torque: 39 N•cm ,
with silicone grease

RECOMMENDED OPERATING RANGES at Ta = 25°C (Note 2)

■VCC1

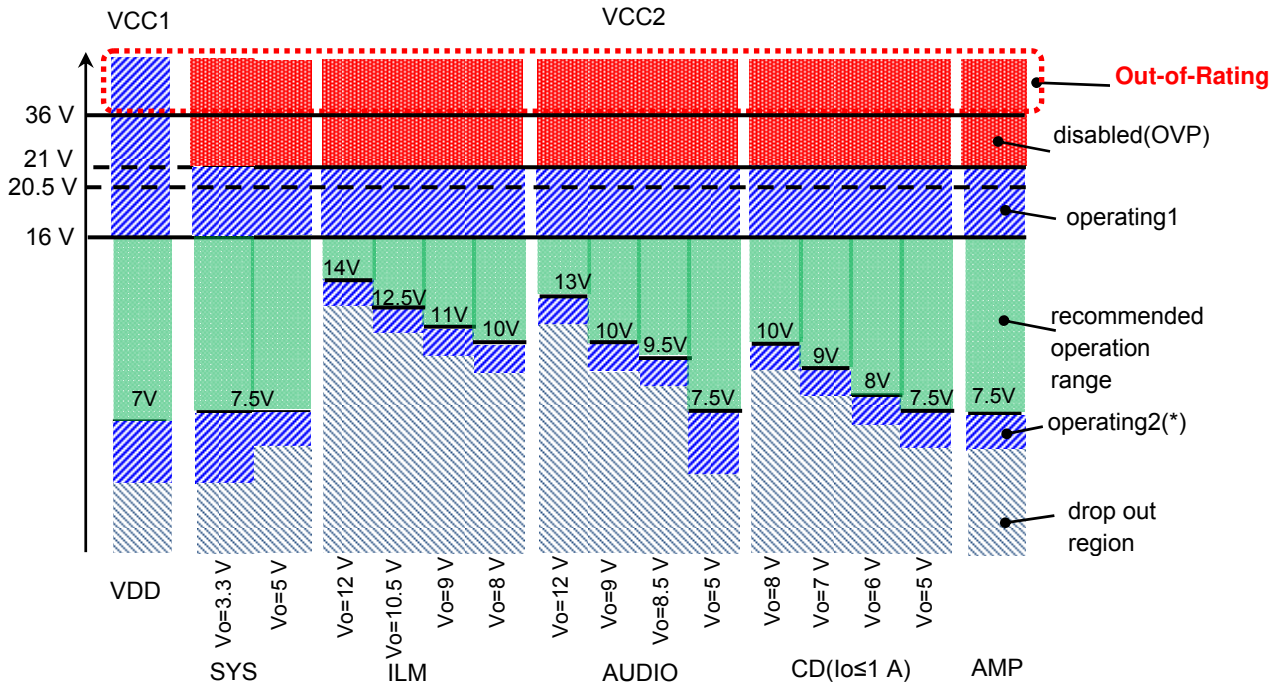
Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage1	VCCop1	VDD output	7 to 16	V

■VCC2

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage2	VCCop2	ILM(10.5 V) output ILM(8 V) output	12.5 to 16 10 to 16	V
Operating supply voltage3	VCCop3	AUDIO(8.5 V) output	9.5 to 16	V
Operating supply voltage4	VCCop4	CD(8V) output(Io=1.5 A) CD(8V) output(Io≤ 1 A)	10.5 to 16 10 to 16	V
Operating supply voltage5	VCCop5	AMP output	7.5 to 16	V
Operating supply voltage6	VCCop6	SYS output	7.5 to 16	V

2. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

• “Maximum Rating” and “Recommended operating range”



(*) Each lower limit value is determined by “Output voltage”-“Dropout voltage”.

ELECTRICAL CHARACTERISTICS at Ta = 25°C(Note 4), VCC1=VCC2=14.4 V unless otherwise noted. (Note 3)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent current	Icc	VDD w/out load, ACCIN=0V I^2C register Gr0/Gr1/Gr2=00h		60	100	μA
VDD output (3.3 V)						
Output voltage	Vo1	Io1=200 mA	3.13	3.3	3.47	V
Output current	Io1	Vo1≥ 3.1 V	300			mA
Line regulation	$\Delta Vo_{LN}1$	7.5 V<VCC1<16 V, Io1=200 mA		30	90	mV
Load regulation	$\Delta Vo_{LD}1$	1 mA<Io1<200 mA		70	150	mV
Dropout voltage	$V_{DROP}1$	Io1=200 mA		0.5	1.0	V
Ripple rejection (Note 5)	$R_{REJ}1$	f=120 Hz, VCC1=0.5 Vpp Io1=200 mA	40	50		dB
RESET						
Reset voltage	Vrst0	VDD falling	2.7	2.8	2.94	V
	Vrst	As a ratio of Vo1, VDD falling		85		%
Hysteresis voltage	Vrshs	As a ratio of Vo1		1.6		%
Detection Delay1	Td1	H to L, VDD=Vrst+0.4 V to Vrst-0.4 V		25		μsec
Detection Delay2	Td2	L to H, VDD=Vrst-0.4 V to Vrst+0.4 V		100		μsec
SYS output (3.3 V/5 V) ; SYS_EN=1						
Output voltage 1	Vo21	Io2=200 mA, SYS_V=0	3.13	3.3	3.47	V
Output voltage 2	Vo22	Io2=200 mA, SYS_V=1	4.75	5.0	5.25	V
Output current	Io2	Vo21≥3.1 V, Vo22≥4.7 V	300			mA
Line regulation	$\Delta Vo_{LN}2$	7.5 V<VCC2<16 V, Io2=200 mA		30	90	mV
Load regulation	$\Delta Vo_{LD}2$	1 mA<Io2<200 mA		70	150	mV
Dropout voltage	$V_{DROP}2$	Io2=200 mA		0.4	0.8	V
Ripple rejection (Note 5)	$R_{REJ}2$	f=120 Hz, VCC2=0.5 Vpp Io2=200 mA	40	50		dB
ILM output (8-12 V); ILM_EN=1						
Output voltage 1	Vo31	Io3=200 mA, ILM_V[1:0]=00	7.6	8.0	8.4	V
Output voltage 2	Vo32	Io3=200 mA, ILM_V[1:0]=01	8.55	9.0	9.45	V
Output voltage 3	Vo33	Io3=200 mA, ILM_V[1:0]=10	9.97	10.5	11.03	V
Output voltage 4	Vo34	Io3=200 mA, ILM_V[1:0]=11	11.4	12	12.6	V
Output current	Io3		300			mA
Line regulation	$\Delta Vo_{LN}3$	Vo+2 V<VCC2<16 V, Io3=200 mA		30	90	mV
Load regulation	$\Delta Vo_{LD}3$	1 mA<Io3<200 mA		70	150	mV
Dropout voltage	$V_{DROP}3$	Io3=200 mA		0.6	1.05	V
Ripple rejection (Note 5)	$R_{REJ}3$	f=120 Hz ,Io3=200 mA	40	50		dB

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CD output (5-8 V); CD_EN=1						
Output voltage 1	Vo41	Io4=1000 mA, CD_V[1:0]=00	4.75	5.0	5.25	V
Output voltage 2	Vo42	Io4=1000 mA, CD_V[1:0]=01	5.7	6.0	6.3	V
Output voltage 3	Vo43	Io4=1000 mA, CD_V[1:0]=10	6.65	7.0	7.35	V
Output voltage 4	Vo44	Io4=1000 mA, CD_V[1:0]=11	7.6	8.0	8.4	V
Output current	Io4	Vo41≥4.7 V, V44≥7.6 V	1500			mA
Line regulation	$\Delta Vo_{LN}4$	Vo+2 V<Vcc2<16 V,Io4=1000 mA		50	100	mV
Load regulation	$\Delta Vo_{LD}4$	10 mA<Io4<1000 mA		100	200	mV
Dropout voltage 1	$V_{DROP}4$	Io4=1000 mA		0.9	1.5	V
Dropout voltage 2	$V_{DROP}4'$	Io4=500 mA		0.45	0.75	V
Ripple rejection (Note 5)	$R_{REJ}4$	f=120 Hz ,Io4=1000 mA	40	50		dB
AUDIO output (5-12 V); AUDIO_EN=1						
Output voltage 1	Vo51	Io5=200 mA, AUD_V[1:0]=00	4.75	5.0	5.25	V
Output voltage 2	Vo52	Io5=200 mA, AUD_V[1:0]=01	8.13	8.5	8.87	V
Output voltage 3	Vo53	Io5=200 mA, AUD_V[1:0]=10	8.55	9.0	9.45	V
Output voltage 4	Vo54	Io5=200 mA, AUD_V[1:0]=11	11.4	12	12.6	V
Output current	Io5		400			mA
Line regulation	$\Delta Vo_{LN}5$	Vo+1 V<VCC2<16 V,Io5=200 mA		30	90	mV
Load regulation	$\Delta Vo_{LD}5$	1 mA<Io5<200 mA		70	150	mV
Dropout voltage	$V_{DROP}5$	Io5=200 mA		0.3	0.6	V
Ripple rejection (Note 5)	$R_{REJ}5$	f=120 Hz, Io5=200 mA	40	50		dB
AMP HS-SW; AMP_EN=1						
Output voltage	Vo6	Io6=500 mA	Vcc2-1.5	Vcc2-0.75		V
Output current	Io6	Vo6≥VCC2-1.5 V	500			mA
ACC detection						
Detection voltage 1	Vacc1	ACC_V[1:0]=00, ACCIN falling	2.62	2.7	2.78	V
Detection voltage 2	Vacc2	ACC_V[1:0]=01, ACCIN falling	3.1	3.2	3.3	V
Detection voltage 3	Vacc3	ACC_V[1:0]=10, ACCIN falling	3.49	3.6	3.71	V
Detection voltage 4	Vacc4	ACC_V[1:0]=11, ACCIN falling	4.07	4.2	4.33	V
Release voltage 1	Vaccr1	ACC_V[1:0]=00, ACCIN rising	2.81	2.9	2.99	V
Release voltage 2	Vaccr2	ACC_V[1:0]=01, ACCIN rising	3.3	3.4	3.5	V
Release voltage 3	Vaccr3	ACC_V[1:0]=10, ACCIN rising	3.68	3.8	3.92	V
Release voltage 4	Vaccr4	ACC_V[1:0]=11, ACCIN rising	4.26	4.4	4.54	V
Threshold hysteresis	Vachs			0.2		V

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Under-Voltage detection(UVDET)						
detection voltage 1	Vuv1	VCC2 falling, UVD_V[1:0]=00	6.3	6.5	6.7	V
detection voltage 2	Vuv2	VCC2 falling, UVD_V[1:0]=01	7.27	7.5	7.73	V
detection voltage 3	Vuv3	VCC2 falling, UVD_V[1:0]=10	7.27	7.5	7.73	V
detection voltage 4	Vuv4	VCC2 falling, UVD_V[1:0]=11	7.76	8.0	8.24	V
release voltage 1	Vuvr1	VCC2 rising, UVD_V[1:0]=00	6.79	7.0	7.21	V
release voltage 2	Vuvr2	VCC2 rising, UVD_V[1:0]=01	7.76	8.0	8.24	V
release voltage 3	Vuvr3	VCC2 rising, UVD_V[1:0]=10	8.73	9.0	9.27	V
release voltage 4	Vuvr4	VCC2 rising, UVD_V[1:0]=11	8.24	8.5	8.76	V
detection hysteresis 1	Vuvhs1	UVD_V[1:0]=00		0.5		V
detection hysteresis 2	Vuvhs2	UVD_V[1:0]=01		0.5		V
detection hysteresis 3	Vuvhs3	UVD_V[1:0]=10		1.5		V
detection hysteresis 4	Vuvhs4	UVD_V[1:0]=11		0.5		V
Over-Voltage detection(OVDET)						
detection voltage	Vovd	VCC2 rising	17	18	19	V
detection hysteresis	Vodhys			0.5		V
Over-Voltage protection(OVP)						
detection voltage	Vovp	VCC1/VCC2 rising, output disabled		21		V
detection hysteresis	Vovhys			0.5		V
CMOS Output(ACCDET, BDET)						
“H” voltage	VflgH	Isource=1 mA		VDD-0.3	VDD	V
“L” voltage	VflgL	Isink=1 mA		0.3	0.4	V
RSTB :						
Input “L” voltage	Vilrs	Internal circuit reset	0		0.4	V
Input “H” voltage	Vihrs	Internal circuit reset released	2.8	VDD	VDD+0.3	V
“L” voltage	VrsbL	Isink=1 mA		0.3	0.4	V
I^2C-bus I/F; SCL,SDA						
Input “L” voltage	Vils		0		0.4	V
Input “H” voltage	Vihs		2.8	VDD	VDD+0.3	V
SDA “L” voltage	Vols	Isink=1 mA, ACK or data read		0.3	0.4	V

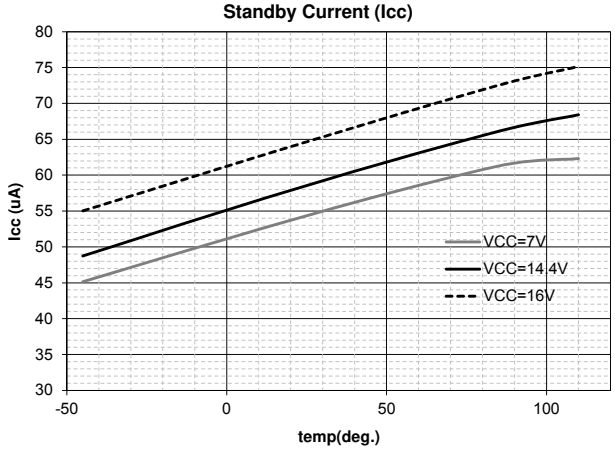
3. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. All the specification is defined based on the tests performed under the conditions where Tj and Ta(=25°C) are almost equal. These tests were performed with pulse load to minimize the increase of junction temperature (Tj).

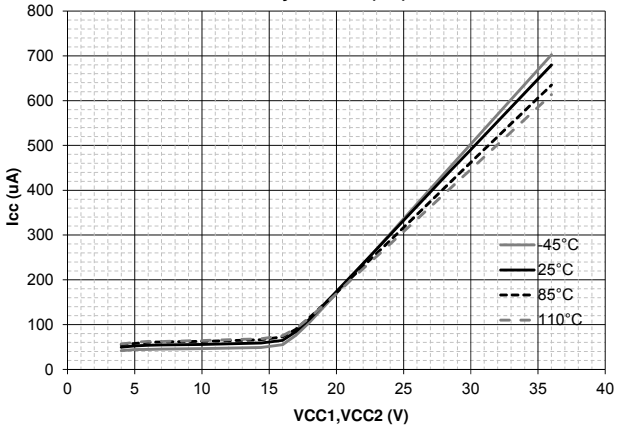
5. Guaranteed by design

TYPICAL CHARACTERISTICS

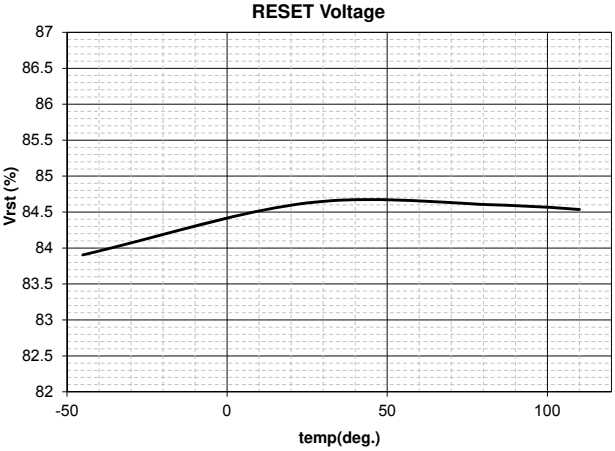
Standby Current (Icc)



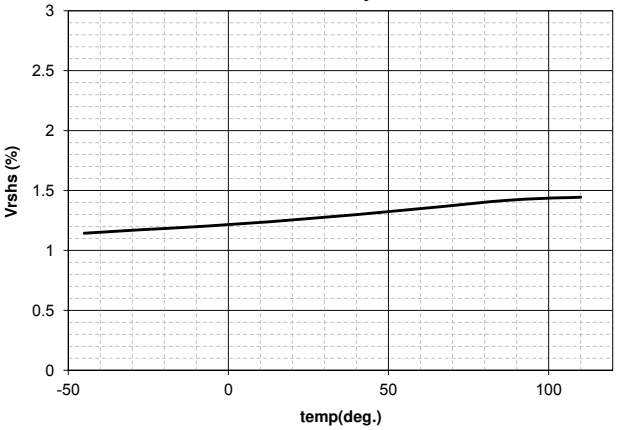
Standby Current (Icc)



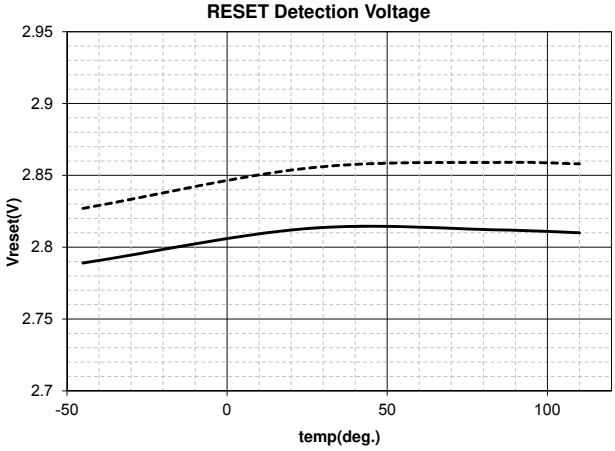
RESET Voltage



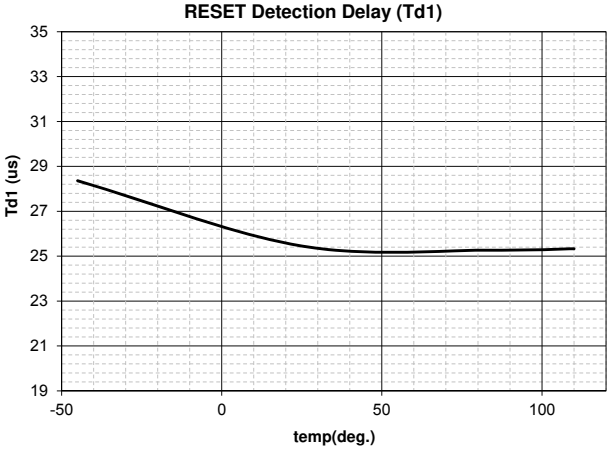
RESET detection hysteresis



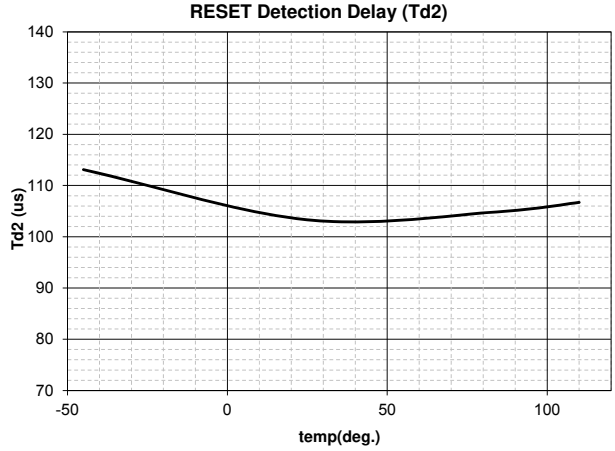
RESET Detection Voltage



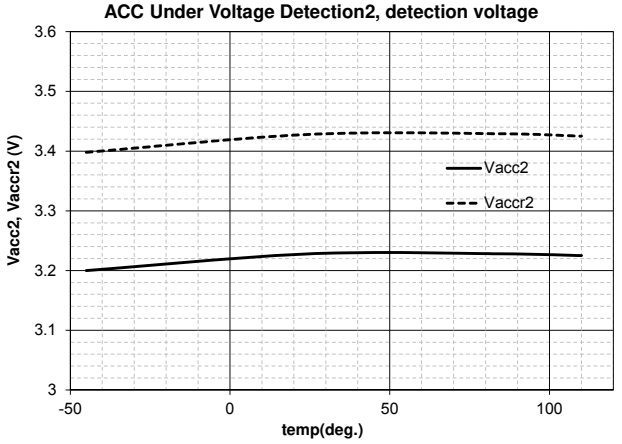
RESET Detection Delay (Td1)



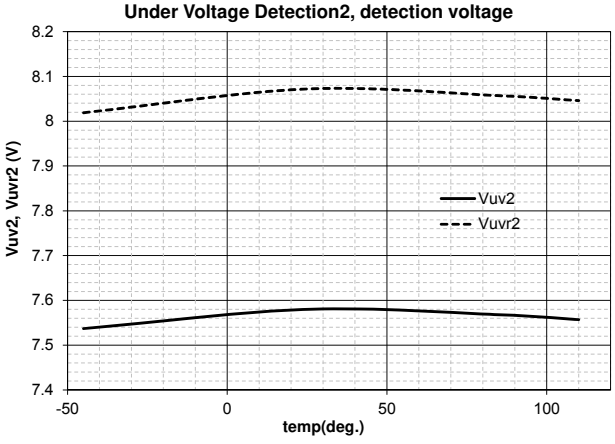
RESET Detection Delay (Td2)



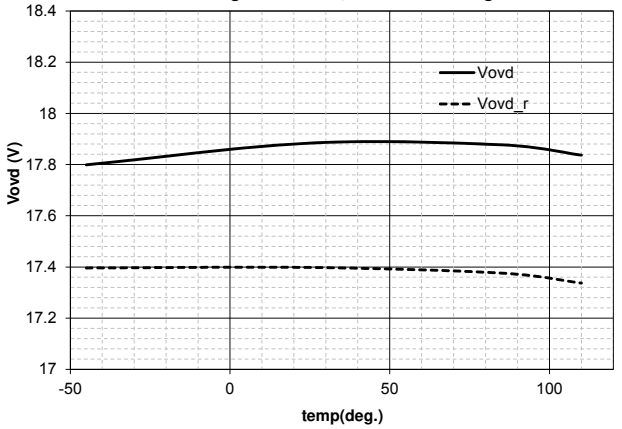
ACC Under Voltage Detection2, detection voltage



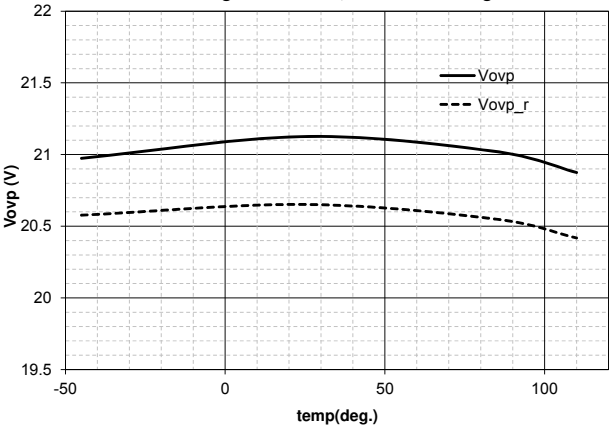
Under Voltage Detection2, detection voltage



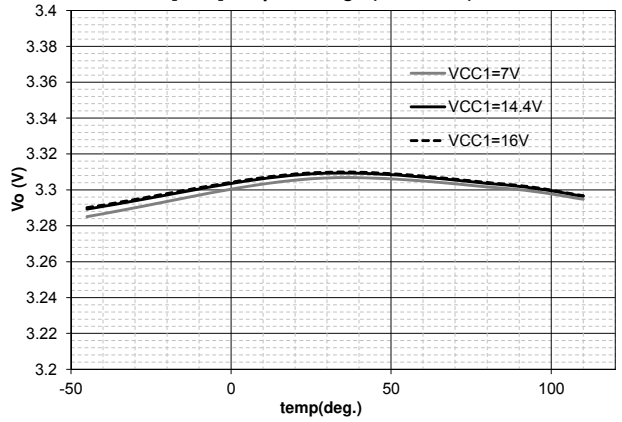
Over Voltage Detection, detection voltage



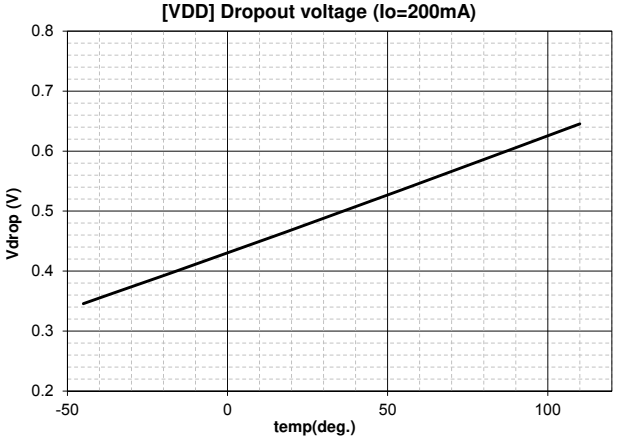
Over Voltage Protection, detection voltage



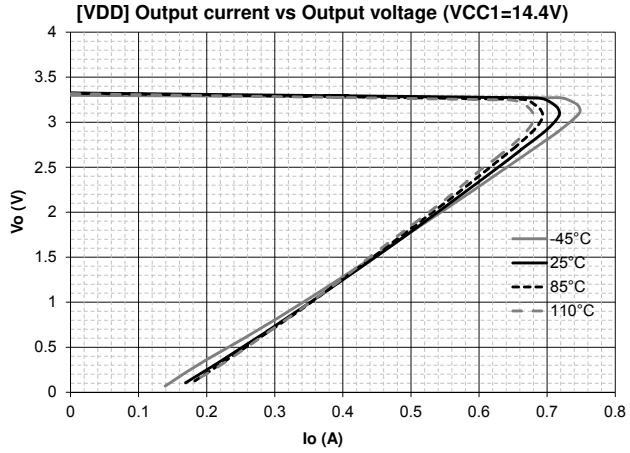
[VDD] Output voltage (Io=200mA)



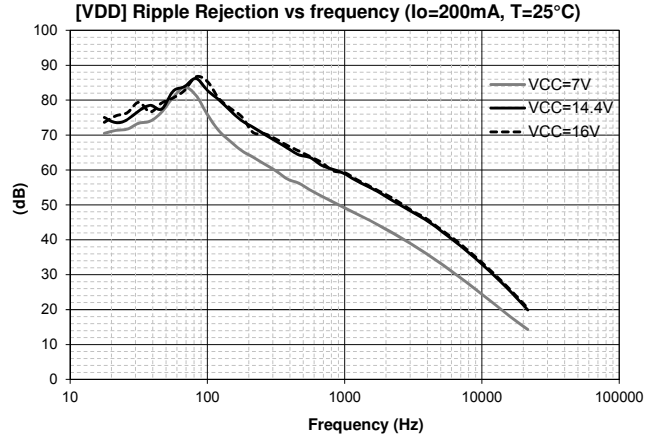
[VDD] Dropout voltage (Io=200mA)



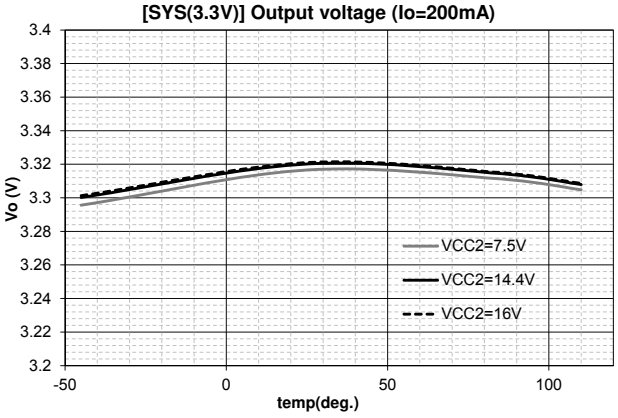
[VDD] Output current vs Output voltage (VCC1=14.4V)



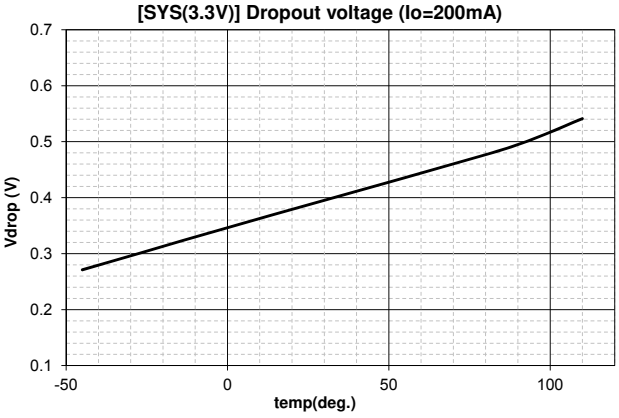
[VDD] Ripple Rejection vs frequency (Io=200mA, T=25°C)



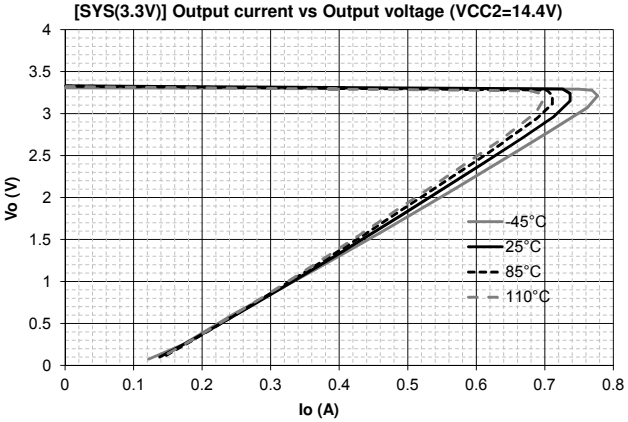
[SYS(3.3V)] Output voltage (Io=200mA)



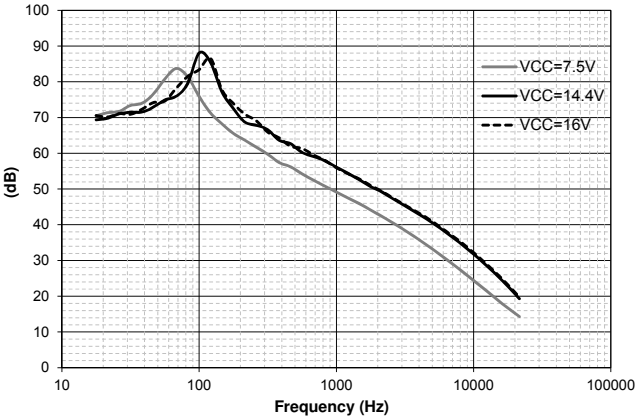
[SYS(3.3V)] Dropout voltage (Io=200mA)



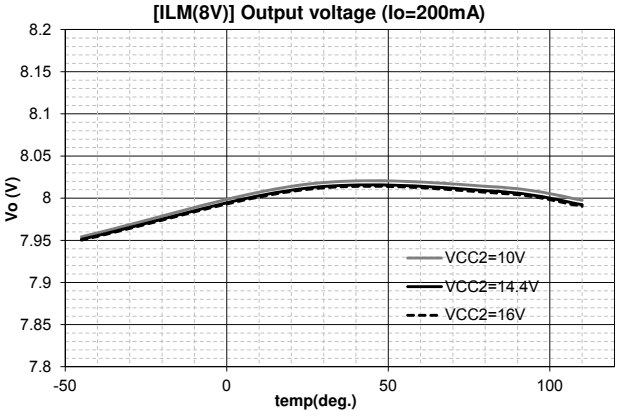
[SYS(3.3V)] Output current vs Output voltage (VCC2=14.4V)



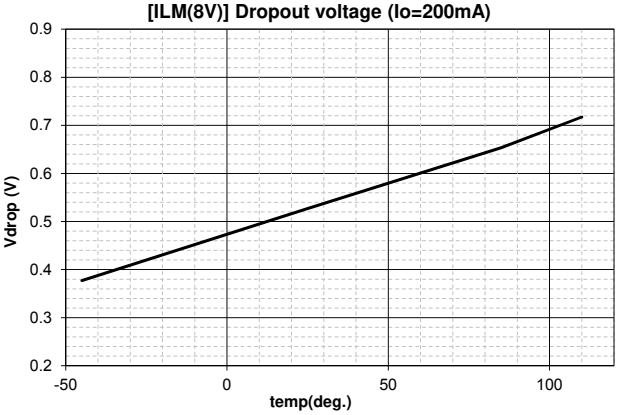
[SYS(3.3V)] Ripple Rejection vs frequency (Io=200mA, T=25°C)



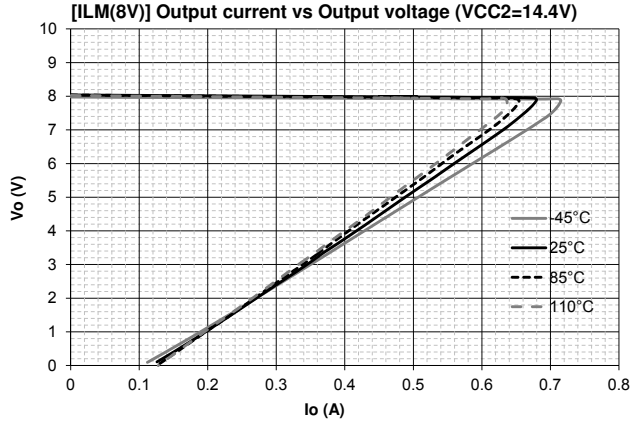
[ILM(8V)] Output voltage (Io=200mA)



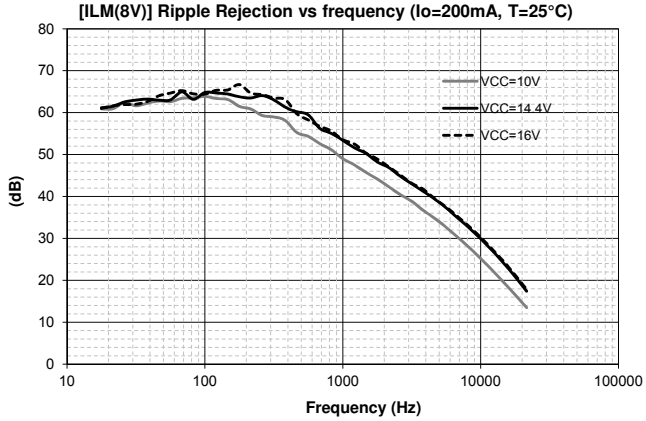
[ILM(8V)] Dropout voltage (Io=200mA)



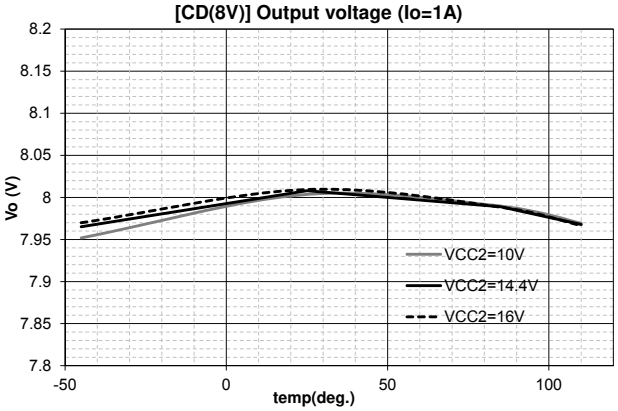
[ILM(8V)] Output current vs Output voltage (VCC2=14.4V)



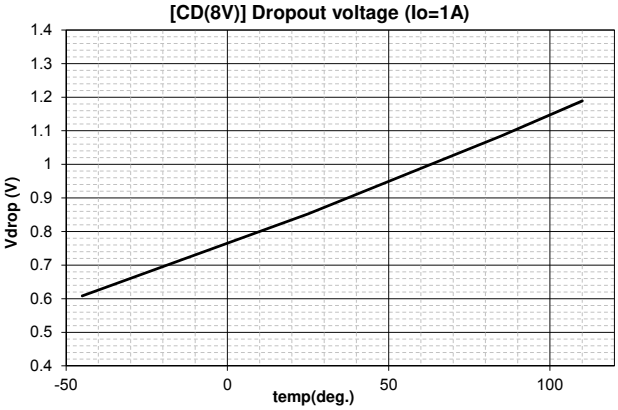
[ILM(8V)] Ripple Rejection vs frequency (Io=200mA, T=25°C)



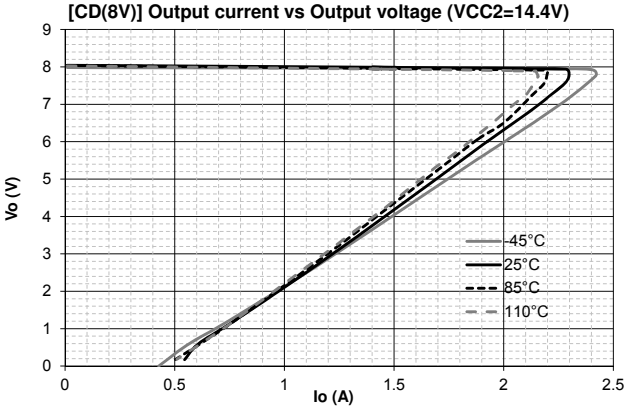
[CD(8V)] Output voltage (Io=1A)



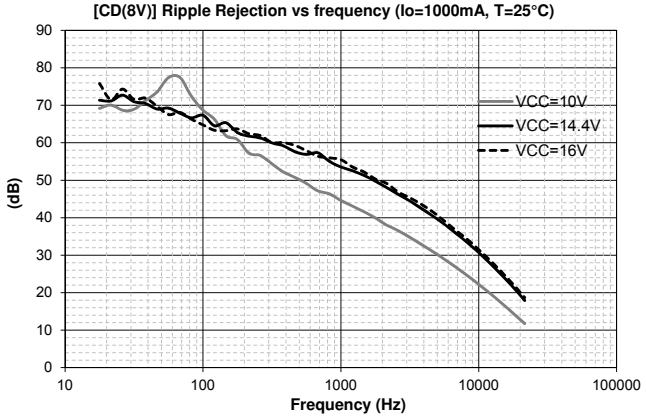
[CD(8V)] Dropout voltage (Io=1A)



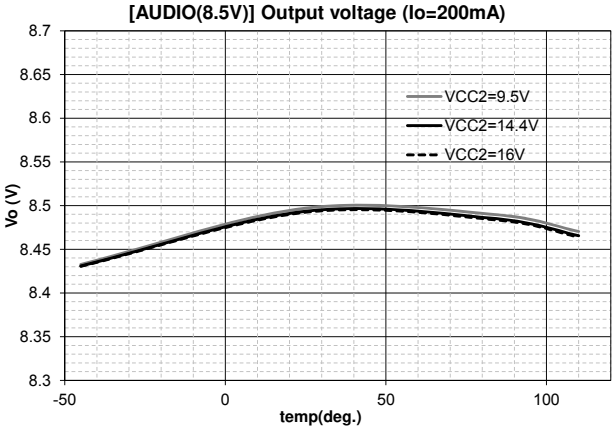
[CD(8V)] Output current vs Output voltage (VCC2=14.4V)



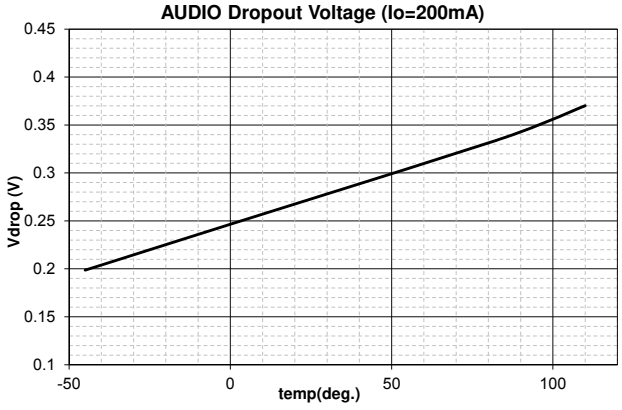
[CD(8V)] Ripple Rejection vs frequency (Io=1000mA, T=25°C)



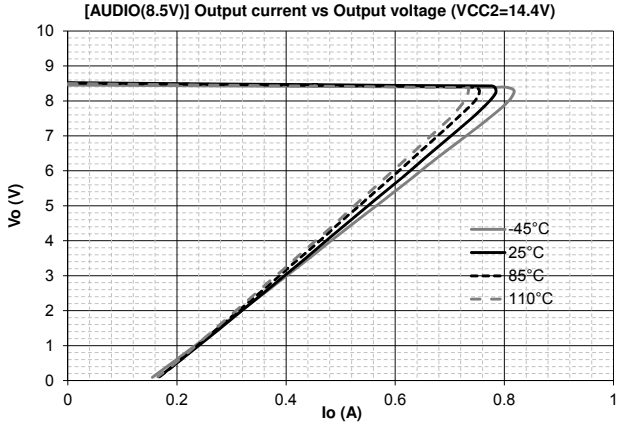
[AUDIO(8.5V)] Output voltage (Io=200mA)



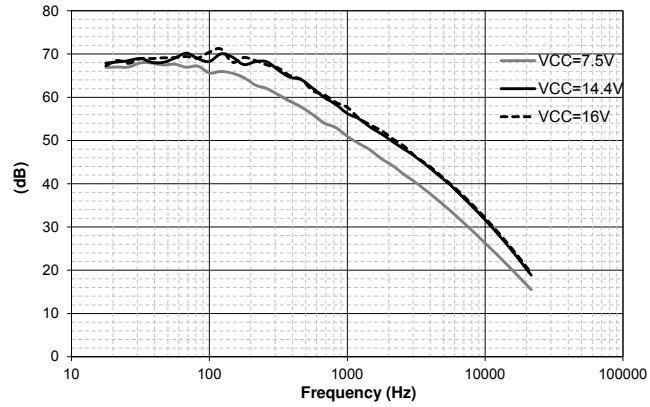
AUDIO Dropout Voltage (Io=200mA)

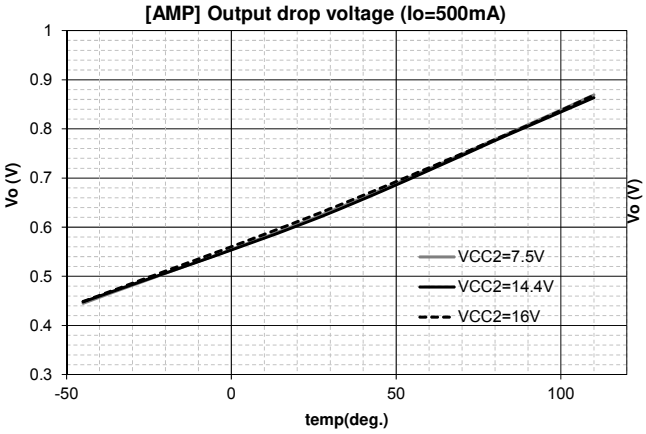


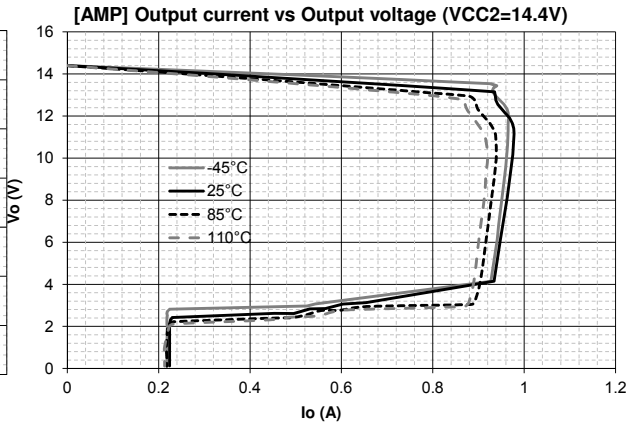
[AUDIO(8.5V)] Output current vs Output voltage (VCC2=14.4V)



[AUDIO] Ripple Rejection vs frequency (Io=200mA, T=25°C)

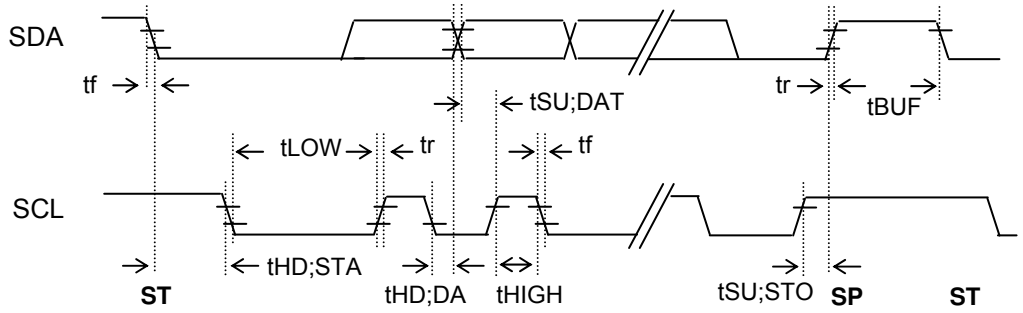



[AMP] Output drop voltage (Io=500mA)
Vo (V)
temp(deg.)
VCC2=7.5V
VCC2=14.4V
VCC2=16V


[AMP] Output current vs Output voltage (VCC2=14.4V)
Vo (V)
Io (A)
-45°C
25°C
85°C
110°C

I²C-bus Interface timing

Parameter	Symbol	min	typ	max	unit
SCL clock frequency	fSCL	0		400	kHz
START condition hold time	tHD;STA	0.6			us
SCL “L” pulse-width	tLOW	1.3			us
SCL “H” pulse-width	tHIGH	0.6			us
DATA hold time	tHD;DAT	0			us
DATA setup time	tSU;DAT	0.1			us
SDA/SCL rise time	tr			0.3	us
SDA/SCL fall time	tf			0.3	us
STOP condition setup time	tSU;STO	0.6			us
Bus free time between STOP and START condition	tBUF	1.3			us
Bus line load capacitance	Cb			400	pF



I²C-bus interface format (MSB first)

This part is I²C controlled power supply, using 2 wires of SCL,SDA.

The communication protocol comprises start-condition, device-address, sub-address, data and stop-condition.

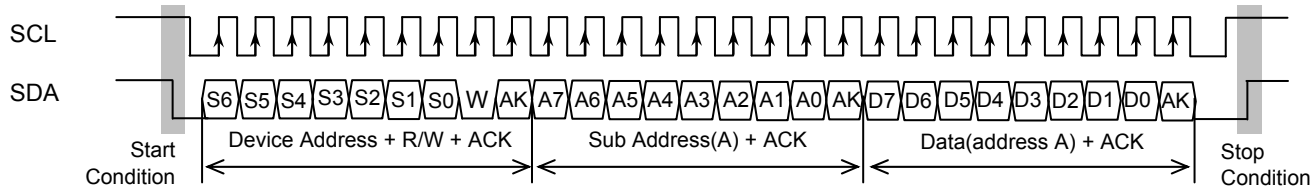
Every 8 bits are followed by ACK bit, and the receiver device pulls down SDA line during ACK period.

This part doesn't accept sub-address auto increment format. (Single data byte write per a communication.)

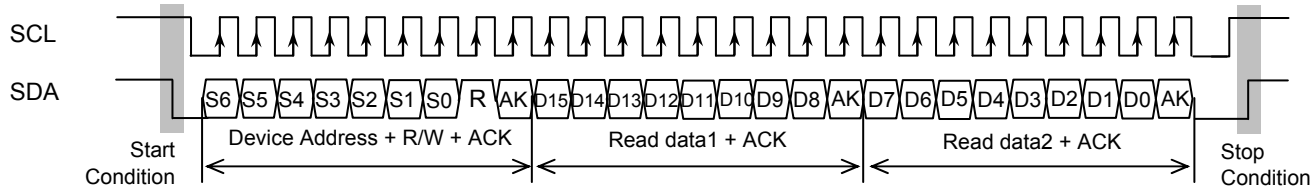
The protocol in Read-mode comprises start-condition, device-address, data1, data2 and stop-condition.

(Note)The I²C-bus communication may be unstable when VDD voltage is not stable or out of specification range, since I²C-BUS circuitry is supplied by VDD.

Write mode



Read mode



• Device address

S6	S5	S4	S3	S2	S1	S0	R/W
0	0	0	1	0	0	0	1/0

• Register map

Write

	D7	D6	D5	D4	D3	D2	D1	D0	init
PM	ILM_EN	CD_EN	AUDIO_EN	SYS_EN	AMP_EN	0	0	0	00000000
VCTL	ILM_V1	ILM_V0	CD_V1	CD_V0	AUD_V1	AUD_V0	SYS_V	0	00000000
DET	ACC_V1	ACC_V0	UVD_V1	UVD_V0	BDETMD	0	(Reserved)		00000000

Read

	D15	D14	D13	D12	D11	D10	D9	D8	init
VCTL	ILM_V1	ILM_V0	CD_V1	CD_V0	AUD_V1	AUD_V0	SYS_V	0	00000000

	D7	D6	D5	D4	D3	D2	D1	D0	init
FLG	ACCUV	UV	OV	OVP	TWARN	OC	0	0	00000000

Write Register explanation

ADR	bit	Name	init	Description
00h	7	ILM_EN	0	ILM output enable 1: ON 0: OFF
	6	CD_EN	0	CD output enable 1: ON 0: OFF
	5	AUDIO_EN	0	AUDIO output enable 1: ON 0: OFF
	4	SYS_EN	0	SYS output enable 1: ON 0: OFF
	3	AMP_EN	0	AMP output enable 1: ON 0: OFF
	2		0	
	1		0	
	0		0	

ADR	bit	Name	init	Description
01h	[7:6]	ILM_V[1:0]	00	ILM output voltage(*) 11: 12 V 10: 10.5 V 01: 9 V 00: 8 V
	[5:4]	CD_V[1:0]	00	CD output voltage(*) 11: 8 V 10: 7 V 01: 6 V 00: 5 V
	[3:2]	AUD_V[1:0]	00	AUDIO output voltage(*) 11: 12 V 10: 9 V 01: 8.5 V 00: 5 V
	1	SYS_V	0	SYS output voltage(*) 1: 5 V 0: 3.3 V
	0		0	

(*) “Output voltage setting” is only valid when corresponding output is set disabled(xxx_EN=0). It is ignored when the output is set enabled(xxx_EN=1).

ADR	bit	Name	init	Description
02h	[7:6]	ACC_V[1:0]	00	ACC detection voltage 11: 4.2 V 10: 3.6 V 01: 3.2 V 00: 2.7 V
	[5:4]	UVD_V[1:0]	00	UVDET detection voltage 11: 8 V 10: 7.5 V(9 V) 01: 7.5 V(8 V) 00: 6.5 V
	3	BDETMD	0	BDET output mode 1: BDET/TWARN 0: BDET only
	2		0	
	[1:0]	(Reserved)	00	(For TEST) Must be set to “00” for normal use.

Read Register explanation

ADR	bit	Name	init	Description
	[15:14]	ILM_V[1:0]	00	ILM output voltage 11: 12 V 10: 10.5 V 01: 9 V 00: 8 V
	[13:12]	CD_V[1:0]	00	CD output voltage 11: 8 V 10: 7 V 01: 6 V 00: 5 V
	[11:10]	AUD_V[1:0]	00	AUDIO output voltage 11: 12 V 10: 9 V 01: 8.5 V 00: 5 V
	9	SYS_V	0	SYS output voltage 1: 5 V 0: 3.3 V
	8		0	
	7	ACCUV	0	ACC detection 1: Under voltage 0: Nornmal
	6	UV	0	Under voltage detection 1: Under voltage 0: Normal
	5	OV	0	Over voltage detection 1: Over Voltage 0: Normal
	4	OVP	0	Over voltage protection 1: Over Voltage Protection 0: Normal
	3	TWARN	0	Thermal Warning 1: High temperature 0: Normal
	2	OC	0	Output Over Current 1: Over current 0: Normal
	1		0	
	0		0	

FUNCTIONAL DESCRIPTION

[Standby mode]

When VCC1 is applied, internal control circuitry is automatically reset and goes into Stand-by mode.
In Stand-by mode, following functions are active.
VDD(3.3 V) output
I^2C-bus communication
Over voltage protection(OVP)/UVDET/OVDET/ACC detection/BDET output
Thermal shutdown(TSD)

[VCC1/VCC2]

VCC1 input is necessary for any operation of this device since VCC1 supplies VDD and common circuitry such as reference voltage, internal control circuitry.
VCC2 is the supply for AUDIO/ILM/CD/AMP/SYS outputs.
LV56851UV can tolerate up to 50 V peak surge voltage on VCC1/2 or ACCIN, but for more safety design, adding power clamp such as power zener diode on battery connected line is recommended in order to absorb applied surge.
LV56851UV has no protection against battery reverse connection. If a negative voltage input is possible, adding Schottky diode between VCC and GND is recommended to protect the device from the negative voltage.

[Controls]

The functions of LV56851UV can be controlled via I^2C-bus. See “I2C bus interface format” term for details.

[Linear Regulators]

VDD output

When VCC1 is applied, VDD output is active regardless of control states.

SYS/CD/AUDIO/ILM output

These outputs are individually enabled or disabled via I^2C-bus.
The voltage of each output can be selected via I^2C-bus. These commands must be set prior to enabling corresponding output. If you intend to change the voltage setting for these outputs, be sure to do it after the output is set disabled. In order to avoid unintended output voltage change, each “output voltage setting” is valid only when corresponding output is set disabled(xxx_EN=0). The “output voltage setting” is ignored when the output is set enabled(xxx_EN=1).
Output voltage setting can be referred by reading via I^2C-bus(VCTL register). It is strongly recommended to read and check VCTL register value just before setting enable the output in order to avoid unintended output voltage change even in case if communication error were to happen and incorrect voltage setting were written to the device.
Each regulator output limits output current if the output gets over-loaded condition. The limit current decreases as the output voltage gets lower, in order to reduce the stress applied to the device.

All regulators in LV56851UV are low dropout outputs, because the output stage of all regulators is P-channel LDMOS.
When you select output capacitors for linear regulators, you should consider three main characteristics: startup delay, transient response and loop stability. The capacitor values and type should be based on cost, availability, size and temperature constraints. Tantalum, Aluminum electrolytic, Film, or Ceramic capacitors are all acceptable solutions. However, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but if the circuit operates at low temperatures (-25 to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's datasheet usually provides this information.

[High-side switch]

AMP is a high-side power switch connected to VCC2. The output is enabled or disabled via I^2C-bus.
The high-side switch limits output current if the output gets over-loaded condition. The limit current becomes lower value, if the output voltage gets lower than 2.5

V(typ) in order to reduce the stress applied to the device.

If the output is connected to inductive load or loads which have different ground potential, protection diodes (D1,D2) are necessary to protect the device from negative voltage.

[Current Limiting]

When the each output becomes in over loaded condition, the device limits the output current.

All outputs are also protected against short circuit to GND by fold back current limiter.

If one of each output except VDD is in over-current condition, OC bit of FLG register is set 1, which can be read via I^2C-bus.

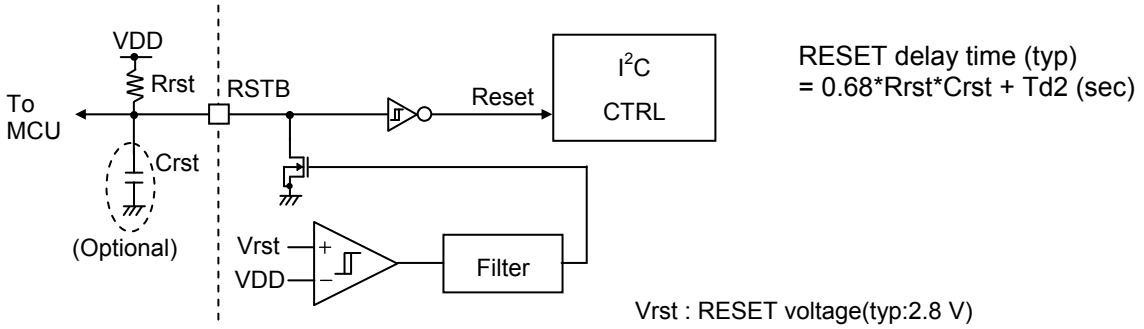
[Detections]

RESET circuit

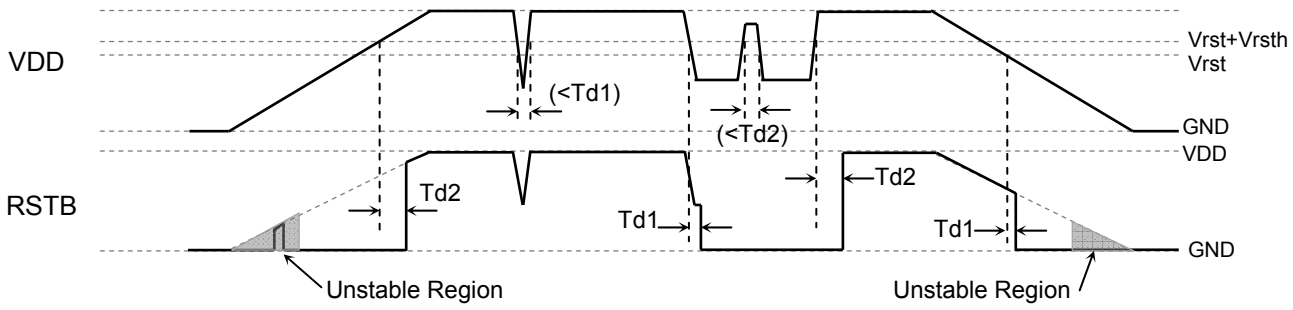
When the VDD voltage drops below the reset threshold (typ:2.8 V, 85% of Vo1:3.3 V) for more than Detection delay period(Td1), RSTB is pulled low. During RSTB=Low, internal control circuitry is reset and all the registers of I^2C-bus are initialized.

When the VDD voltage rises higher than the threshold (typ:2.86 V, 86.6% of Vo1:3.3 V), RSTB becomes open state and reaches high level by external resistor Rrst, internal reset is released after the delay period(Td2).

Add an optional capacitor between RSTB to GND in order to obtain longer reset time (>Td2). The approximate delay time can be calculated by the expression below.



RESET circuit block diagram



RSTB Timing Chart

Under voltage detection (UVDET)

If the VCC2 voltage gets lower than set value (UVD_V[1:0]), Under-Voltage is detected and the UV bit of FLG register is set 1, which can be read via I^2C-bus. BDET pin keeps "Low" during UVDET condition. Each output status keeps the same condition even if UV is detected.

Over voltage detection (OVDET)

If the VCC2 voltage exceeds 18V(typ), Over-Voltage is detected and the OV bit of FLG register is set 1, which can be read via I^2C-bus. BDET pin keeps "Low" during OVDET condition. Each output status keeps the same condition even if OV is detected.

ACC Under voltage detection

If the ACCIN voltage gets lower than set value (ACC_V[1:0]), the ACCUV bit of FLG register is set 1, which can be read via I^2C-bus. ACCDET pin keeps "Low" during ACCUV is detected.

Each output status keeps the same condition even if ACCUV is detected.

Over voltage protection (OVP)

If the voltage of VCC1 or VCC2 exceeds 21 V(typ), OVP is detected and the OVP bit of FLG register is set 1, which can be read via I^2C-bus. And all the outputs except VDD are automatically turned off. When the voltage of VCC1 and VCC2 get lower than 20.5 V(typ), OVP detection is released. But output voltages are not automatically restored, because once OVP is detected, PM register of I^2C-bus is reset.

BDET pin keeps "Low" during OVP condition.

Thermal Shutdown

To protect the device from overheating, a thermal shutdown circuitry is included. If the junction temperature exceeds approximately 175°C(typ), all outputs are turned off regardless of control state. After the junction temperature drops below 145°C(typ), VDD output is automatically restored and I^2C-bus control becomes available.

The thermal shutdown circuit does not guarantee the protection of the final product because it operates out of maximum rating (exceeding Tjmax=150°C).

Thermal Warning

To inform over-temperature of the die, when the junction temperature exceeds approximately 140°C(typ), the TWARN bit of FLG register is set 1, which can be read via I^2C-bus. After the junction temperature drops below 130°C(typ), TWARN is released and TWARN bit is reset.

Each output status keeps the same condition even if TWARN is detected.

If you set BDETMD bit=1 of DET register, BDET pin becomes "Low" when TWARN is detected.

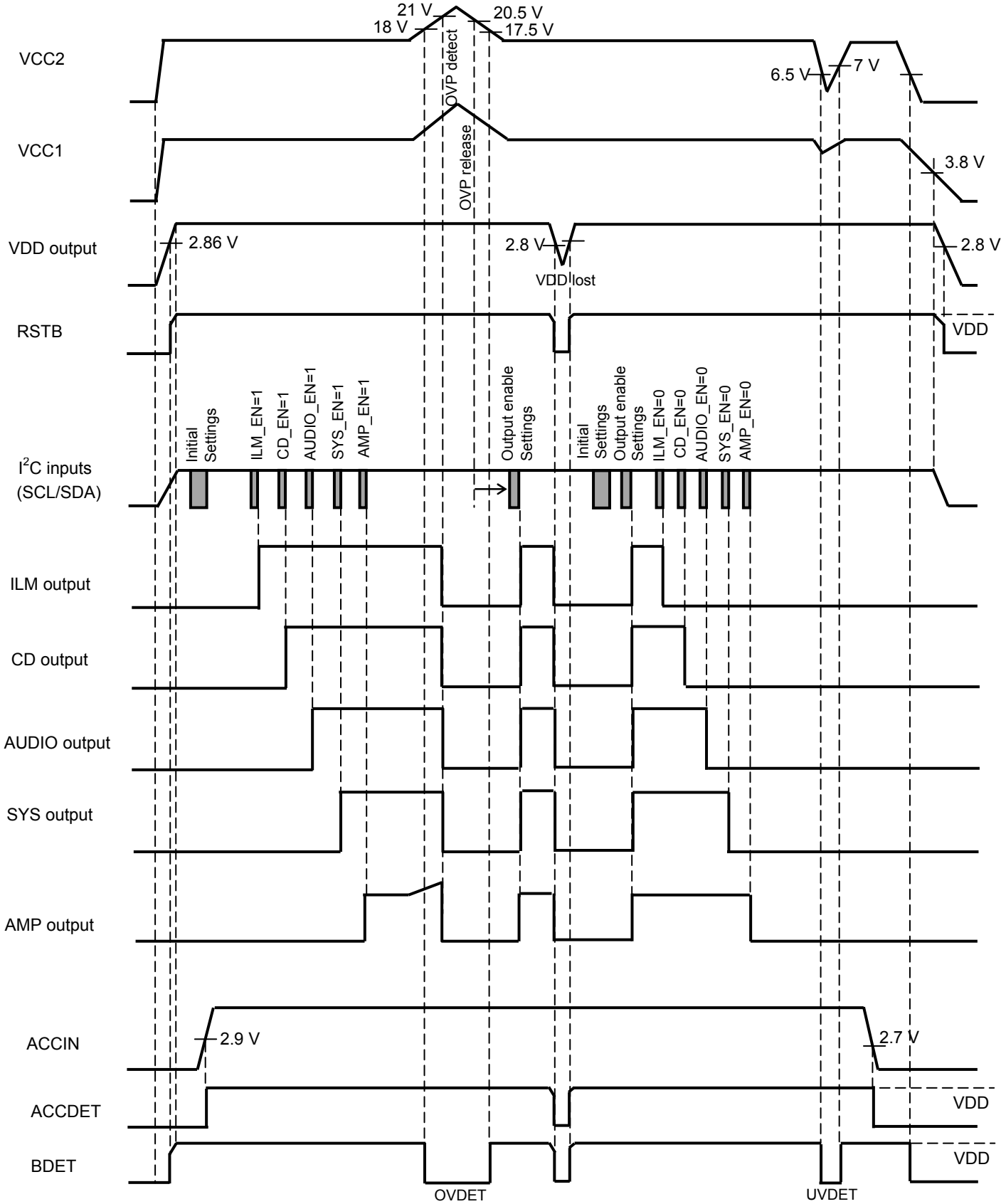
BDET output

BDET output depends on BDETMD bit setting of DET register as shown on the table below.

When each of the listed condition is satisfied, BDET is pulled "Low".

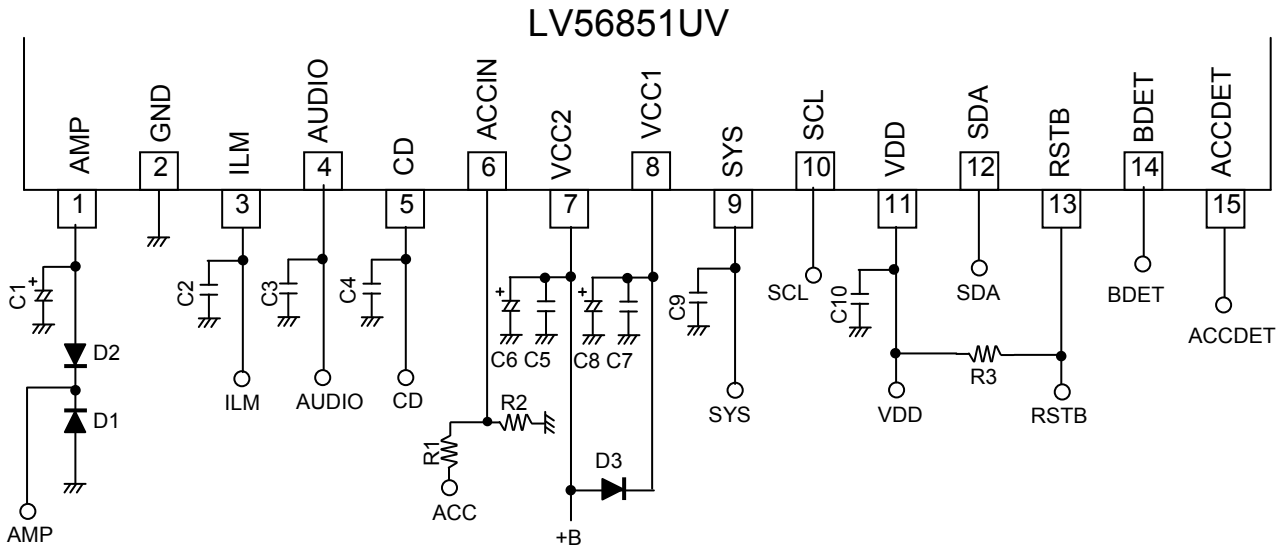
Conditions for BDET=Low		BDETMD	
	Conditions	0 (default)	1
UV	VCC2 < UVDET Threshold	✓	✓
OV	VCC2 > OVDET Threshold	✓	✓
TWARN	Tj > 140°C(typ)	ignored	✓

Timing Chart



Note: The above values are obtained when typ. All the voltage setting are default values

APPLICATION CIRCUIT EXAMPLE



Peripheral parts

Part name	Description	Recommended value	Note
C1	Capacitor for AMP output stabilization	greater than 2.2 μF	
C2,C3,C4,C9,C10	output stabilization capacitor	greater than10 μF(*)	
C6,C8	Power supply bypass capacitor	C6: greater than 100 μF C8: greater than 47 μF	Make sure to implement close to VCC and GND.
C5,C7	Capacitor for oscillation protector	greater than 0.22 μF	
D1,D2	Internal device protection diode	ON Semiconductor SB1003M3	
D3	Reverse current protection diode	ON Semiconductor SB1003M3	
R1,R2	ACC divider resistors		R1>R2
R3	Pull-up resistor	100 kΩ	

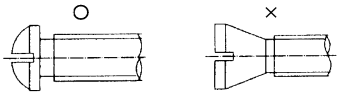
(*) Make sure that output capacitors are greater than 10 μF and meets the condition of ESR=0.001 to 10 Ω , in which voltage/temperature dependence and their tolerances are taken into consideration. Moreover, in case of electrolytic capacitor, high-frequency characteristics should be sufficiently good.

HZIP15 Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating the heat.

a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.

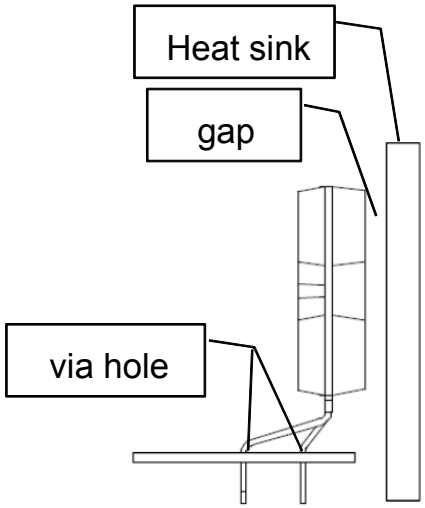
b. Heat sink attachment



Binding-head machine-screw　　Countersunk head machine screw

- Use flat-head screws to attach heat sinks.
- Use also washer to protect the package.
- Use tightening torques in the ranges 39-59 Ncm(4-6 kgcm) .
- If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
- **Do not make gap**, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Take care to the position of via hole.
- Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Verify that there are no press burrs or screw-hole burrs on the heat sink.
- Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
- Twisting must be limited to under 0.05 mm.
- Heat sink and semiconductor device **should be mounted in parallel**.

  Take care of electric or compressed air screw driver
- The speed of these torque wrenches must not exceed 700 rpm, and should typically be about 400 rpm.



c. Silicone grease
- Spread the silicone grease evenly when mounting heat sinks.
- Sanyo recommends YG-6260 (Momentive Performance Materials Japan LLC)

d. Mount
- First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- In case of attaching a heat sink after mounting a semiconductor device into the printed circuit board, be sure not to apply mechanical stress to the semiconductor device and the external pins when tightening up a heat sink with the screw.

e. When mounting the semiconductor device to the heat sink using jigs, etc.,
- Take care not to allow the device to ride onto the jig or positioning dowel.
- Design the jig so that no unreasonable mechanical stress is applied to the semiconductor device.

f. Heat sink screw holes
- Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.

- When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15 % larger than the diameter of the screw is recommended.
- When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15 % smaller than the diameter of the screw is recommended.

g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.