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LV8163QA

Bi-CMOS IC

Fan Motor Driver

Single-Phase Full-Wave Driver

Overview

The LV8163QA is a driver IC for single phase fan motor which operates noiselessly by BTL linear output method. The LV8163QA has variable speed function that corresponds to external PWM single input. Therefore, this IC is suitable for CPU cooler for note PC and the like which requires low power consumption, noiseless operation and variable speed functions.

Functions

- Single phase full wave drive by BTL output method.
- Speed control function by PWM input.
- Integrated lock protector and auto recovery circuit.
- Standby mode and quick start function.
- Hall bias output pin.
- Startup support function (100% DUTYSTART)
- FG signal pin, RD signal pin
- Integrated TSD (Thermal ShutDown) circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------|-------------------------|-------------------------------|-------------|------|
| Power supply voltage | V _{CC} max | | 7 | V |
| Output pin current | I _{OUT} max | | 0.7 | A |
| Output pin withstand voltage | V _{OUT} max | | 7 | V |
| HB output current | I _{HB} max | | 10 | mA |
| PWM pin voltage | V _{PWM} max | | 7 | V |
| FG/RD pin sink current | I _{FG/IRD} max | | 5 | mA |
| FG/RD output pin voltage | V _{FG/VRD} max | | 7 | V |
| Allowable power dissipation | P _d max | Mounted on specified board *1 | 1050 | mW |
| Operating temperature | T _{opr} | | -30 to +95 | °C |
| Storage temperature | T _{stg} | | -55 to +150 | °C |

*1 Specified substrate : 105mm × 120mm × 1.6mm, two-sided glass epoxy board

*2 Do not exceed T_{jmax} = 150°C

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

LV8163QA

Operating Conditions at Ta = 25°C

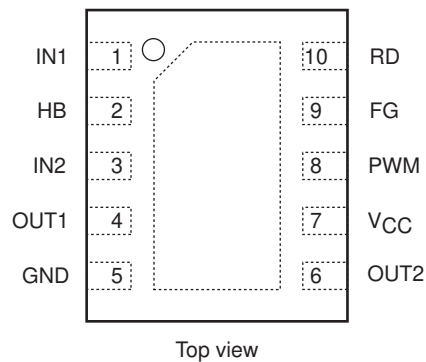
| Parameter | Symbol | Conditions | Ratings | Unit |
|--|--------|------------|----------------|------|
| Power supply voltage | VCC | | 5.0 | V |
| Operating power supply voltage | VCCop | | 2.0 to 6.0 | V |
| Hall input common-mode input voltage range | VICM | | 0.2 to VCC-1.2 | V |
| PWM pin input frequency | FPWMIN | | 20 to 60 | kHz |

Electrical Characteristics at Ta = 25°C, VCC = 5V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-----------|---------------------------|----------|------|---------|------|
| | | | min | typ | max | |
| Circuit current | ICC | During operation | 0.95 | 1.3 | 1.6 | mA |
| | ICC st | During Standby mode | | 10 | 30 | μA |
| HB pin voltage | VHB | IHB = 5mA | 0.9 | 1.03 | 1.2 | V |
| Output pin high-level voltage | VOH | IOUT = 200mA (VCC - VOUT) | | 0.16 | 0.23 | V |
| Output pin low-level voltage | VOL | IOUT = 200mA | | 0.10 | 0.15 | V |
| Hall amplifier input offset voltage | VINOFFS | | -6 | | 6 | mV |
| Hall amplifier voltage gain | GH | | 44 | 45.5 | 47 | dB |
| PWM pin input Low level voltage | VPWML | | 0 | | VCC×0.2 | V |
| PWM pin input High level voltage | VPWMH | VCC < 4V | 1.8 | | 6.0 | V |
| | | 4V VCC | VCC×0.45 | | 6.0 | V |
| FG/RD pin low-level voltage | VFGL/VRDL | IFG/IRD = 3mA | | | 0.3 | V |
| FG/RD pin leak current | IFGL/IRDL | VFG/VRD = 7V | | | 10 | μA |
| FG comparator hysteresis width | FGHYS | | | ±8 | ±16 | mV |
| Lock-detection output ON time | LT1 | | 0.4 | 0.6 | 0.8 | sec |
| Lock-detection output OFF time | LT2 | | 4 | 6 | 8 | sec |
| Lock-detection output ON/OFF ratio | LRTO | LRTO=LT2/LT1 | 8 | 10 | 12 | |
| Thermal shutdown operating temperature | TSD | Design guarantee * | | 180 | | °C |
| Thermal shutdown hysteresis width | ΔTSD | Design guarantee * | | 30 | | °C |

* Design target: These values are the target value in designs. The parameters are not measured independently.

Pin Assignment



Truth value table

| IN1 | IN2 | PWM | OUT1 | OUT2 | FG | RD | Mode |
|------|------|------|------|------|-----|-------------------------|-------------------------|
| High | Low | High | Low | High | OFF | Low | Operation (OUT2→OUT1) |
| | | Low | | Low | | Recirculation | |
| | | * | | OFF | | Lock protector (see *1) | |
| Low | High | High | High | Low | Low | Low | Operation (OUT1→OUT2) |
| | | Low | Low | | | Low | Recirculation |
| | | * | OFF | | | OFF | Lock protector (see *1) |
| * | | Low | Low | Low | OFF | Low | Standby (see *2) |

*1 If FG pulse is not switched when lock detection output is ON, lock protector mode is set.

*2 Standby mode is set when time of lock protector + PWM input low level voltage is greater than 750μs.

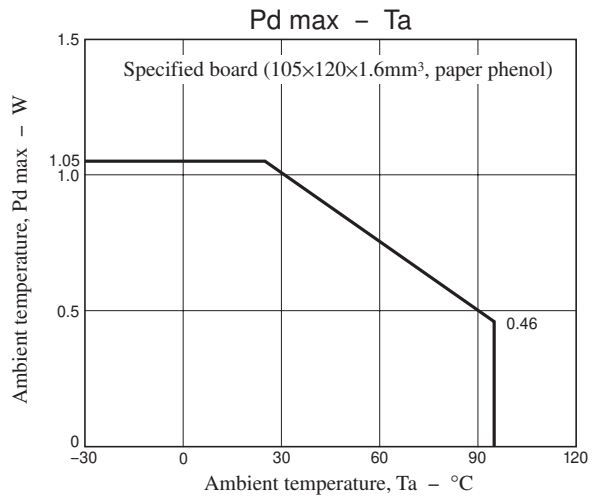
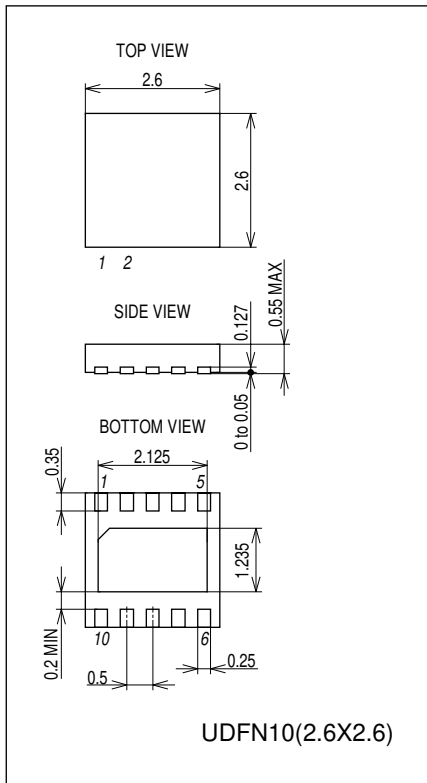
Standby mode is set when time of low level voltage is 750μs and voltage is supplied and PWM input is at low level voltage.

LV8163QA

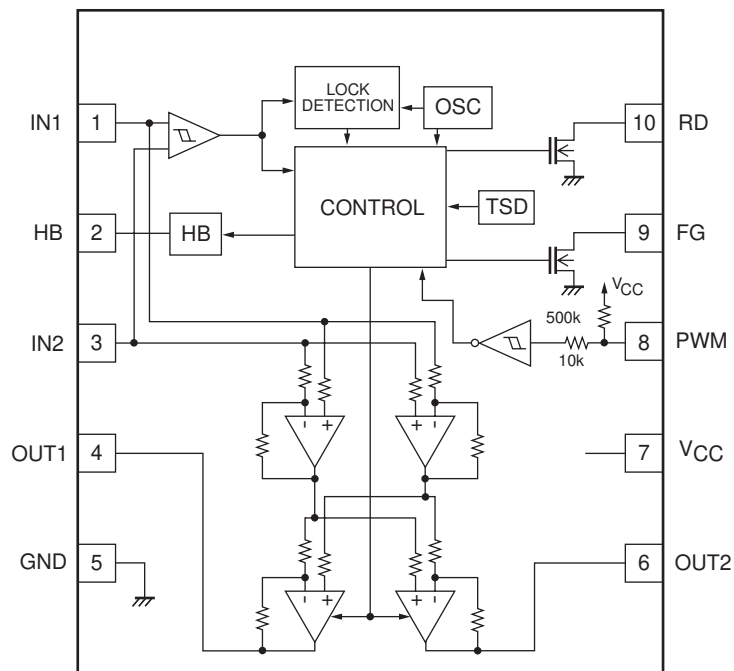
Package Dimensions

unit : mm (typ)

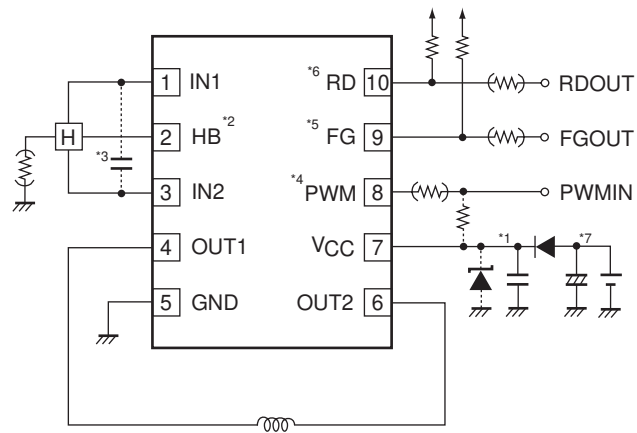
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Block Diagram



Example of circuit application



*1 < Capacitor for power stabilization >

The capacitor for power stabilization must be 1 μ F or greater. The capacitor is not removable.

Make sure to connect the capacitor with the thickest and shortest possible pattern between VCC and GND.

When a protection diode against reverse connection is used. If supply voltage increases due to coil kickback, connect zener diode between power supply and GND.

This IC performs synchronous rectification to reduce heat generation and to enhance efficiency.

Depends on usage conditions, coil current may flow back to power supply by synchronous rectification.

*when output DUTY is reduced rapidly.

*When PWM input frequency is low.

The increase of supply voltage varies depends on the presence of diode (to prevent IC destruction from reverse connection), the size of power capacitor, and usage fan. If the increase of supply voltage is excessive, use capacitor with enough capacitance or connect zener between power supply and GND so that the voltage is within the absolute maximum ratings.

*2 < HB pin >

Constant voltage output pin, which is used as bias for Hall element.

When Hall element is biased from VCC line and HB pin is unused, HB pin should be pulled down to GND with resistor of 1k Ω .

Bias for power supply and bias for HB pin cannot be used together.

Connect a resistor between Hall element and GND to adjust amplitude of Hall element.

*3 < IN1,IN2 pin >

Hall element signal input pin.

Make sure to keep the wiring short to prevent noise.

If noise is generated, use capacitor between IN1 and IN2.

As for Hall input level, the following conditions must be met:

Difference of voltage between IN1 and IN2 > usage voltage / Hall amplifier gain + Hall amplifier input offset

*4 < PWM pin >

Motor speed control signal input pin.

PWM pin is pulled up at 500k Ω in LV8136QA.

Resistance of 500k Ω is used for full-speed setting when PWM pin is open.

In order to control motor speed using open Collector input method (open drain), pull-up is required using suitable resistance.

Pull-up resistance is not required when motor speed is controlled by Push-pull input method.

The order of power supply is optional; either to power supply voltage or PWM input, under one of the following conditions.

1) When open collector input method is used.

2) Pull-up resistance is not implemented and Push-pull input method is used.

It is recommended to connect a resistance greater than 1k Ω in series to protect PWM pin against open GND and misconnection.

*5 < FG pin >

Used as rotation counter.

This pin is open drain output. You can count rotations according to phase change.

This pin is set to off during standby mode.

Make sure to set this pin open when unused.

It is recommended to connect a resistance greater than 1k Ω in series to protect PWM pin against open GND and misconnection.

*6 < RD pin >

Used as lock detector.

This pin is open drain output. During rotation, RD pin is set to low-level voltage. During lock detection, it is set to off.

During standby, it is set to low-level voltage.

Make sure to set this pin open when unused.

It is recommended to connect a resistance greater than 1k Ω in series to protect PWM pin against open GND and misconnection.

*7 < Low power dissipation during standby >

During standby, the fan motor used in LV8136QA can reduce power dissipation into 10 μ A (under room temperature, Typ).

However, power dissipation cannot be reduced into 10 μ A under the following conditions.

- When bias of Hall element is supplied from power supply:

- Current flowing into Hall element increases.

- When pull-up resistor is used to PWM pin

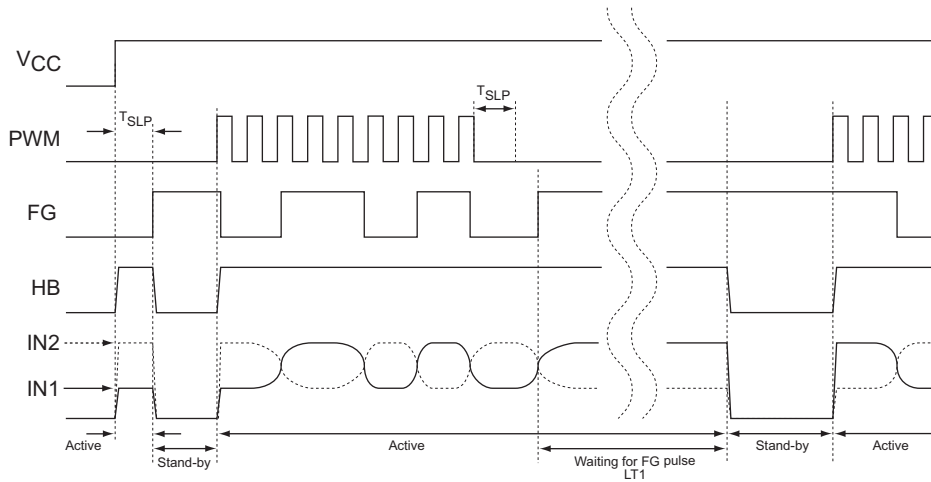
- During standby, the current flowing into pull-up resistor increases because PWM pin must be set to low-level voltage.

- When using RD pin

- During standby, the current flowing into pull-up resistor increases because RD pin turns low-level voltage.

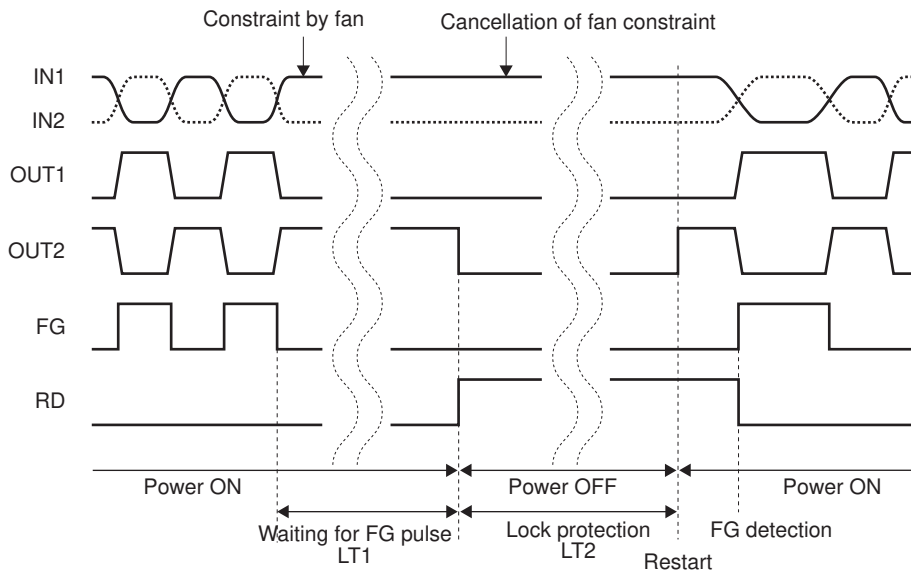
Timing Chart

Switch: stand-by/operation



- *1 $T_{SLP}=750\mu s(\text{typ})$
- *2 If PWM signal is low-level voltage for the period of T_{SLP} and FG signal is not switched for the period of $LT1$, the mode is set to standby.
When turning on power, if PWM signal is low-level voltage for the period of T_{SLP} , the mode is set to standby.
- *3 During standby mode, FG pin is set to OFF and RD pin is set to low-level voltage.

Lock protector



- *1 When lock protector is in operation, OUT1 and OUT2 are both set to low-level voltage.
- *2 RD is set to off during the period of lock protection. After lock protector is cancelled, RD is set to low-level voltage when FG switches from OFF to L or L OFF.
- *3 If PWM = low-level voltage is inputted for the period of T_{SLP} during lock protection, the mode is set to standby.
- *4 The operations start at 100% DUTY when turning on the power, cancelling lock protection, or recovering from standby mode.
(Switch of FG between OFF \rightarrow L and L \rightarrow OFF takes place for 5 or 6 times)

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