Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

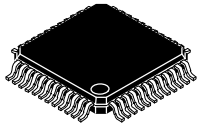
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LV8726TA

Stepper Motor Pre-Driver, PWM, Constant-Current Control, Micro step

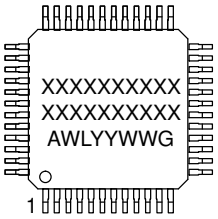
ON Semiconductor®

www.onsemi.com



48-pin TQFP with exposed pad
7 mm x 7 mm

MARKING DIAGRAM



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Ordering Code:
LV8726TA-NH

Package
TQFP48 EP
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Overview

The LV8726 is a bipolar stepper motor driver with ultra-small micro step drive capability. The device uses external dual H-bridges consisting of P and N channel MOSFETs. The operation voltage range is from 9V to 55V, and it is applicable to various industrial applications. Synchronous rectification control is implemented for all H-bridges to minimize power dissipation during a MOSFET switching.

The device implements constant-current control using PWM. The step advance sequencer covers from half step to 1/128 micro step, and is driven by a clock input.

The configuration registers can be programmed through an SPI serial interface. To enhance energy efficiency further, the device can be put into a power saving standby mode.

Features

- H-bridge gate drivers
  - For bipolar stepper motor
  - Clockwise(CW) and Counter-clockwise(CCW) direction control
  - Built-in step vector, selectable number of step resolutions from 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 32, 36, 50, 64, 100 and 128
  - Constant-current control
  - Synchronous rectification to reduce power dissipation
- Single clock input to advance the excitation step
- Low power 1μA(max) standby mode
- Separate power supplies for control logic (3.3-5V) and motor drivers (9V – 55V)
- SPI 8-bit 3-wire serial interface for system configuration
- Input pins for standby and active mode
- Built-in system protection features such as:
  - Under-voltage
  - Over-current
  - Over-temperature

Typical Applications

- Textile machines
- Packing machines
- Large printers
- Engraving machines
- Industrial products

BLOCK DIAGRAM

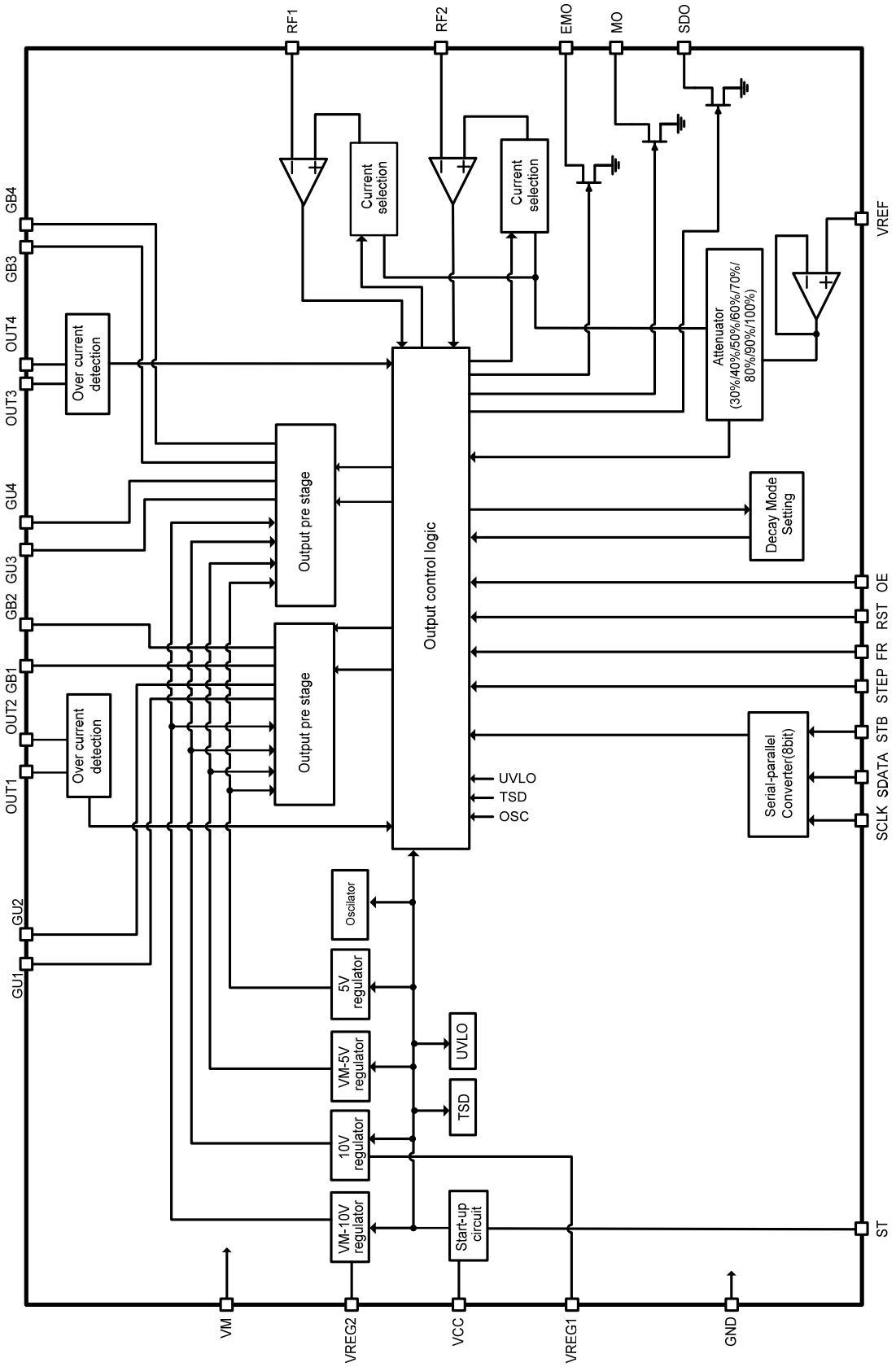


Figure 1. Block Diagram

APPLICATION CIRCUIT EXAMPLE

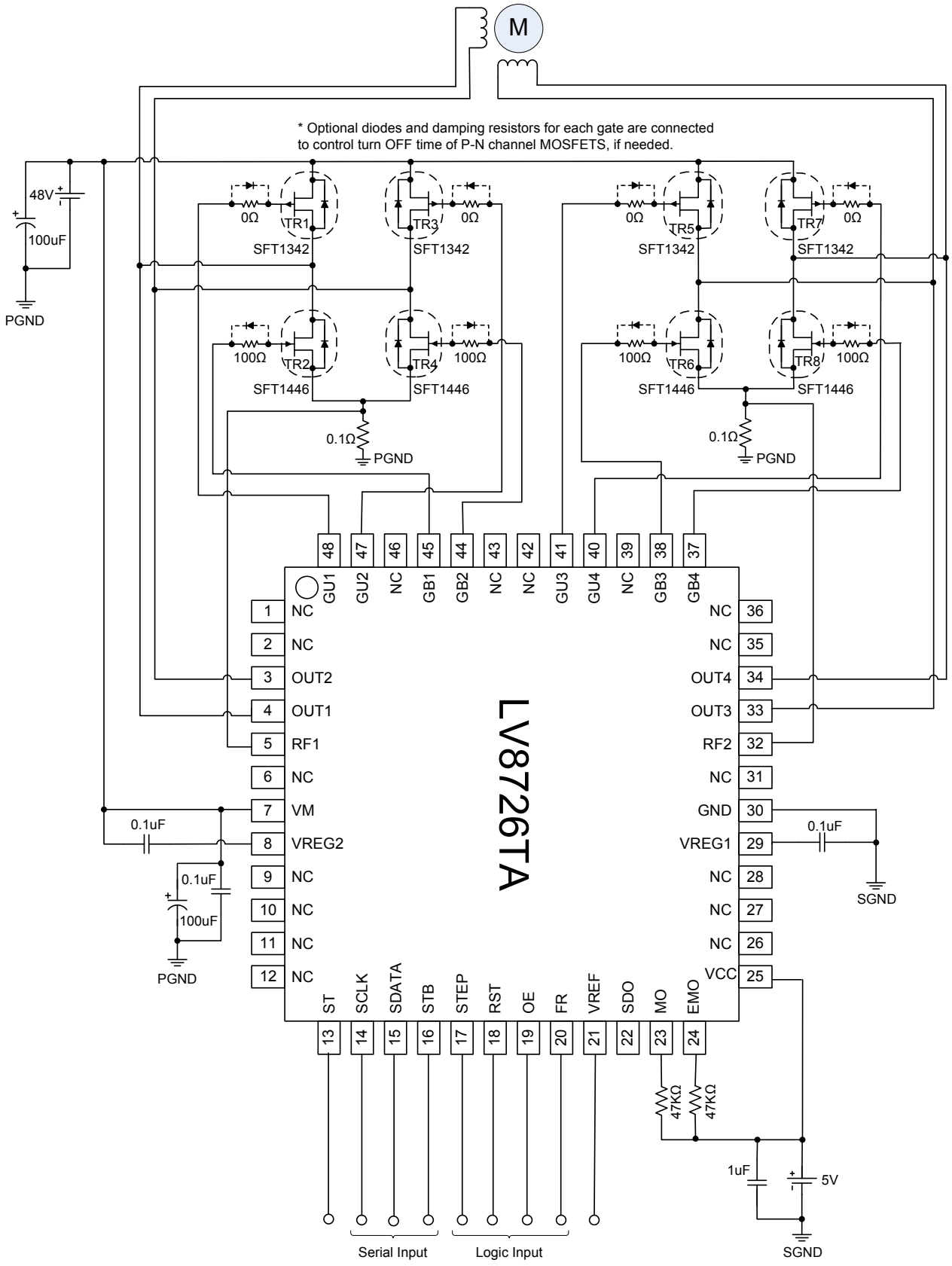


Figure 2. Application Circuit Example

PIN ASSIGNMENT

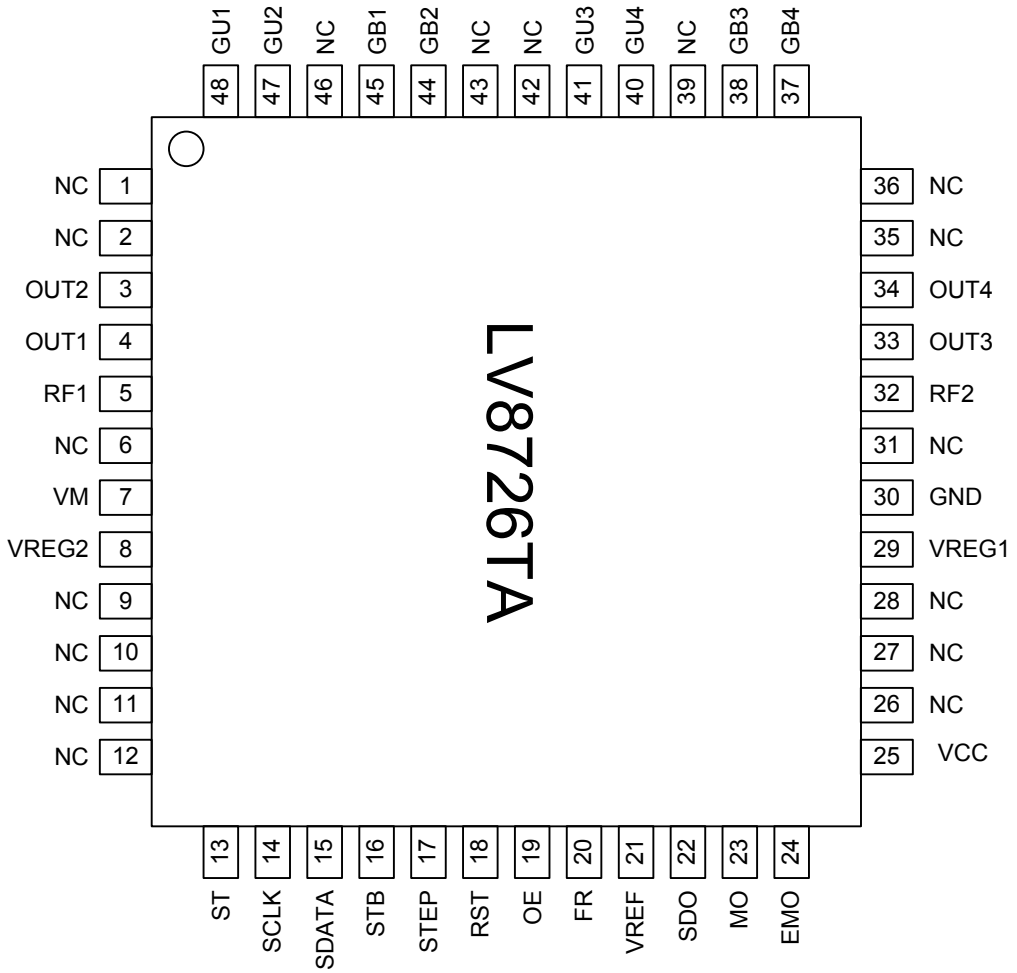
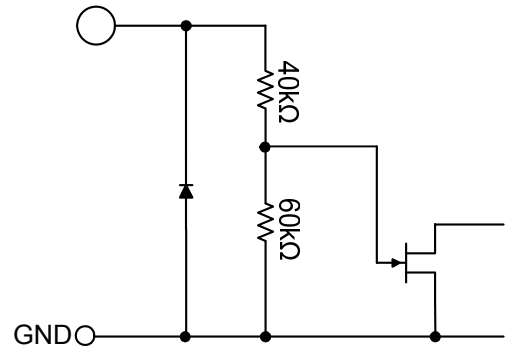
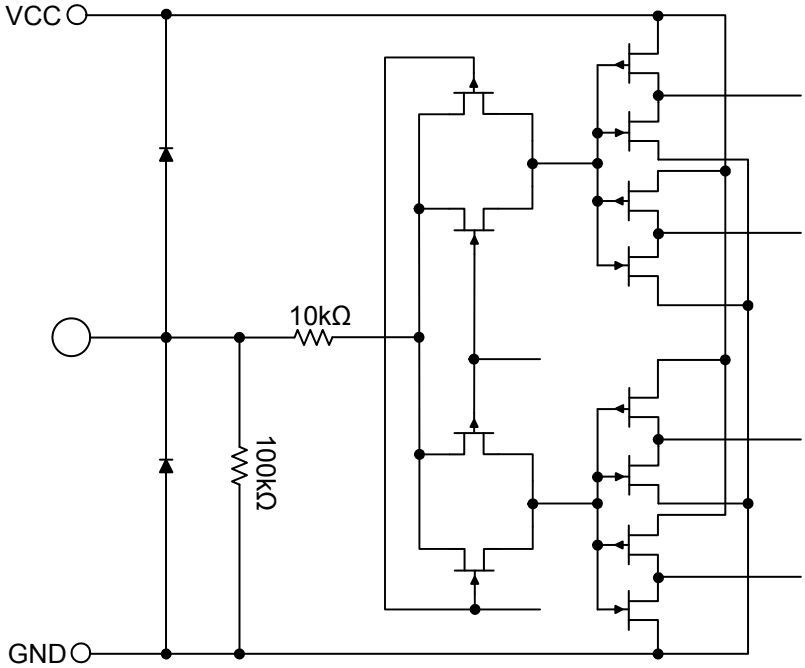
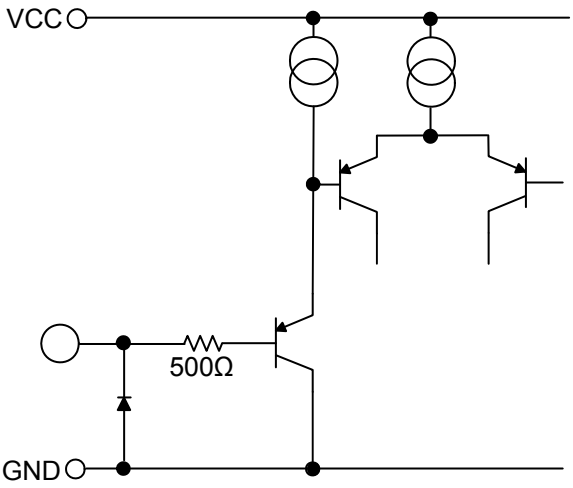


Figure 3. Pin Assignment

PIN FUNCTION DISCRIPTION

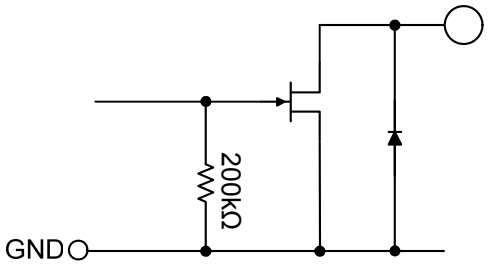
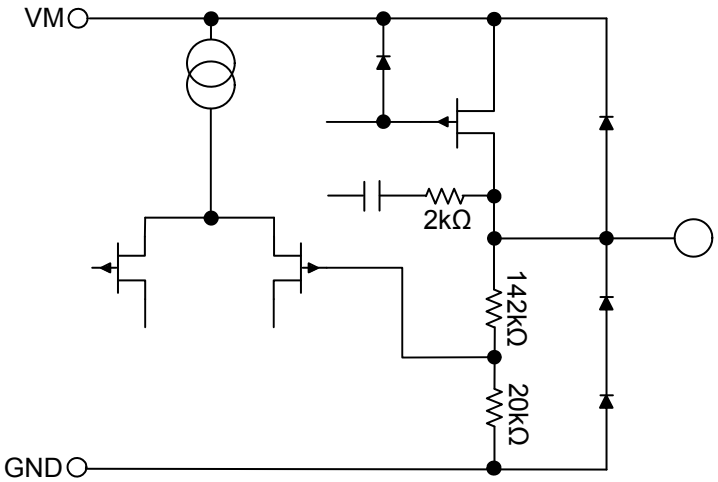
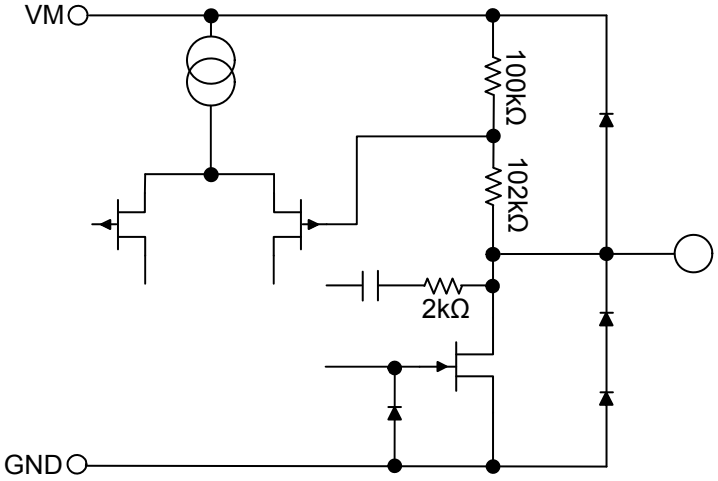
Pin No.	Pin Name	Description
1	NC	No connection
2	NC	No connection
3	OUT2	OUT2 voltage detection pin
4	OUT1	OUT1 voltage detection pin
5	RF1	Channel 1 Output current detection pin
6	NC	No connection
7	VM	Motor power supply pin
8	VREG2	Internal regulator capacitor connection pin for high side FET drive
9	NC	No connection
10	NC	No connection
11	NC	No connection
12	NC	No connection
13	ST	Chip enable pin.
14	SCLK	Serial data transfer clock input
15	SDATA	Serial data input
16	STB	Serial data latch pulse input
17	STEP	Step clock signal input pin
18	RST	Reset signal input pin
19	OE	Output enable signal input pin
20	FR	Direction control signal input pin
21	VREF	Constant-current control reference voltage input pin.
22	SDO	STEP detection output pin
23	MO	Position detecting monitor pin
24	EMO	Unusual condition warning output pins
25	VCC	Logic power supply pin
26	NC	No connection
27	NC	No connection
28	NC	No connection
29	VREG1	Internal regulator capacitor connection pin for low side FET drive
30	GND	GND pin
31	NC	No connection
32	RF2	Channel 2 Output current detection pin
33	OUT3	OUT3 voltage detection pin
34	OUT4	OUT4 voltage detection pin
35	NC	No connection
36	NC	No connection
37	GB4	Output terminal for low side gate drive 4
38	GB3	Output terminal for low side gate drive 3
39	NC	No connection
40	GU4	Output terminal for high side gate drive 4
41	GU3	Output terminal for high side gate drive 3
42	NC	No connection
43	NC	No connection
44	GB2	Output terminal for low side gate drive 2
45	GB1	Output terminal for low side gate drive 1
46	NC	No connection
47	GU2	Output terminal for high side gate drive 2
48	GU1	Output terminal for high side gate drive 1

PIN EQUIVALENT CIRCUITS

Pin No.	Pin Name	Equivalent Circuit
13	ST	
14 15 16 17 18 19 20	SCLK SDATA STB STEP RST OE FR	
21	VREF	

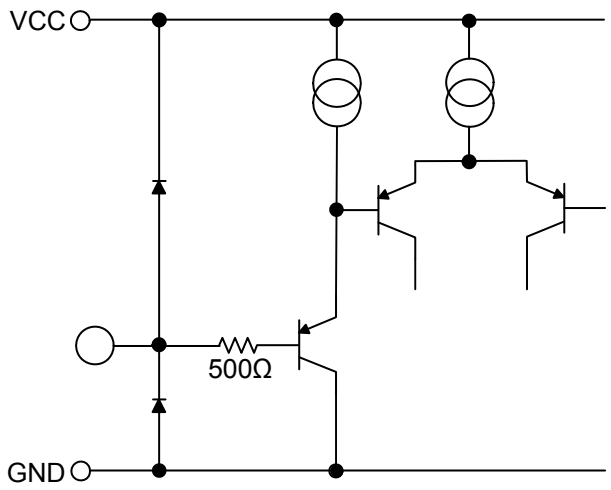
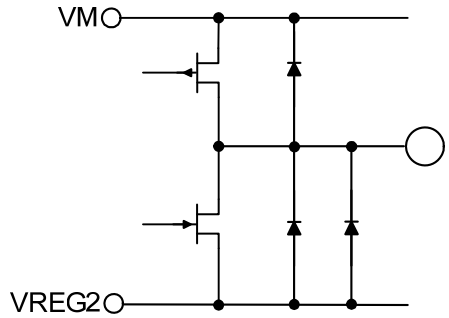
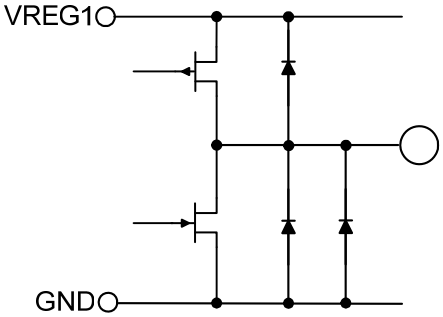
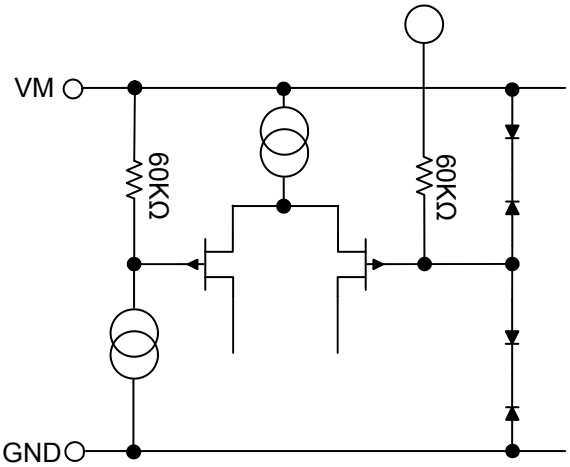
Continued on next page.

Continued from preceding page.

Pin No.	Pin Name	Equivalent Circuit
22 23 24	SDO MO EMO	
29	VREG1	
8	VREG2	

Continued on next page.

Continued from preceding page.

Pin No.	Pin Name	Equivalent Circuit
5 32	RF1 RF2	
40 41 47 48	GU4 GU3 GU2 GU1	
37 38 44 45	GB4 GB3 GB2 GB1	
3 4 33 34	OUT2 OUT1 OUT3 OUT4	

MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Motor Supply Voltage (VM)	V_M	60	V
Logic Supply Voltage (VCC)	V_{CC}	6	V
Logic Input Voltage (ST, SCLK, SDATA, STB, STEP, RST, OE, FR)	V_{IN}	6	V
Output current (GU1, GU2, GU3, GU4, GB1, GB2, GB3, GB4)	I_O	50	mA
Reference input voltage (VREF)	V_{REF}	6	C
Allowable Power Dissipation (Note 2)	Pd	3.35	W
Storage Temperature	T_{stg}	−55 to 150	°C
Junction Temperature	T_J	150	°C
Moisture Sensitivity Level (MSL) (Note 3)	MSL	3	-
Lead Temperature Soldering Pb-Free Versions (10sec or less) (Note 4)	T_{SLD}	260	°C
ESD Human Body Model: HBM (Note 5)	ESD_{HBM}	±2000	V
ESD Charged Device Model: CDM (Note 6)	ESD_{CDM}	±500	V

1. Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Specified circuit board: 90mm× 90mm× 1.6mm, glass epoxy 2-layer board, with backside mounting. It has 1 oz copper traces on top and bottom of the board.
3. Moisture Sensitivity Level (MSL): 3 per IPC/JEDEC standard: J-STD-020A
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D http://www.onsemi.com/pub_link/Collateral/SOLDERRM-D.PDF
5. ESD Human Body Model is based on JEDEC standard: JESD22-A114
6. ESD Charge Device Model is based on JEDEC standard: JESD22-C101

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	37.3	°C/W
Thermal Resistance, Junction-to-Ambient (Note 7)		56.8	°C/W
Thermal Resistance, Junction-to-Case (Top) (Note 2)	$R_{\Psi JT}$	4.8	°C/W
Thermal Resistance, Junction-to-Case (Top) (Note 7)		14.9	°C/W

7. Specified circuit board: 90mm× 90mm×1.6mm, glass epoxy 2-layer board, without backside mounting. It has 1 oz copper traces on top and bottom of the board.

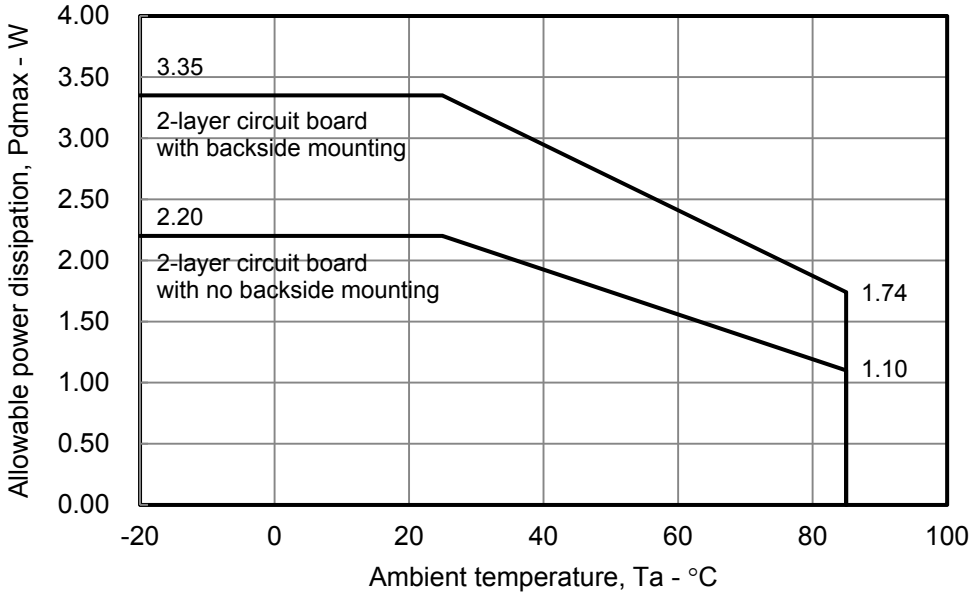


Figure 4. Power Dissipation vs Ambient Temperature Characteristic

RECOMMENDED OPERATING RANGES (Note 8)

Parameter	Symbol	Ratings	Unit
Motor Supply Voltage Range (VM)	V_M	9 to 55	V
Logic Supply Voltage Range (VCC)	V_{CC}	2.7 to 5.5	V
Logic Input Voltage Range (ST, SCLK, SDATA, STB, STEP, RST, OE, FR)	V_{IN}	0 to V_{CC}	V
VREF Input Voltage Range (3.8V≤ V_{CC} ≤5.5V)	V_{REF}	0 to 2.0	V
VREF Input Voltage Range (2.7V≤ V_{CC} ≤3.8V)		0 to V_{CC} – 1.8	V
Ambient Temperature	T_A	−40 to 85	ºC

8. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A=25ºC, V_M = 48V, V_{CC}=5V, V_{REF}=1.5V unless otherwise noted. (Note 9)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Standby Mode Current		I_{Mstn}	ST="L", No load			1	μA
		I_{CCstn}	ST="L", No load			1	μA
Supply Current		I_M	ST="H", OE="L",RST="L", No load		1.6	2.3	mA
		I_{CC}	ST="H", OE="L",RST="L", No load		1.7	2.3	mA
Thermal Shutdown Temperature		TSD	Guaranteed by design	150	180	210	˚C
Thermal hysteresis		ΔTSD	Guaranteed by design		40		˚C
Under-voltage Monitor							
VCC under-voltage threshold		V_{thvc}	VCC falling		2.3	2.45	V
		V_{revc}	VCC rising		2.5	2.7	V
VM under-voltage threshold		V_{thvm}	VM falling		7.6	8.4	V
		V_{revm}	VM rising		7.85	8.7	V
Regulator							
REG10 Output Voltage		V_{REG1}		9.4	10	10.6	V
VM-10V Output Voltage		V_{REG2}		37	38	39	V
MOSFET Drivers							
High Side Output On Resistance		R_{onH1}	GU1,GU2,GU3,GU4-source Io=-10mA		20	32	Ω
		R_{onH2}	GU1,GU2,GU3,GU4-sink Io=10mA		25	40	Ω
Low Side Output On Resistance		R_{onL1}	GB1,GB2,GB3,GB4-source side Io=-10mA		20	32	Ω
		R_{onL2}	GB1,GB2,GB3,GB4-sink side Io=10mA		25	40	Ω
Logic Inputs							
Logic Input Current		I_{INL}	ST,SCLK,SDATA,STB,STEP,RST,OE,FR V_{IN}=0.8V	4	8	12	μA
		I_{INH}	ST,SCLK,SDATA,STB,STEP,RST,OE,FR V_{IN}=5V	30	50	70	μA
Logic Input Voltage	High	V_{INH}	ST,SCLK,SDATA,STB,STEP,RST,OE,FR	2.0		5.5	V
	Low	V_{INL}		0		0.8	V
System Monitoring							
Step signal OFF detection time		T_{SDO0}	No rising edge in STEP pin Register D[7]='0', D[1:0]='01'	0.39	0.52	0.65	S
		T_{SDO1}	No rising edge in STEP pin Register D[7]='1', D[1:0]='01'	0.78	1.04	1.3	S

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PWM Current Control						
VREF Pin Input Current	I_{REF}	V_{REF}=1.5V	−0.5		0	μA
Current setting comparator threshold voltage	V_{REF000}	Register D[4:2]='000', D[1:0]='01'	0.291	0.3	0.309	V
	V_{REF001}	Register D[4:2]='001', D[1:0]='01'	0.261	0.27	0.279	V
	V_{REF010}	Register D[4:2]='010', D[1:0]='01'	0.231	0.24	0.248	V
	V_{REF011}	Register D[4:2]='011', D[1:0]='01'	0.201	0.21	0.218	V
	V_{REF100}	Register D[4:2]='100', D[1:0]='01'	0.172	0.18	0.188	V
	V_{REF101}	Register D[4:2]='101', D[1:0]='01'	0.142	0.15	0.158	V
	V_{REF110}	Register D[4:2]='110', D[1:0]='01'	0.112	0.12	0.128	V
	V_{REF111}	Register D[4:2]='111', D[1:0]='01'	0.082	0.09	0.098	V
PWM (Chopping) Period	F_{chop1}	Register D[7:6]='00', D[1:0]='10'	6	8	10	μs
	F_{chop2}	Register D[7:6]='01', D[1:0]='10'	12	16	20	μs
	F_{chop3}	Register D[7:6]='10', D[1:0]='10'	18	24	30	μs
	F_{chop4}	Register D[7:6]='11', D[1:0]='10'	24	32	40	μs
Open Drain Outputs						
SDO pin saturation voltage	V_{satsdo}	I_{sod}=1mA			400	mV
MO pin saturation voltage	V_{satmo}	I_{mo}=1mA			400	mV
EMO pin saturation voltage	V_{satemo}	I_{emo}=1mA			400	mV
Serial Data Interface (Note 10)						
SCLK "H" Pulse Width	T_{ckh}		0.125			μs
SCLK "L" Pulse Width	T_{ckl}		0.125			μs
SCLK start setup time	T_{sup1}	STB=Low -> SCLK rising edge	0.125			μs
STB setup time	T_{sup2}	SCLK rising edge -> STB rising edge	0.125			μs
Serial Packet STB Interval	T_{stbw}		0.125			μs
SDATA setup time	T_{ds}		0.125			μs
SDATA hold time	T_{dh}		0.125			μs
SCLK Frequency	F_{clk}				4	MHz

9. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. See Figure 5 for the definition of the timing

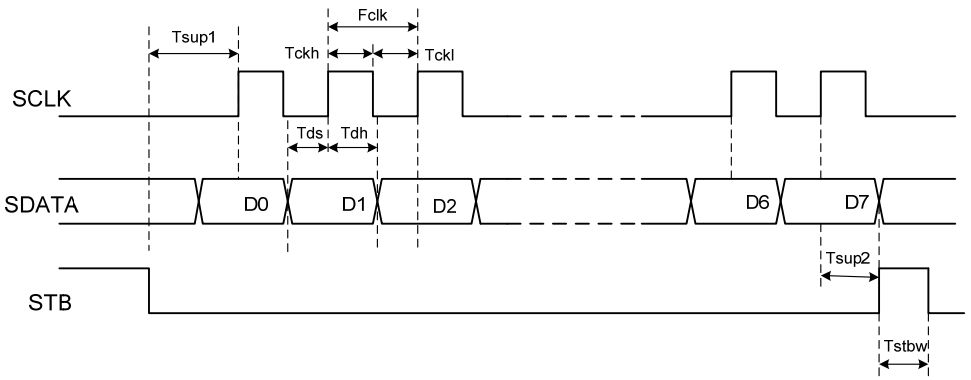


Figure 5. Serial Interface (SPI) Timing Chart

TYPICAL CHARACTERISTICS

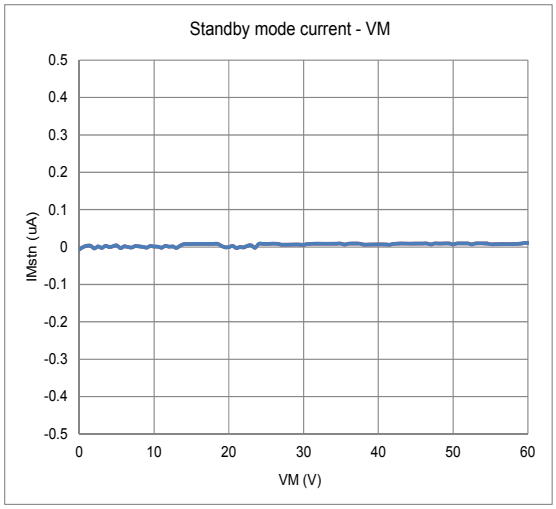


Figure 6. Standby Mode Current vs VM Voltage

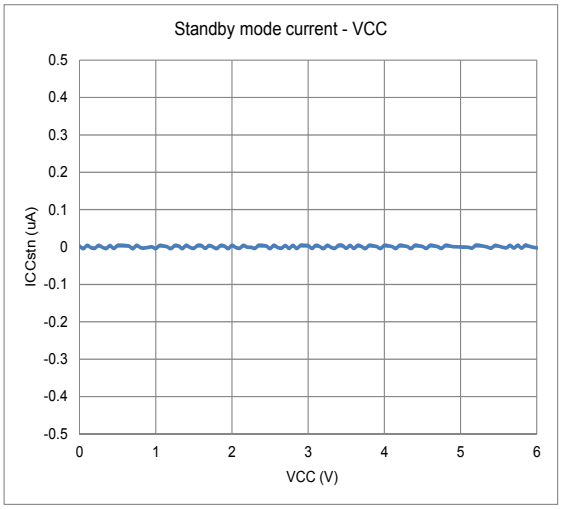


Figure 7. Standby Mode Current vs VCC Voltage

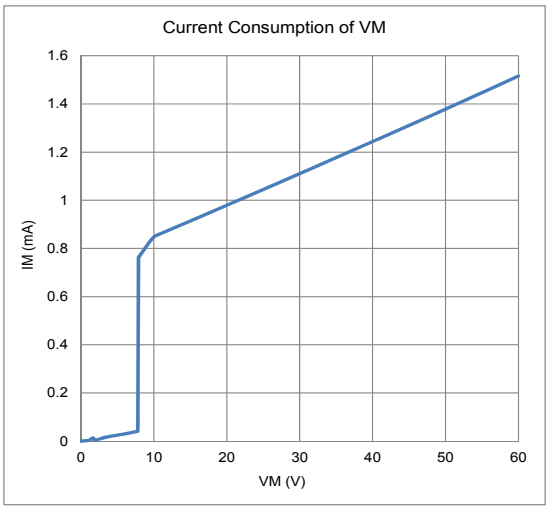


Figure 8. Current Consumption(I_M) vs VM Voltage

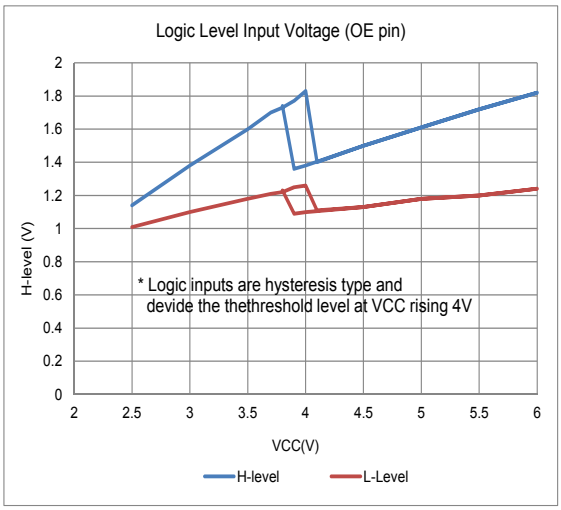


Figure 9. Logic H/L-Level Input Voltage (except ST pin) vs VCC Voltage

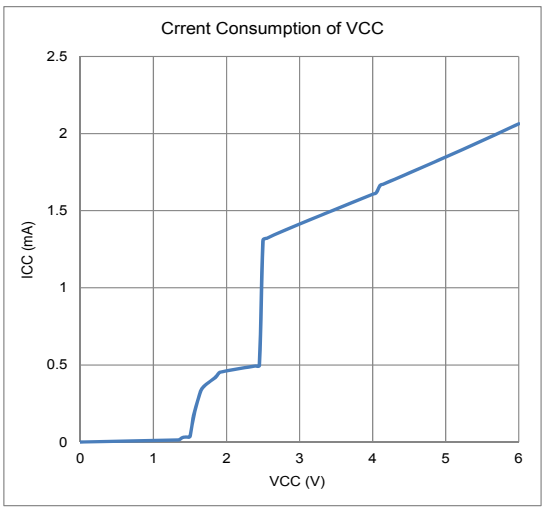


Figure 10. Current Consumption (I_{CC}) vs VCC Voltage

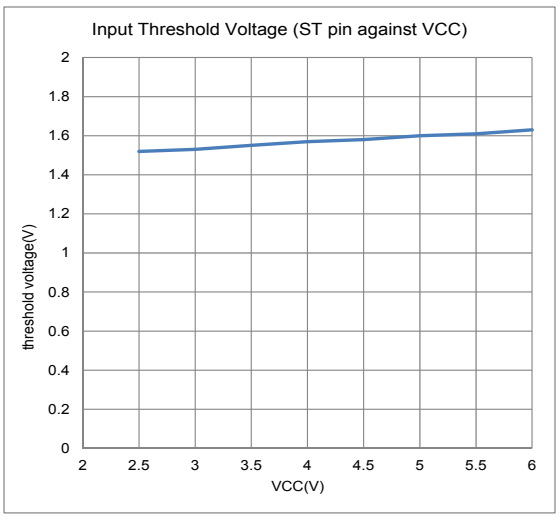


Figure 11. ST pin Input Threshold Voltage vs VCC Voltage

TYPICAL CHARACTERISTICS (CONTINUED)

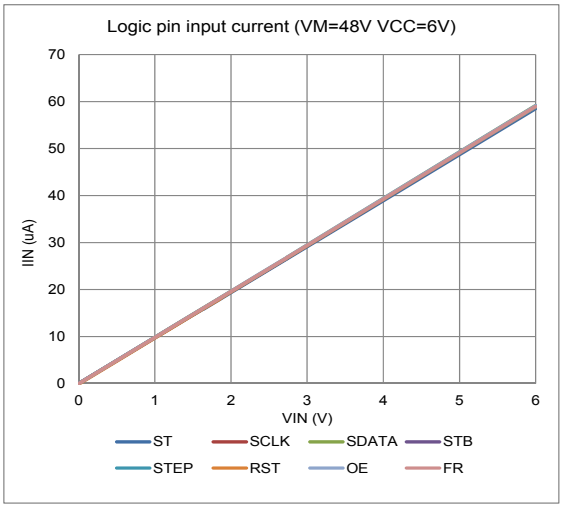


Figure 12. Logic Input Current vs Input Voltage

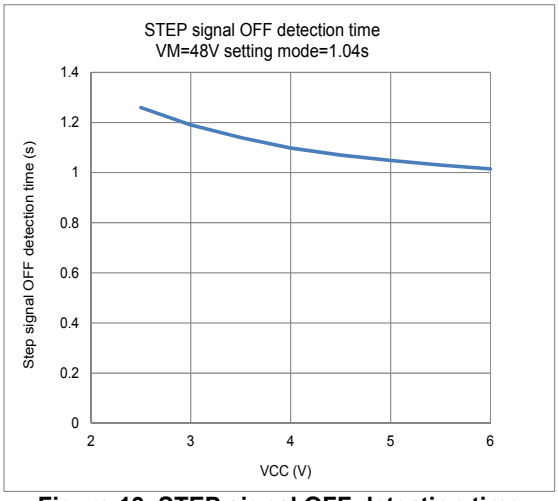


Figure 13. STEP signal OFF detection time vs VCC Voltage

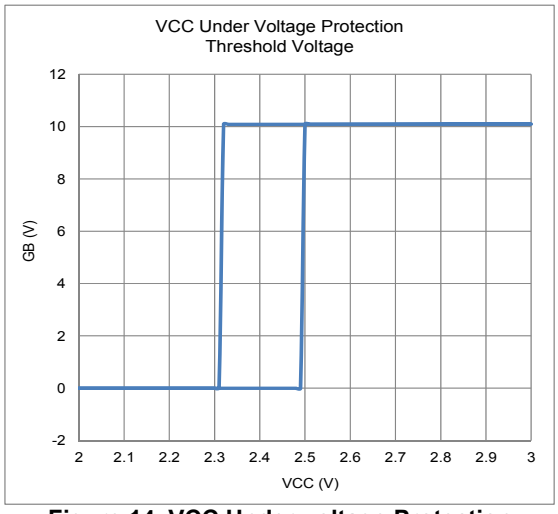


Figure 14. VCC Under-voltage Protection Threshold Voltage vs VCC Voltage

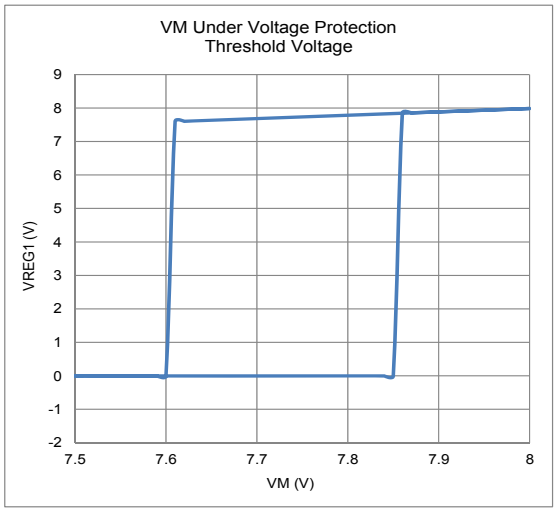


Figure 15. VM Under-voltage Protection Threshold Voltage vs VM Voltage

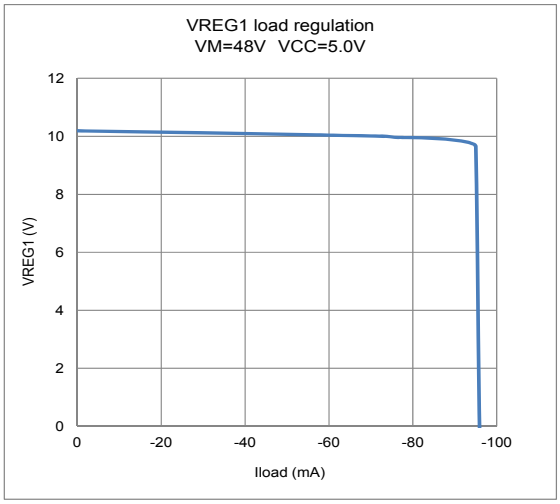


Figure 16. VREG1 Output Voltage vs VREG1 Load Current

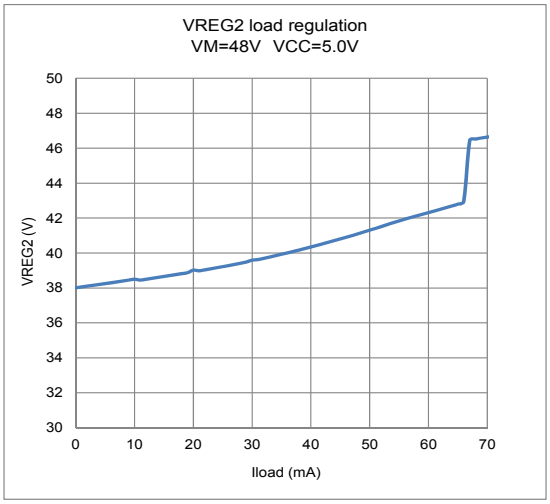


Figure 17. VREG2 Output Voltage vs VREG2 Load Current

TYPICAL CHARACTERISTICS (CONTINUED)

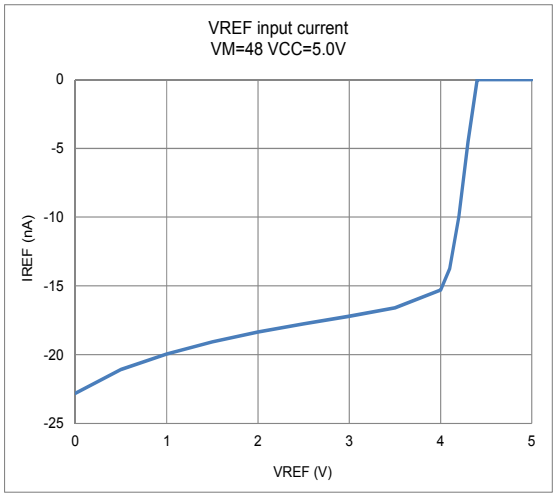


Figure 18. VREF pin Input Current (I_{REF}) vs VREF Voltage

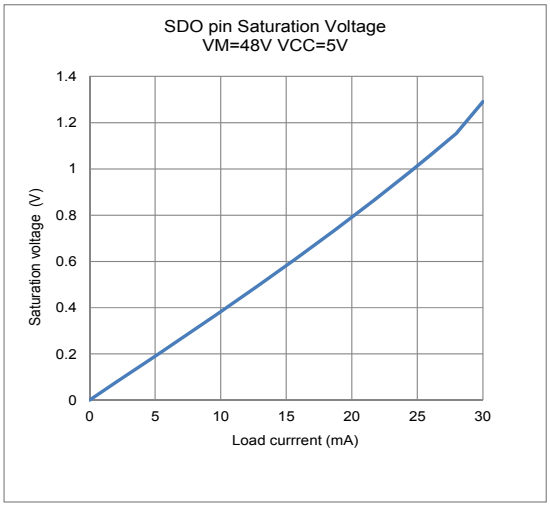


Figure 19. SDO pin Saturation Voltage vs SDO Load current

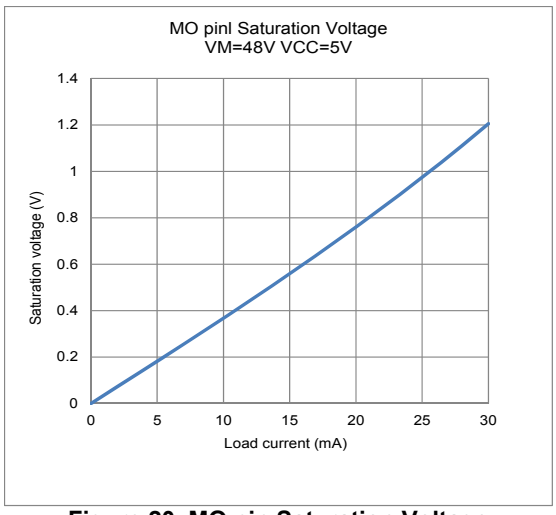


Figure 20. MO pin Saturation Voltage vs MO Load Current

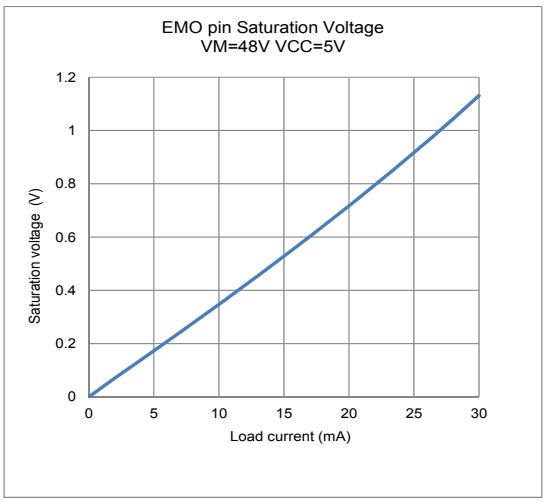


Figure 21. EMO pin Saturation Voltage vs EMO Load Current

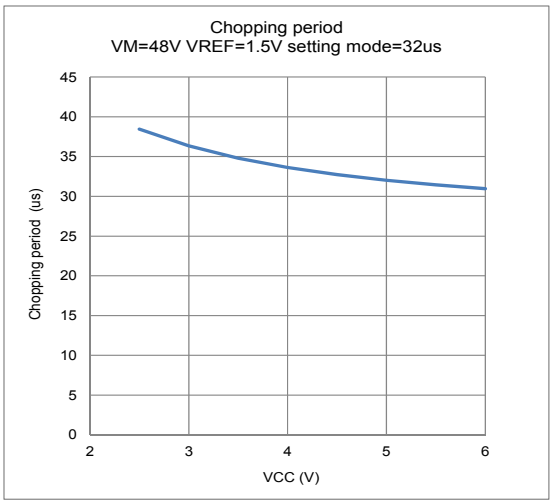


Figure 22. PWM (Chopping) Period vs VCC Voltage

FUNCTIONAL DESCRIPTION

Power Supply Input (VM, VCC)

The LV8726 has two power supply pins, VM and VCC. VM is the motor power supply rail which is also connected externally to the power MOSFETs. VCC supplies power to internal circuits. It is highly recommended to provide a decoupling capacitor of 100μF for each position close to the VM pin and VM line of external MOSFETs on the application board.

Driver Pins (GUx, GBx and OUTx)

The pins GUx are the high side P-MOSFET gate driver outputs, and GBx are the low side N-MOSFET gate driver outputs. The pins OUTx are the voltage sense inputs used for the over-current protection function to measure the P-MOSFET voltage between drain and source. The channel pairing is shown in the following table.

Table 1: External MOSFETs Connection

Channel	P-MOS gate	P-MOS drain	N-MOS gate	Motor coil
1	GU1	OUT1	GB1	1A
	GU2	OUT2	GB2	1B
2	GU3	OUT3	GB3	2A
	GU4	OUT4	GB4	2B

Refer to the APPLICATION CIRCUIT EXAMPLE of page 3.

Internal Voltage Regulator for N-MOSFETs (VREG1)

This 10V regulator provides required biasing for low side N-MOSFET gate drivers. The output of this regulator is connected to pin VREG1. Do not use VREG1 to drive any external load. It is recommended to connect a 0.1μF decoupling capacitor between VREG1 pin and GND.

Internal Voltage Regulator for P-MOSFETs (VREG2)

This regulator provides required biasing for high side P-MOSFET gate drivers at 10V below VM. The output of this regulator is connected to pin VREG2. Do not use VREG2 to drive any external load. It is recommended to connect a 0.1μF decoupling capacitor between VREG2 and VM.

Standby Mode (ST)

When pin ST is pulled down to GND, the device enters standby mode: all power MOSFETs are turned off, and, all logic as well as the step counter are reset.
When ST pin is pulled to High, the device enters active mode. The motor is excited at the home position. A rising edge at the STEP pin will advance the motor (which direction). Refer to Table 5 of page 16 for the home position.

Table 2: Operating Mode control by ST pin

ST	Operating mode	Internal regulator
L	Standby	Standby
H	Active	Active

Initialize Step Position Pin (RST)

While pin RST is set High, the home position is excited. After RST is released (Low), the first rising edge of STEP pulse advances the step. The position monitor output (MO pin) indicates that the output state is in the home position by outputting Low level.

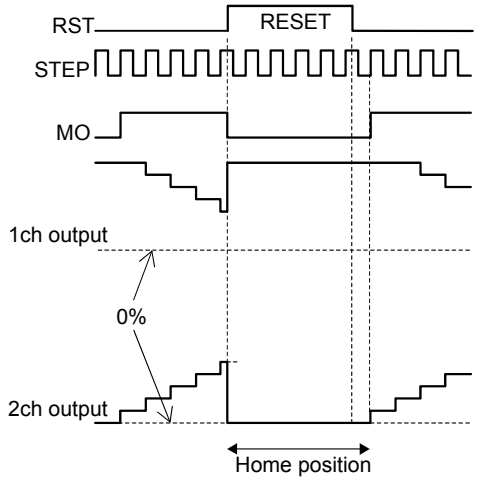


Figure 23. Initialize Step Position (RST)

Output Enable Pin (OE)

While OE pin is High, the output power MOSFETs are turned off. During the output disabled, the internal step sequencer keeps operation, advancing the step position based on the clock at STEP pin.

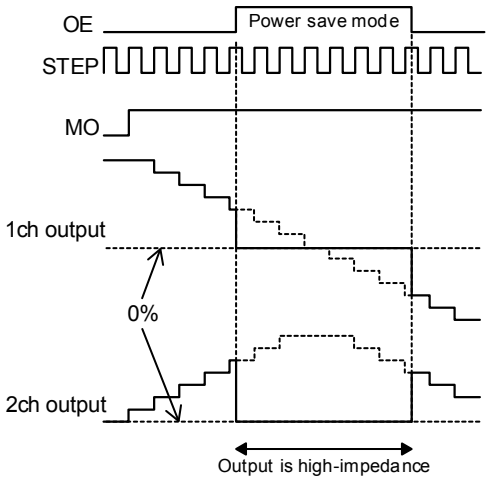


Figure 24. Example of Output Enable (OE)

Summary of System Mode Control (ST, OE, RST)
The following table shows the summary of the system mode control function with ST, OE and RST pins.

Table 3: System Mode Control

ST	OE	RST	Output	Step position
L	*	*	High impedance	-
H	H	H	High impedance	Home position
H	H	L	High impedance	Based on STEP signal
H	L	H	Active	Home position
H	L	L	Active	Based on STEP signal

Step Clock Signal Input Pin (STEP)
A rising edge of the step clock signal at STEP pin advances the step position of the stepper motor by advancing the electrical angle of the excitation current for the motor coils. The number of steps for 90 degree of an electrical cycle (i.e. resolution) is determined by the register bits which are accessible through the serial interface.

Table 4: Step Position Control by STEP pin

ST	STEP	Operating mode
L	*	Standby mode
H		Advancing step position
H		step position is kept

Table 5: Micro Step Resolution Setting

Bit setting (D1=0, D0=0)				Micro step resolution: STEPMODE	Home position	
D5	D4	D3	D2		1ch current	2ch Current
0	0	0	0	1/2	100%	0%
0	0	0	1	1/4	100%	0%
0	0	1	0	1/8	100%	0%
0	0	1	1	1/16	100%	0%
0	1	0	0	1/32	100%	0%
0	1	0	1	1/64	100%	0%
0	1	1	0	1/128	100%	0%
0	1	1	1	1/3	100%	0%
1	0	0	0	1/6	100%	0%
1	0	0	1	1/12	100%	0%
1	0	1	0	1/36	100%	0%
1	0	1	1	1/5	100%	0%
1	1	0	0	1/10	100%	0%
1	1	0	1	1/20	100%	0%
1	1	1	0	1/50	100%	0%
1	1	1	1	1/100	100%	0%

Rotational Direction Control Pin (FR)
FR controls the progression of the electrical angle of the motor. When FR is Low, the direction is clockwise, and when FR is High, direction is counter-clockwise.

Table 6: Direction Control by FR pin

FR	Operating mode
Low	Clockwise (CW)
High	Counter-clockwise (CCW)

Figure 25 shows an example of the direction change with FR pin.

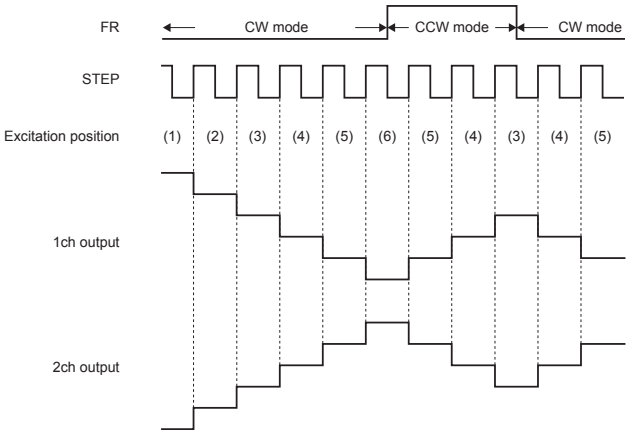


Figure 25. Example of Direction Reversal

Position Monitor Output Pin (MO)
The active low, open drain pin MO indicates the home position of the motor. An example of pin MO waveform is as shown Figure 44 and Figure 45 of page 33 and 34.

Current Control Setting (VREF, RF1, RF2)

The LV8726 implements a current sense mechanism for each channel using external shunt resistors.

To control a coil current, a RFx pin is provided for each channel. A resistor connected at this RFx pin defines the current gain of the coil current.

The resistive voltage generated by the coil current is sensed by the RFx pin and the output duty cycle is adjusted so that the RFx voltage level is equal to the internal reference voltage (Equation 1). The reference voltage is determined by the input voltage level at VREF pin and the programmable attenuator. For this VREF pin, it is required to provide an external constant voltage source circuit. Refer to RECOMMENDED OPERATING RANGES of page 10 for VREF range.

Table 7: VREF Attenuation Ratio Setting

Bit setting (D1=0, D0=1)			V_{REF} (Reference voltage) attenuation ratio: VREFATT
D4	D3	D2	
0	0	0	100%
0	0	1	90%
0	1	0	80%
0	1	1	70%
1	0	0	60%
1	0	1	50%
1	1	0	40%
1	1	1	30%

The output current calculation method for using of attenuation function of the VREF input voltage is as shown in Equation 1.

Equation 2 is utilized to calculate the coil peak current, I_{OUT}.

$$I_{OUT} \cdot R_{RFx} = \frac{V_{REF}}{5} \cdot ATT_{RATIO} \ldots\ldots\ldots (1)$$

$$I_{OUT} = \frac{V_{REF} \cdot ATT_{RATIO}}{5 \cdot R_{RFx}} \ldots\ldots\ldots (2)$$

Where,

I_{OUT} : Coil current [A]
R_{RFx} : Resistor between RFx and GND [Ω]
V_{REF} : Input voltage at the VREF pin [V]
ATT_{RATIO} : Attenuator Ratio for the VREF pin

For example, in case of

$R_{RFx} = 0.1[\Omega]$
$V_{REF} = 1.5[\mathrm{V}]$
ATT_{RATIO}=1.0 (100%)

The coil current is

$$I_{OUT} = \frac{1.5 \times 1.0}{5 \times 0.1} = 3.0[\mathrm{A}]$$

The LV8726 provides the built-in current vector generator. The current ratio between channel 1 and 2 are preset based on cosine and sine element individually.

PWM Constant-Current Control Ratio

The LV8726 implements constant current control drive by applying a PWM to pins GUx and GBx.

When a coil current reaches the set target value, the constant current control mechanism gets activated and performs a repetitive sequence of Charge and Decay operations as shown Figure 30-32 of page 22 and 23.

The target value is generated based on the step clock pulse number. The angle of one step θ is

$$\theta = 90° \cdot S \ldots\ldots\ldots (3)$$

Where,

θ : Angle of micro step [deg]
S : Micro step (1/2, … 1/128)

The n-th current ratio can be represented by

$$\begin{pmatrix} RATIO_{CH1}(n) \\ RATIO_{CH2}(n) \end{pmatrix} [\%] = \begin{pmatrix} cos(\theta n) \\ sin(\theta n) \end{pmatrix} \cdot 100 \ldots\ldots\ldots (4)$$

The n-th current value can be represented by

$$\begin{pmatrix} I_{CH1}(n) \\ I_{CH2}(n) \end{pmatrix} = I_{OUT} \begin{pmatrix} cos(\theta n) \\ sin(\theta n) \end{pmatrix} \ldots\ldots\ldots (5)$$

Where,

n : the position number of STEP from 0 to 1/S

For example, in case of

$S = 1/128\ step$
$n = 32$

The θ32 is

$$\theta 32 = 90° \cdot \frac{32}{128} = 22.5°$$

Each current ratio is

$RATIO_{CH1}(32) = cos(22.5°) \cdot 100 \approx 92[\%]$
$RATIO_{CH2}(32) = sin(22.5°) \cdot 100 \approx 38[\%]$

Equation 4 represents the theoretical calculation. The actual current ratio between the channel 1 and 2 is the preset value as shown in Table 10-12 of page 28, 30 and 32. In case of 1/128 micro step case, the preset values are plotted in Figure 41 of page 29. The current waveforms for some micro step settings are illustrated in Figure 44-1., Figure 45-1, Figure 46-1.

Output Pin for STEP Input Monitoring (SDO)
The step clock signal at pin STEP is monitored by an internal counter. When the interval time of the rising edge is longer than timeout criteria, open drain pin SDO goes Low. The timeout period is selectable by the register bits shown in the following table. The example of detection timing is illustrated in Figure 26.

Table 8: STEP Signal OFF Detection Time Setting

Bit setting (D1=0, D0=1)	STEP signal OFF detection time: TSDO
D7	
0	0.52sec
1	1.04sec

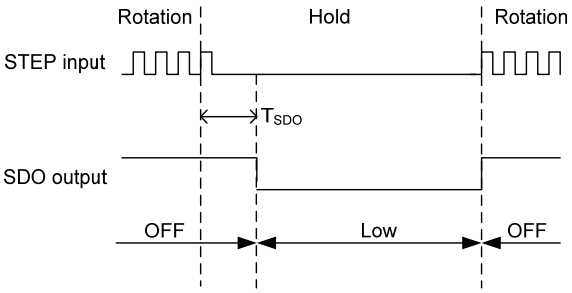


Figure 26. Example of SDO Timing

SDO Output for Current Reduction
To avoid to applying high current to a motor coil for long term at one step position, the SDO output may be used to reduce the reference current. SDO is asserted when the step clock interval is longer than T_{SDO}. With the circuit is shown in Figure 27. VREF voltage can be reduced in case of an SDO assertion.

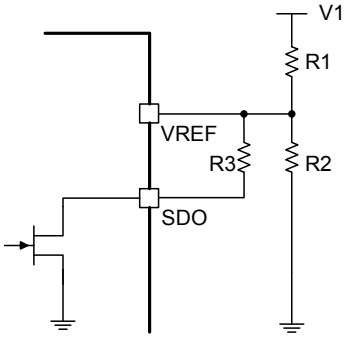


Figure 27. VREF Voltage Attenuation Circuit

Fault Detection Output (EMO)
When a fault event is detected, open drain pin EMO goes Low. The fault event is selectable by register from the following four conditions.

Table 9: Fault Detection Output Setting

Bit setting (D1=0, D0=0)		Fault detection output: EMOSEL
D7	D6	
0	0	Over-current detection
0	1	None
1	0	VM low voltage < 7.6V (typ)
1	1	Thermal Shutdown

The all fault protection functions always work regardless of the EMO output selection.

Serial Interface (ST, SDATA, SCLK, STB)
The LV8726 has registers to program settings and parameters which are accessed through the serial interface. It consists of the following three pins:

1. STB: When STB is Low, SDATA is input at the rising edge of SCLK. SCLK signal is not accepted when STB is High. The transmitted data is latched at the rising edge of STB.
2. SDATA: LSB first 8-bit word. Its direction is from external processor to the device. The written data cannot be read back.
3. SCLK: Serial clock. The device fetches each data bit at the rising edge of the clock.

The settings of 'Micro step resolution' and 'Decay mode' are taking effect at the first rising edge of STEP after a register write. Other settings are active immediately after a register change.
When more than eight bits of data were received, the latest eight bits are considered effective data. During standby mode (ST=Low), the registers cannot be accessed and all logic is reset.

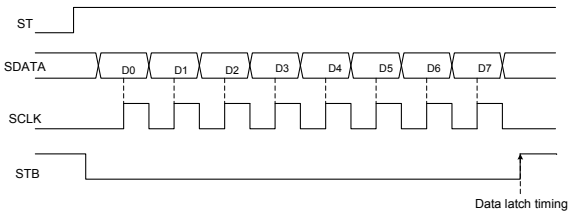


Figure 28. Serial Interface Timing Chart

Register Map

The following Figure shows the register map. The two lowest bits are assigned for selecting one of four addresses.

D7	D6	D5	D4	D3	D2	D1	D0	Address
EMOSEL		STEPMODE				ADDR1	ADDR0	00
TSDO	DECAY		VREFATT					01
TPWM		TOFF		TBLANK				10
NA	NA	NA	NA	OCM	OCE			11

Figure 29. Register Map

ADDR D[1:0]: 00 (Address 00)

D7	D6	D5	D4	D3	D2	D1	D0
EMOSEL		STEPMODE				0	0

STEPMODE D[5:2]

Step mode setting

D5	D4	D3	D2	Micro step resolution (Step mode)
0	0	0	0	1/2
0	0	0	1	1/4
0	0	1	0	1/8
0	0	1	1	1/16
0	1	0	0	1/32
0	1	0	1	1/64
0	1	1	0	1/128
0	1	1	1	1/3
1	0	0	0	1/6
1	0	0	1	1/12
1	0	1	0	1/36
1	0	1	1	1/5
1	1	0	0	1/10
1	1	0	1	1/20
1	1	1	0	1/50
1	1	1	1	1/100

EMOSEL D[7:6]

Fault detection output select for EMO output

D7	D6	Fault detection output
0	0	Over-current detection
0	1	None
1	0	VM low voltage < 7.6V (typ)
1	1	Thermal shutdown

ADDR D[1:0] : 01 (Address 01)

D7	D6	D5	D4	D3	D2	D1	D0
TSDO	DECAY		VREFATT			0	1

VREFATT D[4:2]

Attenuator ratio for VREF

D4	D3	D2	V_{REF} attenuation ratio
0	0	0	100%
0	0	1	90%
0	1	0	80%
0	1	1	70%
1	0	0	60%
1	0	1	50%
1	1	0	40%
1	1	1	30%

DECAY D[6:5]

Selection of Decay mode:

In the case of 25%FAST at Mixed decay, 25% of the PWM period operates with Fast decay mode.

In the case of 50%FAST at Mixed decay, 50% of the PWM period operates with Fast decay mode.

D6	D5	Decay mode: DECAY
0	0	Mixed (25% Fast)
0	1	Mixed (50% Fast)
1	0	Slow
1	1	Fast

TSDO D[7]

STEP signal OFF detection time

D7	Step signal OFF detection time: TSDO
0	0.52sec
1	1.04sec

ADDR D[1:0]: 10 (Address 10)

D7	D6	D5	D4	D3	D2	D1	D0
TPWM		TOFF		TBLANK		1	0

TBLANK D[3:2]

Blanking time: During this period, the mode is not switched from Charge to Decay even if the comparator detects the coil current higher than the target current.

D3	D2	Blanking time
0	0	0.5μs
0	1	1.0μs
1	0	2.0μs
1	1	4.0μs

TOFF D[5:4]

Time for turning off the MOSFETs to avoid shoot through current

D5	D4	Through current protector OFF time
0	0	0.5μs
0	1	1.0μs
1	0	2.0μs
1	1	4.0μs

TPWM D[7:6]

PWM (Chopping) period

D7	D6	PWM (Chopping) period
0	0	8μs
0	1	16μs
1	0	24μs
1	1	32μs

ADDR D[1:0]: 11 (Address 11)

D7	D6	D5	D4	D3	D2	D1	D0
NA	NA	NA	NA	OCM	OCE	1	1

OCE D[2]

Turn on/off the over-current protection function

D2	Over-current protection
0	ON
1	OFF

OCM D[3]

Over-current protection mode

D3	Over-current protection mode
0	Latch type
1	Auto reset type

The output is turned off at the over-current detection. In case of the latch type, the outputs are turned off until the standby pin ST is set Low when over-current is detected with second detection at 256μs after the first detection. Refer to Figure 47 of page 36 for a timing chart of latch type. In case of the auto reset type, the output is turned on with 2ms interval.

Current Decay Mode Sequencing

LV8726 provides four selectable decay modes in one PWM period:

1. Mixed decay mode
   (Ratio is register programmable)
2. Slow decay mode
3. Fast decay mode

The description of the mixed decay sequence covers all operation modes in detail. For slow and fast decay operation only, the selected mode (slow, fast) covers the entire decay period. Figures 30-32 show the sequence of events in detail.

Mixed Decay Sequence

In Mixed Decay operation the following charge-discharge sequence of three steps is applied assuming a current direction from "A" to "B". Refer to Figure 33 and Figure 34 of page 24 for the timing chart of PWM based constant-current by Mixed decay:

1. During Charge operation the voltage VM is applied to the "A" side of the coil until the coil current exceeds the target. In case the current has already exceeded the target value at the end of blanking time, the Charge operation is directly changed over to Slow decay operation (3).
2. Next the device activates Slow decay until 50% (or 75%) of the PWM period depending on register setting. The slow decay shorts the coil to make the circulation current decrease slowly as seen in (3) event in Figure 30
3. For the remaining PWM period Fast decay is applied by reversing the voltage across the.

The operation is changed to Charge again from Fast decay. During transition from the upper MOSFET to the lower MOSFET of the same leg a programmable dead time period avoids turning on both MOSFETs at the same time. During this dead time, the coil current flows through the body diode of the MOSFET as seen in (2), (4) and (6) events in Figure 30. Dead time is determined by the register bits through the serial interface.

For Slow decay and Fast decay mode, the coil current flows through the body diode as shown in (2) event in Figure 31 and Figure 32 same as Mixed decay.

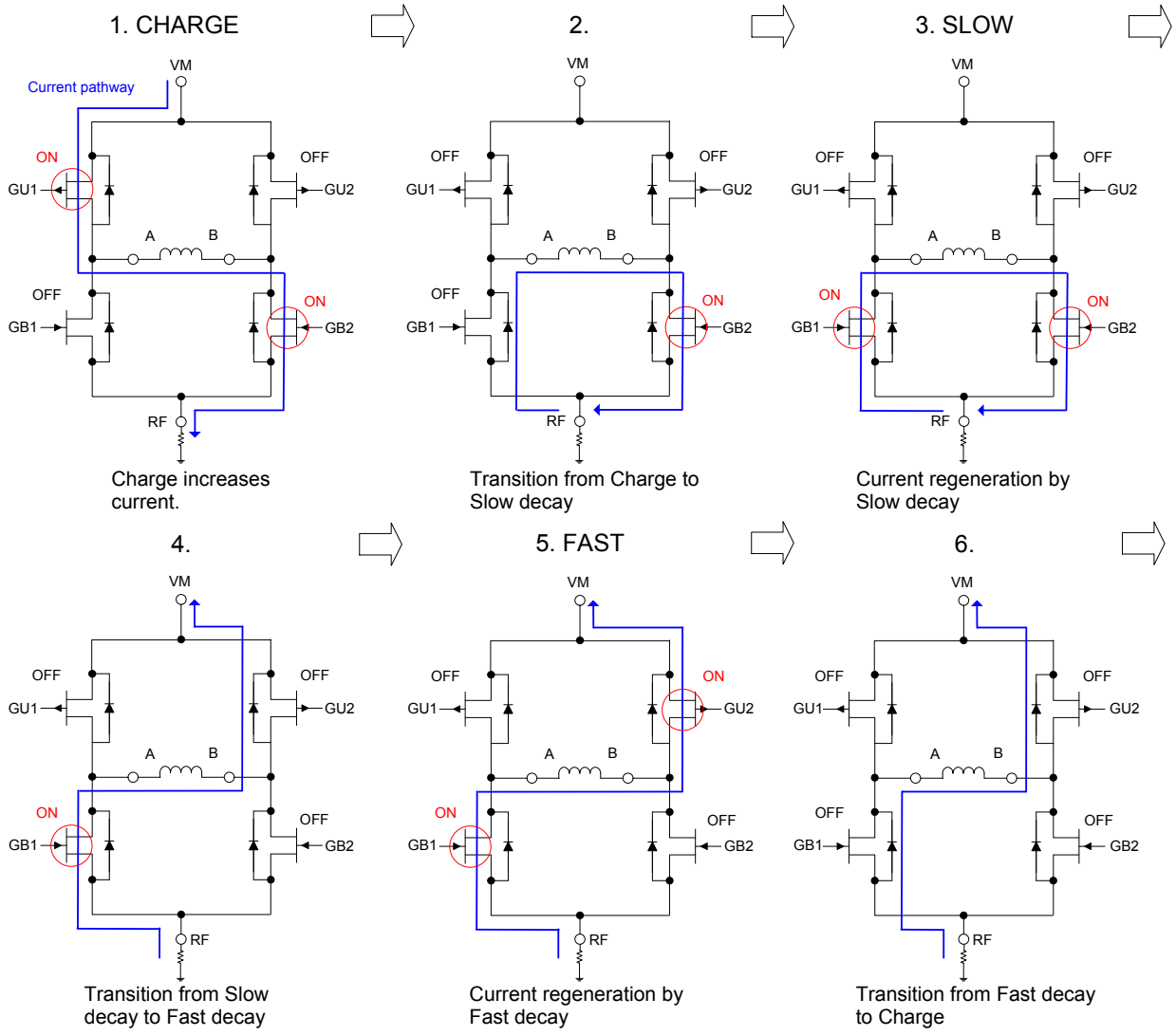


Figure 30. Mixed Decay Sequence

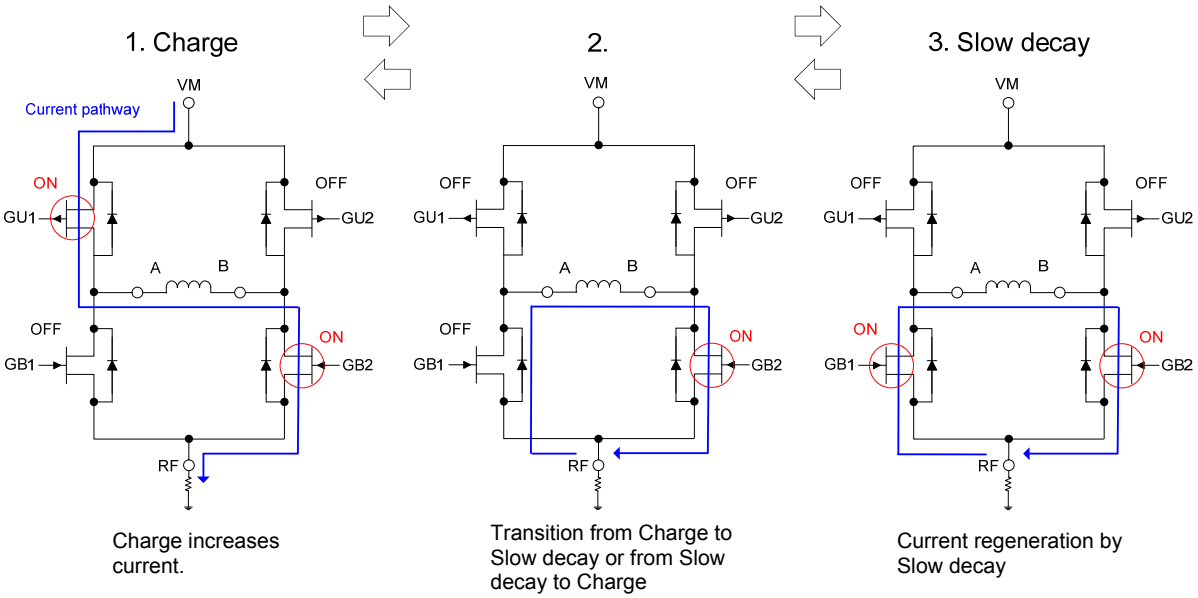


Figure 31. Slow Decay Sequence

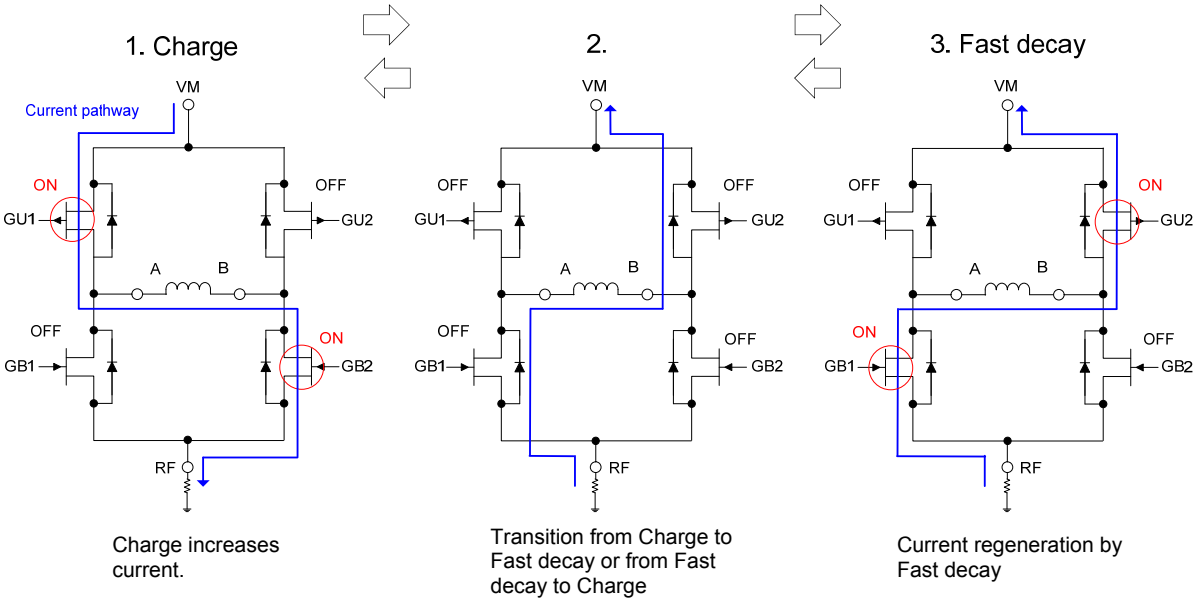


Figure 32. Fast Decay Sequence

Timing Chart of PWM Constant-Current Control

When the current control mode is switched from Decay mode to Charge mode, a noise in the current sense resistance occurs by a recovery current, and it may erroneously detect the voltage of the sense pin. Blanking time is provided in order to prevent this erroneous detection. During this period, the mode is not switched from Charge to Decay even if the comparator detects the coil current higher than the target current.

Mixed decay current control

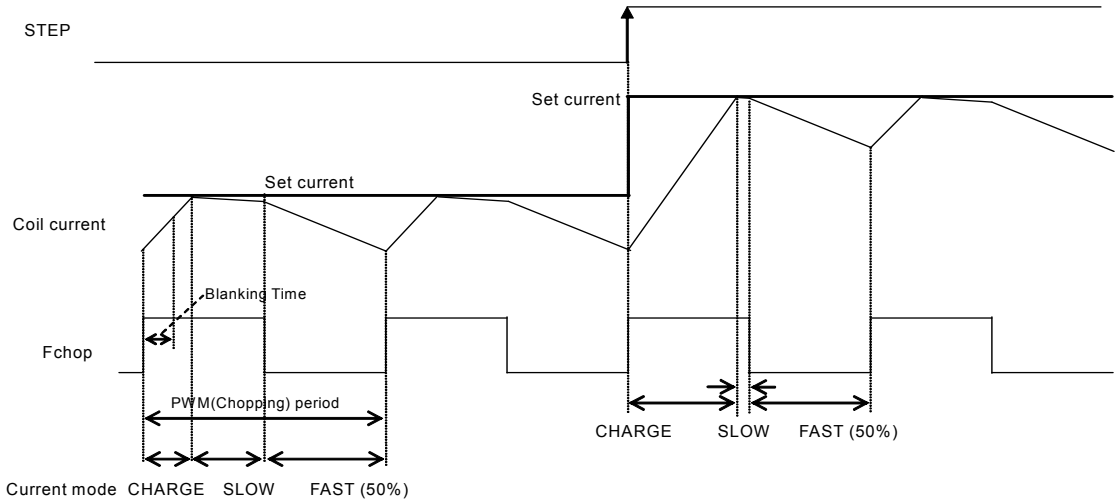


Figure 33. Mixed Decay (50%FAST) Rising Slope

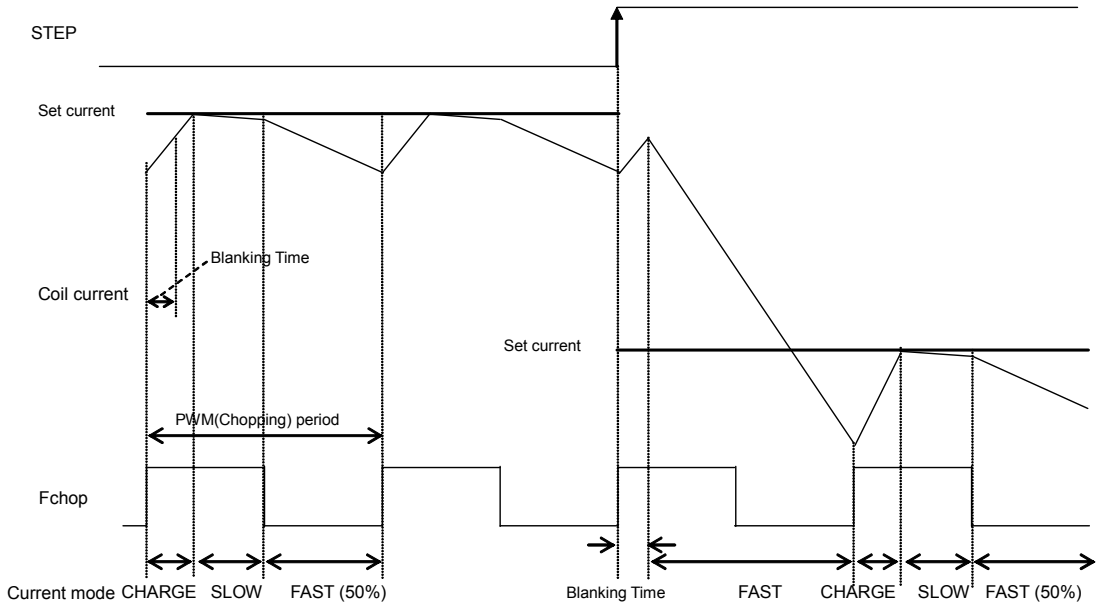


Figure 34. Mixed Decay (50%FAST) Falling Slope

When a coil current reached the set current, external MOSFETs are repeated Charge mode-> Slow decay mode-> Fast decay mode according to PWM period. The coil current is controlled constant-current by repeating three modes.

As for the Fast period, it is selectable in 50% and 25% of PWM period by serial interface.

The coil current (ICOIL) and set current (IREF) are compared in blanking time.

When ICOIL < IREF:

The Charge mode is continued until ICOIL ≥ IREF. If ICOIL reaches IREF, the mode is switched to Slow decay mode, and then is changed Fast decay mode.

When ICOIL > IREF:

The Fast decay mode begins. The coil current is attenuated in the Fast decay mode till one PWM period is over.

Slow decay current control

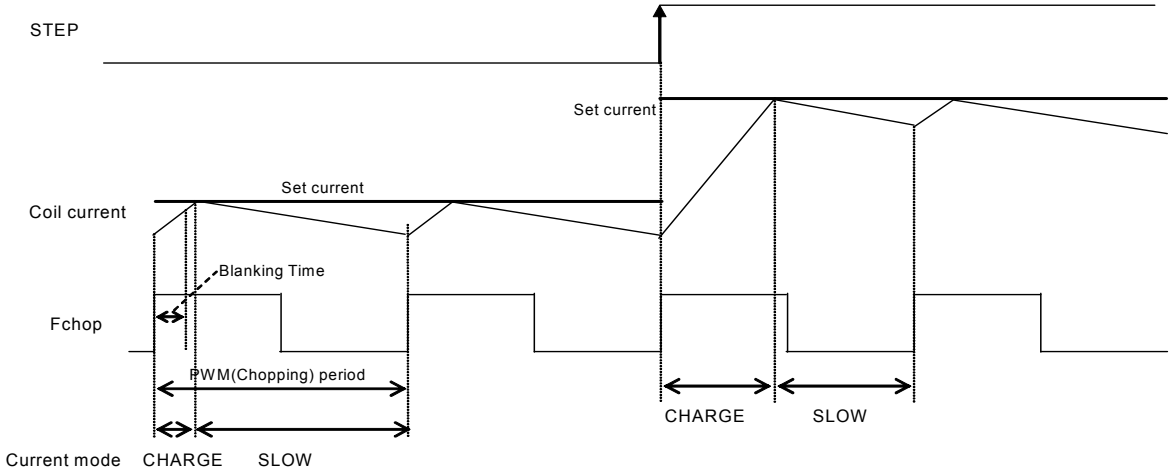


Figure 35. Slow Decay Rising Slope

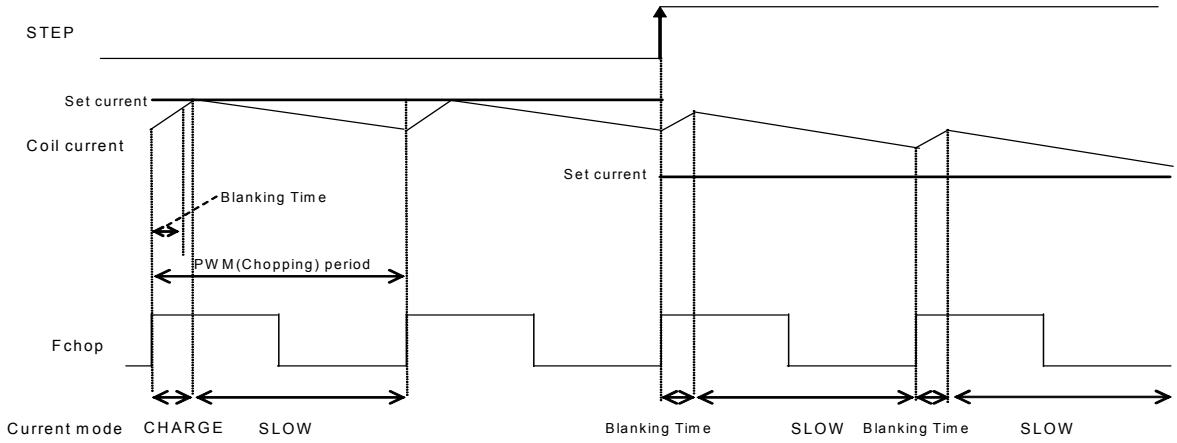


Figure 36. Slow Decay Falling Slope

When a coil current reached the set current, external MOSFETs are repeated Charge mode-> Slow decay mode according to PWM period. The coil current is controlled constant-current by repeating two modes.