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Ordering number : ENA1702D

LV8729V

Bi-CMOS IC

PWM Constant-Current Control Stepper Motor Driver

ON Semiconductor®

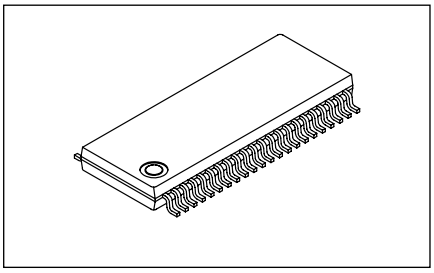
http://onsemi.com

Overview

The LV8729V is a PWM current-controlled microstep bipolar stepper motor driver.
This driver can perform eight times of excitation of the second phase to 32W1-second phase and can drive simply by the CLK input.

Function

- Single-channel PWM current control stepper motor driver.
- BiCDMOS process IC.
- Output on-resistance (upper side : 0.35Ω ; lower side : 0.3Ω ; total of upper and lower : 0.65Ω ; Ta = 25°C, I_O = 1.8A)
- 2-phase, 1-2 phase, W1-2 phase, 2W1-2 phase, 4W1-2 phase,8W1-2 phase, 16W1-2 phase, 32W1-2 phase excitation are selectable.
- Advance the excitation step with the only step signal input.
- Available forward reverse control.
- Over current protection circuit.
- Thermal shutdown circuit.
- Input pull down resistance
- With reset pin and enable pin.



SSOP44K (275mil)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VM max	VM , VM1 , VM2	36	V
Maximum output current	I_O max	Per 1ch	1.8	A
Maximum logic input voltage	V_{IN} max	ST , MD1 , MD2 , MD3 , OE , RST , FR ,	6	V
Maximum VREF input voltage	VREF max		6	V
Maximum MO input voltage	V_{MO} max		6	V
Maximum DOWN input voltage	V_{DOWN} max		6	V
Allowable power dissipation	Pd max	*	3.85	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 90.0mm×90.0mm×1.6mm, glass epoxy 2-layer board, with backside mounting.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 21 of this data sheet.

June, 2014

619114NK/42413NK 20121220-S00010 No.A1702-1/21

Allowable Operating Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VM	VM , VM1 , VM2	9 to 32	V
Logic input voltage	V_{IN}	ST , MD1 , MD2 , MD3 , OE , RST , FR , STEP	0 to 5	V
VREF input voltage range	VREF		0 to 3	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, VM = 24V, VREF = 1.5V

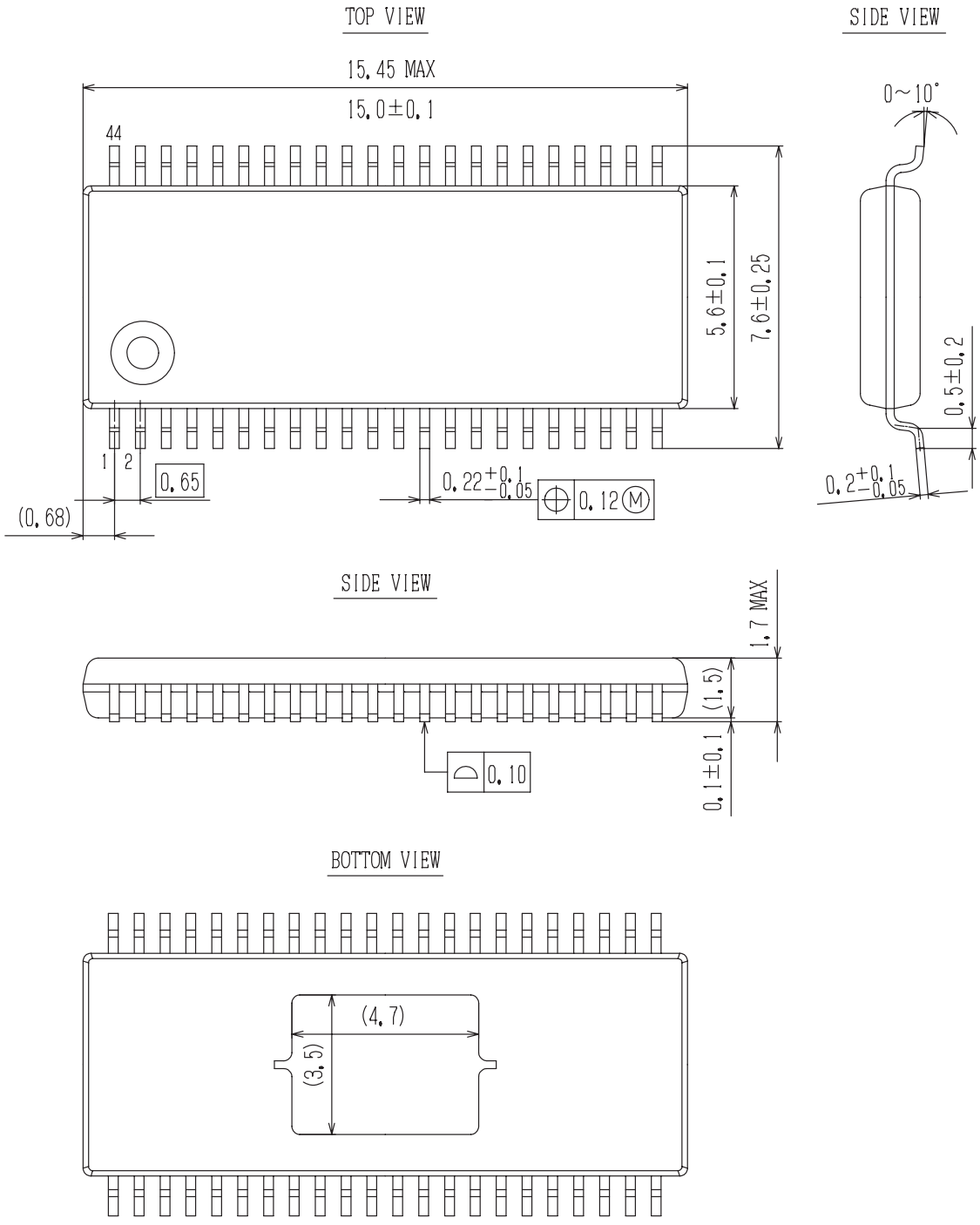
Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Standby mode current drain		I_Mst	ST = "L" , VM+VM1+VM2		70	100	μA
Current drain		IM	ST = "H", OE = "H", no load VM+VM1+VM2		3.3	4.6	mA
Thermal shutdown temperature		TSD	Design guarantee	150	180	200	°C
Thermal hysteresis width		ΔTSD	Design guarantee		40		°C
Logic pin input current		I_{IN}L	ST , MD1 , MD2 , MD3 , OE , RST , FR , STEP , V_{IN} = 0.8V	3	8	15	μA
		I_{IN}H	ST , MD1 , MD2 , MD3 , OE , RST , FR , STEP , V_{IN} = 5V	30	50	70	μA
Logic input voltage	High	V_{IN}H	ST , MD1 , MD2 , MD3 , OE , RST , FR , STEP	2.0		5.0	V
	Low	V_{IN}L		0		0.8	V
Chopping frequency		Fch	Cosc1 = 100pF	70	100	130	kHz
OSC1 pin charge/discharge current		Iosc1		7	10	13	μA
Chopping oscillation circuit threshold voltage		Vtup1		0.8	1	1.2	V
		Vtdown1		0.3	0.5	0.7	V
VREF pin input voltage		Iref	VREF = 1.5V	-0.5			μA
DOWN output residual voltagr		V_O1DOWN	Idown = 1mA		40	100	mV
MO pin residual voltage		V_O1MO	Imo = 1mA		40	100	mV
Hold current switching frequency		Fdown	Cosc2 = 1500pF	1.12	1.6	2.08	Hz
Hold current switching frequency threshold voltage		Vtup2		0.8	1	1.2	V
		Vtdown2		0.3	0.5	0.7	V
VREG1 output voltage		Vreg1		4.7	5	5.3	V
VREG2 output voltage		Vreg2	V_M	18	19	20	V
Output on-resistance		Ronu	I_O = 1.8A, high-side ON resistance		0.35	0.455	Ω
		Rond	I_O = 1.8A, low-side ON resistance		0.3	0.39	Ω
Output leakage current		$I_O$leak	V_M = 36V			50	μA
Diode forward voltage		VD	I_D = -1.8A		1	1.4	V
Current setting reference voltage		VRF	VREF = 1.5V, Current ratio 100%	0.285	0.3	0.315	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

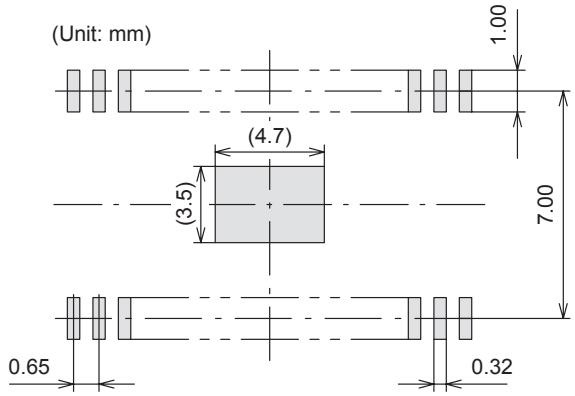
Package Dimensions

unit : mm (typ)

SSOP44K (275mil) Exposed Pad
CASE 940AF
ISSUE A



SOLDERING FOOTPRINT*

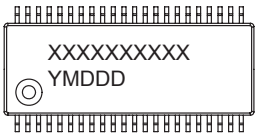


NOTES:

1. The measurements are for reference only, and unable to guarantee.
2. Please take appropriate action to design the actual Exposed Die Pad and Fin portion.
3. After setting, verification on the product must be done.
   (Although there are no recommended design for Exposed Die Pad and Fin portion Metal mask and shape for Through−Hole pitch (Pitch & Via etc), checking the soldered joint condition and reliability verification of soldered joint will be needed. Void ▪ gradient ▪ insufficient thickness of soldered joint or bond degradation could lead IC destruction because thermal conduction to substrate becomes poor.)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

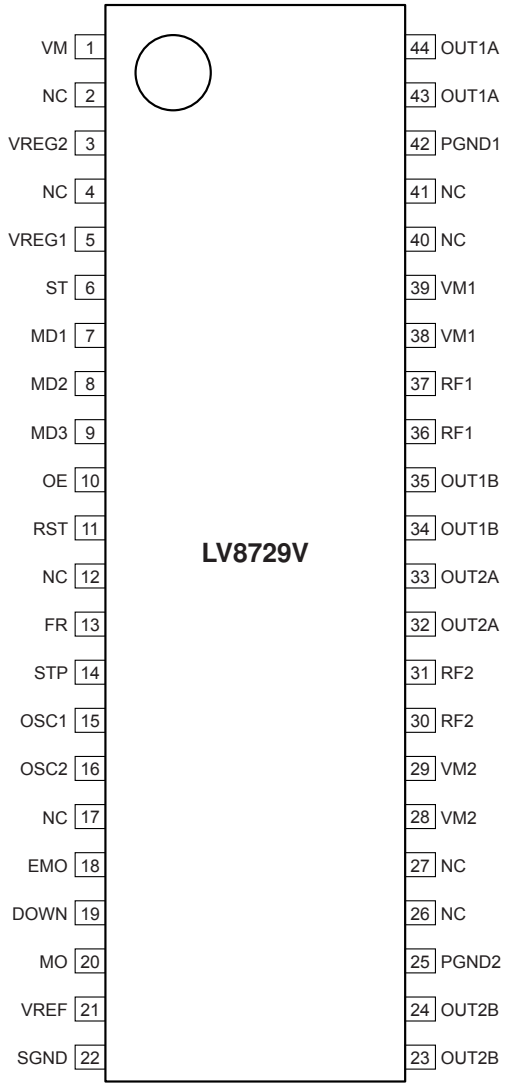
GENERIC
MARKING DIAGRAM*



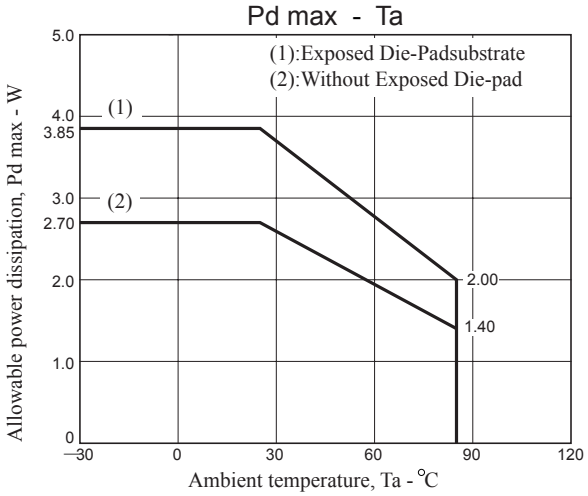
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

Pin Assignment

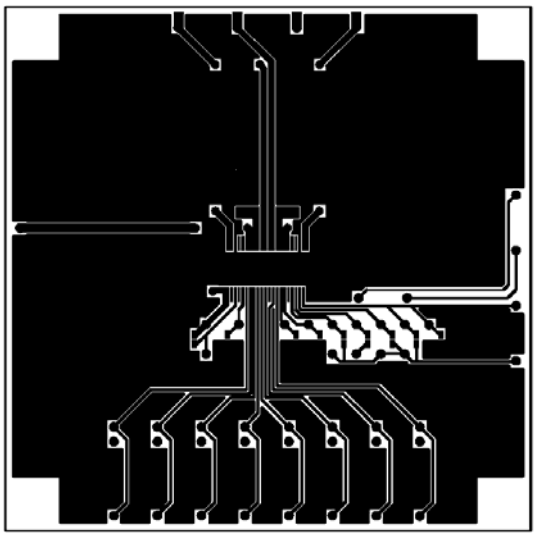


Top view

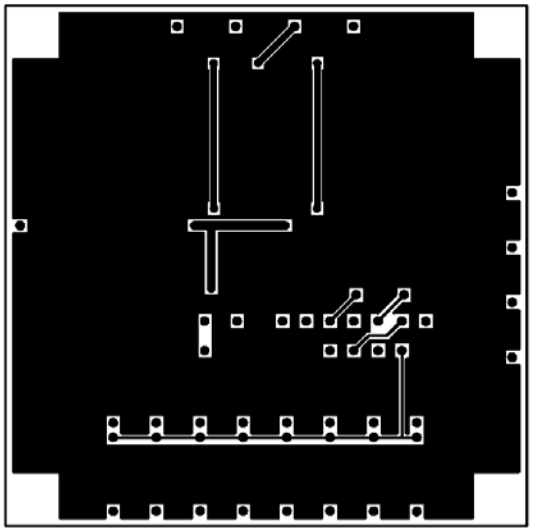


Substrate Specifications (Substrate recommended for operation of LV8729V)

Size : 90mm × 90mm × 1.6mm (two-layer substrate [2S0P])
Material : Glass epoxy
Copper wiring density : L1 = 85% / L2 = 90%



L1 : Copper wiring pattern diagram



L2 : Copper wiring pattern diagram

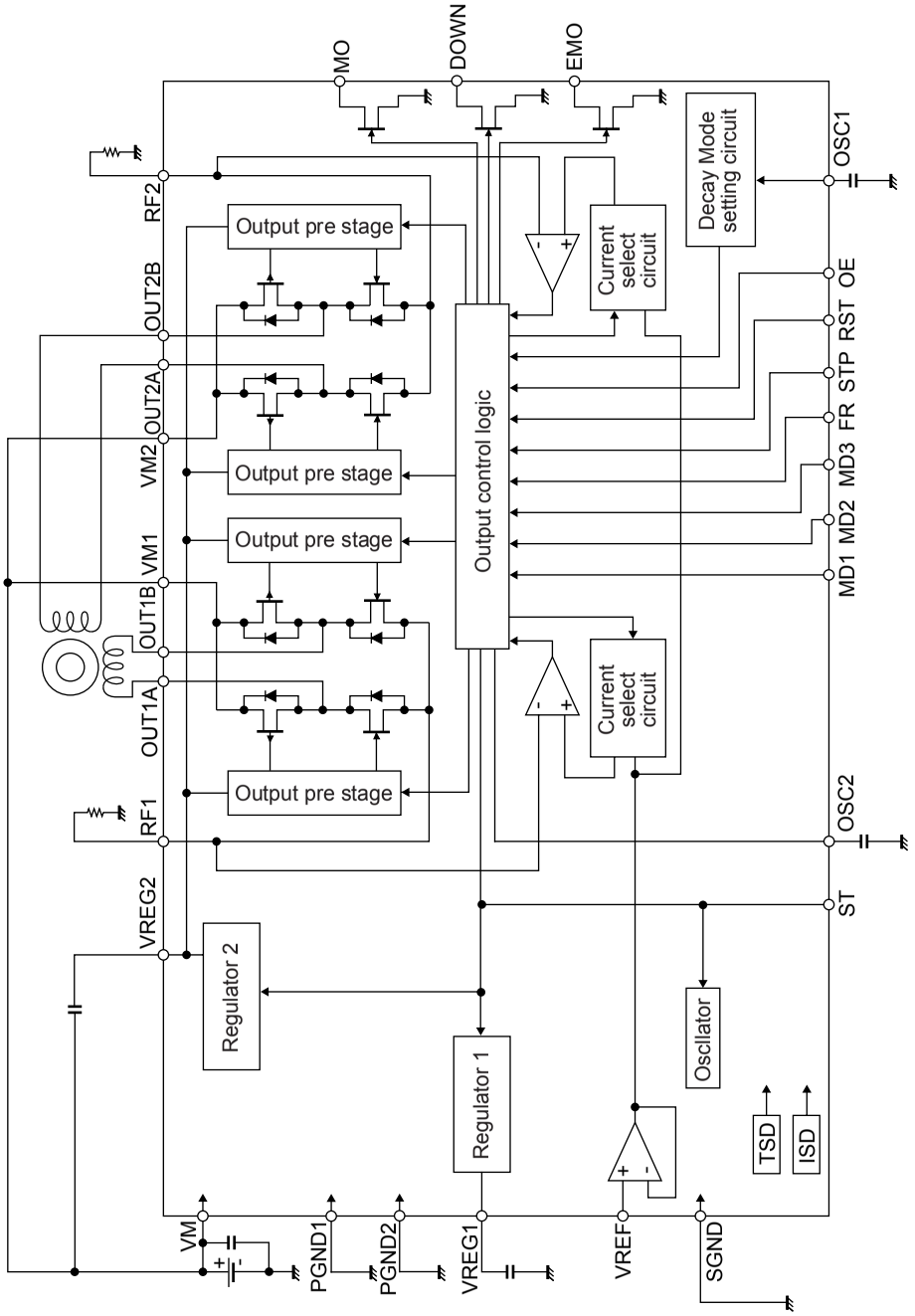
Cautions

1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.

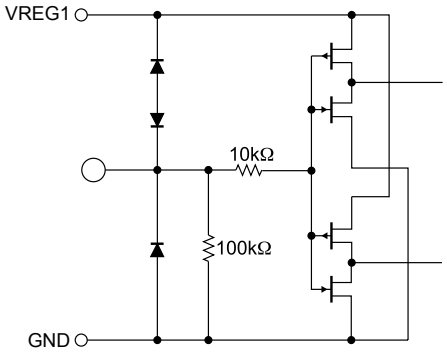
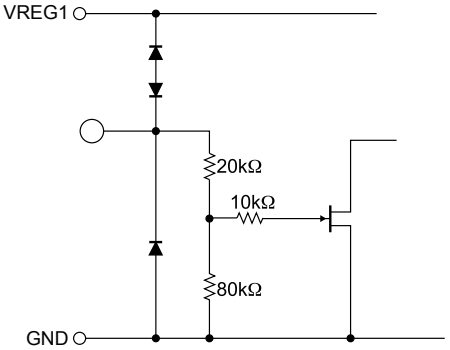
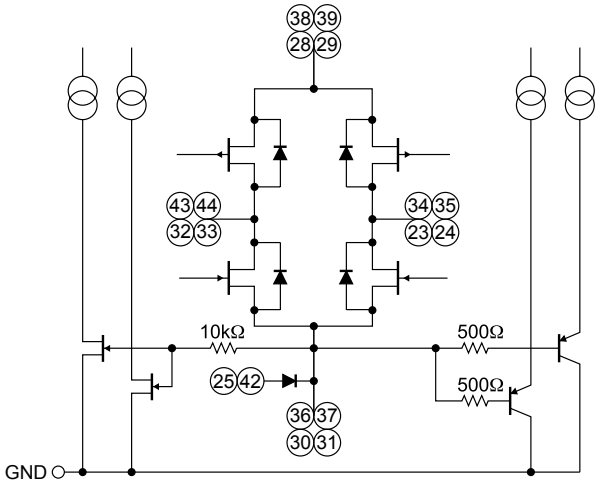
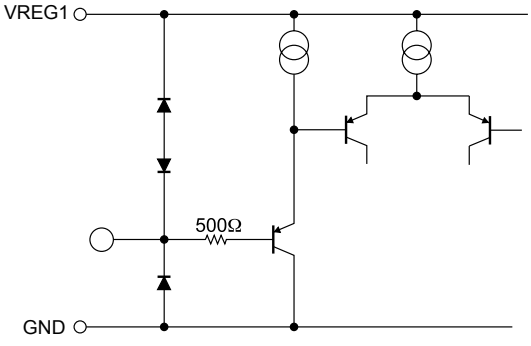
2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below :
(1)Maximum value 80% or less for the voltage rating
(2)Maximum value 80% or less for the current rating
(3)Maximum value 80% or less for the temperature rating

3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

Block Diagram



Pin Functions

Pin No.	Pin Name	Pin Functtion	Equivalent Circuit
7 8 9 10 11 13 14	MD1 MD2 MD3 OE RST FR STP	Excitation mode switching pin Excitation mode switching pin Excitation mode switching pin Output enable signal input pin Reset signal input pin Forward / Reverse signal input pin Step clock pulse signal input pin	
6	ST	Chip enable pin.	
23, 24 25 28, 29 30, 31 32, 33 34, 35 36, 37 38, 39 42 43, 44	OUT2B PGND2 V_M2 RF2 OUT2A OUT1B RF1 V_M1 PGND1 OUT1A	Channel 2 OUTB output pin. Channel 2 Power system ground Channel 2 motor power supply connection pin. Channel 2 current-sense resistor connection pin. Channel 2 OUTA output pin. Channel 1 OUTB output pin. Channel 1 current-sense resistor connection pin. Channel 1 motor power supply pin. Channel 1 Power system ground Channel 1 OUTA output pin.	
21	VREF	Constant-current control reference voltage input pin.	

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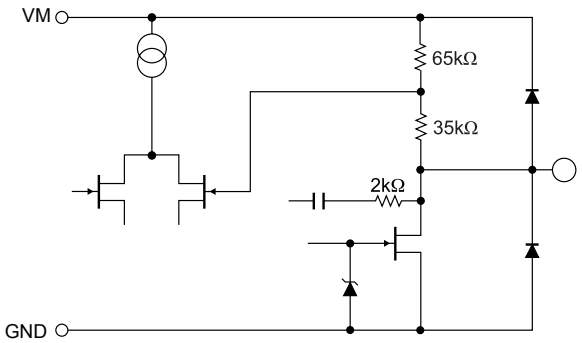
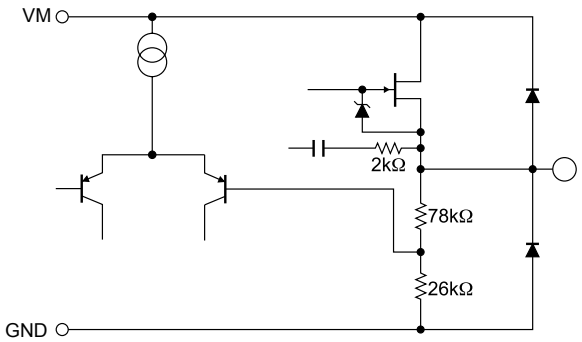
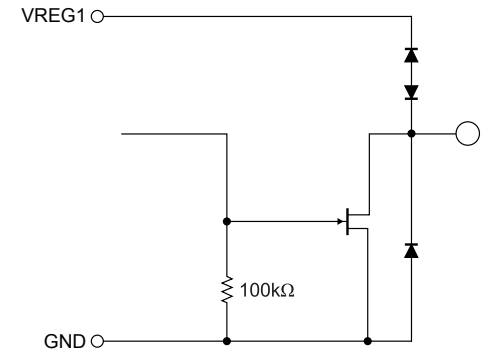
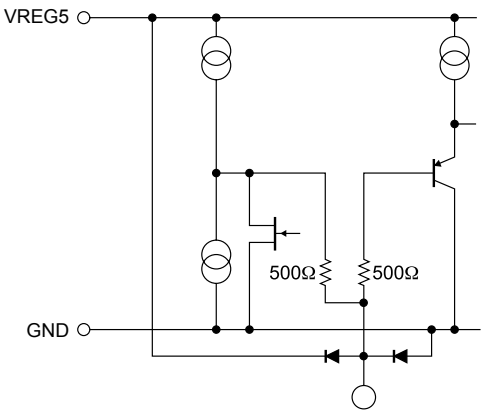
Pin No.	Pin Name	Pin Functtion	Equivalent Circuit
3	VREG2	Internal regulator capacitor connection pin.	
5	VREG1	Internal regulator capacitor connection pin.	
18 19 20	EMO DOWN MO	Over-current detection alarm output pin. Holding current output pin. Position detecting monitor pin.	
15 16	OSC1 OSC2	Copping frequency setting capacitor connection pin. Holding current detection time setting capacitor connection pin.	

Reference describing operation

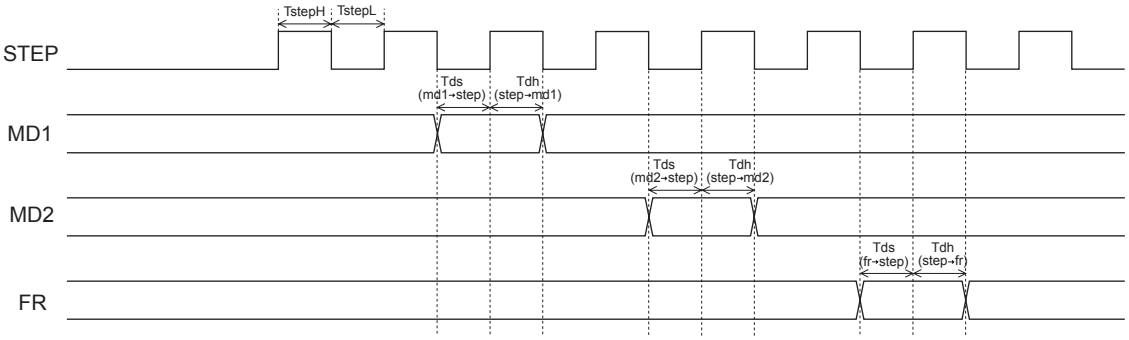
(1) Stand-by function

When ST pin is at low levels, the IC enters stand-by mode, all logic is reset and output is turned OFF.
When ST pin is at high levels, the stand-by mode is released.

(2) STEP pin function

Input		Operating mode
ST	STP	
Low	*	Standby mode
High		Excitation step proceeds
High		Excitation step is kept

(3) Input Timing



TstepH/TstepL : Clock H/L pulse width (min 500ns)
Tds : Data set-up time (min 500ns)
Tdh : Data hold time (min 500ns)

(4) Excitation setting method

Set the excitation setting as shown in the following table by setting MD1 pin, MD2 pin and MD3 pin.

Input			Mode	Initial position	
MD3	MD2	MD1	(Excitation)	1ch current	2ch current
Low	Low	Low	2 phase	100%	-100%
Low	Low	High	1-2 phase	100%	0%
Low	High	Low	W1-2 phase	100%	0%
Low	High	High	2W1-2 phase	100%	0%
High	Low	Low	4W1-2 phase	100%	0%
High	Low	High	8W1-2 phase	100%	0%
High	High	Low	16W1-2 phase	100%	0%
High	High	High	32W1-2 phase	100%	0%

The initial position is also the default state at start-up and excitation position at counter-reset in each excitation mode.

(5) Output current setting

Output current is set shown below by the VREF pin (applied voltage) and a resistance value between RF1(2) pin and GND.

I_{OUT} = (VREF / 5) / RF1 (2) resistance

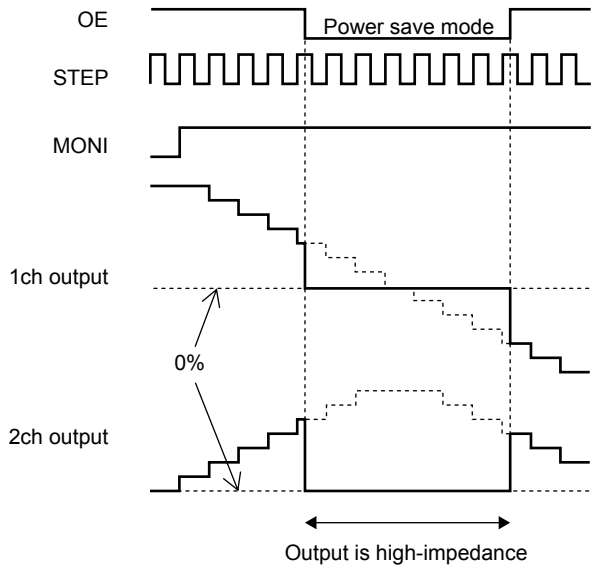
* The setting value above is a 100% output current in each excitation mode.

(Example) When VREF = 1.1V and RF1 (2) resistance is 0.22Ω, the setting is shown below.

I_{OUT} = (1.1V / 5) / 0.22Ω = 1.0A

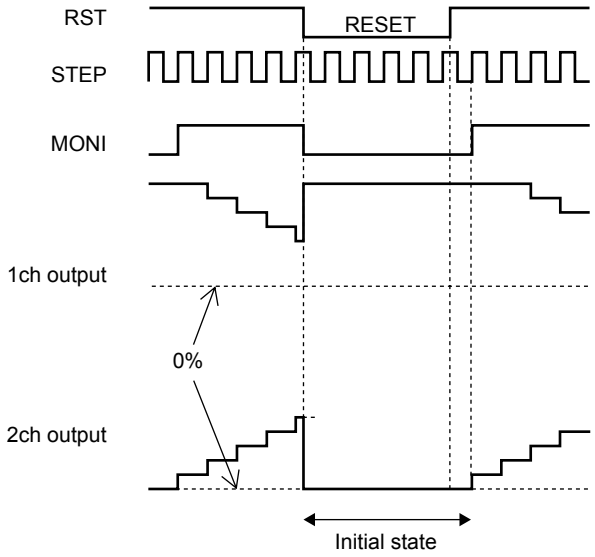
(6) Output enable function

When the OE pin is set Low, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the STP is input. Therefore, when OE pin is returned to High, the output level conforms to the excitation position proceeded by the STP input.



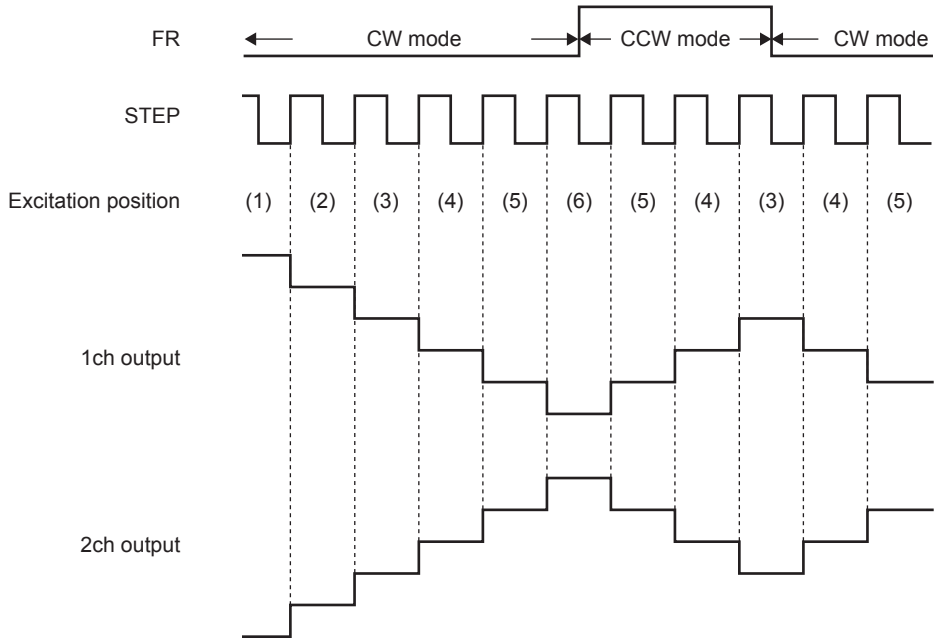
(7) Reset function

When the RST pin is set Low, the output goes to initial mode and excitation position is fixed in the initial position for STP pin and FR pin input. MO pin outputs at low levels at the initial position. (Open drain connection)



(8) Forward / reverse switching function

FR	Operating mode
Low	Clockwise (CW)
High	Counter-clockwise (CCW)



The internal D/A converter proceeds by a bit on the rising edge of the step signal input to the STP pin. In addition, CW and CCW mode are switched by FR pin setting.
In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.
In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(9) EMO, DOWN, MO output pin

The output pin is open -drain connection. When it becomes prescribed, it turns on, and each pin outputs the Low level.

Pin state	EMO	DOWN	MO
Low	At detection of over-current	Holding current state	Initial position
OFF	Normal state	Normal state	Non initial position

(10) Chopping frequency setting function

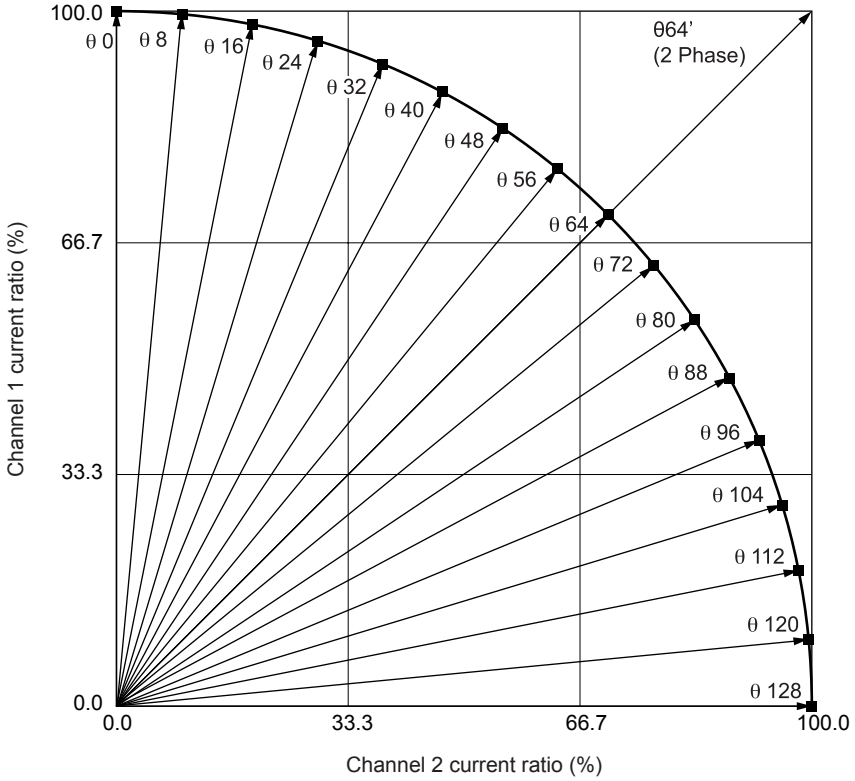
Chopping frequency is set as shown below by a capacitor between OSC1 pin and GND.

$$Fcp = 1 / (Cosc1 / 10 \times 10^{-6}) (Hz)$$

(Example) When Cosc1 = 200pF, the chopping frequency is shown below.

$$Fcp = 1 / (200 \times 10^{-12} / 10 \times 10^{-6}) = 50(kHz)$$

(11) Output current vector locus (one step is normalized to 90 degrees)



Current setting ratio in each excitation mode

STEP	32W1-2 phase(%)		16W1-2 phase(%)		8W1-2 phase(%)		4W1-2 phase(%)		2W1-2 phase (%)		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ0	100	0	100	0	100	0	100	0	100	0	100	0	100	0		
θ1	100	1														
θ2	100	2	100	2												
θ3	100	4														
θ4	100	5	100	5	100	5										
θ5	100	6														
θ6	100	7	100	7												
θ7	100	9														
θ8	100	10	100	10	100	10	100	10								
θ9	99	11														
θ10	99	12	99	12												
θ11	99	13														
θ12	99	15	99	15	99	15										
θ13	99	16														
θ14	99	17	99	17												
θ15	98	18														
θ16	98	20	98	20	98	20	98	20	98	20						
θ17	98	21														
θ18	98	22	98	22												
θ19	97	23														
θ20	97	24	97	24	97	24										
θ21	97	25														
θ22	96	27	96	27												
θ23	96	28														
θ24	96	29	96	29	96	29	96	29								
θ25	95	30														

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STEP	32W1-2 phase		16W1-2 phase		8W1-2 phase		4W1-2 phase		2W1-2 phase		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
026	95	31	95	31												
027	95	33														
028	94	34	94	34	94	34										
029	94	35														
030	93	36	93	36												
031	93	37														
032	92	38	92	38	92	38	92	38	92	38	92	38				
033	92	39														
034	91	41	91	41												
035	91	42														
036	90	43	90	43	90	43										
037	90	44														
038	89	45	89	45												
039	89	46														
040	88	47	88	47	88	47	88	47								
041	88	48														
042	87	49	87	49												
043	86	50														
044	86	51	86	51	86	51										
045	85	52														
046	84	53	84	53												
047	84	55														
048	83	56	83	56	83	56	83	56	83	56						
049	82	57														
050	82	58	82	58												
051	81	59														
052	80	60	80	60	80	60										
053	80	61														
054	79	62	79	62												
055	78	62														
056	77	63	77	63	77	63	77	63								
057	77	64														
058	76	65	76	65												
059	75	66														
060	74	67	74	67	74	67										
061	73	68														
062	72	69	72	69												
063	72	70														
064	71	71	71	71	71	71	71	71	71	71	71	71	71	71	100	100
065	70	72														
066	69	72	69	72												
067	68	73														
068	67	74	67	74	67	74										
069	66	75														
070	65	76	65	76												
071	64	77														
072	63	77	63	77	63	77	63	77								
073	62	78														
074	62	79	62	79												
075	61	80														
076	60	80	60	80	60	80										
077	59	81														
078	58	82	58	82												
079	57	82														
080	56	83	56	83	56	83	56	83	56	83						
081	55	84														
082	53	84	53	84												
083	52	85														
084	51	86	51	86	51	86										
085	50	86														
086	49	87	49	87												
087	48	88														
088	47	88	47	88	47	88	47	88								
089	46	89														
090	45	89	45	89												

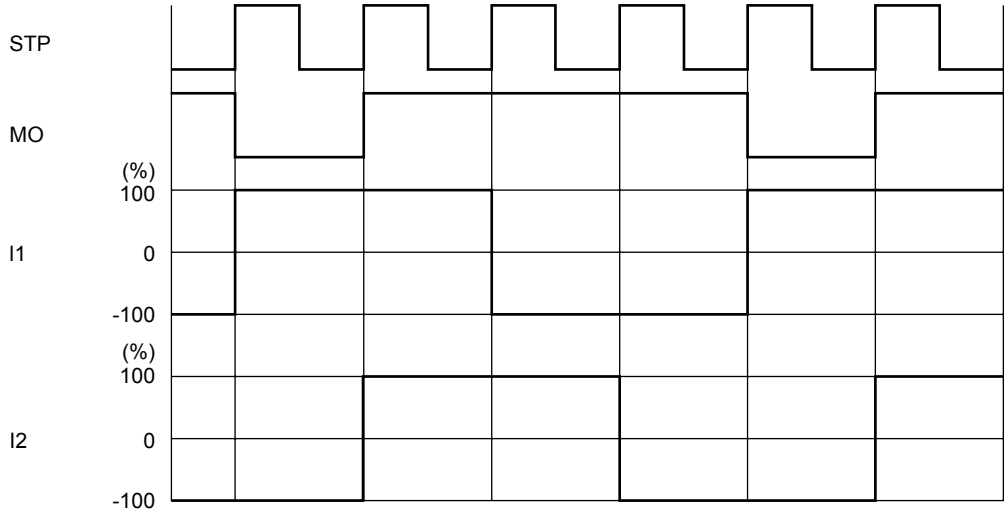
Continued on next page.

Continued from preceding page.

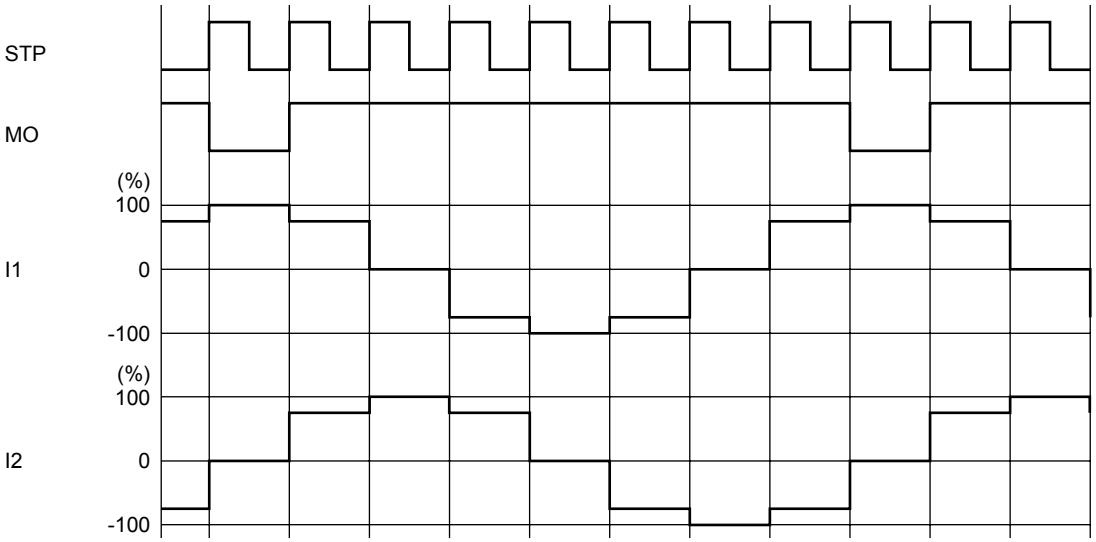
STEP	32W1-2 phase		16W1-2 phase		8W1-2 phase		4W1-2 phase		2W1-2 phase		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ91	44	90														
θ92	43	90	43	90	43	90										
θ93	42	91														
θ94	41	91	41	91												
θ95	39	92														
θ96	38	92	38	92	38	92	38	92	38	92	38	92				
θ97	37	93														
θ98	36	93	36	93												
θ99	35	94														
θ100	34	94	34	94	34	94										
θ101	33	95														
θ102	31	95	31	95												
θ103	30	95														
θ104	29	96	29	96	29	96	29	96								
θ105	28	96														
θ106	27	96	27	96												
θ107	25	97														
θ108	24	97	24	97	24	97										
θ109	23	97														
θ110	22	98	22	98												
θ111	21	98														
θ112	20	98	20	98	20	98	20	98	20	98						
θ113	18	98														
θ114	17	99	17	99												
θ115	16	99														
θ116	15	99	15	99	15	99										
θ117	13	99														
θ118	12	99	12	99												
θ119	11	99														
θ120	10	100	10	100	10	100	10	100								
θ121	9	100														
θ122	7	100	7	100												
θ123	6	100														
θ124	5	100	5	100	5	100										
θ125	4	100														
θ126	2	100	2	100												
θ127	1	100														
θ128	0	100	0	100	0	100	0	100	0	100	0	100	0	100		

(12) Current wave example in each excitation mode (2 phase, 1-2 phase, 4W1-2 phase, 32W1-2 phase)

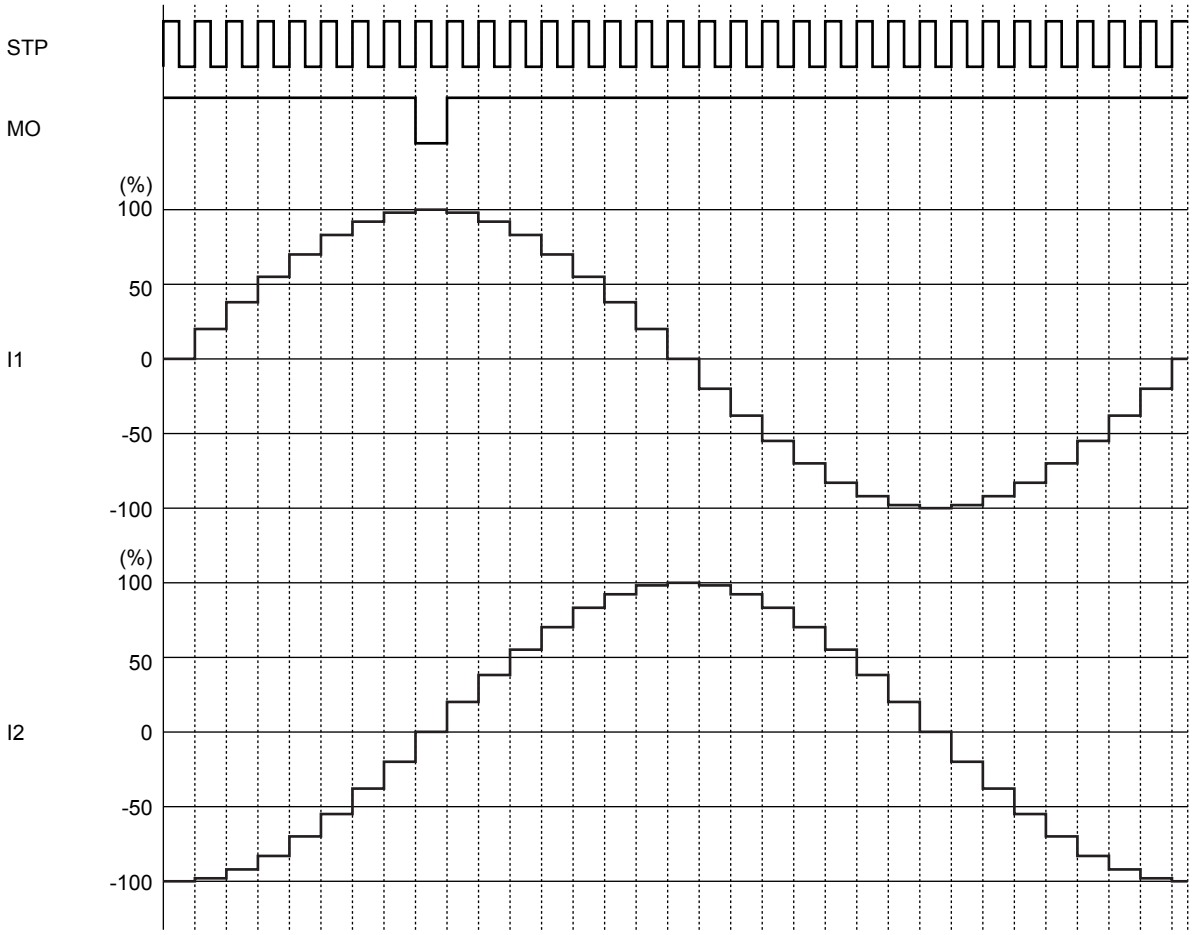
2-phase excitation (CW mode)



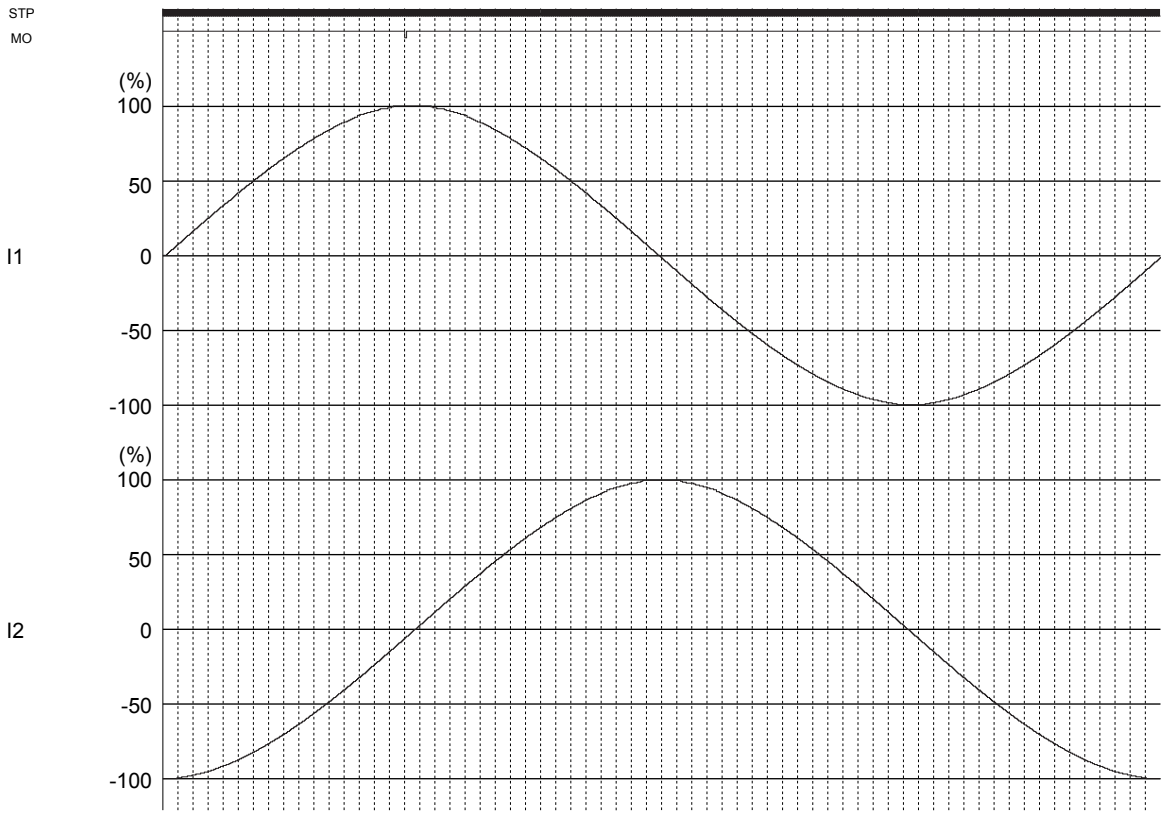
1-2 phase excitation (CW mode)



4W1-2 phase excitation (CW mode)

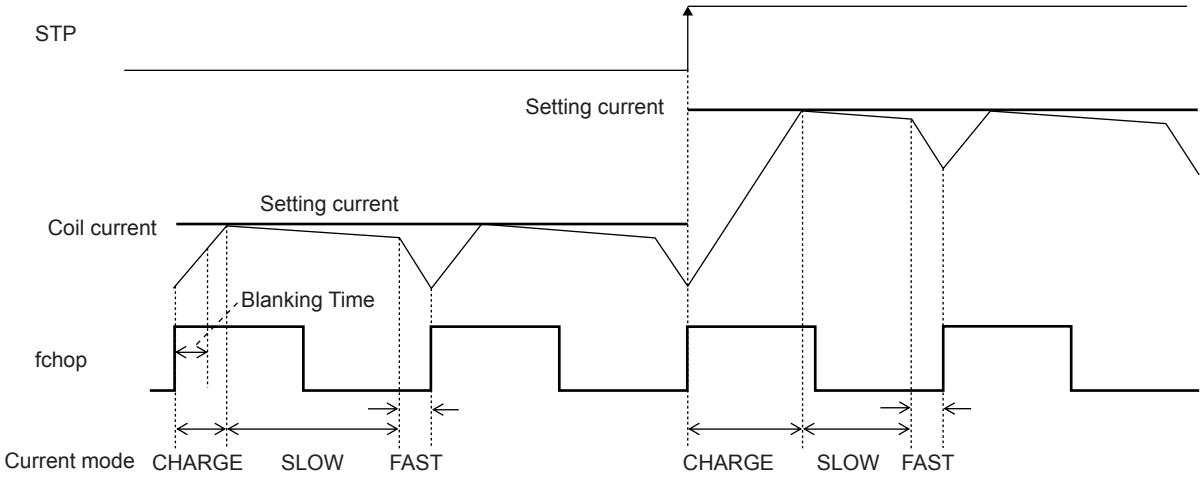


32W1-2 phase excitation (CW mode)

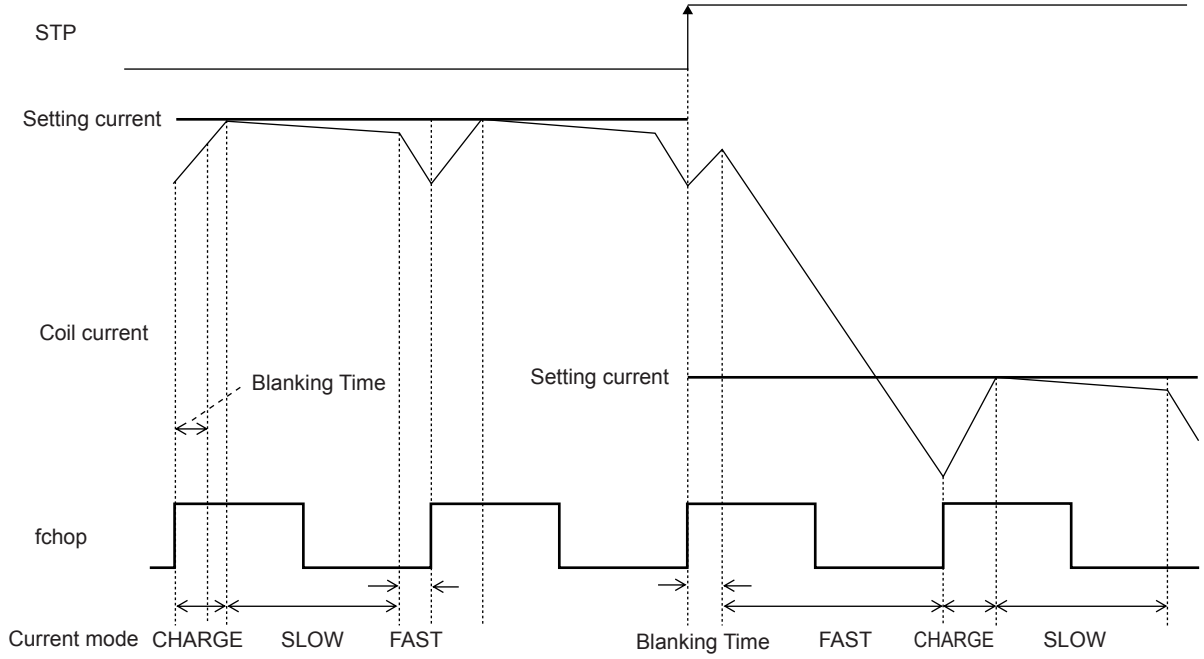


(13) Current control operation

(Sine-wave increasing direction)



(Sine-wave decreasing direction)



Each of current modes operates with the follow sequence.

· The IC enters CHARGE mode at a rising edge of the chopping oscillation. (A period of CHARGE mode (Blanking Time) is forcibly present in approximately 1μs, regardless of the current value of the coil current (ICOIL) and set current (IREF)).

· In a period of Blanking Time, the coil current (ICOIL) and the setting current (IREF) are compared.

If an ICOIL < IREF state exists during the charge period:

The IC operates in CHARGE mode until ICOIL ≥ IREF. After that, it switches to SLOW DECAY mode and then switches to FAST DECAY mode in the last approximately 1μs of the period.

If no ICOIL < IREF state exists during the charge period:

The IC switches to FAST DECAY mode and the coil current is attenuated with the FAST DECAY operation until the end of a chopping period.

The above operation is repeated. Normally, in the sine wave increasing direction the IC operates in SLOW (+ FAST) DECAY mode, and in the sine wave decresing direction the IC operates in FAST DECAY mode until the current is attenuated and reaches the set value and the IC operates in SLOW (+ FAST) DECAY mode.

(14) Output short-circuit protection circuit

Built-in output short-circuit protection circuit makes output to enter in stand-by mode. This function prevents the IC from damaging when the output shorts circuit by a voltage short or a ground short, etc. When output short state is detected, short-circuit detection circuit state the operating and output is once turned OFF. Subsequently, the output is turned ON again after the timer latch period (typ. 256μs). If the output remains in the short-circuit state, turn OFF the output, fix the output to the wait mode, and turn ON the EMO output.

When output is fixed in stand-by mode by output short protection circuit, output is released the latch by setting ST = "L".

(15) Open-drain pin for switching holding current

The output pin is an open-drain connection.

This pin is turned ON when no rising edge of STP between the input signals while a period determined by a capacitor between OSC2 and GND, and outputs at low levels.

The open-drain output in once turned ON, is turned OFF at the next rising edge of STP.

Holding current switching time (Tdown) is set as shown below by a capacitor between OSC2 pin and GND.

$$Tdown = Cosc2 \times 0.4 \times 10^{9} \ (s)$$

(Example) When Cosc2 = 1500pF, the holding current switching time is shown below.

$$Tdown = 1500pF \times 0.4 \times 109 = 0.6 \ (s)$$

(16) Thermal shutdown function

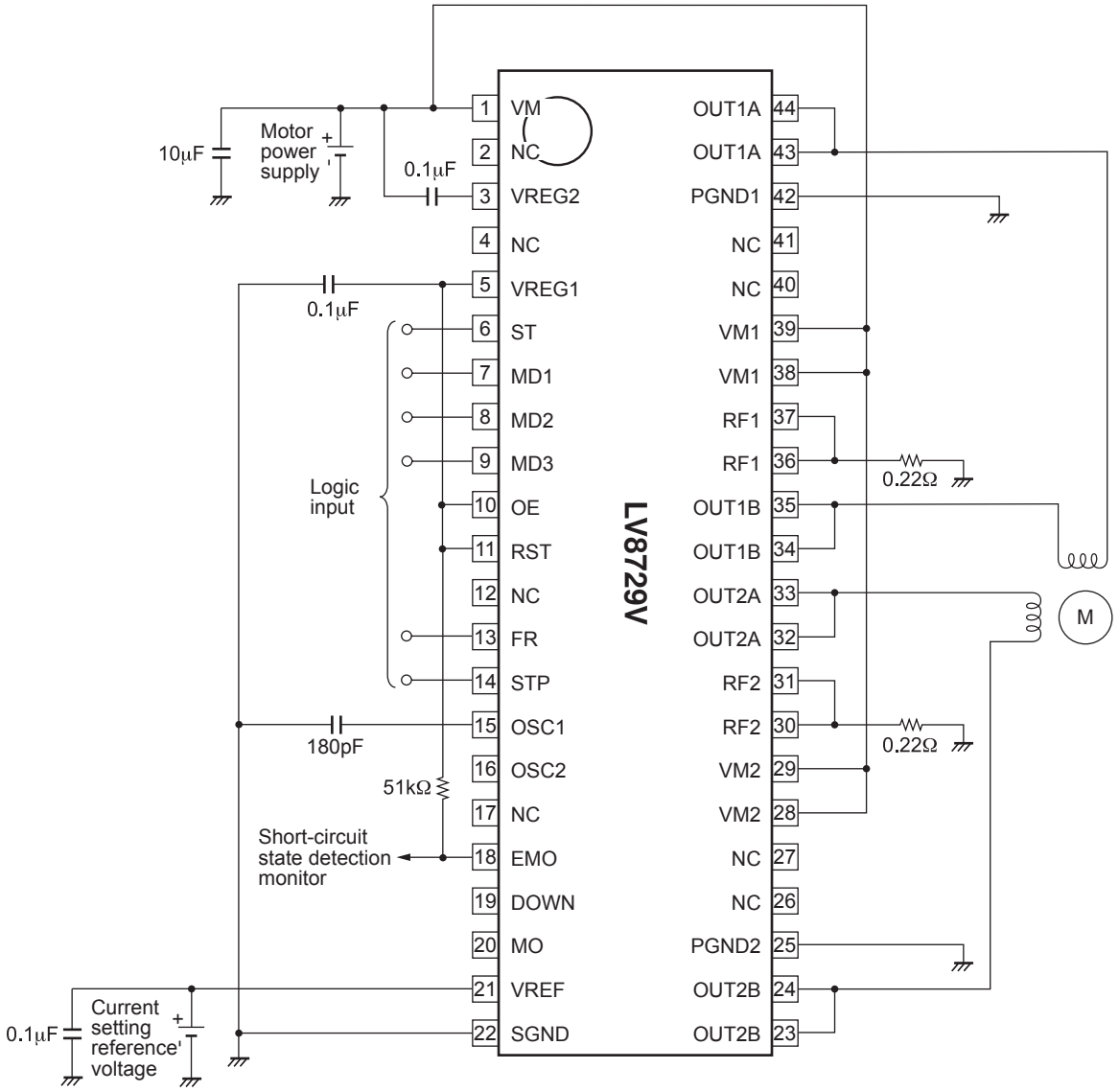
The thermal shutdown circuit is incorporated and the output is turned off when junction temperature Tj exceeds 180°C and the abnormal state warning output is turned on. As the temperature falls by hysteresis, the output turned on again (automatic restoration).

The thermal shutdown circuit does not guarantee the protection of the final product because it operates when the temperature exceed the junction temperature of Tjmax=150°C.

TSD = 180°C (typ)

ΔTSD = 40°C (typ)

Application Circuit Example



The above sample application circuit is set to the following conditions:

- Output enable function fixed to the output state (OE = “H”)
- Reset function fixed to the output state (RST = “H”)
- Chopping frequency : 55.5kHz (Cosc1 = 180pF)

The set current value is as follows :

I_{OUT} = (Current setting reference voltage / 5) / 0.22Ω

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV8729V-TLM-H	SSOP44K (275mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel
LV8729V-MPB-H	SSOP44K (275mil) (Pb-Free / Halogen Free)	30 / Fan-Fold