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LV8907UW

Sensor-less Three-phase Brushless DC Motor Controller, with Gate Drivers, for Automotive

ON Semiconductor®

www.onsemi.com

Overview

The LV8907 is a high performance, AEC-Q100 qualified, sensor-less three-phase BLDC motor controller with integrated gate drivers for driving external N-MOSFETs. An on-chip two-stage charge pump provides required gate voltage for a wide range of low $R_{DS(ON)}$ type external N-MOSFETs. The device offers a rich set of system protection and diagnostic functions such as over-current, over-voltage, short-circuit, under-voltage, over-temperature and many more. It supports open-loop as well as closed-loop speed control with user configurable startup, speed setting and proportional/integral (PI) control coefficients, making it suitable for a wide range of motor and load combinations. With a built-in linear regulator for powering external circuits, a watchdog timer, and a LIN (Local Interconnect Network) transceiver, the LV8907 offers a very small system solution.

The LV8907 stores system parameters in embedded one-time programmable (OTP) non-volatile memory in addition to RAM system memory. An SPI interface is provided for parameter setting and monitoring the system status. With the operating junction temperature tolerance up to 175ºC and electrically LIN compatible control signals (PWM and Enable), the LV8907 is an ideal solution for stand-alone BLDC motor control systems.

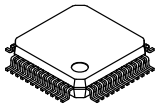
Features

- AEC-Q100 qualified and PPAP capable.
- Operating junction temperature up to 175ºC
- Operating voltage range from 5.5V to 20V with tolerance from 4.5V to 40V
- Embedded proprietary sensor-less trapezoidal and pseudo-sinusoidal commutation
- Supports open-loop as well as closed-loop speed control
- Integrated gate drivers for driving six N-MOSFETs
- Two-stage charge pump for continuous 100% duty cycle operation
- 5V/3.3V regulator, LIN transceiver and Watchdog timer applications using an external microcontroller.
- Configurable speed settings and PI control coefficients
- Various system protection features including:
  - Shoot through protection using configurable dead-time
  - Drain-source short detection
  - Cycle-by-cycle current limit and over-current shutdown
  - Over-voltage and under-voltage shutdown
  - Over-temperature warning and shutdown
  - Input PWM fault detection

Typical Applications

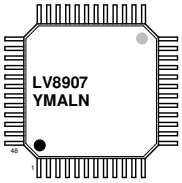
- Automotive pumps (Fuel, Oil, and Hydraulic)
- Fans (HVAC, Radiator, Battery Cooling, LED Headlight Cooling)
- White goods and industrial BLDC motor control

PACKAGE PICTURE



SQFP48K
7 mm x 7 mm

MARKING DIAGRAM



Y: production year
M: production month
A: assembly location
LN: lot number

ORDERING INFORMATION

Ordering Code:
LV8907UWR2G

Package
SQFP48K

Shipping (quantity/packing)
2500 per tape & reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

LV8907 BLOCK DIAGRAM

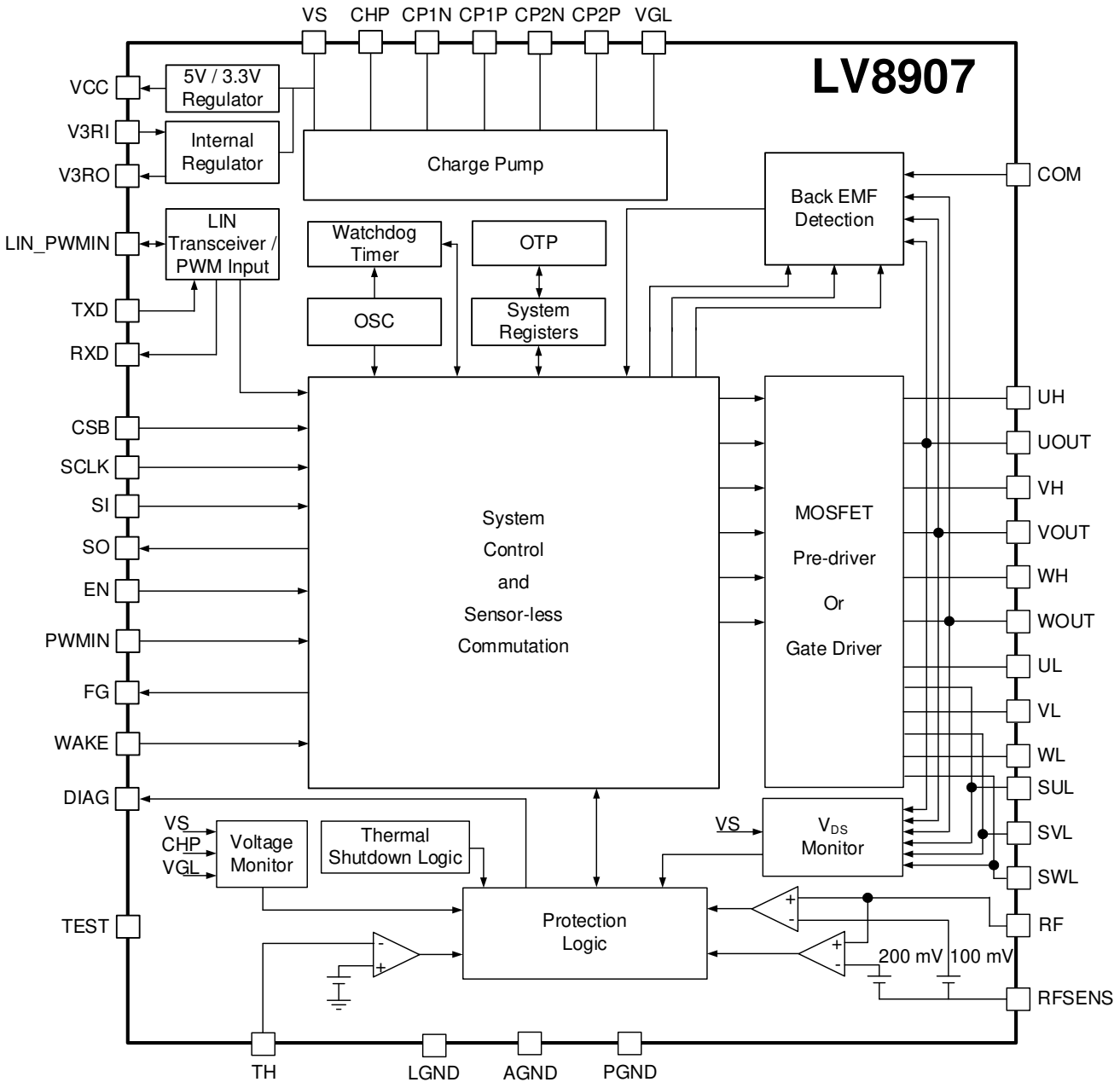


Figure 1: LV8907 Block Diagram

APPLICATION BLOCK DIAGRAMS

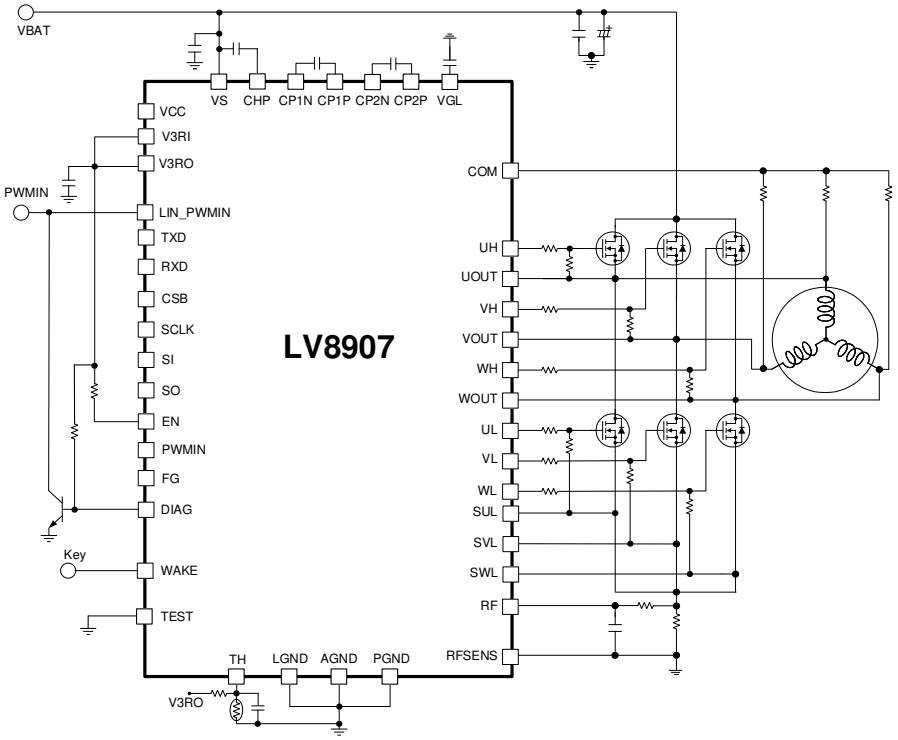


Figure 2: Example of Standalone Configuration

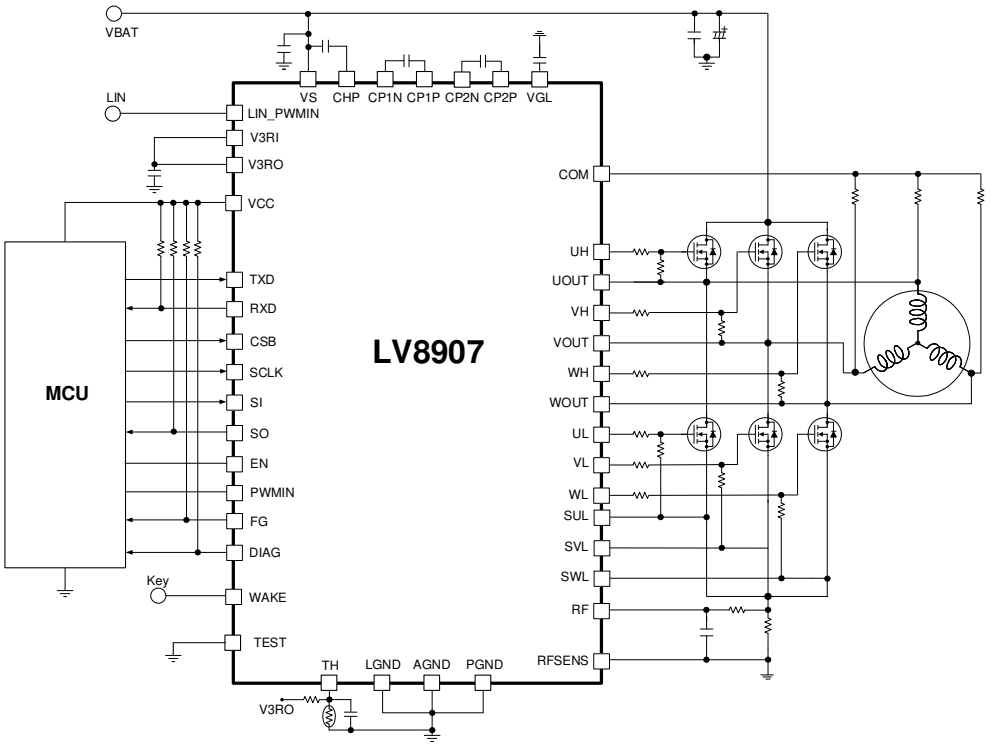


Figure 3: Example of LIN Based Control Configuration

PIN ASSIGNMENTS

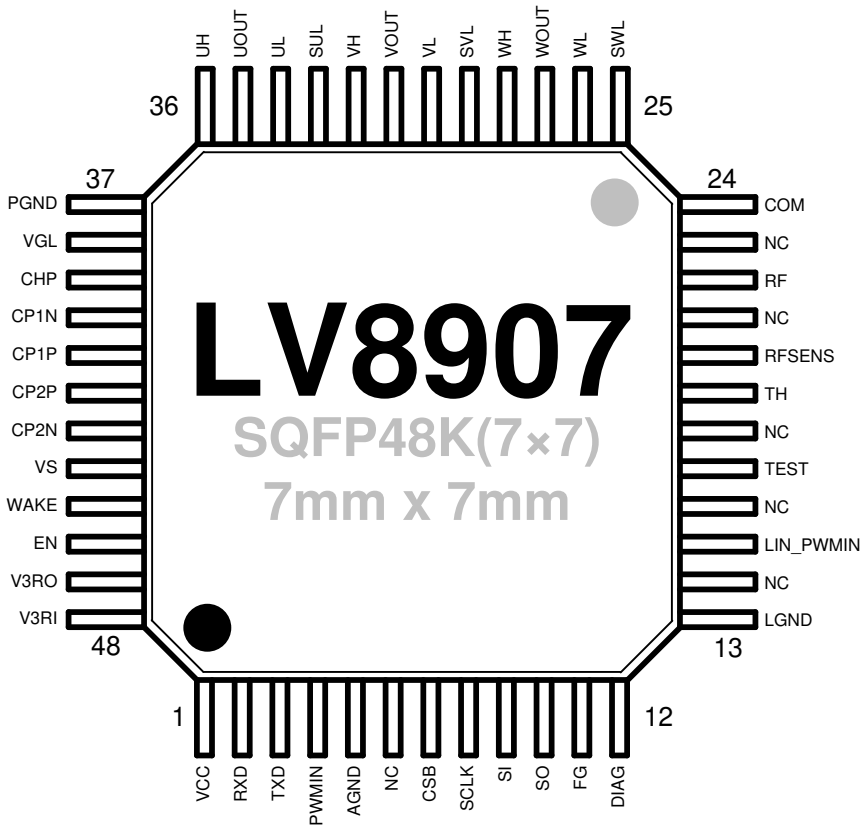


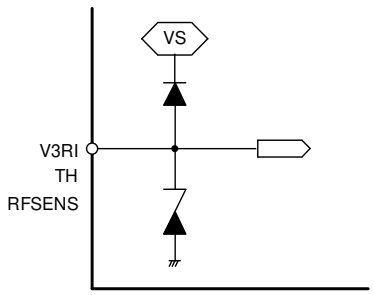
Figure 4: LV8907 Pinout

PIN DESCRIPTION

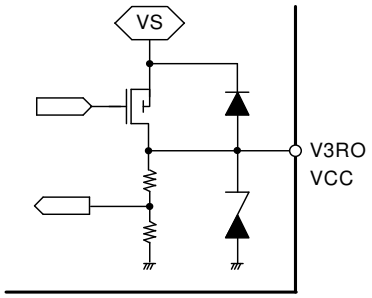
Pin Name	Pin No	Description	Page
VCC	1	5V or 3.3V regulator output pin. (Selected by internal register setting) Power supply for microcontroller. Connect capacitor to AGND for stability.	16
RXD	2	Open drain logic level output of LIN_PWMIN received data. Use pull-up to a voltage less than or equal to VS.	18
TXD	3	Logic level input of transmit data for LIN_PWMIN.	18
PWMIN	4	Digital level PWM input pin for direct drive or speed register selection details. Input polarity can be programmed for either active high or active low.	16
AGND	5	Analog GND pin.	
NC	6, 14, 16,18, 21, 23	No Connections	
CSB	7	Active low SPI interface chip selection pin.	20
SCLK	8	SPI interface clock input pin.	20
SI	9	Active high SPI interface serial data input pin.	20
SO	10	Open drain SPI interface serial data output pin.	20
FG	11	Open drain back-EMF transition output pin. The frequency division ratio is selectable via register settings.	18
DIAG	12	Programmable open drain diagnostic output.	18
LGND	13	LIN Block GND pin. Must be connected to AGND on the PCB.	
LIN_ PWMIN	15	LIN transceiver input/output. Register selectable as high voltage PWM input with a $V_{VS}/2$ threshold.	18
TEST	17	Factory test pin. Connect to GND.	
TH	19	Thermistor input pin for power stage temperature detection. If the input voltage is below the threshold voltage, an error is triggered. The error threshold is programmable. To disable tie to V3RO.	19
RFSENS	20	Shunt resistance reference pin. Connect this pin to the GND side of the Shunt resistor with Kelvin leads.	19
RF	22	Output current detect pin. Connect this pin to higher terminal of the shunt resistor with Kelvin leads.	19
COM	24	COM input pin. Connect this pin to the motor neutral point if available. This point may be derived from a resistive network with 1k resistors to the phases.	14
SUL SVL SWL	33 29 25	Current return path for low-side gate drive. Short circuit shutoff level is measured between this pin and its corresponding phase pin.	18
UL VL WL	34 30 26	Gate driver output pin for the low-side Nch Power FET. Use gate resistors for wave-shaping.	18
UOUT VOUT WOUT	35 31 27	Current return path for high-side gate drive and reference for high-side short circuit shut-off.	18
UH VH WH	36 32 28	Gate driver output pin for the high-side Nch Power FET. Use gate resistors for wave-shaping.	18
PGND	37	GND pin for the charge pump.	
VGL	38	Power supply pin for low-side gate drive. Connect decoupling capacitor between this pin and GND.	16
CHP	39	Power supply pin for high-side gate drive. Connect decoupling capacitor between this pin and VS.	16
CP1N	40	Charge transfer pin of the Charge pump (1N). Connect capacitor between CP1P and CP1N.	16
CP1P	41	Charge transfer pin of the Charge pump (1P). Connect capacitor between CP1P and CP1N.	16
CP2P	42	Charge transfer pin of the Charge pump (2P). Connect capacitor between CP2P and CP2N.	16
CP2N	43	Charge transfer pin of the Charge pump (2N). Connect capacitor between CP2P and CP2N.	16

Pin Name	Pin No	Description	Page
VS	44	Power supply pin.	15
WAKE	45	WAKE pin. “H” = Operating mode, “L” or “Open” = Sleep mode. In Sleep mode all gate drivers are high-impedance. To protect the power stage, pull-down resistors on the gate lines may be required.	15
EN	46	Motor stage Enable pin. “H” = Normal enabled mode; “L” or “Open” = Standby mode. In Standby mode all gate drivers driven low. Motor freewheeling.	15
V3RO	47	3V regulator output pin. Connect capacitor between this pin and AGND.	16
V3RI	48	3V regulator input pin (internally connected to ccontrol, and logic circuits). Connect to V3RO pin.	16

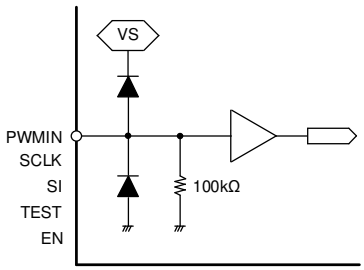
PIN CIRCUIT



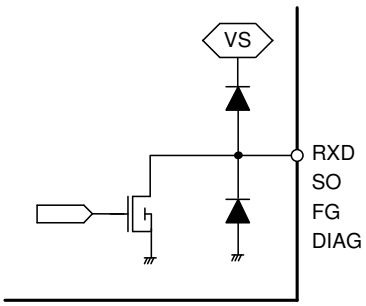
TYPE1: V3RI, TH, RFSENS



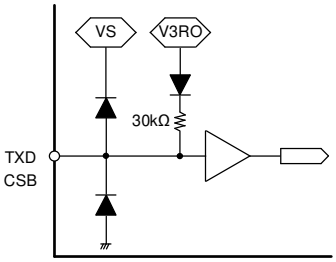
TYPE2: V3RO, VCC



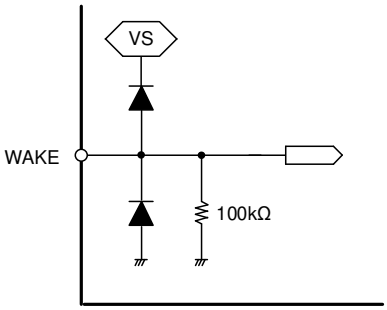
TYPE3: PWMIN, SCLK, SI, TEST, EN



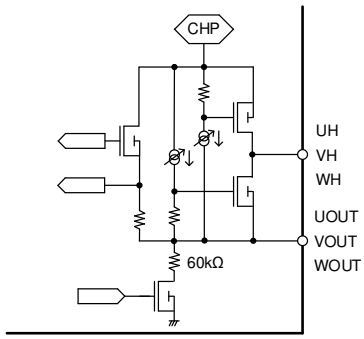
TYPE4: RXD, SO, FG, DIAG



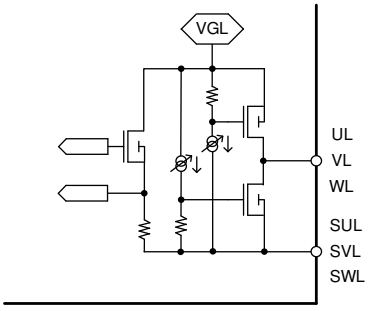
TYPE5: TXD, CSB



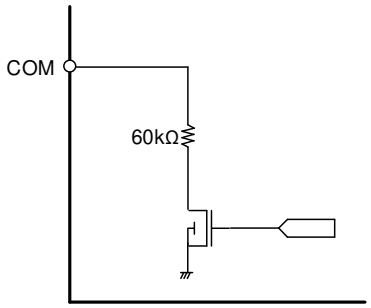
TYPE6: WAKE



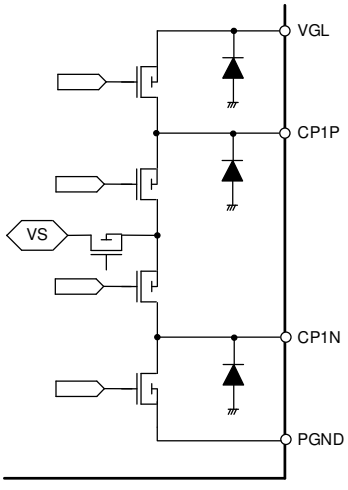
TYPE7: UH, VH, WH, UOUT, VOUT, WOUT



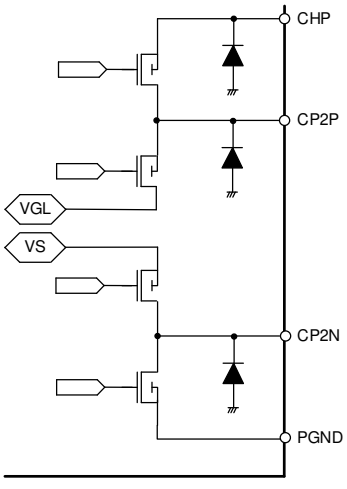
TYPE8: UL, VL, WL, SUL, SVL, SWL



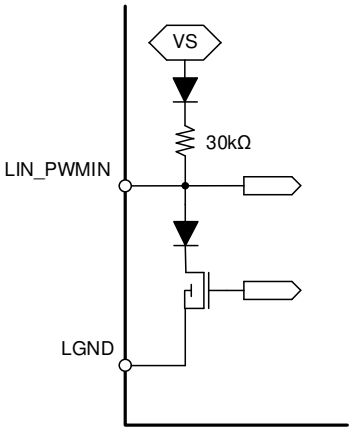
TYPE9: COM



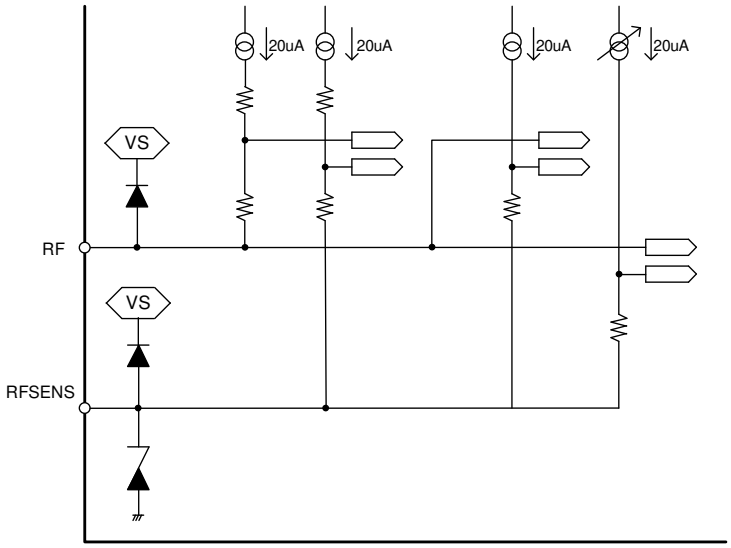
TYPE10: VGL, CP1P, CP1N, PGND



TYPE11: CHP, CP2P, CP2N, PGND



TYPE12: LIN_PWMIN, LGND



TYPE13: RF, RFSENS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Parameter	Pins	Ratings	Unit
Supply voltage	VS	−0.3 to 40	V
Charge pump voltage (high side)	CHP	−0.3 to 40	V
Charge pump voltage (low side)	VGL	−0.3 to 16	V
Logic power supply	VR3I, VR3O	−0.3 to 3.6	V
5V Regulator voltage	VCC	−0.3 to 5.5	V
Digital I/O voltage1	WAKE,EN	−0.3 to 40	V
Digital I/O voltage2	CSB, SCLK, SI, PWMIN, TXD, TEST	−0.3 to 5.5	V
Digital output voltage	DIAG, FG, SO, RXD	−0.3 to 40	V
LIN bus voltage	LIN_PWMIN Voltage differential between Pins are 60V or less	−40 to 40	V
RF input voltage	RF	−3 to 3.6	V
RFSENS input voltage	RFSENS	−0.3 to 1.0	V
TH input voltage	TH	−0.3 to 3.6	V
Voltage Tolerance	UOUT, VOUT, WOUT, COM	−3 to 40	V
High-side output	UH, VH, WH	−3 to 40	V
Low-side output	UL, VL, WL	−3 to 16	V
Low-side Source output voltage	SUL, SVL, SWL	−3 to 3.6	V
Voltage between HS gate and phase	UH-UOUT,VH-VOUT,WH-WOUT	−0.3 to 40	V
Voltage between LS gate and source	UL-SUL, VL-SVL, WL-SWL	−0.3 to 16	V
Output current	UH,VH,WH,UL,VL,WL pulsed (duty5%)	50 400	mA
Open drain output current	DIAG, FG, SO, RXD	10	mA
Thermal Resistance ($R_{\theta jA}$)	with Board (Note 2)	47	°C/W
ESD Human Body Model	AEC Q100-002	2	kV
ESD Charged Device Model	AEC Q100-011	750	V
Storage temperature		−55 to 150	°C
Junction temperature		−40 to 150	°C
	(Note 3)	150 to 175	°C

Note 1: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note 2: 76.2 × 114.3 × 1.6mm, glass epoxy board

Note 3: Operation outside the Operating Junction temperature is not guaranteed. Operation above 150°C should not be considered without a written agreement from ON Semiconductor Engineering staff.

ELECTRICAL CHARACTERISTICS

Valid at a junction temperature range from −40°C to 150°C, for supply Voltage 6.0V≤VS≤20V.
Typical values at 25°C and VS=12V unless specified otherwise. (Note 4)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply-voltage range	VS		6	12	20	V
		Device fully functional.	5.5		20	V
		Full logic functionality, driver stage off.	4.5		40	V
Supply current into VS	I_{S1}	V3RO=V3RI		15	25	mA
	I_{S2}	Sleep Mode		40	80	μA
Operational junction Temperature	Topj		−40		150	°C
OUTPUT BLOCK (UH, VH, WH, UL, VL, WL)						
Low-side output On-resistance 1	RON(L1)	"L" level Io=10mA		6	15	Ω
Low-side output On-resistance 2	RON(L2)	"H" level Io=-10mA		12	22	Ω
High-side output On-resistance 1	RON(H1)	"L" level Io=10mA		6	15	Ω
High-side output On-resistance 2	RON(H2)	"H" level Io=-10mA		12	22	Ω
DRIVE OUTPUT BLOCK (PWM BLOCK)						
Drive output PWM frequency	fPWMO	PWMF=0 Low frequency mode	18.5	19.5	20.5	kHz
Output PWM Duty cycle resolution	ΔPWMDUTY	PWMF=0 Low frequency mode (Note 5)			0.2	%
3V CONSTANT VOLTAGE OUTPUT						
Output voltage	V3RO		3.135	3.3	3.465	V
Voltage regulation	ΔV3R1	VS=6.0 to 20V			50	mV
Load regulation	ΔV3REG2	Io=5mA to 25mA			50	mV
Current Limit	IV3RO	Not for external loads > 5mA	50			mA
VCC 5V CONSTANT VOLTAGE OUTPUT						
Output voltage	VC5RO	VS=6.0 to 20V	4.75	5.00	5.25	V
Voltage regulation	ΔVC5R1	VS=6.0 to 20V			50	mV
Load regulation	ΔVC5R2	Io=5mA to 25mA			50	mV
Current Limit	IVCC5V		50			mA
VCC 3V CONSTANT VOLTAGE OUTPUT						
Output voltage	VC3RO		3.135	3.3	3.465	V
Voltage regulation	ΔVC3R1	VS=6.0 to 20V			50	mV
Load regulation	ΔVC3R2	Io=5mA to 25mA			50	mV
Current Limit	IVCC3V3		50			mA
LOW-SIDE GATE VOLTAGE OUTPUT (VGL Pin)						
Low-side output voltage1	VGLH1	6.0 < VS ≤ 8.0V Io=−10mA	8.0	12.0	14.0	V
Low-side output voltage2	VGLH2	8.0 < VS ≤ 20V Io=−10mA	10.0	12.0	14.0	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
HIGH-SIDE OUTPUT VOLTAGE (CHP Pin)						
Internal charge pump oscillator frequency	FCP	SSCG=0	49.6	52.1	54.6	kHz
Boost voltage1	VGHH1	6.0 < VS ≤ 8.0V Io=−10mA	VS +6.0	VS +12.0	VS +14.0	V
Boost voltage2	VGHH2	8.0 < VS ≤ 20V Io=−10mA	VS +9.0	VS +12.0	VS +14.0	V
PWMIN INPUT PIN in low frequency mode						
Input PWM frequency range	fLPWM		5.3		1000	Hz
PWM signal timeout	TLPWMIN			210	220	ms
PWMIN INPUT PIN in High frequency mode						
Input PWM frequency range	fHPWM		0		18.5	kHz
DIGITAL INPUT PIN (CSB, TXD)						
High-level input voltage	VIH1		0.8×V3RO			V
Low-level input voltage	VIL1				0.2×V3RO	V
Input hysteresis voltage	VIHYS1		0.1	0.35	0.6×V3RO	V
Pull-up resistance.	RDVI1		15	30	60	KΩ
DIGITAL INPUT PIN (SCLK, SI, PWMIN, TEST)						
High-level input voltage	VIH2		0.8×V3RO			V
Low-level input voltage	VIL2				0.2×V3RO	V
Input hysteresis voltage	VIHYS2		0.1	0.35	0.6×V3RO	V
Pull-down resistance	RDVI2		50	100	200	KΩ
WAKE INPUT PIN						
High-level input voltage	VIH3		2.5			V
Low-level input voltage	VIL3				0.6	V
Internal Pull-down resistance	RDVI3		50	100	200	KΩ
EN INPUT PIN						
High-level input voltage	VIH4		0.8×V3RO			V
Low-level input voltage	VIL4				0.2×V3RO	V
Input hysteresis voltage	VIHYS4		0.1	0.35	0.6×V3RO	V
Pull-down resistance	RDVI4		50	100	200	KΩ
DIGITAL OUTPUT PIN (SO, FG, DIAG, RXD)						
Output voltage	VOL	Io=1mA pull-up current			0.2	V
Output leakage current	ILOLK				10	μA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CURRENT LIMIT / OVER-CURRENT PROTECTION (RF, RFSENS)						
Current limit voltage	VRF1	Voltage between RF and RFSENS	90	100	110	mV
Over-current detection Voltage threshold	VRF2	Voltage between RF and RFSENS	180	200	220	mV
EXTERNAL THERMAL PROTECTION (TH)						
Threshold Voltage Falling	VTH0 VTH1 VTH2 VTH3	THTH[1:0]=00 THTH[1:0]=01 THTH[1:0]=10 THTH[1:0]=11	−10%	0.35 0.30 0.25 0.20	+10%	V
Hysteresis range	VTHHYS		0.025	0.05	0.075	V
THERMAL PROTECTION						
Thermal warning temperature	TTW0 TTW1	(Junction temperature) (Note5) TSTS=0 TSTS=1	 125 150			°C
Thermal warning temperature hysteresis	TTWHYS	(Junction temperature) (Note5)		25		°C
Thermal shutdown temperature	TTSD0 TTSD1	(Junction temperature) (Note5) TSTS=0 TSTS=1	 150 175			°C
Thermal shutdown temperature hysteresis	TTSDHYS	(Junction temperature) (Note5)		25		°C
VOLTAGE MONITORING (VS, CHP, VGL, VCC)						
VS under-voltage detection	VSLV		4.8		5.1	V
VS under-voltage detection hysteresis	VSLVHYS		0.1	0.25	0.4	V
VS Over-voltage detection	VSHV		20		24	V
Over-voltage detection hysteresis	VSHVHYS		0.5	1.0	1.5	V
CHP under-voltage detection	CHPLV		VS+4.5		VS+5.5	V
CHP under-voltage detection hysteresis	CHPLVHYS		0.2	0.4	0.7	V
VGL under-voltage detection	VGLLV		4.5		5.5	V
VGL under-voltage detection hysteresis	VGLLVHYS		0.2	0.4	0.7	V
VCC3.3 under-voltage detection	VCLV3	REGSEL=0, VCCEN = 1, VCLVPO=0	2.3		2.7	V
VCC3.3 under-voltage detection hysteresis	VCLVHYS3	REGSEL=0, VCLVPO=0	0.1	0.25	0.4	V
VCC5.0 under-voltage detection	VCLV5	REGSEL=1, VCCEN = 1, VCLVPO=0	3.8		4.2	V
VCC5.0 under-voltage detection hysteresis	VCLVHYS5	REGSEL=1, VCLVPO=0	0.1	0.25	0.4	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LIN_PWMIN PIN (LIN TRANSMITTER)						
LIN output current bus in dominant state	Ibus_pas_dom	Driver OFF Vbus=0V,VS=7V & 18V	−1			mA
LIN output current bus in recessive state	Ibus_pas_rec	Driver OFF Vbus=VS,VS=7V & 18V			20	uA
Short circuit current limitation	Ibus_lim	Driver ON Vbus=VS, VS=7V & 18V	40		200	mA
Internal Pull-up resistance	Rslave	VS=7V & 18V	20	30	47	kΩ
LIN_PWMIN PIN (LIN RECEIVER & PWMIN)						
High-level input voltage	Vbusdom	VS=7V & 18V	0.6×VS		VS	V
Low-level input voltage	Vbusrec	VS=7V & 18V	0		0.4×VS	V
Input hysteresis voltage	Vbushys	VS=7V & 18V	0.05×VS		0.2×VS	V
AC characteristics LIN_PWMIN PIN						
Duty cycle 1	D1	THrecmax=0.744VS THdommax=0.581VS VS=7.0V…18V, tbit=50μs D1=tBusrecmin/(2*tbit)	0.396		0.5	
Duty cycle 2	D2	THrecmin=0.422VS THdommin=0.284VS VS=7.6V…18V, tbit=50μs D1=tBusrecmax/(2*tbit)	0.5		0.581	
Duty cycle 3	D3	THrecmax=0.778VS THdommax=0.616VS VS=7.0V…18V, tbit=96μs D1=tBusrecmin/(2*tbit)	0.417		0.5	
Duty cycle 4	D4	THrecmin=0.389VS THdommin=0.251VS VS=7.6V…18V, tbit=96μs D1=tBusrecmax/(2*tbit)	0.5		0.59	
Propagation delay bus recessive to RXD=high	Trx_pdr	VS=7V & 18V			6	μs
Propagation delay bus dominant to RXD=low	Trx_pdf	VS=7V & 18V			6	μs
Symmetry of receiver propagation delay	Trx_sym	trx_pdr-Trxpdf	−2		2	μs
Normal Slope rise time 12	T_rise_norm 12	VS=12V,LINSLP=0 L1,L2 (Note 6)			22.5	μs
Normal Slope fall time 12	T_fall_norm 12	VS=12V,LINSLP=0 L1,L2 (Note 6)			22.5	μs
symmetry of Normal Slope 12	T_sym_norm 12	VS=12V,LINSLP=0 L1,L2 (Note 6)	−4		4	μs
Normal Slope rise time 3	T_rise_norm 3	VS=12V,LINSLP=0,L3 (Note 6)			27	μs
Normal Slope fall time 3	T_fall_norm 3	VS=12V,LINSLP=0,L3 (Note 6)			27	μs
symmetry of Normal Slope 3	T_sym_norm 3	VS=12V,LINSLP=0,L3 (Note 6)	−5		5	μs
Low Slope rise time	T_rise_low	VS=12V,LINSLP=1,L3 (Note 6)			62	μs
Low Slope fall time	T_fall_low	VS=12V,LINSLP=1,L3 (Note 6)			62	μs

Note 4: Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Note 5: Not tested in production. Guaranteed by design.

Note 6: Load conditions Rbus/Cbus: L1=1kΩ/1nF, L2=660Ω/6.8nF, L3=500Ω/10nF Typical Operating Conditions

DETAILED FUNCTIONAL DESCRIPTON

The LV8907 integrates full sensor-less brushless DC motor commutation and Proportional/Integral (PI) speed control. A robust startup algorithm combined with OTP registers for important system parameters make this IC a solution of choice for many BLDC applications which need to turn a motor in one direction only such as pumps, fans, etc. No detailed BLDC commutation knowledge is necessary.

Building a BLDC application with the LV8907 is even simpler than building a DC motor. Only a PWM pulse train is necessary to control the motor – either directly or via speed control. Switch-only applications are also possible. Speed and error information can be fed back to the control unit via FG and DIAG outputs.

If more complex operation and flexibility are required the LV8907 can be combined with a small microcontroller. The LV8907 implements motor commutation and includes all necessary support circuitry for the microcontroller such as:

- 5V/3.3V Power supply.
- Integrated watchdog timer.
- LIN Transceiver.
- External Temperature Sensor.

In case of system errors such as a missing control signal, or a watchdog error, the LV8907 includes auto-run settings. If one of those errors occur and connection to the microcontroller is lost, the motor can continue running at a pre-defined fixed duty cycle of 25%, 50%, 75% or 100%.

Motor Commutation

Motor position is detected using the BEMF of the un-driven phase of a rotating three-phase motor relative to its neutral point connected to COM. Once an adequate BEMF level has been detected voltages applied via PWM to the other two phases of the motor maintain rotation. The digital equivalent of the BEMF signal appears at FG.

Two different PWM patterns can be selected via register MRCONF12 to match motors with trapezoidal or sinusoidal BEMF.

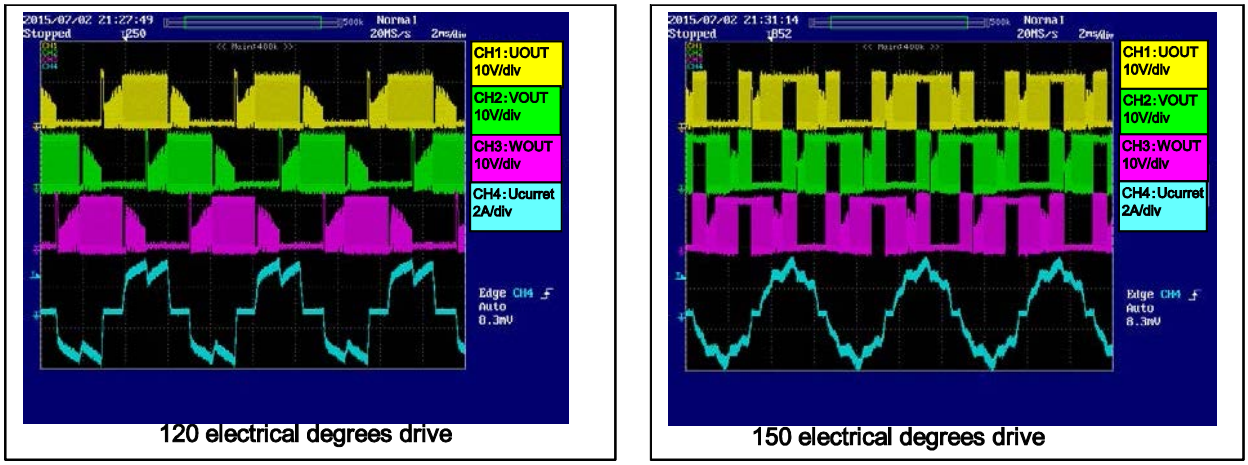


Figure 5: Trapezoidal vs. Sinusoidal Drive @ 50% Duty cycle
(CH1&3=Phase Voltage, CH2=Phase Current, CH4=Speed signal FG)

Figure 5 shows a comparison of a motor driven with normal trapezoidal commutation (left) vs. one driven with sinusoidal drive. With sinusoidal drive each phase is driven 150 electrical degrees with soft transitioning. This results in sinusoidal drive current with lower total harmonic distortion, reducing both torque ripple and noise. Trapezoidal drive results in a higher voltage across the motor phases and may be preferable for high torque and high speed operation.

Maximum Motor Speed

The maximum physical motor speed of the application is limited by the internal clock to approximately 48000 electrical RPM. If this is exceeded the LV8907 coasts the motor until BEMF detection and drive can resume.

Commutation Angle Adjustment

In trapezoidal commutation mode it is possible to advance the commutation angle by up to 28 electrical degrees as defined in register LASET. Early commutation adjusts the rotor magnetic field positioning and allows for higher motor speeds at the expense of efficiency. Advancing commutation can be done dynamically by a companion microcontroller.

Motor Startup

BEMF is used for rotor position sensing but for BEMF generation the motor has to be rotating. A stopped motor will initially be driven open-loop until BEMF can be detected.

Open-loop operation is motor parameter dependent. The most critical parameters depend on load and motor inertia. They are initial commutation frequency and PWM duty cycle (which affects motor flux density).

In the LV8907, the initial commutation frequency is programmed with register STOSC. Flux density is regulated by limiting startup current with a current ramp. During this ramp the current limit is increased in 16 steps from 0 to the maximum current defined by the external shunt. The ramp time from 105ms to 6.72s is

defined in register SSTT. Register SSTEN allows to disable the current ramp if necessary.
Fixed motor speed will be applied until either a valid BEMF has been detected in all three phases or the startup timer expires.

Motor Lock

This timer begins after the end of the current ramp and can be programmed from 420ms to 6.72s in register CPTM. If the timer expires a locked rotor error is flagged. In automatic retry mode, the LV8907 will restart after standby mode for time of eight times of CPTM.

Spin-up of Rotating Motors

The LV8907 can perform free-wheeling detection before applying the open loop spin-up algorithm described above. If the motor is already turning in the right direction the IC will continue with closed loop commutation. If the motor is turning in the wrong direction, the IC will wait for the motor to stop and then perform open-loop startup.

There are two scenarios where this behavior might not be desirable:

1. Fast Startup is required
   Free-wheeling detection takes up to one electrical revolution of the motor, which may be inacceptable for some applications. In this case free-wheeling detection can be disabled by setting FRREN. See section "Fast Startup" on page 18.
2. Wind-milling backwards
   Should the motor be driven by some external force as it is freewheeling in the wrong direction the LV8907 will potentially wait forever. Should start-up under these conditions be required, free-wheeling detection must be disabled as well.

Chip Activation, Shutdown and System States

After power up of VS and WAKE above 2.5V the LV8907 wakes up. Standby mode is entered after VS has exceeded 5.5V (min.).

A high level on WAKE > 2.5V (max.) activates the IC from sleep mode which enables the internal linear regulator at V3RO. Once the voltage on V3RO as sensed on V3RI has passed the power on reset (POR) threshold the system oscillator starts, and after 32 counts of the system clock (3.2µs typical) releases the internal digital reset which simultaneously starts the external regulator VCC and the charge-pump, and loads the system register contents from OTP into the internal registers. During the entire wake-up sequence of 8ms (typ.) DIAG is masked for charge-pump and VCC under-voltage. After wake-up is complete, the IC enters Standby mode and DIAG is activated to display internal errors. During Standby mode full SPI access is possible.
A high on EN takes the LV8907 from Standby to Normal mode. Normal mode allows motor control and SPI access is limited. A low on EN disables the motor stage regardless of the PWM input and returns the part back to Standby mode.
The IC is shut down by taking WAKE below 0.6V (min.). WAKE has priority over the state of EN, if EN hold functionality is desired; it needs to be implemented with an external diode from EN to WAKE.

System States

LV8907 has three operating modes. The operating modes are controlled by WAKE and EN.

Sleep mode
Sleep mode is a power saving mode. All circuits are powered down, charge pump is inactive and the SPI port is unusable. Activating WAKE allows the transition from the sleep mode to either Standby or Normal mode.

Standby mode
In Standby mode the OTP content has been transferred into the master-register. In this mode all outputs are turned off. Any internal writable register that is not locked can be configured by SPI interface.

Normal mode
In normal mode, outputs can be controlled and all blocks are active. All registers can be read through the SPI interface.

Mode	WAKE	EN	Internal bias	Logic	VCC	Charge pump	Drivers
Sleep	L	×	Disable	Reset	Disable	Disable	High-Z
Standby	H	L	Enable	Active	Enable	Enable	Low
Normal	H	H	Enable	Active	Enable	Enable	Enable

Supply Voltage Transients

The LV8907 is well suited to operate during typical automotive transients. It is fully functional during start-stop transients, as it maintains all specified parameters for supply voltages from 6V < VS < 20V. If the supply voltage falls below 5V, for example during cold-cranking, under-voltage error is flagged, but digital functionality is maintained until the internal regulator falls below its under-voltage lockout level of 2.2V. The VCC regulator must be configured for 3.3V if low transient operation is desired.

If over-voltage protection is enabled in MRCONF10 an over-voltage error is indicated if the supply rises beyond 20V(min). In both under- and over-voltage error modes, the power stage drivers UH, VH, WH and UL, VL, and

WL go low, turning the external power stage high-impedance and letting the motor freewheel. The LV8907 will re-engage the motor after conditions have returned to normal.

System Power Supplies

Three power supplies are integrated into the LV8907:

- An internal 3.3V regulator provides power to the digital and interface section.
- The VCC regulator can be configured to provide 5V or 3.3V to an external processor and other loads.
- A dual stage charge-pump allows 100% duty cycle operation and maintains full enhancement to the power stage at low input voltages.

Internal Regulator V3RO, V3RI

The internal regulator is supplied from VS, provides 3.3V at V3RO. V3RI is connected to the power supply inputs of the control and logic circuit blocks. V3RO and V3RI need to be connected externally and bypassed to the GND plane for stability. V3RO must not be used for external loads.

VCC Regulator

The VCC regulator may power external loads up to 50mA(max). VCC becomes active during Standby mode and can be configured via register VCCSEL to provide 5V or 3.3V. Under-voltage error is flagged if the output voltage drops below 4.2V in 5V operation, or 2.7V in 3.3V operation.

The VCC regulator can be enabled or disabled with register VCCEN.

Charge Pump Circuit for CHP and VGL

LV8907 has an integrated charge pump circuit for low-side and high-side pre-driver supply. Low side drive voltage at VGL is 12V(typ.) and high side drive voltage at CHP is VS+12V(typ.). For functionality see Figure 6.

Under-voltage protection for the low side drivers activates if VGL falls below 4.8V in which case the output FET's will be turned off and VGL under-voltage error is flagged in register MRDIAG. Over-voltage protection for the high side drivers activates if VS becomes greater than 20V(min). In that event the driver stage is disabled, over-voltage error is flagged in register MRDIAG, and both VGL and CHP are discharged to prevent output circuit destruction.

The charge pump circuit operates nominally at 52.1KHz. A SSCG function is provided to add a spread-spectrum component for EMI reduction.

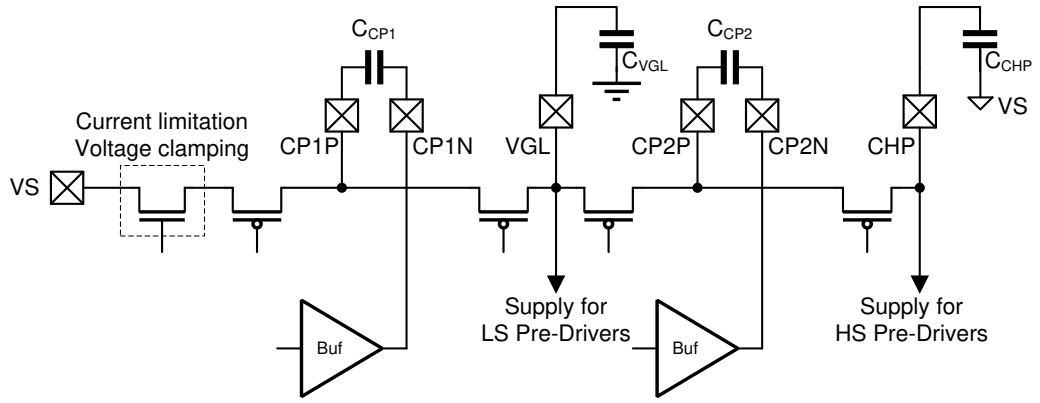


Figure 6: Charge Pump Circuit

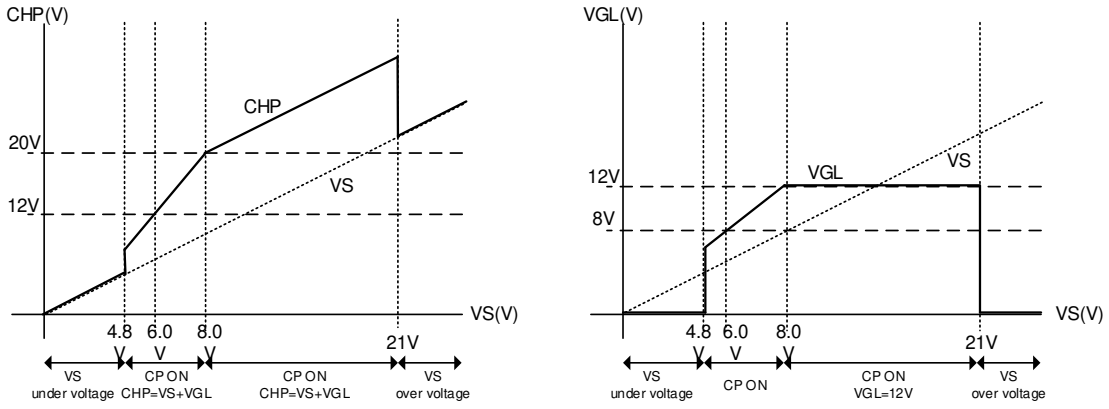


Figure 7: High Side and Low Side Gate Voltages

INPUT PWM and SPEED CONTROL

The LV8907 provides three speed control methods through the input PWM signal:

1. Direct PWM pass-through
2. Indirect PWM translation
3. Closed loop speed control

Direct PWM Pass-through

The input PWM frequency and duty cycle are directly fed to the power stage. This allows a companion microprocessor direct control over duty cycle and output frequency up to 18.5kHz. No input frequency detection takes place in this mode, so 100% and 0% duty cycle can be applied.
NOTE: It is important not to exceed 18.5kHz to maintain reliable back-EMF detection.
When the register bit PWMF is set 1, this control method is selected.

Indirect PWM Translation

This is the preferred mode for stand-alone operation. In this mode the input PWM signal is compared against minimum and maximum PWM frequency thresholds to allow for more robust operation. Frequencies above 1kHz are ignored and frequencies below 5.3Hz(typ.) are considered as 0% or 100% duty cycle (no frequency). The duty cycle of the PWM input signal is measured with a resolution of 9 bits. There is an inherent delay to detect and utilize this duty cycle information, the motor will not start. The delay time is determined by $T_{PWM} \times \left(1 + \frac{1}{8}\right)$. If faster start-up is necessary, see section "Fast Startup" below. If no frequency is detected after 210ms (typ.) the PWMPO flag is set in system warning register MRDIAG1. Even without PWM input the LV8907 can run as described below in section "Fast Startup".
If a valid frequency was detected, the LV8907 evaluates the input duty cycle and translates it into an output duty cycle as shown in Figure 8. The output PWM frequency is fixed to 19.5kHz (typ.).

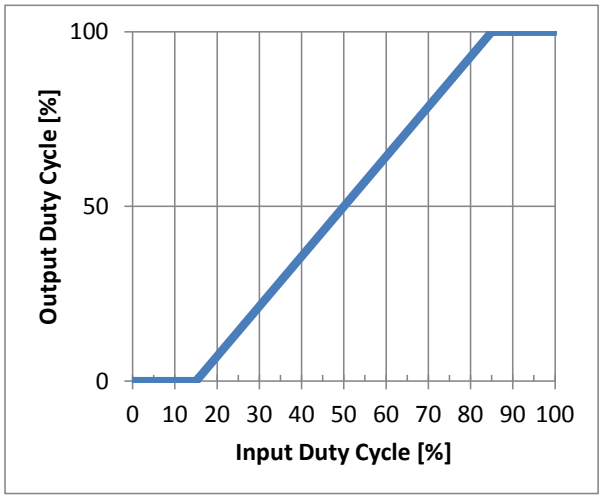


Figure 8: Duty Cycle Translation

Input duty cycles lower than 15% are considered a motor-off command and will also reset the error registers. Input to output duty cycle translation is described by the following formula:

$$d_{OUT} = \begin{cases} 0 & , \quad 0 \le d_{IN} \le 15 \\ \frac{10}{7}(d_{IN} - 15) & , \quad 15 < d_{IN} < 85 \\ 100 & , \quad 85 \le d_{IN} \le 100 \end{cases}$$

Closed loop speed control

For stand-alone operation, the LV8907 offers a PI controller for motor speed which is activated by clearing bit SCEN. Frequencies above 1kHz are ignored and frequencies below 5.3Hz(typ.) are considered as 0% or 100% duty cycle (no frequency). The output PWM frequency is fixed to 19.5kHz (typ.).

LV8907 provides nine target speed values which are stored in registers FGT0 to FGT8. In speed control mode the input PWM duty cycle is encoded as a selector for these registers as shown in Figure 9. A duty cycle hysteresis allows for stable register selection.

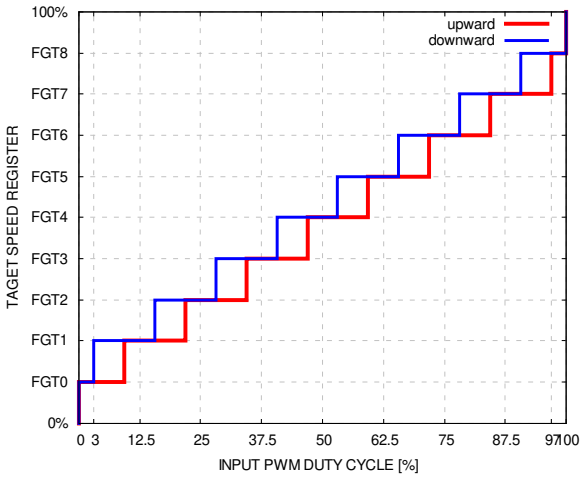


Figure 9: Target Speed Register Selection by Input PWM Duty Cycle

A duty cycle of 50% with a variation band of 6.25% for example will select the motor speed value stored in the 4th speed register FGT4. This allows for non-linear speed curves. When using a companion microcontroller it is possible to write to the speed register in real time during operation to achieve finer RPM resolution. For more information see section "Target speed setting" on page 33.

The Control algorithm

The LV8907 controls the motor speed by comparing the selected target speed to the actual motor speed and incorporating a PI controller with configurable gains for the P and I components which are stored in register MRSPCT0 and MRSPCT1 respectively.

Ramping of Speed Control Values

While tight control is required for optimal speed tracking, it may be undesirable during large input changes as it may lead to sudden supply loading, increasing noise and motor wear. To limit the slope of the control signal, register STEPSEL imposes a ramp on an input step to slew the speed response of the motor.

Decreasing motor speed too fast results in energy recuperation back into the system. To limit over-voltage during energy recuperation, the variable DWNSET allows either

1. to distribute the recuperation energy over a longer period of time or
2. to prevent energy recuperation entirely.

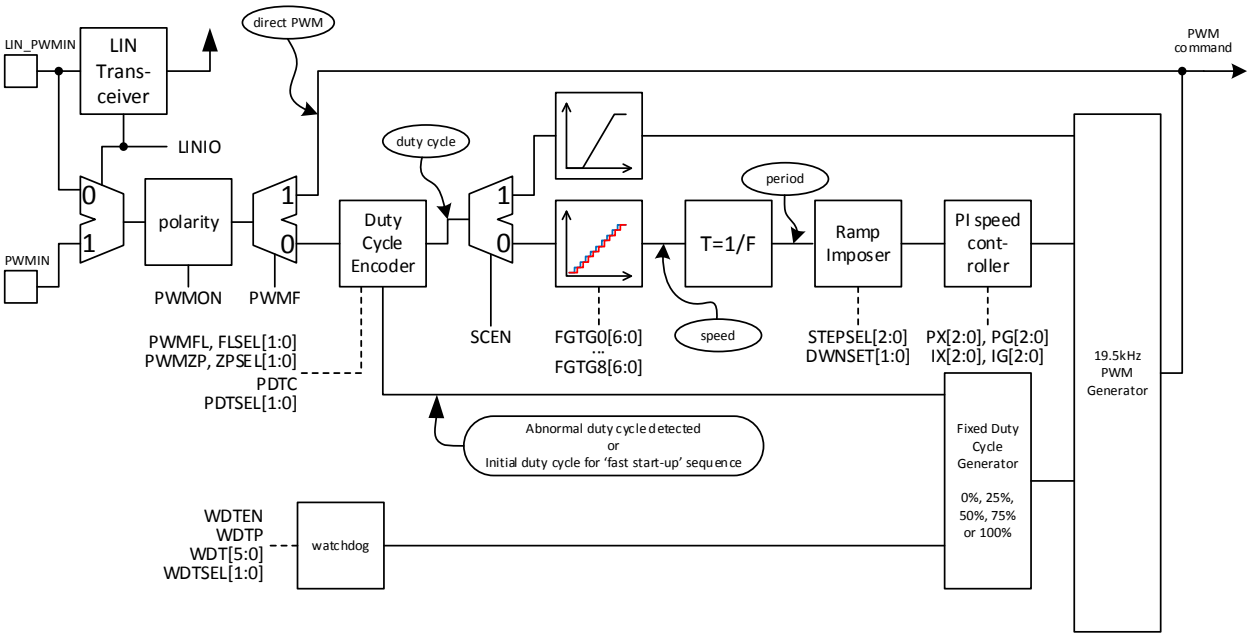


Figure 10: PWM Command Flow and Related Registers

Fast Startup

It may be desirable to have the motor start immediately after EN goes high and not wait for PWM input duty cycle evaluation. Two register settings enable motor operation during this evaluation time: bit PDTC determines if the motor should be running during this time at all, and PDTSEL selects a motor duty cycle of 25, 50, 75 or 100%. This is used as the initial value of the duty cycle command for the closed loop speed control mode. To guarantee smooth transition from fast startup to PWM operation it is important to apply a comparable external PWM duty cycle at startup. Also make sure that free-run detection is disabled (FRREN=1) to improve start-up speed.

Abnormal Duty Cycle Operation (100% or 0%)

For normal duty cycle controlled operation the PWM signal is expected to have a frequency between 5.3Hz and 1kHz. If no frequency is detected, the LV8907 will flag PWMO error and enter 0% or 100% duty cycle mode depending on the level of the PWM signal (all low or all high). Operation during this mode can be selected to be either no motor operation, or motor operation at a fixed motor duty cycle of 25, 50, 75 or 100% as defined by the variables PWMFL and FLSEL or PWMZP and ZPSEL. These PWM values do not enter into the speed control loop.

Speed Feedback FG

The motor speed is shown at open drain output FG where the transitions are direct representations of the BEMF signal transitions on the motor. The relationship between motor rotation and FG pulses is defined in register FGOF.

Fault Output DIAG

A low on open drain output DIAG indicates a system fault and a shutdown of the driver stage. Per default all system faults self-recover when the fault condition is removed. For some potentially destructive faults such as over-current, FET-short circuit and locked rotor conditions, it is possible to latch the fault condition. For more information on system diagnostics see section "System Errors and Warnings" on page 20.

LIN Transceiver

LIN_PWMIN can be used as a local interconnect network (LIN) 2.2A compatible LIN transceiver by setting the LINIO bit and connecting an external microcontroller to RXD and TXD. The microcontroller must handle the LIN communication and control the LV8907 through EN, PWMIN and the SPI interface. The LIN transceiver can be switched to low slope mode to reduce electromagnetic emissions by setting LINSLP=1. For more information on the automotive LIN bus protocol consult publicly available documentation.

Gate Drive Circuit

The gate drive circuit of the LV8907 includes 3 half-bridge drivers which control external N-Channel FETs for the motor phases U, V and W. The high side drivers UH, VH, WH switch their gate connection either to CHP or the respective phase connection UOUT, VOUT and WOUT. The low-side drivers are switched from VGL to the corresponding source connection SUL, SVL, SWL. Both high and low side switches are not current controlled. Slope control has to be implemented with external components.

Current shoot-through protection of the bridge-drivers is implemented by a dead-time counter that delays the turning- on of the complementary switch. The dead-time can be programmed from 100ns < t_{FDTI} < 3.2us into 5bit parameter FDTI.

To protect against external shorts the drain-source voltage of the active external Power FETs is monitored as well. 4 bit register FSCDL selects a short-circuit shutoff voltage 100mV < V_{FSCLD} < 1.6V. To suppress false triggering during the rising edge of FET activation, a four bit masking time can be programmed in FSCDT.

Current Limit and Over-current Shutoff

An integrated current sense amplifier implements current limiting and over-current shutoff by measuring the motor phase current across a single shunt between RF and RFSENS.

Figure 11 on page 19 shows a summary of the current limit and the over-current shutoff, and the descriptions for each function are in the following sections.

Cycle-by-cycle Current Limit

If the voltage between RF and RFSENS exceeds V_{RF1}=100mV(typ.), the active bridge is turned off until the next PWM period. To suppress switching transients a current limit blanking time 0.1us < t_{CLMASK} < 1.6us can be programmed into register CLMASK.

During soft-start this current limit is ramped from 0 to 100mV in 16 steps during a programmable time 105ms < t_{SSTT} < 6.71s as defined in register SSTT.

Over-current Shutoff

If the bit OCPEN is set and the voltage between RF and RFSENS exceeds V_{RF2} = 200mV(typ.), the LV8907 goes into over-current shutoff and all gate drivers are driving low turning the power FETs high-impedance. To suppress switching transients an over-current shutoff blanking time 0.2us < t_{OCMASK} < 3.2us can be programmed into register OCMASK.

Current	Purpose	Flag	Sense point	Threshold	Turn-off	Recovery
Cycle-by-cycle	Limiter	None	Sense Resistor VRF	100mV	PWM FET	Next PWM cycle
Short to VS	Protector	OCPO	Sense Resistor VRF	200mV	All FET	52.4ms later
		FSPO	FET VDS	configurable		
Short to GND	Protector	FSPO	FET VDS	configurable	All FET	52.4ms later

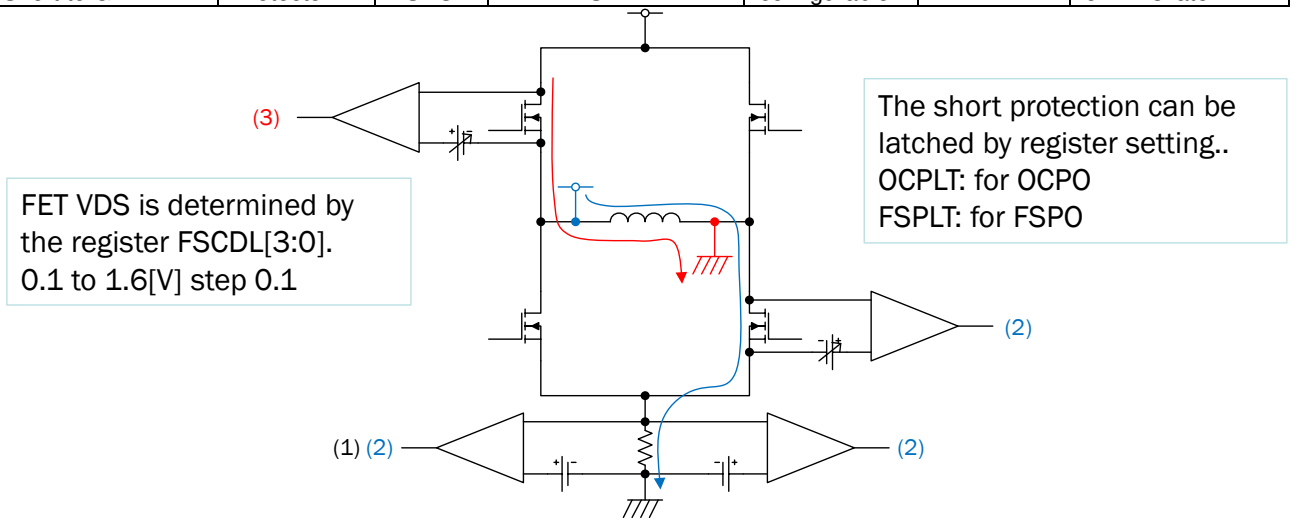


Figure 11: Current Limit vs. Over-current Shutoff

Temperature Sensing

The LV8907 measures internal die temperature and implements internal thermal warning and shutoff. It is also possible to protect external devices by monitoring the voltage at pin TH. Internal and external over-temperature can shut down the driver section.

Internal Over-temperature Measurement

A thermal warning is issued if the internal temperature of the device reaches approximately 25°C below the over-temperature shutoff level. The shutoff level is selected by bit TSTS as 150°C or 175°C(min).

External Over-temperature Shutoff

An analog comparator triggers external over-temperature error if the voltage at pin TH falls below the two bit programmable level 0.2V < V_{THTH} < 0.35V as defined by register THTH. For external temperature measurement connect a resistor between V3RO and TH and an NTC between TH and AGND. The programmed threshold voltage at V_{THTH} should be reached at the intended thermal shutdown temperature of the external component to be protected. During the over-temperature condition, the gate drivers are disabled and a flag, THPO in MRDIAG0 is set.

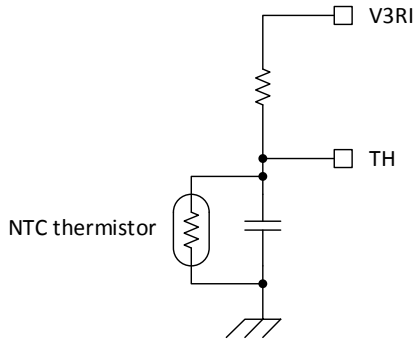


Figure 12: Example Circuit for External Temperature Sensing

Watchdog Operation

The LV8907 includes a watchdog timer to monitor a companion microcontroller and disable the motor if the microcontroller stops working properly. Bit WDTEN enables and disables the watchdog timer. Access to this bit can be blocked – see section “OTP Registers” on page 37 for details. The enabled watchdog will issue an error whenever the watchdog time 1.64ms < t_{WDT} < 104.96ms expires. A write of 00h to register MRST resets the watchdog timer.

A watchdog timeout can result in either a motor stop, or motor operation at four predefined duty cycles (25%, 50%, 75%, 100%) as defined by WDTP and WDTSEL. The duty cycle is directly applied to the power stage, not through the speed selection registers. The microprocessor is not re-set.

System Errors and Warnings

All system errors and most warnings cause a transition on DIAG. The polarity of this transition can be selected in bit DIAGSEL. The ability of stand-alone applications without microcontroller to react to errors and warnings is limited. For this case various auto-retry strategies are implemented.
If a companion microcontroller exists, more complex error handling is possible and DIAG should be connected to an interrupt input of the microcontroller.

Errors that may cause serious damage such as short-circuit, over-current and locked rotor can be latched by enabling the corresponding latch bit in MRCONF10. In this case the LV8907 will keep the output stage disabled until the latch is cleared by one of the following actions:

- Power on reset.
- EN low.
- Low frequency PWM less than 15% duty cycle.
- SPI write of FFh to MRRST.

If bit DLTO is set ONLY latched errors will cause a transition of DIAG. To detect the other less serious errors and warnings, the diagnostic registers MRDIAG0/MRDIAG1 have to be read regularly via SPI access.

Table 1) Error Register: MRDIAG0[7:0]

Bit	Error	Description	Maskable	Latchable	Self Recovery when latch function turned off
0	OCPO	Over-current Error	X	X	After 52.4ms (typ.) the motor will re-start.
1	VSLVPO	VS Under-voltage			Motor is re-started when voltage recovers.
2	VSOVPO	VS Over-voltage	X		Motor is re-started when voltage recovers.
3	CHPLVPO	CHP Under-voltage			Motor is re-started when voltage recovers.
4	VGLLVPO	VGL Under-voltage			Motor is re-started when voltage recovers.
5	FSPO	FET Short Circuit	X	X	After 52.4ms (typ.) the motor will re-start.
6	THPO	TH Over-temperature	X		Motor is re-started when temperature recovers.
7	CPO	Locked Rotor	X	X	Wait 8 t_{CPTM} periods (see “Motor Lock” on page 15)

See register MRCONF10 for error activation and masking and MRCONF11 for latching options.

Table 2) Warning Register: MRDIAG1[7:0]

Bit	Warning	Description	DIAG	Blankable	Effect
0	THWPO	Junction Temp. Warning	X	X	The IC has exceeded the warning temperature but stays in Normal operation.
1	THSPO	Junction Over-temperature	X		The IC has exceeded the shutoff temperature. Drivers are shut down during over-temperature.
2	WDTPO	Watchdog Timeout	X	X	Driver stage is shut off or continues with pre-selected duty cycle (25, 50, 75, 100%).
3	STUPO	Startup Operation			The motor is running open loop.
4	SPCO	Loss of speed lock			Target speed and actual speed are more than 6.25% different.
5	Internal Use				
6	VCLVPO	VCC under-voltage	X	X	Driver stage off.
7	PWMPO	PWM Input Fault	X		No PWM signal detected. Driver stage is shut off or continues with pre-selected duty cycle (25, 50, 75, 100%).

*An “X” in column “DIAG Blank” means that it is possible to prevent a warning from triggering DIAG see register MRCONF10 for details.

SPI Interface

In the LV8907 the SPI interface is used to perform general communications for status reporting, control and programming.

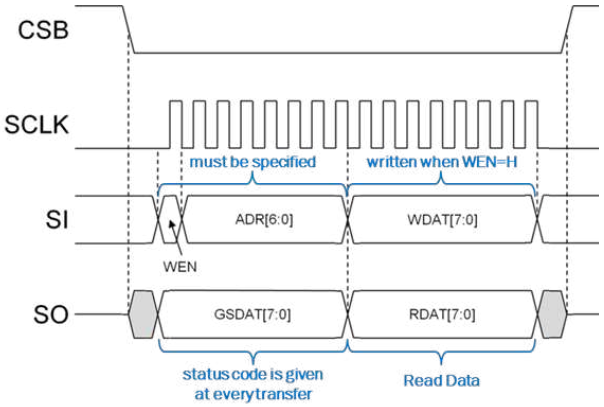


Figure 13: SPI Format

SPI communications with the LV8907 follows established industry standard practices including the use of WEN and start and stop bits as shown above. Data is transferred MSB first and both clock and data are transferred as 'true' data with the higher level indicating a logical 1 or true state. If WEN is LOW, the register data is transferred from LV8907 to the microcontroller. If WEN is HIGH, the register data is transferred from the microcontroller to the LV8907 register.

There are two items to be especially careful of with the general communication scheme:

(1) Communications must be full duplex and simultaneous. It is not allowed to send one transaction and then read data on a second transaction as the status register information will be updated on the first transaction and then be out of date for the second. Some systems break transactions into separate read and write operations which is not acceptable with the LV8907.

(2) It is important the system master uses the clock and data polarities and phases as shown above. Both the clock and data on some systems can be inverted for various reasons but must arrive at the LV8907 per the above drawing. Common errors include SCLK inversion such that the leading edge arrives as a downward transition rather than a rising edge, or having the data to clock phase incorrect. Data phase must be such that the data only changes during a clock falling edge and is completely stable during a clock rising edge. This means a good margin of one half of a bit time exists to eliminate transmission delay hazards.

The first byte returned on all transactions is always the status register, GSDAT, and contains information such as the busy flag during programming operations.

GSDAT[7:0]								
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**	
ORBEN	STUPO	SACF	DIAGS	LATCH	OBSY	SMOD[1:0]		
						0	0	Sleep mode (MRACK[7:0]=FFh)
						0	1	Device start up time
						1	0	Standby mode
						1	1	Normal mode (MRACK [7:0]=55h)
0	x	x	0	0	0	x	x	Normal Operation
					1			OTP busy with read/write access
				1				Latched shutdown condition
			1					Failure Condition
		0						Last SPI access OK
		1						Last SPI access failed*
	0							Motor in Startup mode
	1							Motor in Normal drive mode
1								OTP integrity test mode

The following SPI failures are detectable and reported collectively in GSDAT as general SPI failures:

- Any access to an address which are outside the defined address space.
- The number of SCLK transitions is not 16 within one word transfer.
- Any access to MRCONF, MRACS, ORCONF, ORACS while OBSY=1 (during write operations)
- Write access to MRODL register while OBSY=1 (during write operations.)
- Write access to any of the main registers after setting MSAENB=1 (Implies MRxxxx registers are locked).
- Write access to any of the OTP registers after OSAENB=1 (Implies ORxxxx registers are locked). .
- Write access attempt to a read only or locked register.
- SI signal changed at positive edge of SCLK. (Incorrect data/sclk phase setup)

SPI Timing

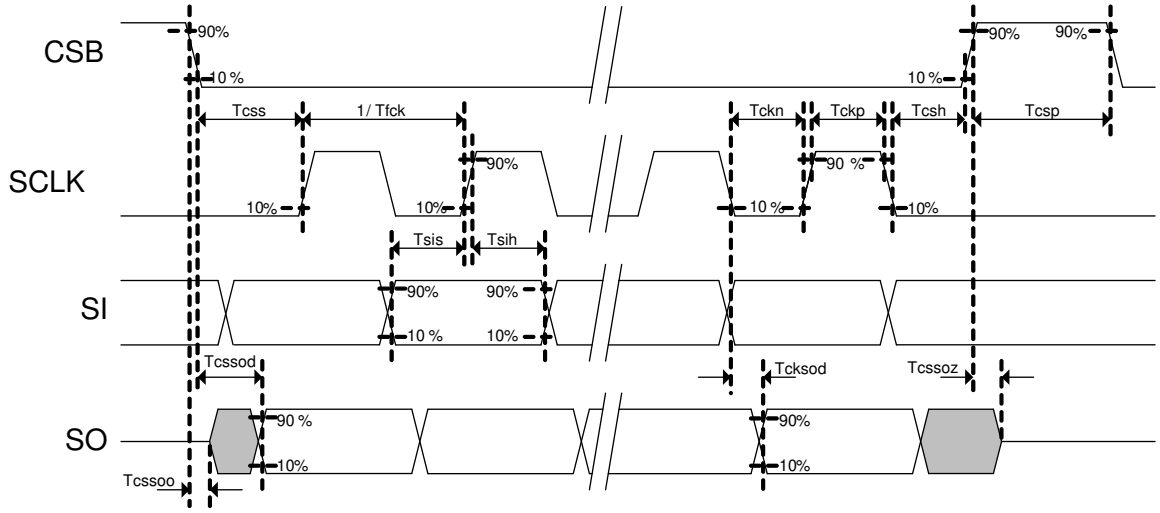


Figure 14: SPI Timing Chart

Tj=-40 to 150°C, VS=4.5 to 20V
Pull-up resistance of SO pin=2.4kΩ, Output load of SO pin=30pF

Symbol	Comment	Min	Typ	Max	Unit
Tfck	SCLK clock frequency			500	kHz
Tckp	SCLK high pulse width	950			ns
Tckn	SCLK low pulse width	950			ns
Tcss	CSB setup time	950			ns
Tcsh	CSB hold time	950			ns
Tcsp	CSB high pulse width	1900			ns
Tsis	SI setup time	450			ns
Tsih	SI hold time	450			ns
Tcssod	CSB fall edge to SO delay time			950	ns
Tcksod	SCLK fall edge to SO delay time			950	ns
Tcssoo	CSB fall edge to SO data out time	0			ns
Tcssoz	CSB rise edge to SO Hi-Z out time			950	ns

REGISTER DESCRIPTION

SPI Register Map

The SPI interface allows read access to the entire address space. The MASTER registers can only be written in Standby mode and then only if the write lock bit MSAENB has never been set high.

Addr	Register	Description	Write Enable	Standby Mode	Normal Mode
IC Setup Register					
00h	MRCONF0	Main function Free-run Detection ON/OFF setup	MSAENB	Read / Write	Read
01h	MRCONF1	PWM Input Specification	MSAENB	Read / Write	Read
02h	MRCONF2	Soft-start EN setup / FG output setup / Dead time setup	MSAENB	Read / Write	Read
03h	MRCONF3	PWM undetected operation mode setup Soft-start setting	MSAENB	Read / Write	Read
04h	MRCONF4	Activation frequency setup	MSAENB	Read / Write	Read
05h	MRCONF5	Current limit detection timing setup / Over-current detection setup	MSAENB	Read / Write	Read
06H	MRCONF5	For Internal Use Only	MSAENB	Read / Write	Read
07h	MRCONF7	Sync rectification setup Protection setup FET short Protection	MSAENB	Read / Write	Read
08h	MRCONF8	SSCG Protection setup Locking Protection Overheat protection	MSAENB	Read / Write	Read
09h	MRCONF9	WDT setup	MSAENB	Read / Write	Read
0Ah	MRCONF10	Error / warning masks and DIAG output setup	MSAENB	Read / Write	Read
0Bh	MRCONF11	Speed FB operation setup at deceleration WDT protection operation setup Latch setup	MSAENB	Read / Write	Read
0Ch	MRCONF12	Lead angle setup Silent drive setup STEP at the time of changing Speed FB target revolution	Always OK	Read / Write	Read / Write
Speed Control Setup					
10h	MRSPCT0	Proportional Gain Setup	Always OK	Read / Write	Read / Write
11h	MRSPCT1	Integral Gain Setup	Always OK	Read / Write	Read / Write
12h	MRSPCT2	3.125% Input PWM	Always OK	Read / Write	Read / Write
13h	MRSPCT3	12.5% Input PWM	Always OK	Read / Write	Read / Write
14h	MRSPCT4	25% Input PWM	Always OK	Read / Write	Read / Write
15h	MRSPCT5	37.5% Input PWM	Always OK	Read / Write	Read / Write
16h	MRSPCT6	50% Input PWM	Always OK	Read / Write	Read / Write
17h	MRSPCT7	62.5% Input PWM	Always OK	Read / Write	Read / Write
18h	MRSPCT8	75% Input PWM	Always OK	Read / Write	Read / Write
19h	MRSPCT9	87.5% Input PWM	Always OK	Read / Write	Read / Write
1Ah	MRSPCT10	96.875% Input PWM	Always OK	Read / Write	Read / Write

Addr	Register	Description	Write Enable	Standby Mode	Normal Mode
System Diagnostics and Test					
20h	MRACS	Lock Bits for OTP and Main Register write		Read	Read
30h	MRACK	SPI Operation Diagnostics	-	Read	Read
31h	MRODL	OTP data READ	Always OK	Read / Write	Read
32h	MRRST	For WDT/Protection Reset	Always OK	Read / Write	Read / Write
33h	MRORB	For OTP Zapping check	Always OK	Read / Write	Read
34h	MRDIAG0	Protection status check	-	Read	Read
35h	MRDIAG1	Protection status check	-	Read	Read
38h	TEST1	Production test register 1			
…					
3C	TEST5	Production test register 5			
OTP Memory Section					
40h	ORCONF0	Default states of MRCONF0 – MRCONF12			
…					
4Ch	ORCONF12	transferred upon startup			
50h	ORSPCT0	Default states of MRSPCT0 – MRSPCT10			
…					
5Ah	ORSPCT10	transferred upon startup			
60h	ORACS	Default states of MRACS			

Motor Configuration Register Overview

ADDR[6:0]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	MRCONF0	FRMD	FRREN	SCEN	PWMF	REGSEL	VCEN	LINSLP	LINIO
01h	MRCONF1	FLSEL[1:0]		ZPSEL[1:0]		PWMFL	PWMZP	PDTC	PWMON
02h	MRCONF2	SSTEN	FGOF[1:0]		FDTI[4:0]				
03h	MRCONF3	PDTSEL[1:0]		SSTT[5:0]					
04h	MRCONF4	STOSC[7:0]							
05h	MRCONF5	CLMASK[3:0]				OCMASK[3:0]			
06h	MRCONF6	Internal Use Only							
07h	MRCONF7	SYNCEN	PPDOSEL	FSCDT[1:0]		FSCDL[3:0]			
08h	MRCONF8	SSCG	CPTM[3:0]				THTH[1:0]		TSTS
09h	MRCONF9	WDTEN	WDTP	WDT[5:0]					
0Ah	MRCONF10	VCLVPEN	CPEN	THWEN	THPEN	FSPEN	OVPEN	OCPEN	DIAGSEL
0Bh	MRCONF11	DWNSET[1:0]		WDTSEL[1:0]		CPLT	FSPLT	OCPLT	DLTO
0Ch	MRCONF12	STEPSEL[2:0]			SLMD	LASET[3:0]			

MRCONF0

Address = 00h				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
FRMD	FRREN	SCEN	PWMF	REGSEL	VCEN	LINSLP	LINIO

FRMD: Forward / reverse selection

The physical motor rotation direction depends on the wiring of the three phases.
FRMD=1 reverses the motor direction.

FRREN: Free-run detection enable

Decides if the LV8907 does a BEMF detection before attempting to start the motor open-loop excitation and commutation.

FRREN=0 Motor will start with a BEMF detection.
FRREN=1 Motor will start open loop with startup parameters.

SCEN: Speed feedback control enable

This bit selects the LV8907 internal speed feedback control or PWM pass-through. Speed feedback control is active when SCEN=0. RPM is selected from input duty cycle as shown in Figure 9 on page 17.
SCEN=1: The closed loop speed control is inactivated.

PWMF: PWM input frequency selection

Decides the PWM input frequency range and PWM translation configuration.
PWMF=0: Indirect PWM translation or closed loop speed control. Valid PWM input frequency from 5.3Hz to 1kHz.
PWMF=1: Direct PWM pass-through. Valid PWM input frequency up to 18.5kHz. In this mode the PWM frequency is directly fed to the power stage. Internal closed loop speed control cannot be used.

The following table shows the configuration summary based on the combination of SCEN and PWMF.

SCEN	PWMF	Speed control	Input PWM frequency range [Hz]	Output PWM frequency
0	0	closed loop	5.3 to 1000	19.5 [kHz]
1	0	indirect translated	5.3 to 1000	19.5 [kHz]
0	1	direct pass-through	up to 18500	same as input
1	1	direct pass-through	up to 18500	same as input

REGSEL: VCC Voltage selection (5V/3.3V)

REGSEL=0 VCC output set to 3.3V.
REGSEL=1 VCC output set to 5V.

VCEN: VCC regulator enable

VCEN=0 VCC is off.
VCEN=1 VCC is active.

LINSLP: LIN slope mode setup

To improve EMI performance the LIN switching slope can be reduced.
LINSLP=0 Normal LIN rise-time.
LINSLP=1 Rise time increased by 1/3.

LINIO: External input system selection

LV8907 has an embedded LIN physical layer which can also be used as a PWM input channel.
LINIO=0 LIN_PWMIN is in PWM input mode.
LINIO=1 The LIN transceiver is active and the PWM signal is taken from PWMIN.

MRCONF1

Address = 01h				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
FLSEL[1,0]		ZPSEL[1,0]		PWMFL	PWMZP	PDTC	PWMON

FLSEL: 100% PWM input duty cycle motor operation

If 100% PWM input duty cycle was detected (no PWM frequency) and PWMFL is set, the motor is driven with the duty cycle programmed into FLSEL as shown in the following table.

FLSEL[1]	FLSEL[0]	Motor Duty Cycle[%]
0	0	25
0	1	50
1	0	75
1	1	100

ZPSEL: 0% PWM input duty cycle motor operation

If 0% PWM input duty cycle is detected (no PWM frequency) and PWMZP is set, the motor is driven with the duty cycle programmed into ZPSEL as shown in the following table.

ZPSEL[1]	ZPSEL[0]	Motor Duty Cycle[%]
0	0	25
0	1	50
1	0	75
1	1	100

PWMFL: Operation mode selection at PWM input duty cycle = 100%

If 100% PWM input duty cycle was detected the motor will be
PWMFL=0: turned off.
PWMFL=1: driven with the duty cycle defined by FLSEL.