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LX1725

15W+15W Stereo Class-D Amplifier
Filterless 30W Mono in BTL

PRODUCTION DATA SHEET

DESCRIPTION

The Microsemi LX1725 is part of a new generation of fully integrated stereo class-D amplifiers from Microsemi. The fully integrated half-bridge output for each channel works with both split and single power supply operation. The outputs can be bridged to run in BTL (Bridge Tied Load) mode. In BTL mode, 3-level modulation is used which allow operation without an L-C filter to reduce system cost and area. The LX1725 has >90% efficiency, with typical output power up to 15W+15W in stereo, and 30W BTL into a 4Ω load with less than 1% THD+N. The amplifier operates over a wide supply voltage range of ±6V to ±15V split supply or 12V to 30V single supply, and consumes a very little quiescent current.

The LX1725 features Mute and Standby modes, over-current protection, POP-free turn-on and turn-off, under-voltage lockout, over-voltage protection and over-temperature protection. All built-in protection modes allow automatic recovery when the fault condition has been cleared. The gain is pin selectable between 14 / 20 / 26dB to accommodate different signal source amplitudes. Several LX1725s can be easily synchronized together to prevent beat frequency interference in multi-channel applications..

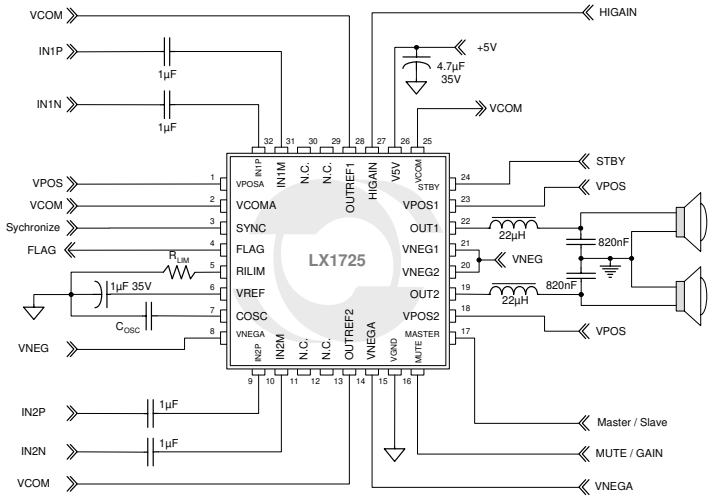
The LX1725 comes in a MLPQ 32 pin package with a 7mmx7mm small outline surface mount.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

KEY FEATURES

- 12Wx2 @ 4Ω THD+N<1%
  16Wx2 @ 4Ω THD+N<10%
- 25W BTL @ 8Ω THD+N<1%
  32W BTL @ 8Ω THD+N<10%
- High Efficiency: >90% @8Ω
- Full Audio Band: 20Hz~20KHz
- Low Distortion:
  <0.1% @1KHz, 8Ω
  <0.4% @20~20KHz, 8Ω
- High Signal-to-Noise Ratio:
  >85dB non A-Weighted
- Split/Single Power Supply
- Wide Supply Voltage Range:
  ±6V ~ ±15V or 12V ~ 30V
- Low Quiescent Current <20mA
- Turn ON/OFF POP Free
- STANDBY/MUTE Feature
- Programmable Gain
  14/20/26dB
- Built-in Over Current Protection
- Built-in Under Voltage Lockout
- Thermal Shut Down
- Power Limiting Based on Die Temperature (gain fold back)
- Synchronization

PRODUCT HIGHLIGHT



APPLICATIONS

- LCD TV, PDP Sets
- CD/DVD Combo Player
- Combo DVD 5.1 Amplifier
- Home Theater System
- Computer Speaker System
- Game Machine

PACKAGE ORDER INFO

T_J(°C)	LQ Plastic MLPQ 32-PIN RoHS Compliant / Pb-free
-40 to +85	**LX1725ILQ**

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1725ILQ-TR)

Rev. 1.2, 2005-12-06

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VPOS/VNEG, VPOSA/VNEGA) ..... -0.3V to ±15V or 30V
Common Supply Voltage (VCOM, VCOMA) ..... -0.3V to ±15V or 30V
Analog Supply Voltage (V5V) ..... -0.3 to 7.0V
Input Voltage (IN1P, IN1M, IN2P, IN2M) ..... -0.3 to 7.0V
Standby and Mute Voltage (STBY, MUTE) ..... -0.3 to 7.0V
Synchronization Input Voltage (MASTER, SYNC) ..... -0.3 to 7.0V
Operating Temperature ..... -40°C to +85°C
Maximum Operating Junction Temperature ..... 150°C
Storage Temperature ..... -65°C to 150°C
Peak Package Solder Reflow Temp.(40 second maximum exposure) ..... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

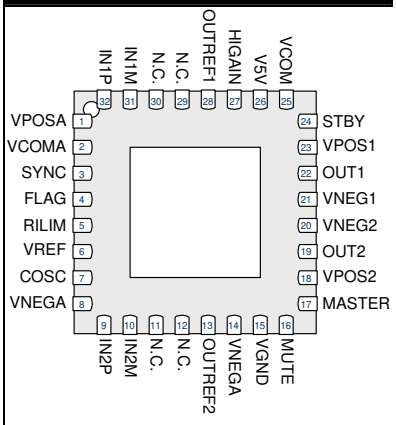
THERMAL DATA

LQ Plastic MLPQ 32-Pin

THERMAL RESISTANCE-JUNCTION TO CASE, θ_{JC}	1.12°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	15.5°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)

Center Pad is VNEG
N.C. – No Internal Connection

RoHS / Pb-free 100% Matte Tin Lead Finish

FUNCTIONAL PIN DESCRIPTION

Name	Description
VPOSA	Analog voltage sense for VPOS voltage. Needs to be protected from noise at VPOS1 and VPOS2. Connect to VPOS bus with appropriate filtering. For VPOSA – VNEGA less than 10V, the under voltage lockout circuit will keep the part in sleep mode. Typically 250µA is drawn at this pin.
VCOMA	Analog voltage sense for VCOM voltage. Typically 150µA is drawn at this pin.
SYNC	Bi-directional clock signal pin. In Master mode, this pin outputs the clock to other slave units. In Slave mode, this pin is a clock input. CMOS logic levels.
FLAG	Monitor point that indicates a fault has been detected. This pin goes high during the power on reset period, when current limiting is in effect, when the voltage at VPOS – VNEG is less than 10V or greater than 33V, when the V5V voltage is less than 4V, and when an over-temperature condition is detected. CMOS logic levels.
RILIM	A current limit-programming resistor should be connected between this pin and ground. A 50KΩ resistor will give a 3.75A current limit threshold. This pin may be connected to V5V in which case both current limiting protection and over-voltage protection will be disabled.
VREF	2.25V reference voltage, used as a local "gnd" reference. Place a decoupling capacitor greater than 1µF between this pin and VGND. This pin will be prone to instability for capacitor values less than this. In applications where more several LX1725s are synchronized together, the VREF pins should all be tied together so that all units use a common VREF voltage.
COSC	Place a capacitor between this pin and VGND to generate the PWM triangle wave. A 125pF capacitor will give an oscillation frequency of about 373KHz. In Master mode, this pin serves as the output for the triangle wave. In Slave mode, this pin is an input. The total capacitance on this pin will determine the frequency of oscillation.

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FUNCTIONAL PIN DESCRIPTION (CONTINUED)

Name	Description
VNEGA	Analog voltage sense for VNEG voltage. Needs to be protected from noise at VNEG1 and VNEG2. Typically, about 180µA is sourced out of this pin.
IN2P	Positive audio input for channel 2. The input signal should be AC-coupled into this pin. The DC bias voltage will be equal to VREF. The input impedance to VREF will be about 17Kohm.
IN2M	Negative audio input for channel 2. The input signal should be AC-coupled into this pin. The DC bias voltage will be equal to VREF. The input impedance to VREF will be about 17Kohm.
OUTREF2	Negative feedback input pin for channel 2. Normally connected to VCOM.
VGND	Ground reference return for the analog +5V power supply. This supply is allowed to "float" between VNEG and VCOM. Typical current out of this pin is about 600µA.
MUTE	Tri-level control pin. When this pin is set to greater than V5V/2, the audio signal path is muted. For voltages between V5V/4 and V5V/2, the audio gain will be set to approximately 5V/V. This allows the "Low Gain" mode to be tested. For voltages less than V5V/4, the normal 10V/V gain is in place.
MASTER	Quad-level control pin. This pin has three thresholds to enable Master/Slave and the "Quick" test mode. Quick mode forces the internal 65224 clock counter to be bypassed in order to speed-up production testing. Here is how the various modes are mapped: **V @ Master** / **Mode** < V5V/4 — Slave, Normal Mode < V5V/2, >V5V/4 — Slave, Quick mode < 3*V5V/4, >V5V/2 — Master, Quick mode > 3*V5V/4 — Master, Normal mode Normally, this pin should be shorted to either V5V or GND.
VPOS2	Positive voltage supply to channel 2's output buffer. In a split supply system, this voltage will range between +5V up to +15V. In a single supply system, this voltage is allowed to be +10V up to +30V. Power supply de-coupling capacitance should be placed between VPOS2 and VNEG2.
OUT2	PWM output for channel 2. This pin drives the L-C low pass filter prior to driving the speaker.
VNEG2	Negative voltage supply to channel 2's output buffer. In a split supply system, this voltage will range between –5V down to –15V. In a single supply system, this represents the 0V point.
VNEG1	Negative voltage supply to channel 1's output buffer. In a split supply system, this voltage will range between –5V down to –15V. In a single supply system, this represents the 0V point.
OUT1	PWM output for channel 1. This pin drives the L-C low pass filter prior to driving the speaker.
VPOS1	Positive voltage supply to channel 1's output buffer. In a split supply system, this voltage will range between +5V up to +15V. In a single supply system, this voltage is allowed to be +10V up to +30V. Power supply de-coupling capacitance should be placed between VPOS1 and VNEG1.
STBY	A logic high as this pin forces a zero current standby mode. CMOS logic levels.
VCOM	Mid-voltage supply for both channel 1 and channel 2. This voltage should be half way between VPOS and VNEG. De-coupling capacitance should be placed between this pin and both VPOS and VNEG.
V5V	Analog +5V supply for the signal processing section. This pin is referenced to VGND. For voltages less than 4V, the under voltage lockout circuit will keep the part in sleep mode. De-coupling capacitance should be placed between this pin and VGND.

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FUNCTIONAL PIN DESCRIPTION (CONTINUED)

Name	Description
HIGAIN	High Gain mode control pin. If connected to V5V gives +6dB more gain.
OUTREF1	Negative feedback input pin for channel 1, normally connected to VCOM.
IN1M	Negative audio input for channel 1. The input signal should be AC-coupled into this pin. The DC bias voltage will be equal to VREF. The input impedance to VREF will be about 17Kohm.
IN1P	Positive audio input for channel 1. The input signal should be AC-coupled into this pin. The DC bias voltage will be equal to VREF. The input impedance to VREF will be about 17Kohm.

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ELECTRICAL CHARACTERISTICS

Notes: Unless otherwise specified, the following specifications apply over the operating ambient temperature T_A = -40 ~ +85°C°C except where otherwise noted (typical @ T_A = 25°C) and the following test conditions: VPOS = +12V, VNEG = -12V, VGND = 0V, V5V = 5V, VCOM = 0V R_{ILIM} = 50Kohm, C_{OSC} = 220pF, R_L = 8Ω.

Parameter	Symbol	Test Conditions	LX1725			Units
			Min	Typ	Max	
OSCILLATOR						
Oscillator Frequency	FOSC	Varies with C_{OSC} capacitor value, value shown is for default conditions.	160	220	280	KHz
Voltage Stability		VPOS-VNEG = 12V to 30V			10	%
Temperature Stability		T_A = 0°C to 70°C			5	%
		T_A = -40°C to 85°C			8	%
POWER SUPPLY						
Supply Voltage	V_{POS}/V_{NEG}	VCOM to GND	±6	±12	±15	V
		VNEG to GND	12	24	30	
	V5V	@ Single Power Supply	4.5	5.0	5.5	
Stand-By Current		STBY Enable, T_A = 25°C @ V5V			250	µA
Operating Current		STBY Disabled, MUTE Enabled @ V5V		15	20	mA
GAIN						
High Gain Mode	GHIGH	P_{OUT} = 4W, F = 1kHz, V_{MUTE} = V_{GND}, HIGAIN = V5V	18	22	26	V/V
Normal Gain	G_{NOM}	Pout=1W, F=1KHz, V_{MUTE} = V_{GND}, HIGAIN = V_{GND}	9	11	13	V/V
Low Gain	G_{LOW}	Pout=0.25W, F=1KHz, V5V / 4 < V_{MUTE} < V5V / 2, HIGAIN = V_{GND}	4.5	5.5	6.5	V/V
Mute Gain	G_{MUTE}	Input 2Vpp, F=1KHz, V_{MUTE} = V5V		0.01	0.045	V/V
OFFSET						
Output DC Offset	Voff	Measured WRT VCOM		100	170	mV
INPUT STAGE						
Input Resistance	R_{IN}	Single-ended	17		27	KΩ
Common Mode Voltage	V_{CM}			2.29		V
Common Mode Rejection Ratio	CMRR			60		dB
OUTPUT STAGE						
PFET On resistance	R_{DSONp}	VPOS = 12V, VNEG = -12V, Ids = 0.2A		550	900	mΩ
NFET On resistance	R_{DSONn}	VPOS = 12V, VNEG = -12V, Ids = 0.2A		550	900	mΩ
CURRENT LIMIT						
Current Limit Threshold	Ith	GBNT **		3.75		A
Pulse Qualification Count	Icount	Any 4 out of 5 clock periods		4		
VOLTAGE THRESHOLDS AT VPOS – VNEG						
Under Voltage Threshold		VPOS – VNEG	10	12	13.2	V
Start Threshold Hysteresis			0.38	1	1.78	V
UNDER VOLTAGE LOCK-OUT @ V5V						
Start Threshold Voltage			3.8	4		V
THERMAL						
Thermal Gain Fold Back Junction Temperature				125		°C
Thermal shut off Junction Temperature				150		°C

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Notes: Unless otherwise specified, the following specifications apply over the operating ambient temperature T_A = -40 ~ 85°C except where otherwise noted (typical @ T_A = 25°C) and the following test conditions: VPOS=+12V, VNEG=-12V, VGND = 0V, V5V = 5V, VCOM = 0V R_{ILIM} = 50Kohm, C_{OSC} = 220pF, R_L=8Ω.

Parameter	Symbol	Test Conditions	LX1725			Units
			Min	Typ	Max	
MUTE / STBY / MASTER SECTION						
MUTE Threshold		Mute Mode @ V5V = 5.0V	2.5			V
		Low Gain Mode @ V5V = 5.0V	1.25		2.5	
		Normal Gain Mode @ V5V = 5.0V			1.25	
STBY Threshold		@ V5V = 5.0V	2.60		2.85	V
STBY To Output Enable		After Power on Reset Pulse, Not Quick Mode		65536		Clocks
Master Threshold		Master, Not Quick Mode @ V5V = 5.0V	3.75			V
		Master, Quick Mode @ V5V = 5.0V	2.50		3.75	
		Slave, Quick Mode @ V5V = 5.0V	1.25		2.50	
		Slave, Not Quick Mode @ V5V = 5.0V			1.25	

* RDSONP and RDSONN include all bond wires and pad resistance.

** GBNT – Guarantee by design and system, no test.

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SYSTEM MODULE CHARACTERISTICS

Notes: Unless otherwise specified, the following specifications apply over the operating ambient temperature T_A = 25°C except where otherwise noted and the following test conditions: VPOS=+12V, VNEG=-12V, VGND = 0V, V5V = 5V, VCOM = 0V R_{ILIM} = 50Kohm, C_{OSC} = 220pF, Output LC filter 47uH/0.68uF, R_L=8Ω, Test equipment built-in BPF 10Hz~22KHz.

Parameter		Symbol	Test Conditions	LX1725 Min	LX1725 Typ	LX1725 Max	Units
AUDIO CHARACTERISTICS							
Output Power Stereo	R_L=8Ω	P_O	V_{POS}/V_{NEG}=±12V; THD+N < 1%		7		W
			V_{POS}/V_{NEG}=±12V; THD+N < 10%		9		
	R_L=4Ω	P_O	V_{POS}/V_{NEG}=±12V; THD+N < 1%		12		
			V_{POS}/V_{NEG}=±12V; THD+N < 10%		16		
Output Power BTL	R_L=8Ω	P_O	V_{POS}-V_{NEG}=±12V; THD+N < 1%		25		
			V_{POS}-V_{NEG}=±12V; THD+N < 10%		32		
Total Harmonic Distortion Stereo	R_L=8Ω	THD+N	V_{POS}/V_{NEG}=±12V ;Pout=1W, FIN=1KHz		0.05	0.08	%
			V_{POS}/V_{NEG}=±12V ;Pout=1W, FIN=20~20KHz			0.5	
	R_L=4Ω	THD+N	V_{POS}/V_{NEG}=±12V ;Pout=1W, FIN=1KHz		0.08	0.1	
			V_{POS}/V_{NEG}=±12V ;Pout=1W, FIN=20~20KHz			0.3	
Total Harmonic Distortion BTL	R_L=8Ω	THD+N	V_{POS}-V_{NEG}=±12V;Pout=1W, FIN=1KHz		0.05	0.08	
			V_{POS}/V_{NEG}=±12V ;Pout=1W, FIN=20~20KHz			0.3	
Power Efficiency R_L=8Ω	Stereo	η	V_{POS}/V_{NEG}=±12V, Pout=Max, THD+N<1%	89	91		%
Power Efficiency R_L=4Ω	Stereo		V_{POS}/V_{NEG}=±12V, Pout=Max, THD+N<1%	80	85		
Channel Crosstalk		V_{XTALK}	Pout=1W, F=1KHz		-60		dB
Audio Bandwidth		BW	Pout=1W, F=20-20KHz R_L=8Ω		2	3	dB
Stage Gain	HIGH	G_{SYS}	V_{IN}=200mVrms, F=20Hz~20KHz		26		dB
	MID		V_{IN}=200mVrms, F=20Hz~20KHz		20		
	LOW		V_{IN}=200mVrms, F=20Hz~20KHz		14		
Mute Output		V_{MUTE}	Input short, system muted, stereo		-60		dB
			Input short, system muted, BTL		-60		
Signal to Noise Ratio	Stereo	SNR	20-20KHz, non A-Weighted, 8Ω		85		dB
			20-20KHz, non A-Weighted, 4Ω		89		
Output Noise Floor	Stereo	V_N	Input short, non A-Weighted @ 20-20KHz, 8Ω		400		μV_{RMS}
			Input short, non A-weighted @ 20-20KHz, 4Ω		300		
CURRENT LIMIT							
Current Limit Threshold		I_{TH}			3.75	4.0	A
Pulse Qualification Count			Any 4 out of 5 clock periods		4		cycles
SUPPLY VOLTAGE LIMIT							
Under Voltage Lock-Out	Split	V_{UVLO}	VPOS	+5			V
			VNEG	-5			
	Single	V_{UVLO}	VPOS, VNEG tied to GND	10			

Note: Characteristics done by system module evaluation.

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SIMPLIFIED BLOCK DIAGRAM

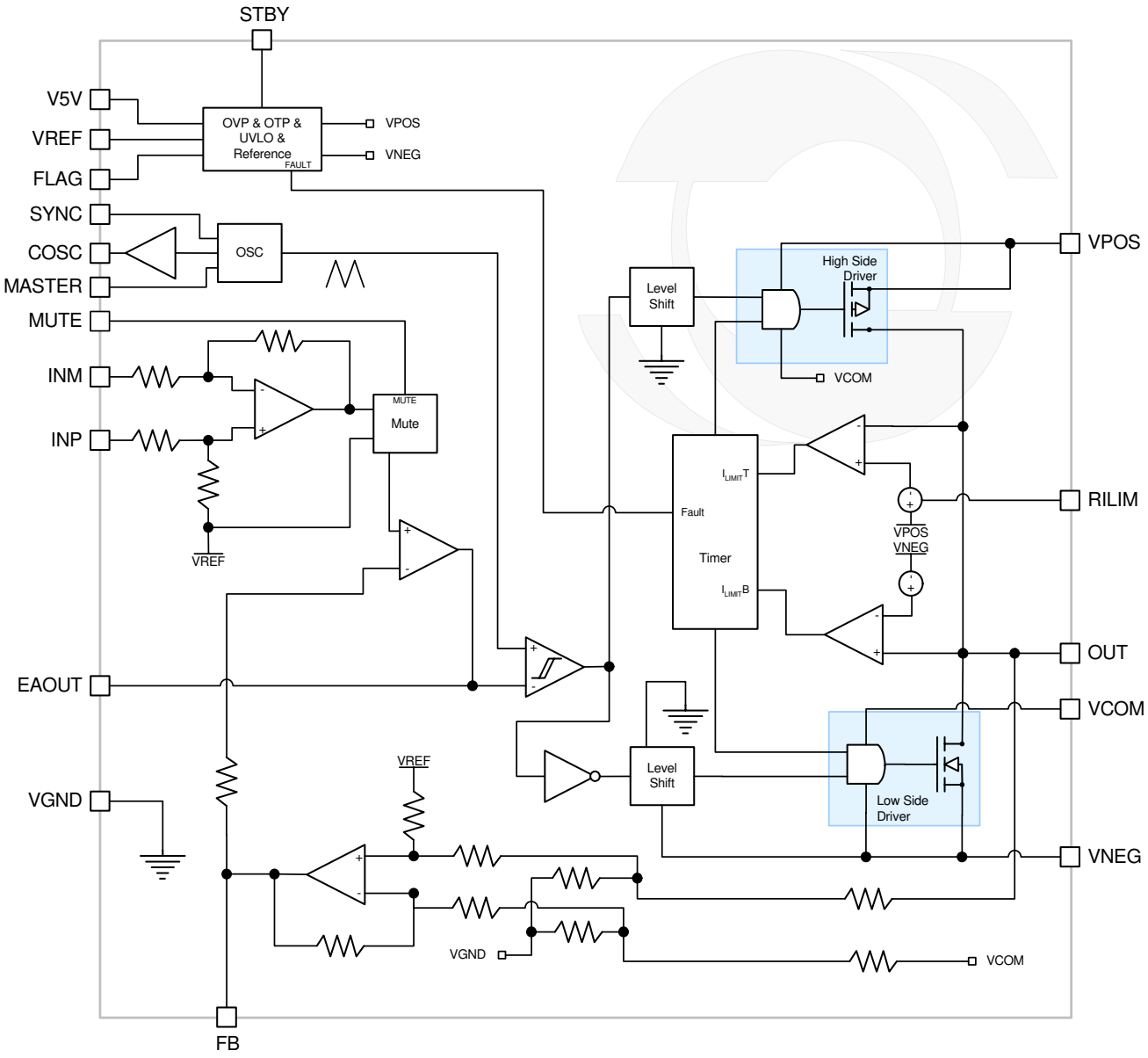

Figure 1 – Simplified Block Diagram (half of the circuit)

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FUNCTION DESCRIPTION

OSCILLATOR

LX1725 has a fixed PWM modulation frequency, but it is programmable by using an external capacitor connected to C_{OSC} pin to GND. The switching frequency is approximately 235KHz with capacitor's value 220pF. With the capacitor value given, the switching frequency can be calculated as follows:

$F_{OSC} = 52000 / C_{OSC}$
F_{OSC} in KHz, and C_{OSC} in pF.

The suggested switching frequency is 250KHz

SYNCHRONIZATION

Two or more LX1725 oscillators can be configured for synchronous operation. One unit, the master, is programmed for the desired frequency with C_{OSC} as usual, also with the MASTER pin tied to V5V. The SYNC pin and the C_{OSC} pin of the slave units should be tied to the SYNC pin and the C_{OSC} pin of the master unit respectively. The MASTER pin of slave components is tied to GND. In this configuration, the SYNC pins of the slave units begin receiving instead of transmitting clock pulses. Also, the C_{OSC} pins quit driving the PWM capacitor in the slave units. Note that for optimum performance, all slave units should be located as close to the master unit as possible (Figure 2).

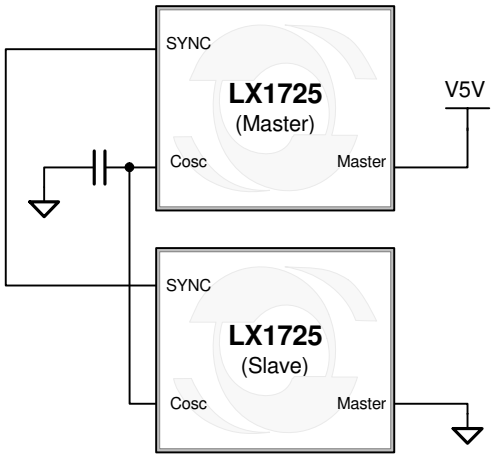

Figure 2 – Two Devices Synchronized Block Diagram

POWER ON RESET (POR)

At start up or upon recovery from a fault condition, an internal "hiccup" counter counts 65536 clock cycles before allowing the outputs to begin switching. See the POR timing sequence in Figure 3.

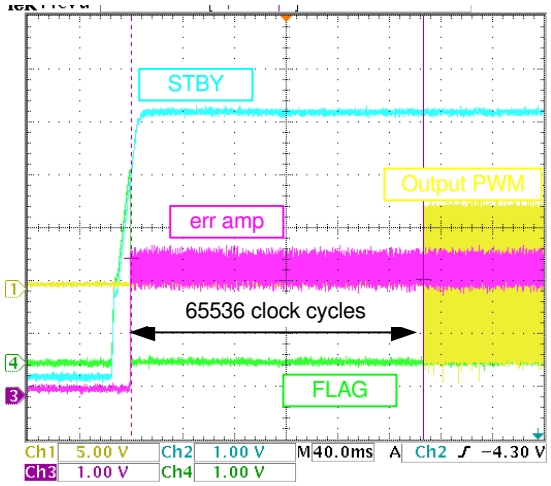

Figure 3 – Power-On-Reset Timing Sequence

The MASTER pin, as mentioned in **SYNCHRONIZATION,** is for multi devices operation. It is also a Quad-level control pin with three thresholds to enable Master/Slave and the "Quick" test mode. Quick mode forces the internal 65536 clock counter to be bypassed in order to speed-up production testing; this is usually for factory production test purposes.

V @ Master	Mode
< V5V/4	Slave, Normal Mode
< V5V/2, >V5V/4	Slave, Quick mode
< 3*V5V/4, >V5V/2	Master, Quick mode
> 3*V5V/4	Master, Normal mode

GAIN SELECTION/MUTE

The channel gain can be programmed between 26dB and 20dB by setting the HIGAIN pin to V5V or to GND. The MUTE pin is a Tri-level control pin for test purposes. When this pin is set to greater than V5V/2, the audio signal path is muted. For voltages between V5V/4 and V5V/2, the audio gain will be reduced by 6dB. This allows the "Low Gain" mode to be tested. For voltages less than V5V/4, the normal gain is in place (Figure 4).

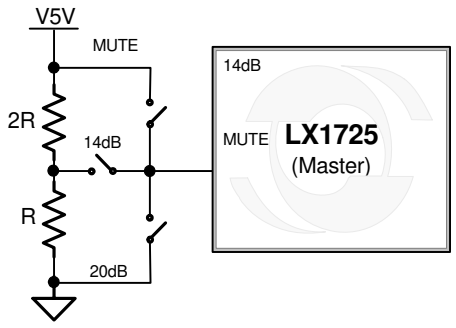

Figure 4 – Gain Selection Block Diagram

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FUNCTION DESCRIPTION(CONTINUED)

STAND BY

Forcing the STBY pin high puts the LX1725 into a zero current sleep mode. The outputs enter a high impedance mode and all internal bias circuits are disabled.

OVER CURRENT LIMIT

The LX1725 has built-in over circuit protection. The circuit works by monitoring the voltage drop across whichever power FET is active. When this voltage is greater than a certain threshold, an over-current condition is assumed. If this condition occurs during five consecutive clock cycles, then the output transistors are immediately disabled. The hiccup counter then counts 65536 clock cycles before allowing the outputs to begin switching again. During this period the FLAG pin goes to HIGH to indicate a system fault. A "hiccup" condition will be clearly audible if a speaker is connected to the outputs. The threshold for the over-current condition is set to 3.75A.

The over current circuit hiccup protection can be disabled by pulling the RILIM pin to V5V.

UNDER VOLTAGE LOCK-OUT (UVLO)

If the voltage drops below ±5V under dual supply operation or 10V under single supply operation, the under voltage lock out circuit is activated and the LX1725 will enter the standby mode. This switch-off will be silent and without pop noise. It will be recovered when the supply voltage rises above the threshold level.

The FLAG pin will go logic HIGH to indicate the system fault. A similar circuit monitors V5V with a threshold of 4V.

THERMAL PROTECTION

When the junction temperature exceeds 125°C, the gain is reduced by 6dB (gain fold back) to reduce the output power and on-chip power dissipation., when the temperature drops below 110°C the gain will returns to normal. When the temperature exceeds 155°C the outputs are shut off to force the output current to zero. Again, when the temperature drops below 130°C the outputs are allowed to switch and normal operation resumes.

AUDIO INPUT

For a high common mode rejection ratio and a maximum flexibility in the application, the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the channels can be inverted, so that a load can be connected between the two output filters. In this case the system operates as a mono BTL amplifier and with the same loudspeaker impedance an approximately four times higher output power can be obtained. The input configuration for a mono BTL application is illustrated in Figure 6. In the stereo single-ended configuration it is also recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies.

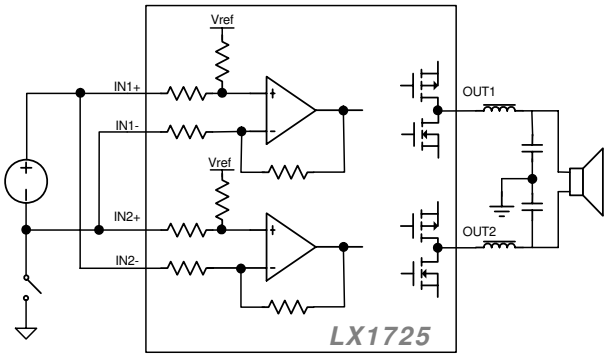

Figure 6 – Audio Input Block Diagram

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TEST CIRCUIT SCHEMATIC

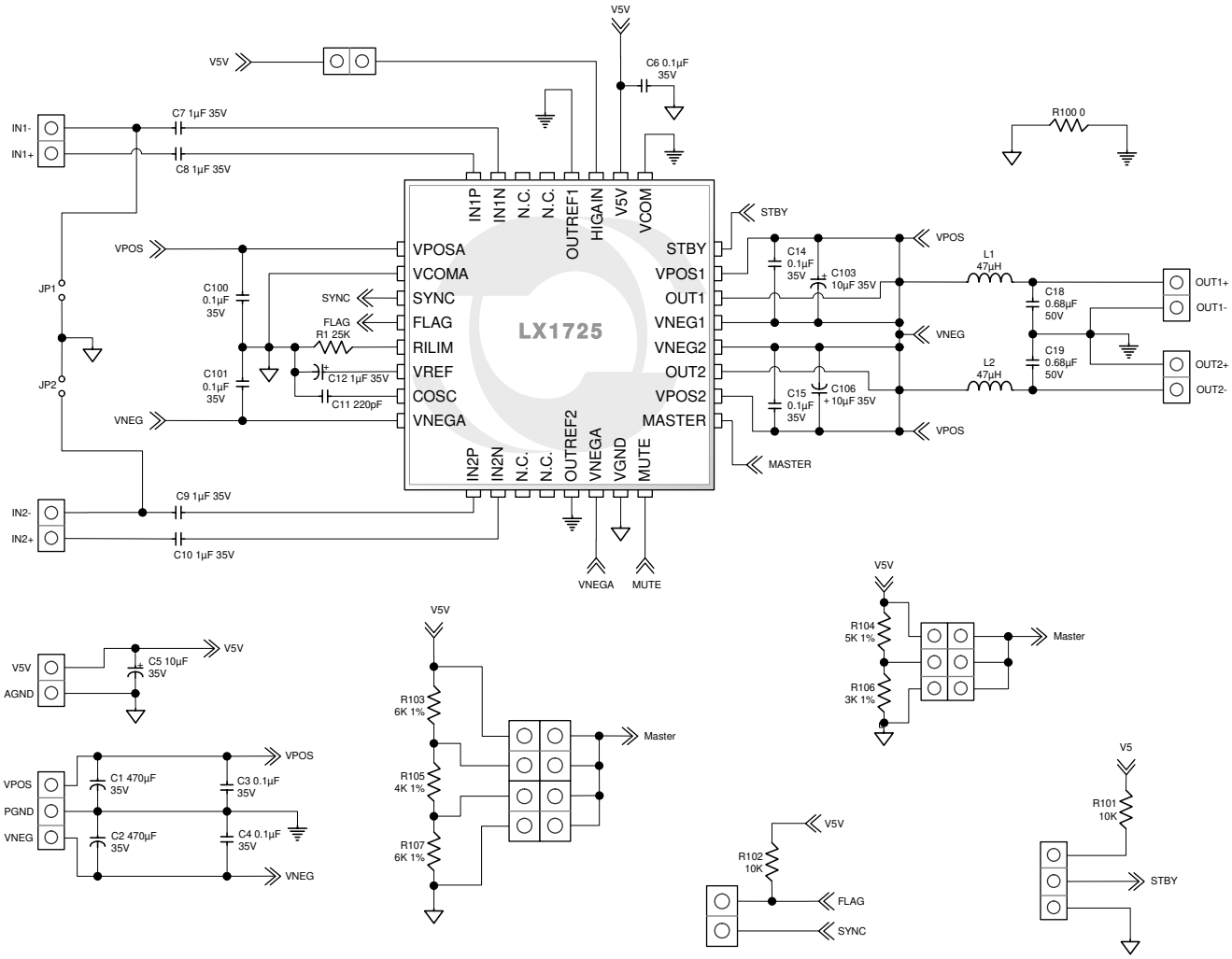

Figure 7 – Test Circuit Schematic (Stereo, Split Supply)

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TEST SYSTEM SET-UP

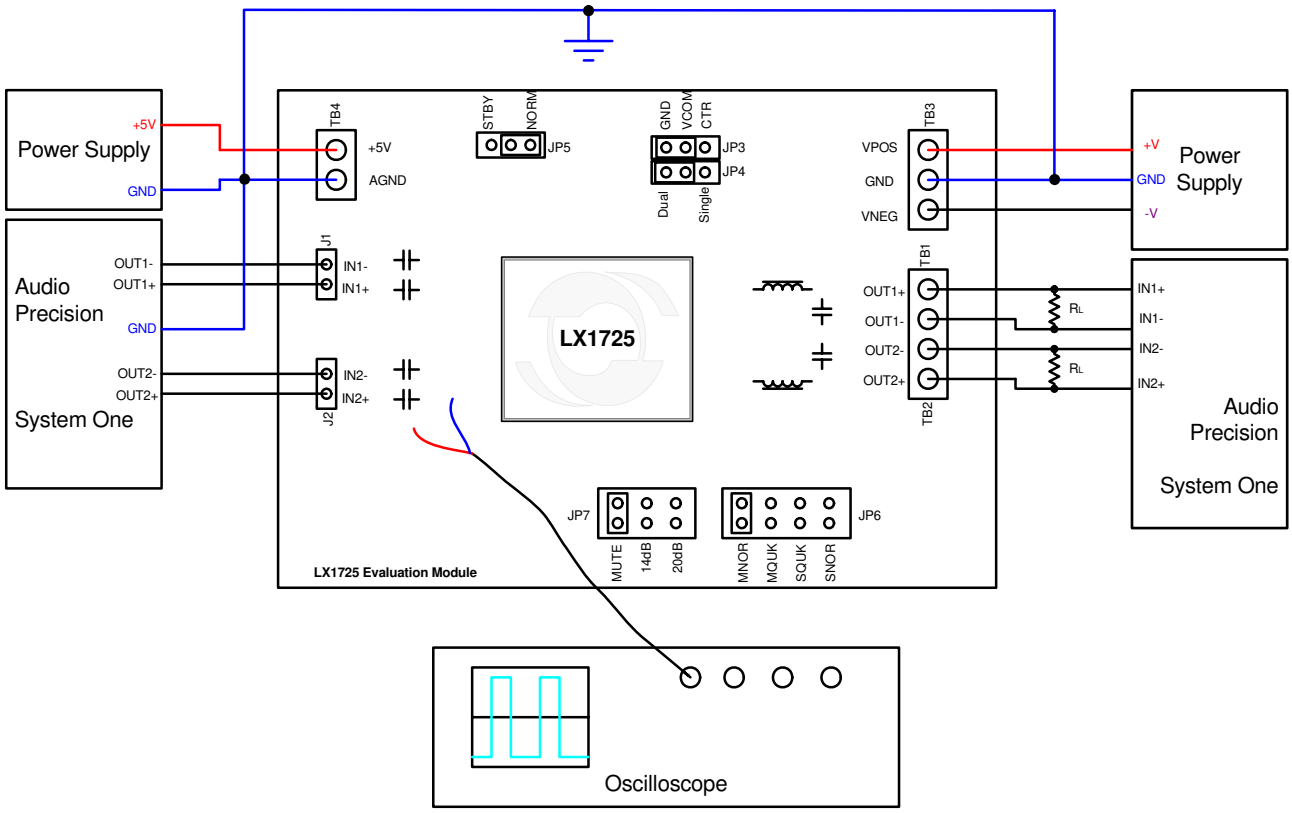

Figure 8 – System Test Set-up

TEST SYSTEM CONFIGURATION

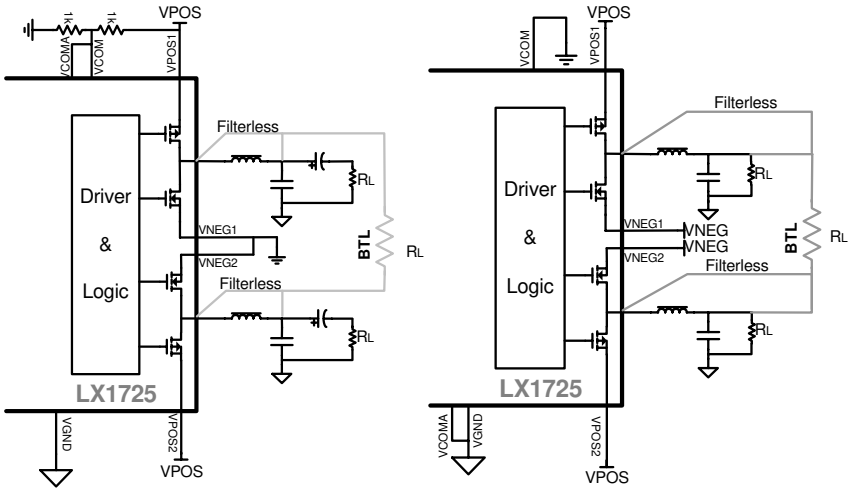

Figure 9 – System Test Configuration

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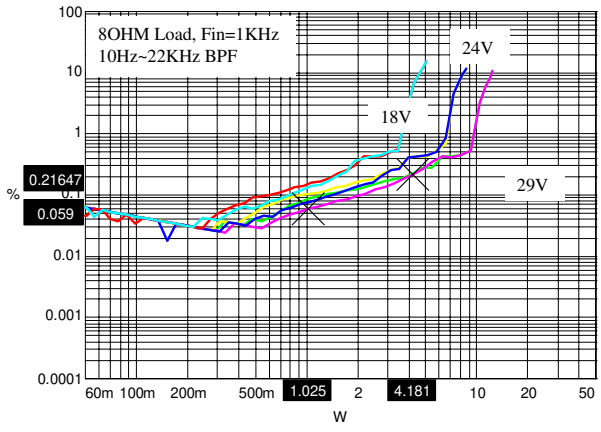
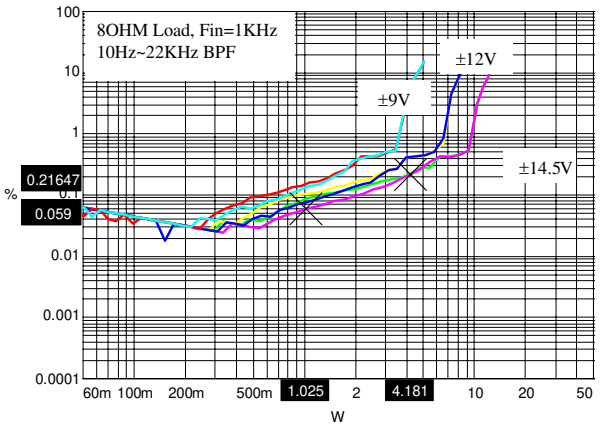
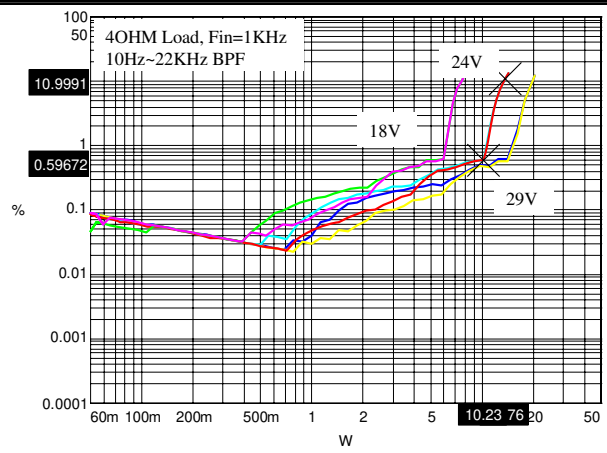
THD+N VS POWER



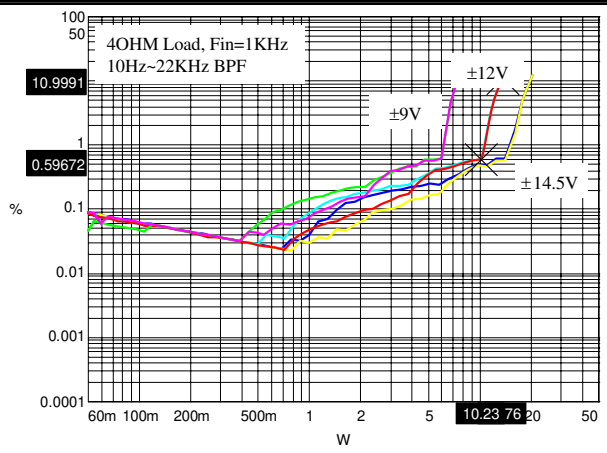
THD+N VS. POWER



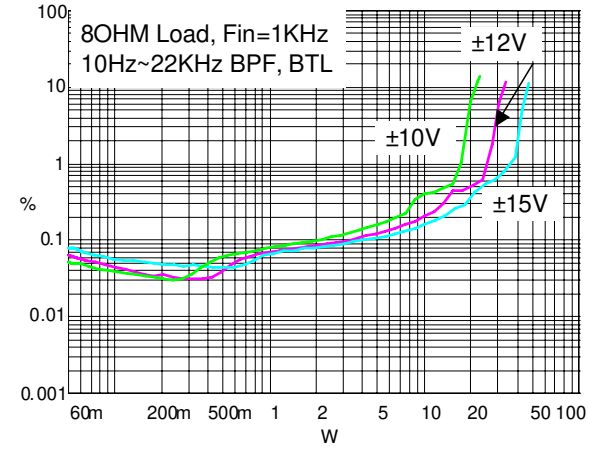
THD+N VS POWER



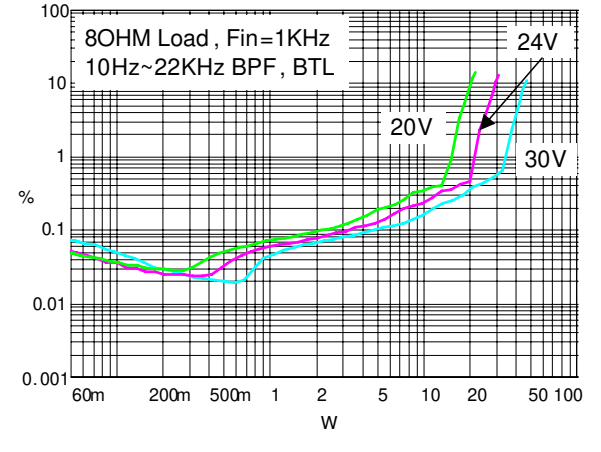
THD+N VS. POWER



THD+N VS POWER



THD+N VS. POWER



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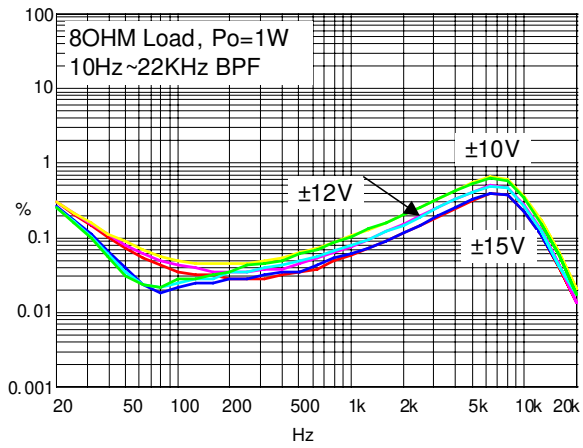
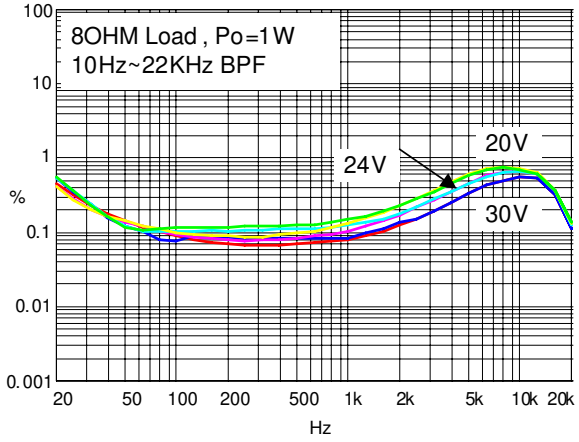
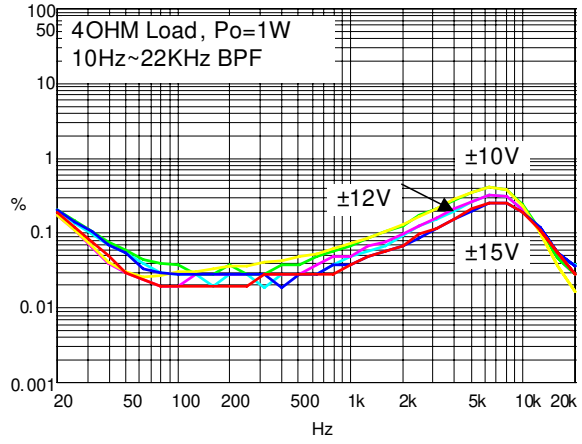
THD+N VS. FREQUENCY



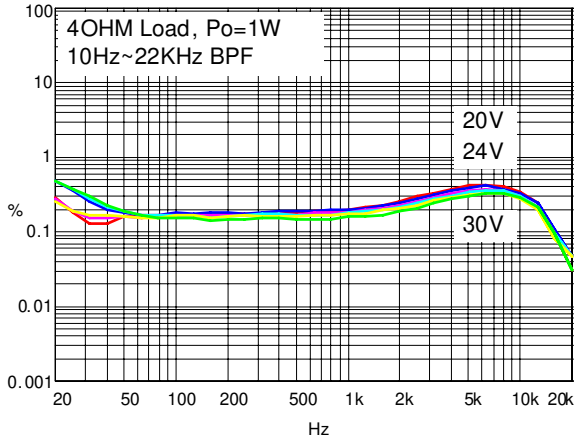
THD+N VS. FREQUENCY



THD+N VS. FREQUENCY



THD+N VS. FREQUENCY



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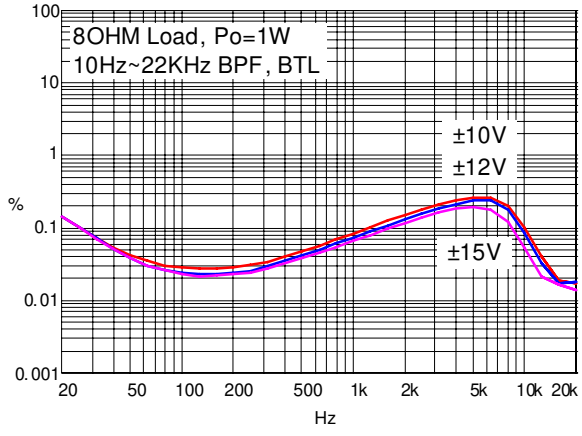
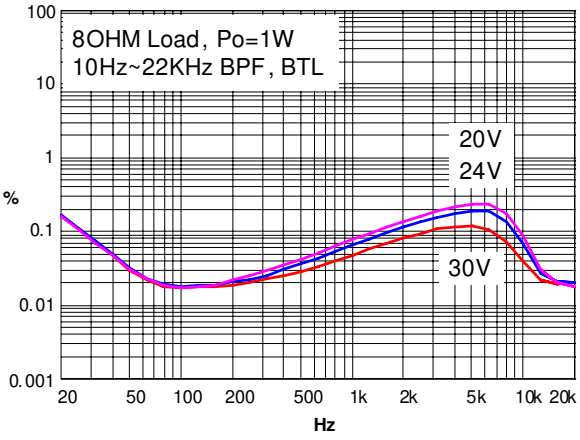


THD+N VS. FREQUENCY



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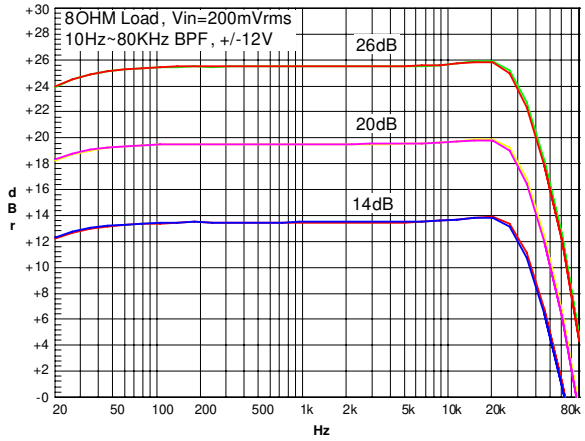
GAIN @ 20 – 20KHZ



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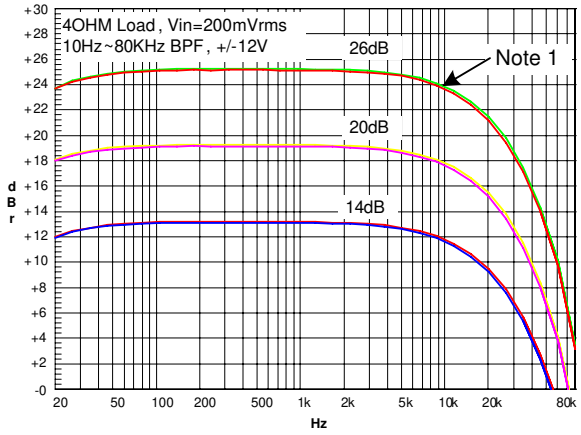

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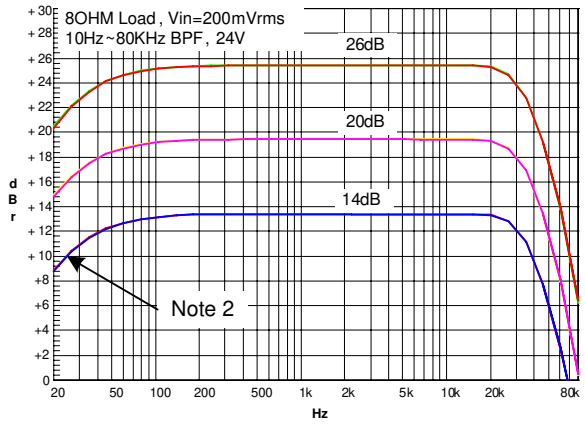

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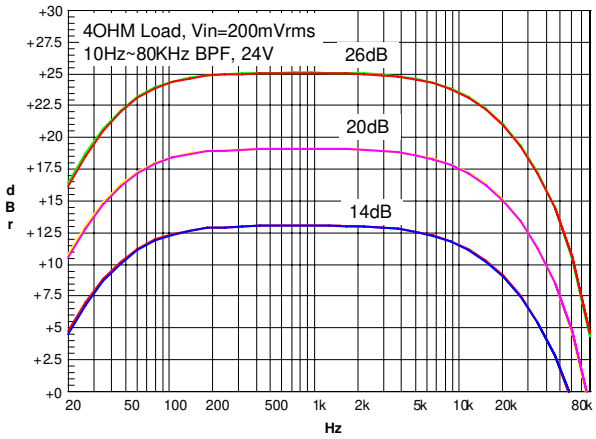

Note 1 – The output LC filter are based on 8OHM design, L=47uH, C=0.68uF, the 4OHM load LC filter design please refer to the application notes.
Note 2 – At single supply mode, the output AC coupling capacitor value based on 470uF, for lower cut-off frequency, please refer to the application notes.

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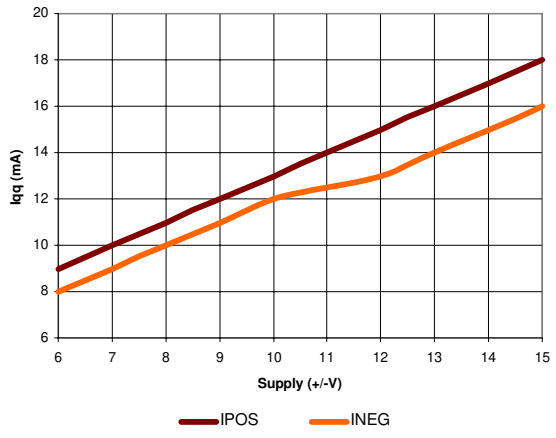
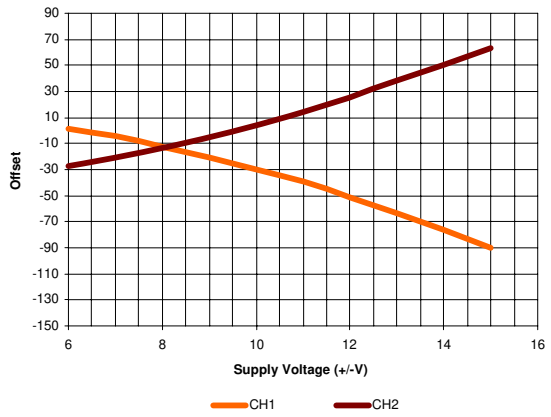
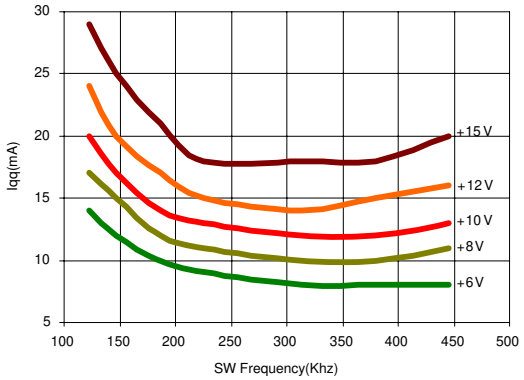
IQQ VS. SUPPLY VOLTAGE



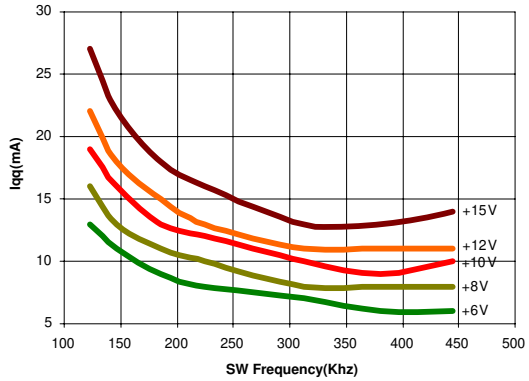
DC OFFSET @SUPPLY



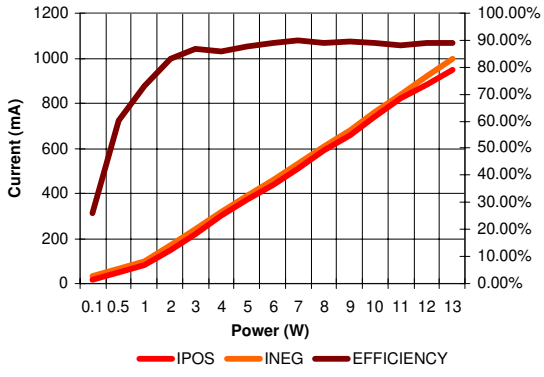
IQQ (POS) VS. SW FREQUENCY



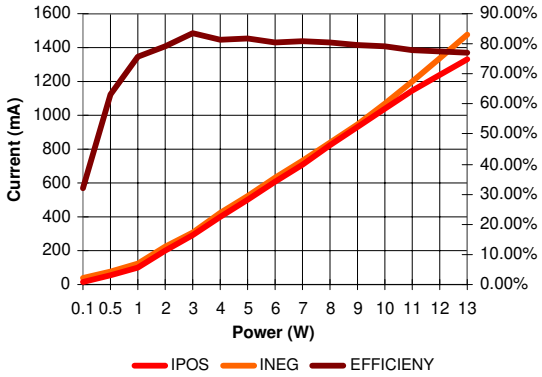
IQQ (NEG) VS. SW FREQUENCY



EFFICIENCY @8OHM LOAD



EFFICIENCY @4OHM LOAD



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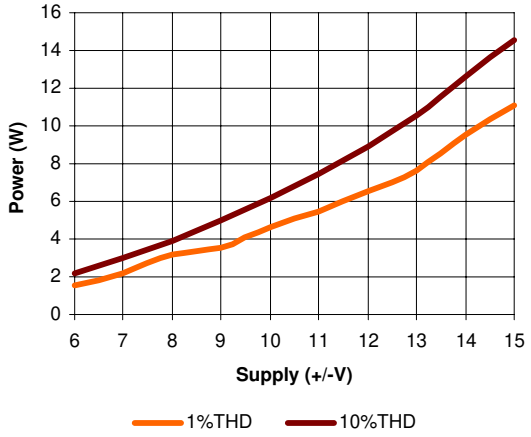
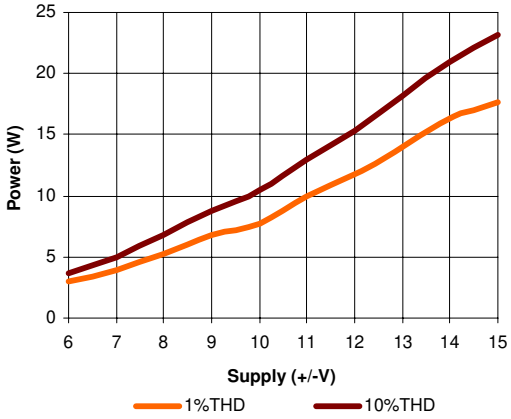
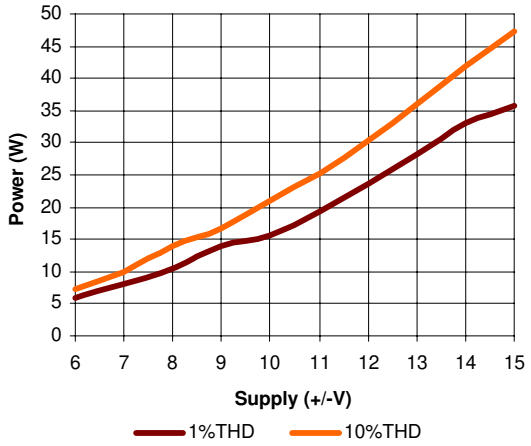
POWER VS. SUPPLY @8OHM



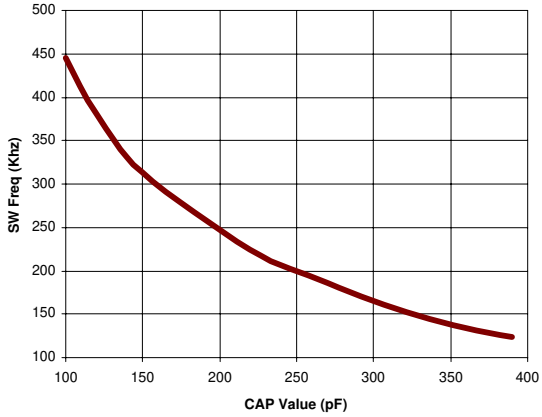
POWER VS. SUPPLY @4OHM



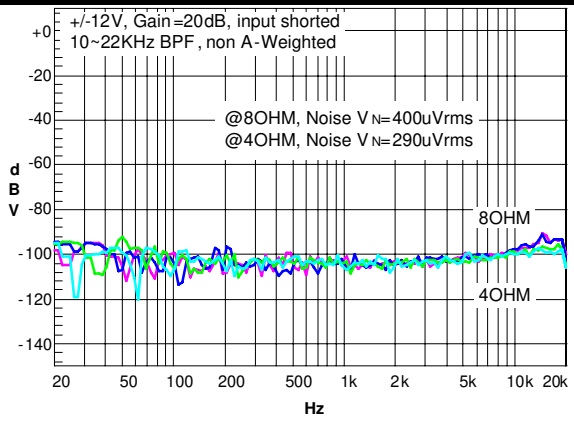
POWER VS. SUPPLY @8OHM BTL



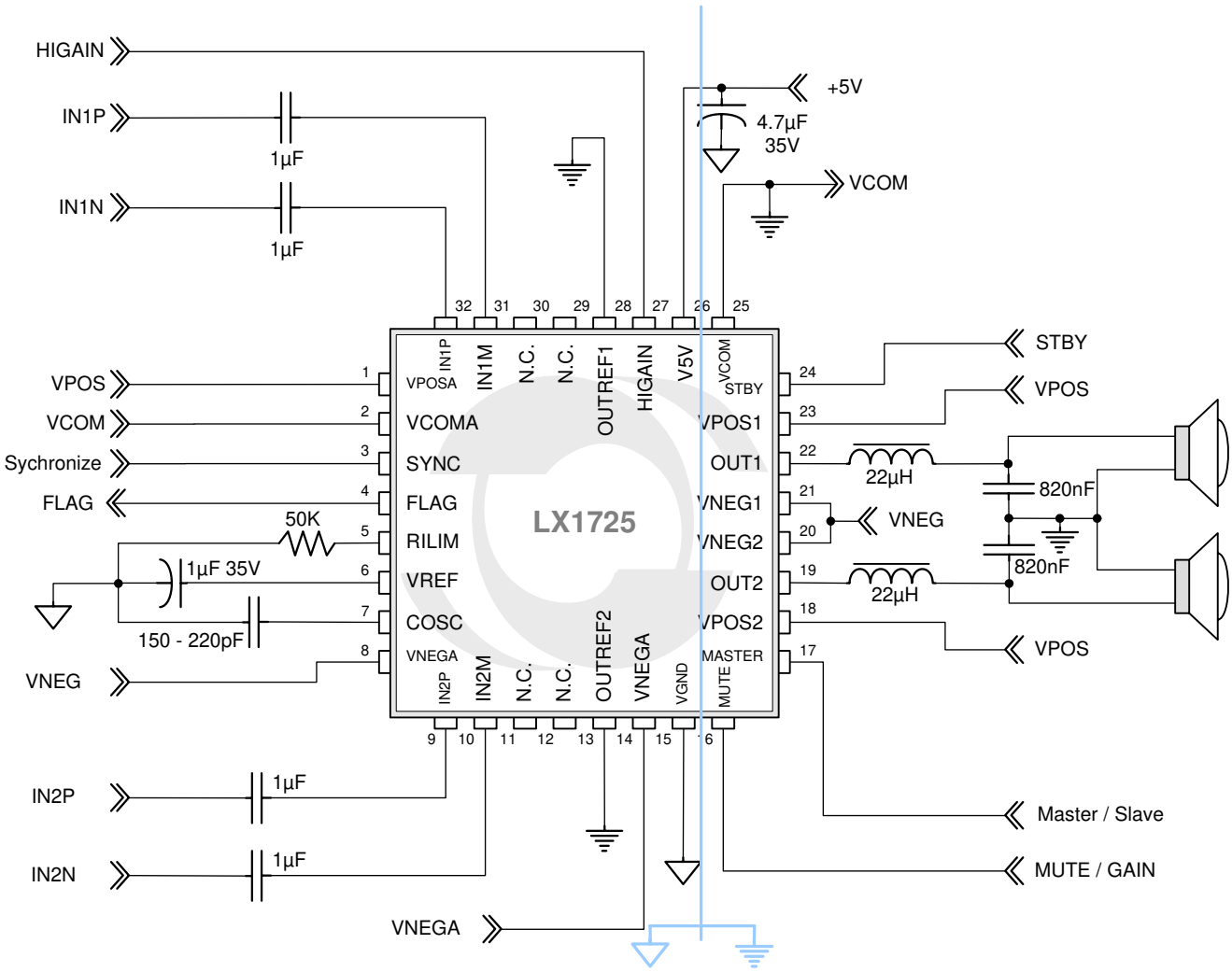
SW FREQUENCY VS. COSC

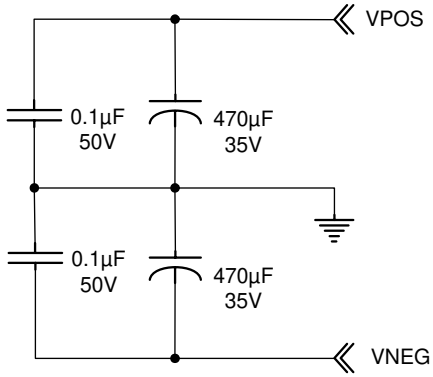


NOISE FLOOR @20-20KHZ



APPLICATION SCHEMATICS





Note: This design for Typical 4Ω load, other than 4Ω. Please refer to application notes AN-35 to change L.C. value

Figure 17 – Application Schematic (Stereo, Split Supply)

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APPLICATION SCHEMATICS (CONTINUED)

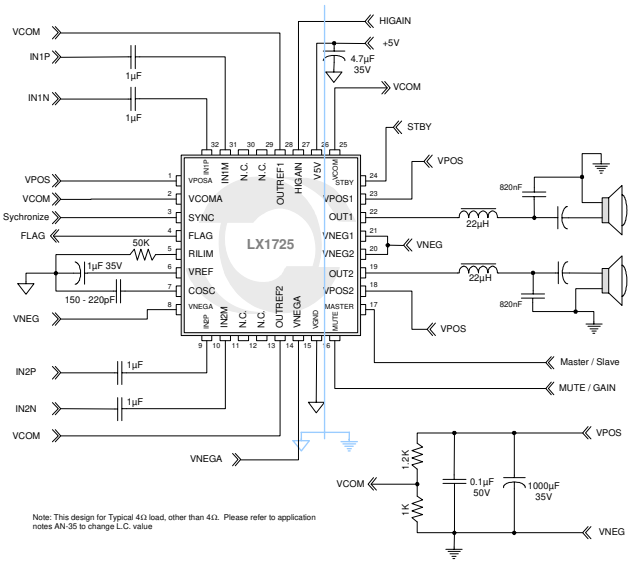

Figure 18 – Application Schematic (Stereo, Single Supply)

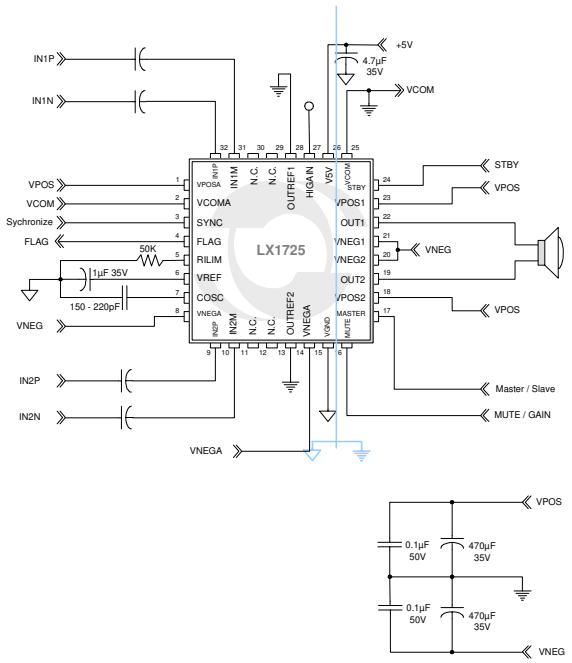

Figure 19 – Application Schematic (BTL, Split Supply)

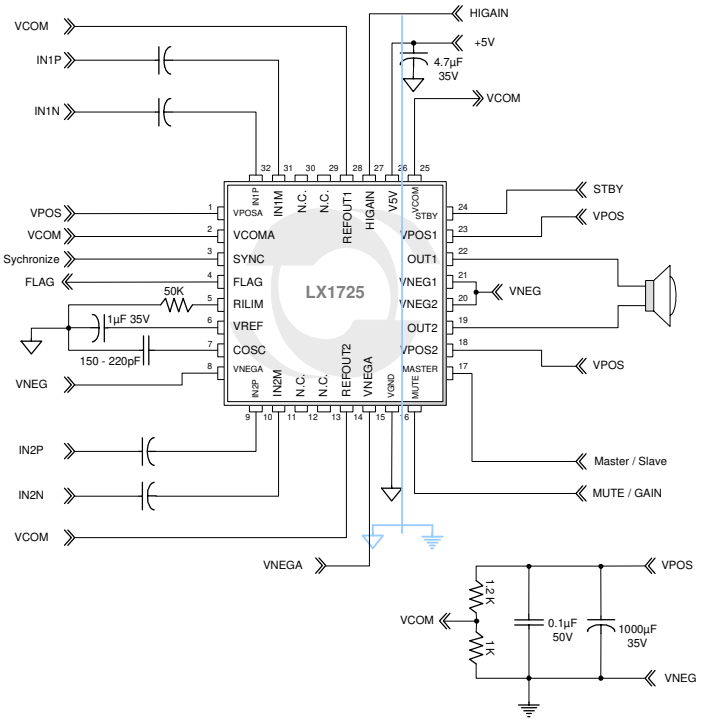

Figure 20 – Application Schematic (BTL, Single Supply)

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PCB DESIGN GUIDELINES

PCB DESIGN GUIDELINES

One of the key efforts in implementing the MLP package on a pc board is the design of the land pattern. The MLP has rectangular metallized terminals exposed on the bottom surface of the package body. Electrical and mechanical connection between the component and the pc board is made by screen printing solder paste on the pc board and then reflowing the paste after placement. To guarantee reliable solder joints it is essential to design the land pattern to the MLP terminal pattern, exposed PAD, and Thermal PAD via. There are two basic designs for PCB land pads for the MLP: Copper Defined style (also known as Non Solder Mask Defined (NSMD)) and the Solder Mask Defined style (SMD). The industry has had some debate on the merits of both styles and although Microsemi recommends the Copper Defined style land pad (NSMD), both styles are acceptable for use with the MLP package.

NSMD pads are recommended over SMD pads due to the tighter tolerance on copper etching than solder masking. NSDM by definition also provides a larger copper pad area and allows the solder to anchor to the edges of the copper pads thus providing improved solder joint reliability.

DESIGN OF PCB LAND PATTERN FOR PACKAGE TERMINALS

As a general rule, the PCB lead finger pad (Y) should be designed 0.2-0.5mm longer than the package terminal length for good filleting. The pad length should extend 0.05mm towards the centerline of the package. The pad width (X) should be a minimum 0.05mm wider than the package terminal width (0.025mm per side), refer to figure 21. However, the pad width is reduced to the width of the component terminal for lead pitches below 0.65mm. This is done to minimize the risk of solder bridging.

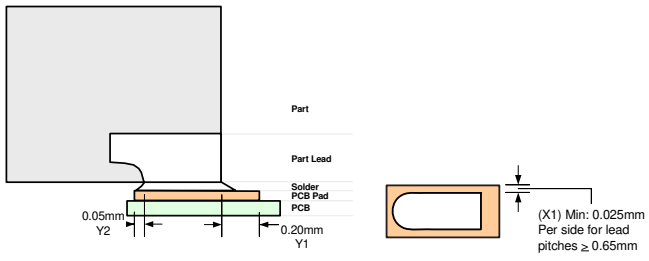


Figure 21 – PC Board Land Pattern Geometry for MLP Terminals

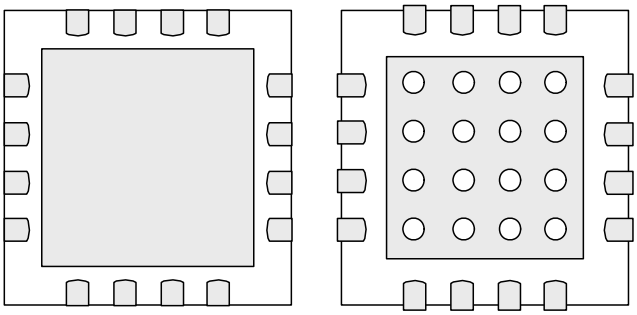
EXPOSED PAD PCB DESIGN

The construction of the Exposed Pad MLP enables enhanced thermal and electrical characteristics. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder. The exposed pad is internally connected to the die substrate potential which is VNEG so it is very important that the PCB substrate potential be connected to VNEG as well.

The thermal pad (D2th) should be greater than D2 of the MLP whenever possible; however adequate clearance (Cpl > 0.15mm) must be met to prevent solder bridging. If this clearance cannot be met, then D2th should be reduced in area. The formula would be: D2TH >D2 only if D2TH < Gmin - (2 x Cpl).

THERMAL PAD VIA DESIGN

There are two types of on-board thermal PAD designs: one is using thermal vias to sink the heat to the other layer with metal traces. Based on the Jedec Specification (JESD 51-5) the thermal vias should be designed like Figure 22. Another one is the no via thermal PAD which is using the same side copper PAD as heat sink, this type of thermal PAD is good for a two layer board, since the bottom side is filled with all other kinds of trace also, it's hard to use the whole plane for the heat sink. But you still can use vias to sink the heat to the bottom layer by the metal traces, then layout a NMSD on which a metal heat sink is put to sink the heat to the air.



Micro Lead Quad Package Land Pattern

Land Pattern for Four Layer Board with Vias

Figure 22 – Comparison of land pattern theory

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PCB DESIGN GUIDELINES (CONTINUED)

The LX1725 is supplied in an MLPQ-7mmx7mm, 32 pin package. θ_{JA} =29.3°C/W for the package by itself in still air. When running at a continuous 20W output power, the on-chip power dissipation will be 3.5W assuming 85% efficiency. With no reduction in the thermal resistance, the die temperature will rise 103 above ambient. θ_{JC} is about 4°C/W. If the exposed pad is properly connected to a heat sink, then the temperature rise will be reduced to around 16°C under these condition. So the non-via type thermal PAD is suggested.

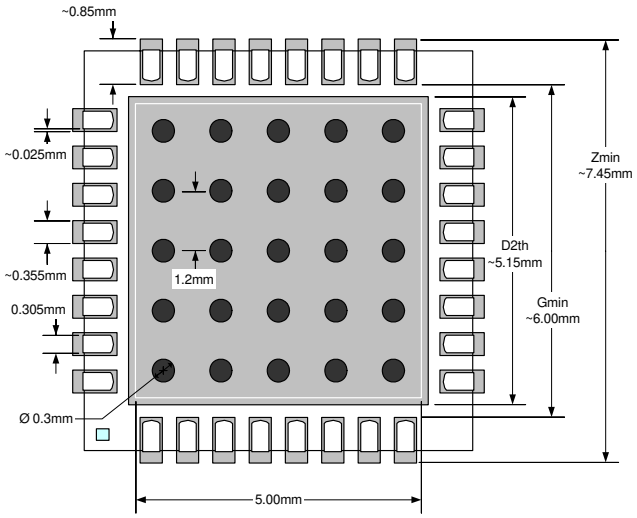

Figure 23 – Recommended Land Pad with Vias for LQ32 (7mm²)

Zmin= D + aaa + 2(0.2)
(where pkg body tolerance aaa=0.15)
(where 0.2 is outer pad extension)
Gmin= D-2(Lmax)-2(0.05)
(where 0.05 is inner pad extension)
(Lmax=0.50 for this example)
D2th max = Gmin-2(CpL)
(where CpL=0.2)

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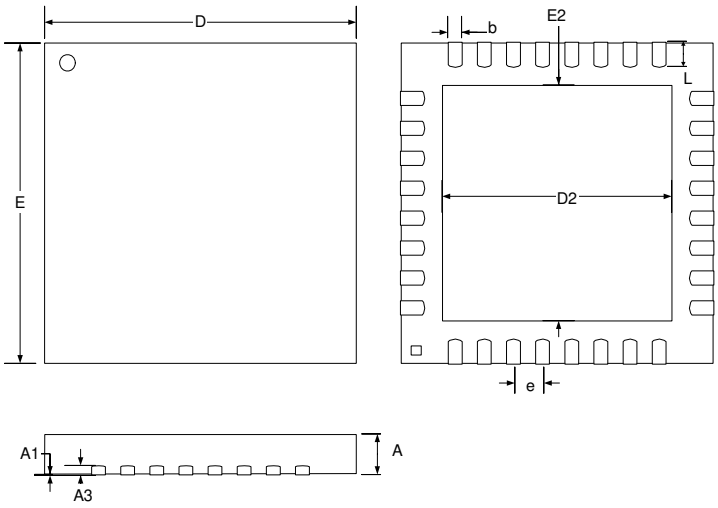
PACKAGE DIMENSIONS

LQ 32-Pin Package Description (Micro Lead Quad Package)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.25 REF		0.010	
b	0.23	0.38	0.009	0.015
D	7.00 BSC		0.276 BSC	
D2	5.00	5.25	0.197	0.207
E	7.00 BSC		0.276 BSC	
E2	5.00	5.25	0.197	0.207
e	0.65 BSC		0.026	
L	0.45	0.65	0.018	0.026

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES