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Microsemi

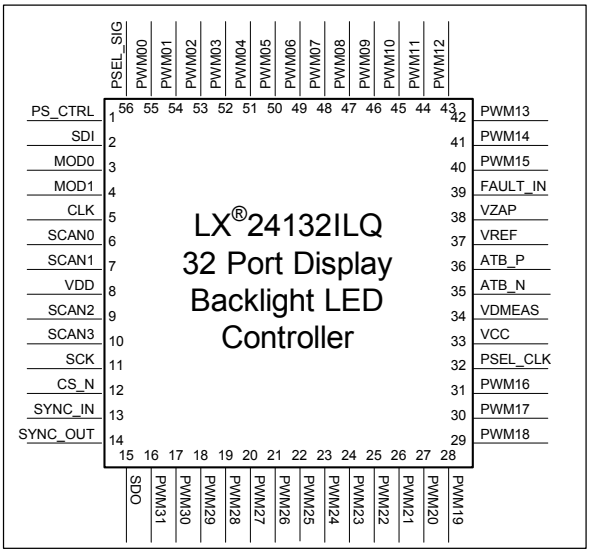
LX24132ILQ - 32 Port Display Backlight LED Controller

Introduction

DESCRIPTION	KEY FEATURES
The LX®24132ILQ is a 32 Port Display Backlight LED Controller. The device is part of a chipset where each LX®24132ILQ is capable of controlling four LX®23108ILQ 8 Port LED Drivers. Each LX®23108ILQ 8 Port LED Driver contains eight FETs driving and controlling up to 4 x 8 LED channels, where each channel is capable of driving a current of up to 200 mA. The LX24132ILQ's internal power supply control circuitry adjusts the voltage level of an external LED power source. This is done by regulating the LED supply voltage to the optimum level, thus minimizing the system power loss. At the same time, accurate current regulation for each of the 32 LED strings is maintained. The LX®24132ILQ 32 Port Display Backlight LED Controller is configured through the SPI interface which speeds up communication and reduces the number of control signals between the LX®24132ILQ and the Host system (FPGA, Video Processor, CPU). The LX®24132ILQ supports a daisy chain connection in cases where more than 32 different LED Controllers (different PWM/Duty cycle) are required. PWM output signals can be synchronized with an external Video Processor V-Sync signal. Each one of the 32 PWM channels can be enabled/disabled by external one out of four SCAN0-3 input pins. The LX®24132ILQ 32 Port Display Backlight LED Controller can detect three types of system faults on each of its 32 channels (over-temperature, open LEDs and short LEDs). After detecting the faults the unit takes the required measures to protect the system.	◆ White or RGB LEDs Backlight controller for large size display panels ◆ Up to 32 LED strings with ±1.5% precision current matching ◆ Wide dimming ratio with PWM and LED current amplitude control ◆ 12-bit PWM duty-cycle resolution and 8-bit resolution for LED current setting ◆ LED power supply voltage control ◆ Automatic minimum FET Vd report ◆ SPI communication interface ◆ Open string, short LED and over-temperature protection for each individual channel ◆ On-chip thermal monitoring ◆ Synchronization to external input pulse (Sync-In) ◆ Enable/Disable PWM output by four input pins (SCAN0-3) ◆ Internal power supply trimming DAC

IMPORTANT: For the most current data, consult Microsemi's website: *http://www.microsemi.com*

Pin Configuration



PACKAGE ORDER INFO	
T_A (°C)	Plastic MLPQ 8 x 8 mm QFN 56 pin
	RoHS Compliant/Pb free
-40° to +85° C	**LX24132ILQ**
Note: Available in Tape & Reel. Add the letters "TR" to the part number. (LX24132ILQ-TR)	

Typical Application

- LCD Display Back-lighting
- LED Signage
- LED Displays

Figure 1 illustrates a typical application where a System Controller communicates with a LX®24132ILQ 32 Port Display Backlight LED Controller through an SPI bus. The LX®24132ILQ is connected to four LX®23108LILQ arrays supporting a total of 32 LED strings. Each LX®23108LILQ transmits current very accurately and can drive eight LED strings. The output currents' value is set by the LX®24132ILQ which produces a precise and stable voltage V_{REF}.

All four LX®23108LILQs are cascaded, allowing the LX®24132ILQ LED Controller to sequentially select all 32 channels for monitoring, search for VDMIN and optimally adjust the power supply voltage through PDM control. Channel dimming is individually adjusted by 32 PWM output pins; 8 inputs per single LX®23108LILQ. Currents are scaled by the external sense resistors.

Figure 2 illustrates multiple connections of several LX®24132ILQs supporting 32x4 LED strings.

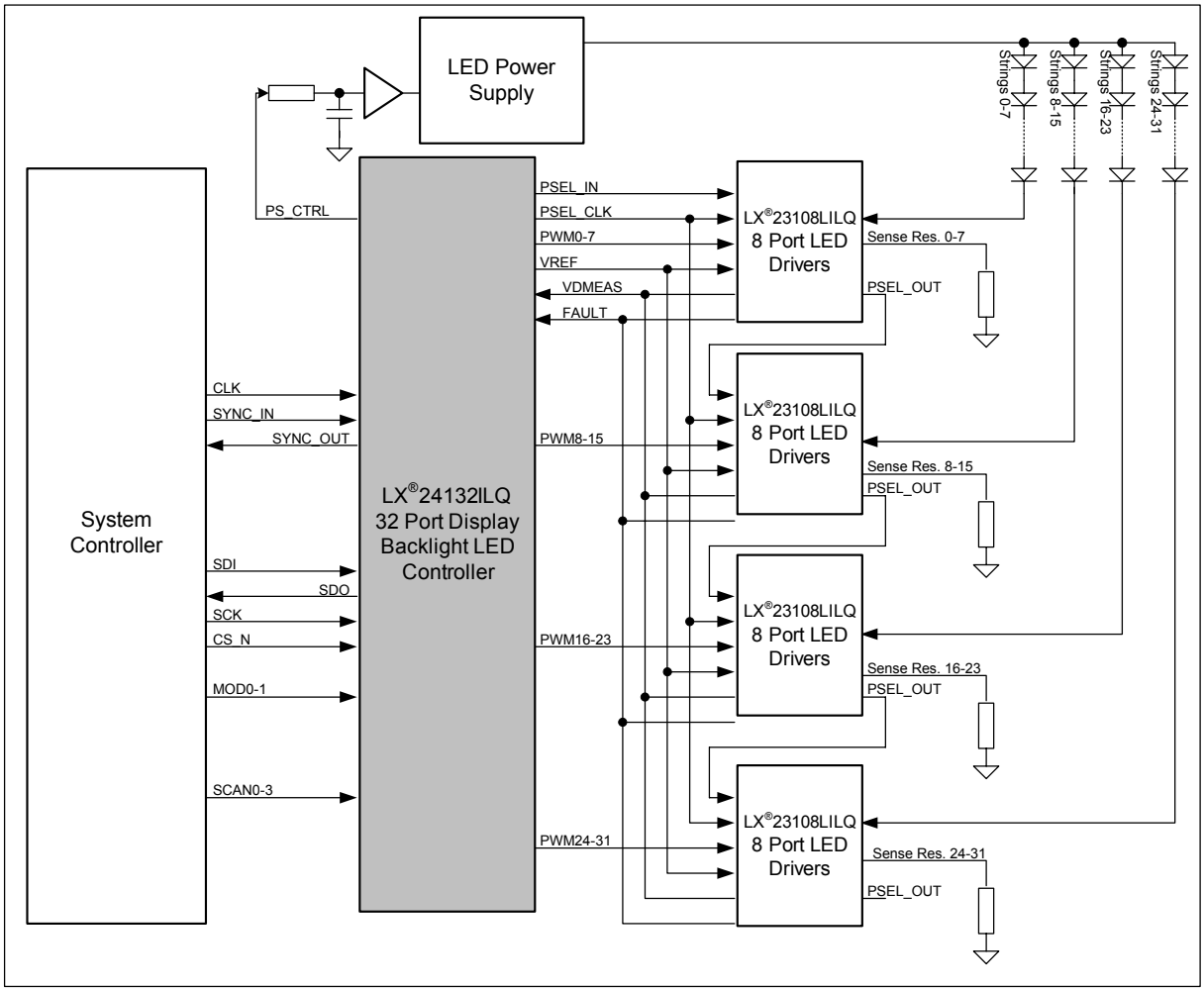


Figure 1: Low Voltage LX®24132ILQ and LX®23108LILQ - Typical Application

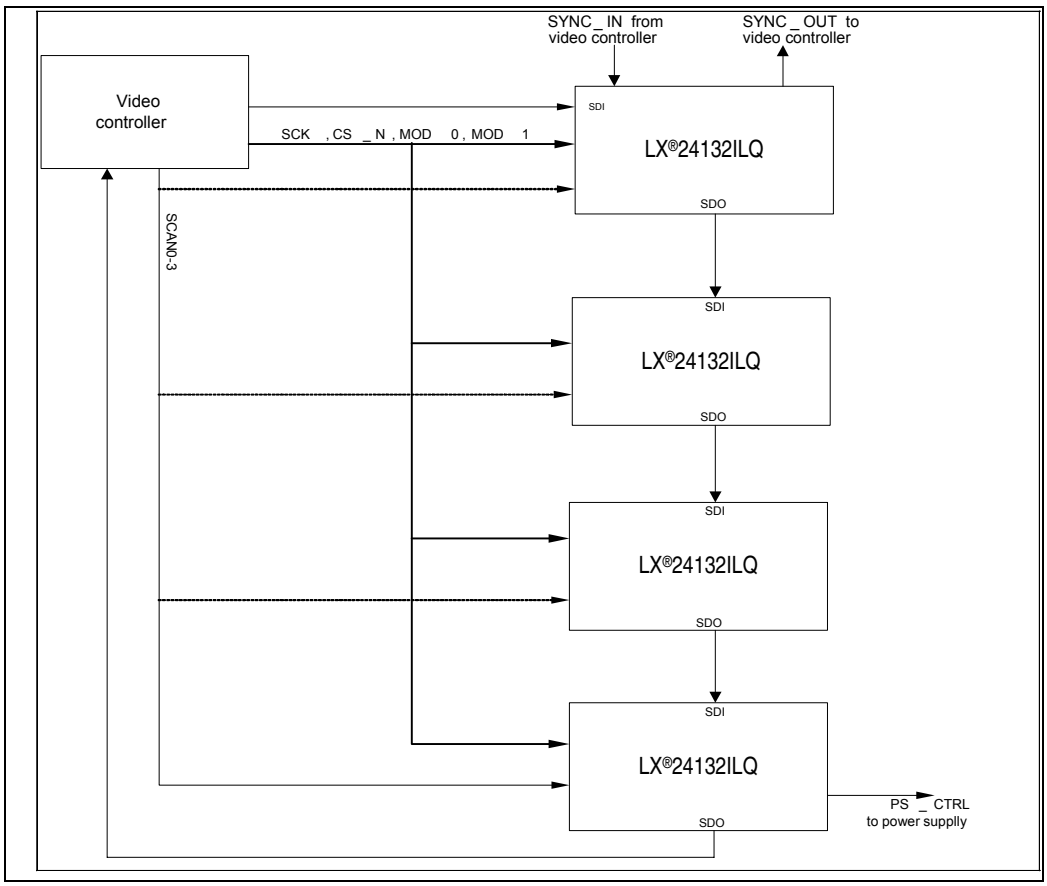


Figure 2: Typical Application with Four LED Controllers

APPLICABLE DOCUMENTS

- LX®23108ILQ 8 Port LED Drivers Datasheet, Catalogue Number 06-0074-058
- LX®24132ILQ /LX®23108ILQ AN-182, Designing a Low Current LED BackLight Driver System, Catalogue Number 06-0077-080

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (VCC, VDD)	-0.5 to 4.5 VDC
All Other Pins	-0.5 VDC to VCC+0.3 up to 4.5 VDC
Operating Ambient Temperature Range	-40° to +85° C
Maximum Operating Junction Temperature	150° C
ESD Protection at All I/O pins	± 2 KV HBM
Storage Temperature Range	-65° to +150° C
Package Peak Temperature for Solder Reflow (40 seconds maximum exposure)	+260° C (+0, -5° C)

Notes: Exceeding these ratings could result in damage to the device. All voltages are with respect to Ground.

THERMAL DATA (POWER CONSUMPTION)

21°C/W, according to JESD51-7.
thermal resistance-junction to ambient
Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{jA})$.

Electrical Characteristics

Unless otherwise specified, the following specifications apply to the operating ambient temperature and the following test conditions: V_{DD} = V_{CC} = 3.3 VDC. Performance is guaranteed for 0° C ≤ T_J ≤ +110° C.

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX®24132ILQ LED CONTROLLER			UNITS
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Input voltage	V_{DD}, V_{CC}	*Note 1	3.0	3.3	3.6	VDC
Operating current	I_{DD}	From VDD power supply		3	5	mA
	I_{CC}	From VCC power supply		3.5	5	mA
DIGITAL INTERFACE						
Input logic high threshold	V_{IH}		2.2			VDC
Input logic low threshold	V_{IL}				0.8	VDC
Output high voltage	V_{OH}	I_{OH} = -1 mA	2.4			VDC
Output low voltage	V_{OL}	I_{OH} = 1 mA			0.4	VDC
SCK clock frequency	Fsck				32	MHz
SDI set up time to SCK	Tsu_sdi		5			nS
SDI hold time to SCK	Thld_sdi		5			nS
SDO prop delay from SCK	Tprop_sdo	20 pF capacitive load			12	nS
CS_N set up time to SCK	Tsu_cs		5			nS
CS_N hold time to SCK	Thld_cs		5			nS
Time between adjacent SPI transactions	Tadj_cs			37		Clocks
Time from deassertion of CS_N to 1st SCK rising edge	Tdel_sck		4			Clocks
MOD[1:0] set up time to CS	Tsu_mod		0			nS
MOD[1:0] hold time to CS	Thld_mod		0			nS
CLK frequency	Fclk	Duty cycle 40% - 60%	4		8.192	MHz
SYNC_IN pulse width	sync_in_pulse		3			Clocks
SYNC_OUT pulse width	sync_out_pulse	T_{SYNC_OUT} [CLK] = 320*(PWM_FRDIV+1)		320		Clocks
LED CURRENT CONTROL						
DAC resolution	Vref_err			8		bits
V_{REF} output accuracy error		1.25 VDC < VREF ≤ 2.5 VDC			± 1.43	%
		0.5 VDC < VREF < 1.25 VDC			± 2	%
	Vref	0.234 VDC < VREF < 0.5 VDC			± 5.26	%
V_{REF} output range				2.5		VDC
Note 1: During power up VDD should not precede VCC.						

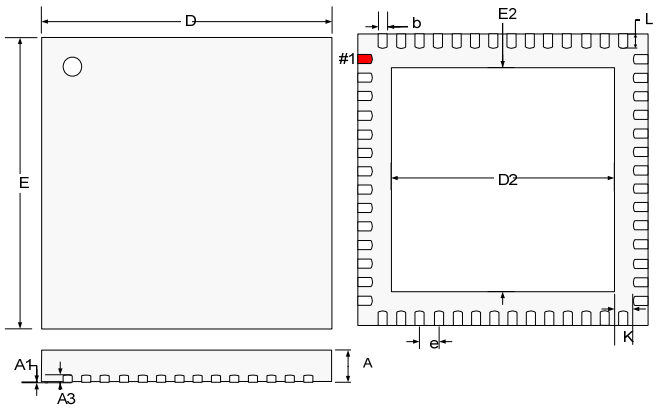
PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX®24132ILQ LED CONTROLLER			UNITS
			MIN.	TYP.	MAX.	
POR CELL						
POR threshold		High threshold	2.5	2.7	2.9	VDC
POR hysteresis			0.2	0.25	0.3	VDC
POR time delay		Power on reset activation pulse to all blocks.		0.6	1.2	mS
ADC						
Resolution				7		bits
LSB				15.6		mV
Offset error				1		LSB
Reading error		1 VDC ≤ Drain Voltage ≤ 2 VDC			± 3	LSB
Full scale ADC input				2		V
PWS CONTROL						
Duty-cycle resolution		At all system clock frequencies (fPWM)		12		bits
PWM frequency range		f_{PWM}[kHz] = f_{CLK}[kHz]/(4096x(PWM_FRDIV+1)) Refer to Table 1 for more details.	50		2K	Hz
SYSTEM PARAMETERS - PROTECTIONS						
Open LED detection		Open LED detection is digitally controlled and configurable by user (See *Application Note AN-182, Catalogue Number 06-0077-080*. Per Channel detection is traced when LED voltage is lower than the set "Open Drain Voltage Threshold".				
Short LED detection		At T_{AMB} = 25° C and V_{CC} = 5 VDC Short LED detection for the LX®23108LILQ FET Array is digitally controlled. Per channel detection is traced when LED voltage is higher than the "Short Drain Voltage Threshold".	8	8.8	10	VDC
Over-temperature detection		The LX®24132ILQ LED Controller has a reading mechanism which receives per channel over-temperature indications from the LX®23108LILQ LED Driver.	150	180	210	° C

Functional Pin Description

NAME	PIN #	DESCRIPTION
AGND	EPAD	Exposed PAD - Analog ground. A proper ground plane should be deployed around this pin wherever possible.
V_{CC}	33	Supply voltage for the internal analog circuit. A low ESR bypass capacitor (not less than 1 uF) should be placed as close as possible to this pin, using low impedance traces to AGND.
ATB_N ATB_P	35, 36	Production test output pins; do not connect.
SDI	2	Serial data input pin. The data from the SPI Host to this pin is clocked into the input shift register at the rising edge of the SCK clock. The MSB is inputted first.
SDO	15	Serial data output pin. The data from the input shift register is shifted out from this pin at the falling edge of the SCK clock. The MSB is outputted first. The SDO pin can be connected to the SDI pin of another device to form a cascaded SPI chain. Data from the LED controller can also be transmitted to the System Controller from this pin. If not used, leave this pin disconnected.
SCK	11	Clock signal for the SPI operation. A single clock shifts the data by one bit. It is only active when shifting data. This happens when CS_N is at 'low' level.
CS_N	12	Chip Select - SPI control signal input. The data shift starts when the CS falls from 'high' to 'low' and the data shifted into the input register is latched into the buffer registers at the rising edge of this signal.
SYNC_IN	13	Synchronization input. A new PWM cycle is started when a rising edge is received from this pin, regardless of the on-going PWM cycle's status. The PWM counter is reset to zero and the PWM comparator is reloaded if data is available. If not used, connect this pin to ground. **Note:** Minimum SYNC_IN positive pulse width should be less than two CLK pulses width.
SYNC_OUT	14	Synchronization output utilized for multi-chip applications. It synchronizes several LX®24132ILQ 32 Port Display Backlight LED Controller devices. It can also be utilized to synchronize the LCD frame timing through the Video Controller.
CLK	5	System clock - PWM control clock. This signal clocks the counting of the internal PWM counter and is also used for internal logic operations.
V_{DD}	8	Connects to the Core Logic and I/O supply rail. A ceramic 1 uF decoupling capacitor or greater should be connected from this pin to the DGND.
PWM0-31	55 to 40 31 to 16	PWM Gate control output signals used to command up to 4 x 8-channel LX23018LILQ LED Driver ICs
VDMEAS	34	MOSFET drain voltage sensing input. The external MOSFET drain voltage is sensed via this pin and used to control the external power supply, maintaining the optimum voltage for the LED strings.
FAULT_IN	39	Fault input signal coming from the LED Driver IC. It is asserted 'low' when fault event is detected at one of the LED strings.
PS_CTRL	1	Power supply control signal output. This Pulse Density Modulation signal (PDM) is used to interface to the power supply, adjusting the DC voltage of the LED strings to the optimum level.
MOD0	3	An input signal; used for production only. Should be connected to GND
MOD1	4	An input signal; selects between Configuration (VDD) mode and Operation (GND) mode.
SCAN0-3	6, 7, 9, 10	Input logic signals utilized for scanning zone selection.
VZAP	38	Zapping input for IC production trimming; must be tied to VCC.
VREF	37	Analog reference output signal used for the 8-channel LED Drivers.
PSEL_SIG	56	Channel selection serial output signal to LX®23108LILQ which is a 32 bits packet, used to select (for monitoring) one of the 32 strings drain voltages and thermal sensors signals.
PSEL_CLK	32	Channel selection serial clock signal. Each single clock shifts the internal register data of the LX®23108LILQ by one bit, allowing the monitoring of the next channel.

Package Information

LQ **56-Pin 8x8mm QFN**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.00	6.25	0.236	0.246
E2	6.00	6.25	0.236	0.246
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

LX24132ILQ Principle of Operation

The LX®24132ILQ 32 Port Display Backlight LED Controller is designed to drive up to 32 LED strings and control external power supplies to regulate the LED current. The interface with the Hosting system (Video Processor / FPGA / CPU) is accomplished via a standard SPI bus. LED current and PWM dimming duty-cycle commands are received from the Hosting system in a digital format and executed by the internal circuitry to obtain the desired BackLight control. In addition, the device provides a power supply control signal (PS_CTRL) used to control the external power supply and trim it to the optimum level. This minimizes system power dissipation, while maintaining accurate current regulation for each of the 32 LED strings.

Block Diagram

Figure 3 shows the LX®24132ILQ LED 32 Port Display Backlight LED Controller block diagram, describing its main functions. The SPI block implements the communication with the external Controller. The power supply control circuitry adjusts the LED strings' main voltage by utilizing the PDM method (Pulse Density Modulation). The scanning control circuitry includes the required logic needed to perform the zone selection.

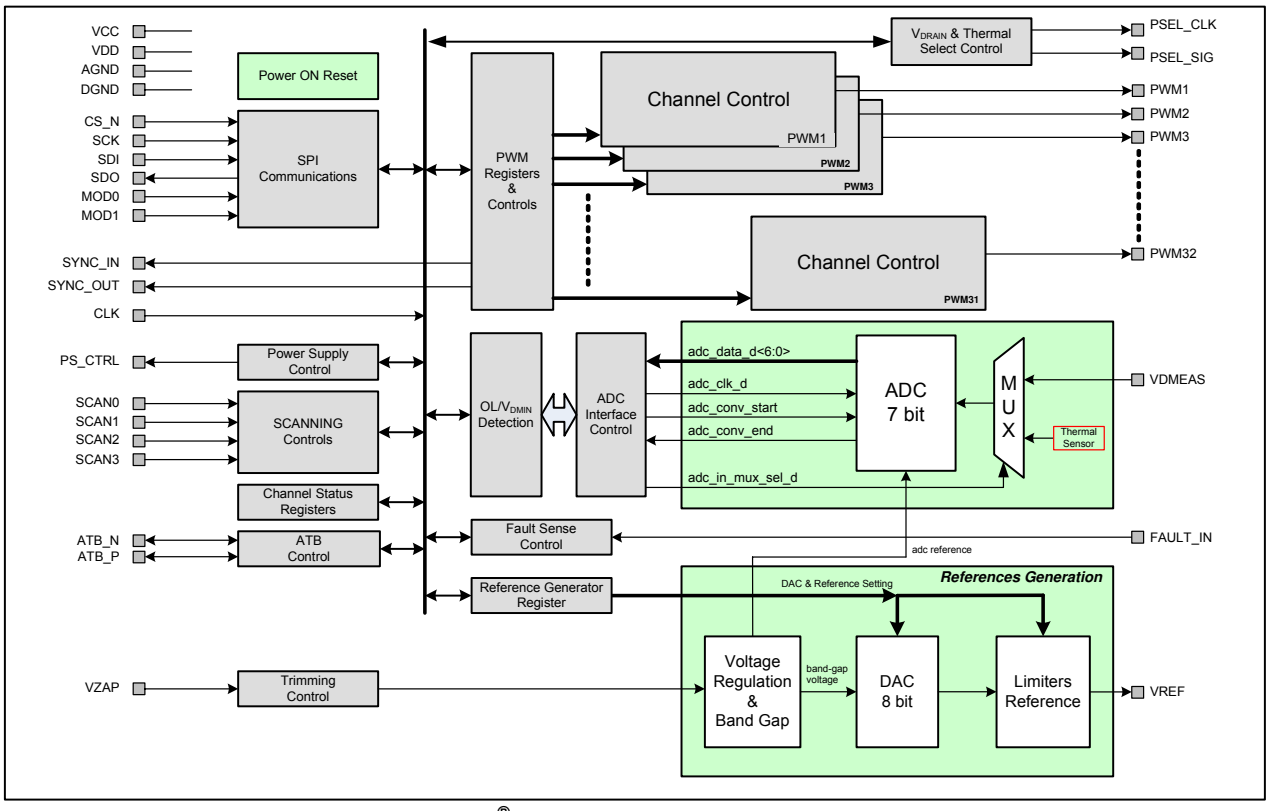


Figure 3: LX®24132ILQ: Detailed Block Diagram

The Channel Status Registers are used to enable/disable channels and indicate their status (thermal event, under-load, etc.). The ATB Control block is used for testing purposes. The PWM registers and control signals establish the PWM parameters common to all channels. Each Channel Control block generates PWM command signals individually. The OL/VDMIN Detection block controls the search for open strings and a valid VDMIN. An ADC Interface Control block selects (for monitoring) the required channel voltages and the internal thermal sensor. The Fault Sense Control circuitry detects thermal and load short-circuit events at the associated LX®23108LILQ devices.

The Reference Generator register in conjunction with the Reference Generation block produce an accurate output voltage used to set the string currents. The VDRAIN & Thermal Select Control instruct the LX®23108LILQ as which channel is to be monitored. The Trimming Control is used for production purposes.

Slave SPI Interface

The SPI interface consists of four signal lines: SDI, SDO, SCK, and CS_N (see Figure 4).

- **SDI**: Serial data input to the LX®24132ILQ
- **SDO**: Serial data output from the LX®24132ILQ
- **SCK**: Serial data clock input
- **CS_N**: Serial data chip select

The SDI signal is sampled at the rising edge of the SCK, while the SDO is driven at the falling edge of the SDK, where the MSB is shifted out first.

SPI data transmission/reception should be executed, starting from bit 415 to bit 0 (Operation mode), or starting from bit 223 to bit 0 (Configuration mode) Figure 5 shows the SPI timing diagram for a 4-driver configuration. The SPI data of the fourth LX®24132ILQ is transmitted first, following the SPI data of the third, second and then the first LX®24132ILQ.

SPI Noise Immunity

The LX®24132ILQ SPI interface includes special noise immunity protection mechanisms, which improve the electrical SPI interface immunity against high frequencies noise, short spikes and glitches in a noisy PCB environment. These mechanisms include:

- Filter short glitches and spikes of SPI CS_N signal
- If SPI CS_N chip select signal is Set Low for less than 2 x System Clocks, this pulse is ignored, the transaction is canceled and the internal registers remains unchanged.

Ignore the SPI transaction if the number of SPI SCK clocks is not module 8 (8, 16, 24, 32, etc.); in this case the internal registers remains unchanged.

SPI Timing

Figure 4 describes LX®24132ILQ SPI timing (refer to Electrical Characteristics for timing values).

In addition to various SPI timing values, the first SCK SPI rising edge should occur Tdel_sck (four system clocks) after CS_N SPI chip select negation. Minimum time between the end of SPI transaction to the start of the next SPI transaction should be Tadj_cs (37 system clocks). Refer to Electrical Characteristics, page 5 for more details.

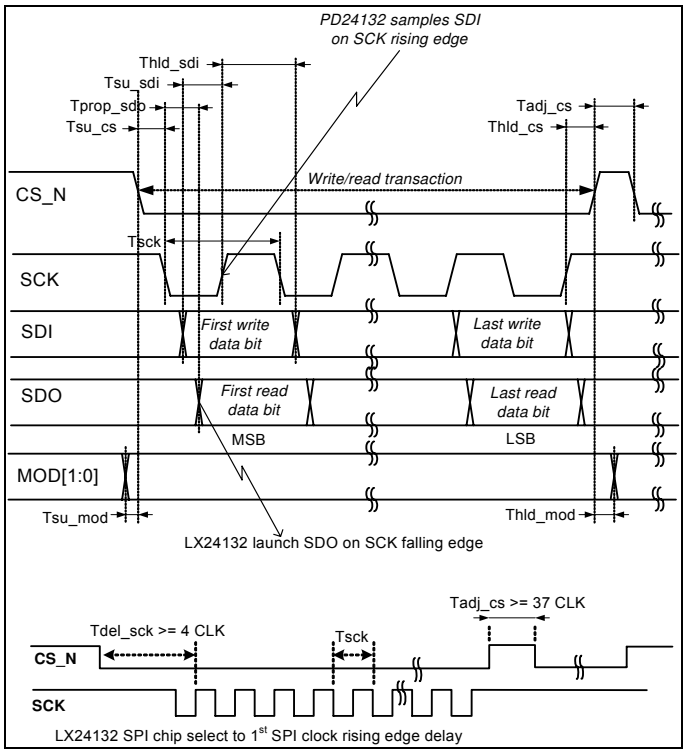


Figure 4: SPI Signals Diagrams

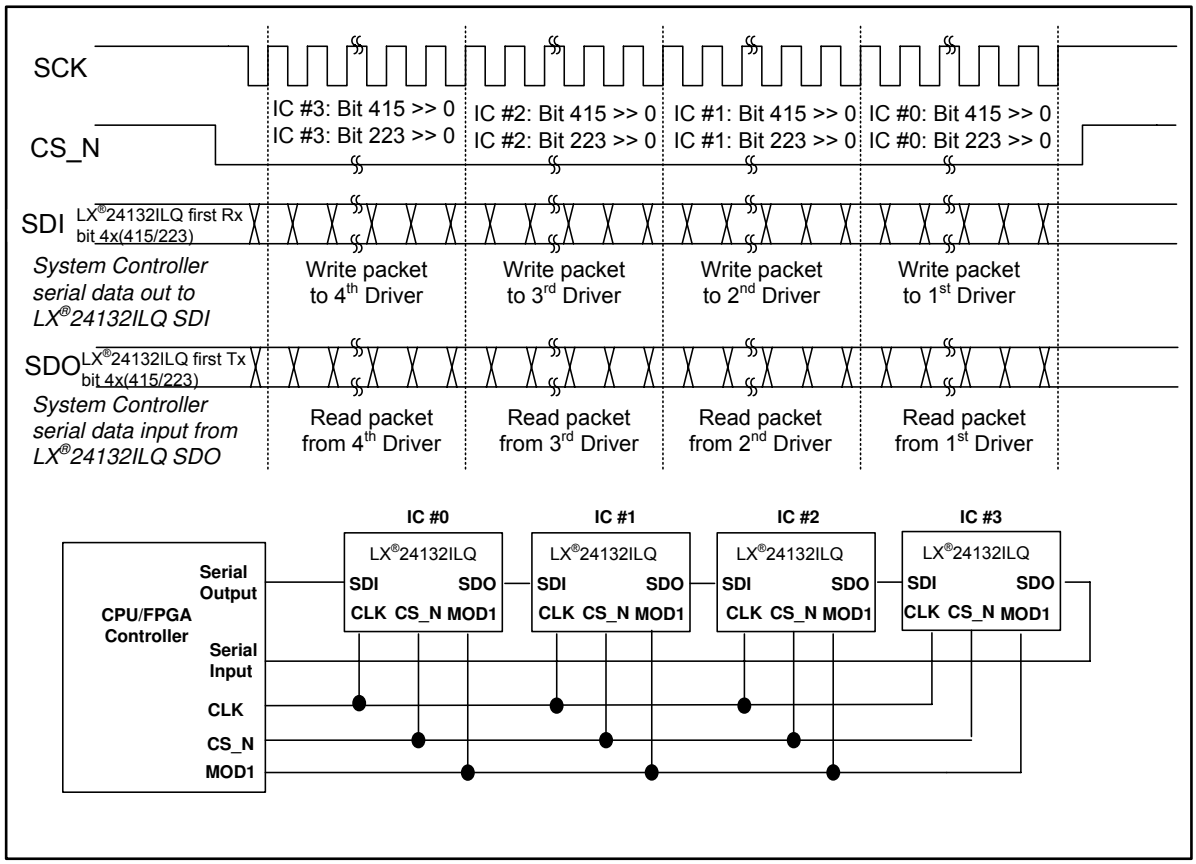


Figure 5: SPI Signals Diagram for a Four LED Controllers Configuration

Communication Modes

Chip configuration and monitoring is accomplished by sending and receiving a series of bits over the SPI.

There are two communication modes:

- Operation mode (MOD1 input pin = Low)
- Configuration mode (MOD1 input pin = High)

COMMUNICATION MODE	MOD1 INPUT PIN
Operation Mode	GND
Configuration Mode	VDD

Operation mode: Bit pattern involves reading and writing registers accessed periodically, providing LED PWM pulse width and more.

Configuration mode: Bit pattern involves reading and writing registers that are usually configured only once, for example PWM_FRDIV (crystal frequency divider) register etc.

Figure 6 and Figure 7 illustrate the read/write registers involved in each SPI bit stream for operation and configuration mode.

For multiple chip applications, the SPI communication should be cascaded (see Figure 5).

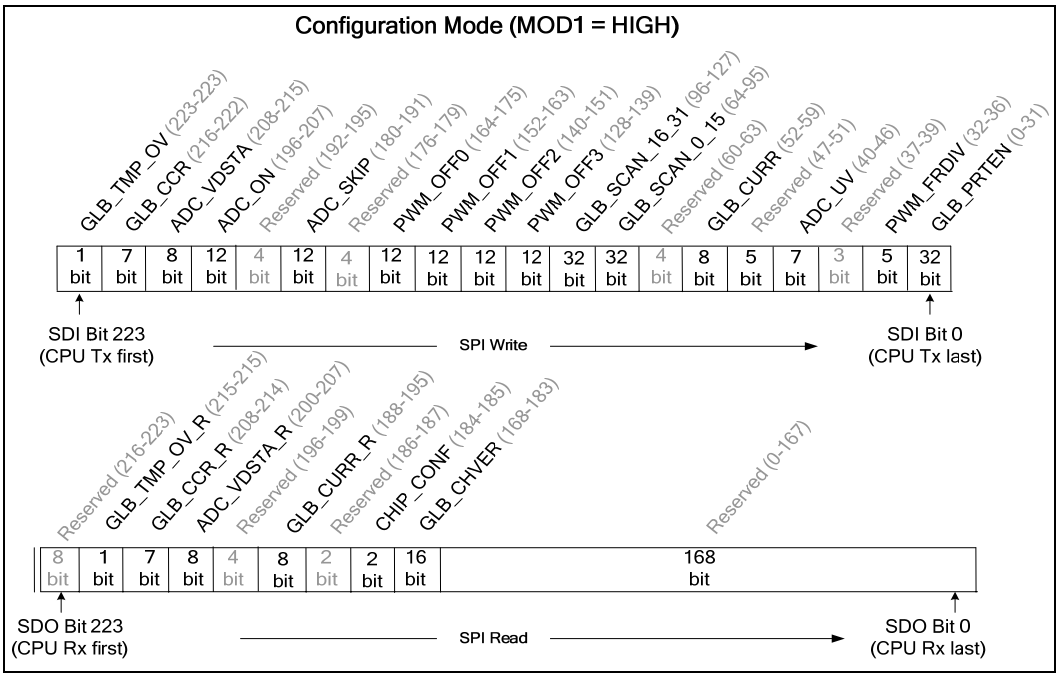


Figure 6: Configuration Mode SPI Bit Stream

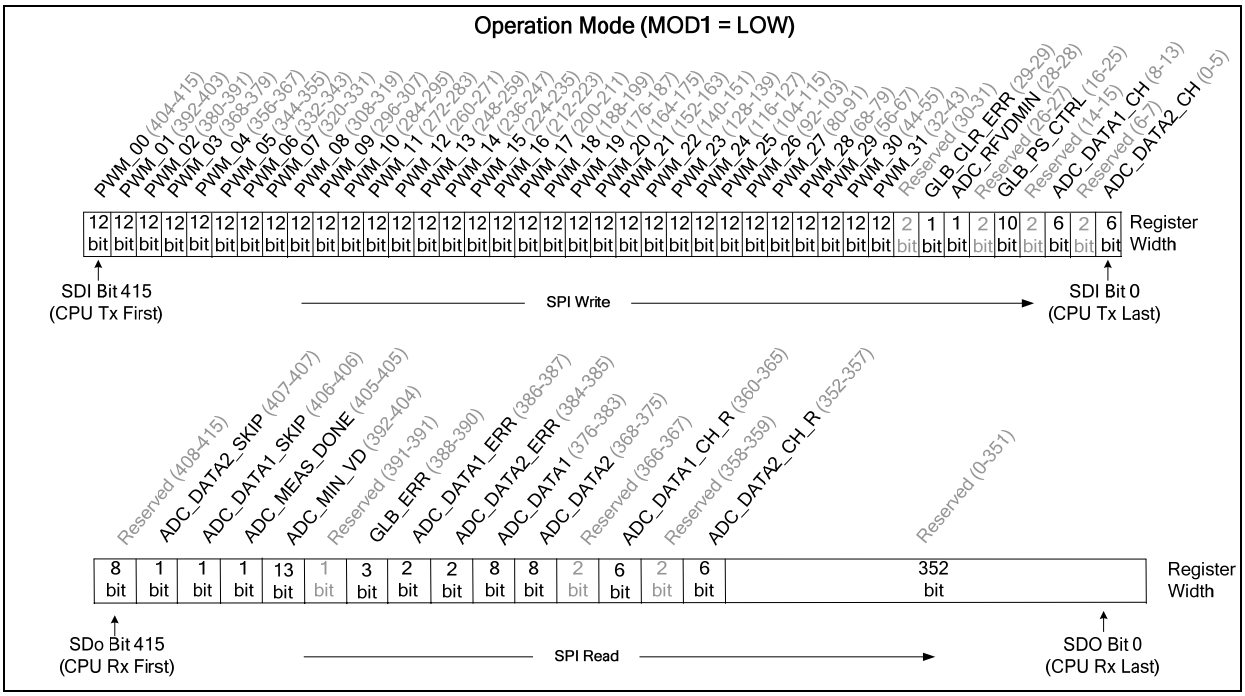


Figure 7: Operation Mode SPI bit Stream

PWM Control Input Pin: SYNC_IN

The SYNC_IN input signal determines if the PWM output will be synchronized with the SYNC_IN input clock.

Clearing GLB_CCR register/ bit1 resets the internal 12 bit PWM counter (clocked via the CLK pin divided by PWM_FRDIV+1 register) to zero on each SYNC_IN rising clock.

The counter continues to increment up to '4095' and restarts from '0' again, unless another SYNC_IN pulse resets the counter before reaching '4095'.

PWM Control Input Pins: SCAN0-3

SCAN0-3 input signals (Figure 8), together with the GLB_CCR bit0 register, control the PWM output signals.

SCAN0-3 input pins can be used to enable/disable PWM output signals.

Lowering the SCAN0-3 input enforces PWM[N] output pins to 'Low' (no current through the LEDs). Restoring the SCAN0-3 input to 'High' re-enables the PWM[N] output generation.

Note that only PWM channels linked by the GLB_SCAN0_15 and the GLB_SCAN16_31 to this specific SCAN[N] input pin will be affected.

The GLB_CCR bit0 determines the way that the SCAN[N] input affects the PWM[N] outputs. Setting Bit0 to '0' synchronizes the SCAN[N] input with the internal 12 bit PWM counter, preventing partial PWM output pulses.

However, setting Bit0 to '1' causes SCAN[N] input to perform binary AND function with the PWM[N] output signal, which consequently may generate partial PWM output pulses (see Figure 8).

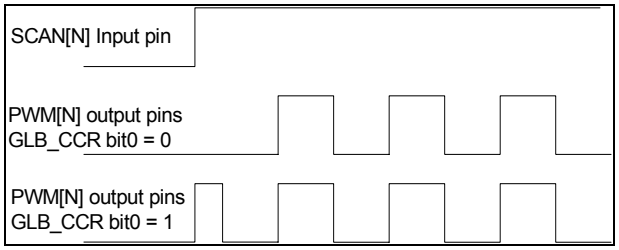


Figure 8: SCAN Input Operation

PWM Output Pins PWM0-PWM31

PWM output generation (see Figure 9) is based on:

- Internal 12-bit PWM counter clocked via the CLK pin divided by PWM_FRDIV+1 register,
- PWM_00-PWM_31 registers controlling the duty cycle of each PWM[N] channel
- Four PWM_OFF0 – PWM_OFF3 registers controlling the PWM off timing (stop LED current).

12 bit internal PWM counter counts from 0-4095, repeatedly, unless SYNC_IN input pulse resets the counter to zero on each SYNC_IN rising edge.

PWM_[N] registers modification is performed by sending new SPI Operation mode bit pattern with various PWM values. Since PWM_[N] is double buffered, new SPI Operation mode PWM_[N] values are written to the first buffer on the SPI CS rising edge and are loaded into the second buffer on the PWM_OFF timing of each string. The new PWM value is effective on the next PWM cycle.

GLB_SCAN_0_15 and GLB_SCAN_16_31 registers link each PWM[N] channel (two bit per PWM channel) to one out of four PWM_OFF[N] registers. Whenever an internal 12 bit PWM counter value matches any of the PWM_OFF0, PWM_OFF1, PWM_OFF2 or PWM_OFF3 registers, all the PWM[N] channels which were linked by the GLB_SCAN_0_15 and GLB_SCAN_16_31 registers to this specific PWM_OFF[N] register are turned off (stop LED current).

PWM00_PWM31 registers control PWM[N] channel duty cycle. Figure 9 shows an example where PWM0 output pin is configured to use PWM_OFF0 (GLB_SCAN_0_15 bit 0&1 = 0).

The PWM_OFF0 register is set to 3000 and PWM_00 register duty cycle is set to 500. Whenever the 12 bit internal counter reaches 2500 (3000 - 500), PWM0 output pin toggles to High and turns to Low whenever the 12 bit internal PWM counter reaches 500 ticks higher (3000).

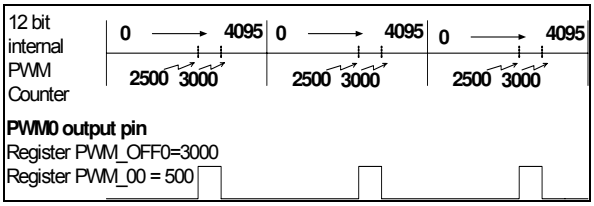


Figure 9: PWM operation

Power Supply Control

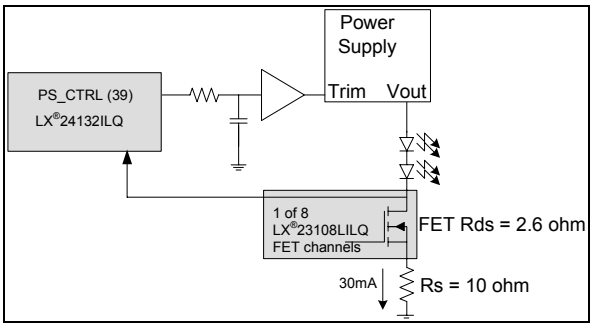


Figure 10: Simplified Power Supply Control Loop

Setting the ADC_RFVDMIN register to '1' causes the LX®24132ILQ 32 Port Display Backlight LED Controller to search for the channel with the lowest FET Vdrain ADC reading. When the searching process ends the LX®24132ILQ sets bit 0 in the ADC_MEAS_DONE register. The CPU/FPGA/Video Controller manages the LX®24132ILQ that reads the ADC_MIN_VD register (reports channel number and

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lowest FET Vdrain ADC reading). As shown in Figure 10, the current is 30 mA. Minimum FET Vdrain should be at least:

- 30 mA x (10 Ohm + 2.6 Ohm) = 0.378 Volt
- 10 Ohm = FET external sense resistor
- 2.6 Ohm = LX®23108LILQ FET rds resistance

The ADC_MIN_VD register reading can be converted to voltage by:

$$\text{Min FET Vdrain[v]} = \frac{2\text{ V}}{128} \times \text{ADC\_MIN\_VD[0-6]}$$

The Controller increases the power supply voltage when the minimum FET Vdrain is too low and decreases it in cases where minimum FET Vdrain is too high.

Power supply trimming is implemented by writing to the GLB_PS_CTRL register (10 bit DAC) which uses a PDM system to generate an equally distributed number of pulses proportional to the GLB_PS_CTRL value. Each pulse's duration equals to a single CLK clock length.

After low pass filtering, the PS_CTRL output DC component is used to trim the LED power supply (see AN-182 for more details).

ADC_UV register: Prevents very low ADC readings from being part of the minimum FET Vdrain search algorithm (reported by the ADC_MIN_VD register).

Any FET Vdrain ADC reading lower than ADC_UV register's value is not compared with the ADC_MIN_VD register. By setting ADC_UV to typical value such as '3':

[2000 mV/128] x 3 = 47 mV

This value enforces the ADC_MIN_VD register to reject any ADC reading bellow 47 mV. This protection mechanism is required when the disconnected channel is enabled, or one of the LEDs had failed and was disconnected.

Internal A/D Operation

The internal ADC of the LX®24132ILQ 32 Port Display Backlight LED Controller measures the voltage on the VDMEAS input pin, which connects to the LX®23108ILQ 8 Port LED Drivers VDMEAS output pin. The LX®24132ILQ determines which FET vd voltage of the LX®23108ILQ is multiplexed to the VDMEAS input pin for FET vdrain measurement. ADC_SKIP, ADC_VDSTA and ADC_ON registers control the internal ADC operation (see Figure 11).

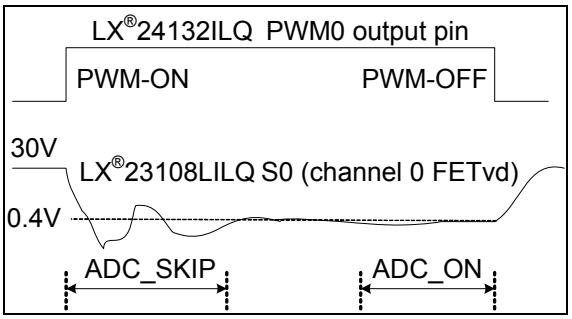

Figure 11: ADC Operation

The LX®24132ILQ contains two additional ADCs used by the system controller which manages the LX®24132ILQ. The ADCs can be configured to measure any of the 32 PWM channels FET Vdrain voltages, report under-voltage, over-voltage and skip an individual PWM channel.

ADC_SKIP register: Determines the time in which no FET Vdrain measurements are taken (starting from PWM-ON). This is done to prevent incorrect FET Vdrain measurements during the period of time where FET Vdrain is unstable. Typical ADC_SKIP value should be around 100 µsec (see Figure 11).

$$\text{ADC\_SKIP} = \frac{\text{CLK[KHz]} \times t_{adc\_skip}\text{[uSec]}}{1000 \times (\text{PWM\_FRDIV}+1)}$$

ADC_ON register: Controls the allocated time for the A/D system to measure FET Vdrain of the various channels. If only some channels were measured, unmeasured channels are measured on the next PWM cycle (see Figure 11).

A typical ADC channel measurement takes around 6 µsec, assuming that the ADC_VDSTA register is set to 5 µsec and CLK input pin is connected to an 8 MHz clock source.

ADC measurements are conducted by the state machine from channel #0 to channel #31. In cases where a channel is temporarily turned off (due to scan input pin, or phase shift), ADC measurements are not performed although there is enough time for such measurements.

The measurements continue only after the channel will be turn on.

$$\text{ADC\_ON} = \frac{\text{CLK[KHz]} \times t_{adc\_on}\text{[uSec]}}{1000 \times (\text{PWM\_FRDIV}+1)}$$

The LX®24132ILQ 32 Port Display Backlight LED Controller can measure PWM as low as ADC_SKIP+ADC_ON. For example, assuming ADC_SKIP = 150 µsec, ADC_ON = 50 µsec and

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PWM frequency = 120 Hz. The minimum duty cycle which can be measured is:

$$\left[\frac{150\,e^{-6} + 50\,e^{-6}}{\frac{1}{120}}\right] \times 100\% = 2.4\%$$

Lower PWM duty cycle can be generated by the LX®24132ILQ. However, the internal ADC will not be able to read FET Vdrain voltage for channels with lower PWM duty cycle.

Note: The LX®24132ILQ 32 Port Display Backlight LED Controller sets skip_error bit2 in the GLB_ERR register in cases where it was not able to measure FET Vdrain, due to low PWM duty cycle.

Single ADC conversion takes around 6 µsec (assuming that the ADC_VDSTA register was set to 5 µsec). It takes 192 µsec (6 µsec x 32) to complete all 32 channels' FET Vdrain reading. Setting ADC_ON to 50 µSec requires four PWM cycles (8.3 mSec x 4 = 33.2 mSec for 120 Hz PWM cycle) to complete all 32 channels FET Vdrain reading.

Increasing the ADC_ON decreases the time required by the LX®24132ILQ to sample all 32 FET Vdrain channels, but increases the minimum FET Vdrain readable PWM duty cycle.

ADC_VDSTA register controls the analog mux delay during LX®23108LILQ channel change, before stable FET Vdrain measurement can be performed. LX®23108LILQ analog mux delay should be set to 5 µsec.

$$\text{ADC\_VDSTA} = \frac{\text{CLK[KHz]} \times 5\ \text{uSec}}{1000}$$

An additional 1 µSec is required for ADC conversion; therefore it takes around 6 µSec to measure a single FET Vdrain channel.

Current Setting

Current setting is done by GLB_CURR register.

$$\text{GLB\_CURR} = 0.7168 \times I[\text{mA}] \times Rs[\text{ohm}]$$

Rs = sense resistor connected to the LX®23108ILQ/ S[N] pin.

Fault Detection

Fault events are reported by the GLB_ERR register. Three types of errors and events are reported by bits 0 - 2.

Bit0: under_voltage: Will be set whenever one or more out of 32 channels FET Vdrain voltage value is/are below the ADC_UV register's value. A typical scenario is where a LED is disconnected, or the LX®24132ILQ's unconnected channel is enabled by the GLB_PRTEN register.

Note: Setting bit0 in the GLB_CLR_ERR register to '1' clears this error bit.

Bit1: over_temp_over_volt: Will be set whenever FET Vdrain exceeds 7.5 VDC - 11.5 VDC. A typical scenario is whenever a LED becomes shorted, or LED power supply was trimmed to too high voltage.

Note: Setting bit0 in the GLB_CLR_ERR register's to '1' clears this bit.

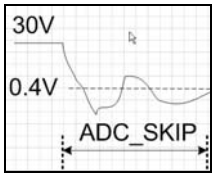
Bit2: skip: Will be set in cases where at least one out of the 32 channels is not measured by the internal ADC due to low PWM duty cycle.

Note: This bit clears itself whenever the LX®24132ILQ measures all 32 channels with no need to skip channels with a very low duty cycle.

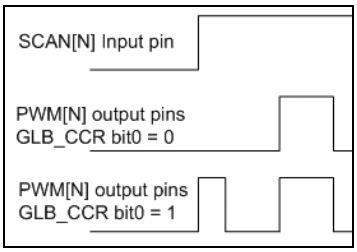
Table 1: Configuration Mode Write Registers Description (For complete SPI bits pattern, see Figure 6)

CONFIGURATION MODE WRITE REGISTERS				
REGISTER NAME	**DESCRIPTION**	**SPI - BIT**	**LENGTH**	**RESET VALUE**
		POSITION	**[BITS]**	
GLB_PRTEN	Bit0 - 31: Enable/Disable PWM channels pulse generation on PWM[N] output pins. Bit[N] 0: PWM[N] output pin is disabled Bit[N] 1: PWM[N] output pin is enabled N = 0 - 31 **Note**: Unused channels should be disabled Field is write only	0 - 31	32	0x0000
PWM_FRDIV	Divide system clock (pin 5) which drives the internal 12 bit PWM counter by: PWM_FRDIV+1. 0: Divide by 1 31: Divide by 32 $\text{PWM Frequency} = \frac{\text{CLK}}{(4096 \times (\text{PWM\_FRDIV}+1)}$ Example: For a system clock of 7.86432 MHz and PWM_FRDIV set to 15 (divide by 16), PWM frequency is 120 Hz. Field is write only	32 - 36	5	0x0F
	Reserved	37 - 39	3	
ADC_UV	Any LX®23108ILQ FET Vdrain ADC measurement during PWM-ON below ADC_UV will be ignored by internal logic responsible to find PWM 0-31 string with the lowest FET Vdrain ADC reading. 0: 0 Volt 127: 2 Volt Typical ADC_UV value should be 3 (47 mVolt) **Note**: If the FET Vdrain measurement in one channel is below the ADC_UV, GLB_ERR register bit0 is set to '1' Field is read-write	40 - 46	7	0x07
	Reserved	47 - 51	5	
GLB_CURR	Bit0-7 control LED current in all PWM channels. GLB_CURR = 0.7168 x I[mA] x Rs[ohm] Rs = LX®23108ILQ sense resistor connected to pin S[0-7] Field is read-write	52 - 59	8	0x80
	Reserved	60 - 63	4	

<table>
<tr><th colspan="5">CONFIGURATION MODE WRITE REGISTERS</th></tr>
<tr><th>REGISTER NAME</th><th>DESCRIPTION</th><th>SPI - BIT POSITION</th><th>LENGTH [BITS]</th><th>RESET VALUE</th></tr>
<tr><td>GLB_SCAN_0_15</td><td>Each two bits associate their channel to one of the SCAN0-SCAN3 input pins and one of PWM_OFF0 - PWM_OFF3 registers. Setting SCANx input signal to Low, forces all PWM channels assigned to same input SCANx pin to turn off. Restoring SCANx input signal to High restores all assigned channels to normal operation.
Example: Setting GLB_SCAN_0_15 register bit0 = High, Bit1 = High, assign SCAN3 input signal to control PWM channel 0, as well as assigning PWM_OFF3 register to control the turn off timing of PWM channel 0 (used for PWM phase shift).
Field is read-write
<table>
<tr><th>Bit 2*N+1 (N = channel)</th><th>Bit 2*N (N = channel)</th><th>SCANx Input pin</th><th>PWM_OFFx Register</th></tr>
<tr><td>0</td><td>0</td><td>SCAN0</td><td>PWM_OFF0</td></tr>
<tr><td>0</td><td>1</td><td>SCAN1</td><td>PWM_OFF1</td></tr>
<tr><td>1</td><td>0</td><td>SCAN2</td><td>PWM_OFF2</td></tr>
<tr><td>1</td><td>1</td><td>SCAN3</td><td>PWM_OFF3</td></tr>
</table>
Note: View GLB_CCR register related to the scanning mode and PWM synchronization.
<table>
<tr><td>Bit0-1: PWM Channel [0]</td><td>Bit16-17: PWM Channel [8]</td></tr>
<tr><td>Bit2-3: PWM Channel [1]</td><td>Bit18-19: PWM Channel [9]</td></tr>
<tr><td>Bit4-5: PWM Channel [2]</td><td>Bit20-21: PWM Channel [10]</td></tr>
<tr><td>Bit6-7: PWM Channel [3]</td><td>Bit22-23: PWM Channel [11]</td></tr>
<tr><td>Bit8-9: PWM Channel [4]</td><td>Bit24-25: PWM Channel [12]</td></tr>
<tr><td>Bit10-11: PWM Channel [5]</td><td>Bit26-27: PWM Channel [13]</td></tr>
<tr><td>Bit12-13: PWM Channel [6]</td><td>Bit28-29: PWM Channel [14]</td></tr>
<tr><td>Bit14-15: PWM Channel [7]</td><td>Bit30-31: PWM Channel [15]</td></tr>
</table></td><td>64 - 95</td><td>32</td><td>Not defined</td></tr>
<tr><td>GLB_SCAN_16_31</td><td>Same as GLB_SCAN_0_15 for PWM channels 16-31.
Field is read-write
<table>
<tr><td>Bit0-1: PWM[16]</td><td>Bit16-17: PWM[24]</td></tr>
<tr><td>Bit2-3: PWM[17]</td><td>Bit18-19: PWM[25]</td></tr>
<tr><td>Bit4-5: PWM[18]</td><td>Bit20-21: PWM[26]</td></tr>
<tr><td>Bit6-7: PWM[19]</td><td>Bit22-23: PWM[27]</td></tr>
<tr><td>Bit8-9: PWM[20]</td><td>Bit24-25: PWM[28]</td></tr>
<tr><td>Bit10-11: PWM[21]</td><td>Bit26-27: PWM[29]</td></tr>
<tr><td>Bit12-13: PWM[22]</td><td>Bit28-29: PWM[30]</td></tr>
<tr><td>Bit14-15: PWM[23]</td><td>Bit30-31: PWM[31]</td></tr>
</table></td><td>96 - 127</td><td>32</td><td>Not defined</td></tr>
</table>

CONFIGURATION MODE WRITE REGISTERS				
REGISTER NAME	**DESCRIPTION**	**SPI - BIT**	**LENGTH**	**RESET VALUE**
		POSITION	**[BITS]**	
PWM_OFF3	All PWM channels which were assigned by the GLB_SCAN_0_15 and GLB_SCAN_16_31 register to PWM_OFF3 will be turned off each time 0-4095 internal cyclic counter reaches the PWM_OFF3 register value; see Figure 9. **Value** / **Phase Shift** 0 / 0% 2048 / 50% 4095 / 99.99% Note that the 0-4095 internal counter increments at a rate of sys clock/ (PWM_FRDIV+1) Use this register to perform PWM phase shift; see Figure 9. Field is write only	128 - 139	12	Not defined
PWM_OFF2	Same as PWM_OFF3 for all PWM channels which were assigned to use PWM_OFF2. See Figure 9.	140 - 151	12	Not defined
PWM_OFF1	Same as PWM_OFF3 for all PWM channels which were assigned to use PWM_OFF1. See Figure 9.	152 - 163	12	Not defined
PWM_OFF0	Same as PWM_OFF3 for all PWM channels which were assigned to use PWM_OFF0. See Figure 9.	164 - 175	12	Not defined
	Reserved	176 - 179	4	
ADC_SKIP	Prevents internal ADC from measuring FET Vdrain as long as FET Vdrain voltage is unstable. Delay is required to ensure stable ADC Vdrain measurement. Typical value should be around 100 µsec. For the best recommended value, contact Microsemi's technical support. See Figure 11. Field is write only  $ADC\_SKIP = \frac{CLK[KHz] \times t_{adc\_skip}[uSec]}{1000 \times (PWM\_FRDIV+1)}$	180 - 191	12	0x011
	Reserved	192 - 195	4	

CONFIGURATION MODE WRITE REGISTERS				
REGISTER NAME	**DESCRIPTION**	**SPI - BIT POSITION**	**LENGTH [BITS]**	**RESET VALUE**
ADC_ON	Allocated time for internal ADC to sample the 32 PWM channels. In cases where ADC cannot measure all 32 channels during a single PWM pulse, it continues channel measurement on the next PWM cycle. ADC_ON time is measured from the end of the PWM pulse. See Figure 11. For the best recommended value, contact Microsemi's technical support. $ADC\_ON = \frac{CLK[KHz] \times t_{adc\_on}[uSec]}{1000 \times (PWM\_FRDIV+1)}$ **Note: Minimum ADC_ON is 6µsec** Field is write only	196 - 207	12	0x003
ADC_VDSTA	The time required for the LX®23108LILQ internal mux to stabilize before the LX®24132ILQ 32 Port Display Backlight LED Controller can measure the FET Vdrain voltage. Stabilization time = 5 µsec. $ADC\_VDSTA = \frac{CLK[KHz] \times 5uSec}{1000}$ Example: LX®24132ILQ CLK frequency = 7864 KHz. ADC_VDSTA = (7864 x 5)/1000 = 39 Field is read-write	208 - 215	8	0x28

CONFIGURATION MODE WRITE REGISTERS				
REGISTER NAME	**DESCRIPTION**	**SPI - BIT**	**LENGTH**	**RESET VALUE**
		POSITION	**[BITS]**	
GLB_CCR	**Bit 0: Scanning_Mode**: Synchronization control of PWM outputs to SCAN0-SCAN3 input pins and PWM cycle.  0: PWM output is synchronized with the SCANx input pin and internal PWM cycle, see above figure. 1: PWM output follows SCANx input SIGNAL asynchronously in respect to internal PWM cycle, see above figure. This bit is read-write. **Bit 1: sync_in_dis:** Disables PWM output synchronization with SYNC_IN input pin. 0: PWM[N] output pins are synchronized with SYNC_IN signal. 12 bit internal PWM counter will be reset on each SYNC_IN rising edge pulse. 1: SYNC_IN input pin has no effect on PWM outputs. This bit is read-write. **Bit 2: sleep_mode:** Switch off analog and partial digital sections of the chip for power saving purposes. 0: Normal operation 1: Switch off analog and partial digital chip sections. This bit is read-write. **Bit 3: sync_out_disable:** Enable/Disable pulse at SYNC_OUT output pin each time internal PWM counter reaches "0". 0: Enable sync_out. Set Bit4 & bit5 to 00 1: SYNC_OUT output pin = Low. This bit is read-write. **Bit 4&5: sync_out_func:** For internal use. Set bits 4 and 5 to Low. These bits are write only.Read value always 0. **Bit 6: read_mode:** 0: For internal use. Set to Low. This bit is write only. Read value always 0.	216 - 222	7	0x00

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CONFIGURATION MODE WRITE REGISTERS				
REGISTER NAME	DESCRIPTION	SPI - BIT POSITION	LENGTH [BITS]	RESET VALUE
GLB_TMP_OV	Enable/Disable LX®23108ILQ internal FET Vdrain over-voltage and over-temperature protection. **0: Enabled** **Over Voltage**: LX®23108ILQ 8 Port LED Drivers turns off PWM channels whenever FET Vdrain voltage exceeds 7.5 VDC -11.5 VDC. To re-enable turned off channels, the user should set bit0 in the GLB_CLR_ERR register. **Over Temperature**: LX®23108ILQ turns off PWM channels whenever FET temperature exceeds 180 +/- 20[c]. To re-enable turned off channels, the user should set bit0 in register GLB_CLR_ERR. **1: Disabled** **Over Voltage**: LX®23108ILQ FTE Vd over-voltage protection is disabled. **Over Temperature**: LX®23108ILQ turns off PWM channels whenever FET temperature exceeds 180 +/- 20[c]. However, PWM channels are automatically re-enabled whenever FET cools down. **Note**: Setting bit0 in GLB_CLR_ERR register re-enables PWM channels, regardless of FET temperature. However, if FET temperature is too high, FET channels are turned off again. This field is read-write.	223	1	0x1

Table 2: Configuration Mode Read Registers Description (For complete SPI bits pattern, see Figure 6)

CONFIGURATION MODE READ REGISTERS				
REGISTER NAME	DESCRIPTION	SPI - BIT POSITION	LENGTH [BITS]	RESET VALUE
	Reserved	0 - 167	168	
GLB_CHVER	Chip version; for internal use	168 - 183	16	0x180
CHIP_CONF	Chip sub version; for internal use	184 - 185	2	0x0
	Reserved	186 - 187	2	
GLB_CURR_R	Reports same value as written to GLB_CURR register (bits 52-59).	188 - 195	8	0x80
	Reserved	196 - 199	4	
ADC_VDSTA_R	Reports same value as written to ADC_VDSTA register (bits 208-215).	200 - 207	8	0x28
GLB_CCR_R	Reports same value as written to GLB_CCR register (bits 216-222).	208 - 214	7	0x0
GLB_TMP_OV_R	Reports same value as written to GLB_TMP_OV register (bit 223).	215	1	0x1
	Reserved	216 - 223	8	

Table 3: Operation Mode Write Registers Description (For complete SPI bits pattern, see Figure 6)

OPERATION MODE WRITE REGISTERS				
REGISTER NAME	**DESCRIPTION**	**SPI - BIT**	**LENGTH**	**RESET VALUE**
		POSITION	**[BITS]**	
ADC_DATA2_CH	0-31: Select which PWM FET Vdrain channel should be measured by ADC2. 32: ADC2 measures the LX®24132ILQ 32 Port Display Backlight LED Controller chip temperature. Refer to ADC_DATA2 register (Operation mode read registers bits 368-375) This field is read-write.	0 - 5	6	0x00
	Reserved	6 - 7	2	
ADC_DATA1_CH	0-31: Selects which PWM FET Vdrain channel should be measured by ADC1. 32: ADC1 measures LX®24132ILQ chip temperature. Refer to ADC_DATA1 register (Operation mode read registers bits 376-383). This field is read-write.	8 - 13	6	0x00
	Reserved	14 - 15	2	
GLB_PS_CTRL	Ten bit D/A used to control PS voltage feeding the LEDs. Register value controls the PDM (Pulsed Density Modulation) signal on the PS_CTRL output pin. External hardware converts the PDM signal to DC voltage ranging from 0 - 3.3 VDC. This field is write only.	16 - 25	10	0x100
	Reserved	26 - 27	2	
ADC_RFVDMIN	Setting bit to 1 sets ADC_MINVD register measured bits 0-6 to 0x7F and clears valid bit 7 (operation mode read bits 392-398, 399). ADC_RFMINVD bit is immediately cleared. Chip starts measuring FET Vdrain for all 32 strings. After all 32 FET Vdrain channels are measured, ADC_MIN_VD register bits 0-6 (adc_measure bits) contains the lowest FET Vdrain ADC reading. ADC_MIN_VD Valid bit 7 is set to '1' and ADC_MEASURE_DONE register bit 0 is set to '1'. Whenever ADC_MEASURE_DONE register equals '1', it means that LX®24132ILQ had found the lowest FET Vdrain out of 32 channels. The user should read the ADC_MIN_VD register's value and trim PS voltage by writing to the GLB_PS_CTRL register. Setting again ADC_RFMINVD bit to 1 will start new minimum FET Vdrain search cycle. This field is write only.	28	1	0x0

OPERATION MODE WRITE REGISTERS				
REGISTER NAME	**DESCRIPTION**	**SPI - BIT**	**LENGTH**	**RESET VALUE**
		POSITION	**[BITS]**	
GLB_CLR_ERR	Setting bit to 1, clears GLB_ERR register error bits (read bits 388-391) and re-enables all channels that were turned off by the LX®23108ILQ 8 Port LED Drivers due to FET Vdrain over-voltage or over-temperature. Note that over temperature/over-voltage bit in the GLB_ERR register cannot be cleared by the GLB_CLR_ERR register in cases where it was set due to over temperature event. This field is cleared on write.	29	1	0x0
	Reserved	30 - 31	2	
PWM_31	Sets PWM duty cycle from 0-99.999% by writing to PWM_31 register values ranging from 0-4095. **Note1**: New PWM_0 to PWM_31 values are loaded to the PWM_0–PWM_31 registers on the rising edge of CS_N input signal (SPI chip select) and are effective whenever PWM channel is turned off (PWM_OFF timing). This field is read-write.	32 - 43	12	Not defined
PWM_30	See PWM_31	44 - 55	12	
PWM_29	See PWM_31	56 - 67	12	
PWM_28	See PWM_31	68 - 79	12	
PWM_27	See PWM_31	80 - 91	12	
PWM_26	See PWM_31	92 - 103	12	
PWM_25	See PWM_31	104 - 115	12	
PWM_24	See PWM_31	116 - 127	12	
PWM_23	See PWM_31	128 - 139	12	
PWM_22	See PWM_31	140 - 151	12	
PWM_21	See PWM_31	152 - 163	12	
PWM_20	See PWM_31	164 - 175	12	
PWM_19	See PWM_31	176 - 187	12	
PWM_18	See PWM_31	188 - 199	12	
PWM_17	See PWM_31	200 - 211	12	Not defined
PWM_16	See PWM_31	212 - 223	12	
PWM_15	See PWM_31	224 - 235	12	
PWM_14	See PWM_31	236 - 247	12	
PWM_13	See PWM_31	248 - 259	12	
PWM_12	See PWM_31	260 - 271	12	
PWM_11	See PWM_31	272 - 283	12	
PWM_10	See PWM_31	284 - 295	12	
PWM_09	See PWM_31	296 - 307	12	
PWM_08	See PWM_31	308 - 319	12	
PWM_07	See PWM_31	320 - 331	12	
PWM_06	See PWM_31	332 - 343	12	
PWM_05	See PWM_31	344 - 355	12	
PWM_04	See PWM_31	356 - 367	12	

OPERATION MODE WRITE REGISTERS				
REGISTER NAME	DESCRIPTION	SPI - BIT	LENGTH	RESET VALUE
		POSITION	[BITS]	
PWM_03	See PWM_31	368 - 379	12	
PWM_02	See PWM_31	380 - 391	12	
PWM_01	See PWM_31	392 - 403	12	
PWM_00	See PWM_31	404 - 415	12	