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Microsemi

LX24232

32 CHANNEL LED BACKLIGHT CONTROLLER

DATASHEET

DESCRIPTION

LX24232 is a 32 channel display backlight LED controller. The device is part of a chipset consisting of LX24232 and *LX23108* – an 8 channel LED driver.

Each LX24232 controller is capable of controlling up to 32 LED channels, by controlling up to 4 LX23108 LED drivers. Each LX23108 8-channel LED driver contains eight FETs driving and controls up to 4x8 LED channels, where each channel is capable of driving a current of up to 200mA.

LX24232 has 32 independent, frame-by-frame controlled PWM output channels; each output channel supports independent duty-cycle and phase delay control.

LX24232 uses V_{sync} input for flexible synchronization schemes, including synchronization to either rising or falling edges, optimal V_{sync} jitter support, as well as single or multiple PWM cycles per frame support, and loss of V_{sync} support.

LX24232 consists of an on-chip internal power supply control circuitry that can be used to adjust voltage level of an external LED power source. This is done by regulating LED supply voltage to optimum level, and thus minimizing system power loss. At the same time, accurate current regulation for each of the 32 LED strings is maintained.

LX24232 includes an on-chip analog to digital converter for drain voltage (VD) measurements, for power supply control, fault detection and protection.

LX24232 32-Channel Display Backlight LED Controller is configured through SPI interface which speeds up communication and reduces the number of control signals between LX24232 and host system (FPGA, Video Processor, and CPU).

LX24232 supports a daisy chain connection in case more than 32 channels are required.

LX24232 32-Channel Display Backlight LED Controller can detect three types of system faults on each of its 32 channels (over-temperature, open LEDs and short LEDs). After detecting faults, unit takes the required measures to protect system.

LX24232 is capable of controlling up to 8 LX23108 drivers in a special configuration, where two consecutive channels are connected together for increased current support. For more details refer to application note.

KEY FEATURES

- 32 independent PWM output channels with independent 12-bit resolution duty-cycle (PWM high-time) control for each channel.
- Independent 12-bit phase delay (PD) control for each PWM output channel, optimized for 3D applications.
- 32 independent, frame-by-frame controlled, Duty-Cycle data (DTC)
- 32 independent, frame-by-frame controlled, Phase Delay data (PD)
- Duty-cycle & Phase Delay can be updated multiple times per frame
- Single or multiple PWM cycles in a single frame support.
- Frame-by-frame or multiple times per frame data rate through high-speed SPI interface
- V_{sync} synchronization.
- Configurable PWM output synchronization to either rising or falling edge of external sync pulse.
- Advanced V_{sync} jitter support
- Loss of V_{sync} support
- Optimized LED power supply voltage control.
- On-chip power supply trimming DAC for enhanced power supply control.
- ±1.5% precision current matching.
- 8-bit resolution current setting.
- Internal A/D for drain voltage measurements.
- Automatic minimum FET Vd report.
- Open string, short LED and over-temperature protection for each individual channel.
- On-chip thermal monitoring.

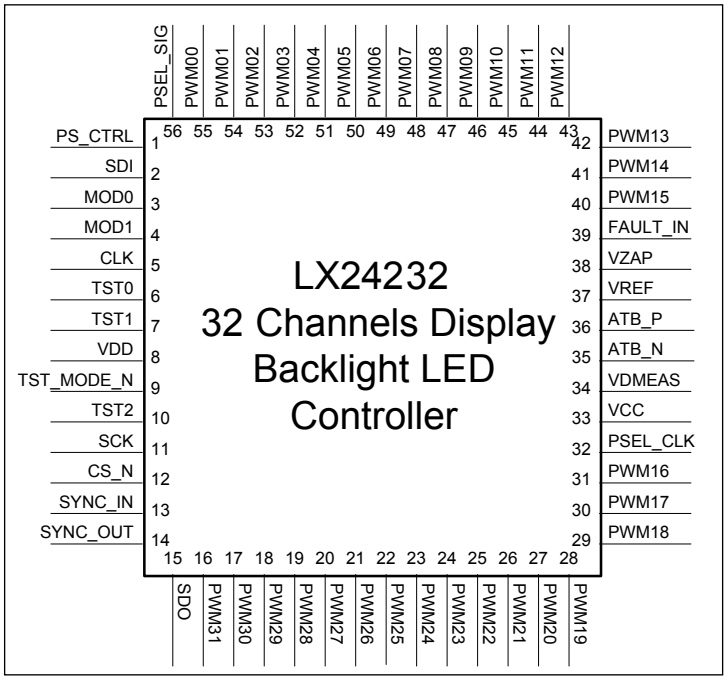
IMPORTANT: For the most current data, consult Microsemi's website: http://www.microsemi.com

PACKAGE ORDER INFO

T_A (°C)	Plastic MLPQ 8 x 8mm QFN 56 pin RoHS Compliant/Pb free MSL1
-40° to +85°C	**LX24232ILQ**

Note: Available in Tape & Reel. Append the letters ”TR” to part number. (LX24232ILQ-TR)

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, USA; Phone: 714-898-8121, Fax: 714-893-2570



THERMAL DATA (POWER CONSUMPTION)

21°C/W, according to JESD51-7.
Thermal resistance-junction to ambient
Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{jA})$.

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (V_{CC}, V_{DD})	-0.5V_{DC} to 4.5V_{DC}
All other pins	-0.5V_{DC} toV_{CC}+0.3 up to 4.5V_{DC}
Operating Ambient Temperature Range…	-40°C to +85°C
Maximum Operating Junction Temperature	150°C
ESD Protection at all I/O pins	± 4KV HBM
Storage Temperature Range	-65°C to +150°C
Package Peak Temperature for Solder Reflow (40 seconds maximum exposure)	+260°C (+0,-5°C)

Notes: Exceeding these ratings could result in damage to device. All voltages are with respect to Ground.

APPLICABLE DOCUMENTS

- LX23108AL – 8 Channel LED Drivers datasheet (32QFN 5x5)
- LX23108AH – 8 Channel LED Drivers datasheet (32QFN 7x7)
- AN-182, Designing a Low Current LED Backlight Driver System, cat no. 06-0077-080

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TYPICAL APPLICATION INFORMATION

Typical Applications

- LCD Display Back-lighting
- LED Signage
- LED Displays

Figure 1 illustrates a typical application where a System Controller communicates with a LX24232 32 Channel Display Backlight LED Controller through an SPI bus. LX24232 is connected to four LX23108 arrays supporting a total of 32 LED strings. Each LX23108 transmits current very accurately and can drive eight LED strings. Output currents' value is set by the LX24232 which produces a precise and stable voltage, V_{REF}.

All four LX23108 components are cascaded, allowing LX24232 LED controller to sequentially select all 32 channels for monitoring, searching for VD_{MIN} and optimally adjusting power supply voltage through PDM control. Channel dimming is individually adjusted by 32 PWM output pins; 8 input channels per single LX23108 component. Currents are scaled by the external sense resistors.

Figure 2 shows a multiple connection of several LX24232 controllers, supporting 32x4 LED strings.

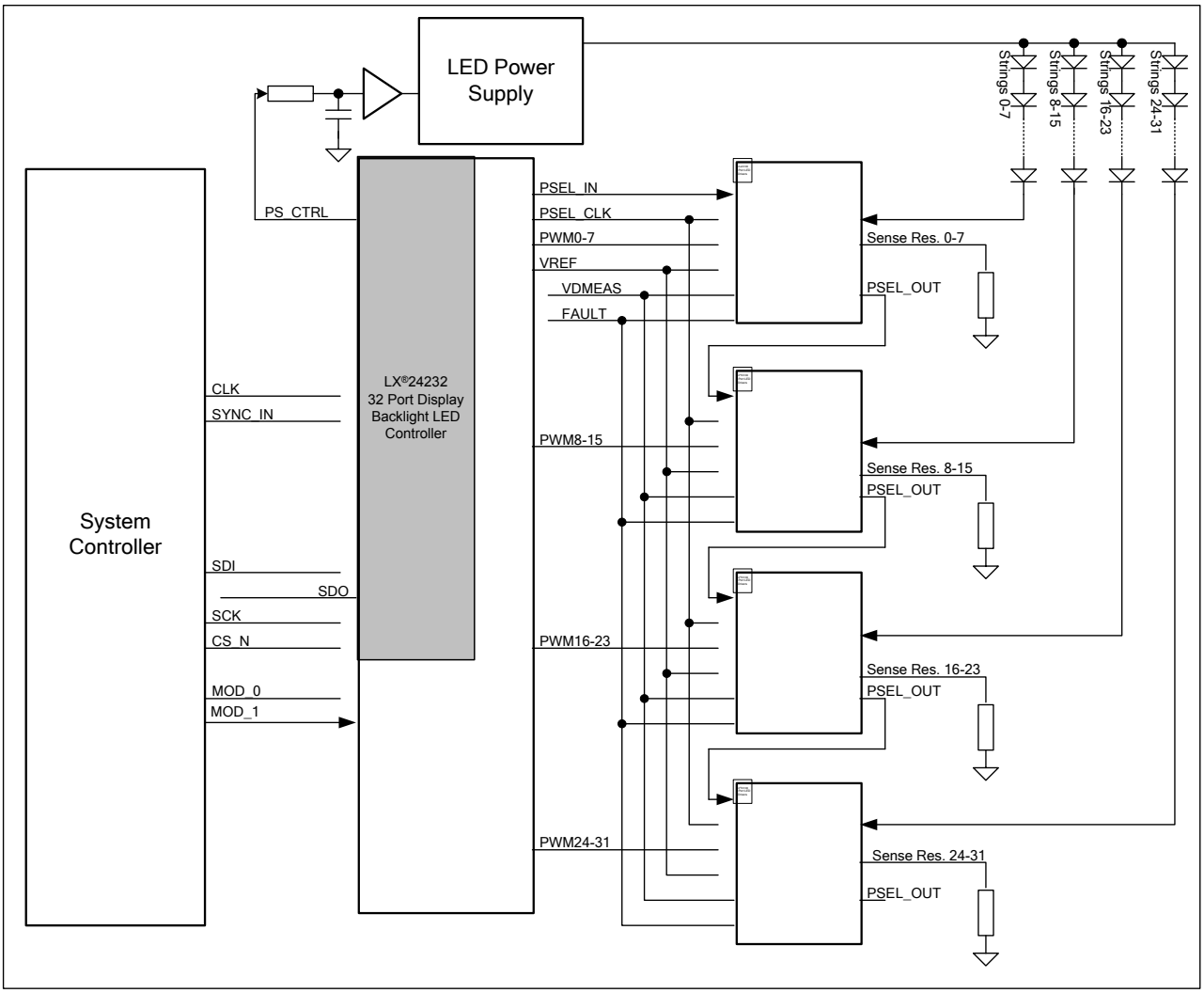


Figure 1: Low Voltage LX24232 and LX23108 – A Typical Application

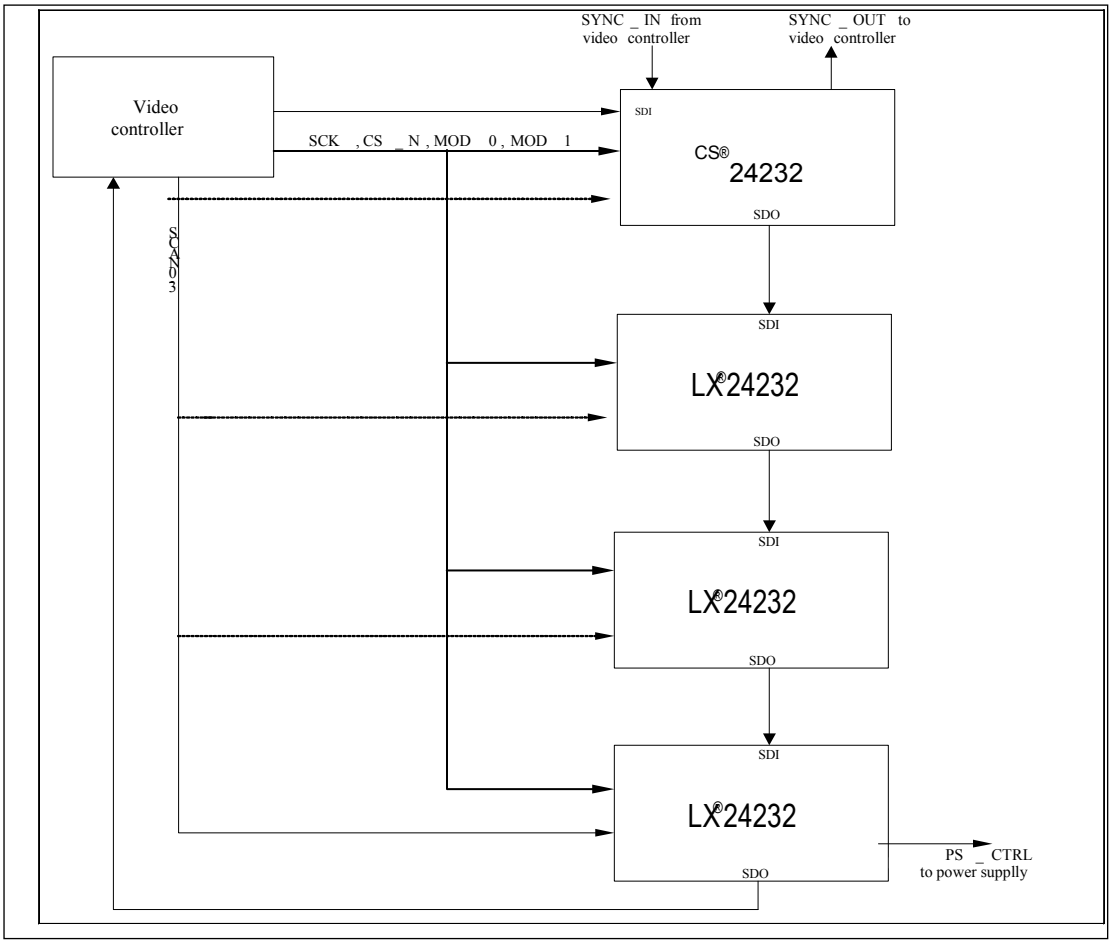


Figure 2: Typical Application with Four LED Controllers

Electrical Characteristics

Unless otherwise specified, the following specifications apply to the operating ambient temperature, -40° to +85° C, and the following test conditions: $V_{DD} = V_{CC} = 3.3$ VDC.

Performance must be guaranteed for $0°C \leq T_J \leq +110°C$.

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX24232 LED CONTROLLER			UNITS
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Input voltage	V_{DD}, V_{CC}	*Note 1	3.0	3.3	3.6	VDC
Operating current	I_{DD}	From V_{DD} power supply		3	5	mA
	I_{CC}	From V_{CC} power supply		3.5	5	mA
DIGITAL INTERFACE						
Input logic high threshold	V_{IH}		2.2			VDC
Input logic low threshold	V_{IL}				0.8	VDC
Output high voltage	V_{OH}	I_{OH} = -1mA	2.4			VDC
Output low voltage	V_{OL}	I_{OH} = 1mA			0.4	VDC
SCK clock frequency	F_{sck}				32	MHz
CLK frequency	F_{clk}	Duty Cycle 40% - 60%	3.5		8.192	MHz
SYNC_IN pulse width	sync_in_pulse		3			Clocks
SYNC_OUT pulse width	sync_out_pulse	T_{SYNC_OUT} [CLK] = 320*(PWM_FRDIV+1)		320		Clocks
LED CURRENT CONTROL						
DAC resolution	V_{ref_err}			8		bits
V_{REF} output accuracy error		1.25 V_{DC} < V_{REF} ≤ 2.5 V_{DC}			± 1.43	%
		0.5 VDC< V_{REF} < 1.25 V_{DC}			± 2	%
	V_{ref}	0.234 V_{DC}< V_{REF} < 0.5 V_{DC}			± 5.26	%
V_{REF} output range					2.5	V_{DC}
Note 1: During power up, V_{DD} should not precede V_{CC}.						
ADC						
Resolution				7		bits
LSB				15.6		mV
Offset error				1		LSB
Reading error		1 V_{DC} ≤ Drain Voltage ≤ 2 V_{DC}			± 3	LSB
Full scale ADC input				2		V
PWS CONTROL						
Duty-cycle resolution		At all system clock frequencies (fPWM)		12		bits
Phase-delay resolution		At all system clock frequencies (fPWM)		12		bits

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX24232 LED CONTROLLER			UNITS
			MIN.	TYP.	MAX.	
PWM frequency range		$F_{PWM}[Hz] = \frac{CLK[MHz] \cdot 10^6}{4096 \cdot (PWM\_FRDIV + 1)}$	50		2K	Hz
SYSTEM PARAMETERS – PROTECTIONS						
Short LED detection		At T_{AMB} = 25°C and V_{CC} = 5VDC Short LED detection of *LX23108* FET Array. Detection is traced per channel when LED voltage is higher than "Short Drain Voltage Threshold".	6.0	6.4	6.8	V_{DC}
Over-temperature detection		Over-temperature indications per channel from *LX23108* LED Driver.	150	180	210	° C

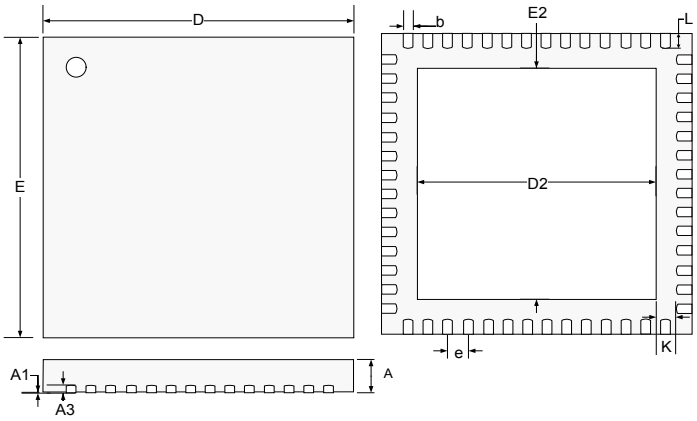
Functional Pin Description

NAME	PIN #	DESCRIPTION
AGND	EPAD	Exposed PAD – Analog ground. A proper ground plane should be deployed around this pin wherever possible.
VCC	33	Supply voltage for the internal analog circuit. A low ESR bypass capacitor (1µF) should be placed as close as possible to this pin, using low impedance traces to AGND.
ATB_N ATB_P	35, 36	Internal test output pins; do not connect.
SDI	2	Serial Data Input pin. Data from SPI Host to this pin is clocked into input shift register at the rising edge of SCK clock. MSB is input first.
SDO	15	Serial Data Output pin. Data from input shift register is shifted out from this pin at the falling edge of SCK clock. MSB is output first. SDO pin can be connected to SDI pin of another device to form a cascaded SPI chain. Data from LED controller can also be transmitted to System Controller from this pin. If not used, leave this pin disconnected.
SCK	11	Clock signal for SPI operation. A single clock shifts data by one bit. It is only active when shifting data. This happens when CS_N is at 'low' level.
CS_N	12	Chip Select – SPI control signal input. Data shift starts when CS falls from 'high' to 'low' and data shifted into input register is latched into buffer registers at the rising edge of this signal.
SYNC_IN	13	Synchronization input. If not used, connect this pin to Ground.
SYNC_OUT	14	Synchronization output utilized for multi-chip applications. If unused, leave unconnected.
CLK	5	LX24232 system clock.

<table>
<tr><th>NAME</th><th>PIN #</th><th>DESCRIPTION</th></tr>
<tr><td>VDD</td><td>8</td><td>Connects to Core Logic and I/O supply rail. A ceramic 1µF or greater decoupling capacitor should be connected from this pin to DGND.</td></tr>
<tr><td>PWM0-31</td><td>55 to 40
31 to 16</td><td>PWM Gate control output signals used to command up to 4 x 8-channel LX23018LILQ LED Driver ICs</td></tr>
<tr><td>VDMEAS</td><td>34</td><td>MOSFET drain voltage sensing input. External MOSFET drain voltage is sensed via this pin and used to control external power supply, maintaining optimum voltage for LED strings.</td></tr>
<tr><td>FAULT_IN</td><td>39</td><td>A fault input signal coming from LED Driver IC. It is asserted 'low' when fault event is detected at one of the LED strings.</td></tr>
<tr><td>PS_CTRL</td><td>1</td><td>Power supply control signal output. This Pulse Density Modulation signal (PDM) is used for interfacing to power supply, adjusting DC voltage of LED strings to optimum level. Should be connected to power supply control through resistor-capacitor low pass filter.</td></tr>
<tr><td>MOD0</td><td>3</td><td rowspan="2"><table>
<tr><th>MOD_1</th><th>MOD_0</th><th>TRANSACTION TYPE</th></tr>
<tr><td>0</td><td>0</td><td>Duty Cycle Packet (12-bits resolution per channel)</td></tr>
<tr><td>0</td><td>1</td><td>Phase Delay Packet (12 bits resolution per channel)</td></tr>
<tr><td>1</td><td>0</td><td>Configuration Packet</td></tr>
<tr><td>1</td><td>1</td><td>Reserved for production</td></tr>
</table></td></tr>
<tr><td>MOD1</td><td>4</td></tr>
<tr><td>TST0</td><td>6</td><td>Internal test pins. Should be tied to VDD.</td></tr>
<tr><td>TST1</td><td>7</td><td>Internal test pins. Should be tied to VDD.</td></tr>
<tr><td>TEST_MODE_N</td><td>9</td><td>Production test mode pin. Should be tied to VCC for normal operation.</td></tr>
<tr><td>TST2</td><td>10</td><td>Internal test pins. Should be tied to VDD.</td></tr>
<tr><td>VZAP</td><td>38</td><td>Zapping input for IC production trimming; must be tied to VCC.</td></tr>
<tr><td>VREF</td><td>37</td><td>Analog reference output signal used for 8-channel LED drivers.</td></tr>
<tr><td>PSEL_SIG</td><td>56</td><td>Channel selection serial output signal to LX23108, which is a 32 bits packet, used for selecting (monitoring) one of the 32 strings drain voltages and thermal sensors signals.</td></tr>
<tr><td>PSEL_CLK</td><td>32</td><td>Channel selection serial clock signal. Each single clock shifts internal register data of LX23108 by one bit, allowing monitoring the next channel.</td></tr>
</table>

Package Information

LQ **56-Pin 8x8mm QFN**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.00	6.25	0.236	0.246
E2	6.00	6.25	0.236	0.246
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

LX24232ILQ Principle of Operation

LX®24232ILQ 32-Channel Display Backlight LED Controller is designed to drive up to 32 LED strings and control external power supplies to regulate LED current. Interface with the Hosting system (Video Processor / Timing Controller (TCON) / MCU) is accomplished via a standard SPI bus. LED current and PWM dimming duty-cycle commands are received from Hosting system in a digital format and executed by internal circuitry to obtain desired backlight control. In addition, device provides a power supply control signal (PS_CTRL) used to control external power supply and trim it to optimum level. This minimizes system power dissipation, while maintaining accurate current regulation for each of the 32 LED strings.

Block Diagram

Figure 3 shows LX®24232ILQ LED 32-Channel Display Backlight LED Controller block diagram, describing its main functions. SPI block implements communication with external Controller. Power supply control circuitry adjusts LED strings' main voltage by utilizing PDM method (Pulse Density Modulation). Scanning control circuitry includes the required logic needed for performing zone selection.

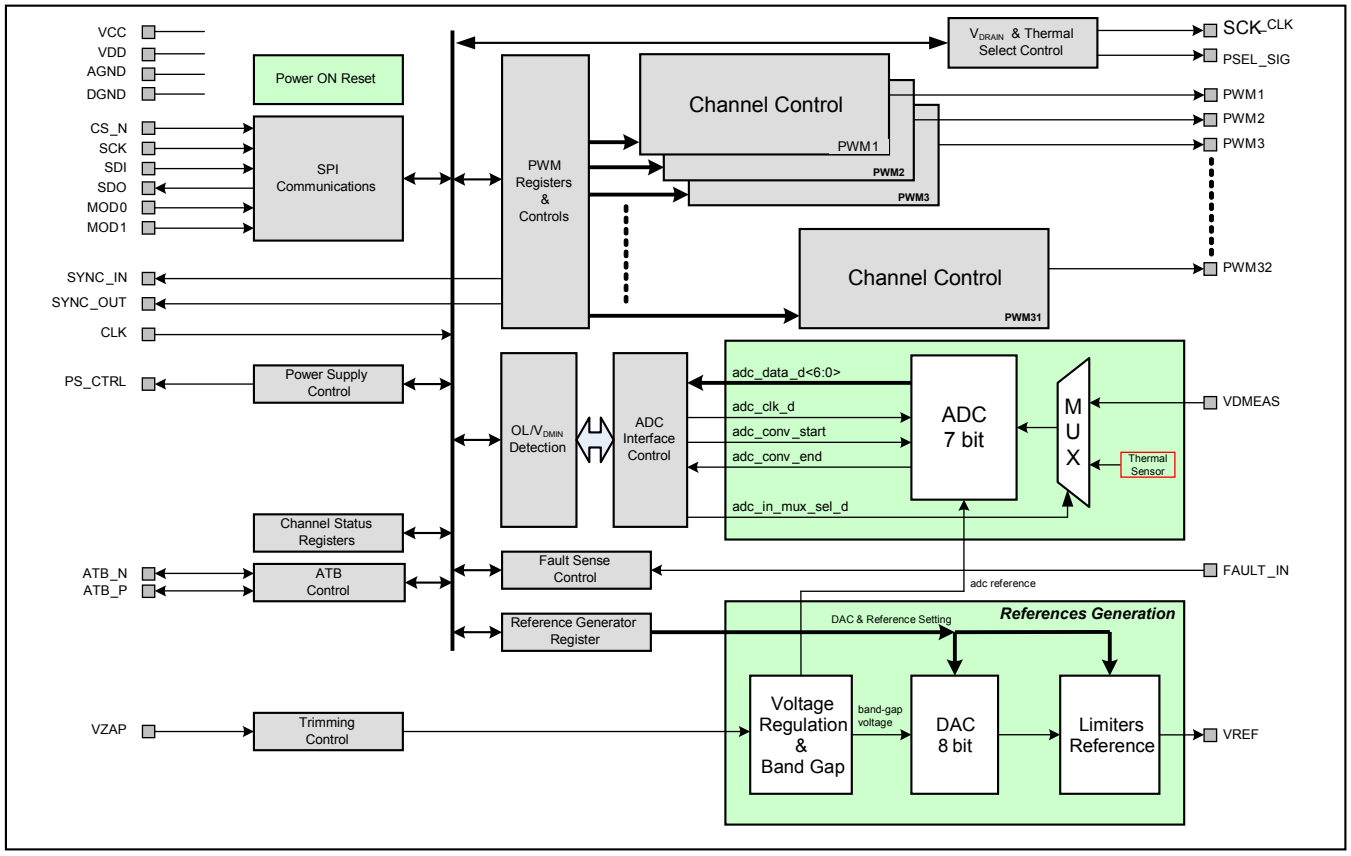


Figure 3: LX®24232ILQ: Detailed Block Diagram

SPI Interface Characteristics

SPI interface consists of four signal lines: SDI, SDO, SCK, and CS_N (see

Figure 4).

- **SDI**: Serial data input to LX®24232ILQ
- **SDO**: Serial data output from LX®24232ILQ
- **SCK**: Serial data clock input
- **CS_N**: Serial data chip select

SDI signal is sampled at the rising edge of SCK, while SDO is driven at the falling edge of SDK, where MSB is shifted out first.

SPI data transmission/reception should be executed, starting from bit 447 to bit 0 (DTC Packet / Phase-Delay Packet modes), or starting from bit 223 to bit 0 (Configuration mode). Figure 5 displays SPI timing diagram for a 4-driver configuration. SPI data of the fourth LX®24232ILQ is transmitted first, following SPI data of the third, second and then first LX®24232ILQ.

SPI Noise Immunity

LX®24232ILQ SPI interface includes special noise immunity protection mechanisms, which improve electrical SPI interface immunity against high frequencies noise, short spikes and glitches in a noisy PCB environment. These mechanisms include:

- Filter short glitches and spikes of CS_N, MOD_0 and MOD_1 signals. These signals should remain in either logic "1" or logic "0" for at least 8 clocks (CLK). Shorter periods will be ignored.
- Ignore SPI transaction if number of SPI SCK clocks is not an integer multiple of 8 (8, 16, 24, 32, etc.); in this case internal registers remains unchanged.
- If SPI CS_N chip select signal is Set Low for less than 8 x System Clocks, this pulse is ignored, the transaction is canceled and the internal registers remains unchanged.

SPI Timing

Figure 4 and Figure 5 describe LX®24232ILQ SPI timing. Refer to Table 1 for timing characteristics.

- Last communication transaction before main counter wraps MUST be of "DTC Packet" type, otherwise transaction will not be loaded.
- First SCK SPI rising edge should occur Tdel_sck after CS_N SPI chip select negation.
- Minimum time between the end of SPI transaction to the beginning of the next one should be Tadj_cs.
- CS_N must be set to "1" at least 8 sysclks before SYNC_IN signal arrives. Otherwise, data will be ignored.

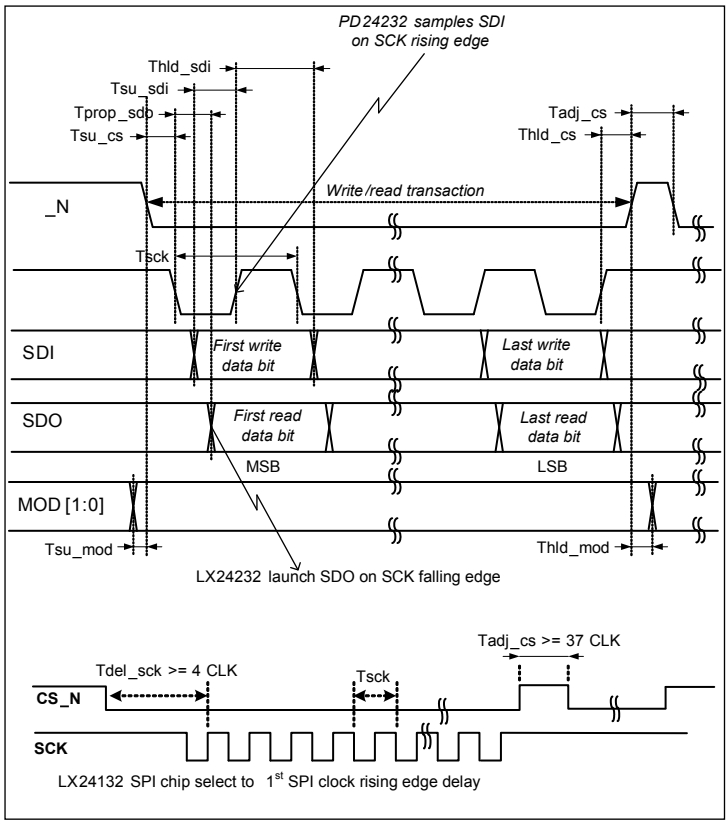
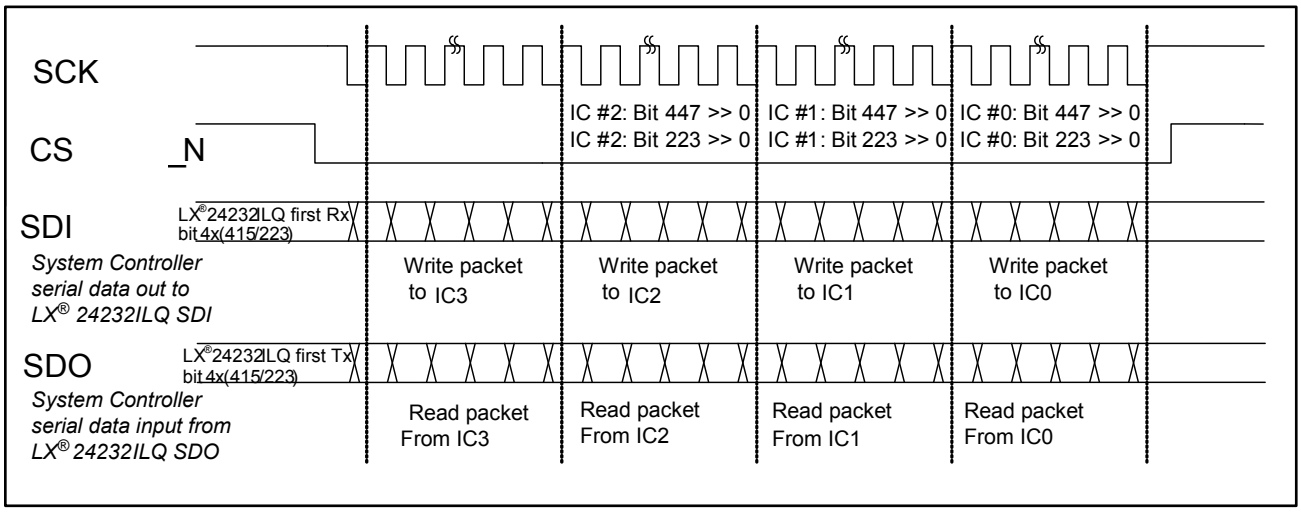


Figure 4: SPI Signals Diagrams

Table 1 -Timing Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX®24232ILQ LED CONTROLLER			UNITS
			MIN.	TYP.	MAX.	
SDI set up time to SCK	T_{su_sdi}		5			ns
SDI hold time to SCK	T_{hld_sdi}		5			ns
SDO prop delay from SCK	T_{prop_sdo}	20 pF capacitive load			12	ns
CS_N set up time to SCK	T_{su_cs}		5			ns
CS_N hold time to SCK	T_{hld_cs}		5			ns
Time between adjacent SPI transactions	T_{adj_cs}			37		CLK
Time from de-assertion of CS_N to 1st SCK rising edge	T_{del_sck}		8			CLK
MOD[1:0] set up time to CS	T_{su_mod}		8			CLK
MOD[1:0] hold time to CS	T_{hld_mod}		0			CLK
SYNC_IN propagation delay	$T_{PD\_SYNC\_IN}$		8			CLK
SYNC_IN pulse width	sync_in_pulse		4			CLK
SYNC_OUT pulse width	sync_out_pulse	T_{SYNC_OUT} [CLK] = 320*(PWM_FRDIV+1)		320		CLK



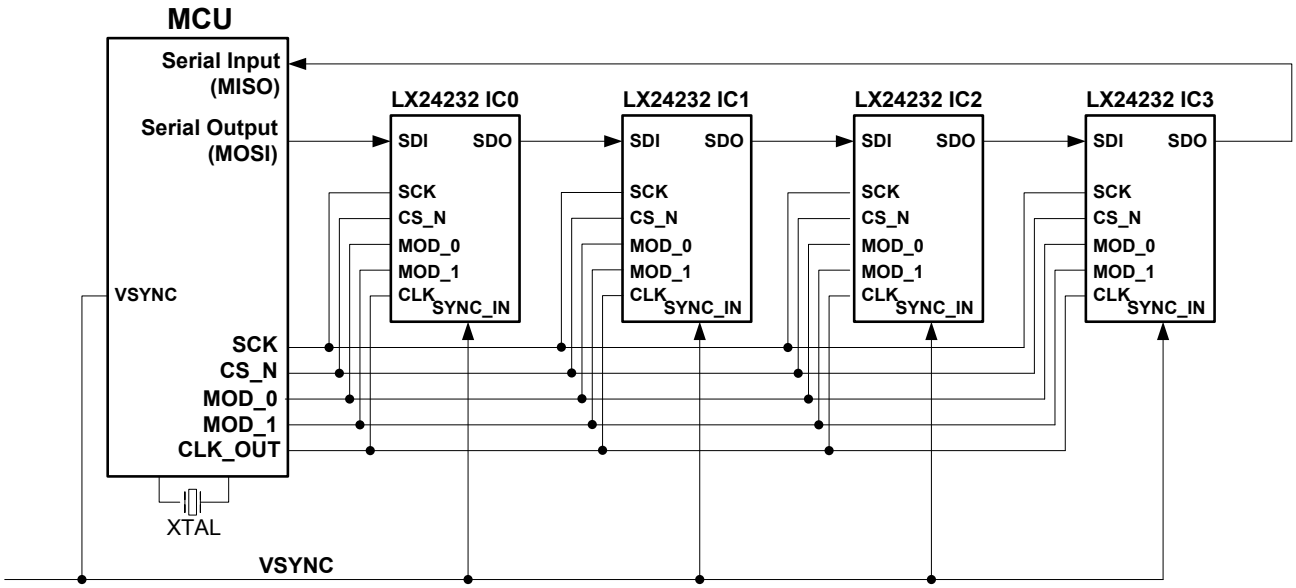


Figure 5: SPI Signals Diagram for a Four LED Controllers Configuration

LX24232ILQ Application Information

Communication packet types

Chip configuration and monitoring is accomplished by sending and receiving a series of bits over SPI.

There are four transaction types that select the type of communication packet to be transmitted to LX24232. Only three of the four possible transaction types are used. These transactions are described in Table 2:

Table 2 – Communication Packet Types

MOD_1 pin	MOD_0 pin	TRANSACTION TYPE
"0"	"0"	Duty Cycle Packet (12-bits resolution per channel)
"0"	"1"	Phase Delay Packet (12 bits resolution per channel)
"1"	"0"	Configuration Packet
'1"	'1"	*Reserved for production*

Packet type is chosen by setting MOD_0 and MOD_1 pins of LX24232ILQ according to Table 2, where:
"0" – MOD_x signal is logic low.
"1" – MOD_x signal is logic high.

SPI Transaction Packets Overview:

LX24232ILQ SPI mechanism is based on a shift-register.

For each SPI transaction sent to LX24232ILQ (*Write* transactions), an SPI transaction of the same length is sent back to MCU (*Read* transaction).

There are four types of transaction packets:

- **DTC (Duty-Cycle) Packet**: Write packet contains duty-cycle data for each channel, in addition to control bits for controlling on-going operations. Read packet contains all information (ADC measurements, channel number having minimum drain-voltage measurement, etc.) required for on-going operation.
- **PD (Phase-Delay) Packet**: Write packet contains phase-delay values for each channel; Read packet contains no information (don't care).
- **CONFIG (Configuration) Packet**: Write packet contains all LX24232ILQ configuration fields, such as PWM frequency, LED current, etc. Read packet contains read-back of configuration information.
- **Production packet**: For production purposes only; cannot be accessed in normal operation.

Important note: Bit locations with higher values indicate the most significant bit.

Example:

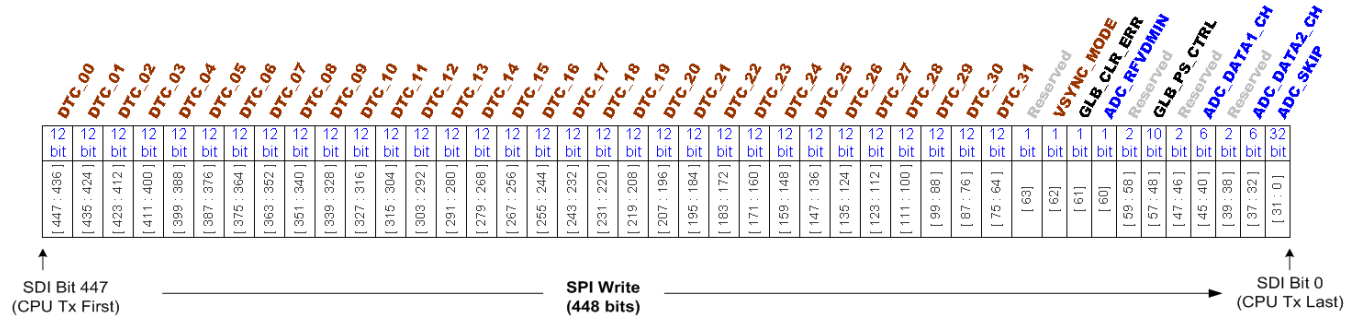
In ADC_DATA2 register in DTC-Read packet, bits 0-6 (bit location 400-406) represent ADC measurement value. Therefore, bit location 406 (bit 6 of the register) is the Most Significant bit, and bit location 400 (bit 0 of the register) is the least significant bit.

Figure 6, Figure 7, and Figure 8 illustrate the read/write registers involved in each SPI bit stream for operation and configuration mode[1].

[1] For more details regarding specific bit(s) functions, contact your local Microsemi© representative.

DTC (Duty-Cycle) Packet (Mode Select Pins MOD_1, MOD_0 = "00"):

Write Packet:



Read Packet:

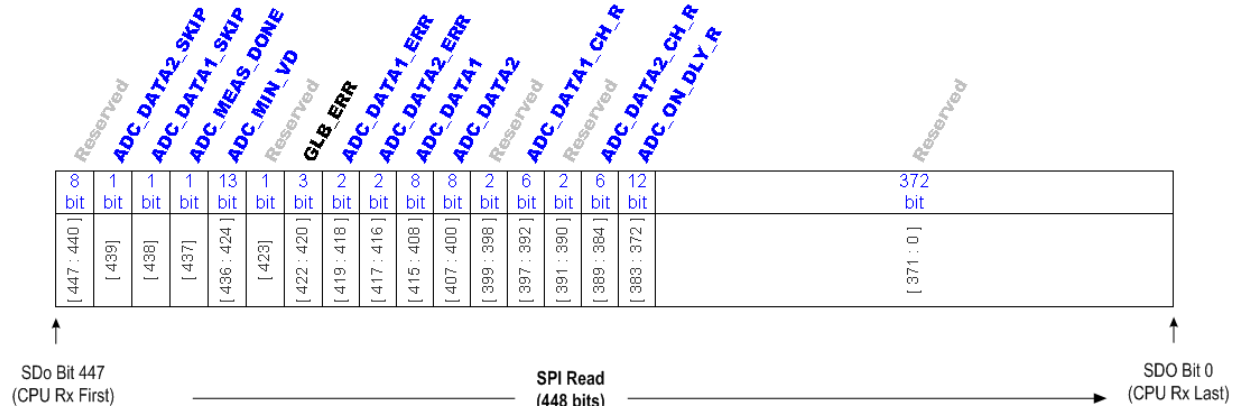
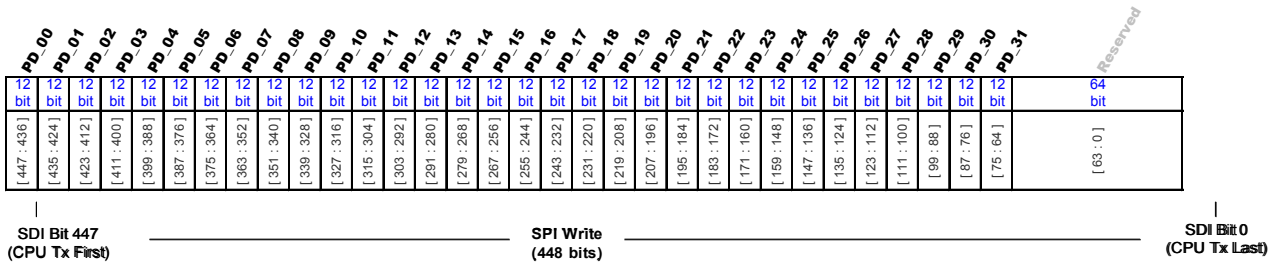


Figure 6 - DTC (Duty-Cycle) Write / Read SPI Communication Packets

PD (Phase Delay) Packet (Mode Select Pins MOD_1, MOD_0 = "01"):

Write Packet:



Read Packet:

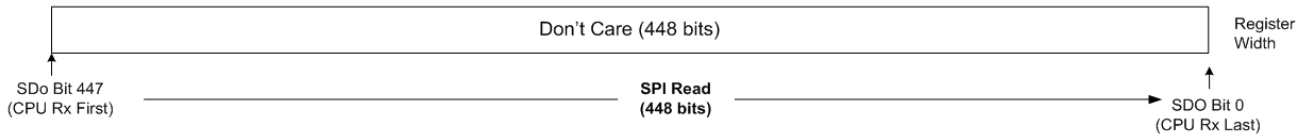
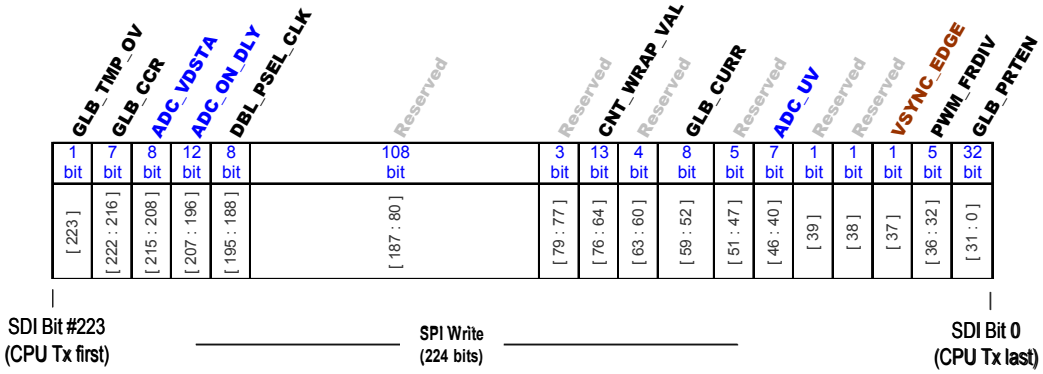


Figure 7 - Phase Delay Write / Read Packets

Configuration Packet (Mode Select Pins MOD_1, MOD_0 = "10"):

Write Packet:



Read Packet:

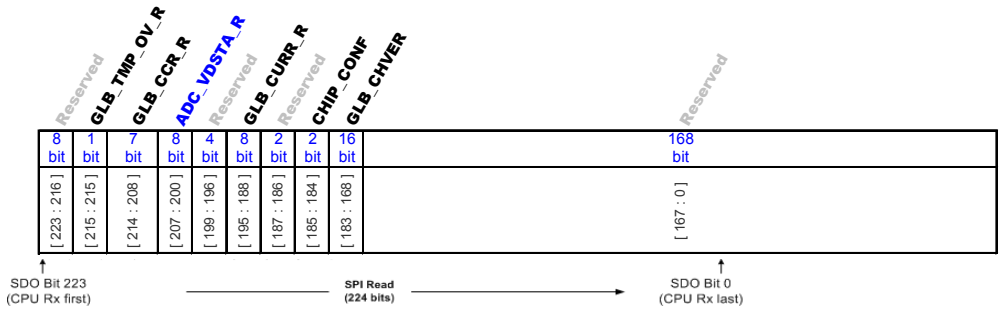


Figure 8 - Config Packet Write / Read Packets

For multiple chip applications, SPI communication should be cascaded (see Figure 5).

Detailed SPI Transaction Packets Description

DTC-Write Packet Bit Description (MOD_1, MOD_0 = "00"):

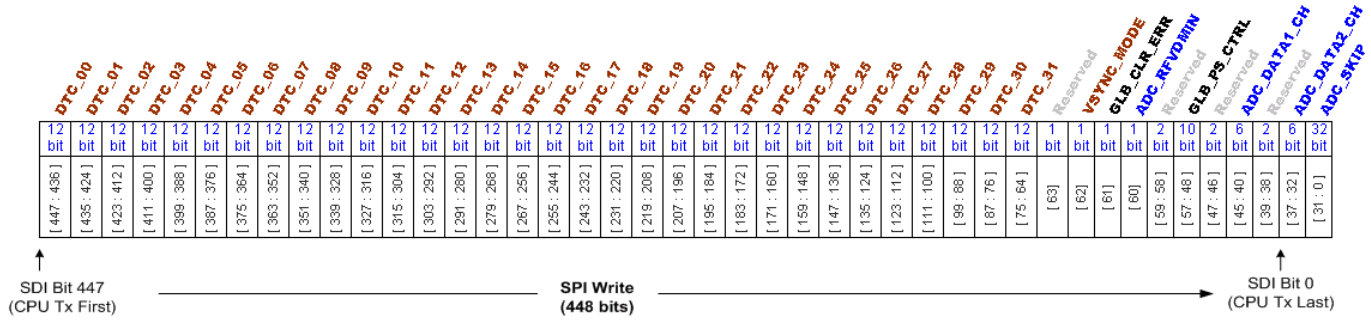


Figure 9 - DTC (Duty-Cycle) Write SPI Communication Packets

Table 3 - DTC Write Packet Bit Description Table

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
1	ADC_SKIP	ADC converter "skip channel measurement" control bit. Bit-per-channel control. When ADC_SKIP(n) bit is set, ADC will skip drain voltage measurement of the selected channel. For example, if ADC_SKIP(1) = "1", then LX23108ILQ channel connected to PWM1 pin will be skipped. ADC_SKIP bit should be set if duty-cycle value (DTC_xx) of a channel is lower than ADC_ON_DLY register value (see CONFIG-Write packet): $\text{set ADC\_SKIP(n)} = \begin{cases} 0 & if(DTC\_n > ADC\_ON\_DLY) \\ 1 & if(DTC\_n \le ADC\_ON\_DLY) \end{cases}$	DTC Write	0-31	32	N/A
2	ADC_DATA2_CH	ADC_DATA2_CH = 0 to 31: Selects which PWM FET V_{drain} channel ADC2 should measure. ADC_DATA2_CH = 32: ADC2 measures LX®24232ILQ chip temperature. Refer to ADC_DATA2 register (DTC read-packet)	DTC Write	32-37	6	0x00
3	Reserved	Reserved	DTC Write	38-39	2	N/A
4	ADC_DATA1_CH	ADC_DATA2_CH = 0 to 31: Selects which PWM FET Vdrain channel ADC1 should measure. ADC_DATA2_CH = 32: ADC1 measures LX®24232ILQ chip temperature. Refer to ADC_DATA1 register (DTC read-packet).	DTC Write	40-45	6	0x00
5	Reserved	Reserved	DTC Write	46-47	2	N/A

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
6	GLB_PS_CTRL	Ten bit D/A used for controlling PS voltage, controlling LEDs power supply. Register value controls PDM (Pulsed Density Modulation) signal on PS_CTRL output pin. External RC-filter (typically 2KΩ and 0.1µF) converts PDM signal to DC voltage ranging from 0 to 3.3VDC. $$PS\_CTRL[V]^{*} = GLB\_PS\_CTRL \cdot \frac{3.3V}{1024}$$ * After RC low-pass filter	DTC Write	48-57	10	0x100
7	Reserved	Reserved	DTC Write	58-59	2	N/A
8	ADC_RFVDMIN	ADC refresh minimum VD measurement control bit. Setting bit to "1" sets ADC_MINVD register measured bits 0-6 to 0x7F and clears valid bit 7 (DTC read-packet). ADC_RFMINVD bit is immediately cleared. Chip starts measuring FET V_{drain} for all 32 strings. After all 32 FET V_{drain} channels are measured, ADC_MIN_VD register, bits 0-6 (adc_measure bits), contains the lowest FET V_{drain} ADC reading. ADC_MIN_VD Valid bit 7 is set to '1' and ADC_MEASURE_DONE register bit 0 is set to '1'. Whenever ADC_MEASURE_DONE register equals '1', it means LX®24232ILQ had found the lowest FET V_{drain} out of 32 channels. User should read ADC_MIN_VD register's value and trim PS voltage by writing to the GLB_PS_CTRL register. Setting again ADC_RFMINVD bit to 1 will start a new minimum FET V_{drain} search cycle.	DTC Write	60	1	0x00
9	GLB_CLR_ERR	Setting bit to 1 clears GLB_ERR register error bits (DTC Read-packet bits 420 to 422) and re-enables all channels that were turned off by LX®23108ILQ 8-Port LED Drivers due to FET V_{drain} over-voltage or over-temperature. Note that over temperature/over-voltage bit in GLB_ERR register cannot be cleared by GLB_CLR_ERR register in cases where it was set due to over temperature event. This field is cleared on write.	DTC Write	61	1	0x00
10	VSYNC_MODE	External ***SYNC_IN pin*** synchronization mode. **VSYNC_MODE = "0":** No synchronization mode (Stand-Alone operation). In this mode LX24232ILQ ignores SYNC_IN input pin state, and PWM block internal 13-bit main counter automatically wraps-around at 4095 --> 0. **VSYNC_MODE = "1":** External Synchronization mode. In this mode, PWM output signals are synchronized to either a rising-edge or a falling edge (selected by VSYNC_EDGE field in CONFIG packet, bit 37) of SYNC_IN pin. PWM block 13-bit main counter wraps-around when synchronization signal arrives, synchronizing PWM output signals. If synchronization signal fails to arrive (SYNC_IN pin state does not change), 13-bit main counter wraps-around at the value written in CNT_WRAP_VAL register (CONFIG-Write packet, bits 64 to 76). For more information, see "PWM Synchronization input (SYNC_IN pin)".	DTC Write	62	1	0x00

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
11	Reserved	Reserved	DTC Write	63	1	N/A
12	DTC_31	PWM output high-time (duty-cycle) control. Sets PWM high-time (PWM output = "1") of PWM31 output pin. DTC range is 0 to 4095. Value written in this field is written to PWM channel 31 one-shot down-counter. Absolute high-time of PWM output is defined by the following formula: $$T_{PWM(n)="1"}[ms] = \begin{cases} \frac{DTC\_(n)}{4096} \cdot T_{PWM\_CYCLE}[ms] & \text{if } 0 \le DTC\_(n) \le 4094 \\ \text{Always "1"} & \text{if } DTC\_(n) = 4095 \end{cases}$$ Where: n = 0 to 31, and: $$T_{PWM\_CYCLE}[ms] = \frac{4096 \cdot (PWM\_FRDIV + 1)}{1000 \cdot CLK[MHz]}$$ **Note**: New DTC_0 to DTC_31 values are loaded to DTC_0-DTC_31 registers on next PWM main-counter wrap-around, after rising edge of CS_N input signal. For more information see "Advanced PWM output control".	DTC Write	64-75	1	N/A
13	DTC_30	PWM high-time (duty-cycle) control for PWM30. Refer to DTC_31.	DTC Write	76-87	12	N/A
14	DTC_29	PWM high-time (duty-cycle) control for PWM29. Refer to DTC_31.	DTC Write	88-99	12	N/A
15	DTC_28	PWM high-time (duty-cycle) control for PWM28. Refer to DTC_31.	DTC Write	100-111	12	N/A
16	DTC_27	PWM high-time (duty-cycle) control for PWM27. Refer to DTC_31.	DTC Write	112-123	12	N/A
17	DTC_26	PWM high-time (duty-cycle) control for PWM26. Refer to DTC_31.	DTC Write	124-135	12	N/A
18	DTC_25	PWM high-time (duty-cycle) control for PWM25. Refer to DTC_31.	DTC Write	136-147	12	N/A
19	DTC_24	PWM high-time (duty-cycle) control for PWM24. Refer to DTC_31.	DTC Write	148-159	12	N/A
20	DTC_23	PWM high-time (duty-cycle) control for PWM23. Refer to DTC_31.	DTC Write	160-171	12	N/A
21	DTC_22	PWM high-time (duty-cycle) control for PWM22. Refer to DTC_31.	DTC Write	172-183	12	N/A
22	DTC_21	PWM high-time (duty-cycle) control for PWM21. Refer to DTC_31.	DTC Write	184-195	12	N/A

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
23	DTC_20	PWM high-time (duty-cycle) control for PWM20. Refer to DTC_31.	DTC Write	196-207	12	N/A
24	DTC_19	PWM high-time (duty-cycle) control for PWM19. Refer to DTC_31.	DTC Write	208-219	12	N/A
25	DTC_18	PWM high-time (duty-cycle) control for PWM18. Refer to DTC_31.	DTC Write	220-231	12	N/A
26	DTC_17	PWM high-time (duty-cycle) control for PWM17. Refer to DTC_31.	DTC Write	232-243	12	N/A
27	DTC_16	PWM high-time (duty-cycle) control for PWM16. Refer to DTC_31.	DTC Write	244-255	12	N/A
28	DTC_15	PWM high-time (duty-cycle) control for PWM15. Refer to DTC_31.	DTC Write	256-267	12	N/A
29	DTC_14	PWM high-time (duty-cycle) control for PWM14. Refer to DTC_31.	DTC Write	268-279	12	N/A
30	DTC_13	PWM high-time (duty-cycle) control for PWM13. Refer to DTC_31.	DTC Write	280-291	12	N/A
31	DTC_12	PWM high-time (duty-cycle) control for PWM12. Refer to DTC_31.	DTC Write	292-303	12	N/A
32	DTC_11	PWM high-time (duty-cycle) control for PWM11. Refer to DTC_31.	DTC Write	304-315	12	N/A
33	DTC_10	PWM high-time (duty-cycle) control for PWM10. Refer to DTC_31.	DTC Write	316-327	12	N/A
34	DTC_09	PWM high-time (duty-cycle) control for PWM9. Refer to DTC_31.	DTC Write	328-339	12	N/A
35	DTC_08	PWM high-time (duty-cycle) control for PWM8. Refer to DTC_31.	DTC Write	340-351	12	N/A
36	DTC_07	PWM high-time (duty-cycle) control for PWM7. Refer to DTC_31.	DTC Write	352-363	12	N/A
37	DTC_06	PWM high-time (duty-cycle) control for PWM6. Refer to DTC_31.	DTC Write	364-375	12	N/A
38	DTC_05	PWM high-time (duty-cycle) control for PWM5. Refer to DTC_31.	DTC Write	376-387	12	N/A
39	DTC_04	PWM high-time (duty-cycle) control for PWM4. Refer to DTC_31.	DTC Write	388-399	12	N/A
40	DTC_03	PWM high-time (duty-cycle) control for PWM3. Refer to DTC_31.	DTC Write	400-411	12	N/A

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
41	DTC_02	PWM high-time (duty-cycle) control for PWM2. Refer to DTC_31.	DTC Write	412-423	12	N/A
42	DTC_01	PWM high-time (duty-cycle) control for PWM1. Refer to DTC_31.	DTC Write	424-435	12	N/A
43	DTC_00	PWM high-time (duty-cycle) control for PWM0. Refer to DTC_31.	DTC Write	436-447	12	N/A

DTC-Read Transaction Packet (MOD_1, MOD_0 = "00"):

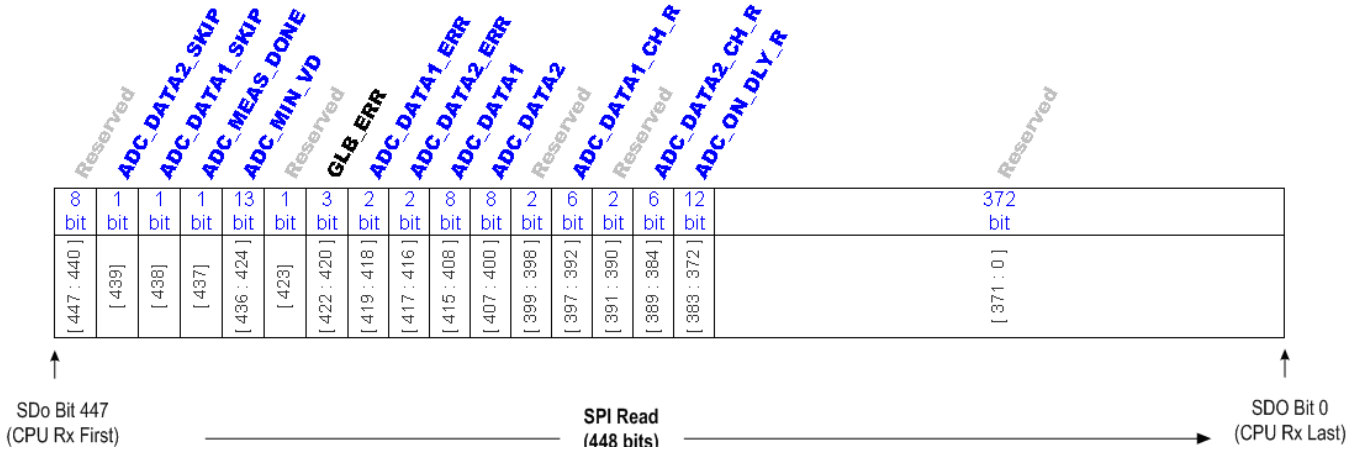


Figure 10 - DTC (Duty-Cycle) Read SPI Communication Packets

Table 4 - DTC Read Packet Bit Description Table

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
1	Reserved	Reserved. Value of this field has no meaning.	DTC Read	0-371	372	N/A
2	ADC_ON_DLY_R	Reports back the value written to ADC_ON_DLY register in CONFIG-Write packet (bit location 196-207).	DTC Read	372-383	12	0x03
3	ADC_DATA2_CH_R	Channel number indicated by this register is the channel used for ADC_DATA2 measurements. ADC_DATA2_CH_R reports channel number (0 to 31) or temperature (32) measured by ADC_DATA2. ADC_DATA2_CH_R is the channel number selected by ADC_DATA2_CH of the previous DTC-Write transaction. For more information see "Internal A/D Operation".	DTC Read	384-389	6	0x00
4	Reserved	Reserved. Value of this field has no meaning.	DTC Read	390-391	2	N/A
5	ADC_DATA1_CH_R	Channel number indicated by this register is the channel used for ADC1 measurements. ADC_DATA1_CH_R reports channel number (0 to 31) or temperature (32) measured by ADC1. ADC_DATA1_CH_R is the channel number selected by ADC_DATA1_CH of the previous DTC-Write transaction. For more information see "Internal A/D Operation".	DTC Read	392-397	6	0x00
6	Reserved	Reserved. Value of this field has no meaning.	DTC Read	398-399	2	N/A

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
7	ADC_DATA2	ADC_DATA2 measurement report. This field contains measurement value, and a valid bit. **Bit 0-6: ADC measurement value (bit location 400-406):** Value in these bits is the ADC measurement ADC_DATA2_CH_R register (bits 384-389). For ADC_DATA2_CH_R = **0 to 31**, the value that represents LX23108ILQ FET drain-voltage measurement connected to PWM channel specified by ADC_DATA2_CH_R: $$VD[V] = ADC\_DATA2[6:0] \cdot \frac{2V}{128}$$ These bits are read only. For ADC_DATA2_CH_R = **32,** the value that represents ADC measurement of LX24232ILQ temperature**:** $$LX24232ILQ\ Temp[°C] = 4.3427 \cdot ADC\_DATA2[6:0] - 273$$ **Bit 7 (bit location 407): valid bit** "0": ADC measurement bits 0-6 are invalid. Value should be ignored. "1": ADC measurement bits 0-6 are valid. This bit is cleared on read. **Note**: Since valid bit is of the "clear on read" type (RC), each SPI transaction clears this bit.	DTC Read	400-407	8	0x00
8	ADC_DATA1	ADC_DATA1 measurement report. This field contains measurement value, and a valid bit. **Bit 0-6: ADC measurement value (bit location 408 – 414):** Value in these bits is the ADC measurement ADC_DATA1_CH_R register (bits 384-389). For ADC_DATA1_CH_R = **0 to 31**, the value that represents LX23108ILQ FET drain-voltage measurement connected to PWM channel specified by ADC_DATA1_CH_R: $$VD[V] = ADC\_DATA1[6:0] \cdot \frac{2V}{128}$$ These bits are read only. For ADC_DATA1_CH_R = **32,** the value that represents ADC measurement of LX24232ILQ temperature**:** $$LX24232ILQ\ Temp[°C] = 4.3427 \cdot ADC\_DATA1[6:0] - 273$$ **Bit 7 (bit location 415): valid bit** "0": ADC measurement bits 0-6 are invalid. Value should be ignored. "1": ADC measurement bits 0-6 are valid. This bit is cleared on read. **Note**: Since valid bit is of the "clear on read" type (RC), each SPI transaction clears this bit.	DTC Read	408-415	8	0x00

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
9	ADC_DATA2_ERR	ADC_DATA2 Measurement Fault indications. **Bit 0 (bit location 416): Under Voltage fault** "0" – No faults. "1" – Under-Voltage Fault. When "1", ADC reading for channel number indicated by ADC_DATA2_CH_R register is below the value specified in ADC_UV register (CONFIG-Write packet, bits location 40-46). This Fault is used for indicating an open-string / LED disconnection fault condition. **Note**: a channel with under-voltage fault will not be included in the automatic search for minimum VD measurement. **Bit 1 (bit location 417): over temperature / over voltage fault:** "0" – No faults. "1" – Over Temperature / Over Voltage Fault. When "1", at least one of the following faults has occurred: 1. LX23108ILQ FET drain voltage connected to PWM channel indicated by ADC_DATA2_CH_R was above Short LED Detection level (8-10V, typical 8.8V) 2. An over-temperature event occurred in channel number indicated by ADC_DATA2_CH_R register. Setting bit 0 in GLB_CLR_ERR register (DTC-Write packet) to "1" clear both bits. **Note**: ADC_DATA2_ERR error is valid only in cases where valid bit (bit 7) of ADC_DATA2 register is set.	DTC Read	416-417	2	0x00
10	ADC_DATA1_ERR	ADC_DATA1 Measurement Fault indications. **Bit 0 (bit location 418): Under Voltage fault** "0" – No faults. "1" – Under-Voltage fault. When "1", ADC reading for channel number indicated by ADC_DATA1_CH_R register is below the value specified in ADC_UV register (CONFIG-Write packet, bits location 40-46). This Fault is used for indicating an open-string / LED disconnection fault condition. **Note**: a channel with under-voltage fault will not be included in the automatic search for minimum VD measurement. **Bit 1 (bit location 419): Over Temperature / Over Voltage fault:** "0" – No faults. "1" – Over Temperature / Over Voltage fault. When "1", at least one of the following faults has occurred: 1. LX23108ILQ FET drain voltage connected to PWM channel indicated by ADC_DATA1_CH_R was above the Short LED Detection level (8-10V, typical 8.8V) 2. An over-temperature event occurred in channel number indicated by ADC_DATA1_CH_R register. Setting bit 0 in GLB_CLR_ERR register (DTC-Write packet) to "1" clears both bits. **Note**: ADC_DATA1_ERR error is valid only in cases where the valid bit (bit 7) of ADC_DATA1 register is set.	DTC Read	418-419	2	0x00

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
11	GLB_ERR	Global Error Register. **Bit 0 (bit location 420): Global Under-Voltage** "0": No Faults. "1": Under-Voltage fault occurred in one of the channels. Setting bit 0 in *GLB_CLR_ERR* register to "1" clear this bit. **Bit 1 (bit location 421): Global Over-Temp / Over-Voltage** "0": No Faults. "1": Over-Voltage or Over-Temperature occurred in one of the channels Setting bit 0 in *GLB_CLR_ERR* register to "1" clear this bit. **Bit 2 (bit location 422): Global Skip indication:** "0" – Normal operation "1" – At least one of the 32 channels was not sampled by the internal ADC, due to a skip command. See *ADC_DATA1_SKIP* and *ADC_DATA2_SKIP* fields in this packet, bit location 438 and 439). This bit is updated automatically (set or cleared) by LX24232ILQ.	DTC Read	420-422	3	0x00
12	Reserved	Reserved	DTC Read	423	1	N/A

Field #	Register Name	Description	Trans. Type	Bit Location	Length (bits)	Reset Value
13	ADC_MIN_VD	**ADC Automatic minimum drain-voltage (VD) register.** This register has three fields: 1. Minimum drain voltage (VD) value (bits [6:0]) 2. Valid bit (bit [7]) 3. Channel number having the minimum VD voltage (bits [12:8]). **Bits 0-6 (bit location 424-430) minimum VD value** Setting bit 0 in ADC_RFVDMIN register to '1' sets bits 0-6 to 0x7F (highest value equivalent to 1.984V). LX24232ILQ continuously scans channels 0-31. Channel having the minimum VD (drain voltage) value (7 bit) is saved in ADC_MIN_VD[6:0]: $$\text{Minimum VD[V]} = \text{ADC\_MIN\_VD}[6:0] \cdot \frac{2\text{V}}{128}$$ **Note**: Minimum VD voltage is continuously with minimum VD measurement and updated by internal LX24232ILQ mechanism through automatically scanning channels 0 to 31. **Bit 7 (bit location 431): valid bit** 0: Minimum VD measurement bits are invalid 1: Minimum VD measurement bits are valid *Note 1:* Since valid bit is of the "**Clear on Read**" type (RC), each SPI transaction clears this bit. *Note 2:* Reading ADC_MIN_VD register before ADC_MEAS_DONE register (see next field) is set clears valid bit. *Note 3:* In cases where a valid bit is set during the time that ADC_RFVDMIN was set to '1' until ADC_MEAS_DONE become '1', consider adc_measure bits and channel bits as valid, regardless of valid bit 7 state. **Bits 8-12 (bit location 431-436): channel number** Value reported in this field indicates channel number (0 to 31) having the lowest FET VD reading.	DTC Read	424-436	13	0x7F
14	ADC_MEAS_DONE	ADC Measure Done indication. This bit indicates that "All enabled channels have been scanned". Setting bit 0 in ADC_RFVDMIN register (DTC-Write packet) clears this bit. This bit is set after all enabled channels (up to 32) are scanned by internal ADC. **Note**: This bit is set to "1" after all 32 channels have been scanned. Channels with ADC_SKIP bit set to "1" are skipped and not measured, but are part of the scan.	DTC Read	437	1	0x00