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High Performance LED Controller

Description

The LX27902 is a high performance LED controller optimized for LCD-TV and other LCD display systems and provides a cost competitive solution for off-PFC LED drive applications.

The controller provides a versatile solution for both DC power regulation and LED drive control within a single 24 pin IC chip. In addition, the power circuit architecture supported by LX27902 allows the designer to use a single power transformer and single primary switching stage with Microsemi's proprietary synchronous regulation technology to supply both the DC outputs and LED drive power, further saving the total cost of the power system.

The device provides on chip 5.25V output from VIN input with the working range of up to 27V.

The controller provides two sets of drive signals: AOUT and BOUT to drive a LLC switching stage, and COUT to drive a synchronous regulation stage, both with independent control loop. The drive format of COUT can be further configured by the voltage level of ENABLE signal to support either synchronous regulation operation or direct LED current control to satisfy a particular PWM dimming requirement.

In addition, a proprietary ACU_BRITE algorithm is incorporated in the dimming control operation to allow the user to adaptively adjust the PWM dimming duty to achieve accurate brightness control over a wide dimming duty cycle range while maintaining the highest operating efficiency.

It also provides analog LED current control to allow the system to change the LED current dynamically in real time to facilitate particular application requirement such as display mode switching between 2D and 3D. Direct PWM input dimming operation can be realized by inputting a dimming pulse train to DIM pin directly.

The synchronous regulation technology and ACU_BRITE algorithm changes the traditional approach in LED backlight control. The synchronous regulation scheme helps user to eliminate the DC-DC converter stage and ACU_BRITE algorithm maintains accurate brightness control without the need of a dimming control switch to turn on and off the LED current directly, providing the benefits of both cost saving and efficiency improvement without compromise of performance.

A versatile set of system monitoring and protection functions are also incorporated in the LX27902 design to provide reliable protection of the device and the system.

In addition the LX27902 supports standby power control thus providing a single system controller.

The device is available in 24 lead SOIC surface mount package in the industrial temperature range.

Features

- Single Chip to Support DC Output Regulation and LED Lighting Control
- Simplified Power Circuit Architecture with High Operating Efficiency and Reduced System Cost
- Supports Single Transformer Architecture for Regulated DC Output and LED Drive Without the Need for Secondary Side DC to DC Converter
- ACU_BRITE Algorithm Provides Accurate Brightness Control over Wide Dimming Duty Range Regardless the Circuit Topology and LED Current Wave Shape
- 0.6A Source & Sink Drive & On Chip 5.25V Regulator
- Input Supply Voltage up to 27V
- Versatile LED Current and Voltage Monitoring and Reliable Fault Detection and Protection
- Accurate LED Current Control Without Involvement of Dissipative Power Regulation Stage
- Robust Operation at Open and Short LED Conditions
- Dedicated Fault Indication Signal
- RoHS Compliant & Halogen Free

Applications

- LCD LED Backlight TV
- LCD LED Backlight Monitors
- Other LED Backlight Systems

Block Diagram

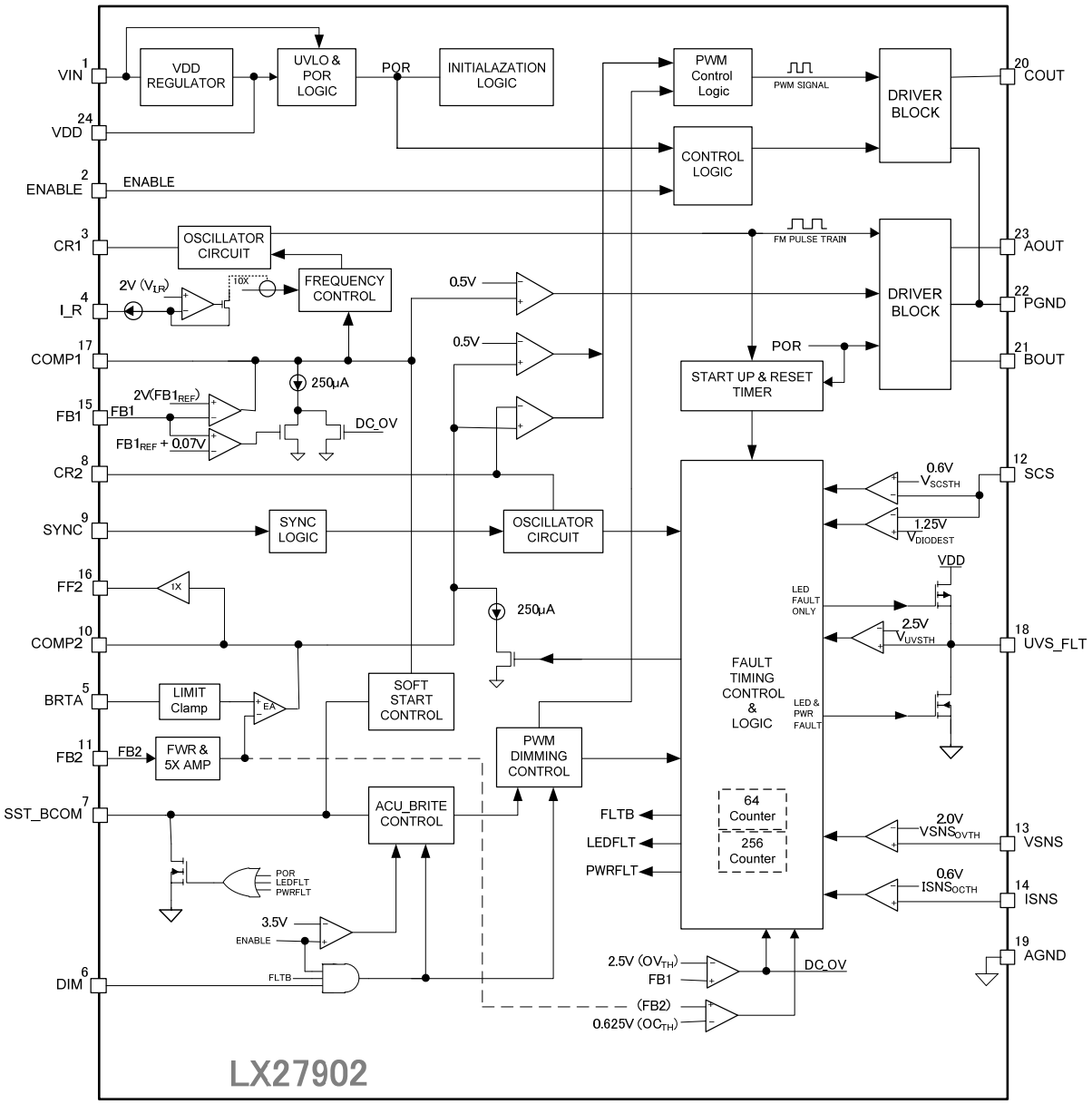


Figure 1 · Functional Block Diagram

Pin Configuration

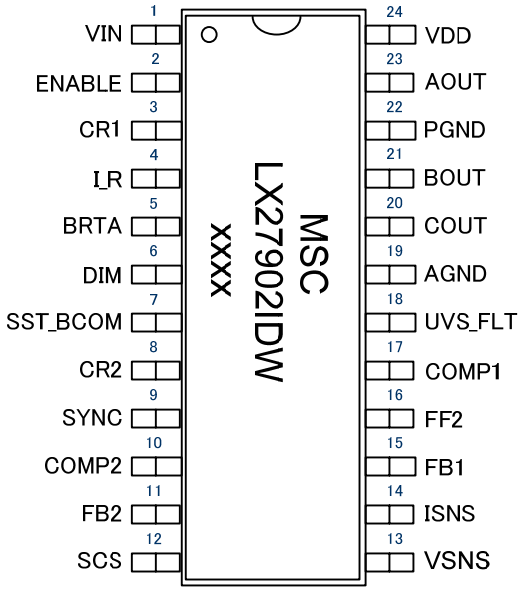


Figure 2 · Pinout

- Top view XX XX= Encoded date code
- 24 Pin Wide body SOIC package

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS2 compliant, Pb-free	SOIC24	LX27902IDW	Bulk / Tube
			LX27902IDW-TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	VIN	Input voltage pin. A built-in regulator is connected from this pin to supply a regulated voltage to VDD pin to feed the internal circuits. This pin can accept input voltage from 7.5V to 27V providing the flexibility of interfacing with either 12V or 24V system supplies. A low ESR decoupling capacitor of not less than 2.2µF should be connected from this pin to AGND with low impedance traces.
2	ENABLE	A signal >2V activates the LED operation of the controller. The DC signal level on this pin also sets the dimming operation mode. When 2V < V_{ENABLE} < 3.3V dimming operation is performed in ACU_BRITE dimming mode. When 3.7V < V_{ENABLE} < VDD dimming operation is performed in regular dimming mode. The dimming mode selection is active throughout the entire operation cycle of the controller.
3	CR1	Frequency programming terminal for LLC drive of AOUT and BOUT. A pull-up resistor from this pin to VDD, and a capacitor connected from this pin to AGND determines the operating frequency of the inverter. A frequency control circuit is connected to this pin internally for LLC modulation control.
4	I_R	Current source setting terminal for limiting the maximum switching frequency of AOUT and BOUT. A reference voltage of 2V is provided internally for setting the current with an external resistor.
5	BRTA	Terminal for programming the analog LED current setting. An analog signal is accepted from this pin to set the reference level for the LED current control loop. Effective operating range is 0.2V to 2V. A clamping circuit is built-in to limit the signal feeding to the internal circuit within the effective range.
6	DIM	PWM dimming control input. V_{DIM} > 2V sets the dimming operation in continuous analog mode. A PWM signal amplitude low level < 0.5V, high level > 2.0V will force the PWM dimming operation to follow the PWM signal directly. Input level <0.5V will stop the controller output.
7	SST_BCOM	ACU_BRITE dimming compensation and soft start. The elapsed dimming demand and the accumulated LED current over the active dimming period are compared at this pin and comparison result is used to control the LED light output to exactly match the dimming demand. Accurate LED dimming control is guaranteed with closed loop compensation for the distortions of the LED current during dimming operation. At start up this pin is connected to a 2µA charging current source to control the soft start process. An internal active clamping circuit is connected from this pin to COMP to force the COMP voltage to rise slowly with the charge of the capacitor at this pin. Soft start terminates when the voltage rises to 3V and the control enters normal operation mode. The 2µA charging source and the COMP pull down circuit are disconnected then, and this pin is connected to the ACU_BRITE circuit. Clamping the voltage of this pin below 3V will disable the ACU_BRITE compensation and the burst dimming control will follow the conventional PWM operation mode.
8	CR2	Ramp generation oscillator for COUT drive circuit. The frequency of the oscillator should be synchronized to the input signal from SYNC pin. A resistor from this pin to VDD and a capacitor from this pin to AGND sets the base frequency. The base frequency should be normally lower than the minimum operating frequency of CR1.
9	SYNC	Synchronization signal input pin. The frequency of CR2 oscillator is synchronized by the signal from this pin.

Pin Number	Pin Designator	Description
10	COMP2	Error amplifier output of the COUT drive loop. The error amplifier is a GM type that provides robust control behavior and simple compensation. The signal on this pin feeds to the PWM modulation circuit to control the drive output to regulate the LED current. In addition, a 250µA pull down current source is connected to this pin and will be activated when the VSNS signal >2V, LED over current or short circuit, or ENABLE signal is off. COUT will be shut off when COMP2 voltage drops below 0.5V.
11	FB2	Sense input for the COUT loop. The input signal at this pin is amplified by 5 times internally before feeding to the error amplifier to compare with the reference signal from BRTA pin. The amplified signal is also used to detect open LED, over current and short circuit conditions. The threshold for open LED is set to be 50% of the reference signal divided by 5, the threshold of over current is 600mV. The 8 bit fault counter will be activated when FB2 signal stays below the open lamp threshold or above the over current threshold and the fault flag will be asserted if the fault persists when the fault counter is full.
12	SCS	Short circuit sensing input for detection of short circuit conditions of the LED drive circuit. A protection action will be initiated to cut off the LED supply and activate the fault timing. The fault flag will be raised when the fault timing counter reaches full count.
13	VSNS	Voltage sense input pin. The sense signal at this pin feeds the over voltage detection circuit. A threshold of 2V is set internally for over voltage detection. When the VSNS signal reaches the threshold of 2V, the voltage regulation current source will be activated to pull down COMP2 to limit the amplitude of the voltage. Meanwhile, the fault monitoring circuit will start counting with an 8 bit fault counter and raise the fault flag when the fault counter is full.
14	ISNS	Current sense feedback of the power stage driven by AOUT, BOUT. A threshold of 0.6V is set internally as the over current protection limit with a negative current sense input. A 250µA internal current regulation source will be turned on to pull down the COMP1 signal at the instant the input signal drops below the 0.6V over current threshold. A fault flag will be raised when an over current event occurs 32 times consecutively and a soft start process will be initiated. The capacitor at the ST_BCOM pin will be discharged and COMP1 signal will be forced to rise together with the charge of the SST_BCOM capacitor until the voltage reaches 3V.
15	FB1	Sense feedback for AOUT, BOUT drive loop. The signal is compared with an internal reference of 2.0V for output regulation. This signal is also used to detect over voltage conditions. The threshold for over voltage detection is 2.5V. The fault counter will start counting when the over-voltage condition occurs. A fault flag will be asserted if the fault condition persists when the counter reaches 32 counts, and a soft start cycle will be initiated upon the assertion of the fault flag. A hysteresis control loop is also equipped with this pin to maintain the signal level at this pin between the reference level of 2V and upper limit of $FB1_{REF}$ +0.07V at standby or open load condition. The 250µA current source will be activated to pull down COMP1 signal when FB1 reaches the upper limit of $FB1_{REF}$ +0.07V.
16	FF2	This pin provides a compensation function to the AOUT, BOUT drive loop to enhance the cross regulation effect from the COUT drive loop operation.
17	COMP1	Output of the error amplifier of AOUT, BOUT drive loop. The error amplifier is a GM type that provides robust control behavior and simple compensation. The signal of this pin feeds to the LLC control circuit to regulate the DC output according to the feedback signal at FB1 pin. A 0.5V comparator is equipped at this pin to control the on/off of the LLC drive signal. AOUT and BOUT will

Pin Number	Pin Designator	Description
		be shut off when COMP1 voltage drops below 0.5V. Loop compensation is also provided by external components connected to this pin. The effective control range of COMP1 is 0.5V to 3V. The maximum voltage of this signal is clamped by an internal circuit to 3V.
18	UVS_FLT	Multi-function pin for under voltage detection and fault indication. At normal operation the sensed signal at this pin is compared with an internal reference of 2.5V, an internal fault counter will be triggered when the sensed signal drops below the 2.5V reference. A fault signal will be asserted when the fault counter reaches 256 counts. In addition, Fault conditions from other input signals are also asserted by changing the state of this pin, with active high indicates an LED fault and active low indicates a DC fault. Under other fault conditions the fault counter will also be triggered and assert a fault flag by pulling this pin down to ground when the counter reaches full count. The internal 2.5V comparator circuit will be disconnected from this pin when a fault is asserted.
19	AGND	Analog Ground return of the on chip control circuit. It is important to provide a low impedance ground plane to this pin and the signal control circuitry in PCB layout, and not let the ground return current of the power circuit flow through the signal ground plane. Low ESR bypass capacitors for VIN and VDD should be connected to this pin through ground traces with lowest possible impedance.
20	COUT	Gate signal to drive an external switch for LED current regulation and PWM dimming control. The signal is in synchronous with the CR2 oscillator frequency and can be configured as either leading edge or falling edge modulated signal by the voltage level at ENABLE pin.
21	BOUT	Gate drive outputs for LLC half bridge operation. These drive outputs are capable of providing 0.6A source and sink current at nominal operating voltage. Dead time is inserted to prevent possible shoot through at full duty cycle operation. Internal pull down resistors of 20kΩ is provided at each pin. The frequency of AOUT and BOUT is half of COUT and varies with the COMP1 signal level. The drive output always starts from AOUT and ends with BOUT.
23	AOUT	
22	PGND	Power Ground return of the on chip drive circuit. It is important to provide a low impedance ground plane to this pin and the power circuitry in PCB layout.
24	VDD	Internal 5.25V Regulator. A built-in regulator supplies a regulated 5.25V derived from VIN. A low ESR decoupling capacitor of not less than 2.2µF should be connected from this pin to AGND with low impedance traces.

Absolute Maximum Ratings

Parameter	Value	Units
Supply Input Voltage, VIN	-0.3 to 36	V
Signal Outputs, VDD, AOUT, BOUT, COUT	-0.3 to 6.5	V
Signal Inputs, CR1,CR2, BRTA,ISNS,VSNS,UVS_FLT, ENABLE, DIM, FB1,FB2,SYNC,SCS	-0.3 to VDD+0.3	V
Signal Outputs COMP1,COMP2,SST_BCOM,FF1,FF2	-0.3 to VDD	V
Maximum Junction Temperature	150	°C
Storage temperature range	-65 to 150	°C
Peak Package Solder Reflow Temperature (40 seconds maximum exposure)	260	°C
Lead Temperature. (Soldering 10 seconds)	300	°C
Operational ground slug temperature	0 to 70	°C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to AGND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability

Electrical Specifications

The following specifications apply over the operating ambient temperature of -40°C < T_A < 85°C, and VIN = 8V to 27V, except where otherwise noted and the following test conditions: VIN = 12V, C_{CR1} = 330pF, R_{CR1}= 15kΩ

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
POWER						
VIN	Controller Input voltage		8		27	V
VDD	Built-in 5.25V Regulator output Voltage	2.2µF bypass cap on VDD pin, I_{VDD} = 0 to 5mA	5.0	5.25	5.5	V
I_{IN}	VIN Supply Current	AOUT, BOUT = no load, COUT = off, T_A=25°C		4.7	6.5	mA
ENABLE						
EN_H	Enable On	COUT on , does not control AOUT/BOUT	2			V
EN_L	Shutdown	COUT off, does not control AOUT/BOUT			0.8	V
EN_{IIH}	Input High Current	V_{ENABLE} = 2V			10	µA
EN_{IIL}	Input low Current	0V < V_{ENABLE} <0.8V			5	µA
VEN_{ACU}	ACU_BRITE Mode		2		3.3	V
VEN_{NOR}	NORMAL BRITE Mode		3.7		VDD	V
Under Voltage Lock Out						
VDD_{UVLOH}	VDD Startup Threshold	Rising Threshold, Controller starts		4.28		V
VDD_{UVLOL}	VDD Lockout Threshold	Falling Threshold, Controller stops		3.55		V
VIN_{UVLOH}	VIN Startup Threshold	Rising Threshold	7.38	7.75	8.11	V
VIN_{UVLOL}	VIN Lockout Threshold	Falling Threshold	5.90	6.20	6.50	V
OUTPUT						
R_{SINK}	Output resistance AOUT& BOUT Sink	AOUT & BOUT, T_A = 25°C		6	8	Ω
R_{SOURCE}	Output Resistance AOUT& BOUT Source	AOUT & BOUT, T_A = 25°C		6	8	Ω
OUT_{DT}	Dead Time of AOUT, BOUT	T_A = 25°C, Full Duty	290	370	450	ns
R_{COUT}	COUT Output resistance	Sink and Source, T_A=25°C		15	18	Ω
$COUT_{DT}$	COUT Dead Time	C_{CR2} = 330pF,R_{CR2} = 18kΩ T_A = 25°C		260	310	ns
Switching Frequency Oscillator						
$OSCIN_{MIN}$	Minimum Switching Frequency Tolerance	T_A = 25°C, AOUT, BOUT	144	150	156	kHz
$I_{LLCRANGE}$	LLC Frequency Control Current Source Range		0		200	µA
R_{I_RRANGE}	Resistance RANGE of I_R		100		OEN	kΩ
I_{LLC}	LLC Frequency control current	R_{I_R} = 100 kΩ		200		µA
V_{I_R}	I_R reference voltage	I_{I_R} = 1mA (R_{I_R} = 2kΩ)	1.90	2.0	2.10	V
GI_{LLC}	I_{LLC}/I_{I_R} current Ratio	I_{LLC}/I_{I_R}		10		

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
OSCVV	Ramp Valley Voltage	CR1 pin		0.5		V
OSCPV	Ramp Peak Voltage	CR1 pin		2.5		V
F_{OSC}	Operating Frequency Range	GBD	5		500	kHz
LED Dimming Control						
$FB2_{REF}$	FB2 reference voltage	T_A = 25°C, positive & negative input, BRTA =2V	405	413	421	mV
	FB2 Linear Input Range	Positive Input	500			mV
	BRTA Input Range		0.2		2.0	V
I_{COMP2}	COMP2 (Error Amp) Current Source/Sink capacity			100		µA
$V_{COMP2OTH}$	COMP2 COUT turn off threshold	COUT OFF		0.5		V
V_{DIML}	DIM Input Low Threshold	LED current off			0.5	V
V_{DIMH}	DIM input High Threshold	LED current on	2.5		VDD	V
F_{DIMR}	DIM Frequency Range		50		100	Hz
LLC Regulation						
$FB1_{REF}$	FB1 Reference Voltage	T_A = 25°C, positive input	1.94	2.0	2.06	V
	FB1 Linear Input Range	From $FB1_{REF}$	1			V
I_{COMP1}	COMP1 (Error Amp) Current Source/Sink capacity			100		µA
$V_{COMP1OTH}$	COMP1 AOUT, BOUT Output Turn-off Threshold	AOUT, BOUT OFF		0.5		V
$FB1_{REFHYS}$	FB1 Hysteresis	T_A = 25°C, above $FB1_{REF}$		70	120	mV
FF_{DRV}	Feed Forward Drive Capacity	Output capacity from FF2		150		µA
FAULT MONITORING & PROTECTION						
$VSNS_{OVTH}$	VSNS threshold	Fault when V_{VSNS} > $VSNS_{OVTH}$	1.8	2.0	2.2	V
V_{COMP2L}	COMP2 Pull down level	when V_{VSNS} > $VSNS_{OVTH}$			0.4	V
I_{COMP2L}	COMP2 Pull down current	V_{VSNS} > $VSNS_{OVTH}$		250		µA
V_{UVSTH}	UVS threshold	Fault when V_{UVS} < V_{UVSTH}	2.3	2.5	2.7	V
	COMP1 Pull down level	V_{FB1} >$FB1_{REF}$+0.07V			0.4	V
	COMP1 Pull down current	V_{FB1}=$FB1_{REF}$+0.07V		250		µA
$ISNS_{OCTH}$	ISNS Over Current Threshold	Negative going	550	600	650	mV
UC_{TH}	Open LED Fault threshold			45%		V_{REF}
OC_{TH}	LED Over Current Threshold	Upper threshold of FB2	575	625	675	mV
V_{SCSTH}	LED Short Circuit Threshold	Negative going, SCS input	550	600	650	mV
$V_{DIODEST}$	Rectifier Short Threshold	Negative going, SCS input	1.10	1.25	1.40	V

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
OV_{TH}	Over voltage threshold	FB1 input	2.35	2.5	2.65	V
C_{PFC}	Power Fault Count	V_{UVS_FLT} <V_{UVSTH}		64		Count
C_{LFC}	LED Fault Count	LED open, short, OC		256		Count
FCT_{RESET}	Fault Counter Reset Interval	@ Clock of AOUT or BOUT		524288		Count
F_{SINK}	Fault Sink Current	VFAULT ≤ 0.8V, T_A = 25°C	3	4		mA
R_F	Fault Open Impedance	When in open state	5			MΩ
SOFT START CONTROL						
I_{SSC}	Soft Start Charging current	SST_BCOM		2		µA
V_{SSTTH}	Soft Start End Threshold			3		V
V_{COMP1C}	COMP1 Clamp level			3.5		V
POWER-UP SEQUENCING						
TPOR	Power On Reset Time		50			µs
TSTART	Start-Up Time Out	After POR, Clock of AOUT		32768		Count

Note: GBD Guaranteed by design, not production tested.

Characteristic Curves

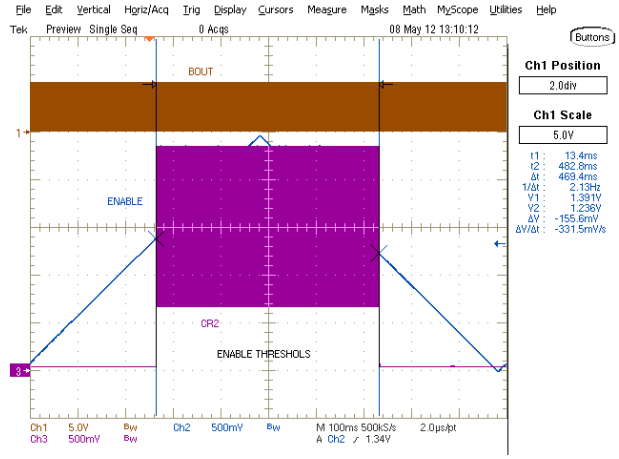


Figure 3 · Enable Threshold

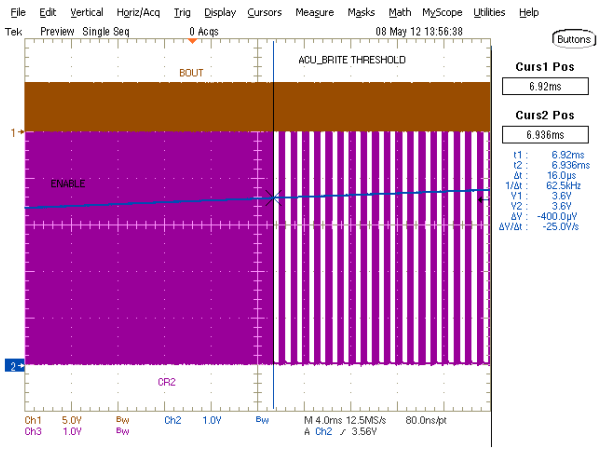


Figure 4 · ACU_BRITE Threshold

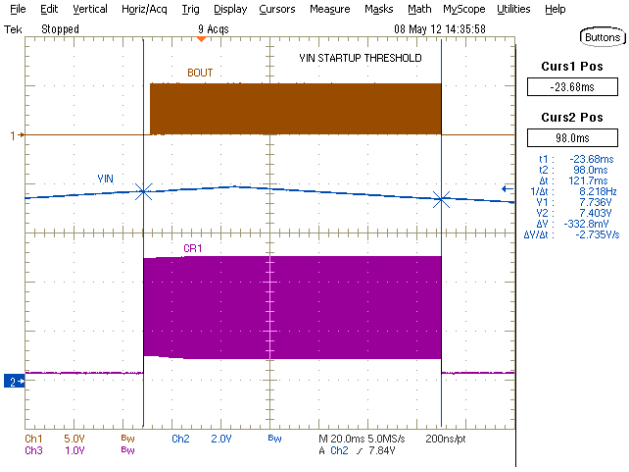


Figure 5 · VIN Startup Threshold

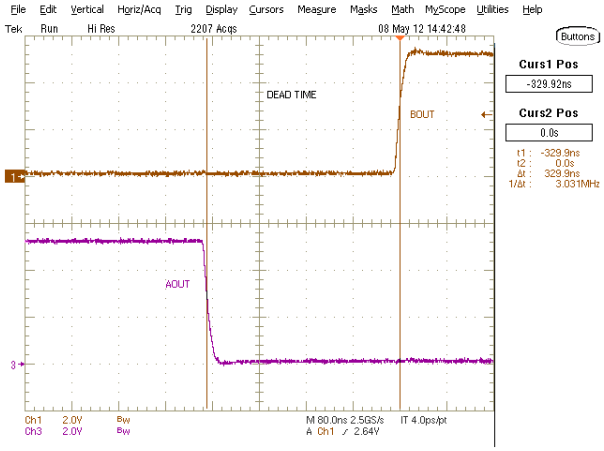


Figure 6 · Dead time between AOUT and BOUT

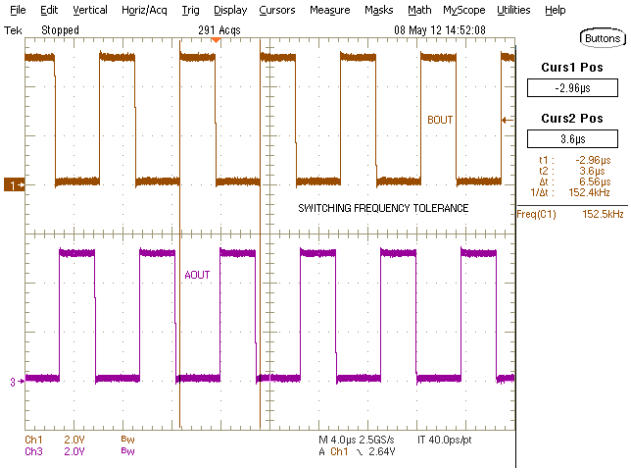


Figure 7 · Switching Frequency Tolerance

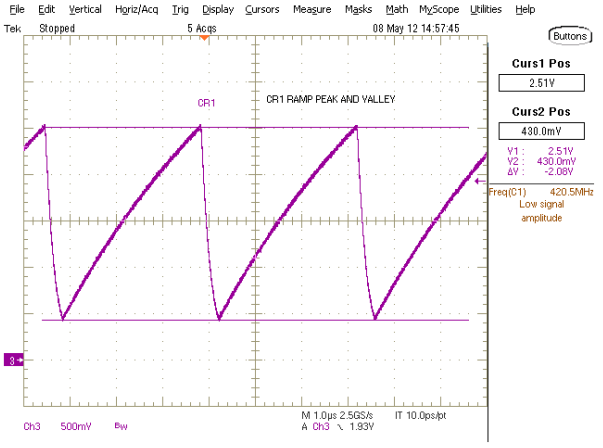


Figure 8 · Switching Frequency Tolerance

Characteristic Curves

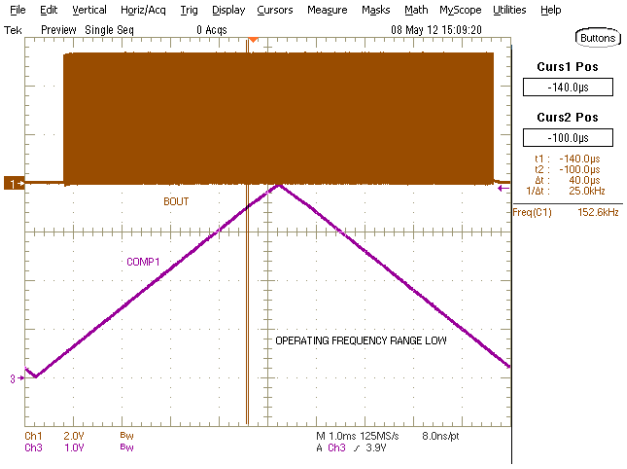


Figure 9 · Operating Frequency Range Low

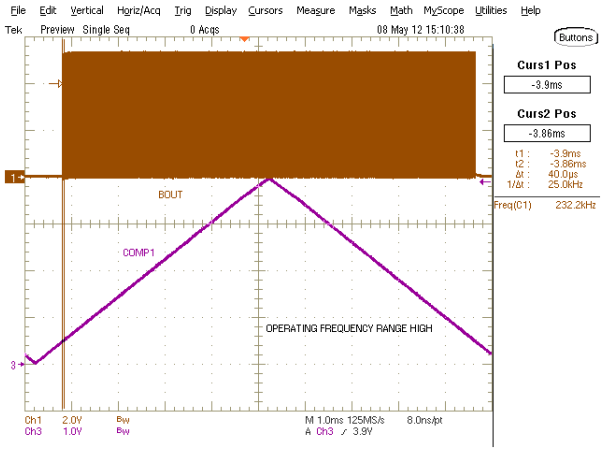


Figure 10 · Operating Frequency Range High

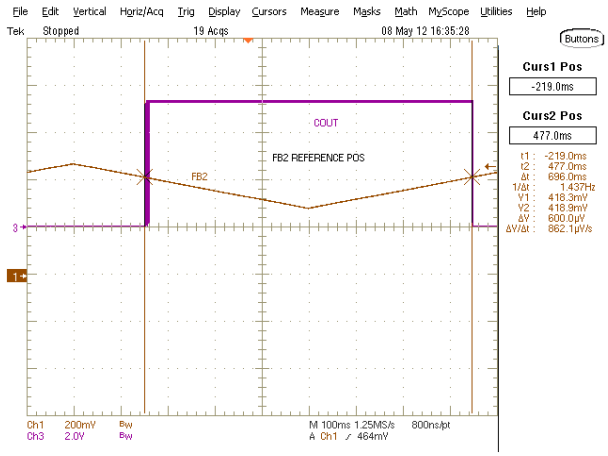


Figure 11 · FB2 Reference Positive

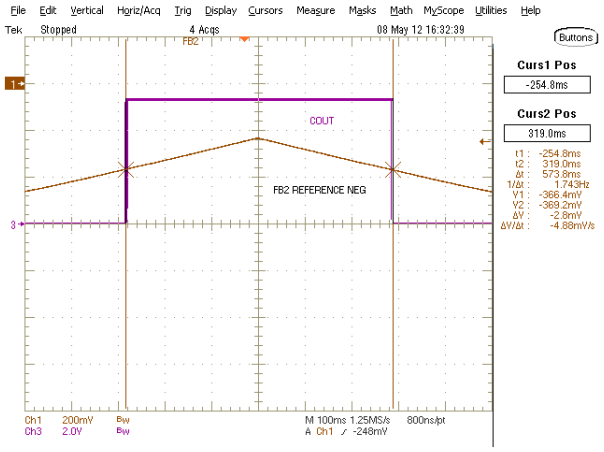


Figure 12 · FB2 Reference Negative

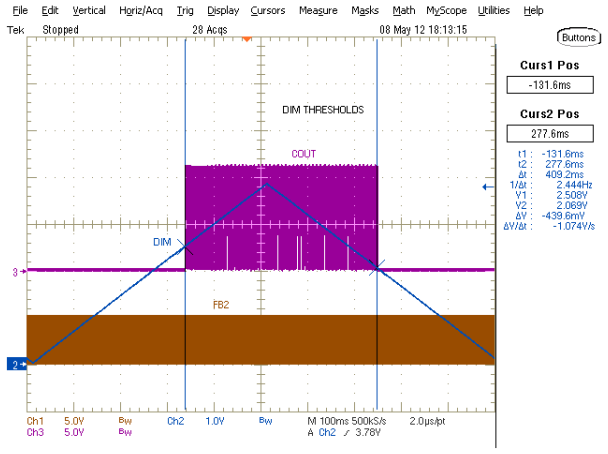


Figure 13 · Dim Thresholds

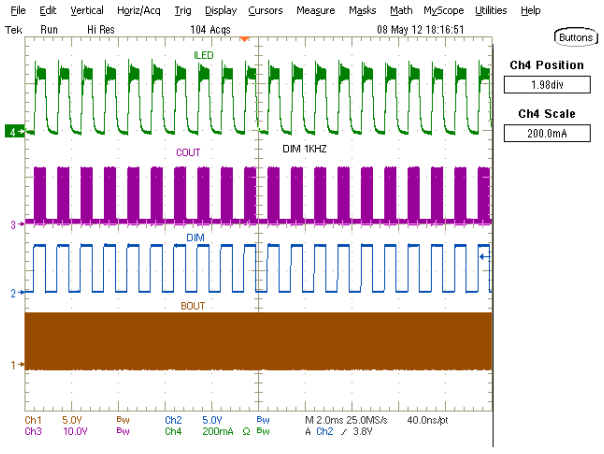


Figure 14 · DIM 1kHz

Characteristic Curves

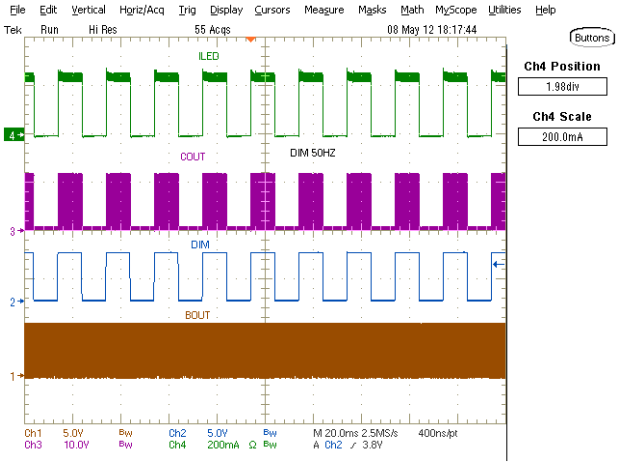


Figure 15 · DIM operation (50Hz)

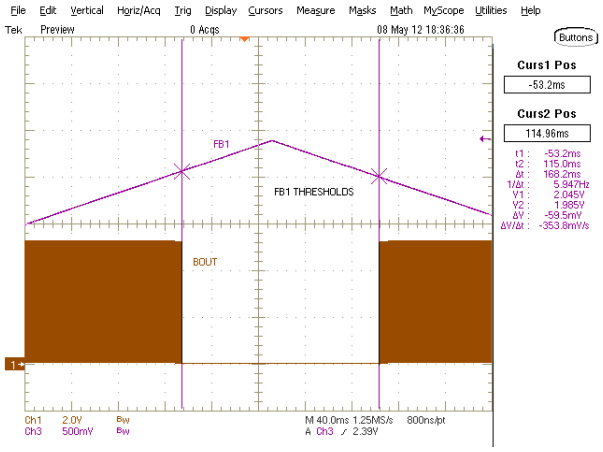


Figure 16 · FB1 Thresholds

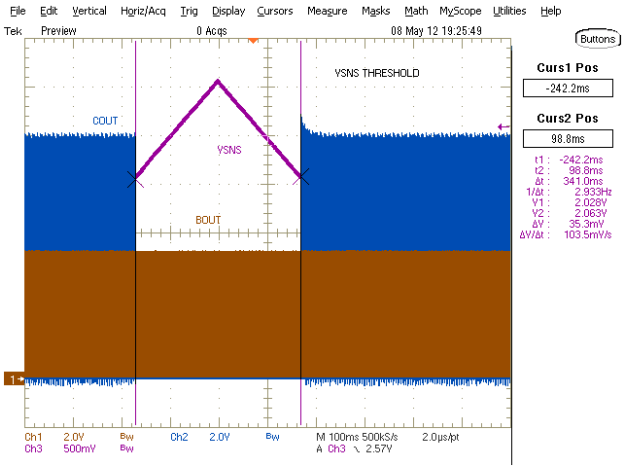


Figure 17 · VSNS Threshold

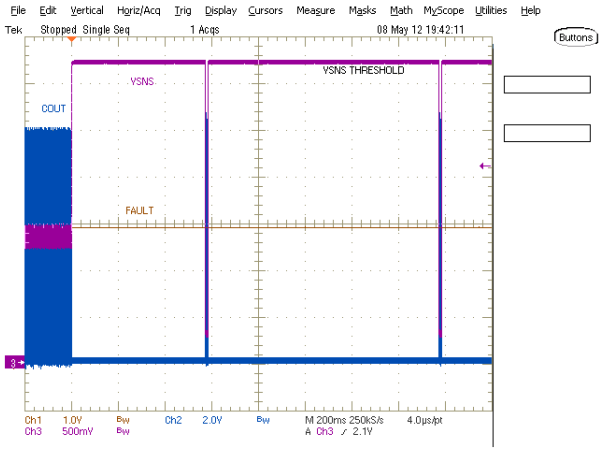


Figure 18 · VSNS Threshold No Fault

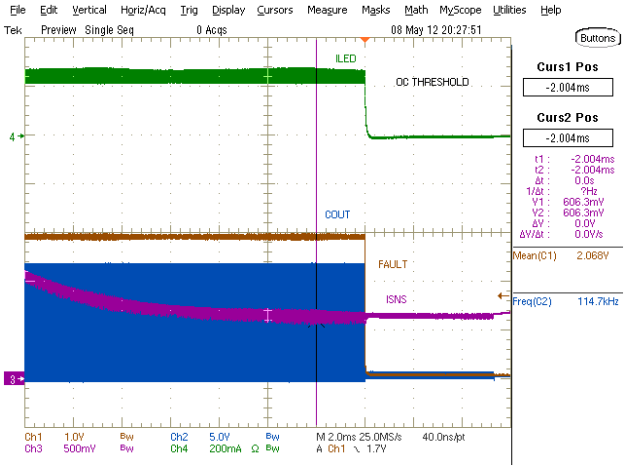


Figure 19 · OC Threshold

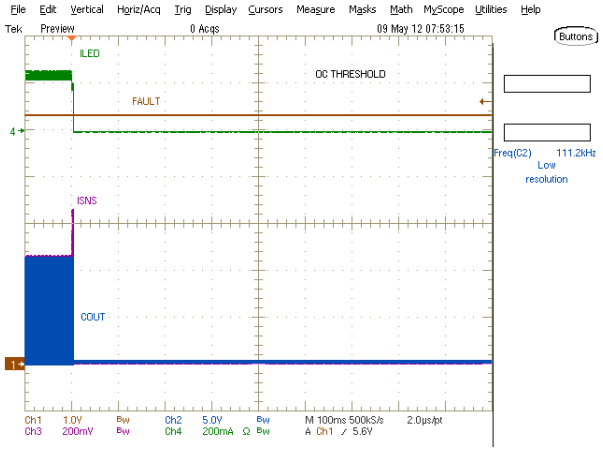


Figure 20 · OC Threshold

Characteristic Curves

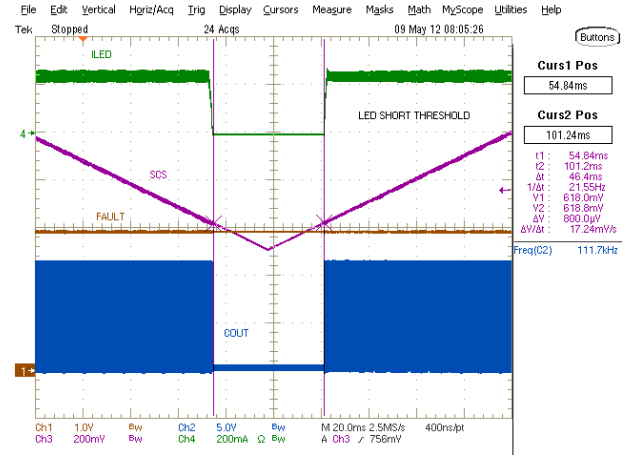


Figure 21 · LED Short Threshold

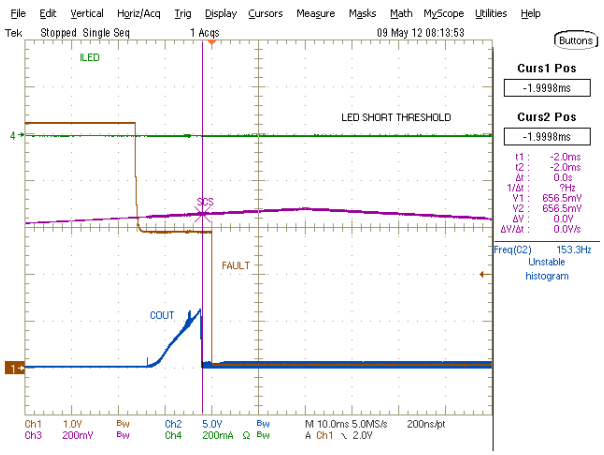


Figure 22 · LED Short Threshold

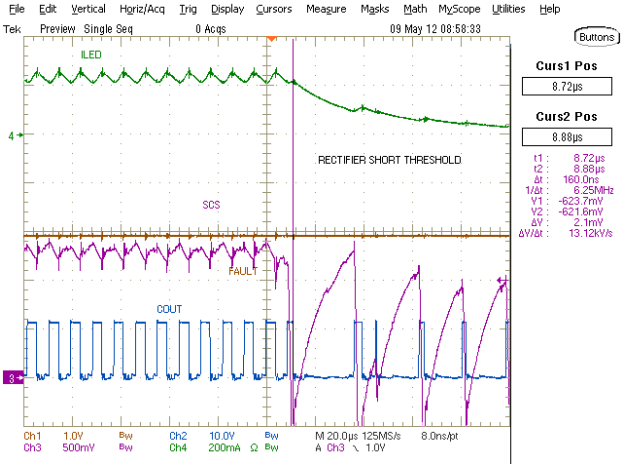


Figure 23 · Rectifier Short Threshold

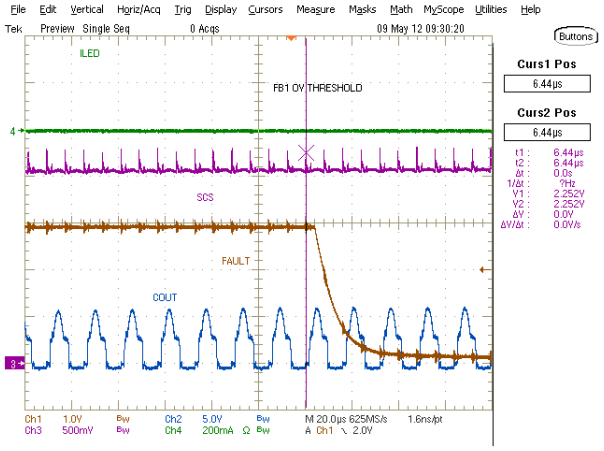


Figure 24 · FB1 OV Threshold

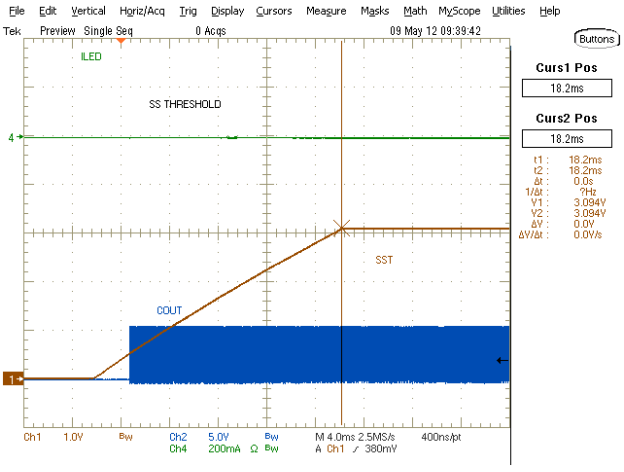


Figure 25 · SS Threshold

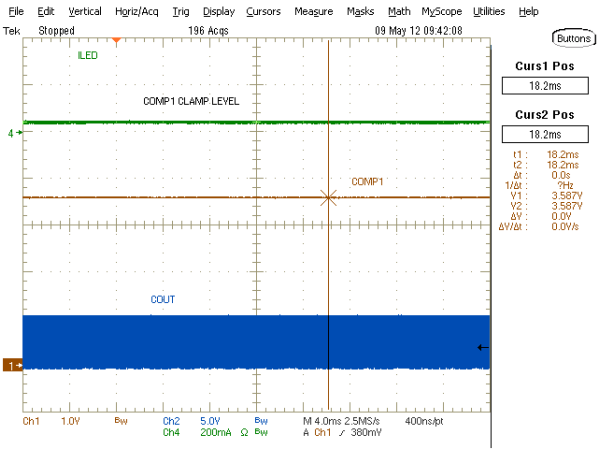


Figure 26 · COMP1 Clamp Level

Operation Description

INTRODUCTION

This section describes the operation of LX27902 LED drive controller. The LX27902 is primarily designed to provide a single chip, single power stage solution for LIPS power systems for LED backlit LCD TV and other large screen backlight applications that drive the DC outputs and LED backlight from a 400V PFC output across the safety isolation barrier. The dual loop control architecture offers an optimized low cost solution for such applications while providing a set of comprehensive system performance features to best address the design requirements of these applications.

1. SYSTEM OVERVIEW

The system contains the following main function blocks:

Power Control and Start-Up Logic

Oscillator and Frequency Control Circuit

DC Regulation Control Circuit

LED Control Circuit

Drive Control Circuitry

Fault Detection and Protection Circuitry

The power sequencing and start-up logic provides regulated power to the on-chip circuitry and controls the start-up sequencing, power on reset, and soft start operation etc. The oscillator and frequency logic generates the clock signals for the LLC and PWM operation and timing for operation and protection. The DC regulation logic controls the LLC operation of the AOUT, BOUT drive to regulate the DC output; the LED control circuit controls the LED current regulation and dimming operation through the COUT drive signal with Microsemi's proprietary synchronous regulation and ACU_BRITE technology to provide accurate brightness control with non-dissipative operation of the power devices. The drive control circuit converts the PWM signal from the regulation and control circuit to power drive signals to drive the external power devices of the power supply and LED dimming control. The fault detection and protection logic monitors the operation of the internal and external circuits and provides fault warning and protection for the system.

2. POWER CONTROL AND START UP

The LX27902 has a built-in regulator to step down the input voltage from VIN to a regulated 5.25V supply VDD to support the on chip circuitry. Because the controller is designed to support standby power, it turns on automatically whenever the input power is sufficient to support its operation. UVLO circuits are employed to monitor both the VIN and the VDD voltage. The UVLO circuit releases the lock out function when both VIN and VDD reach their rising thresholds and initiates the Power On Reset (POR) signal. A wide tolerance is allowed to set the VIN start up threshold to ensure a reliable start up at wide range of starting power conditions. The POR signal initializes the whole control circuitry by resetting the counters, registers, fault latches etc and discharging the soft start capacitor, while holding off the output signals to pre-determined inactive states. After the preset delay time the POR signal is released and the controller starts from a soft start operation of the DC output. Upon the completion of soft start the RUN flag is set and LED operation is activated when the ENABLE and DIM signal is present. During operation if the ENABLE signal is recycled or a recycle signal is generated from the 19 bit recycle counter, a reset signal is also generated to reset the fault counters and fault registers for a new start up sequence.

3. OSCILLATOR AND FREQUENCY CONTROL

The system has a built in switching frequency oscillator to provide a ramp signal and clock signal to the LLC drive circuit and the internal counters etc. A resistor connected between VDD and CR1 pin and a capacitor from CR1 pin to AGND sets the minimum operating frequency of AOUT, BOUT drive. A controlled charging current source set by I_R pin is also provided internally to the CR1 pin to adjust the oscillator frequency for LLC regulation control. In addition, a reference voltage of 2V is provided on I_R pin to allow the user to use an external resistor to set a current source value precisely to limit the maximum operating frequency of the LLC control circuit. Another oscillator circuit is provided at CR2 pin to control the COUT drive operation. A SYNC pin is dedicated to receive a synchronization signal to synchronize the frequency and phase of CR2 oscillation circuit. In actual applications the synchronization signal is normally from the secondary drive winding of the power transformer, so that the COUT drive signal can be synchronized with the output voltage of the power transformer.

4. DC REGULATION CONTROL

The DC regulation circuit regulates the DC output voltage through control loop tied to FB1 and COMP1. The signal from the error amplifier output COMP1 adjusts the operating frequency of AOUT and BOUT to maintain the output voltage with LLC regulation. The regulated DC voltage is sensed and fed to the FB1 pin as a feedback signal where it is regulated by matching the feedback signal with a 2V internal reference signal. The error amplifier is a GM type which is essentially a voltage controlled current source. The output of the error amplifier is tied to COMP1 pin to allow the user to adjust the compensation for the control loop with external components network. In addition, a shut down function is equipped with COMP1 signal. AOUT and BOUT will be shut down when COMP1 signal is dropped below 0.5V. This feature allows a fast protection and also a hysteretic voltage regulation operation at light or no load condition. Special attention should paid that in LLC mode operation the operating frequency of the drive signal should be always higher than the resonance frequency of the external power circuit in order to maintain stable operation of the system.

5. LED CONTROL

The LED regulation and dimming control is implemented with another control loop associated with CR2, SYNC, FB2, COMP2, BRTA, DIM and COUT pins. The LED current regulation is realized with a proprietary synchronous regulation technique. In this approach the COUT signal drives a switching device in series with the LED string(s) and the switching operation is synchronous with the signal fed to the SYNC pin in both frequency and phase. The LED current regulation is accomplished with a PWM modulation, where the turn-on or turn-off operation of the switching device can be synchronized with the drive voltage from the transformer or the switching action of the LLC stage. Such approach helps to reduce the system cost significantly with the elimination of a DC to DC conversion stage while improving the operating efficiency by eliminating the dissipative LED current regulation and minimizing the switching loss of the power device. The switching operation of COUT is controlled in falling edge modulation mode where the rising edge of the drive signal can be synchronous with the zero crossing point of the transformer voltage waveform to further minimize the switching losses.

In addition to current regulation capability, the burst dimming operation can also be realized by turning on and off the switching operation of COUT according to the burst dimming signal from DIM pin. In order to maintain dimming accuracy under the circumstance of finite rise and fall time of the LED current at the on/off edge of the dimming signal, a unique control algorithm called ACU_BRITE is incorporated to compensate the error caused by the distortion of LED current. The algorithm incorporates a closed integration outer loop compensation to ensure the dimming accuracy regardless the distortion of the LED current shape. A capacitor from SST_BCOM pin to ground provides dual functions of ACU_BRITE integration and soft start. In ACU_BRITE operation a controlled charging input current source and a controlled discharging current source are connected

internally to the SST_BCOM pin. The charging current source is linearly proportional to the internal LED current reference signal and is turned on and off by the input burst dimming signal. The discharging current source is proportional to the feedback signal from FB2 at the same ratio as the charging source to the internal reference. At power on reset the SST_BCOM capacitor is discharged to zero and the capacitor is used for soft start operation. When the capacitor voltage reaches 3V it switches over to ACU_BRITE dimming control function. The controlled charging and discharging current source matches their integration result over the SST_BCOM capacitor voltage. The voltage of SST_BCOM is fed to a comparator and compared with the threshold level of 3V to control the on and off of the dimming operation. When V_{SST_BCOM} is greater than 3V, the LED current is turned on, and when V_{SST_BCOM} is lower than 3V, the LED current is turned off. An accurate dimming control can thus be achieved by matching the integration of the charging and discharging current over each dimming cycle. Conventional dimming mode can also be selected by ENABLE voltage.

6. DRIVE CIRCUIT

The drive control circuit receives the logic drive signals and converts them to drive signals to drive external power devices directly from AOUT, BOUT and COUT pins. The signals from AOUT and BOUT are 180° out of phase and used to drive a half bridge or push-pull circuit. Since AOUT and BOUT are operating in LLC mode, they remain at near full duty all the time with the switching frequency varying according to the COMP1 signal level to adjust the DC power output.

Because the controller is designed to support stand-by power when the power system is in sleep mode, AOUT, BOUT can operate at burst mode by hysteretic control of COMP1 loop at light load. In order to avoid possible DC bias of the power transformer, care has been taken with the internal drive logic such that the AOUT and BOUT signal always output as a symmetrical pair starting from AOUT and ending with BOUT.

COUT provides drive signal for the external device for LED control. The drive signal is synchronous with the signal from SYNC pin. In actual applications the SYNC pin is normally fed with the output voltage from a secondary winding of the power transformer. The discharge of the saw tooth signal of the CR2 oscillator is synchronized by the zero crossing point of the SYNC input signal, and the turn on or turn off edge of COUT drive signal is synchronized to the discharge edge of CR2 signal, while its pulse width is modulated by the signal level of COMP2**.**

7. SOFT START AND POWER SEQUENCING

Soft start is accomplished by internal circuitry in combination with the SST_BCOM capacitor charging control. At power up the SST_BCOM capacitor is discharged to zero by POR signal. When the operation commences following POR pulse the SST_BCOM pin is disconnected from the dimming control circuit and a small soft start current source of 2 µA is turned on to charge the SST_BCOM capacitor slowly. The voltage of the SST_BCOM capacitor pulls down the COMP1 signal through the soft start circuit to force V_{COMP1} to rise slowly together with it. During this course the voltage amplitude of SST_BCOM is monitored by a level comparator. When the SST_BCOM signal rises to 3V, the soft start current source is turned off and the SST_BCOM pin switches over to the ACU_BRITE dimming control circuit. The COMP1 signal resumes its regulation function when SST_BCOM voltage reaches 3V, or when the FB1 signal reaches the internal reference of 2V during the slow charging of SST_BCOM capacitor. During the soft start, the LED operation is held off until SST_BCOM reaches 3V, an internal RUN flag is set upon completion of soft start and the LED operation is activated when the ENABLE and DIM signal are present.

During operation if the LED or the DC load is shut off due to a protection action, a 19 bit recycle counter will be activated. When the recycle counter reaches full count, the system will be reset to re-start the operation.

8. FAULT DETECTION AND PROTECTION

The following system operating conditions are monitored with fault report and protection actions from the following input signals:

1) LED string open from FB2;
2) LED over current from FB2;
3) LED over voltage from VSNS;
4) LED ground short from SCS;
5) Rectifier diode short from SCS;
6) DC over voltage from FB1;
7) DC over current or short circuit from ISNS.

Protection actions are determined according to the seriousness of the fault. When a LED open, LED over current or over voltage is detected, the operation of LED circuit from COUT drive is shut off and the recycle counter is activated to prepare for the re-start operation. When a LED ground short or a rectifier diode short is detected, the operation of the whole system including AOUT, BOUT and COUT is shut off to prevent power device failure.

Likewise, a two level protection is also incorporated with DC power faults. When a DC fault is detected, a fault counter is activated to count the fault time. When the counter reaches 64 counts, the UVS_FLT pin will be pulled low and the external circuit can use this signal to shut off the DC load and LED and in the meanwhile, the recycle counter is activated. If the fault is removed by shutting off the DC load, the system will re-start when the recycle counter reaches full count. However, if the fault persists after the DC load is shut off, a level 2 fault will be declared when the fault counter reaches 256 counts, and the operation of the whole system including AOUT, BOUT and COUT is shut down.

Because of the burst operation of LED dimming, a blanking counter of 15 counts is employed to blank the open LED detection at the rising edge of the burst dimming signal. If the open fault is detected after the blanking time is over, the LED fault counter will be activated and the fault flag will be raised when the counter reach full count of 256. The UVS_FLT pin will be pulled up to indicate an LED fault.

Application Description

Setting Operating Frequency

The minimum switching frequency of AOUT and BOUT is programmed with the external capacitor and resistor, R_{CR1} and C_{CR1} and I_R pin is opened.

$$f_{SW} \approx \frac{720000}{R_{CR1} \cdot C_{CR1}}$$

f_{SW} is the switching frequency in kHz, R_{CR1} is in kΩ, and C_{CR1} is in pF.

Normally C_{CR1} can be chosen from 220pF to 470pF, and the value of C_{CR1} can also be used to adjust the frequency control range in LLC mode.

Setting I_R Resistor

The maximum switching frequency of AOUT and BOUT is programmed with the external resistor, R_{I_R} connected to I_R pin and AGND. Maximum frequency range is controlled by current flowing thru I_R multiplied by 10. Maximum frequency is able to set up to 20μA of I_R pin.

The current can be calculated is: $I_{I\_R} = \frac{2000}{R_{I\_R}}$

Where , I_{I_R} is the current in μA, R_{CR1} is in kΩ

The minimum value of R_{CR1} is 100kΩ.

SETTING COMP1 PIN CAPACITOR

An external capacitor C_{COMP1} is connected from this pin to AGND to adjust loop response of the DC regulation module. The error amplifier is a GM type that provides robust control behavior and simple compensation. The ideal current error amplifier compensation depends on the output power.

If value of C_{COMP1} is small the gain will be increased and may result in overshoot, and the loop could become unstable. However as the capacitor value is increased it will reduce the gain and the loop response may be too slow. Therefore it is necessary to choose an optimal compensation method (Type 1, 2 or 3), typical recommended compensation method is Type 1, but should be selected depending on the application requirements.

SETTING COMP2 PIN CAPACITOR

An external capacitor C_{COMP2} is connected from this pin to AGND to adjust loop response of the LED regulation module. The error amplifier is a GM type that provides robust control behavior and simple compensation. The ideal current error amplifier compensation depends on the dimming mode operation range. If minimal dimming is required by the application the loop response can be slower, but for wide range digital dimming it must be fast enough to allow the lamp current to get to full amplitude within a few current cycles.

If value of C_{COMP2} is small the gain will be increased and may result in overshoot, and the loop could become unstable. However as the capacitor value is increased it will reduce the gain and the loop response may be too slow. Therefore it is necessary to choose an optimal value, typical recommended values range from 1nF to 10nF, but should be adjusted depending on the application requirements.

SETTING CR2 FREQUENCY

The switching frequency of COUT is programmed with the external capacitor and resistor, R_{CR2} and C_{CR2}. The frequency should be lower than minimum operating frequency set by CR1 pin.

Recommended part value are R_{CR2} = 1.1x R_{CR1}, and C_{CR2} = C_{CR1}

VIN, VDD BYPASS CAPACITOR

The LX27902 has internal Low Dropout Regulator to generate an accurate 5V supply for the internal control circuitry. In order to have stable operation, it is required to provide bypass capacitor with low ESR between both VIN and VDD and ground. It is recommended to use a capacitance of not less than 2.2μF for VIN and 2.2μF for VDD.

LAYOUT GUIDELINES

It is important to have a good PCB layout to achieve stable operation. Especially, high voltage section and the power switching section of the circuit layout require particular attention. High voltage section layout also needs to be planned carefully to meet Safety requirement as well as proper isolation from the control circuit. Following are guidelines for inverter PCB layout:

1) Use a star-ground connection for analog and power ground. Analog ground should be isolated from power ground except one connection point, GND pin.
2) Route high speed digital signal traces away from sensitive analog signals.

3) Place decoupling cap as close to related pin as possible.
4) Make shortest and direct connection from feedback sources.
5) Keep short and wide for high current signal paths especially ground.
6) Make trace as thick as possible.
7) Route current sense and voltage divider traces away from high voltage field.

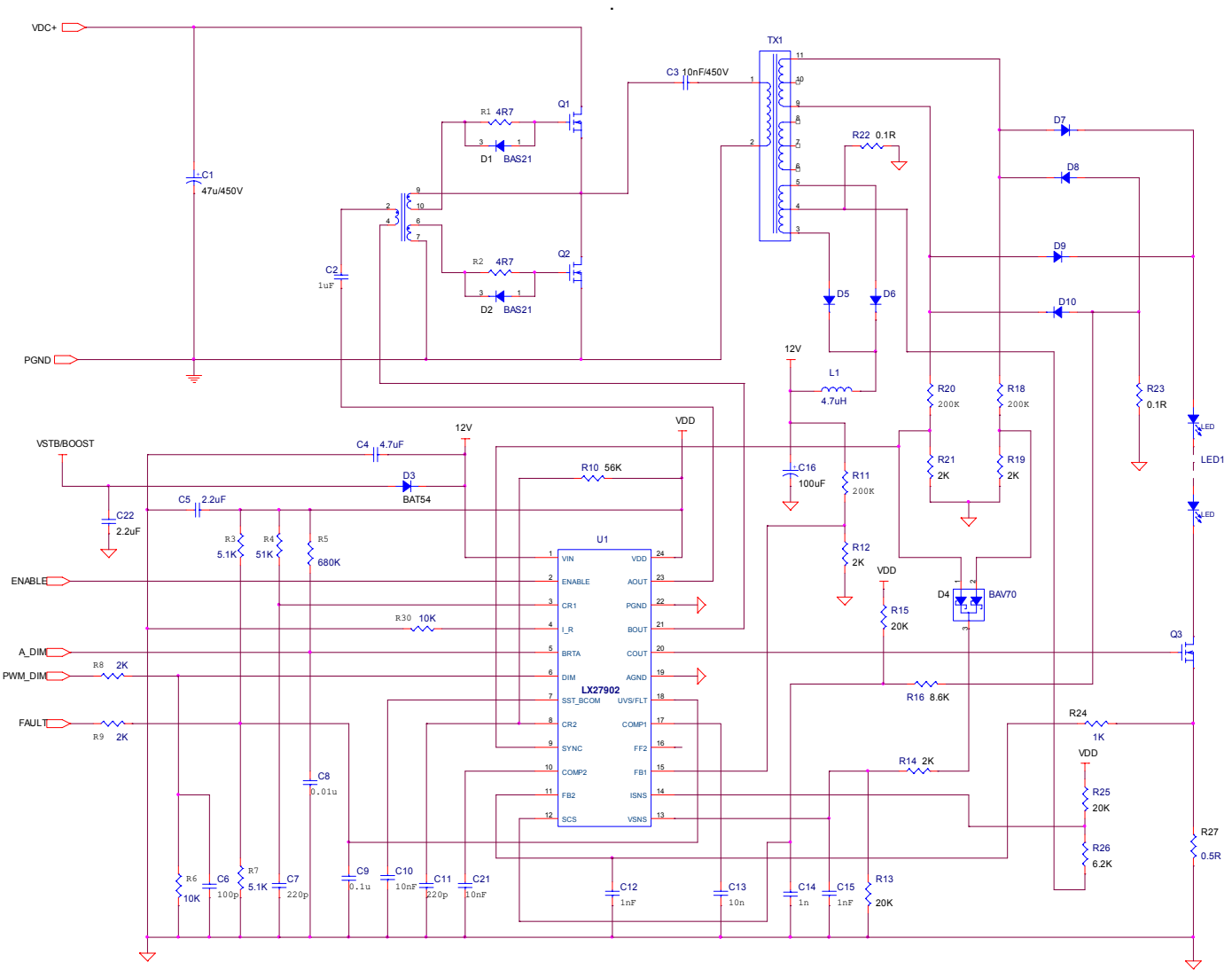


Figure 27 · Application Schematic

(The component values are for reference only, modifications may be necessary for a particular application requirement.)

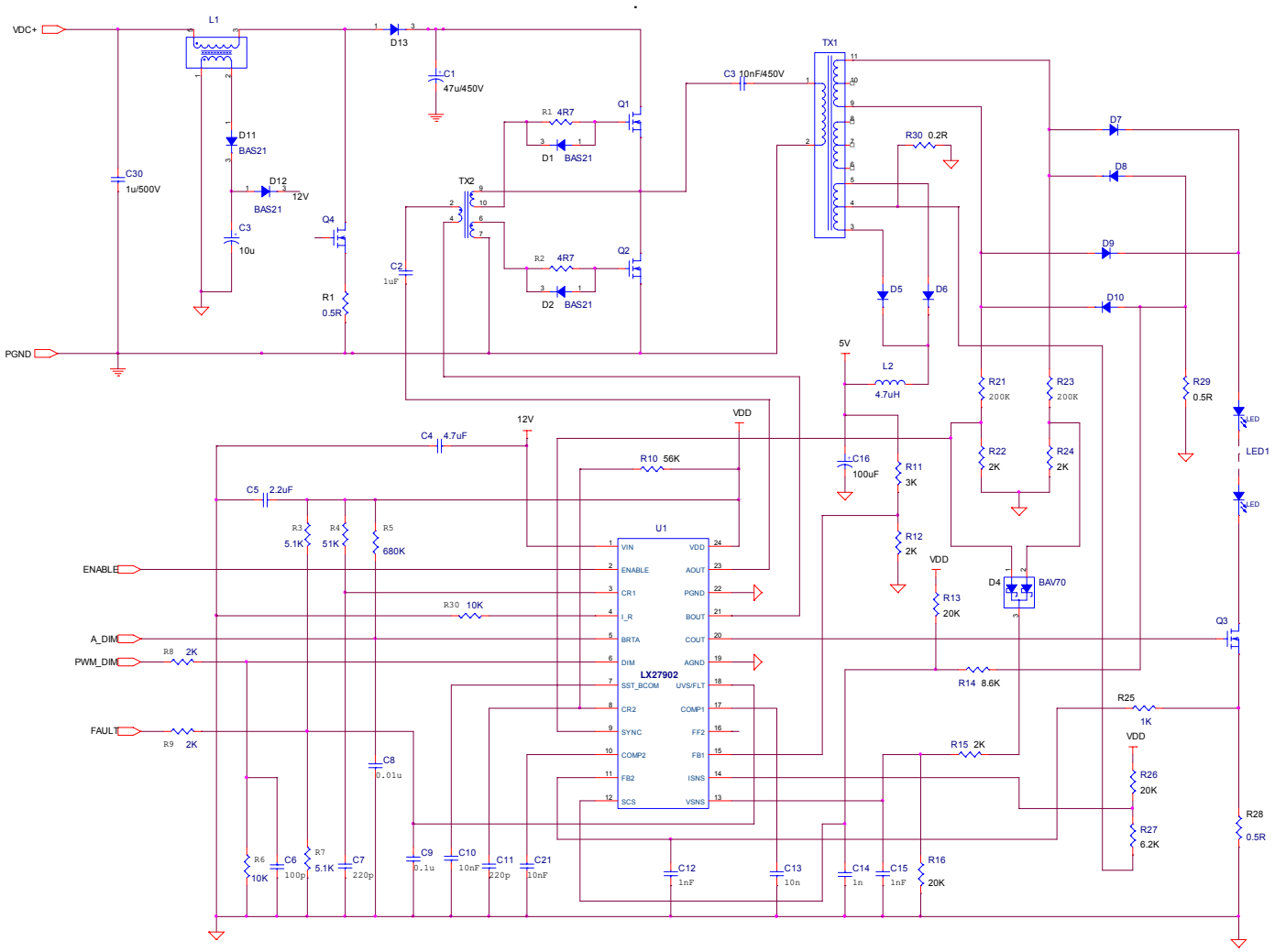
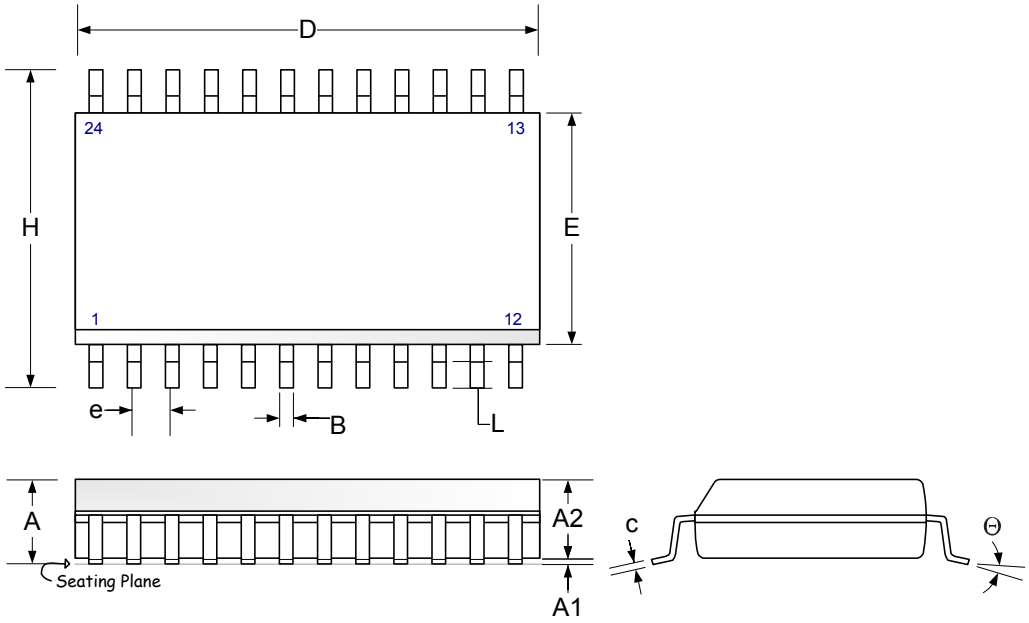


Figure 28 · Application Schematic, With Standby Power Management

(The component values are for reference only, modifications may be necessary for a particular application requirement.)

Package Outline Dimensions

The package is halogen free and meets RoHS2 and REACH standards.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
A2	2.20	2.55	0.086	0.100
B	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	15.20	15.57	0.598	0.613
E	7.40	7.60	0.291	0.299
e	1.27BSC		0.05 BSC	
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
Θ	0°	8°	0°	8°
*LC	-	0.10	-	0.004

*Lead Coplanarity

Figure 29 · 24-Pin Plastic Wide-body SOIC (SOWB) Package Dimensions

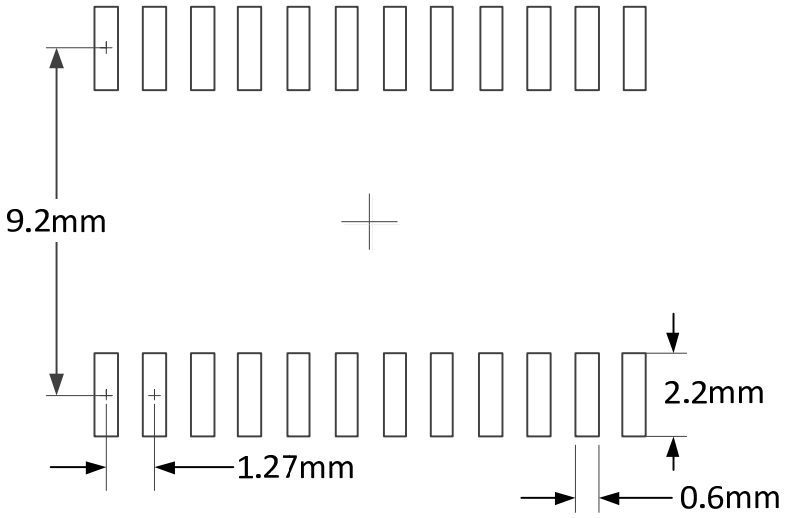


Figure 30 · PCB Layout Footprint (Top View)

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