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LX5261

27-Line LVD SCSI Source/Sink Regulator

PRODUCTION DATASHEET

DESCRIPTION

The LX5261 is a source/sink regulator designed to provide the correct reference voltages and bias currents for SCSI LVD applications. With the proper LVD termination network (475Ω, 121Ω, 475Ω), the LX5261 assures that LVD performance is compliant to the SPI-2 (Ultra2), SPI-3 (Ultra160) and SPI-4 (Ultra320) specification.

The LX5261 provides two fixed regulated outputs (1.75V and 0.75V) each capable of sourcing / sinking 200mA, along with a buffered 1.3V output for DIFSENS signaling.

The LX5261 features on-chip trimming of the internal voltage enabling precise output voltages; typically +/- 1% of its specified value. Thermal Shutdown and Current Limiting is integrated on-chip.

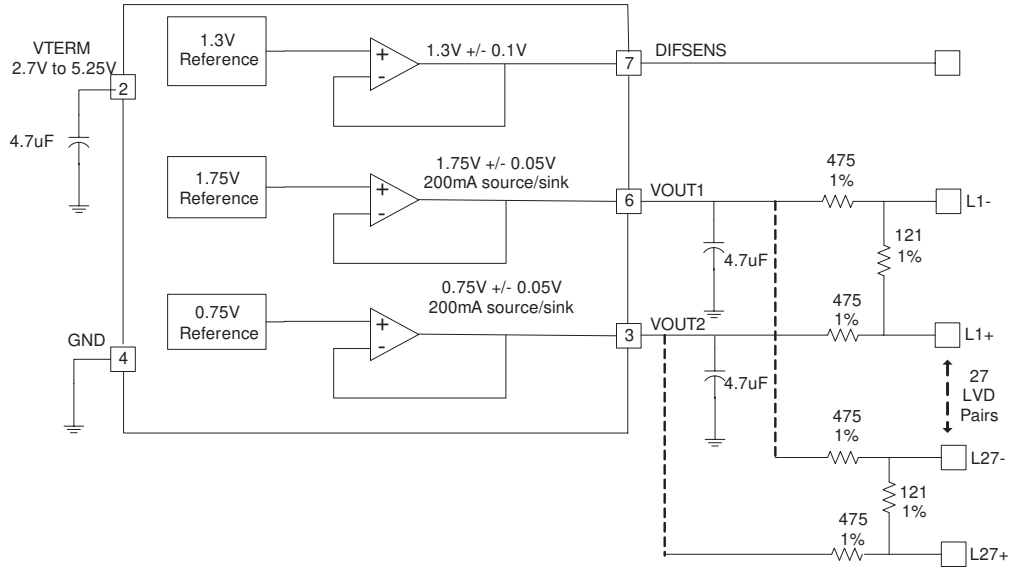
The LX5261 is available in the 16-pin SOIC (DP) package.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- Compliant with SPI-2 (Ultra2), SPI-3 (Ultra160), and SPI-4 (Ultra320)
- 2.7V to 5.25V Operation
- 200mA Source/Sink Capability
- DIFSENS Line Driver
- Current Limit and Thermal Protection
- Pin Compatible With Unitrode UCC561

TYPICAL APPLICATION



PACKAGE ORDER INFO

T_A (°C)	DP SOIC 16-Pin RoHS Compliant / Pb-free Transition DC: 0440
0 to 70	**LX5261CDP**

Note: Available in Tape & Reel.
Append the letters "TR" to the part number. (i.e. LX5261CDP-TR)

Rev. 1.0c, 2005-02-08

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ABSOLUTE MAXIMUM RATINGS

Term Power (VTERM) 6V
Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
RoHS / Pb-freePeak Package Solder Reflow Temperature
(40 second maximum exposure) ..... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

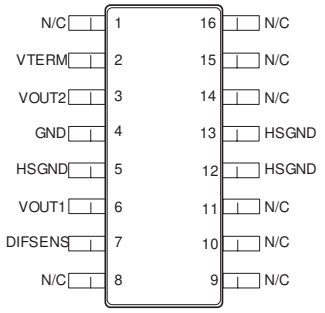
THERMAL DATA

DP 16-Pin SOIC

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	111.8 °C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow. θ_{JA} can vary significantly depending on mounting technique. (See Application Notes Section: Thermal considerations)

PACKAGE PIN OUT



DP PACKAGE
(Top View)
NC – No Internal Connection

RoHS / Pb-free 100% Matte Tin Lead Finish

FUNCTIONAL PIN DESCRIPTION

PIN NAME	DESCRIPTION
VOUT1	1.75V Regulated Output. Capable of sourcing/sinking 200mA.
VOUT2	0.75V Regulated Output. Capable of sourcing/sinking 200mA.
VTERM	Power supply pin for terminator. Connect to SCSI bus VTERM. Usually decoupled by one 4.7µF low-ESR capacitor. It is absolutely necessary to connect this pin to the decoupling capacitor through a very low impedance (big traces to PCB). Keeping distances very short from the decoupling capacitors is somewhat layout dependent and some applications may benefit from high frequency decoupling with 0.1µF capacitors at VTERM pin.
DIFSENS	1.3V buffered output for DIFSENS signaling.
GND	Regulator ground pin. Connect to ground.
HSGND	Attached to die mounting pad, but not bonded to GND pin. Pins should be considered a heat sink only, and not a true ground connection. It is recommended that these pins be connected to ground, but can be left floating.

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RECOMMENDED MAX OPERATING CONDITIONS

Parameter	Symbol	LX5261			Units
		Min	Typ	Max	
VTERM	V_{TERM}	2.7		5.25	V
Signal Line Voltage		0		5.0	V
Operating Junction Temperature	T_J	0		70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C, and V_{TERM} = 3.3V.

Parameter	Symbol	Test Conditions	LX5261			Units
			Min	Typ	Max	
TERMPWR Section						
VTERM Supply Current	I_{TERM}	No Load		35	40	mA
VTERM Voltage	V_{TERM}		2.7		5.25	V
Regulator Section						
1.75V Regulator	V_{REG1}	-125mA < I_{OUT} < 125mA, 2.7V < V_{IN} < 5.25V	1.7	1.75	1.8	V
1.3V Regulator	V_{DIFS}	DIFSENS; No Load	1.2	1.3	1.4	V
0.75V Regulator	V_{REG2}	-125mA < I_{OUT} < 125mA, 2.7V < V_{IN} < 5.25V	0.7	0.75	0.8	V
1.75V Regulator Source Current	I_{SRC1}	V_{OUT} = 1.25V			-200	mA
1.75V Regulator Sink Current	I_{SNK1}	V_{OUT} = 2.25V	200			mA
1.75V Source Current Limit			-700			mA
1.75V Sink Current Limit					700	mA
1.3V Regulator Source Current	I_{DIFS_SRC}	DIFSENS; 0V	-5		-15	mA
1.3V Regulator Sink Current	I_{DIFS_SNK}	DIFSENS = 2.4V	50		200	µA
0.75V Regulator Source Current	I_{SRC2}	V_{OUT} = 0.25V			-200	mA
0.75V Regulator Sink Current	I_{SNK2}	V_{OUT} = 1.25V	200			mA
0.75V Source Current Limit			-700			mA
0.75V Sink Current Limit					700	mA

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BLOCK DIAGRAM

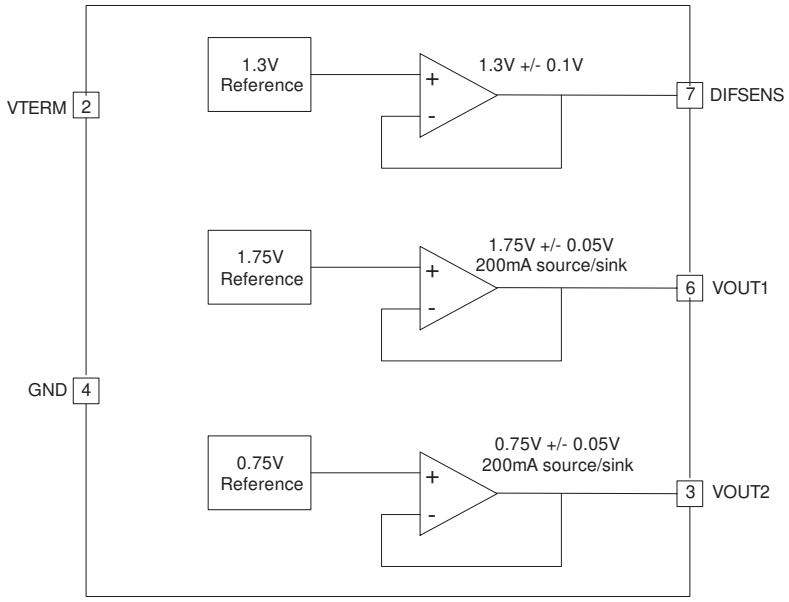
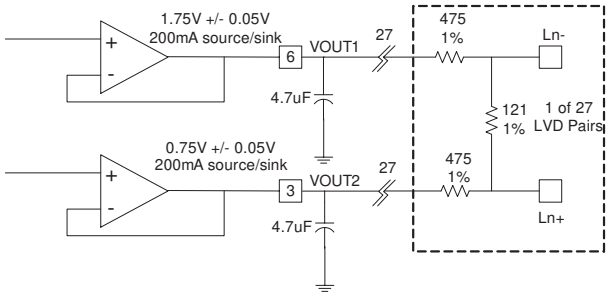


Figure 1 – LX5261 Block Diagram

APPLICATION INFORMATION

LVD SCSI with Resistor Stack

The LX5261 is used with a LVD resistor network (475Ω, 121Ω, 475Ω) to meet LVD SCSI performance. Connecting the top side of the LVD resistor network to the 1.75V regulated output ($V_{REG1,}$ pin 6), and the bottom side of the LVD resistor network to the 0.75 regulated output (V_{REG2}, pin 3) provides the correct bias voltage, differential impedance, common mode differential impedance, and common mode voltage required by the SPI-2 through SPI-4 SCSI specification (see Figure 2. below). The LX5261 is designed to drive up to 27 LVD pairs.



Parameter	LX5261	SCSI Standard	Units
Differential Impedance	107.3	100 to 110	ohm
Differential Bias Voltage	112.9	100 to 125	mV
Common Mode Impedance	237	100 to 300	ohm
Common Mode Voltage	1.25	1.2 to 1.3	V

Figure 2 – LX5261 with LVD Resistor Stack

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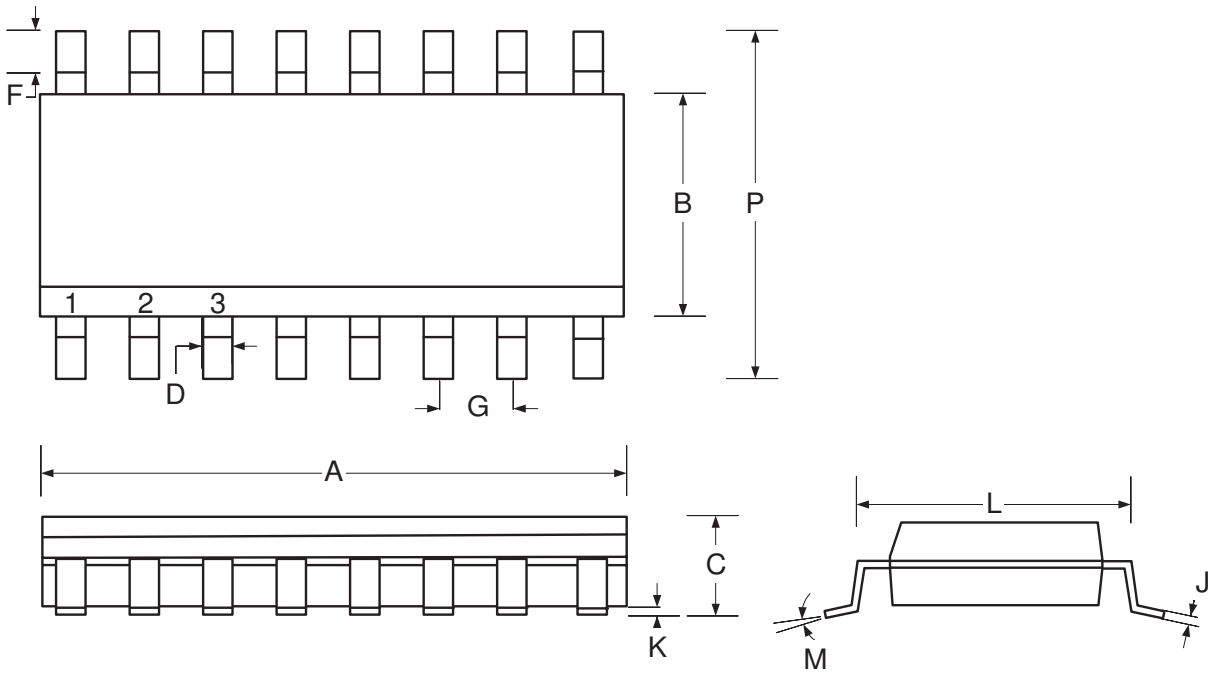
MECHANICAL DRAWINGS

DP 16-Pin Small Outline Package (SOIC) Narrow Body



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.01	0.385	0.394
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F		0.77		0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.007	0.010
K	0.10	0.25	0.004	0.010
L	4.82	5.21	0.189	0.205
M	0	8	0	8
P	5.79	6.20	0.228	0.244
*LC		0.10		0.004

Note:
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

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NOTES

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