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ispGDX2™ Device Datasheet

June 2010

Select Devices Discontinued!

Product Change Notifications (PCNs) #09-10 has been issued to discontinue select devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
LX64V	LX64V-3F100C	Active / Orderable	
	LX64V-3FN100C		
	LX64V-5F100C		
	LX64V-5FN100C		
LC64B	LX64B-3F100C	**Discontinued**	PCN#09-10
	LX64B-3FN100C		
	LX64B-5F100C		
	LX64B-5FN100C		
LX64C	LX64C-3F100C	**Discontinued**	PCN#09-10
	LX64C-3FN100C		
	LX64C-5F100C		
	LX64C-5FN100C		
LX128V	LX128V-32F208C	Active / Orderable	
	LX128V-32FN208C		
	LX128V-5F208C		
	LX128V-5FN208C		
LX128B	LX128B-32F208C	**Discontinued**	PCN#09-10
	LX128B-32FN208C		
	LX128B-5F208C		
	LX128B-5FN208C		
LX128C	LX128C-32F208C	**Discontinued**	PCN#09-10
	LX128C-32FN208C		
	LX128C-5F208C		
	LX128C-5FN208C		
LX256V	LX256V-35F484C	Active / Orderable	
	LX256V-35FN484C		
	LX256V-5F484C		
	LX256V-5FN484C		
LX256B	LX256B-35F484C	**Discontinued**	PCN#09-10
	LX256B-35FN484C		
	LX256B-5F484C		
	LX256B-5FN484C		

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Product Line	Ordering Part Number	Product Status	Reference PCN
LX256C	LX256C-35F484C	**Discontinued**	PCN#09-10
	LX256C-35FN484C		
	LX256C-5F484C		
	LX256C-5FN484C		
LX64EV	LX64EV-3F100C	Active / Orderable	
	LX64EV-3FN100C		
	LX64EV-5F100C		
	LX64EV-5F100I		
	LX64EV-5FN100C		
	LX64EV-5FN100I		
LX64EB	LX64EB-3F100C	**Discontinued**	PCN#09-10
	LX64EB-3FN100C		
	LX64EB-5F100C		
	LX64EB-5F100I		
	LX64EB-5FN100C		
	LX64EB-5FN100I		
LX64EC	LX64EC-3F100C	**Discontinued**	PCN#09-10
	LX64EC-3FN100C		
	LX64EC-5F100C		
	LX64EC-5F100I		
	LX64EC-5FN100C		
	LX64EC-5FN100I		
LX128EV	LX128EV-32F208C	Active / Orderable	
	LX128EV-32FN208C		
	LX128EV-5F208C		
	LX128EV-5F208I		
	LX128EV-5FN208C		
	LX128EV-5FN208I		
LX128EB	LX128EB-32F208C	**Discontinued**	PCN#09-10
	LX128EB-32FN208C		
	LX128EB-5F208C		
	LX128EB-5F208I		
	LX128EB-5FN208C		
	LX128EB-5FN208I		
LX128EC	LX128EC-32F208C	**Discontinued**	PCN#09-10
	LX128EC-32FN208C		
	LX128EC-5F208C		
	LX128EC-5F208I		
	LX128EC-5FN208C		
	LX128EC-5FN208I		
LX256EV	LX256EV-35F484C	Active / Orderable	
	LX256EV-35FN484C		
	LX256EV-5F484C		
	LX256EV-5F484I		
	LX256EV-5FN484C		
	LX256EV-5FN484I		

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Product Line	Ordering Part Number	Product Status	Reference PCN
LX256EB	LX256EB-35F484C	**Discontinued**	PCN#09-10
	LX256EB-35FN484C		
	LX256EB-5F484C		
	LX256EB-5F484I		
	LX256EB-5FN484C		
	LX256EB-5FN484I		
LX256EC	LX256EC-35F484C	**Discontinued**	PCN#09-10
	LX256EC-35FN484C		
	LX256EC-5F484C		
	LX256EC-5F484I		
	LX256EC-5FN484C		
	LX256EC-5FN484I		

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ispGDX2™ Family

High Performance Interfacing and Switching

Includes High-Performance, Low-Cost "E-Series"

September 2005

Data Sheet

Features

High Performance Bus Switching

- High bandwidth
  - Up to 12.8 Gbps (SERDES)
  - Up to 38 Gbps (without SERDES)
- Up to 16 (15x10) FIFOs for data buffering
- High speed performance
  - f_{MAX} = 360MHz
  - t_{PD} = 3.0ns
  - t_{CO} = 2.9ns
  - t_S = 2.0ns
- Built-in programmable control logic capability
- I/O intensive: 64 to 256 I/Os
- Expanded MUX capability up to 188:1 MUX

sysCLOCK™ PLL

- Frequency synthesis and skew management
- Clock multiply and divide capability
- Clock shifting up to +/-2.35ns in 335ps steps
- Up to four PLLs

sysIO™ Interfacing

- LVCMOS 1.8, 2.5, 3.3 and LVTTL support for standard board interfaces
- SSTL 2/3 Class I and II support
- HSTL Class I, III and IV support
- GTL+, PCI-X for bus interfaces
- LVPECL, LVDS and Bus LVDS differential support
- Hot socketing
- Programmable drive strength

Two Options Available

- High-performance sysHSI (standard part number)
- Low-cost, no sysHSI ("E-Series")

sysHSI Blocks Provide up to 16 High-speed Channels

- Serializer/de-serializer (SERDES) included
- Clock Data Recovery (CDR) built in
- 800 Mbps per channel
- LVDS differential support
- 10B/12B support
  - Encoding / decoding
  - Bit alignment
  - Symbol alignment
- 8B/10B support
  - Bit alignment
  - Symbol alignment
- Source Synchronous support

Flexible Programming and Testing

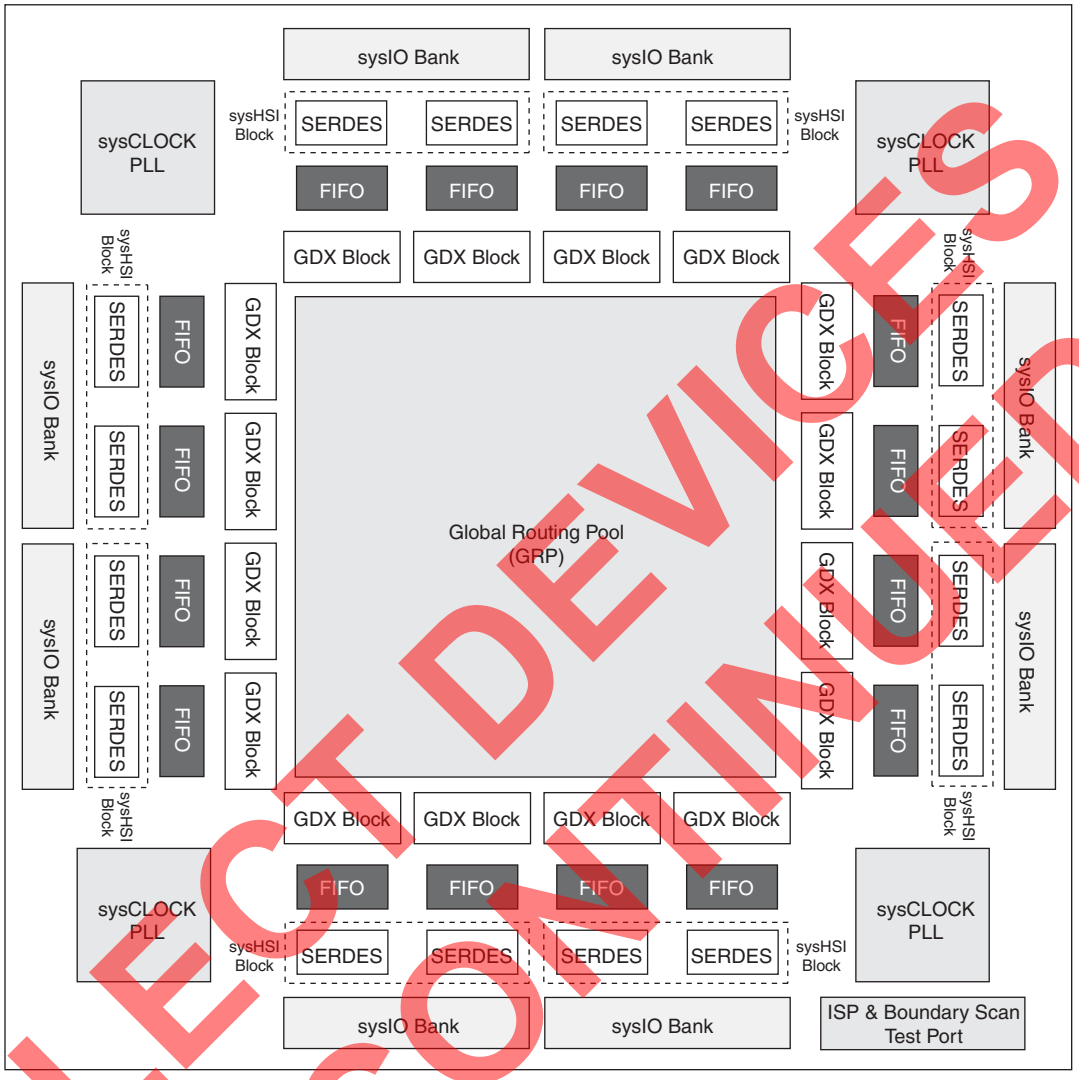
- IEEE 1532 compliant In-System Programmability (ISP™)
- Boundary scan test through IEEE 1149.1 interface
- 3.3V, 2.5V or 1.8V power supplies
- 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces

Table 1. ispGDX2 Family Selection Guide

		ispGDX2-64/E	ispGDX2-128/E	ispGDX2-256/E
I/Os		64	128	256
GDX Blocks		4	8	16
t_{PD}		3.0ns	3.2ns	3.5ns
t_S		2.0ns	2.0ns	2.0ns
t_{CO}		2.9ns	3.1ns	3.2ns
f_{MAX} (Toggle)		360MHz	330MHz	300MHz
Max Bandwidth	SERDES[1, 2]	3.2Gbps	6.4Gbps	12.8Gbps
	Without SERDES[3]	11Gbps	21Gbps	38Gbps
sysHSI Channels[2]		4	8	16
LVDS/Bus LVDS (Pairs)		32	64	128
PLLs		2	2	4
Package		100-ball fpBGA	208-ball fpBGA	484-ball fpBGA

1. Max number of SERDES channels per device * 800Mbps
2. "E-Series" does not support sysHSI.
3. f_{MAX} (Toggle) * maximum I/Os divided by 2.

Figure 1. ispGDX2 Block Diagram (256-I/O Device)



Introduction

The ispGDX2™ family is Lattice's second generation in-system programmable generic digital crosspoint switch for high speed bus switching and interface applications.

The ispGDX2 family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications while the lower-cost "E-series" supports the same high-performance FPGA fabric without the sysHSI Block.

This family of switches combines a flexible switching architecture with advanced sysIO interfaces including high performance sysHSI Blocks, and sysCLOCK PLLs to meet the needs of the today's high-speed systems. Through a muliplexer-intensive architecture, the ispGDX2 facilitates a variety of common switching functions.

The availability of on-chip control logic further enhances the power of these devices. A high-performance solution, the family supports bandwidth up to 38Gbps.

Every device in the family has a number of PLLs to provide the system designer with the ability to generate multiple clocks and manage clock skews in their systems.

The sysIO interfaces provide system-level performance and integration. These I/Os support various modes of LVCMOS/LVTTL and support popular high-speed standard interfaces such as GTL+, PCI-X, HSTL, SSTL, LVDS and Bus-LVDS. The sysHSI Blocks further extend this capability by providing high speed serial data transfer capability.

Devices in the family can operate at 3.3V, 2.5V or 1.8V core voltages and can be programmed in-system via an IEEE 1149.1 interface that is compliant with the IEEE 1532 standard. Voltages required for the I/O buffers are independent of the core voltage supply. This further enhances the flexibility of this family in system designs.

Typical applications for the ispGDX2 include multi-port multi-processor interfaces, wide data and address bus multiplexing, programmable control signal routing and programmable bus interfaces. Table 1 shows the members of the ispGDX2 family and their key features.

Architecture

The ispGDX2 devices consist of GDX Blocks interconnected by a Global Routing Pool (GRP). Signals interface with the external system via sysIO banks. In addition, each GDX Block is associated with a FIFO and a sysHSI Block to facilitate the transfer of data on- and off-chip. Figure 1 shows the ispGDX2 block diagram. Each GDX Block can be individually configured in one of four modes:

- Basic (No FIFO or SERDES)
- FIFO Only
- SERDES Only
- SERDES and FIFO

Each sysIO bank has its own I/O power supply and reference voltage. Designers can use any output standard within a bank that is compatible with the power supply. Any input standard may be used, providing it is compatible with the reference voltage. The banks are independent.

Global Routing Pool (GRP)

The ispGDX2 architecture is organized into GDX Blocks, which are connected via a Global Routing Pool. The innovative GRP is optimized for routability, flexibility and speed. All the signals enter via the GDX Block. The block supplies these either directly or in registered form to the GRP. The GRP routes the signals to different blocks, and provides separate data and control routing. The data path is optimized to achieve faster speed and routing flexibility for nibble oriented signals. The control routing is optimized to provide high-speed bit oriented routing of control signals.

There are some restrictions on the allocation of pins for optimal bus routing. These restrictions are considered by the software in the allocation of pins.

GDX Block

The blocks are organized in a “block” (nibble) manner, with each GDX Block providing data flow and control logic for 16 I/O buffers. The data flow is organized as four nibbles, each nibble containing four Multiplexer Register Blocks (MRBs). Data for the MRBs is provided from 64 lines from the GRP. Figure 2 illustrates the groups of signals going into and out of a GDX Block.

Control signals for the MRBs are provided from the Control Array. The Control Array receives the 32 signals from the GRP and generates 16 control signals: eight MUX Select, four Clock/Clock Enable, two Set/Reset and two Output Enable. Each nibble is controlled via two MUX select signals. The remaining control signals go to all the MRBs.

Besides the control signals from the Control Array, the following global signals are available to the MRBs in each GDX Block: four Clock/Clock Enable, one reset/preset, one power-on reset, two of four MUX select (two of two in 64 I/O), four Output Enable (two in 64 I/O) and Test Out Enable (TOE).

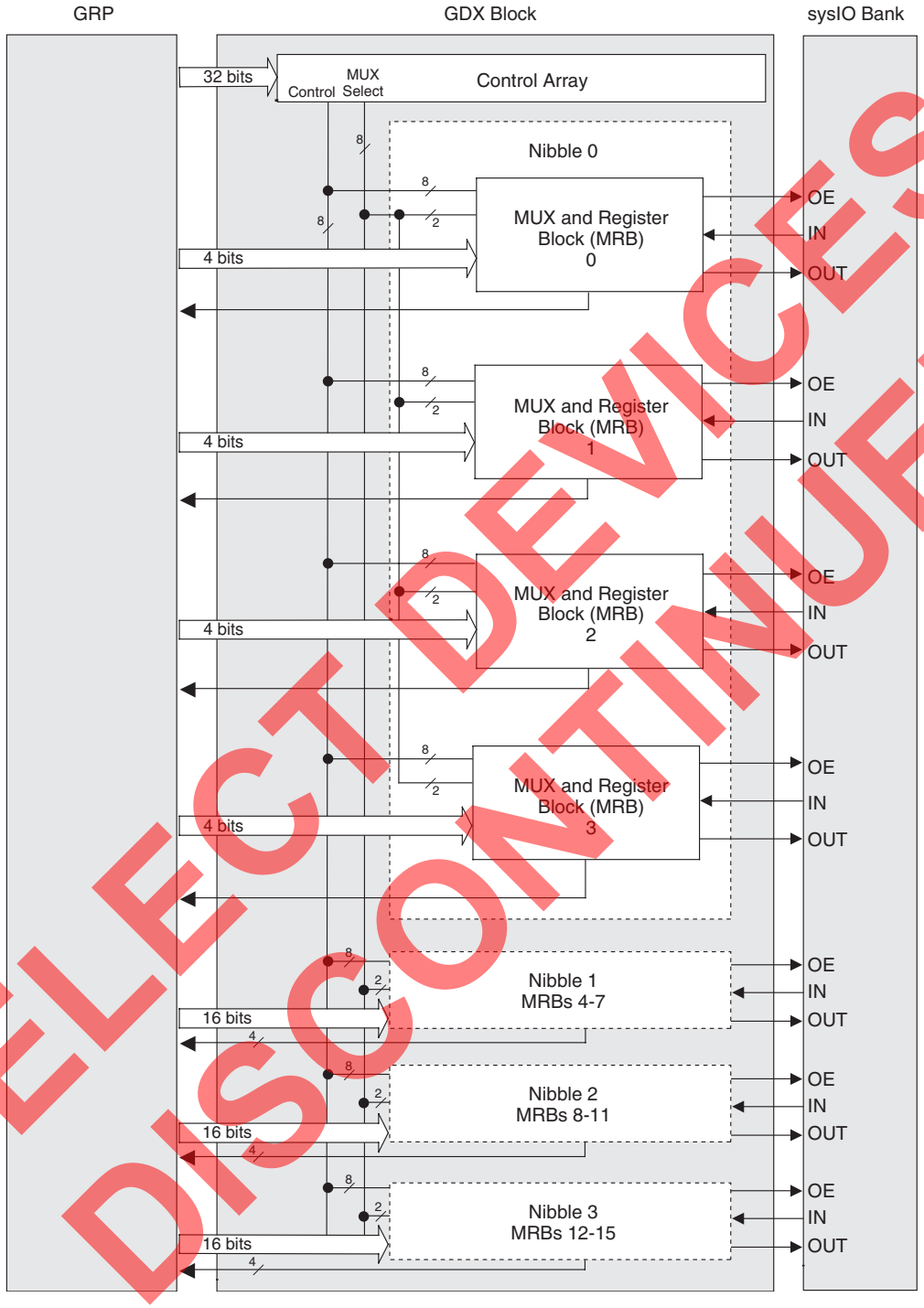
MUX and Register Block (MRB)

Every MRB Block has a 4:1 MUX (I/O MUX) and a set of three registers which are connected to the I/O buffers, FIFO and sysHSI Blocks. Multiple MRBs can be combined to form large multiplexers as described below. Figure 3 shows the structure of the MRB.

Each of the three registers in the MRB can be configured as edge-triggered D-type flip-flop or as a level sensitive latch. One register operates on the input data, the other output data and the last register synchronizes the output enable function. The input and output data signals can bypass each of their registers. The polarity of the data out and output enable signals can be selected.

The Output and OE register share the same clock and clock enable signals. The Input register has a separate clock and clock enable. The initialization signals of each register can be independently configured as Set or Reset. These registers have programmable polarity control for Clock, Clock Enable and Set/Reset. The output enable register input can be set either by one of the two output enables generated locally from the Control Array or from one of the four (two in 64 I/O) Global OE enable pins. In addition to the local clock and clock enable signals, each MRB has access to Global Clock, Clock Enable, Reset and TOE nets.

Figure 2. GDX Block



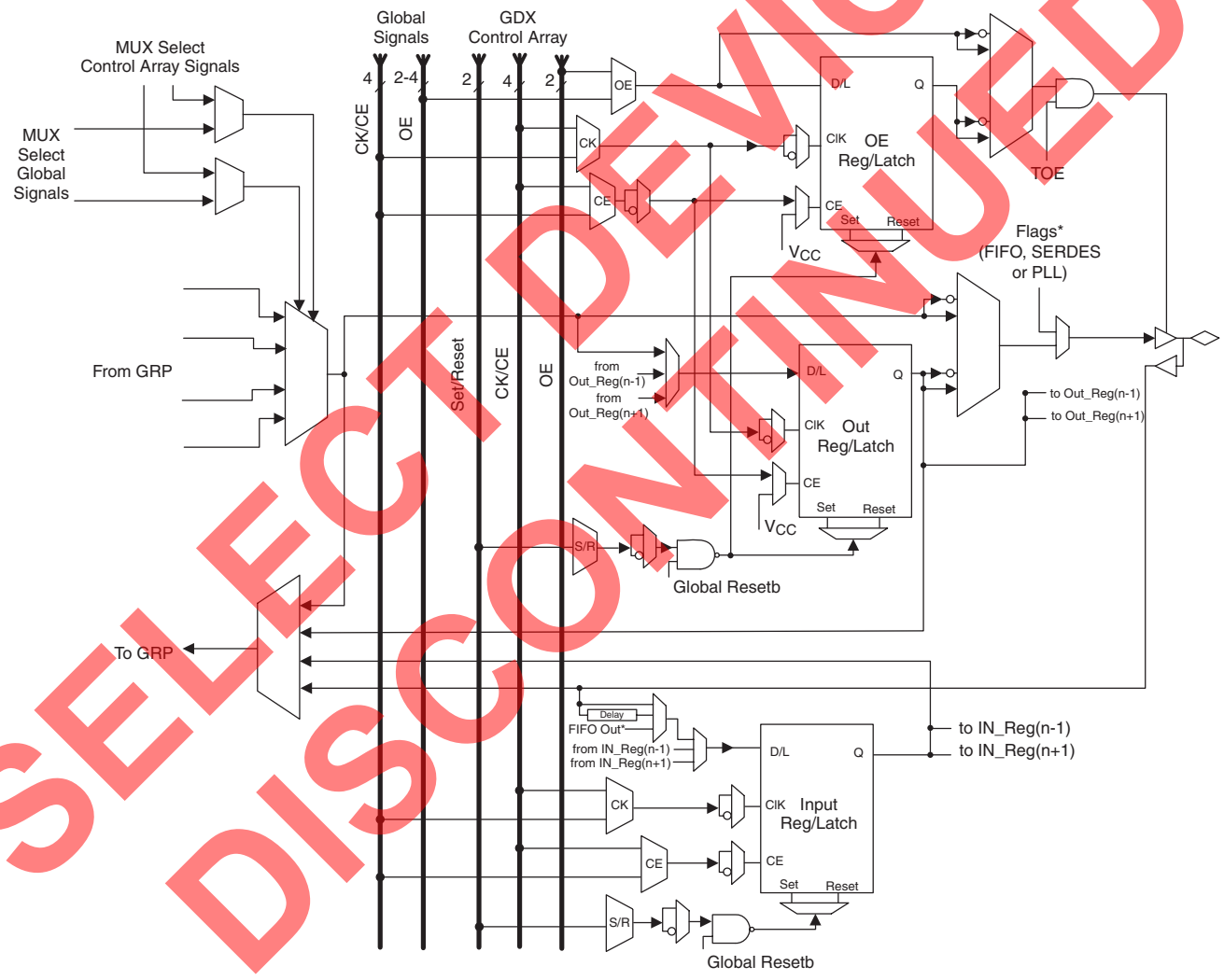
The output register of the MRB has a built-in bi-directional shift register capability. Each output register corresponding to MRB "n", receives data output from its two adjacent MRBs, MRB (n-1) and MRB (n+1), to provide shift register capability. Like the output register, each input register of the MRB has built-in shift register capability. Each input register can receive data from its two adjacent MRB input registers, to provide bi-directional shift register capability. The chaining crosses GDX Block boundaries. The chain of input registers and the chain of output registers can be combined as one shift register via the GRP.

The four data inputs to the 4:1 MUX come from the GRP. The output of this MUX connects to the output register. A fast feedback path from the MUX to the GRP allows wider MUXes to be built. Table 2 summarizes the various MUX sizes and delay levels.

Table 2. MUX Size Versus Internal Delay

MUX Sizes	Levels of Internal GRP Delays
4:1	One Level
Up to 16:1	Two Levels
Up to 64:1	Three Levels
Up to 188:1 (with ispGDX2-256)	Four Levels

Figure 3. ispGDX2 Family MRB

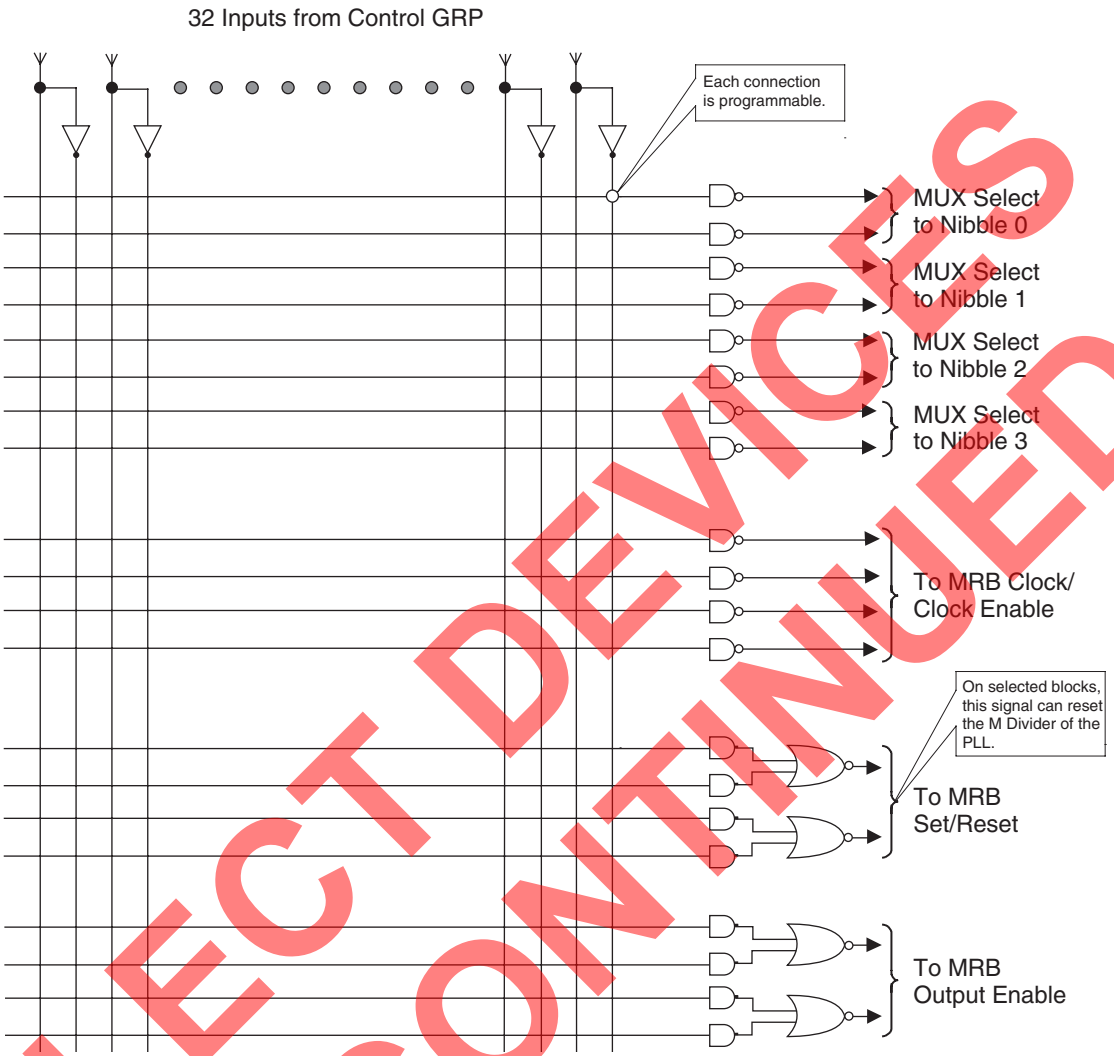


*Selected MRBs see Logic Signal Connection Table for details

Control Array

The control array generates control signals for the 16 MRBs within a GDX Block. The true and complement forms of 32 inputs from the GRP are available in the control array. The 20 NAND terms can use any or all of these inputs to form the control array outputs. Two AND terms are combined with a NOR term to form Set/Reset and OE signals. Figure 4 illustrates the control array.

Figure 4. ispGDX2 Family Control Array

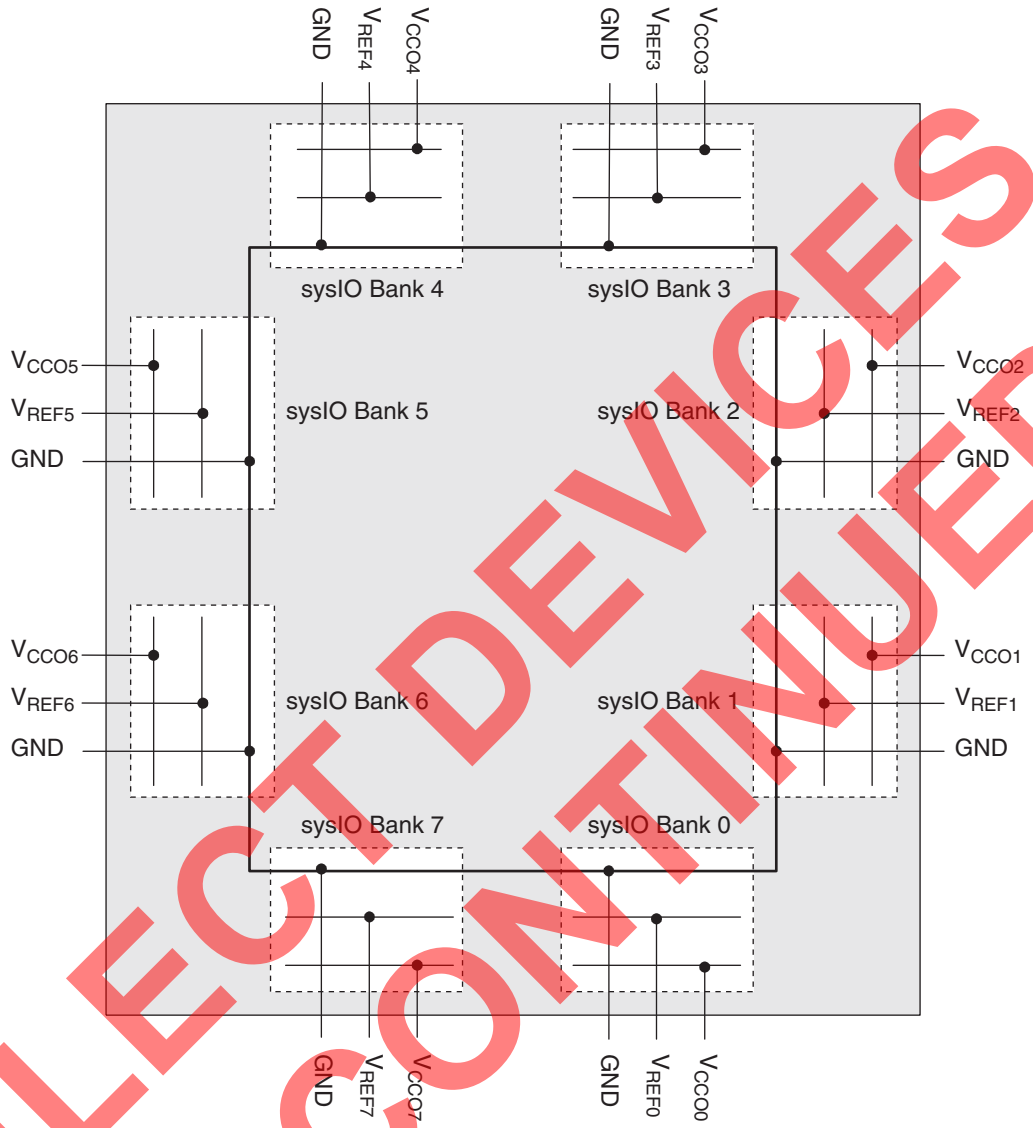


sysIO Banks

The inputs and outputs of ispGDX2 devices are divided into eight sysIO banks, where each bank is capable of supporting different I/O standards. The number of I/Os per bank is 32, 16 and 8 for the 256-, 128- and 64-I/O devices respectively. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}), allowing each bank complete independence from the other banks. Each I/O within a bank can be individually configured to any standard consistent with the V_{CCO} and V_{REF} settings. Figure 5 shows the I/O banks for the ispGDX2-256 device.

The I/O of the ispGDX2 devices contain a programmable strength and slew rate tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. These programmable capabilities allow the support of a wide range of I/O standards.

Figure 5. ispGDX2-256 sysIO Banks



There are three classes of I/O interface standards implemented in the ispGDX2 devices. The first is the non-terminated, single-ended interface; it includes the 3.3V LVTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. The slew rate and strength of these output buffers can be controlled individually. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this interface type. The second interface class implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Use of these I/O interfaces requires an additional V_{REF} signal. At the system level, a termination voltage, V_{TT}, is also required. Typically, an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving. The final types of interfaces implemented are the differential standards LVPECL, LVDS and Bus LVDS. Table 3 shows the I/O standards supported by the ispGDX2 devices along with nominal V_{CCO}, V_{REF} and V_{TT}.

The ispGDX2 family also features 5V tolerant I/O. I/O banks with V_{CCO} = 3.3V may have inputs driven to a maximum of 5.5V for easy interfacing with legacy systems. Up to 64 I/O pins per device may be driven by 5V inputs.

Table 3. ispGDX2 Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVCMOS 3.3	3.3V	—	—
LVCMOS 2.5	2.5V	—	—
LVCMOS 1.8	1.8V	—	—
LVTTL	3.3V	—	—
PCI 3.3	3.3V	—	—
PCI -X	3.3V	—	—
AGP-1X	3.3V	—	—
SSTL3 class I & II	3.3V	1.5V	1.5V
SSTL2 class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL class I	1.5V	0.75V	0.75V
HSTL class III	1.5V	0.9V	0.75V
HSTL class IV	1.5V	0.9V	1.5V
GTL+	1.8/2.5/3.3V	1.0V	1.5V
LVPECL[1, 2, 3]	3.3V	—	—
LVDS	2.5/3.3V	—	—
Bus-LVDS	2.5/3.3V	—	—

1. LVPECL drivers require three resistor pack (see Figure 17).
2. Depending on the driving LVPECL output specification, GDX2 LVPECL input driver may require terminating resistors.
3. For additional information on LVPECL refer to Lattice technical note number TN1000, *sysIO Design and Usage Guidelines.*

The dedicated inputs support a subset of the sysIO standards indicated in Table 4. These inputs are associated with a bank consistent with their location.

Table 4. I/O Standards Supported by Dedicated Inputs

	LVCMOS	LVDS	All other ASIC I/Os
Global OE Pins	Yes	No	Yes[2]
Global MUX Select Pins	Yes	No	Yes[2]
Resetb	Yes	No	Yes[2]
Global Clock/Clock Enables	Yes	Yes	Yes[2]
ispJTAG™ Port	Yes[1]	No	No
TOE	Yes	No	No

1. LVCMOS as defined by the V_{CCJ} pin voltage.
2. No PCI clamp.

For more information on the sysIO capability, please refer to Lattice technical note number TN1000, *sysIO Design and Usage Guidelines.*

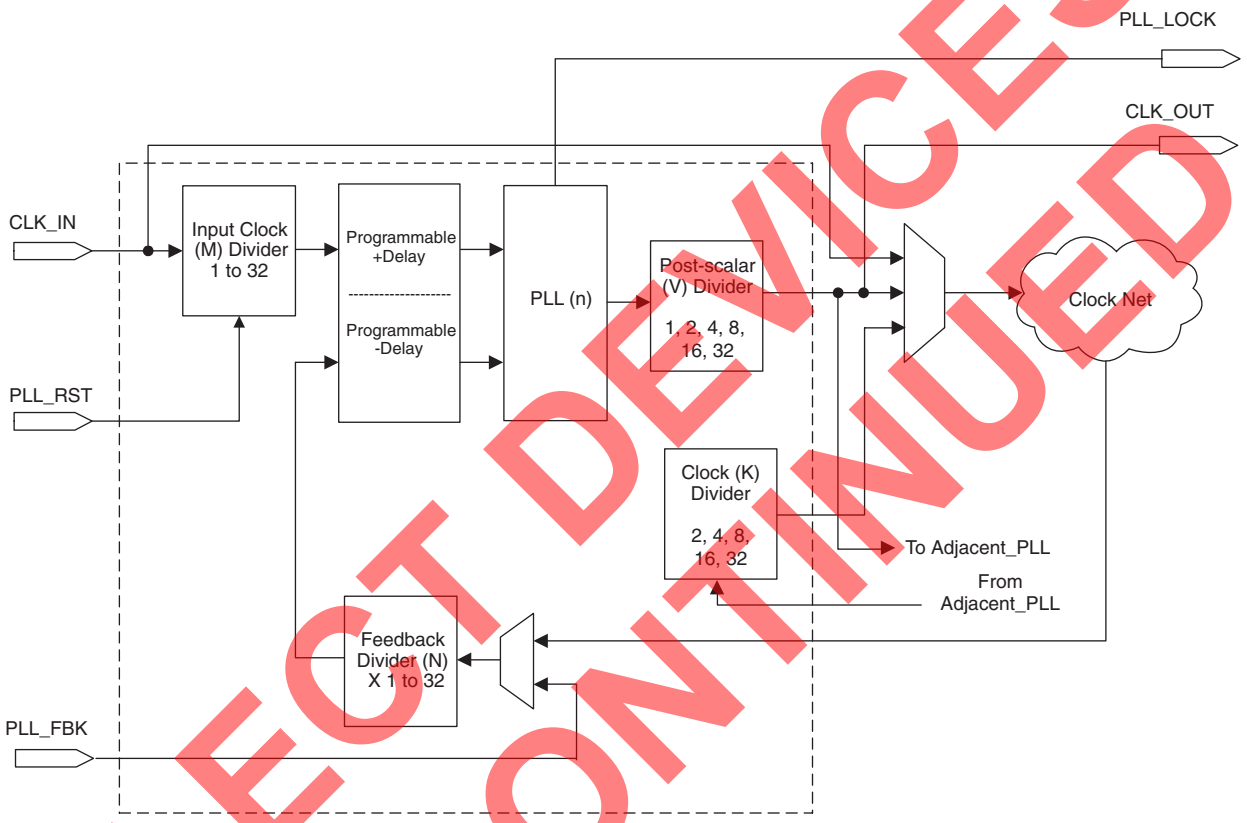
sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) along the various dividers and reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level. Figure 6 shows the ispGDX2 PLL block diagram.

Each PLL has a set of PLL_RST, PLL_FBK and PLL_LOCK signals. In order to facilitate the multiply and divide capabilities of the PLL, each PLL has associated dividers. The M divider is used to divide the clock signal, while the

N divider is used to multiply the clock signal. The K divider is used to provide a divided clock frequency of the adjacent PLL. This output can be routed to the global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to Lattice technical note number TN1003, *sysCLOCK PLL Design and Usage Guidelines*.

Figure 6. sysCLOCK PLL

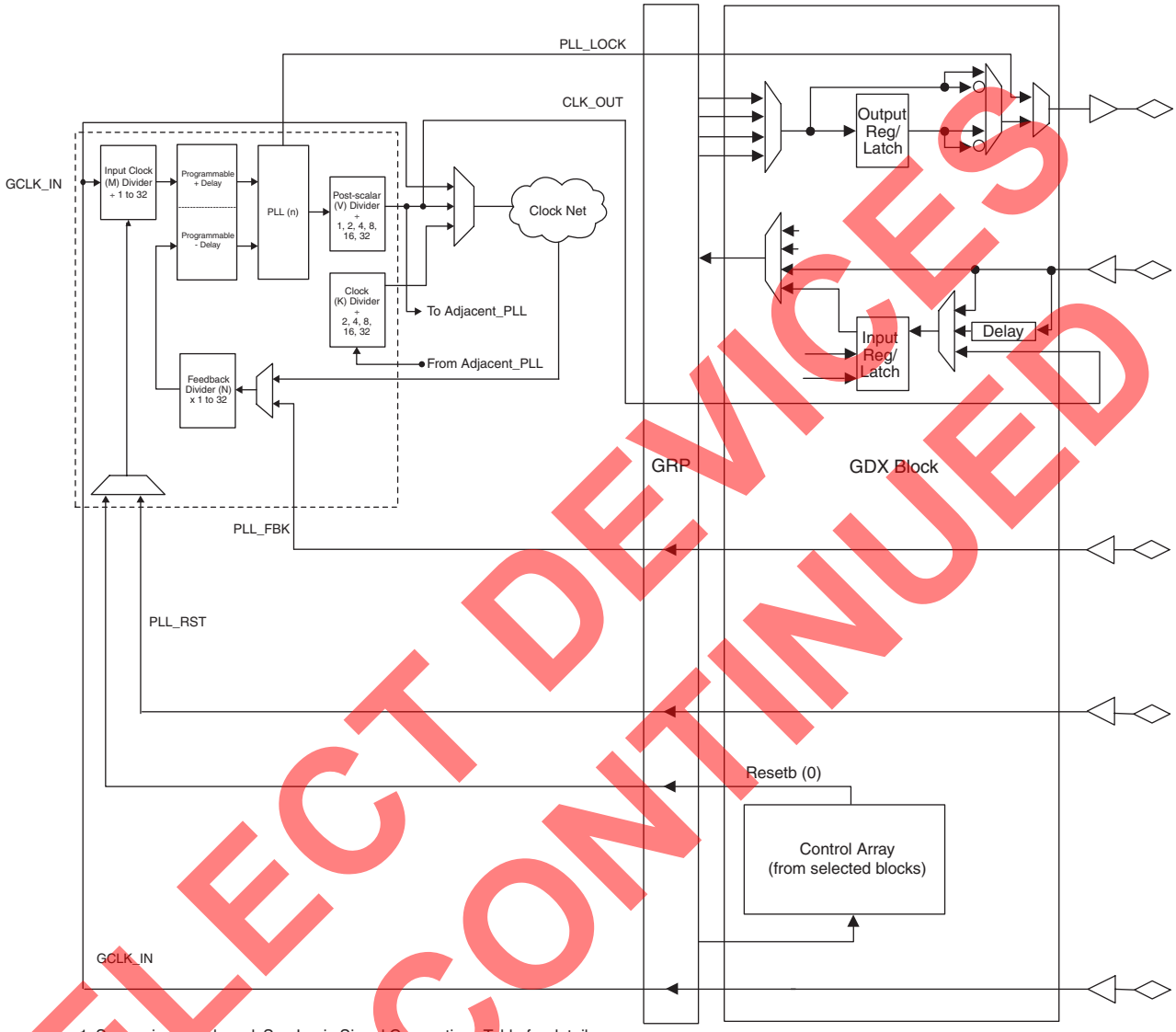


There are four global clock networks routed to each MRB block. These global clocks, CLK0-3, can either be generated by the PLL circuits or supplied externally. External clock pins can be configured as single-ended or differential (LVDS) input. Figure 7 illustrates how the sysCLOCK PLL inputs and outputs can be routed to the I/O pins or general routing. Figure 10 shows the clock network for the ispGDX2-256 and Figure 8 shows the clock networks for ispGDX2-128 and ispGDX2-64. The Reset (0) pin from the Control Array of selected GDX Blocks can be programmed to reset the M Divider of the PLLs. This provides a means for generating the reset signal internally. Table 5 details which GDX Block provides reset to the PLLs.

Table 5. Internal Reset Input of the PLL (M Divider)

	PLL0	PLL1	PLL2	PLL3
ispGDX2-256	GDX Block 5A	GDX Block 7B	GDX Block 1A	GDX Block 3B
ispGDX2-128	GDX Block 2A	—	GDX Block 0A	—
ispGDX2-64	GDX Block 0A	—	GDX Block 1B	—

Figure 7. I/O Pin Connection to the sysCLOCK PLL[1]



1. Some pins are shared. See Logic Signal Connections Table for details.

Figure 8. ispGDX2-64 CLOCK Network

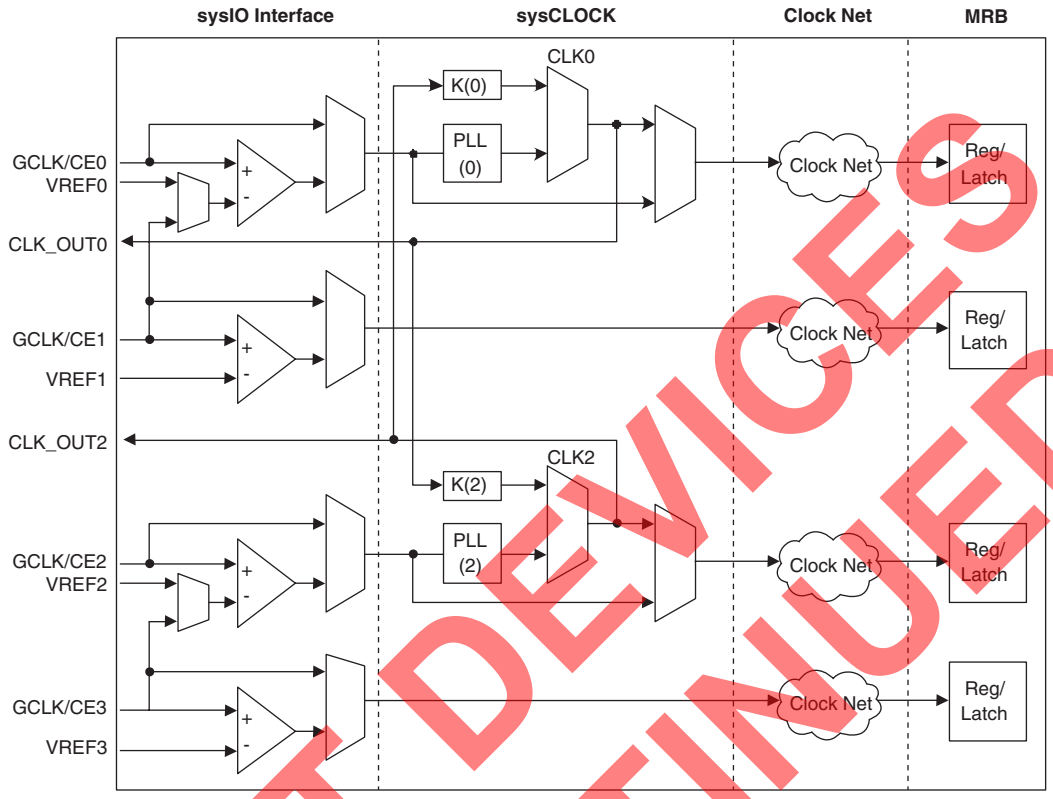


Figure 9. ispGDX2-128 CLOCK Network

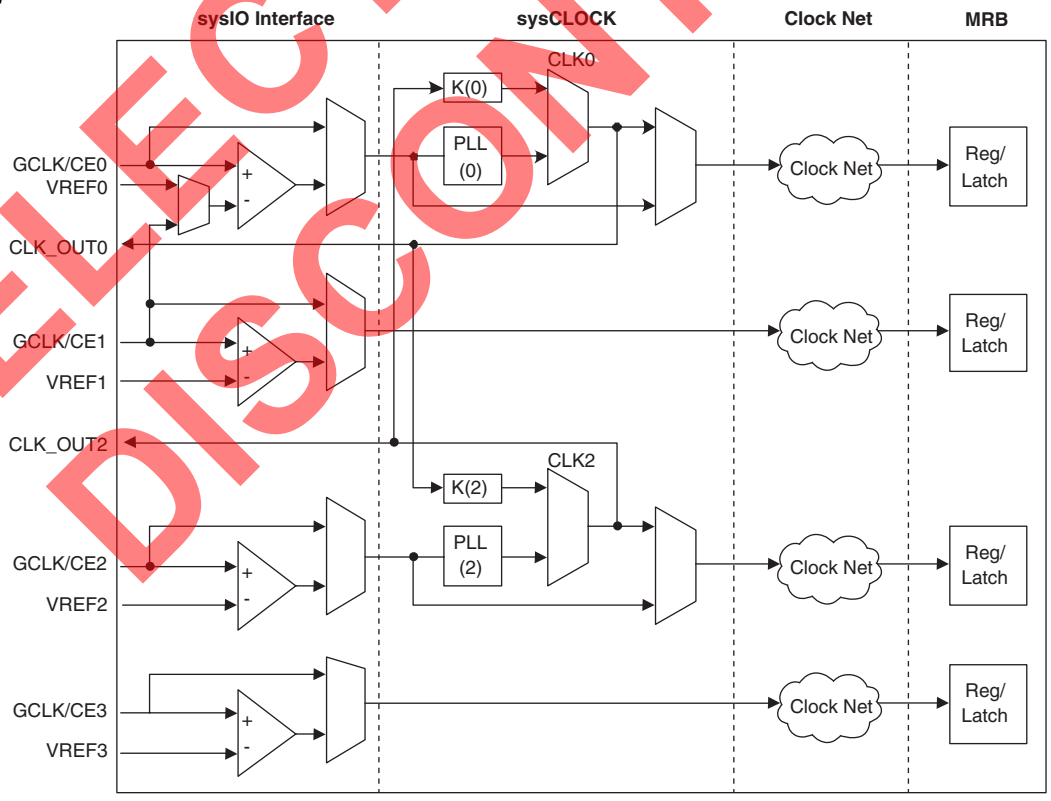
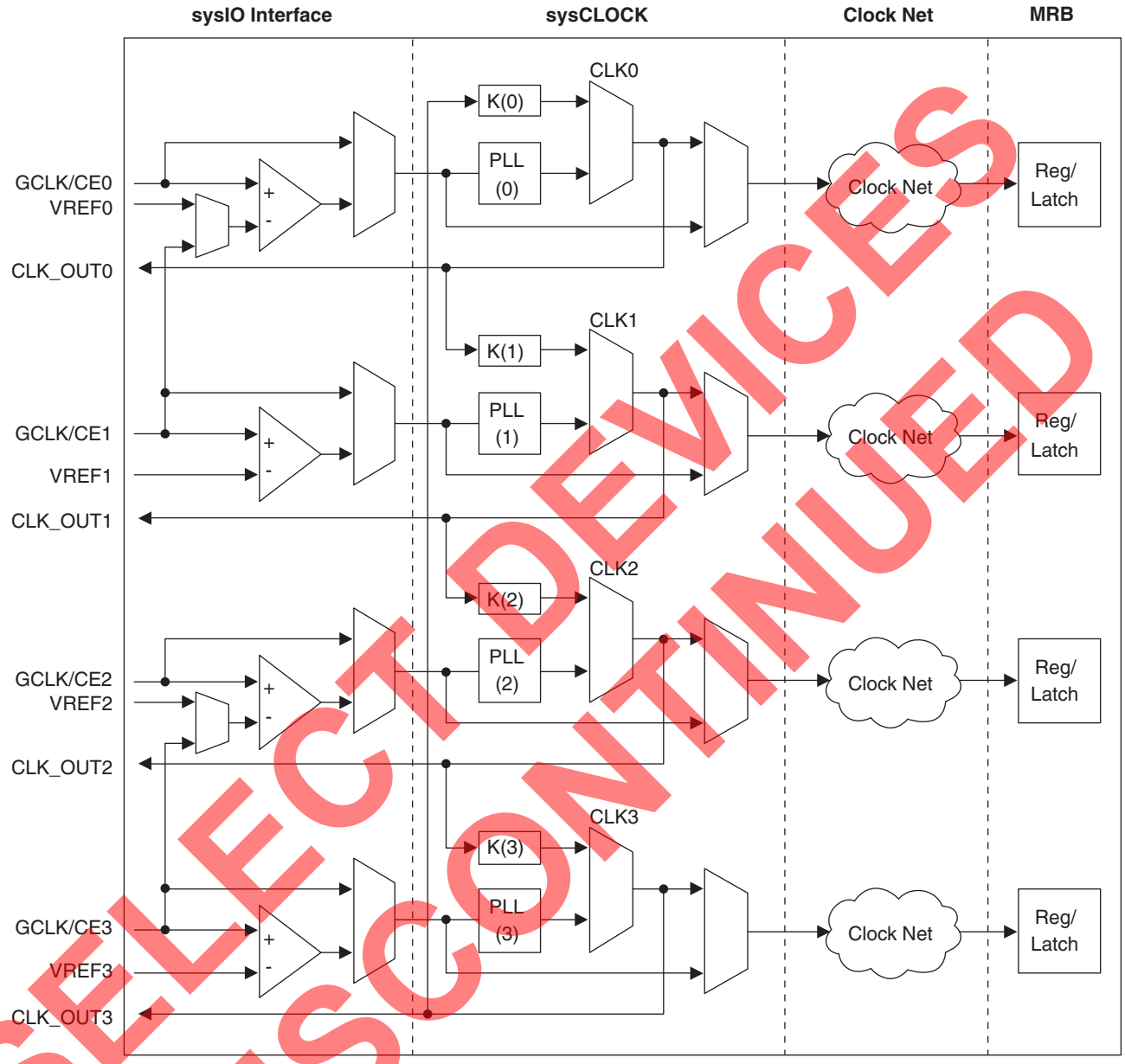


Figure 10. ispGDX2-256 CLOCK Network

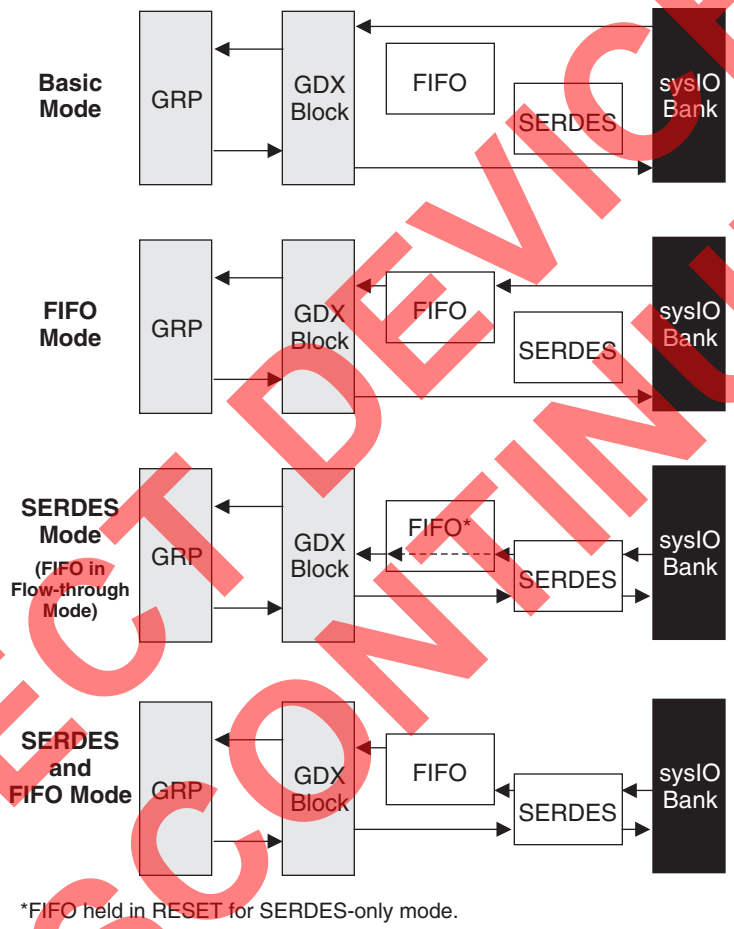


Operating Modes

All the GDX Blocks in the ispGDX2 family can be programmed in four modes: Basic, FIFO only, SERDES only, and FIFO with SERDES mode. In basic mode, the SERDES and FIFO are disabled and the MUX output of the MRB connects to the output register. Inputs are connected to the GRP via the MRB.

Figure 11 shows the four different operating modes. Precise detail of the FIFO and SERDES connections is provided in their respective sections.

Figure 11. Four Operating Modes of ispGDX2 Devices

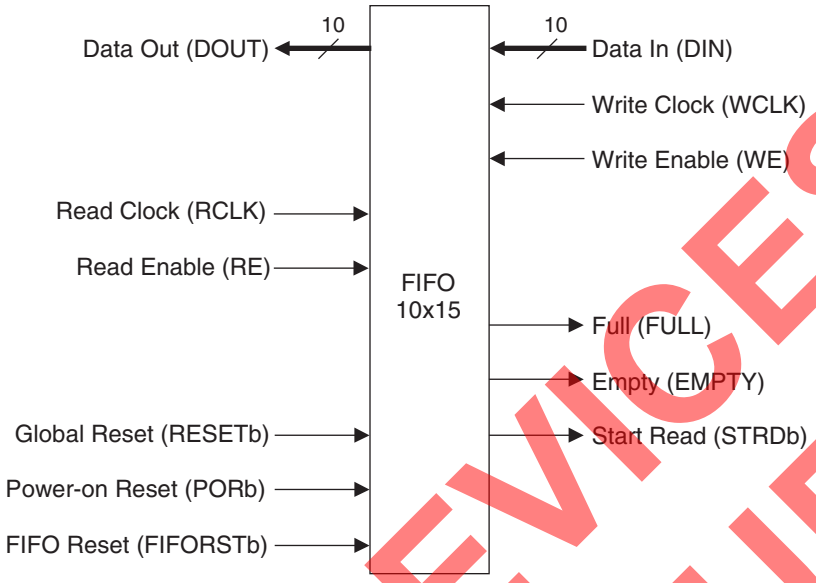


*FIFO held in RESET for SERDES-only mode.

FIFO Operations

Each GDX Block is associated with a 10-bit wide and 15-word deep (10x15) RAM. This RAM, combined with two address counters and two comparators, is used to implement a FIFO as a “circular queue”. The FIFO has separate clocks, the Read Clock (RCLK) and Write Clock (WCLK), for asynchronous operation. The FIFO has three additional control signals Write Enable, Read Enable and FIFO Reset. Three flags show the status of the FIFO: Empty, Full and Start Read. Each FIFO receives the global Power-on Reset and Reset signals. Figure 12 shows the connections to the FIFO.

Figure 12. ispGDX2 FIFO Signals

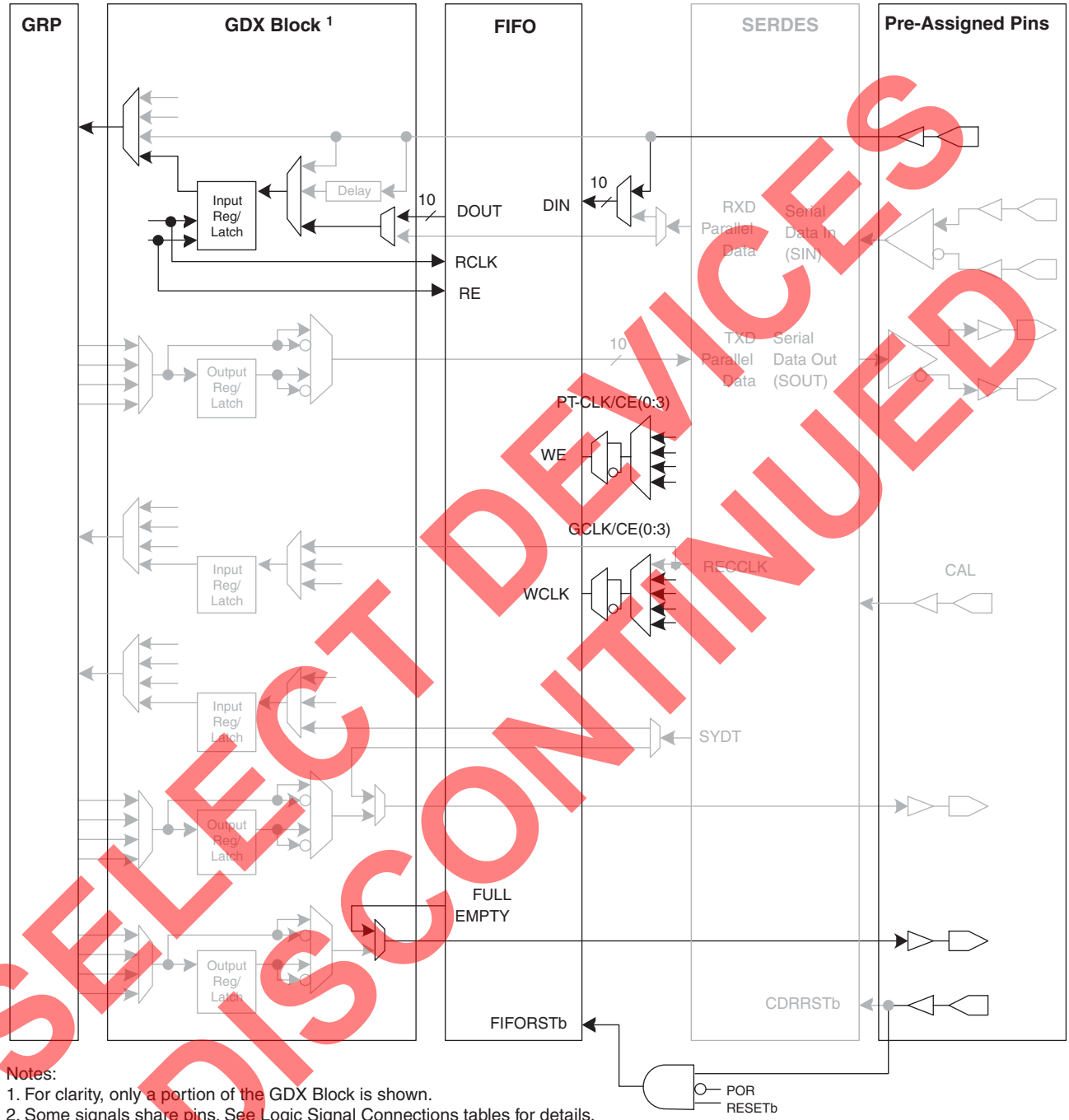


Read Clock and Read Enable are the same as the Clock and Clock Enable signals of the input registers of the associated MRB. These registers are used to register the FIFO outputs, and in modes that utilize the FIFO are configured to use the same clock and clock enable signals. The Write Clock is selected from one of the GCLK/CE signals or the RECCLK (Recovered Clock) signal from the associated SERDES. The Write Enable is selected from one of the local MRB product term CLK/CE signals. All FIFO operations occur on the rising edge of the clock although clock polarity of these signals can be programmed.

The flags from the FIFO, FULL, EMPTY and STRDb (Start Read) are each fed via a MUX in the MRB to an I/O buffer. The STRDb (half full) signal is used in conjunction with SERDES. STRDb is an active low signal, the signal is inactive (high) on FIFO RESET. After the FIFO reset when the FIFO contains data in five memory locations, at the following write clock transition the STRDb becomes active (low). Note, if the Read Clocks arrive before writing the sixth location, it may take longer than five write clocks before the STRDb becomes active. When the FIFO has data in the first six locations, at the next write clock transition the STRDb becomes inactive (high). Again, if the Read Clocks arrive before writing the seventh location, the STRDb may stay active for longer than one write clock period, even if the FIFO contains data in less than five locations. After this event, the STRDb stays inactive until the FIFO is RESET again. STRDb does not become active again even if less than six memory locations are occupied in the FIFO. It is the user's responsibility to monitor the FULL and EMPTY signals to avoid data underflow/overflow and to take appropriate actions.

Figure 13 shows how the FIFO is connected between the I/O banks and the GDX Blocks in FIFO mode. For more information on the FIFO, please refer to Lattice technical note number TN1020, *sysHSI Usage Guidelines*.

Figure 13. Operation in FIFO Mode[2]



Notes:
1. For clarity, only a portion of the GDX Block is shown.
2. Some signals share pins. See Logic Signal Connections tables for details.

High Speed Serial Interface Block (sysHSI Block)[1]

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispGDX2 devices have multiple sysHSI Blocks.

Each sysHSI Block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in a given sysHSI Block share a common clock and must operate at the same nominal frequency. Figure 14 shows the sysHSI Block.

Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI application notes). The encoding and decoding of the 10B/12B standard are performed within the device in dedicated logic. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the device.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, the SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

Additionally, multiple sysHSI Blocks can be grouped together to form a source synchronous interface of between 1-8 channels.

Figure 15 shows the connections of the SERDES block with the FIFO, sysIO block and the MRB. Table 6 provides the descriptions of the SERDES.

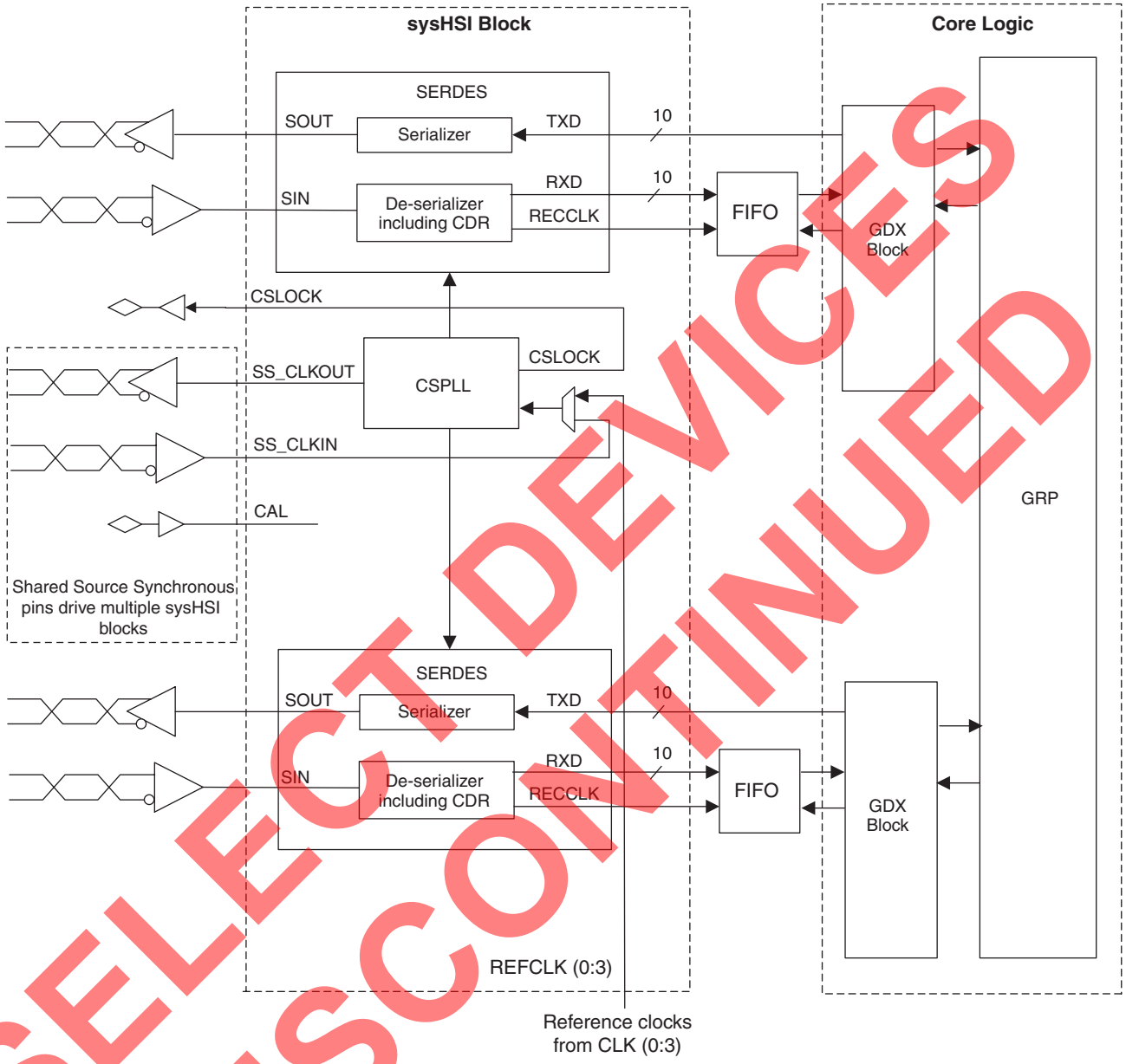
For more information on the SERDES/CDR, refer to Lattice technical note number TN1020, *sysHSI Usage Guidelines*.

Table 6. SERDES Signal Descriptions

Signal	I/O	Description
CDRRSTb	I	Resets the CDR circuit of sysHSI block
SYDT	O	Symbol alignment detect for sysHSI block
CAL	I	Initiates source synchronous calibration sequence
RXD	Internal	Parallel data in for sysHSI block
TXD	Internal	Parallel data out for sysHSI block
REFCLK	Internal	Reference clock received from the clock tree
SIN	I	Serial data input for sysHSI block (LVDS input)
SOUT	O	Serial data output for sysHSI block (LVDS output)
SS_CLKIN	I	Clock input for source synchronous group
SS_CLKOUT	O	Clock output for source synchronous group
RECCLK	Internal	Recovered clock from encoded data by CDR of sysHSI block
CSLOCK	Internal	Lock output of the PLL associated with sysHSI block

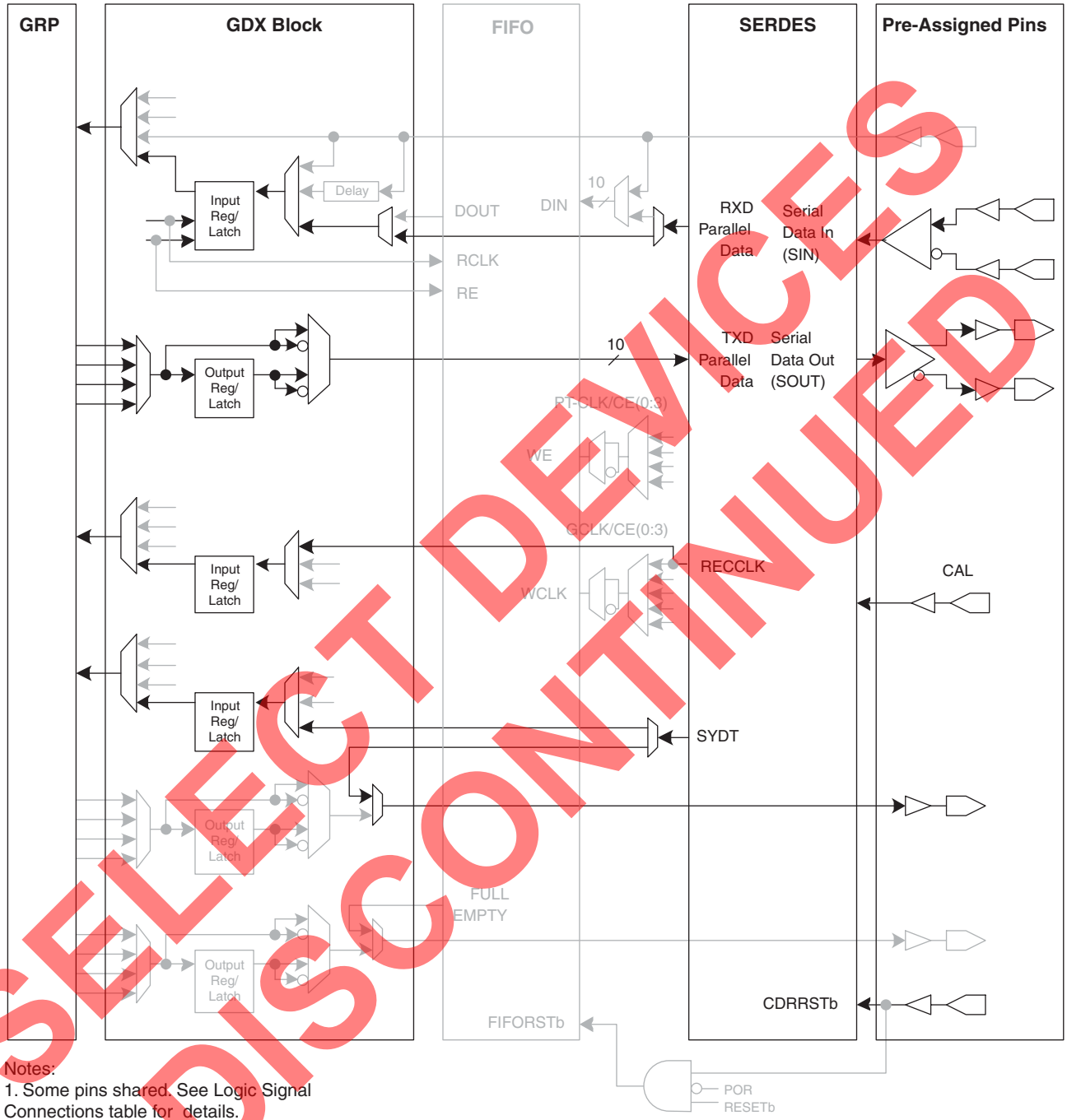
1. "E-Series" does not support sysHSI.

Figure 14. sysHSI Block with SERDES and FIFO



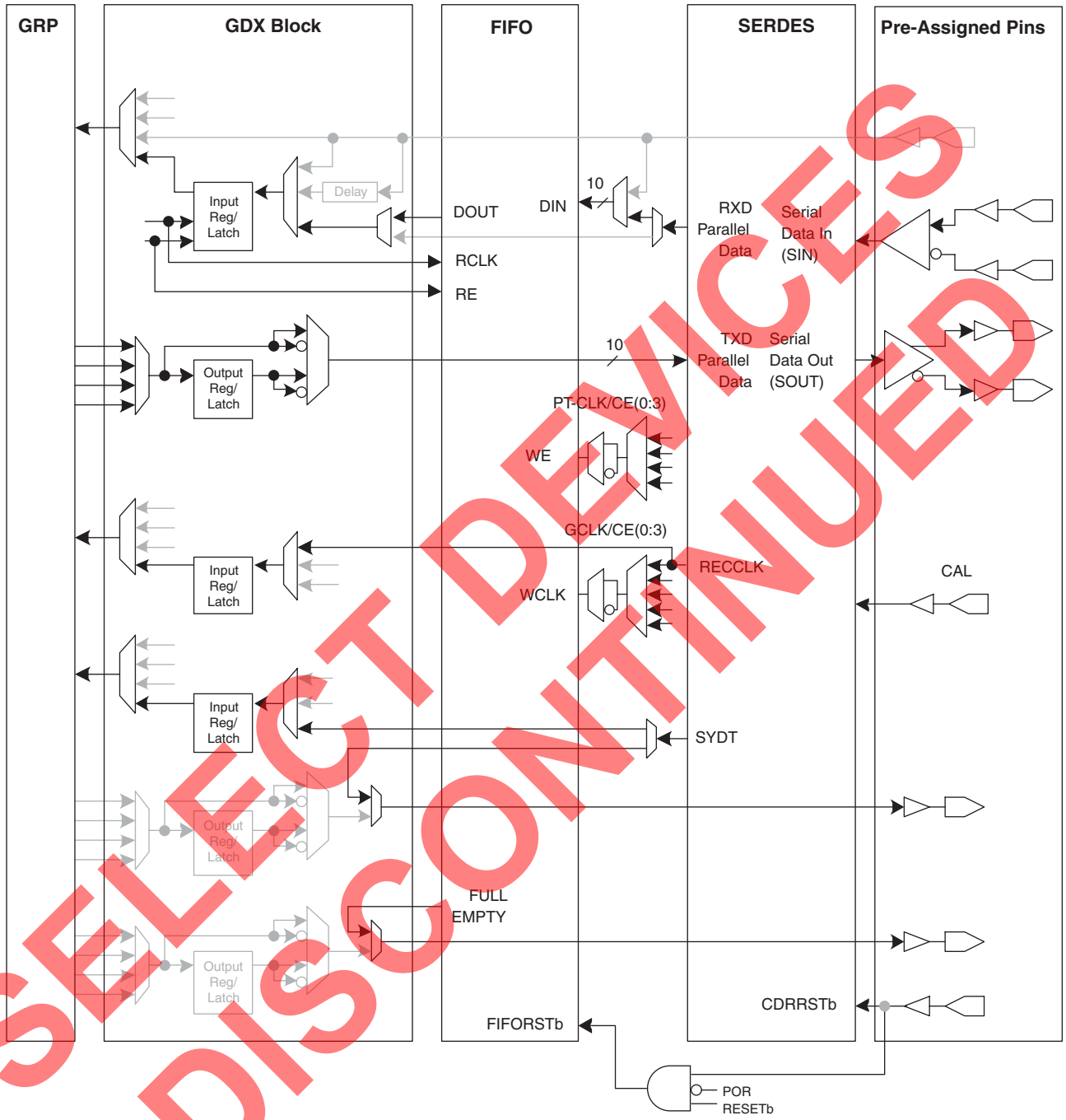
Note: Some pins are shared. See Logic Signal Connections table for details

Figure 15. Operation in SERDES Only Mode[1, 2]



Notes:
1. Some pins shared. See Logic Signal Connections table for details.
2. For SERDES only mode programmable bit holds FIFO in reset. Input registers used for DOUT, and RECCLK configured as latches and held in pass through.

Figure 16. Operation in SERDES with FIFO Mode



IEEE 1149.1-Compliant Boundary Scan Testability

All ispGDX2 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port has its own supply voltage that can operate with LVCMOS3.3, 2.5 and 1.8 standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispGDX2 family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispGDX2 devices provide In-System Programming (ISP) capability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, designers get the benefit of a standard, well defined interface.

The ispGDX2 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispGDX2 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispGDX2 devices during the testing of a circuit board.

Security Scheme

A programmable security scheme is provided on the ispGDX2 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this scheme prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security scheme also prevents programming and verification. The entire device must be erased in order to reset the security scheme.

Hot Socketing

The ispGDX2 devices are well suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Absolute Maximum Ratings [1, 2, 3]

	ispGDX2C (1.8V)	ispGDX2B/V (2.5/3.3V)
Supply Voltage V_{CC}	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage V_{CCP}	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage V_{CCO}	-0.5 to 4.5V	-0.5 to 4.5V
JTAG Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied [4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temp. (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX)+2) volts is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices[1]	1.65	1.95	V
	Supply Voltage for 2.5V Devices	2.3	2.7	V
	Supply Voltage for 3.3V Devices	3	3.6	V
V_{CCP}	Supply Voltage for PLL and sysHSI Blocks, 1.8V Devices[1]	1.65	1.95	V
	Supply Voltage for PLL and sysHSI Blocks, 2.5V Devices	2.3	2.7	V
	Supply Voltage for PLL and sysHSI Blocks, 3.3V Devices	3	3.6	V
V_{CCJ}	Power Supply Voltage for JTAG Programming 1.8V Operation	1.65	1.95	V
	Power Supply Voltage for JTAG Programming 2.5V Operation	2.3	2.7	V
	Power Supply Voltage for JTAG Programming 3.3V Operation	3	3.6	V
T_J (COM)	Junction Commercial Operation	0	90	°C
T_J (IND)	Junction Industrial Operation	-40	105	°C

1. sysHSI specification is valid for V_{CC} and V_{CCP} = 1.7V to 1.9V.

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Specifications [1, 2, 3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}[4]	Input or Tristated I/O Leakage Current	0 ≤ V_{IN} ≤ 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. LVTTL, LVCMOS only.
3. 0 < V_{CC} ≤ V_{CC} (MAX), 0 < V_{CCO} ≤ V_{CCO} (MAX).
4. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.